DESIGN AND VERIFICATION OF nMOSFET FOR LOW LEAKAGE AT 90nm PROCESS TECHNOLOGY

Submitted in the partial fulfillment of requirement for the award of the Degree of

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND CAD

Submitted by
Parul Trivedi
Roll No. 600961016

Under guidance of
Mr. Arun Kumar Chatterjee
Assistant Professor, ECED
T.U., Patiala.

Electronics and Communication Engineering Department
Thapar University, Patiala-147004, India

July, 2011.

CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled" DESIGN AND VERIFICATION OF nMOSFET FOR LOW LEAKAGE AT 90nm PROCESS TECHNOLOGY" in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design and CAD at the Electronics and Communication Engineering Department of Thapar University Patiala, is an authentic record of my own work carried out under the supervision of Mr. Arun Kumar Chatterjee , Assistant Professor, ECED, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other University for the award of Degree.

Date 12-07-2011

Parul Trivedi

600961016

It is certify that the above statement made by student is correct with the best of my knowledge and belief.

Arun Kumar Chatterjee 12/7/11

Mr. Arun Kumar Chatterjee

Assistant Professor

ECED, Thapar University, Patiala.

Counter signed by

Prof. A. K. Chatterjee 12.7.11.

HEAD, ECED

Thapar University

Patiala, PUNJAB

Prof. S. K. Mohpatra

Dean of academic Affaris

Thapar University

Patiala, PUNJAB

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(Parul Trivedi)

ABSTRACT

Leakage is a big challenge in planar bulk IGFET at sub-100nm technologies. The research is focused on the development of sub-100nm technology nMOSFET. Simulation of the process is carried out using Silvaco TCAD tool in Athena Atlas framework to modify physical values and obtain more accurate process parameters. Several type of leakage in a short channel MOSFET has been investigated. The most common leakage that generally occurs at sub-100nm technology MOSFETs is subthreshold leakage and gate tunneling.

Several advanced method such as lightly-doped drain (LDD), halo implant and retrograde well have been applied to reduce the short channel effects. By device simulation the electrical characteristics have been obtained and further investigated. Several design analysis are performed to investigate the effectiveness of the advanced method in order to prevent the variation of threshold voltage and short channel effect of a MOSFET device.

Leakage reduction from 1.9×10^{-9} A to 4.36×10^{-12} A by using halo doping and retrograde well doping has been achieved.

Further the MOSFET designed has been incorporated in an inverter circuit and simulated with the help of MIXEDMODE of Silvaco. The results obtained have been compared with the simulation results of same circuit on T-SPICE of Tanner by using 90nm BSIM model. It has been obtained that the designed MOSFET is faster than BSIM model by 60%.

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CHAPTER 1
INTRODUCTION

J.E Lilienfield about 80 years ago patented the first ever field effect transistor concept, named "Method and Apparatus for Controlling Electric Currents" which evolved into the modern metal oxide semiconductor field effect transistor (MOSFET). Lilienfield proposed a three terminal device where the source to drain current is controlled by a field effect from the gate and is dielectrically insulated from the device. The active part of the device was built on a thin semiconductor film deposited on an insulator.

The first working MOSFET was discovered in 1960. The MOSFET continues to lead the industry thereafter. The complementary MOSFET, CMOS technology is currently the driving technology and have the largest market share among all kinds of transistors.

According to Moore's law, Sir Gordon Moore predict that the number of transistor is going in the trend of doubling every two years. Thus with increasing numbers of transistor in a chip each transistor size is decreasing geometrically, leading to improved performance. In order to continue Moore's law aggressive scaling in the last few years to enter into the nanometer range various secondary effects such as threshold voltage variation, drain induced barrier lowering, sub-threshold swing, and current leakage comes in to picture. These short channel effects cause large power dissipation and degraded performance of the device. At nanoscale short channel effects are accounted by introducing standard process steps such source/drain doping, halo doping and retrograde well doping in the channel of MOSFET. As the dimension of MOSFET continue to decrease the effect of process induced stress on the device performance become more important then before. Besides scaling, some of the innovative mobility enhancement techniques are used to improve CMOS performance.

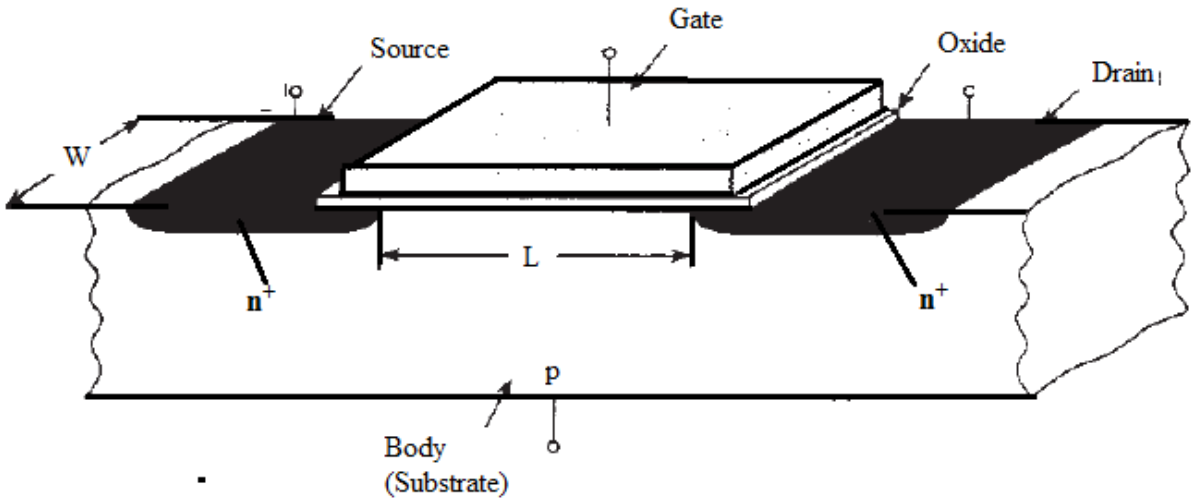

Fig.1.1 Cross section View of MOSFET[]

1.1 Need for Low Power:

Operation of vacuum tubes required several hundred volts of anode voltage and few watts power. In comparison the transistor required milliwatts of power. Since the invention of the transistor decades ago, power dissipation is though not entirely ignored, was of a little concern. The greater emphasis was on performance and miniaturization. Application powered by battery pocket calculators, mobile phone. Hearing aids, portable military equipments and wrist watches demands low power electronics. In all the application it is important to prolonged the battery life as much as possible. And now with the portable computing and wireless communication power dissipation has become the most important factor in the continued development of the microelectronics technology.

In recent years, the demand for power sensitive designs has grown significantly due to the fast growth of battery-operated portable applications. As the technology scaling continues unabated, subthreshold device design has gained a lot of attention due to the low-power and ultra-low-power consumption in various applications. Design of low-power high-performance submicron and deep submicron CMOS devices and circuits is a big challenge. Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) has been the major device for integrated circuits over the past two decades. With technology advancement and the high scalability of the device structure, silicon MOSFET-based VLSI circuits have continually delivered performance gain and/or cost reduction to semiconductor chips for data processing and memory functions. Metal-Oxide-

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1.2 Objective:

The main objective of the project is to develop a 90nm n-channel (NMOS) MOSFET for low power application. Many design aspects has to be considered when the MOSFET device is scaled down into deep submicron regime. Short channel effects that will appear whenever the MOSFET device is scaled down and gate oxide has to be thin enough to increase the device performance. There were several advanced fabrication processes is applied to the 0.18μm MOSFET design such as halo implant for the punch-through stopper, light doped drain (LDD) to avoid hot electron and retrograde well to suppress the parasitic bipolar devices (latch up immunity). Therefore, the summary of objectives and aims of this project are:

- To apply 90nm process to fabricate NMOSFET and to study the effects on device performance.
- To study the factors that caused the variation of threshold voltage.
- To study the effectiveness of advanced technique in preventing threshold voltage variation.
- To reduce the short channel effects of a deep-submicron device.

- To be exposed to MOSFET design procedures and would be able to reinforce the understanding of MOSFET devices by participating in the device design process.

1.3 Thesis Organization:

The integration of a new manufacturing process flow has been implemented through the design of 90nm MOSFET device. The remainder of this thesis describes the challenges facing device design in the deep sub-micron region, paying special attention to those that have the most relevance for the rest of this thesis: short channel effects. Device design considerations such as channel, halo and retrograde well doping are then presented.

Chap-2 (literature survey) discussed the fundamental of long and short channel MOSFET, limitations of long channel MOSFET, various type of leakage mechanisms and there reduction techniques.

In chap-3 all the processing steps necessary to design the structure of a NMOS and advanced techniques used have been discussed.

Chap-4 discussed simulation of the nMOS device obtained from the Silvaco TCAD tool in Athena framework. All types of simulation have been done on the device and finally leakage reduction has been discussed, this chapter also discussed about the mixed mode simulator and works done on this to simulate the NMOS.

CHAPTER 2
LITERATURE SURVEY

2.1 MOSFET and Scaling

From past decades, the MOSFET has continually been scaled down in size, typical MOSFET channel lengths were several micrometers, but today's technologies are dealing MOSFETs with channel lengths of the order of nanometer. The problems with decreasing the size of the MOSFET have been related with the semiconductor device fabrication process.

Smaller MOSFETs are desirable three main reasons.

1. Smaller MOSFETs allow more current to pass, because of the low resistance.
2. Smaller MOSFETs have smaller gates, and thus lower gate capacitance.

These two factors provide lower switching times, and thus higher speeds.

3. One more reason is that, smaller MOSFETs can be packed more densely, resulting in chips with more computing power in the same area. Since the cost of chips depends on the number of chips per wafer, that third reason is more important for scaling.

The scaling theory, based on a *constant electric-field*, in which the electric field and shape will remain same, requires V_{dd}, V_t, L, T_{ox} to be scaled down by a fix scaling factor. The doping level in the channel must be scaled up by the same scale factor. The junction depth of source and drain also needs to be scaled down to suppress the short-channel effect. Fig. 2.1 shows the cross section of original and scaled NMOS transistor[1].

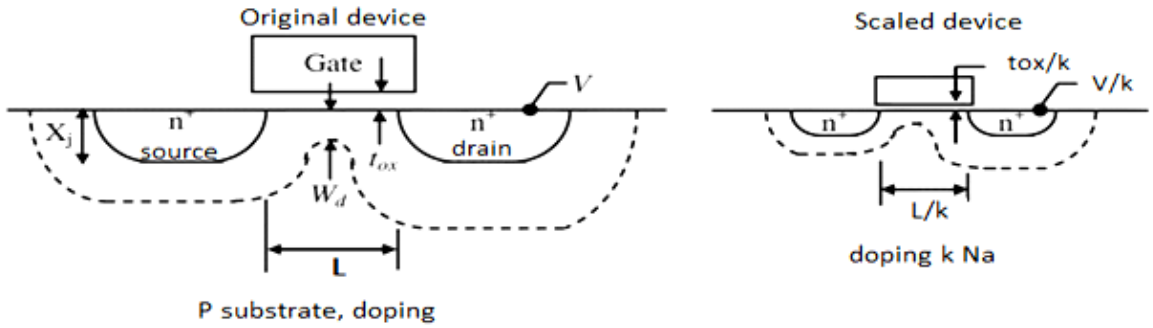


Fig 2.1 constant-electric-field scaling[1]

The constant field scaling presents some problems, as the weak inversion width does not scale and established chip interface requires the voltage levels are fixed, and cannot be scaled. The rules followed in such cases are referred to as *constant voltage scaling*, in which W, L, N_a are scaled by the same factor, but if the T_{ox} is scaled then electric field become too high because the voltage is not scaled making a critical problem mobility degradation.

To avoid extreme cases of constant field and constant voltage scaling compromise scaling rules have been proposed [2]. In which all the factors are not scaled by same factor but some adjustment have been introduced.

2.2 Limitations of the Long Channel Analysis

The channel lengths of the first commercial MOSFETs were more than 20μm. These MOSFETs are modeled by the long-channel theory with its successive approximations and the resulting nonphysical consequences (such as infinite carrier velocities near the drain). The long channel theory says drain currents to increase with increasing drain voltages (when the applied gate voltage is higher than the drain voltage) as mobile electrons in the channel move faster in the increasing field along the channel. According to this theory, sufficiently high drain voltages lead to a "pinch-off" condition, in which the channel mobile-carrier density becomes zero near the drain. The channel current must, however, be constant and therefore the pinch-off condition requires an infinite carrier velocity to maintain a constant current with a vanishing carrier velocity.

2.2.1 Threshold Voltage and Threshold voltage adjust

The Threshold voltage of a uniformly doped and long channel MOS can be expressed by[3]

$$V_{T(\text{uniform doping, long channel})} = \phi_{ms} - (Q_{tot}/C_{ox}) + 2\sqrt{K_{si}\varepsilon_0 q N_{sub}\phi_B}/C_{ox} + 2\phi_B \quad \ldots\ldots(1)$$

where ϕ_{ms}= work function difference between metal-semiconductor

K_{si} = Dielectric constant of Silicon

N_{sub}= Substrate concentration

C_{ox}= Oxide capacitance

Q_{tot}= total charge on oxide

This equation contains of work function difference between gate and semiconductor, ϕ_{ms}, oxide charges and traps, In which mobile ionic charges, fixed oxide charges, interface trapped charges, oxide trapped charges are included.

According to the above equation the only strong candidate to control the V_T is $\sqrt{N_{sub}}$, in a manner that by increasing the substrate doing increase V_T, because all the other terms are only affect the V_T a little bit. The Fig. 2.2 shows the variations of V_T with N_{sub} no adjustment implant were used.

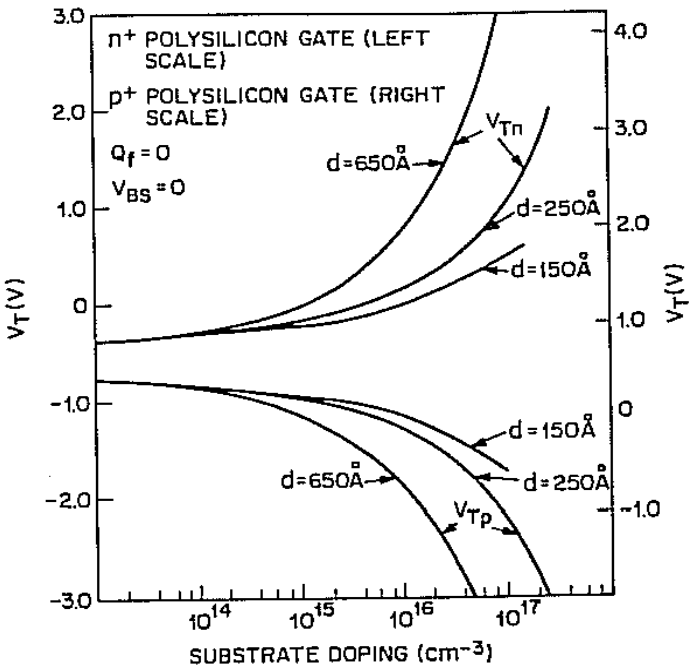


Fig. 2.2 V_t of n-MOS & p-MOS with N_{sub} for different T_{ox} [3]

The development of V_T-adjustment removed the last obstacle to reliable production of n-channel devices for MOS ICs. That is implantation can be used either increase or decrease the net dopant concentration near the surface and V_t can now be set by the V_t-adjustment implant process. [3]

As mentioned earlier, the V_t-adjustment implant techniques involve the implantation of Boron, Phosphorous or Arsenic ions in to the regions under the gate oxide of MOSFET. Boron implantation produces the positive shift in V_t while Arsenic and Phosphorous produce negative shift [3].

To first order, if the implant and substrate are of the same type, and effective depth of implant X_j is less then d_{max}, the threshold voltage shift can be well estimated by

$$\Delta V_T = q/D_i C_{ox} \quad \text{..... (2)}$$

Where D_i = implantation dose for V_t adjust

A more exact formula for calculating the V_T in this case is [3]

$$V_{T(\text{nonuniform doping, long channel})} = V_{FB} + q\, D_i/C_{ox} + \gamma_2(\sqrt{2\varphi_B + q\, D_i x_i/2K_{si}\varepsilon_{si}})/C_{ox} + 2\varphi_B \text{.....(3)}$$

Where $\gamma_2 = (\sqrt{2q\, k_{si}\, \varepsilon_{si} N_A})/C_{ox}$

X_i = effective implant depth.

The V_T adjust implant is often done through an oxide layer. The implant energy is selected to select the peak of the implant slightly below the oxide–silicon interface.

Fig. 2.3 shows the distribution of dopant atoms from a typical implant as a function of depth in to wafer. After the implant the atoms are distributed as a Gaussian profile. The implant concentration is.[3]

$$N_i = \frac{N'}{\Delta R_P \sqrt{2\pi}} \exp\left[-\frac{x - R_P}{2\Delta R_P^2}\right] \text{ cm}^{-3} \text{ .....(4)}$$

Where N' = no. of implanted atoms/area

R_P = average distance an implanted atoms penetrate into the solid

After activation anneal, the implanted distribution becomes slightly broader as shown by the dash curve.

Calculating the effect of this implant on V_T is greatly simplified by approximating the actual distribution via a box distribution as shown. In which the implanted dopant is assumed to have a constant density N_a and depth x_i, Fig. 2.4 shows the variation of threshold voltage with implant depth x_i , we can see that V_T does not change as x_i varies.

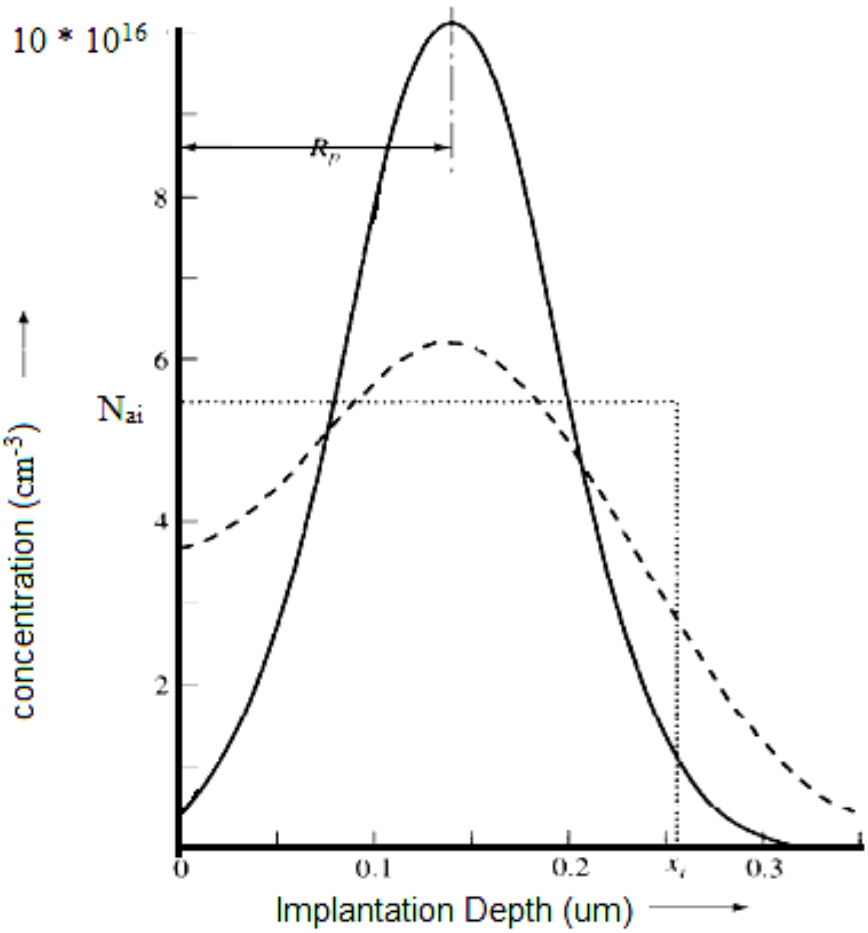


Fig. 2.3 Distribution of implanted dopant (solid) immediately after the implant, and after the activating anneal and diffusions (dashed).[4]

The effective concentration is given by [3]:

$$N_{eff} = N_A' \frac{\varphi_s}{\varphi_i} \left[1 - \frac{N_A}{N_A'} + \frac{N_A'}{N_A} \sqrt{1 + \frac{N_A}{N_A'} \left(\frac{\varphi_s}{\varphi_i} - 1\right)}\right]^2 \quad \text{.....(5)}$$

Where $\varphi_s = kT/q[\ln (N_A \grave{N_A}/n_i^2)]$

$\varphi_i = q\grave{N_A} x_i^2 / 2 k_{si} \varepsilon_{si}$

N_A = Bulk concentration

N_A = concentration after implantation dose.

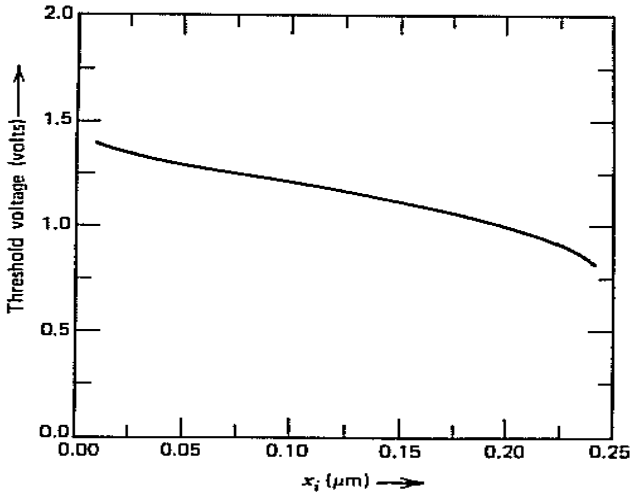


Fig. 2.4 Dependence of V_t on effective implantation depth X_i [4]

2.3 Short Channel Device and Effects

"When the length of a MOSFET approaches of the order of source/drain junction depletion-region width, then the MOSFET is short channel MOSFET".

The term short-channel effects are referring to secondary effects such as mobility degradation and velocity saturation, both of which also occur in long channel devices.

The short-channel effects are attributed to two physical phenomena:

1. The limitation imposed on electron drift characteristics in the channel,
2. The modification of the threshold voltage due to the shortening channel length.

In particular four different short-channel effects can be distinguished:

1. Surface scattering
2. Velocity saturation
3. Impact ionization
4. Hot electrons

2.3.1 Surface scattering

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component E_y increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the *surface scattering [2]* (that is the collisions suffered by the

electrons that are accelerated toward the interface by E_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of E_y, is about half as much as that of the bulk mobility.

2.3.2 Velocity saturation

The performance of short-channel device is also affected by *velocity saturation [2]*, which reduces the transconductance in the saturation mode. At low E_y, the electron drift velocity V_{de} in the channel varies linearly with the electric field intensity. However, as E_y increases above the critical electric field, the drift velocity tends to increase more slowly, and approaches a saturation value. Note that the drain current is limited by velocity saturation instead of pinch-off. This occurs in short channel devices when the dimensions are scaled without lowering the bias voltages. Using V_{de}(sat), the maximum gain possible for a MOSFET can be defined as

$$g_m = W C_{ox} V_{de}(sat) \quad \text{.....(6)}$$

g_m = Transconductance gain
W = Width
C_{ox} = Oxide capacitance

2.3.3 Impact ionization

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by *impact ionization [2]*, that is, by impacting on silicon atoms and ionizing them. It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an n-p-n transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 0.6V, the normally reversed-biased substrate-source p-n junction will conduct appreciably. Then electrons can be injected from the source to the substrate, similar to the

injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new e-h pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip.

2.3.4 Hot electrons

Another problem, related to high electric fields, is caused by so-called *hot electrons*. These high energy electrons can enter the oxide, where they can be trapped, giving rise to oxide charging that can accumulate with time and degrade the device performance by increasing *VT* and affect adversely the gate's control on the drain current [2].

2.4 Transistor Leakage Mechanisms

Reduction of Feature size in MOSFETs is the key part to the continuation of Moore's law. Just as significant as channel length (Le_{ff}) reduction has been the shrinking of the gate oxide layer thickness (T_{ox}). [1]

In long channel devices there are fewer problems in estimation of leakage power but as the technology are scaled down the leakage current increases drastically. In Short channel MOS devices the leakage currents are in the following forms, as shown in fig. 2.5

1. PN- junction reverse-Bias current.(I_1)
2. Subthreshold leakage or Weak inversion.(I_2)
3. Drain induced barrier lowering(I_2)
4. Punch-through (I_6)
5. Effect of channel length
6. Gate oxide tunneling (I_3, I_4)

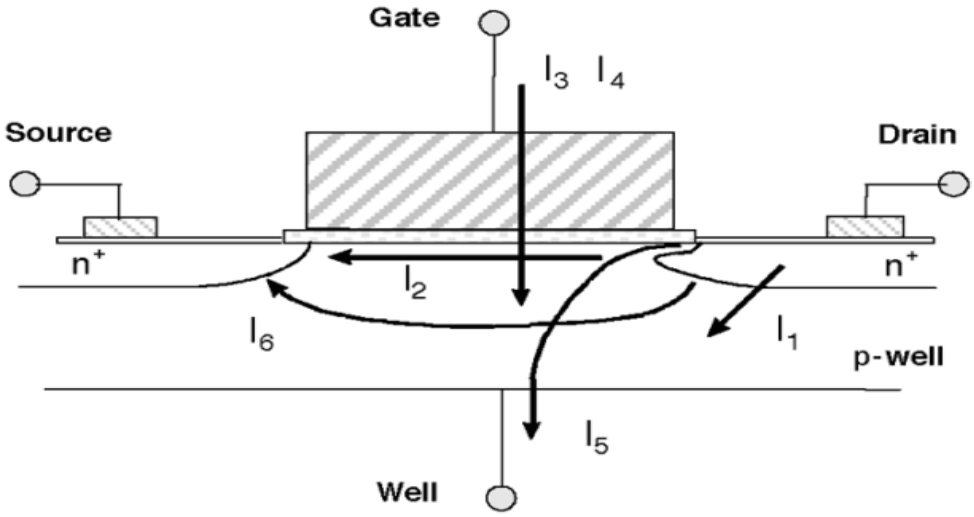


Fig. 2.5 Summary of leakage current mechanisms of deep-submicron transistors.[1]

2.4.1 Band to band tunneling

When a high electric field is applied across the reverse-biased p-n junction then a significant current to is flowing through the junction due to tunneling of electrons. Which is from valence band of the p type to the conduction band of the n type, as shown in Fig. 2.6.. From figure it is clear that for the tunneling to occur, the total voltage drop across the junction has to be more than the band gap.

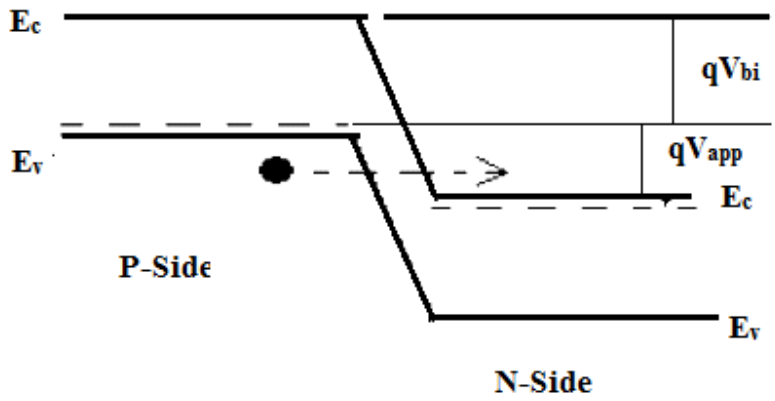


Fig. 2.6 BTBT in Reverse biased p-n junction[1]

2.4.2 Subthreshold leakage

When the gate voltage is below V_{th} in a MOS transistor the subthreshold conduction current flow between source and drain. Supply voltage is made scale down in order to keep the power consumption low. Hence, the transistor threshold voltage has to be scaled to maintain a high drive current and achieve performance improvement. However the threshold voltage scaling results in substantial increase in the subthreshold current the weak inversion region is seen in Fig. 2.7, as the linear region of the curve (semilog plot). In the weak inversion, the minority carrier concentration is small, but not zero[1].

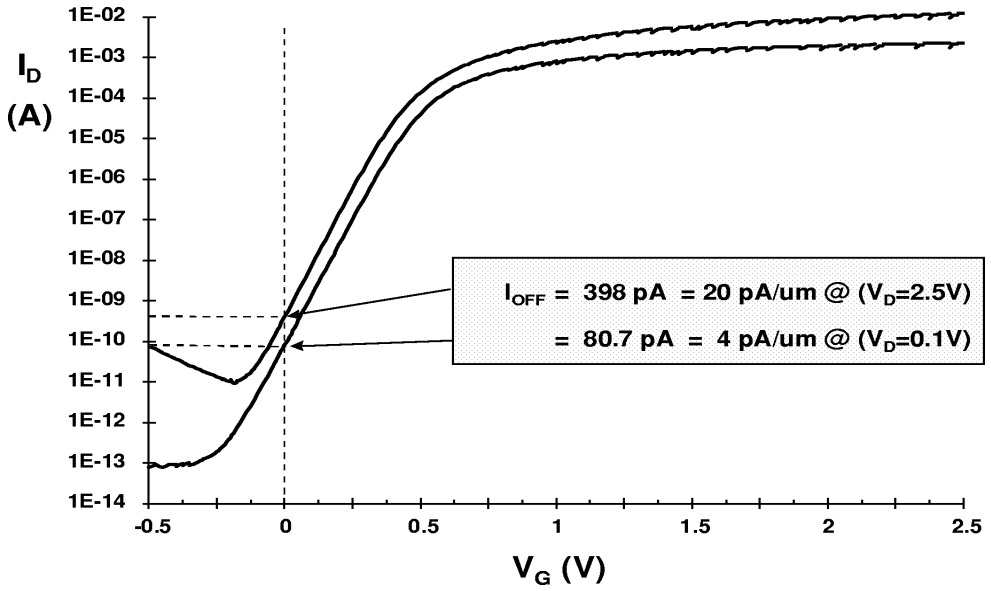


Fig. 2.7 log (I_d) versus V_{gs} at two different drain voltages for 0.35 micron CMOS process [1]

Let us consider that the source of the n-channel MOSFET is grounded, , and the drain to source voltage V_{ds} for such weak inversion condition, drops almost entirely across the reverse-biased substrate-drain p-n junction. The variation of electric field component along the channel is small, and the flow of current is due to the diffusion rather than drifts. The weak inversion current can be expressed based on the following [1]

$$I_{ds} = \mu_0 C_{ox} \times \frac{W}{L}(m-1)(v_t)^2 \times e^{\frac{(V_g - V_{th})}{m v_t}} \times \left(1 - e^{-\frac{V_{DS}}{v_t}}\right) \quad \text{.....(7)}$$

Where $m = 1 + \frac{C_{dm}}{C_{ox}} = 1 + \frac{3T_{ox}}{W_{dm}}$

C_{dm} = capacitance of depletion layer

μ_0 = Mobility

"I_{off} is influenced by the threshold voltage, channel physical dimensions, channel/surface doping profile, drain/source junction depth, gate oxide thickness, and V_{DD} ".

2.4.2a Subthreshold Slope

"Subthreshold slope indicates how effectively the transistor can be turned off (rate of decrease of I_{off}) when V_{gs} is decreased below V_{th} ".

In long-channel devices, the subthreshold current is independent of the drain voltage for V_{ds} larger than a few V_t. On the other hand, the dependence on the gate voltage is exponential, as illustrated in Fig.(6). The inverse of the slope of the $\log_{10}(I_{ds})$ versus V_{gs} characteristic is called the subthreshold slope (S_t) [1].

$$S_t = \left(\frac{d(\log(I_{ds}))}{dV_{gs}}\right)^{-1} = 2.3\frac{mkT}{q}$$

$$= 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right)$$

As the device dimension and supply voltage are scale down to enhance performance power efficiency, and reliability, subthreshold characteristics may limit the scalability of the supply voltage. The parameter is measured in m-V/decade of the drain current. Typical values for a bulk CMOS process can range from 70 to 120 mV/decade. S_t can be made smaller by using a thinner oxide (insulator) layer to reduce T_{ox} or a lower substrate doping concentration (resulting in larger W_{dm}). [1]

2.4.3 Drain Induced Barrier Lowering

DIBL occurs when the depletion region of the drain interacts with the source depletion region and lowers the source potential barrier a small current is flow between the source and drain without any gate voltage. Therefore, the threshold voltage, and consequently the sub-threshold current of short-channel devices, varies with the drain bias. This effect is known as DIBL. For a

long-channel device, the barrier height is mainly controlled by the gate voltage and is not sensitive. However, the barrier of a short-channel device reduces with an increase in the drain voltage, which in turn increases the sub-threshold current due to lower threshold voltage. DIBL is increase at high V_{ds} and shorter L_{eff}. The surface DIBL occurs before the deep bulk punch-through. Higher surface and channel doping and shallow source/drain junction depths reduce the DIBL effect on the sub-threshold leakage current [1].

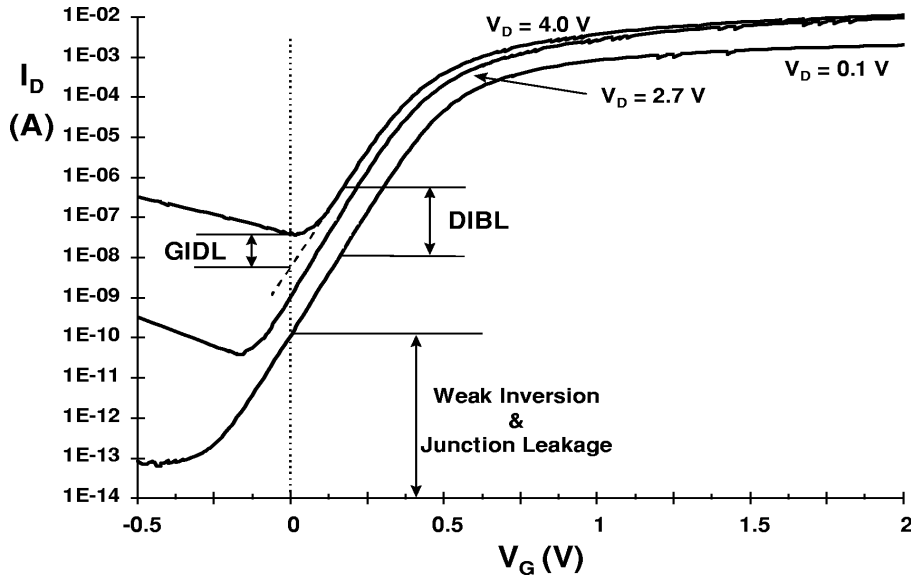


Fig. 2.8 n-channel I_d vs. V_{gs}, showing DIBL, GIDL, weak inversion, and p-n junction reverse-bias leakage components [1]

2.4.4 Punchthrough

When drain and source depletion region approach each other and electrically touch, then bulk Punchthrough occurs. Punchthrough is a condition in which the channel is exists deep into the body region, Punchthrough current varies with drain voltage and S_t Increases. In sub-micrometer MOSFETs, a V_{th} adjust implant is used to have a higher doping at the surface than that in the bulk. This causes a greater expansion of the depletion region below the surface (due to smaller doping there) as compared to the surface. Thus, the punchthrough occurs below the surface[1]. I-V characteristics of a MOSFET with punchthrough given below [2].

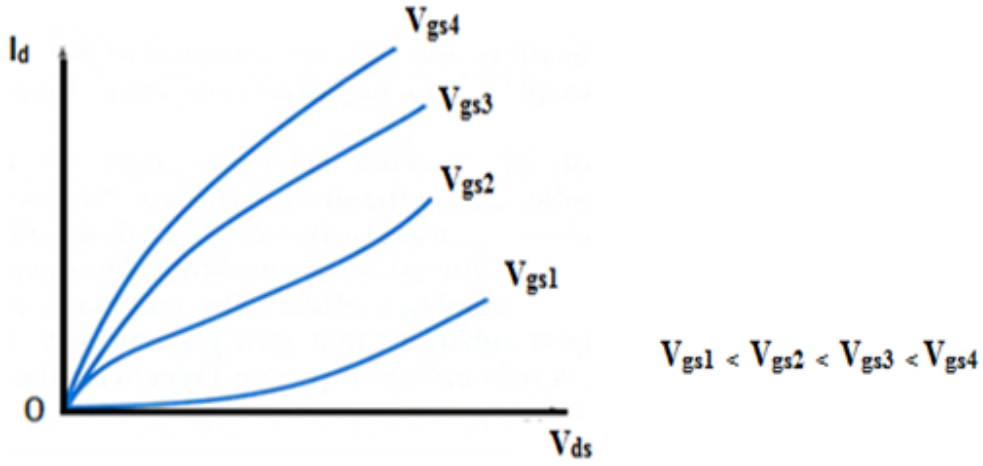


Fig. 2.9 Typical I_d-V_{ds} characteristics with punchthrough problems [2]

2.4.5 Effect of Channel Length (V_{th} Roll-off)

Threshold voltage of MOSFET decreases as the channel length is reduced. Reduction of threshold voltage with reduction of channel length is known as roll-off, As shown in the fig. 2.10. The principal reason behind this effect is the presence of 2-D field patterns in short-channel devices instead of one-dimensional (1-D) field patterns in long-channel devices [1].

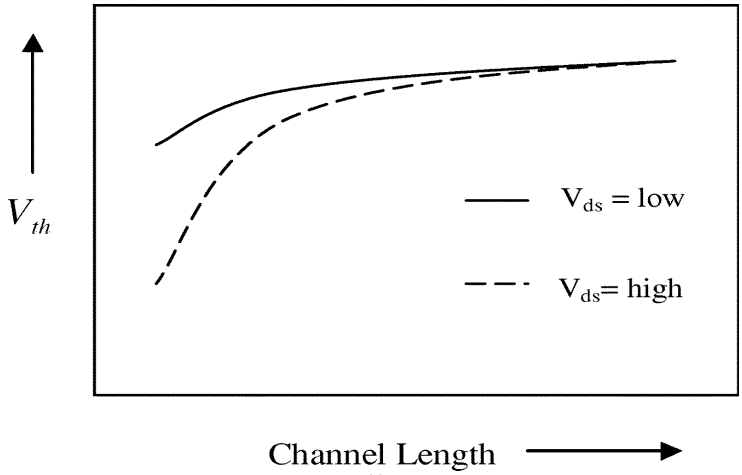


Fig. 2.10 Threshold voltage Roll-off with change in channel length [1]

When the channel length is decreases the area under the gate is decrease and hence less number of chare are required to neutralize the charge under the gate, and hence less gate voltage is required in short channel devices and V_t will decrease according to Fig.2.10. This reduction in V_t increased the subthreshold leakage.

2.4.6 Gate Current

Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons. This is from substrate to gate and from gate to substrate through the gate oxide, resulting in the gate oxide tunneling current.

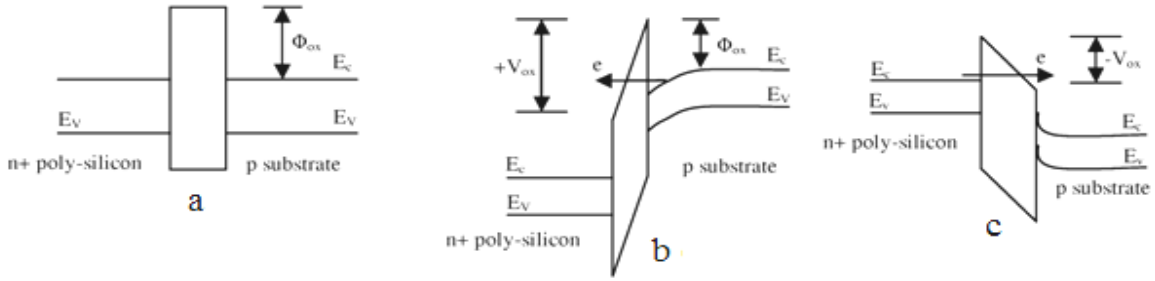


Fig. 2.11 Tunneling of electrons through an MOS capacitor [1]

let us consider an MOS capacitor with a heavily doped n+-type polysilicon gate and a p-type substrate. Also, for simplicity, let us now focus only on the electron tunneling. An energy-band diagram in flat-band condition is shown in Fig. 2.11a, where Φ_{ox} is the Si-SiO_2 interface barrier height for electrons. When a positive bias is applied to the gate, the energy-band diagram becomes as given in Fig. 2.11b. Due to the small oxide thickness, which results in a small width of the potential barrier, the electrons at the strongly inverted surface can tunnel into or through the SiO_2 layer and hence give rise to the gate current. On the other hand, if a negative gate bias is applied, electrons from the n+ polysilicon can tunnel into or through the oxide layer and give rise to the gate current [see Fig. 2.11c]. The tunneling probability of an electron depends on the thickness of the barrier, the barrier height, and the structure of the barrier [1].

The mechanism of tunneling between substrate and gate polysilicon can be primarily divided into two parts, namely:

2.4.6a Fowler–Nordheim Tunneling

In FN tunneling, electrons tunnel into the conduction band of the oxide layer. Fig. 2.12 shows the FN tunneling of electrons from the inverted surface to the gate The FN current equation represents the tunneling through the triangular potential barrier and is valid for $V_{ox}>\Phi_{ox}$, where V_{ox} is the voltage drop across the oxide

2.4.6b Direct Tunneling

In very thin oxide layers (less than 3–4 nm), electrons from the inverted silicon surface, instead of tunneling into the conduction band of SiO_2, directly tunnel to the gate through the forbidden energy gap of the SiO_2 Layer.

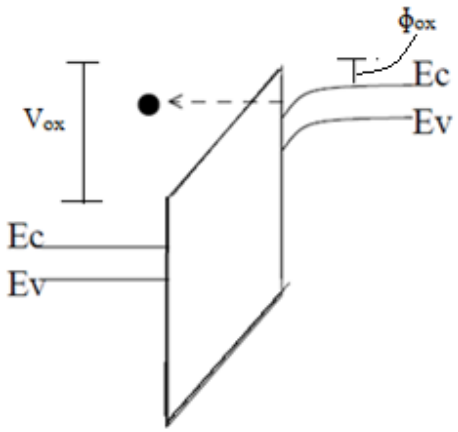


Fig. 2.12 FN Tunneling of electrons[1]

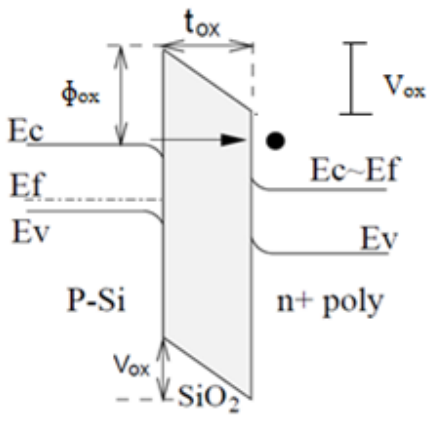


Fig. 2.13 Direct tunneling of electron.

The direct tunneling phenomenon is explained in Fig. 2.13. In the case of direct tunneling, electrons tunnel through a trapezoidal potential barrier instead of a triangular potential barrier. Hence, the direct tunneling occurs at $V_{ox} < \square_{ox}$ [1]

2.5 Solution to Short Channel effects

There are several advanced fabrication technique can be applied to suppress the channel effects. In the following subsection, the solutions of punch-through effects (retrograde well and halo implant) and hot electron effects (light-doped drain) will be discussed.

2.5.1 Channel Engineering

To maintain acceptable off-state leakage with continually decreasing channel lengths will require that channel doping levels increase to offset the degradation in short channel effects for extremely small devices. Although both vertical and lateral channel engineering can be used to improve degradation due to these effects.

2.5.1a Retrograde Channel doping

Retrograde channel doping is a form of vertical channel engineering. It is used to improve short channel effects and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region.

The low surface concentration increases surface channel mobility by minimizing channel impurity scattering while the highly doped subsurface region acts as a barrier against punch-through [1].

To be effective, the retrograde depth should transition from a low to high concentration very quickly. As source/drain junction depths are scaled, the retrograde well depth also be scaled. Fig. 2.14 shows a schematic band-bending diagram at the threshold condition of an extreme retrograde profile with an undoped surface layer of thickness. For the same gate depletion width, the surface electric field and the total depletion charge of an extreme retrograde channel is one-half that of a uniformly doped channel. This reduces the threshold voltage and improves mobility. Retrograde channel doping allows the threshold voltage to be decoupled from the gate-controlled depletion width. However, the body effect coefficient and the subthreshold slope are still coupled to the gate depletion width.

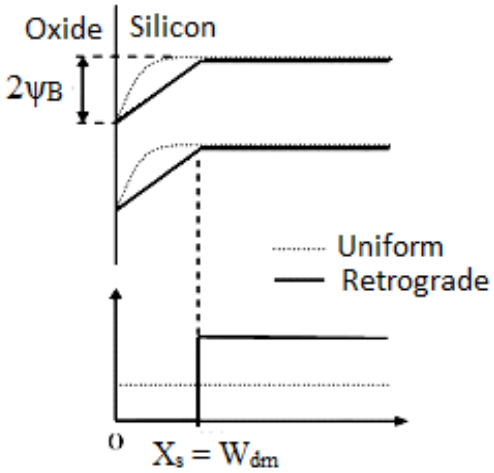


Fig. 2.14 Band diagrams (shown on top) at the threshold condition for a uniformly doped and an extreme retrograde-doped channel (doping profiles shown at bottom)[1]

2.5.1b Halo Doping

The use of halo/pocket implants is another channel engineering technique that can improve short channel effects and thereby control the threshold voltage roll-off.

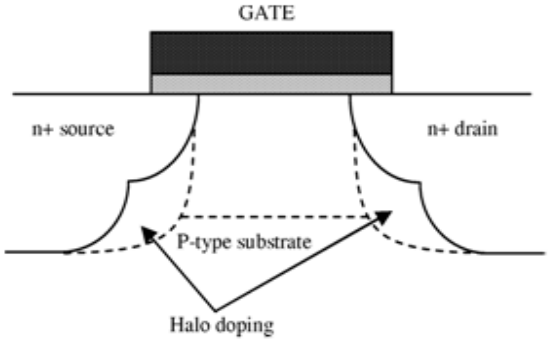


Fig. 2.15. Halo doping [1]

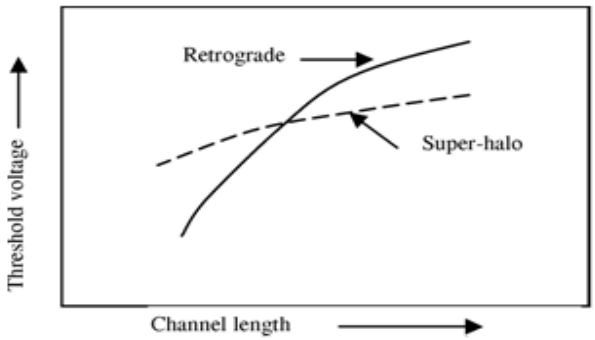


Fig. 2.16. Short-channel threshold-voltage roll- off for retrograde an super-halo [1]

Halo doping or non uniform channel profile in a lateral direction was introduced below 0.25micron technology node to provide another way to control the dependence of threshold voltage on channel length [1]. For n-channel MOSFETs, more highly p-doped regions are introduced near the two ends of the channel which reduces the charge-sharing effects from the source and drain fields. As the channel length is reduced, these highly doped regions consume a larger fraction of the total channel. Reduction of charge-sharing effects reduces the threshold voltage reduction due to channel length reduction. Thus, threshold voltage becomes more almost independence on channel length Fig. 2.16. Hence, the off-current becomes less sensitive to channel length variation [1].

2.5.2 Source/Drain Engineering

The channel doping profile is not the only thing important for device performance. The doping profile in the source/drain region can also have a profound impact on short channel effects. As a result, considerable effort has been put into the optimization of the source/drain doping by the semiconductor industry.

2.5.2a Source/Drain Extension (Light Doped Drain)

The shallow source/drain extension is a commonly found feature in modern MOS device designs. The shallow source/drain extension was originally introduced to relieve high electric fields and the

resulting breakdown of the device due to hot electron effects; for modern high performance devices however, the source/drain extension is motivated more by the trade-offs between short channel effects and source/drain resistance.

Short channel effects improve with decreasing junction depths in the source/drain region. However, shallow source/drain junctions would lead to high extrinsic resistances, which is detrimental to performance. The source/drain extension presents a shallow effective source/drain junction to the channel region, while at the same time, minimizes the contribution of the source/drain region to extrinsic resistance through the presence of the deep source/drain region.

The main objective of LDD extensions is

• To reduce the drain electric field by a lower dopant concentration than in the S/D regions

and/or

• To separate the location of the maximum electric field and the maximum current flow in order to

reduce hot carrier effects

2.5.3 Reducing the gate oxide thickness

On the device front, maintaining good device aspect ratio, by scaling gate oxide thickness is important for controlling short channel effects. With the silicon dioxide gate dielectric thickness approaching scaling limits due to rapid increase in gate tunneling leakage current, researchers have been exploring several alternatives, including the use of high permittivity gate dielectric, metal gate and novel device structures.

CHAPTER 3
PROCESS SIMULATION

3.1 Process Simulation

Process simulation involves the modeling of physical processes with the aim of studying their effects on the external environment and the objects they are applied to. These processes usually involve the interaction between two or more systems. Process simulation comprises the modeling of all process steps which are necessary for the fabrication of semiconductor devices. These process steps are layer deposition**,** lithography**,** etching**,** implantation**,** oxidation and diffusion.

The process simulation uses Athena (module of Silvaco TCAD Tool [Appendix]) as a simulator that provides general capabilities for numerical, physically-based, two-dimensional simulation of semiconductor processing.

Table 3.1 SHOWS the standard values used in the process simulation 90nm process.

Table 3.1 B=>Boron, As=>Arsenic, P=>Phosphorous, E=>Energy

Process	**Value**
Initial substrate	P=1.0e14 cm^{-3} Orientation= <100>
Retrograde well	B=1E13 cm^{-3} , E=250 KeV
Gate Oxide	20Å
V_t adjust implant	B=4.9E13 cm^{-3} , E=29 KeV
Polysilicon Deposition	100nm
Source/Drain Extension(LDD)	As= 2.6e12 cm^{-3} E=13.01 KeV
Halo implant	B=5.0e12 cm^{-3} E=30 KeV Tilt=60^0, fullrotat
Spacer deposition	100nm
Source/Drain	As=1e16 cm^{-3} E=5 KeV
Final Rapid thermal Anneal(RTA)	1000^0C/3 sec.

In process simulation, the result of an implantation step is mostly described by a so-called Pearson function whereas the diffusion equation is solved to derive the influence of an annealing step. Fig. 3.1 illustrates the overview of process simulation

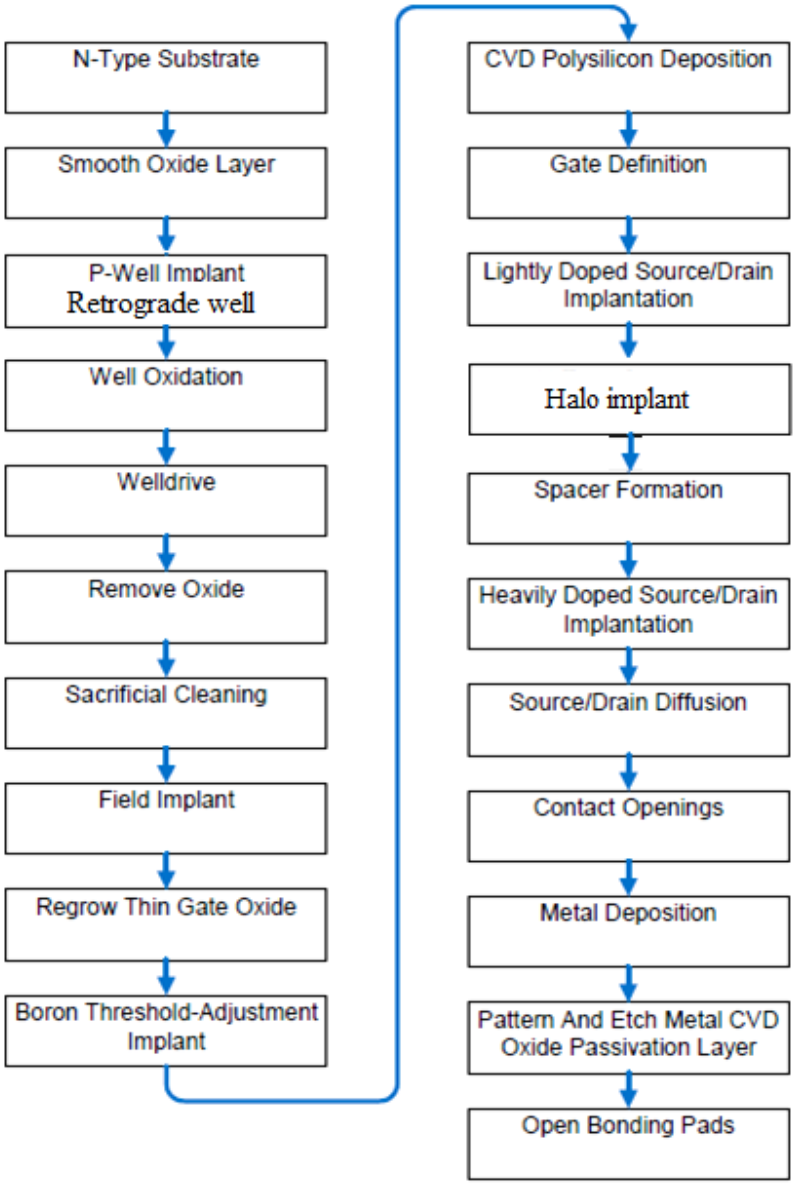


Fig. 3.1 Basic NMOS fabrication flow chart

The above flow chart describe the processing steps foe fabricating the NMOS on Athena, in the first step N-type substrate has been used of orientation of <100> and phosphorous is used. Then smoothing of silicon substrate is done by the dry oxygen in the presence of HCl. Now P-Well

implant is introduced in to the initial substrate and it is oxidized with wet-oxygen, in the P-Well implantation the nature of the P-Well is made retrograde by using energy variation from top to bottom deep in to the bulk. Now well drive is used This step is essential in the preparation of the p-well before further fabrication procedures are performed on this region. More diffusion steps are performed here with varying temperatures, temperature change rates and processing environments. The presence of nitrogen in a diffusion step provides an inert environment for diffusion cause no oxide to generate on the substrate. This process is called anneal. It is then necessary to etch the present oxide from the substrate to provide a surface to begin the process of defining the physical MOSFET features. The last step taken ready the substrate before beginning the processes to develop the physical structure of the MOSFET is to perform a sacrificial cleaning. This process requires oxidation and then the removal of the oxide produced. The oxygen in the oxidation step reacts with the surface silicon forming SiO_2 before it is etched away. As a result, a thin layer of the substrate is removed. This process ensures that the surface substrate layer is free from damage from previous process steps. Then gate oxide if grown with the help of dry oxygen, The thickness of this oxide layer can be varied by changing the time, temperature or type of the oxidation. Then V_t adjust implant is performed for adjusting the threshold voltage boron is is used for this purpose. Poly has been doped on the surface and then etched away to define the physical gate length. Then poly oxidation and LDD is implanted by arsenic. Before using spacer halo pockets have been introduced near the S/D region of the channel by using some angle this is used for leakage reduction. An oxide spacer is then formed to provide a barrier of isolation and to aide in patterning for the
next implantation. The heavy drain/source can then be implanted in the same fashion as the light drain/source. This heavily doped region is several orders of magnitude greater than the lightly doped region. It is then necessary to diffuse the newly created drain/source. This process is done in an inert environment (anneal) to avoid unwanted reactions. The next step in this process requires etching the oxide layer above the drain/source region, this is the contact opening. Aluminum is used for the metal deposition.

The 90nm n-channel MOSFET (NMOS) was designed as a surface channel, which is situated on its p-well. All the physical parameters were tuned to achieve the 90nm actual channel MOSFET design specifications according to ITRS roadmap.

We start with the cleaned, lightly doped silicon substrate (boron, concentration $10^{15}cm^{-3}$ for nMOS).

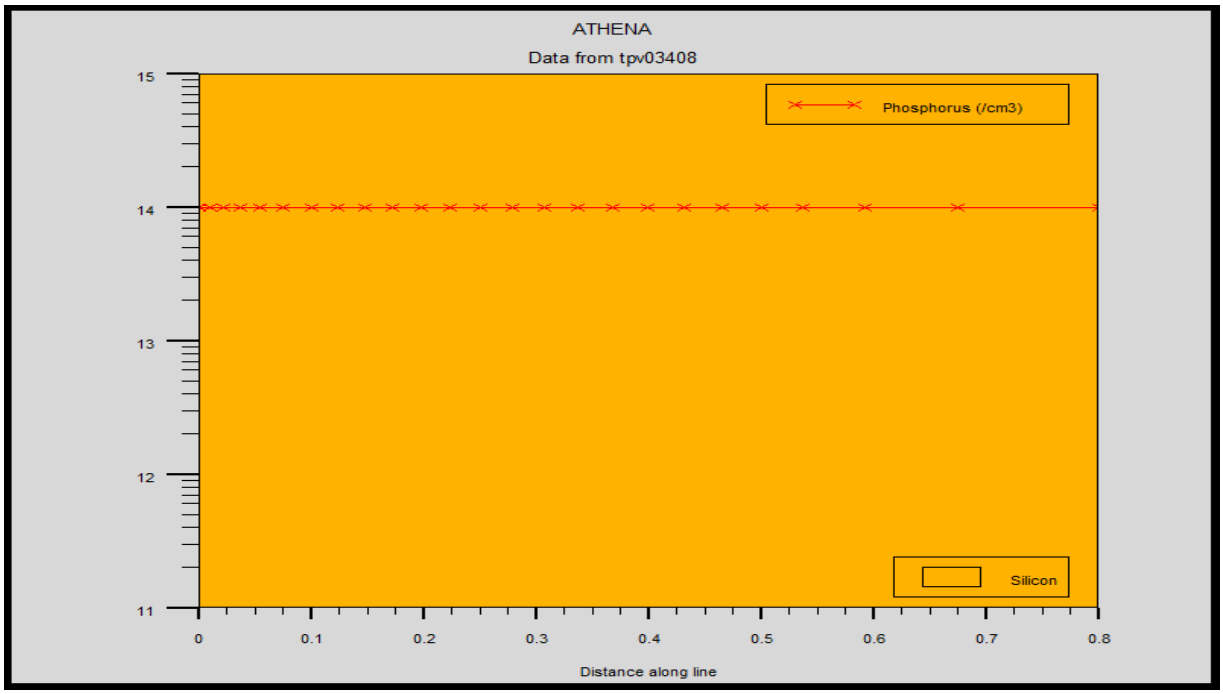


Fig. 3.2. Substrate Doping Concentration

The next step is implantation of Boron to create a p-well (excess holes) in the substrate. A NMOS transistor must be developed in p-type silicon because this material under the gate must be inverted fig 3.3.

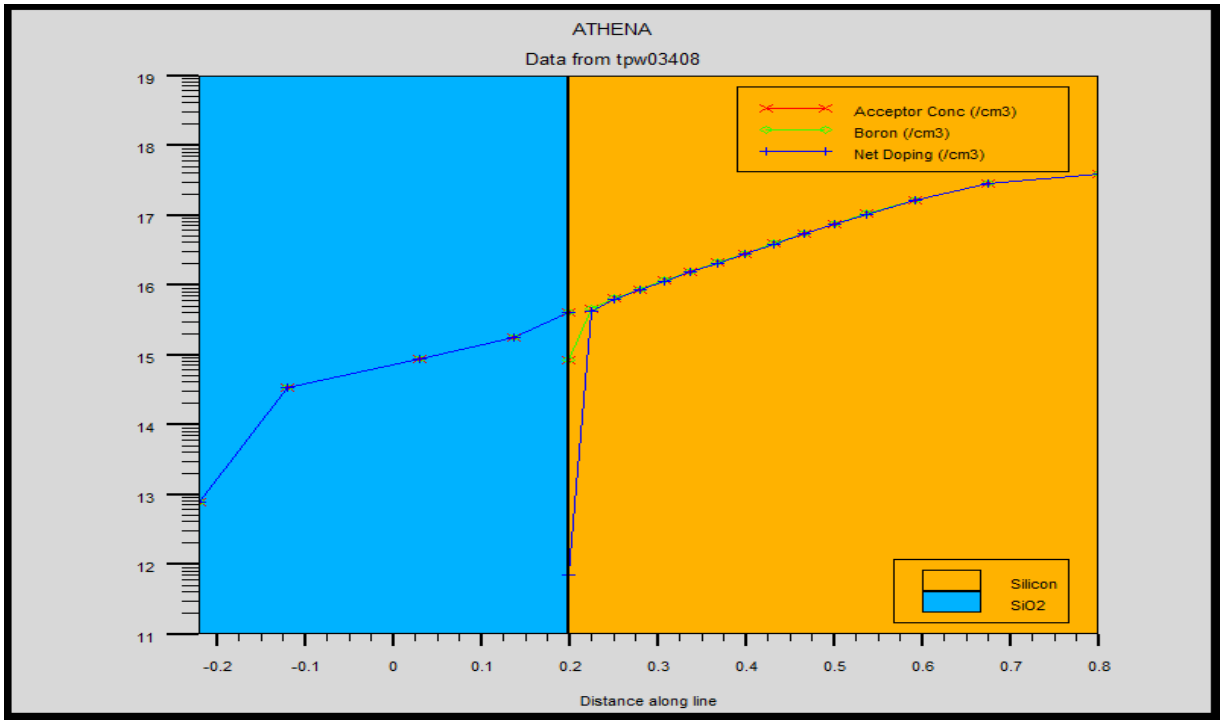


Fig. 3.3 Retrograde P-Well for nMOS (doping concentration)

The gate oxide is then deposited on the substrate by deposition commands. The thickness of this oxide layer can be varied by changing the time, temperature or type of the oxidation. 3.4.

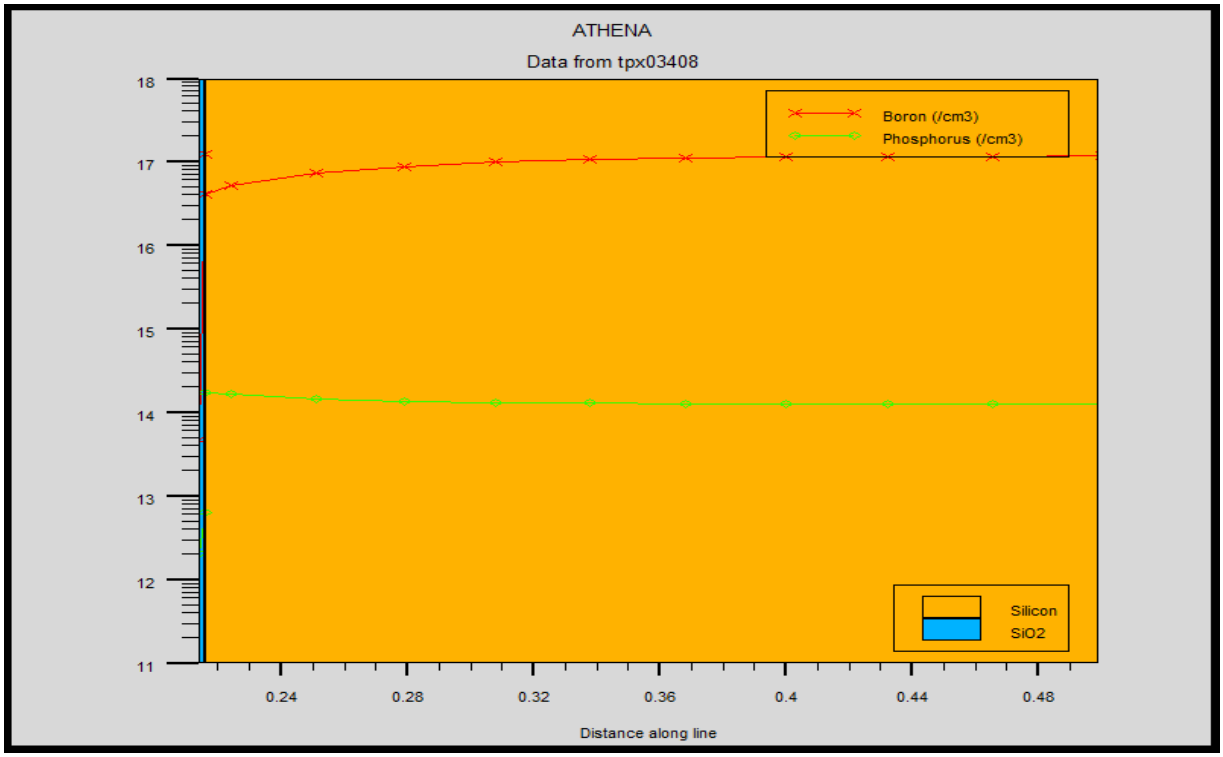


Fig.3.4 Gate oxide deposition after etching of pad oxide.

Boron is then implanted through the gate oxide in a similar fashion as the previous p-well implant was performed, this is called V_t adjust implant. The concentration of the material at the surface adjust the V_t of the MOSFET (Fig.3.5)

The next step in the MOSFET fabrication is the deposition of Polysilicon. This material will be used to create the gate of the MOSFET, and then define the gate through patterning and etching. The implantation of the light drain/source is then performed. This implantation is, again, performed through a deposited oxide layer. A halo implant has been performed after the LDD implantation to produce a highly p-doped region near the source/drain. An oxide spacer is then formed to provide a barrier of isolation and to aide in patterning for the next implantation as in Fig 3.6. The heavy drain/source can then be implanted in the same fashion as the light drain/source. This heavily doped region is several orders of magnitude greater than the lightly doped region. as in fig 3.9.

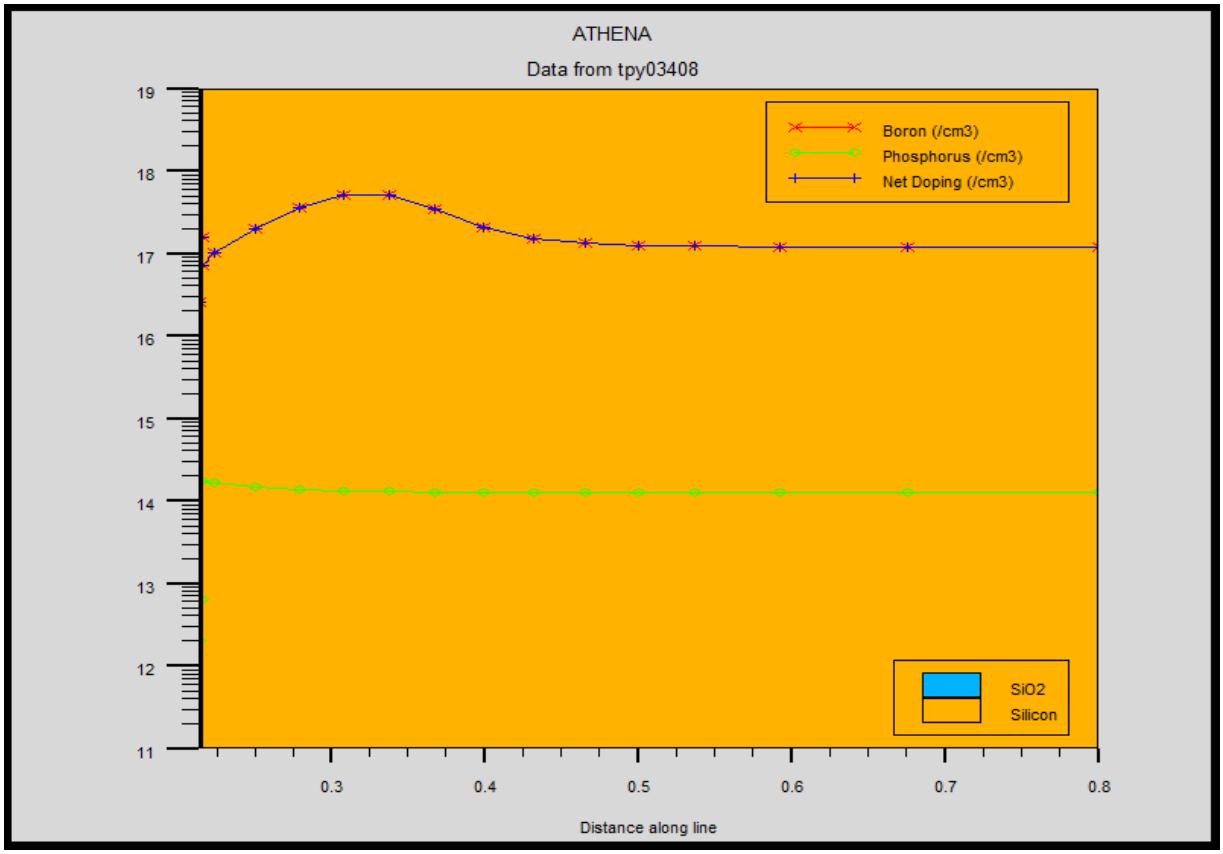


Fig.3.5 Structure after V_t adjust implant (doping concentration)

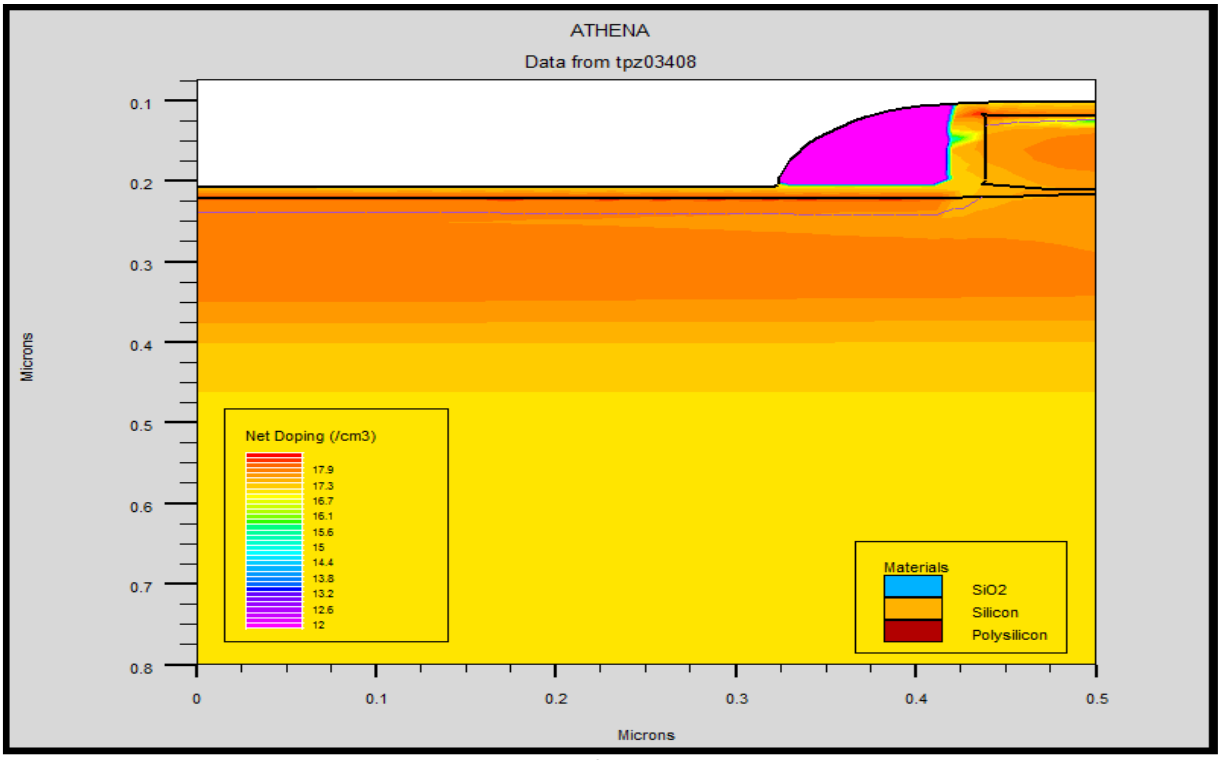


Fig. 3.6 MOSFET structure after poly, spacer and halo doping

After all the the processing steps without halo and retrograde techniques the NMOS is given below (fig. 3.10), the final NMOS with halo and retrograde well is given in the next chapter.

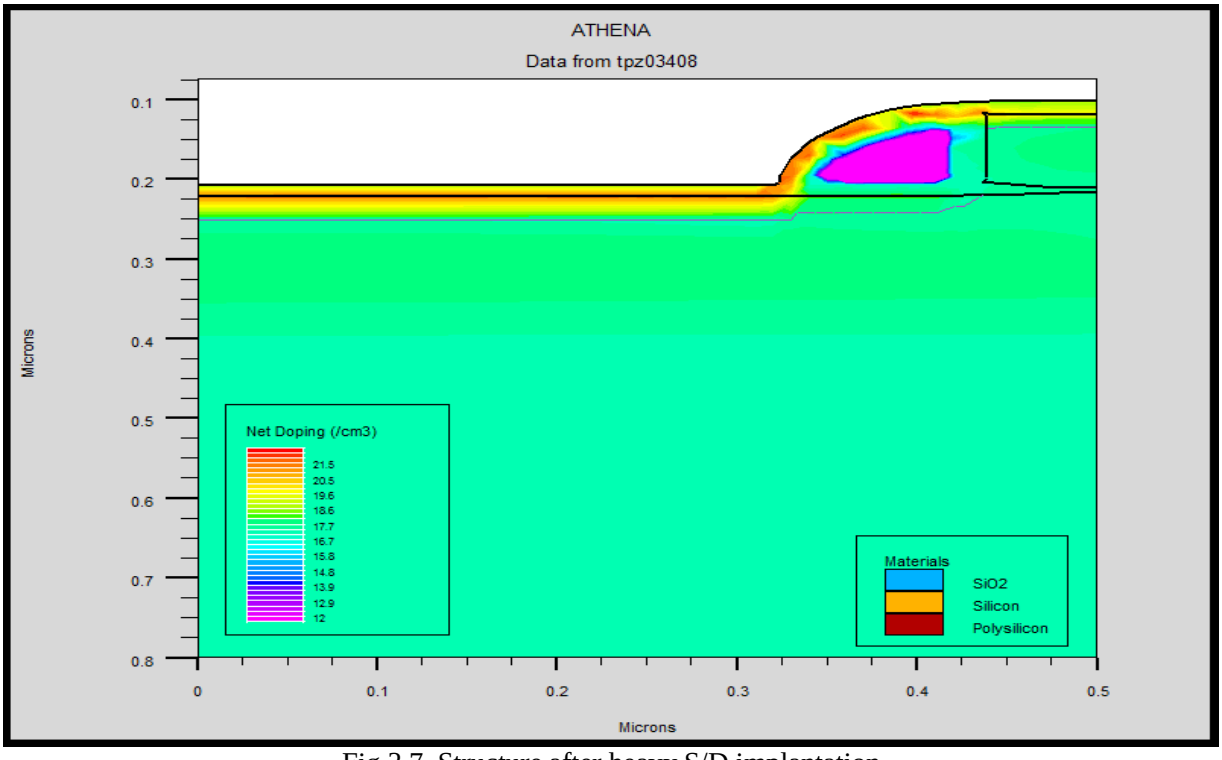


Fig 3.7 Structure after heavy S/D implantation

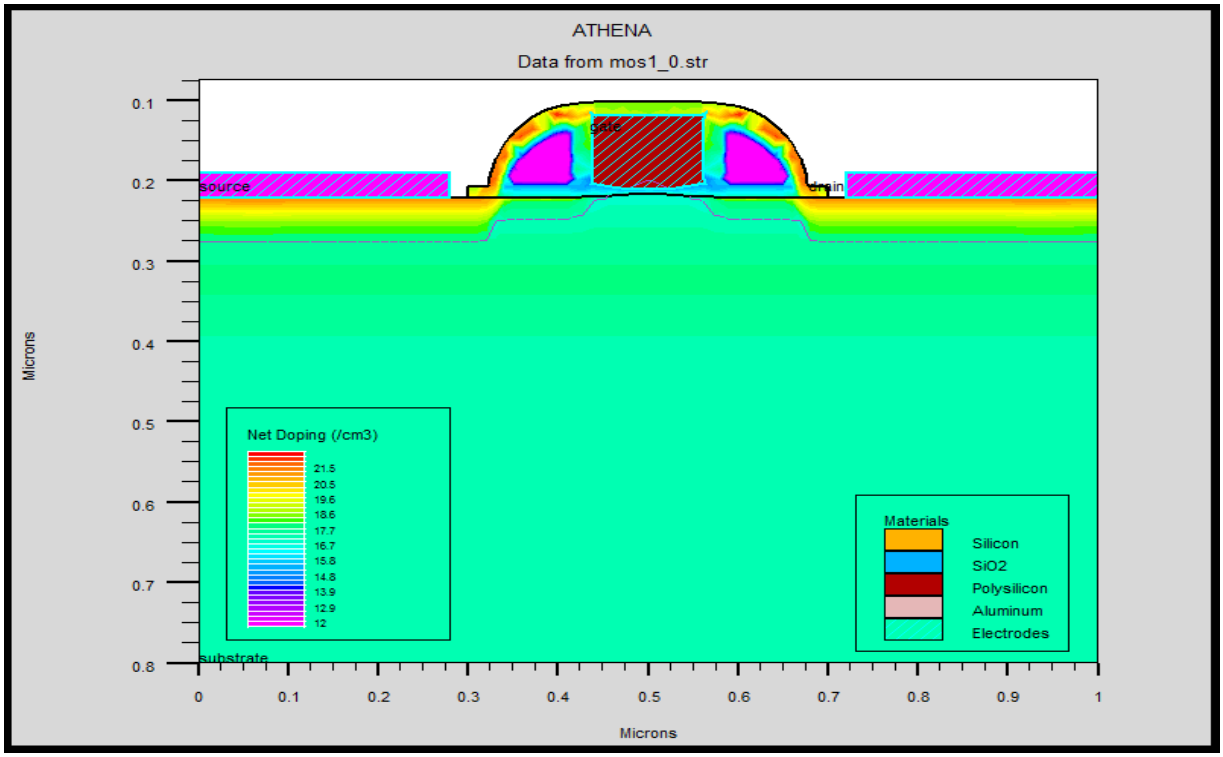


Fig. 3.8 MOSFET structure after all the processing step without halo doping and retrograde well.

CHAPTER 4
RESULTS AND CONCLUSION

4.1 Results and Discussion

After all the processing steps of the NMOS fabrication and introducing the halo and retrograde doping the final device is given below in fig. 4.1.

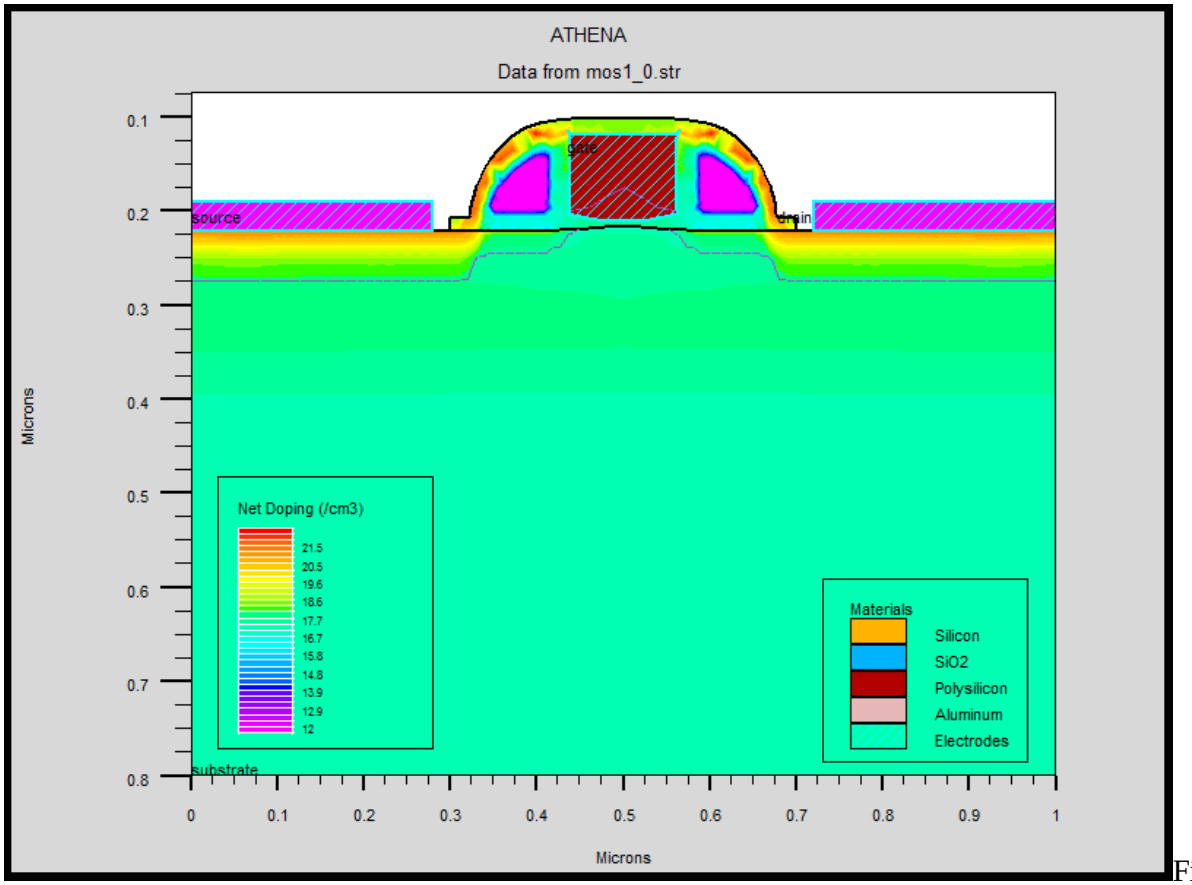


Fig .4.1 Final Structure of MOS with all the advanced fabrication techniques

This device is simulated on Silvaco-Atlas (module of Silvaco[Appendix]) and its characteristics has been analyzed and given below. Device simulation is applied to calculate the electrical behavior of semiconductor devices. The information about device geometry and the local dopant concentrations must be given by some kind of solid modeling or full process simulation.

The log plot $I_d - V_{gs}$ characteristics is given below in Fig. 4.1, from the graph the subthreshold leakage obtained is 1.9×10^{-9} A.

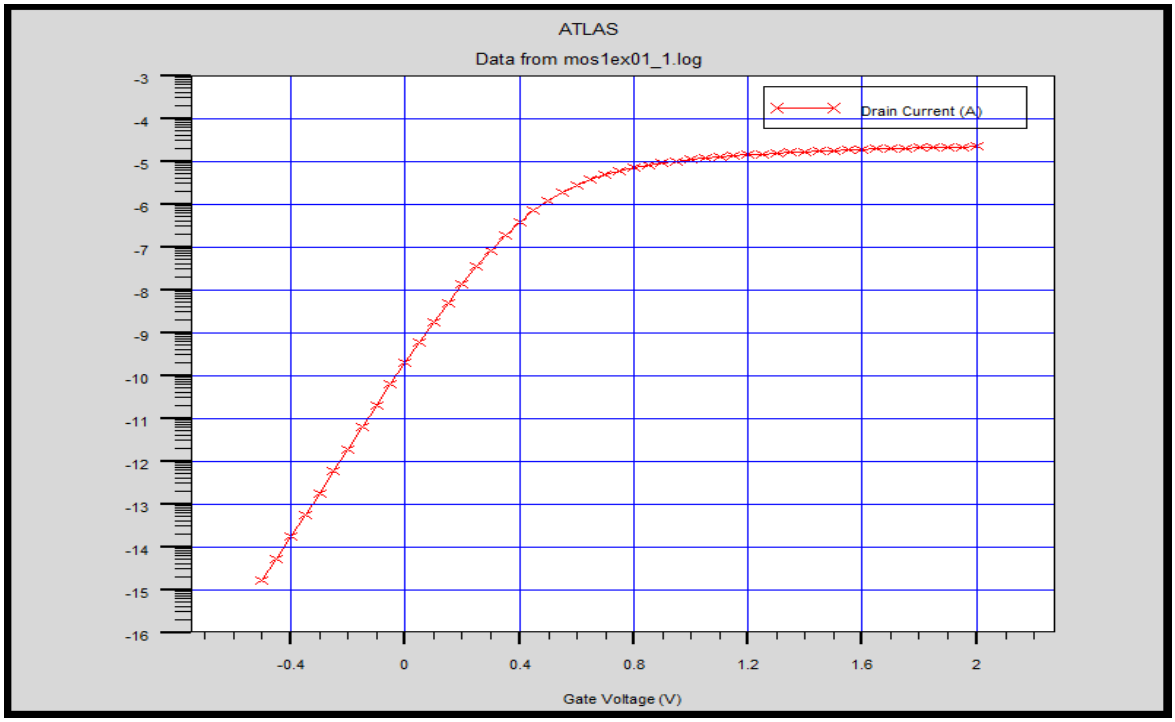


Fig. 4.2. I_d – V_{gs} characteristics of 90nm n-channel NMOS (semilog)

The device has been simulated also by introducing the retrograde well in to the NMOS and the leakage has been reducing up to 1.27×10^{-10} A. The I_d-V_{gs} graph given below.

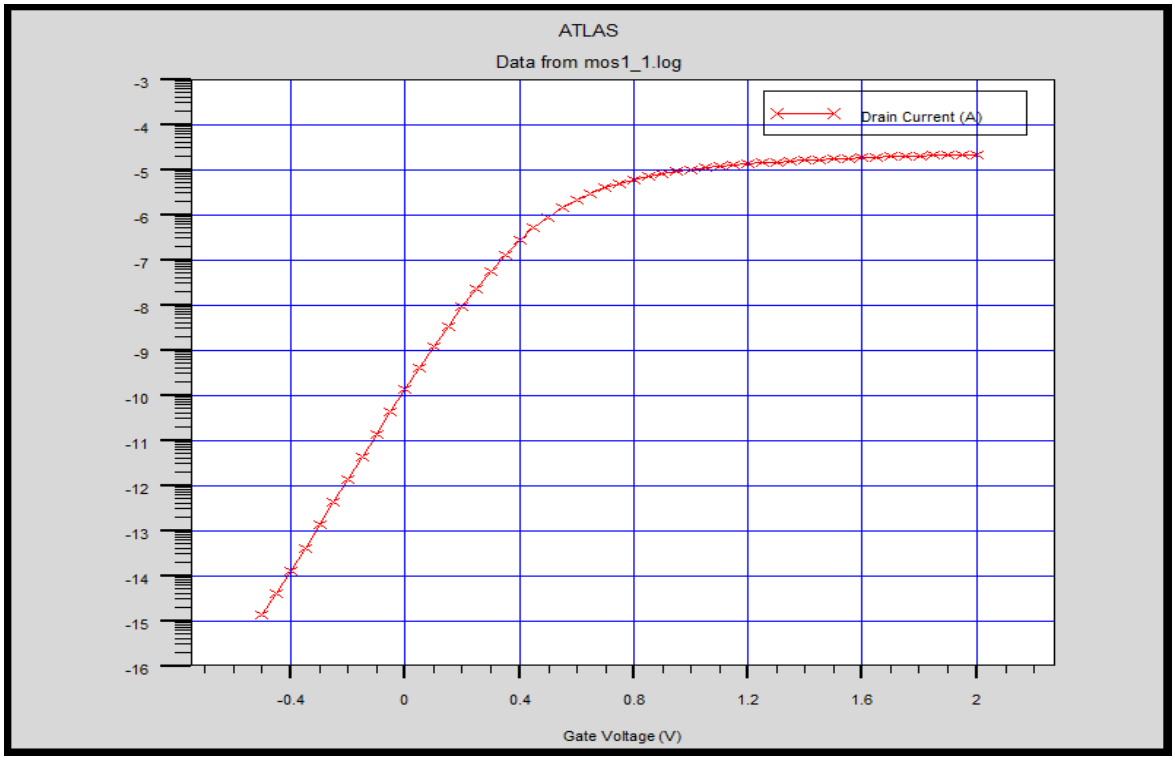


Fig. 4.3. I_d – V_{gs} characteristics of 90nm n-channel NMOS with retrograde well implant (semilog)

The device has been simulated also by introducing the halo doping and Retrograde well in the channel region of nMOS and the leakage has been reduce up to 4.36×10^{-12} A. The I_d-V_{gs} graph with the halo doping and retrograde well is given below in Fig. 4.4.

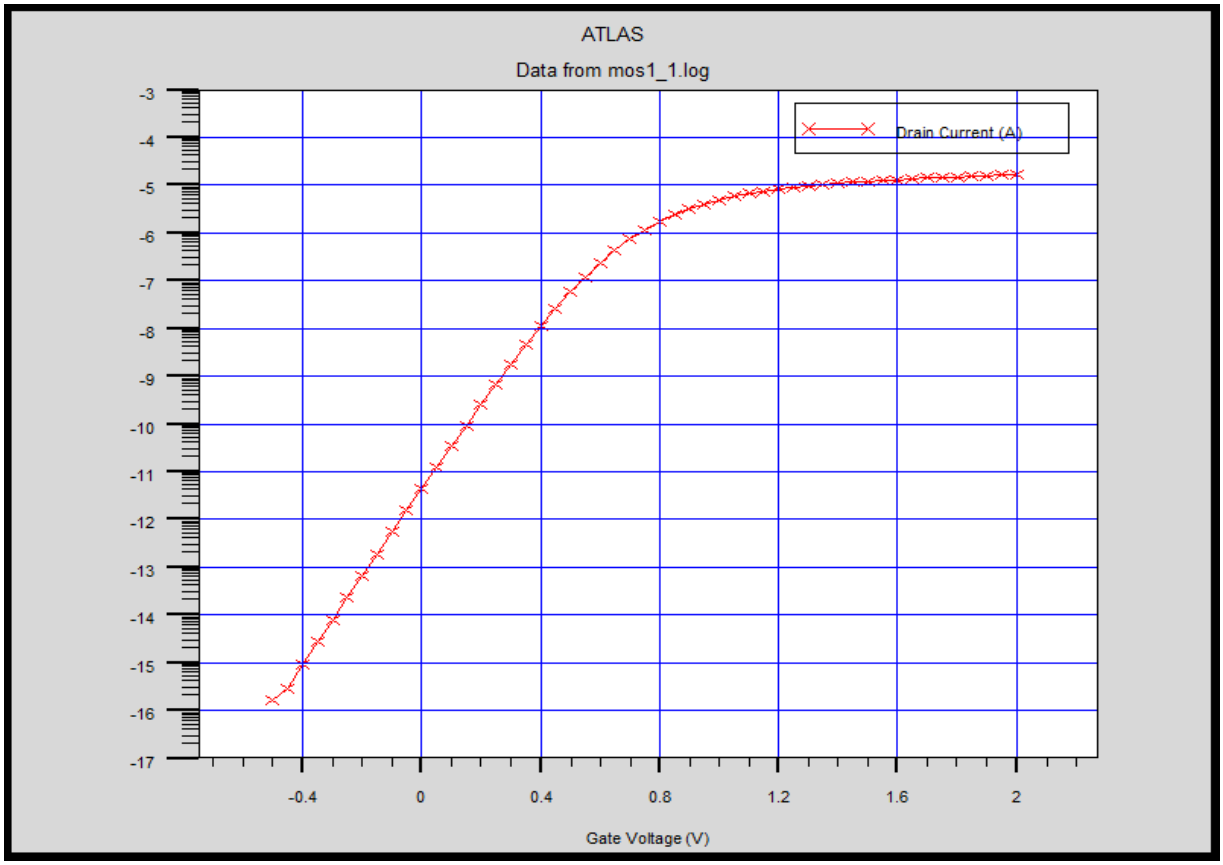


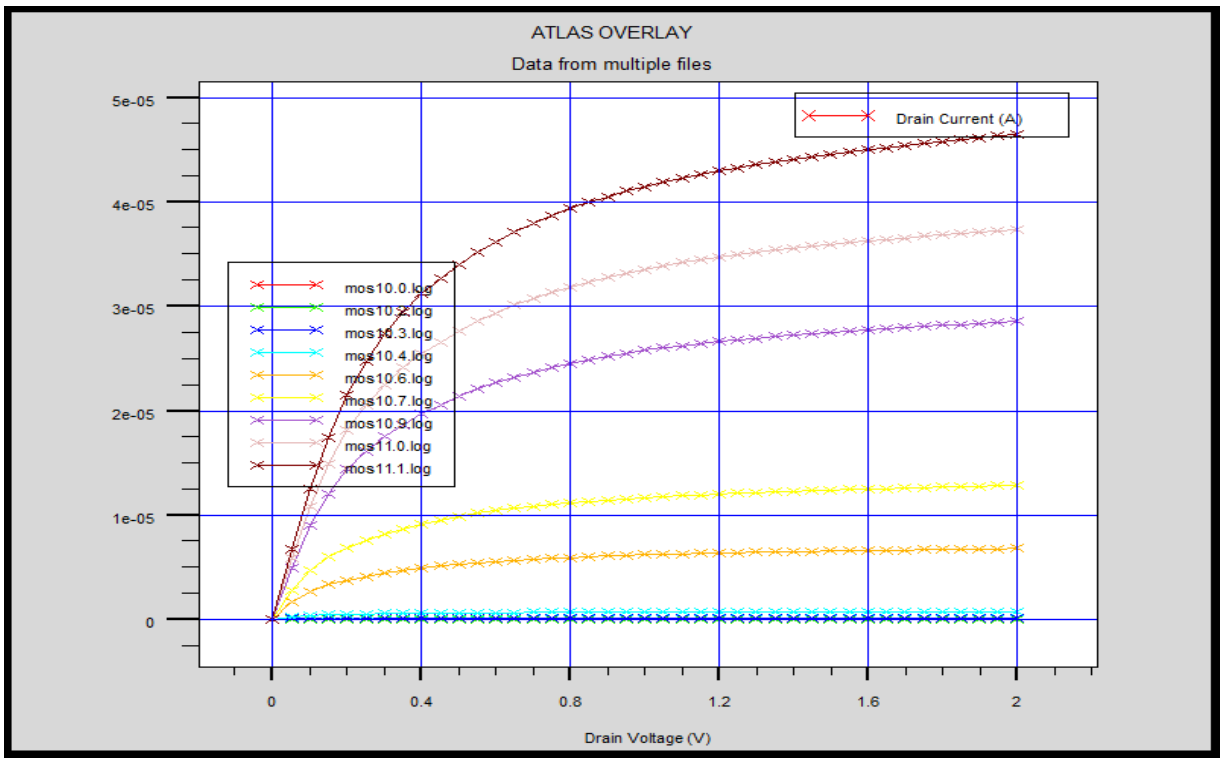
Fig.4.4 I_d – V_{gs} characteristics of 90nm n-channel MOS with halo and retrograde techniques (semilog)

Table 4.1 Leakage current in the NMOS after applying all the process level techniques.

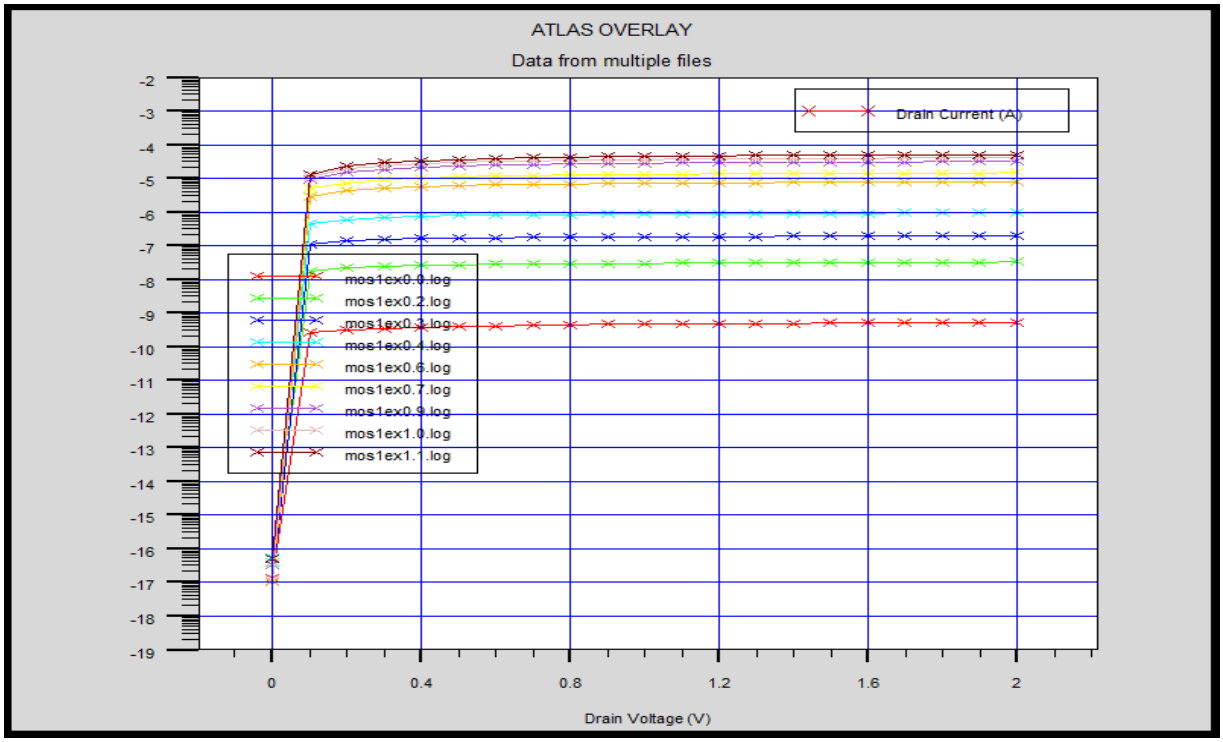
Process techniques emplpoyed	**Leakage observed (in Ampere)**	**I_{on}/I_{off}(uA/nA)**
Simple NMOS fabrication.	1.90×10^{-9}	5.26
Retrograde well.	1.27×10^{-10}	78.50

Retrograde well, halo doping.	4.36×10^{-12}	1146.78

The I_d- V_{ds} characteristics are given below in Fig 4.5.



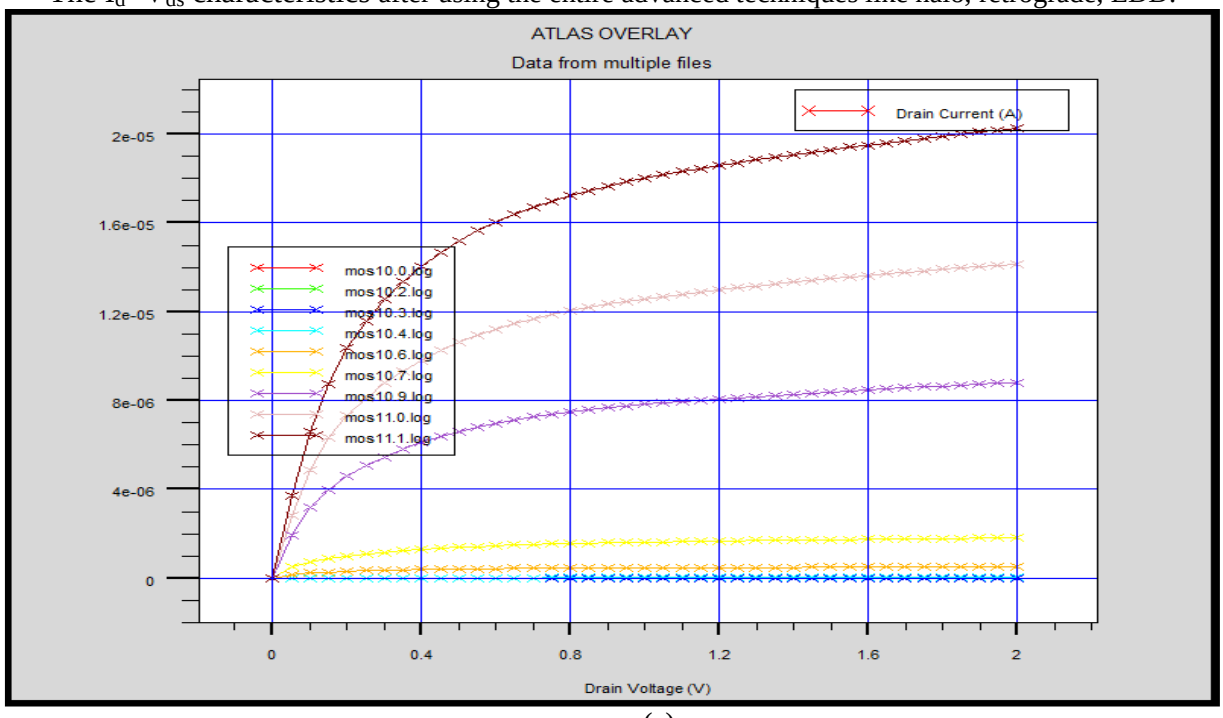
(a)



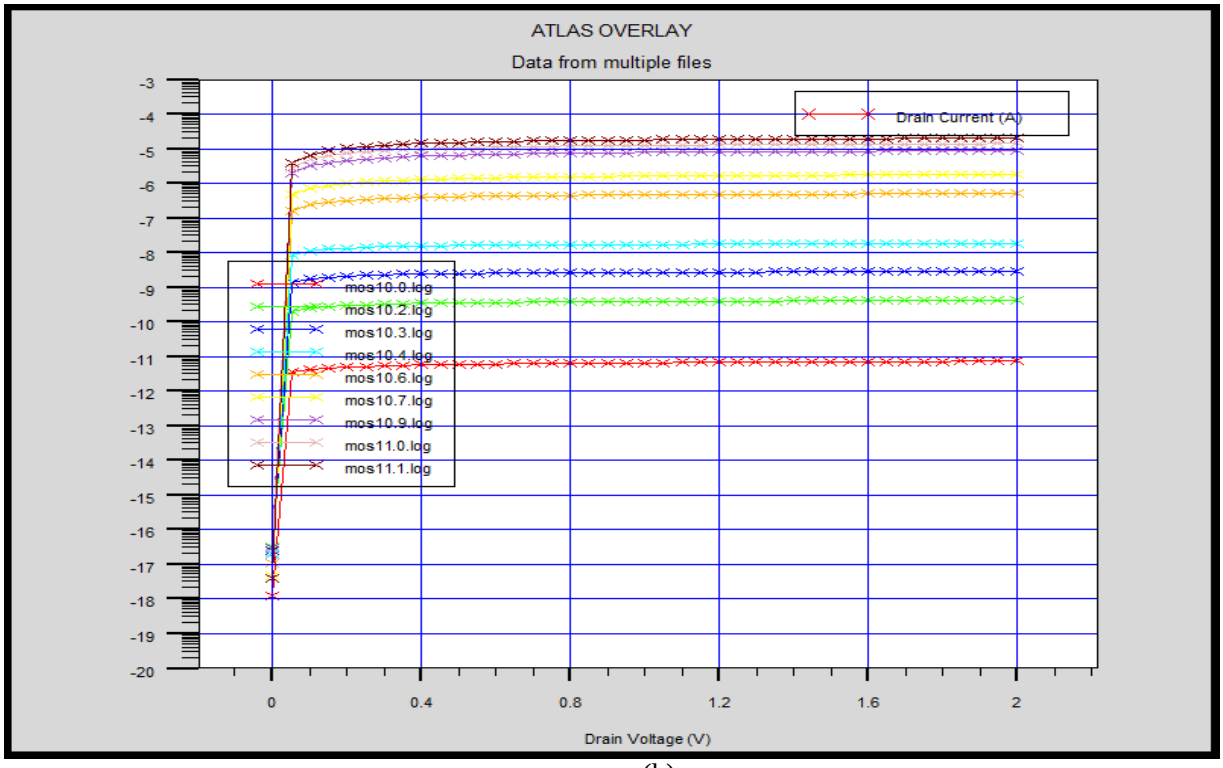
(b)

Fig. 4.5 I_d – V_{ds} characteristics of 90nm n-channel MOS without halo and retrograde. (a) Linear (b) Semilog

The I_d- V_{ds} characteristics after using the entire advanced techniques like halo, retrograde, LDD.



(a)

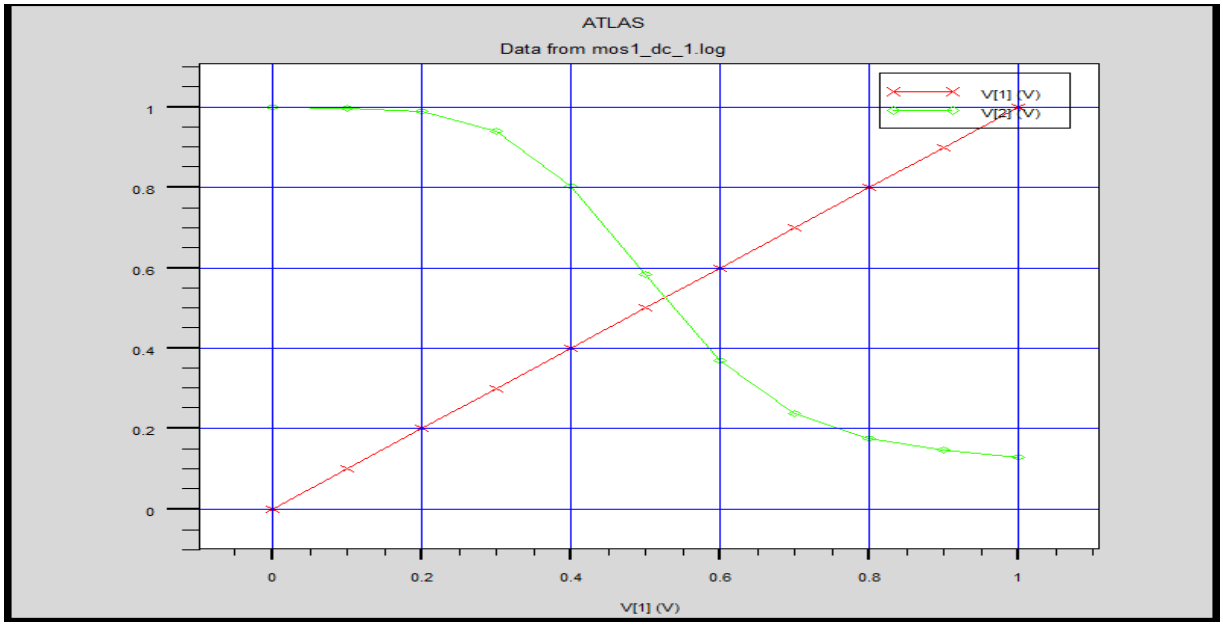


(b)

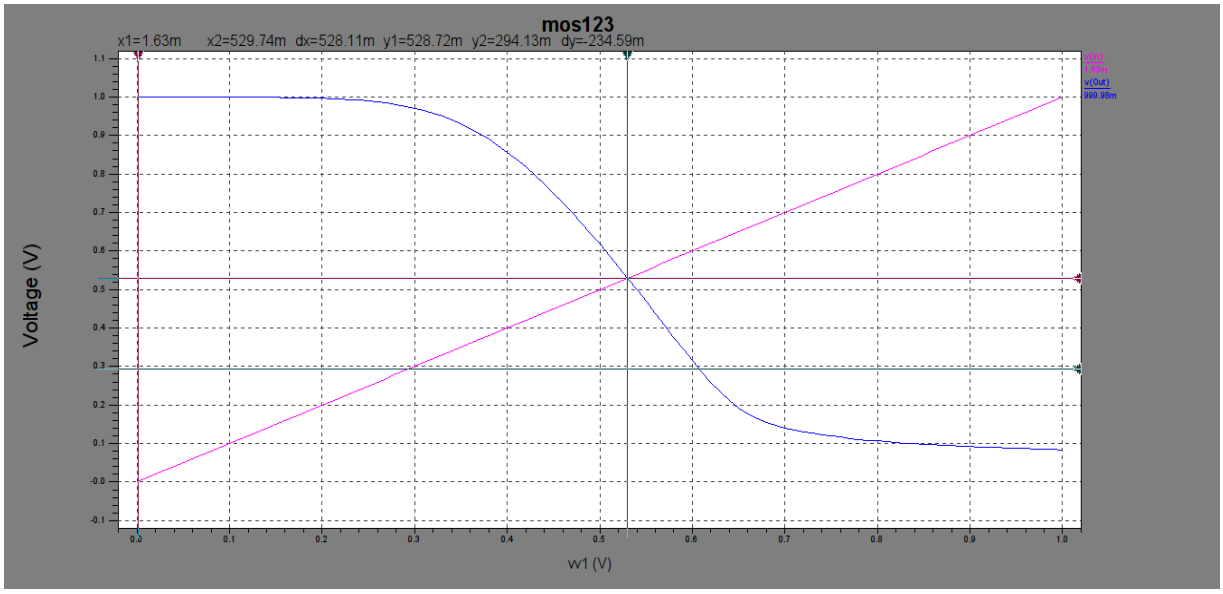
Fig. 4.5 $I_d - V_{ds}$ characteristics of 90nm n-channel NMOS with halo, Retrograde, LDD (a) Linear (b) Semilog

4.2 Resistive Load Inverter

The above designed nMOSFET is incorporated in the resistive load inverter circuit and simulated on MIXEDMODE simulator [Appendix] of Silvaco. Results have been verified with the simulation results of same circuit on T-SPICE at the same technology using BSIM model for nMOSFET. The voltage transfer characteristics of resistive load inverter on both the tool is given below.



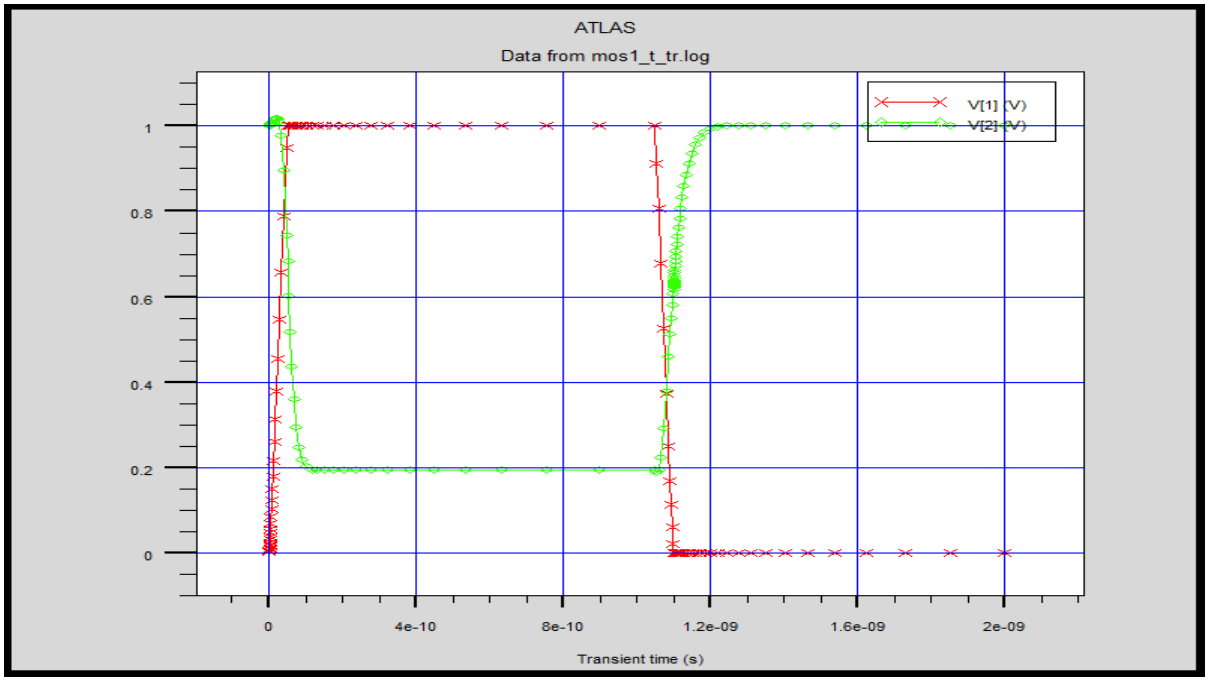
(a)



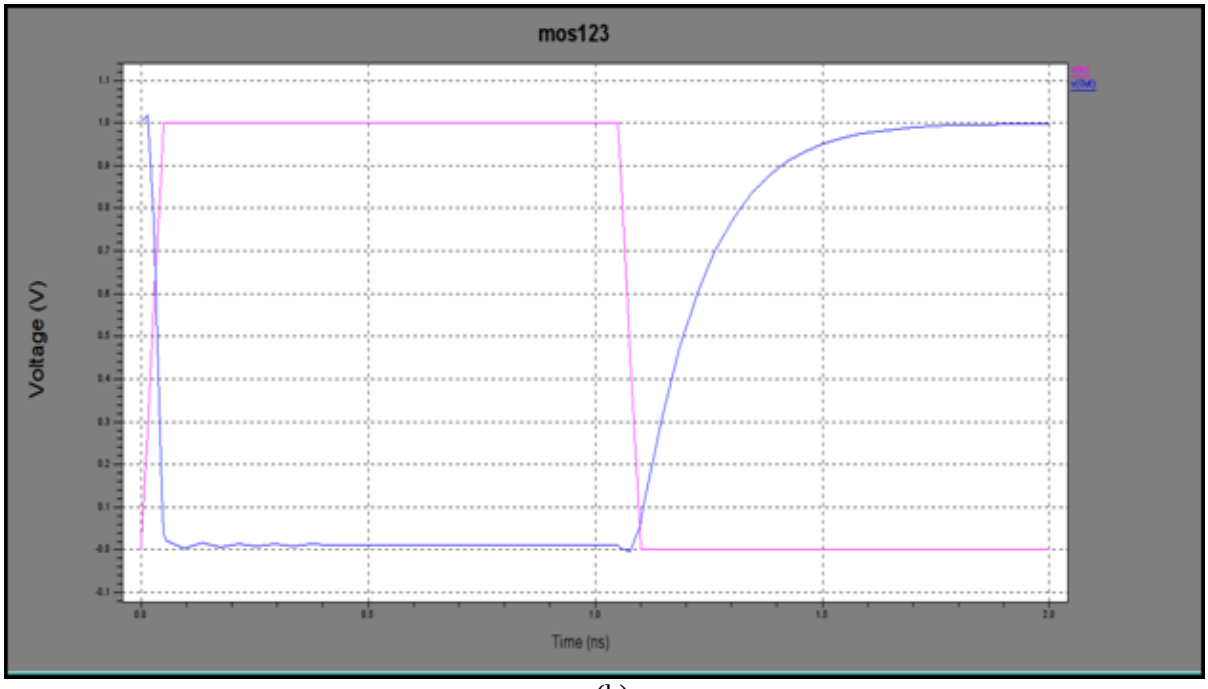
(b)

Fig. 4.6 Voltage Transfer characteristics of a Resistive load Inverter with 90nm n-channel NMOS on (a)MIXEDMODE (b) T-SPICE

The transient analysis also has been done and a propagation delay of 0.02 ns is obtained on mixed mode. The comparison result on both tools has been given below.



(a)



(b)

Fig. 4.7 Transient response of a resistive load inverter with 90nm n-channel NMOS on (a)MIXEDMODE (b)T-SPICE

4.3 Variation of individual parameter

Several design analysis are performed to investigate the effectiveness of advanced method to prevent the varying of the threshold voltage. These analyses are discussed in the following subsection.

4.3.1 Effect of the gate oxide thickness on the threshold voltage

Fig. 4.8 presents the influence of a change in gate oxide thickness on the main transistor parameters (threshold voltage) and is expressed per Angstrom of oxide thickness. The figure shows a decreasing value of threshold voltage with a decreasing value of gate oxide thickness. Therefore, we found that it becomes very important to have very tight control of the electrical parameters that are essential for circuit designers: threshold voltage.

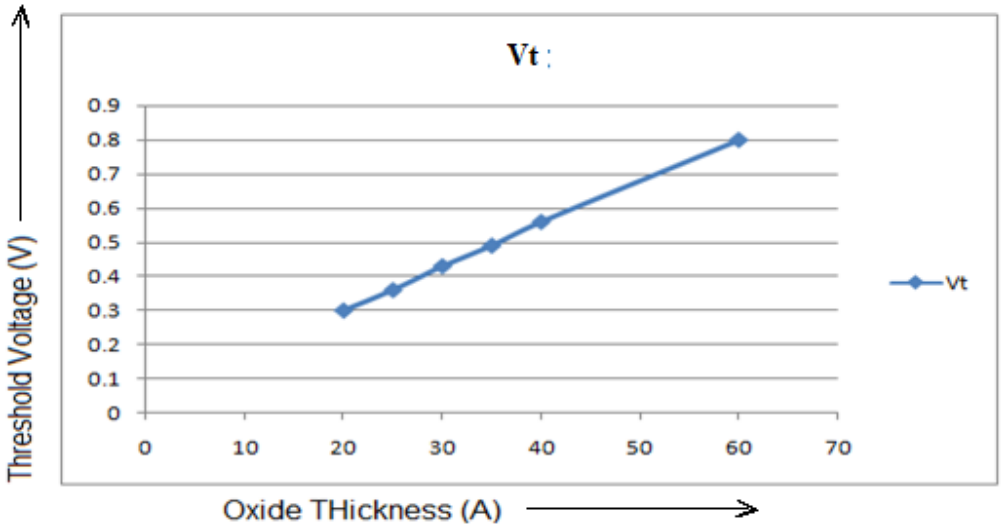


Fig. 4.8 variation of threshold voltage with oxide thickness

4.3.2 Effect of Retrograde-well to the threshold voltage:

Advanced technique such as retrograde well implant is used to suppress the short channel effect. However, this method also causes the changing of the threshold voltage. Instead of adjusting the threshold voltage using normal implantation technique, the implant dose of the retrograde well also can be used to adjust the threshold voltage to a desired value as shown in the fig. 4.9

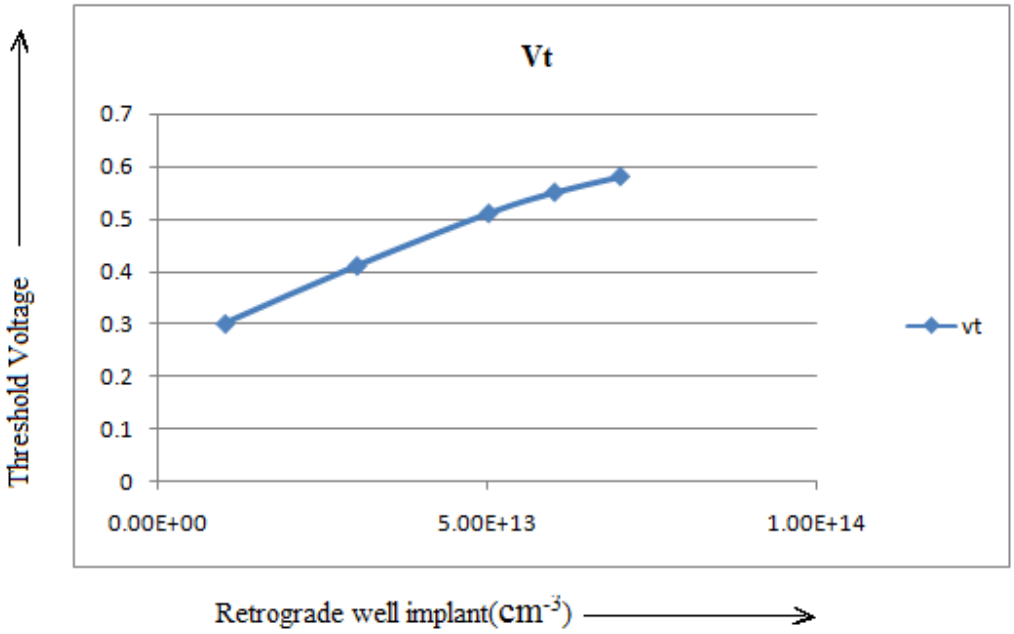


Fig. 4.9 variation of threshold voltage with Retrograde well

Effects of P-Well implant on the channel surface concentration is given below in Fig.4.10

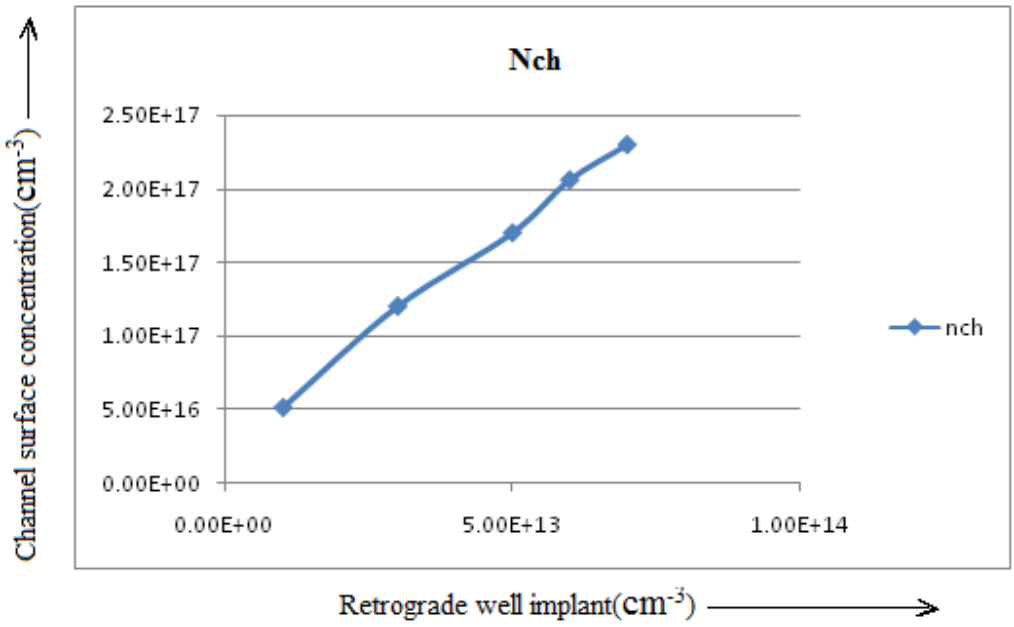


Fig.4.10 effect of P-Well implant on the channel surface concentration

4.3.3 Effect of body bias:

Figure 4.11 shows a plot of threshold voltage versus different value of substrate bias. With the increasing value of substrate bias, the threshold voltage increase.

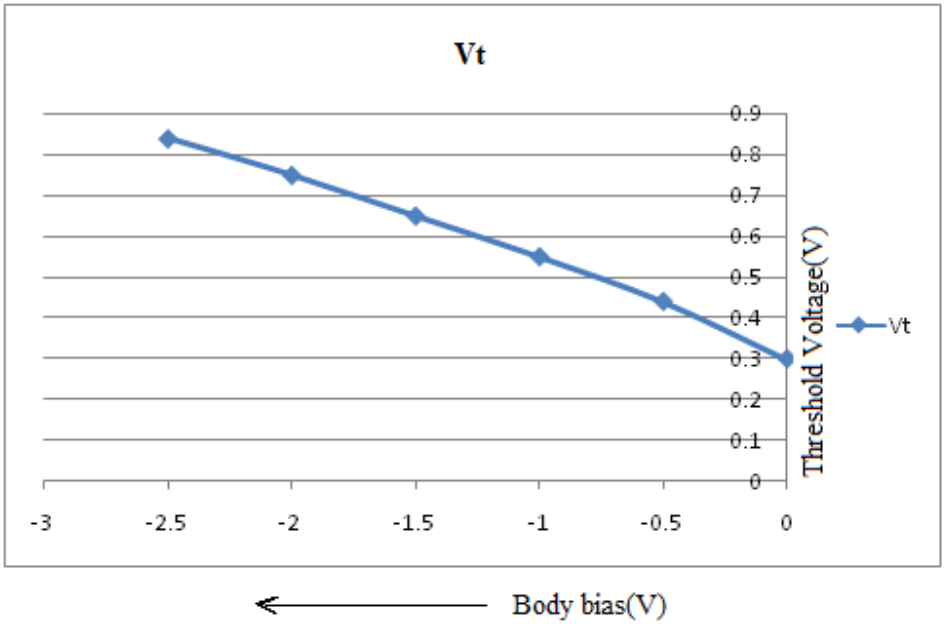


Fig. 4.11 effect of body voltage on the threshold voltage

4.4 Conclusion

A NMOS on sub-100nm channel length has been design and leakage analysis has been done on, Silvaco-Athena/Atlas package, with different types of advance techniques, like halo doping, retrograde well and LDD implant. By applying the retrograde well a leakage current of 1.27×10^{-10} A has been obtained while by adding Halo doping with the retrograde well implant a leakage current of 4.36×10^{-12} A has been obtained. Hence it can be concluded that halo doping and retrograde well techniques can be used to reduce the leakage very well. This nMOS is employed on a resistive load inverter circuit and results have been verified by T-Spice result on the same technology and a 60% improvement on propagation delay has been obtained by the transient response analysis. By using such techniques the unnecessary power consumption can be reduce and speed can be improved on device level for VLSI circuits.

4.5 Future Scope:

Today scaling has progressed without running into a serious obstacle. Engineering problems always overcome challenges at every generation of scaling, improving density and performance along the way. Nevertheless, IC products demand the highest performing and cost effectiveness transistor at each generation, making chip manufacturers bounded to find the best solution possible. In addition, as we approach the physical limits of MOSFET scaling, research on other alternatives to conventional device and process is accelerating. Some of the techniques under intense investigation are Silicon On Insulator (SOI), high-k gate dielectric and gate stack engineering, and non-planar MOSFET. These device structures will further improve the functionality of MOSFET even at nanoscale level.

APPENDIX

A1. ATHENA

The Two-Dimensional Process Simulation Framework is a comprehensive software tool for modeling semiconductor fabrication processes, provides facilities to perform efficient simulation analysis. It combines high temperature process modeling such as impurity diffusion and oxidation and lithography simulation in a single, easy to use framework.

ATHENA is also frequently used in conjunction with the device simulator. ATHENA predicts the physical structures that result from processing. These physical structures are used as input by, which then predicts the electrical characteristics associated with specified bias conditions. Using ATHENA and ATLAS makes it easy to determine the impact of process parameters on device characteristics.

The Value of Physically-Based Simulation

Physically-based process simulators predict the structures that result from specified process sequences. This is done by solving systems of equations that describe the physics and chemistry of semiconductor processes.

Physically-based simulation provides three major advantages: it is predictive, it provides insight, and it captures theoretical knowledge in a way that makes this knowledge available to non-experts.

Physically-based simulation has become very important for two reasons. One, it's almost always much quicker and cheaper than performing experiments. Two, it provides information that is difficult or impossible to measure

Physically-based process simulation tools users must specify the problem to be simulated. Users specify the problem by defining the following:

- The initial geometry of the structure to be simulated.
- The sequence of process steps (e.g., implantation, etching, diffusion, exposure) that are to be simulated.

•The physical models to be used.

A2. ATLAS

ATLAS provides general capabilities for physically-based two (2D) and three-dimensional (3D) simulation of semiconductor devices. If you're new to ATLAS

The Nature of Physically-Based Simulation

ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws, onto this grid you can simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modeled in DC, AC or transient modes of operation.

There are three physically-based simulations like ATHEA. These are

- It is predictive.
- It provides insight.
- It conveniently captures and visualizes theoretical knowledge

ATLAS, specify device simulation problems by defining

- The physical structure to be simulated.
- The physical models to be used.
- The bias conditions for which electrical characteristics are to be simulated

A3. MIXEDMODE

MIXEDMODE is a circuit simulator that can include elements simulated using device simulation and compact circuit models. It combines different levels of abstraction to simulate relatively small circuits where compact models for single devices are unavailable or sufficiently accurate. MIXEDMODE also allows to you do multi-device simulations. MIXEDMODE uses advanced numerical algorithms that are efficient and robust for DC, transient, small signal AC and small signal network analysis.

MIXEDMODE is typically used to simulate circuits that contain semiconductor devices for accurate compact models that don't exist or circuits where devices play a critical role must be modeled accurately. MIXEDMODE circuits can include up to 200 nodes, 300 elements, and up to ten numerical simulated ATLAS devices. These limits are reasonable for most applications. But, they can be increased in custom versions on request to Silvaco. The circuit elements that are supported include dependent and independent voltage and current sources as well as resistors, capacitors, inductors, coupled inductors, MOSFETs, BJTs, diodes, and switches. Commonly used SPICE compact models are available. The SPICE input language is used for circuit specification.

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