MODELING, ANALYSIS AND SIMULATION OF POLY-PHASE BOOST CONVERTER

Thesis submitted in partial fulfillment of the requirements for the award of degree of

Master of Engineering
In
Power Systems and Electric Drives

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CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled, **Modelling, Analysis and Simulation of Poly-phase Boost Converter"** in partial fulfillment of the requirements for the award of degree of Master of Engineering in *Power Systems and Electric Drives* submitted in *Electrical and Instrumentation Engineering Department* of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Mr. S.S.S.R. Sarathbabu Duvvuri, Lecturer, EIED** and refers other researcher's work which are duly listed in the reference section. The matter presented in the thesis has not been submitted for award of any other degree of this or any other University, except as reported in text and references.

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Praveen Kumar Singh

ABSTRACT

The objective of this project is to design Poly-phase boost converter which overcomes the problem of high input ripple current and output ripple voltage Digital control is more convenient for such a topology on account of the requirement of synchronization , phase shift operation , current balancing etc.

This project deals on analysis and implementation of four phase boost converter, each is a 35W unit and switched at 100 KHz. The waveforms are observed using MATLAB Simulink.

The following advantages are obvious in the proposed converter:

• Output capacitor is rated for lower ripple current and higher ripple frequency (nfs).

• Source current has higher ripple and at higher frequency (nfs).

• Another no obvious advantage is that the Poly-phase Converter may be operated with less number of stages when the load current is low. This will lead to operation under CCM at light load as well as better efficiency.

Simulation results are presented for open-loop and closed-loop for four phase boost converter. This control scheme is applicable for PFC rectifiers as well. Thus a comparative analysis based on the obtained results is performed.

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Symbol	Definition	Unit
V_g	DC Input Voltage Source	V
V_S	Voltage Source	V
V_O	Output Voltage	V
P_O	Output Power	W
P_{in}	Input Power	W
E_L	Energy Stored in Inductor	J
E_C	Energy Stored in Output Capacitor	J
I_L	Inductor Current	A
I_{LOAD}	Load Current	A
I_{in}	Input Current	A
I_g	Source Current	A
I_O	Output Current	A
i_D	Diode Current	A
F_S	Switching Frequency	Hz
T_S	Switching Period	Sec
D	Duty Ratio	---
N	Number of Converters in Parallel	---
η	Efficiency	---
C	Capacitor Value	F
L	Inductor Value	H
r_L	Inductor Resistance	Ω
r_C	Capacitor Resistance (ESR)	Ω
R	Load Resistance	Ω

$Z_O(s)$	Output Impedance	Ω
V_{ref}	Reference Voltage	V
$\hat{v}_o$	Small Signal Variation in Output Voltage	V
$\hat{v}_g$	Small Signal Variation in Input Voltage	V
$\hat{i}_g$	Small Signal Variation in Input Current	A
$\hat{d}$	Small Signal Variation in Duty Ratio	---
K_P	Proportional Coefficient	---
K_i	Integral Coefficient	---

CHAPTER 1
INTRODUCTION

1.1 Overview

Boost dc-to-dc converters have very good source interface properties. The input inductor makes the source current smooth and hence these converters provide very good EMI performance. On account of this good property, the boost converter is also the preferred converter for off-line UPF rectifiers.

One of the issues of concern in these converters is the large size of the storage capacitor on the dc link. The boost converter suffers from the disadvantage of discontinuous current injected to the load. The size of the capacitor is therefore large. Further, the ripple current in the capacitor is as much as the load current; hence the ESR specification of the tank capacitor is quite demanding. This is especially so in the emerging application areas of automotive power conversion, where the input voltage is low (typically 12V) and large voltage boost (4 to 5) are desired.

In the UPF rectifier applications, the input voltage varies from zero to maximum value twice in every cycle of the ac input voltage. The duty cycle therefore varies in the full range of zero to one. The inductor current varies from zero to rated current twice in every ac cycle of the input current. On account of these wide operating point variations, the design of the power circuit as well as the closed loop controller is a demanding task. The poly-phase operation of boost converter to overcome the disadvantages of large size storage capacitor in boost converter and off-line UPF rectifiers and a small signal analysis of N converters in parallel to an equivalent second order system in such converters. In designing DC converters, parameters such as ratio of energy stored in inductor and capacitor to energy delivered to load in one period, maximum current in the switch and the value of the rms current in the output capacitor have great importance.

One-way of reducing the storage requirement is increasing the switching frequency however this is not practicable in all instances. During the on state of the switch, the capacitor has to supply the load current in the boost converter and this discontinuity of current in the capacitor increases the rms value of current and also increases the amount of capacitor which is needed for correct operation of the circuit and therefore it results in more dissipation due to ESR of capacitor. In standard designs it is not uncommon to see tank capacitors one or two orders of magnitude higher than the ideally required capacitance A way to overcome this problem is using poly-phase operation with appropriate phase shift in the control circuit of

main switches. This is done in such a way that at anytime one of the inductors is supplying the load current. The frequency of ripple current in the output capacitor is n times compared to the single stage and therefore the value of the capacitor required can be reduced. Extracting continuous current from the input for applications such as unity power factor is usually the reason for choosing boost converter configuration. An advantage of using poly-phase converter is in light load operation.

1.2 Literature Survey

R.Mirzaei and V.Ramanarayanan discussed about the poly-phase boost converter, which overcomes the problem of high ripple current in the tank capacitor. Digital control is more convenient for such a topology on account of the requirement of synchronization, phase shifted operation, current balancing etc. [1].

Laszlo Balogh and Richard Redl discussed about the operation and design trade-offs of the interleaved boost converter in continuous inductor-current mode in a high power factor pre regulator circuit. By using interleaved converters an overall reduction of boost inductor and EM1 filter volume can be achieved, together with reduced switching losses [2]-[3].

Roberto Giral, Luis Martinez-Salamero and Sigmond Singer discussed about a converter family generated by connecting N-identical boost converters in parallel is presented. The proposed control uses interleaving techniques based on a binary state-transition diagram [4].

I.Cadirci, A.Yafavi and M. Ermis discussed about the Unity power factor boost converter with phase shifted parallel IGBT operation for medium power applications [5].

Dragan MaksimoviC, Regan Zane and Robert Erickson discussed about the impact of digital control in high-frequency switched-mode power supplies (SMPS),including point-of-load and isolated DC-DC converters, microprocessor power supplies, power-factor-correction rectifiers, electronic ballasts, etc., where switching frequencies are typically in the hundreds of kilohertz to megahertz range [6].

Jingquan Chen, Aleksandar Prodic and Robert W. Erickson discussed about the predictive digital current programmed control for valley, peak or average current. The control laws are derived for the three basic converters: buck, boost, and buck–boost [7].

Souvik Chattopadhyay and Somshubhra Das discussed about a simple digital current mode control technique for dc-dc converters. It has been shown that we can implement any one of the average, peak and valley current mode controls by adjustment of the sampling instant of the inductor current with respect to the turn on instant of the switch [8].

Slobodan Cuk *et al.* [9] have presented a new concept in the design of switched-mode power conversion circuitry. Because of its extreme simplicity, flexibility, and efficiency it has the potential to replace some conventional electrical power processing methods currently in use.

Peng Li et al. [10] have proposes a new current sharing method which is based on current mode controlled dc–dc converters and achieved the current sharing by forcing all inner current loops to have the same current reference. They also recognize both the benefits and limitations of master-slave methods and the methods using the inherent current source properties of CMC converters.

Yuri Panov and Milan M. Jovanovic have consider Stability and dynamic performance of the CS control. The parallel operation of voltage regulator modules (VRMs) for high-end microprocessors requires a current-sharing (CS) circuit to provide a uniform load distribution among the modules [11].

Isao Matsuura *et al.* [12] have made a comparison of the efficiencies of active and passive soft switching methods for PWM converters. A boost converter was built and tested under the static and dynamic PFC operation condition as well as DC-DC operation condition and found that the passive method has better efficiency in the high power operation region, while the active method outperforms the passive method in the low power region.

Praveen Jain *et al.* [13]-[14] have proposed a novel, zero-voltage switched (ZVS) PWM boost converter that combines soft-switching with constant frequency operation. The converter can be operated with PWM control at a fixed frequency because ZVS operation is achieved with a simple auxiliary resonant circuit that is activated for only a small fraction of the switching period and handles much less power than the main power circuit.

Cliludio M. C. Duarte and Ivo Barbi have introduced a new family of ZVS-PWM active-clamping DC-to-DC boost converters. The technique presents ZVS commutation without additional voltage stress and a significant increase in the circulating reactive energy

throughout the converters so the efficiency and the power density become advantages when compared to the hard-switching boost converter [15], [23].

Milan M. Jovanovic has described a circuit technique that reduces the boost-converter losses caused by the reverse recovery characteristics of the rectifier. The losses are reduced by inserting an inductor in the series path of the boost switch and the rectifier to control the di/dt rate of the rectifier during its turn-off. The energy from the inductor after the boost switch turn-off is returned to the input or delivered to the output via an active snubber [16], [19].

K. Mark Smith *et al.* [17] have conducted a comparison study to characterize the loss mechanisms, component stresses, and overall efficiencies of a group of voltage-mode soft-switching pulse width modulation (PWM) methods. They found that only those methods that softly switch the auxiliary switches, minimize redirection current and recover the auxiliary circuit energy over most of the load range.

Ching-Jung Tseng and Chern-Lin Chen have proposed an active snubber cell is to contrive zero voltage-transition (ZVT) pulse width-modulated (ZVT-PWM) converters. Except for the auxiliary switch, all active and passive Semi-conductor devices in a ZVT-PWM converter operates at zero-voltage-switching (ZVS) turn on and turn off [18].

Tae-Woo Kim *et al.* [20] have proposed an Improved ZVT-PWM boost converter. The main switch of the conventional ZVT-PWM converter is always switched at zero voltage. But the auxiliary switch is turn-off with switching loss due to hard switching condition. The proposed converter is reducing the turn-off switching loss of the auxiliary switch by using additional circuit.

Nikhil Jain, Praveen Jain and Geza Joos have presented a Zero-Voltage-Transition (ZVT) boost converter using a soft switching auxiliary circuit. The improvement over existing topologies lies in the structure and position of the auxiliary circuit capacitors and the subsequent reduction in the main switch resonant current. They analyzed the operation of this converter and presented the characteristic curves [21].

Bo Feng *at el.* [22] have proposed a PFC converter employing compound active clamping technique. It can effectively reduce the loss caused by diode reverse recovery. The parasitic oscillation caused by the parasitic capacitance of the boost diode is eliminated. The

maximum voltage stress of switches and the soft-switching region with relation to the resonant inductor and resonant capacitance are investigated.

M. Veerachary has presented a systematic development of a unified signal flow graph model for an interleaved boost converter with coupled inductor system operating in continuous current mode. This signal flow graph approach provides a means to directly translate the switching converter to its graphic model, from which steady-state and dynamic behaviour of the converter can be studied [24], [26].

Pekik A. Dahono *et al.* [25] have presented an output ripple analysis of multiphase dc-dc converters that having an output LC filter and derived analytical expressions for the output voltage ripple of two- and three-phase dc-dc converters. Influence of the coupling coefficient of the output filter inductor on the output ripple is investigated. They also presented a comparative evaluation of single-phase, two-phase, and three-phase dc-dc converters.

Po-Wa Lee *et al.* [27] have investigated and proposed a converter consisting of two interleaved and inter-coupled boost converter cells. The boost converter cells have very good current sharing characteristics even in the presence of relatively large duty cycle mismatch. They designed it to have small input current ripple and zero boost-rectifier reverse-recovery loss. They also presented the operating principle, steady-state analysis, and comparison with the conventional boost converter.

Anthony Kelly *et al.* [29] have introduced a digital current-mode controller for dc-dc converters. The current-mode loop is sensor-less, relying on constants and internal loop states, removing the need to sense controlled voltages or currents for the inner loop. They also implemented a fast current-mode control mechanism by utilizing dead-beat control.

Dwaraka S. Padimiti and Mehdi Ferdowsi have reviewed and summarized different digital control techniques, including predictive control and dead-beat control technique. Advantages and disadvantages of each method are analyzed by them and their benefits to EVs/HEVs are investigated. They also discussed a predictive digital control method that works well in both continuous and discontinuous mode [30].

Chien-Ming Wang has proposes a new single-phase high power-factor rectifier, which features regulation by conventional pulse width modulation (PWM), soft commutation, and instantaneous average line current control. A new zero-current switching PWM (ZCS-PWM)

auxiliary circuit is configured in the presented ZCS-PWM rectifier to perform ZCS in the active switches and zero-voltage switching (ZVS) in the passive switches [31]-[32].

1.3 Objective of work

The main objective of the present work is to design the Poly-phase Boost Converter, which overcomes the problem of high ripple current in the tank capacitor. Digital control is more convenient for such a topology on account of the requirement of synchronization, phase shifted operation, current balancing etc.

1.4 Organization of Thesis

The thesis is organized into six chapters. The organization of chapters is as follows:

Chapter-1 summarized the overview of the problem, brief literature review, objective of work and organization of the thesis.

Chapter-2 highlights the topic boost converter and its mathematical modeling, it also gives the overview of various related aspects of boost converter and its perspectives.

Chapter-3 explores the digital control of poly-phase boost converter, its methodology and overview aspects.

Chapter-4 presents the software implementation of poly-phase boost converter using MATLAB/Simulink power systems block-set.

Chapter-5 shows the simulation results and analysis of the results i.e. for single and poly-phase boost converter.

Chapter-6 presents the conclusions drawn and also presents the future scope of work followed by reference section.

CHAPTER 2
MATHEMATICAL MODEL OF BOOST CONVERTER

2.1 Introduction

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

2.2 Boost Converter

A boost converter regulates the average output voltage at a level higher than the input or source voltage. For this reason the boost converter is often referred to as a step-up converter or regulator. The DC input voltage is in series with a large inductor acting as a current source. A switch in parallel with the current source and the output is turned off periodically, providing energy from the inductor and the source to increase the average output voltage. The boost converter is commonly used in regulated DC power supplies and regenerative braking of DC motors.

2.3 Ideal Boost Circuit

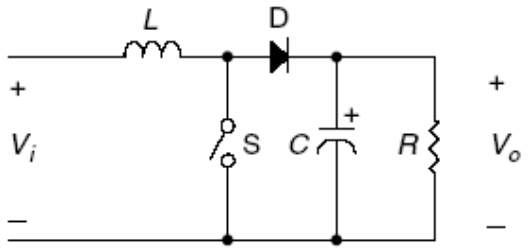

Fig 2.1 Basic boost Converter

The circuit that models the basic operation of the boost converter is shown in Fig2.1 The input voltage in series with the inductor acts as a current source. The energy stored in the inductor builds up when the switch is closed. When the switch is opened, current continues to flow through the inductor to the load. Since the source and the discharging inductor are both providing energy with the switch open, the effect is to boost the voltage across the load. The load consists of a resistor in parallel with a filter capacitor. The capacitor voltage is larger

than the input voltage. The capacitor is large to keep a constant output voltage and acts to reduce the ripple in the output voltage.

2.4 TYPES OF CONDUCTION MODE

There are basically two types of conduction modes which are described as:

2.4.1 Continuous-Conduction Mode

The continuous-conduction mode of operation occurs when the current through the inductor in the circuit of Fig 2.1 is continuous with the inductor current always greater than zero. The operation of the circuit in steady state consists of two states, as illustrated in Fig 2.2.

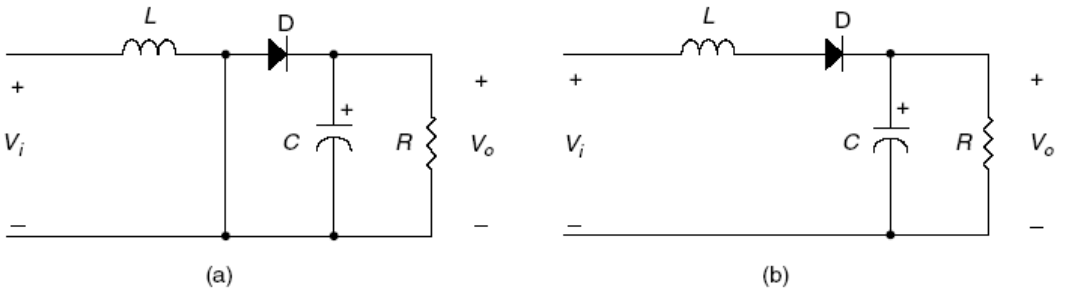

Fig 2.2 Basic boost converter switch states: (a) switch closed; (b) switch open.

The first state with the switch closed has current charging the inductor from the voltage source. The switch opens at the end of the on-time and the inductor discharges current to the load with the input voltage source still connected. This results in an output voltage across the capacitor larger than the input voltage. The output voltage remains constant if the RC time constant is significantly larger than the on-time of the switch. When a boost converter operates in continuous mode, the current through the inductor (I_L) never falls to zero.

$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{2.1a}$$

Or,
$$D = 1 - \frac{V_i}{V_o} \tag{2.1b}$$

From the above expression it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D, theoretically to infinity as D approaches 1. This is why this converter is sometimes referred to as a *step-up* converter.

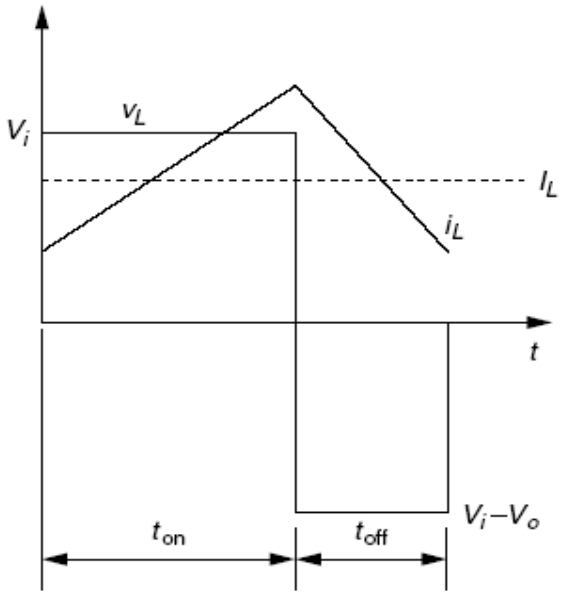

Fig 2.3 Inductor voltage and current waveforms for Continuous mode of boost converter

A representative set of inductor voltage and current waveforms for the continuous conduction mode is shown in Fig 2.3 The voltage ratio for a boost converter is derived based on the time-integral of the inductor voltage equal to zero over one switching period. The voltage ratio is equivalent to the ratio of the switching period to the off-time of the switch as illustrated by Eq. (2.1c)

$$\frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{T_s}{t_{off}} = \frac{T_s}{T_s - t_{off}} = \frac{T}{1-D} \tag{2.1c}$$

The current ratio is derived from the voltage ratio assuming that the input power is equal to the output power, as with ideal transformer analysis.

2.4.2 Discontinuous-Conduction Mode

The discontinuous mode of operation occurs when the value of the load current is less than or equal to zero at the end of a given switching period. Assuming a linear rise and fall of current through the inductor, the boundary point between continuous- and discontinuous-current conduction occurs when the average inductor current over one switching period is half the peak value, as illustrated in Fig 2.4. The average inductor current at the boundary point is calculated using Eq. (2.2)

$$I_{LB} = \frac{1}{2} i_{L(peak)} = \frac{V_o T_s}{2L} D(1-D) \tag{2.2}$$

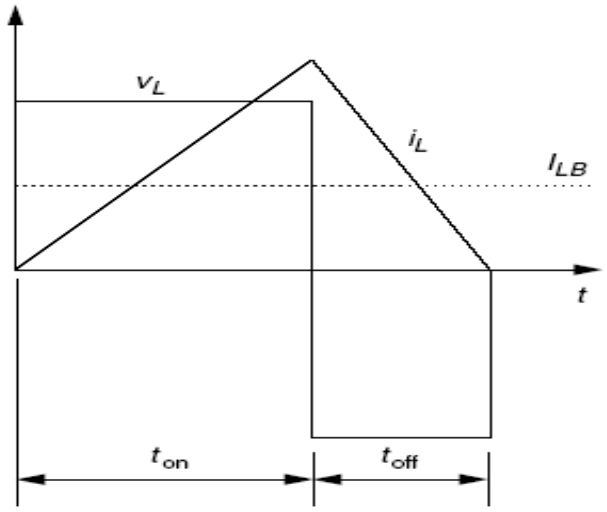

Fig 2.4 Inductor current at boundary point for discontinuous mode of Boost converter

The output current at the boundary condition is derived by using the current ratio of Eq. (2.1) in Eq. (2.2) with the inductor current equal to the input current. This results in Eq. (2.3)

$$I_{OB} = \frac{V_O T_S}{2L} D(1-D)^2 \tag{2.3}$$

For the boost converter in discontinuous mode, the output voltage *Vo* is generally kept constant while the duty ratio *D* varies in response to changes in the input voltage *Vi*.

The duty ratio is defined as a function of the output current for various values of the voltage ratio according to Eq. (2.4)

$$D = \left[\frac{4}{27} \frac{V_o}{V_i} \left(\frac{V_o}{V_i} - 1 \right) \frac{I_o}{I_{ob(\max)}} \right]^{\frac{1}{2}} \tag{2.4}$$

2.5 Output Voltage Ripple

The peak-to-peak voltage ripple for the boost converter in Fig 1.1 for the continuous conduction mode can be calculated for a specified value of output capacitance by calculating the additional charge ΔQ provided by the ripple current in the inductor. This analysis is similar to that discussed for the buck converter. The peak-to-peak voltage ripple is calculated by taking the area under the inductor current i_L (the additional charge ΔQ) and dividing by the capacitance resulting in Equation (1.5)

$$\Delta V_O = \frac{\Delta Q}{C} = \frac{I_O D T_S}{C} = \frac{V_O}{R} \frac{D T_S}{C} \tag{2.5}$$

The percentage output voltage ripple is calculated as in Equation (2.6)

$$\frac{\Delta V_O}{V_O} = \frac{DT_S}{RC} = D\frac{T_S}{\tau} \tag{2.6}$$

Where, τ is the RC time constant of the output filter. The voltage ripple is minimized by increasing the time constant of the output filter.

2.6 Need for Poly-phase Operation

In designing DC converters, parameters such as ratio of energy stored in inductor and capacitor to energy delivered to load in one period, maximum current in the switch and the value of the RMS current in the output capacitor have great importance and it is necessary to be considered.

V_{dc}=1, D=0.5, T_s=1, E_o=1, P_o=1, $\Delta I_L / I_L$ =20%, ΔVo/Vo=1%

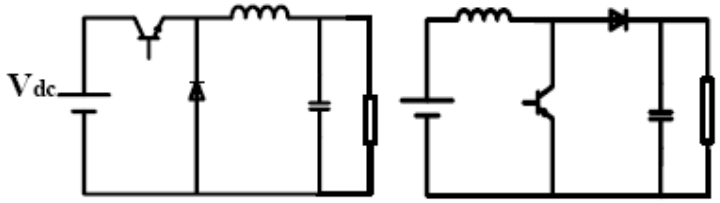

Fig2.5 Buck & Boost Converter respectively

Table 2.1 gives the reactive elements and their energy storage capacity for the basic converters. From the table it is obvious that the boost converter requires total energy storage far in excess of buck converter.

Table 2.1 Comparing Buck & Boost Converters (per unit values)

	L (p.u.)	C (p.u.)	Vo (p.u.)	$\frac{E_L}{P_O T_S}$	$\frac{E_C}{P_O T_S}$
BOOST	2.5	12.5	2	1.25	25
BUCK	1.25	10	0.5	1.25	1.25

One-way of reducing the storage requirement is increasing the switching frequency however this is not practicable in all instances. During the on state of the switch, the capacitor has to supply the entire load current in the boost converter; this discontinuity of current in the capacitor increases the RMS value of current and also increases the amount of capacitor which is needed to keep the ripple voltage low. The power dissipation in the ESR of the capacitor is also high. In standard designs it is not uncommon to see tank capacitors one or

two orders of magnitude higher than the ideally required capacitance A way to overcome this problem is using poly-phase operation with appropriate phase shift in the control circuit of main switches.

2.7 Proposed Converter

Fig 2.6 shows such a poly-phase boost converter (N=4). Fig. 2.7 shows the conduction intervals of the four switches in the converter. It is seen that at any time at least one of the converters is supplying the load in addition to the capacitor. The frequency of ripple current in the output capacitor is N times compared to the single stage and therefore the value of the capacitor required can be reduced. The same circuit topology is also applicable to UPF rectifiers.

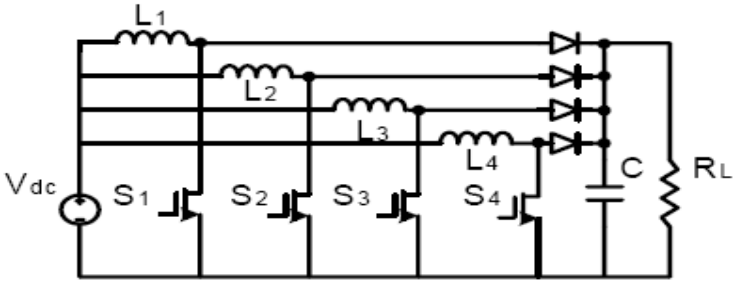

Fig 2.6 Poly-phase Boost Converter(N=4)

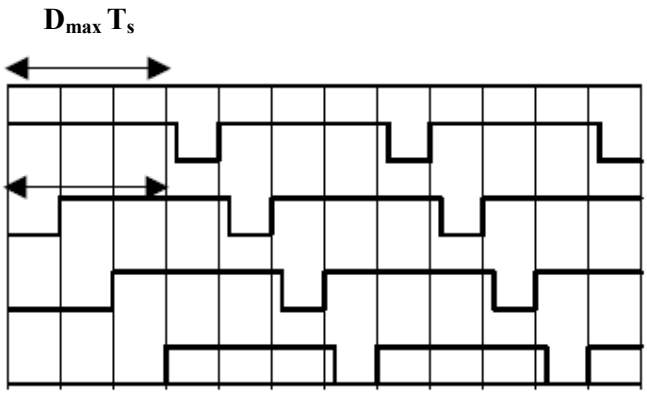

Fig 2.7 The case with $D_{max} \geq 1- 1/4$

In such a scheme, the following advantages are obvious.

• Output capacitor is rated for lower ripple current and higher ripple frequency (nfs).

• Source current has higher ripple and at higher frequency (nfs).

• Another no obvious advantage is that the poly-phase converter may be operated with less number of stages when the load current is low. This will lead to operation under CCM at light load as well as better efficiency.

The control of poly-phase converters has to possess several features such as

• High speed of switching (typically 100KHz).

• Synchronization (typically up to 16 converters).

• Current control (for better protection).

• Selective topology masking (for variable load operation).

2.8 Steady state waveforms

The boost converter steady state waveforms are shown in Fig below:

2.8.1 Voltage gain

By applying volt-sec balance on inductor.

$$V_O = \frac{V_g}{1-d} \tag{2.7}$$

When the parasitic resistance of the inductor (R_l) and the source resistance (Rg) are taken into account, the voltage gain gets degraded.

$$V_O = \frac{V_g}{1-d}\left\{\frac{1}{1+\frac{\alpha}{(1-d)^2}}\right\}; \alpha = \frac{R_1 + R_g}{R} \tag{2.8}$$

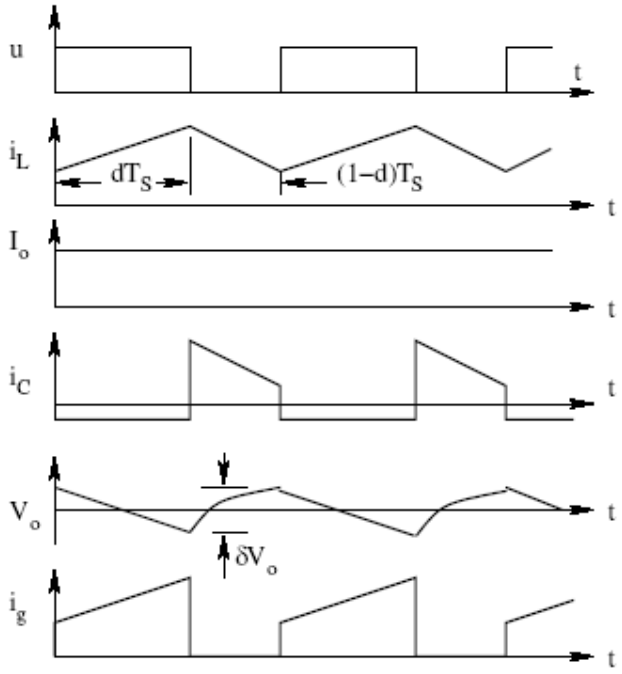

Fig 2.8 Steady State Waveforms of the Boost Converter

2.8.2Current Ripple

In each sub-period [dTs and (1-d)Ts] the rate of change of current is constant.

$$\delta I_L = \frac{V_g d T_S}{L} \tag{2.9}$$

$$\frac{\delta I_L}{I_L} = \delta_i = \frac{d\left(1-d\right)^2 R T_S}{L} \tag{2.10}$$

2.8.3 Voltage Ripple

The charging and discharging current of the capacitor decides voltage ripple. We consider that the entire ac part of the inductor current flows into the capacitor.

$$\delta V_O = \frac{\delta Q}{C} = \frac{I_O d T_S}{C} \tag{2.11}$$

$$\frac{\delta V_O}{V_O} = \delta V = \frac{d T_S}{RC} \tag{2.12}$$

2.8.4 Input Current

The average of the inductor current is the same as the average source current.

$$I_g = \frac{I_O}{1-d} \tag{2.13}$$

2.9 Dynamic and Output Equations of the Converter

The converter consists of linear circuit elements L, C, R as well as non-linear circuit elements, which are switches. The converter as such is not a linear system. However the circuit obtained in the converter for each of the switch options in the converter is a linear circuit. Therefore, it is possible to write the dynamic and output equations of the circuit for each of the switch positions.

Each energy storage element (inductors and capacitors) is a dynamic element of the converter. A dynamic variable is associated with each energy storage element of the converter. The inductor current is a dynamic variable and so also the capacitor voltage. There will be as many dynamic variables for the converter as there are energy storage elements in the converter. By dynamic equations of the converter is meant the equations, which relate the rate of change of dynamic variables, inputs and the parameters of the converter.

The equation relating the output(s) of the converter to the dynamic variables of the converter is the output equation of the converter. The first step in the dynamic modeling of the converter is to write down the dynamic and output equations of the converter for the circuits obtained in the converter for each of the switch positions in the converter.

During ON time,

$$\dot{x} = A_1 x + b_1 v_g \tag{2.14}$$

$$v_o = q_1 x \tag{2.15}$$

During OFF time,

$$\dot{x} = A_2 x + b_2 v_g \tag{2.16}$$

$$v_o = q_2 x \tag{2.17}$$

Equations (2.15) & (2.17) are referred to as the output equations. Equations (2.14) & (2.16) are referred to as the dynamic equations or the state equations of the converter for each of the sub-periods of the switching period.

2.10 Averaged model of the converter

The converter alternates between the two-switched states at high frequency. We wish to represent the converter through a single equivalent dynamic representation, valid for both the ON and OFF durations. If we consider that the variation of the dynamic variables over a switching period, then

$$x = \dot{x}_{avg}\, Ts = \dot{x}_{dTs}\, dTs + \dot{x}_{(1-d)Ts}(1-d)Ts \tag{2.18}$$

where, Xavg is the average rate of change of dynamic variables over a full switching period. The above equivalent description is valid if XdTs and X(1-d)Ts are constant during the ON and OFF duration respectively. This will be valid assumption if the ON and OFF durations are much less compared to the natural time constants of the respective circuits. Then for the averaged dynamic variables,

$$\dot{x}_{avg} = Ax + bv_g + ev_T + nv_D \tag{2.19}$$

$$v_o = qx \tag{2.20}$$

$$A = A_1 d + A_2(1-d); b = b_1 d + b_2(1-d); e = e_1 d + e_2(1-d); \tag{2.21}$$

$$n = n_1 d + n_2(1-d); q = q_1 d + q_2(1-d); \tag{2.22}$$

Since the averaging process has been done over a switching period, the equivalent model is valid for time durations much larger compared to the switching period (or valid for frequency variations much smaller than the switching frequency). As a thumb rule the equivalent model may be taken to be a good approximation of the real converter for a dynamic range of about a tenth of the switching frequency.

Steady state solution

The steady state solution is obtained by equating the rate of change of dynamic variables to zero.

$$0 = Ax + bv_g + ev_T + nv_D \tag{2.23}$$

$$X = A^{-1}\left(bv_g + ev_T + nv_D\right) \tag{2.24}$$

$$V_o = qA^{-1}\left(bv_g + ev_T + nv_D\right) \tag{2.25}$$

The steady state solution of the boost converter is given below. For the sake of simplicity, the converter is taken to be ideal. It may be verified that the averaged model is

$$\dot{x} = Ax + bv_g \tag{2.26}$$

$$V_o = \frac{q}{x} \tag{2.27}$$

$$\dot{x} = \begin{pmatrix} \frac{di_1}{dt} \\ \frac{dv_C}{dt} \end{pmatrix}; A = \begin{bmatrix} 0 & -\frac{1-D}{L} \\ \frac{1-D}{C} & -\frac{1}{RC} \end{bmatrix}; b = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} q = \begin{bmatrix} 0 & 1 \end{bmatrix} \tag{2.28}$$

The steady state solution is

$$X = -\frac{A^{-1}}{\left(b/V_g\right)} \tag{2.29}$$

$$V_o = \frac{q}{X} \tag{2.30}$$

$$A^{-1} = \frac{LC}{(1-D)^2}\begin{bmatrix} -\frac{1}{RC} & -\frac{1-D}{L} \\ \frac{1-D}{C} & 0 \end{bmatrix} \tag{2.31}$$

$$\begin{bmatrix} I_l \\ V_o \end{bmatrix} = \begin{bmatrix} \dfrac{V_g}{R(1-D)^2} \\ \dfrac{V_g}{1-D} \end{bmatrix} \tag{2.32}$$

$$V_O = \frac{V_g}{1-D} \tag{2.33}$$

2.11 Small signal model of the converter

The steady state representation of the averaged system given by the above equations though linear is not time invariant. This is because the gain matrices A, b etc. are functions of time through 'd' embedded within. Therefore it is necessary to linearise the system equations. Such a linearised model will enable us to define the different transfer functions for the converter and apply linear system theory to design closed loop controllers for the converters. We may neglect the terms containing VT and VD for this purpose. Such a step will be valid since these quantities are small (compared to Vg and Vo) and hence small variations in these small terms will only have a second order effect on the overall system. The dynamic equations are thus

$$\dot{x} = \left[A_1 d + A_2(1-d)\right]x + \left[b_1 d + b_2(1-d)\right]v_g \tag{2.34}$$

$$v_o = \left[q_1 d + q_2(1-d)\right]x \tag{2.35}$$

We may now consider that the inputs d and vg are varying around their quiescent operating points D and Vg respectively.

$$d = D + \hat{d}; \frac{\hat{d}}{D} \square \ 1; v_g = V_g + \hat{v_g}; \frac{\hat{v_g}}{V_g} \square \ 1; \tag{2.36}$$

These time varying inputs in d and vg produce perturbations in the dynamic variables x (X + ^x) and vo (Vo + ^vo).

$$\dot{X} + \dot{\hat{x}} = \left[A_1 d + A_2(1-d)\right]\left(X + \hat{x}\right) + \left[b_1 d + b_2(1-d)\right]\left(V_g + \hat{v_g}\right) \tag{2.37}$$

$$V_o + \hat{v}_o = \left[q_1 d + q_2 (1-d) \right] \left(X + \hat{x} \right) \tag{2.38}$$

$$\dot{\hat{X}} + \dot{\hat{x}} = \left[A_1 \left(D + \hat{d} \right) + A_2 \left(1 - D - \hat{d} \right) \right] \left(X + \hat{x} \right) + \left[b_1 \left(D + \hat{d} \right) + b_2 \left(1 - D - \hat{d} \right) \right] \left(V_g + \hat{v}_g \right) \tag{2.39}$$

$$V_o + \hat{v}_o = \left[q_1 \left(D + \hat{d} \right) + q_2 \left(1 - D - \hat{d} \right) \right] \left(X + \hat{x} \right) \tag{2.40}$$

The above equations may be expanded and separated into dc (steady state) terms, linear small signal terms and non-linear terms. When the perturbations in d and Vg are small, the effect of the non-linear terms will be small on the overall response and hence may be neglected.

$$0 = AX + bV_g \qquad \text{DC model} \tag{2.41}$$

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + \left[\left(A_1 - A_2 \right) X + \left(b_1 - b_2 \right) V_g \right] \hat{d} \qquad \text{Linear model} \tag{2.42}$$

The steady state solution (X) is obtained from Eqn. (2.41) and used in Eqn. (2.42) to get the following small signal dynamic model of the converter.

$$\dot{\hat{x}} = A\hat{x} + b\hat{v}_g + f\hat{d} \tag{2.43}$$

$$V_o = q\hat{x} + \left(q_1 - q_2 \right) X \hat{d} \tag{2.44}$$

$$A = A_1 D + A_2 (1-D); b = b_1 D + b_2 (1-D); q = q_1 D + q_2 (1-D); \tag{2.45}$$

$$f = \left[\left(A_1 - A_2 \right) X + \left(b_1 - b_2 \right) V_g \right]; X = A^{-1} b V_g \tag{2.46}$$

2.12 Transfer Functions of the converter

From the above linear small signal model of the converter we may define the following transfer functions of the converter.

2.12.1 Input Transfer Functions

$$\frac{\hat{x}(s)}{\hat{v}_g(s)} = \left(sI - A \right)^{-1} b \tag{2.47}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = q \left(sI - A \right)^{-1} b \tag{2.48}$$

2.12.2 Control Transfer Functions

$$\frac{\hat{x}(s)}{\hat{d}(s)} = (sI - A)^{-1} f \tag{2.49}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = q(sI - A)^{-1} f \tag{2.50}$$

Non idealities in the converter such as the winding resistance, ESR of the capacitors, switch drops etc. may be readily incorporated in this averaging method. The idealized transfer functions of the boost converter are given here.

2.13 Transfer function of Boost Converter

$$\frac{\hat{I}(s)}{\hat{v}_g(s)} = \frac{1}{R(1-D)^2} \frac{1+sCR}{\left[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}\right]} \tag{2.51}$$

$$\frac{\hat{I}(s)}{\hat{d}(s)} = \frac{V_g}{R(1-D)^3} \frac{2+sCR}{\left[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}\right]} \tag{2.52}$$

$$\frac{\hat{v}_o(s)}{\hat{v}_g(s)} = \frac{1}{1-D} \frac{1}{\left[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}\right]} \tag{2.53}$$

$$\frac{\hat{v}_g(s)}{\hat{d}(s)} = \frac{V_g}{(1-D)^2} \frac{1-s\frac{L}{R(1-D)^2}}{\left[1+s\frac{L}{R(1-D)^2}+s^2\frac{LC}{(1-D)^2}\right]} \tag{2.54}$$

CHAPTER 3
DIGITAL CONTROL OF POLYPHASE BOOST CONVERTER

3.1 Poly-phase operation

In poly-phase boost converter each stage has an independent current mode control loop, which uses the same reference current. The reference current in turn is generated by the outer voltage control loop. For correct operation of poly-phase boost converter each PWM gate signal is required to have 90 degrees phase shift respect to the previous one. In order to generate these signals a synchronization circuit is needed. Though practicable, the analog realization leads to certain limitations.

The number of converters in parallel, their synchronization angles, etc has to be decided priory for any application. Freedom in selecting the switching frequency is also not total. This paper presents an alternate total digital realization of the poly-phase controller. Therefore, the need for a different implementation may completely be understood.

Fig. 3.1 shows the architecture of digital control, which has been used here for the poly-phase boost converter. A PI controller based on the error signal from the outer voltage loop builds the reference current. The inductor current in each of the converters or a representative sample of the inductor currents is compared with current reference. Accordingly the individual duty ratios or a single common duty ratio is imposed in the switches.

It is obvious that in digital implementation modularity of the system is preserved. Adding extra stages or changing the switching frequency needs only a modification in the software.

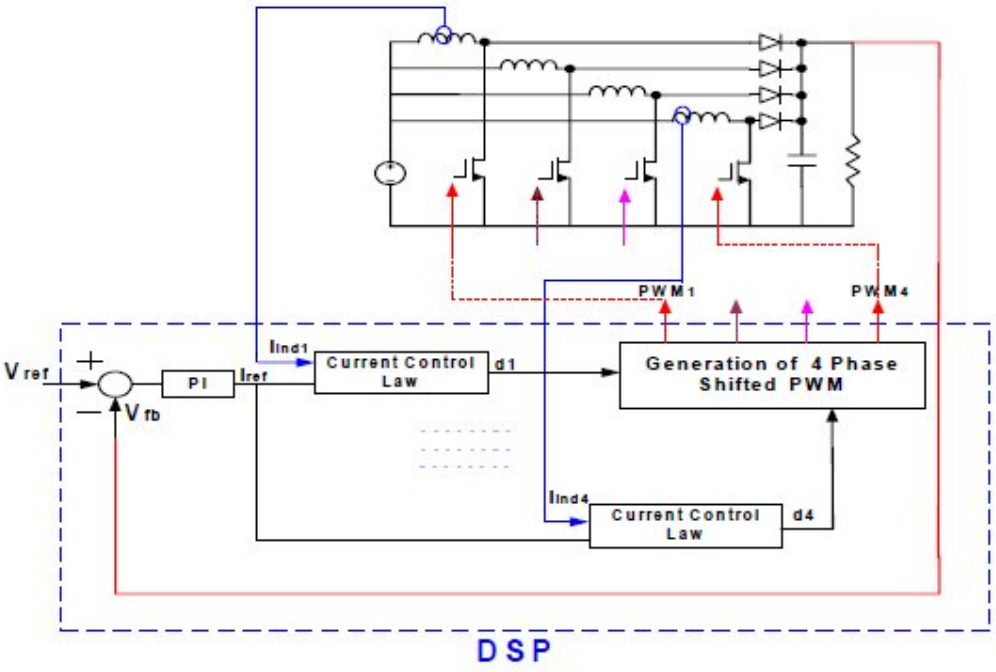

Fig 3.1 Digital Circuit Realization of the Polyphase Boost

Generation of the four phase shifted PWM signals can be done in two ways:

Method A: Programming general purpose timers with period of switching frequency and initializing four different counter registers with 0, 90, 180, 270 degrees phase shift respect to the timer period register.

Method B: The switching pattern of different switches for different values of duty cycles which is stored as lookup table in memory has been shown in table II. On time duration of the switch is determined by ***D′*** and similarly (1-***D′*)** determines the off time duration.

Where, ***D′*** is given by ***D′***=ND−floor(ND)

Then PWM signals can be generated on general-purpose input output pins.

3.2 Digital current control law

The required duty ratio for the next switching cycle is predicted based on the sample current and the input and output voltages but not the previous duty ratio. Fig.3.2 shows the inductor current waveform. The sampled inductor current i(n) at time nTs can be expressed as a function of the previous sampled value i(n-1) and the applied duty ratio d(n).

Table 3.1 Different possibilities of on & off situations of switches for N=4

	Intervals	Switch	$0 \le D \le \frac{1}{4}$	$\frac{1}{4} \le D \le \frac{1}{2}$	$\frac{1}{2} \le D \le \frac{3}{4}$	$\frac{3}{4} \le D \le 1$
1	$0 \le t \le \frac{T_S}{4}$	ON	1 0 0 0	1 0 0 1	1 0 1 1	1 1 1 1
2		OFF	0 0 0 0	1 0 0 0	1 0 0 1	1 0 1 1
3	$\frac{T_S}{4} \le t \le \frac{T_S}{2}$	ON	0 1 0 0	1 1 0 0	1 1 0 1	1 1 1 1
4		OFF	0 0 0 0	0 1 0 0	1 1 0 0	1 1 0 1
5	$\frac{T_S}{2} \le t \le \frac{3T_S}{4}$	ON	0 0 1 0	0 1 1 0	1 1 1 0	1 1 1 1
6		OFF	0 0 0 0	0 0 1 0	0 1 1 0	1 1 1 0
7	$\frac{3T_S}{4} \le t \le T_S$	ON	0 0 0 1	0 0 1 1	0 1 1 1	1 1 1 1
8		OFF	0 0 0 0	0 0 0 1	0 0 1 1	0 1 1 1

$$i(n) = i(n-1) + \frac{V_{ind}[n]T_S}{L} + \frac{(V_{in} - V_O)d'[n]T_S}{L} \tag{3.1}$$

$$i(n) = i(n-1) + \frac{V_{in}T_S}{L} - \frac{V_O d'[n]T_S}{L} \tag{3.2}$$

By using $d' = 1-d$ if we solve the above equation for predicted duty cycle

$$d[n] = \frac{L}{V_O T_S}\left(i_C - i_S[n-1]\right) + 1 - \frac{V_{in}}{V_O} \tag{3.3}$$

where ic=is[n].

It means in each cycle the inductor current follows the reference ic and try to make the difference zero such that in steady state

$$d[n] = 1 - \frac{V_{in}}{V_O} \tag{3.4}$$

This method is simple and has good results. In the second method all the currents are sampled such that each stage has an independent current control loop so different duty cycle values, which are almost same, can be found and will be applied to corresponding compare registers. If some slight differences are observed which may cause difference in current sharing of parallel stages it can be rectified through adjusting the parameters in equation (3.4) because we have independent closed loop controls. Similarly by finding the average of different duty cycles, the error may be applied to force the current sharing.

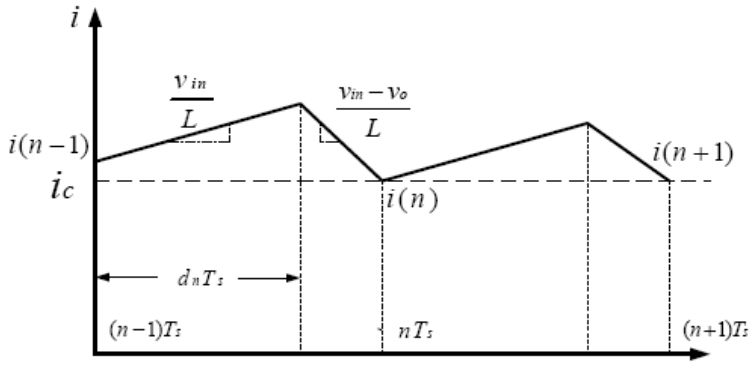

Fig 3.2 Inductor Current Waveform under Valley Current Control

Now it is obvious that single sampling has the advantage of simplicity and consequently it is more suitable for higher switching frequency because only one current is sampled and is processed in fewer amount of time. This method is good if the component values (for example the inductor values in different stages) are almost equal such that no significance difference in current sharing is observed.

On the other hand multiple sampling has the property to adjust each duty cycle value independently and despite of change in component values in other stages. Even for better performance applying the average of these duty values is another option in closed loop control of these converters. However it should be noted that this method takes more time compared to the single sampling method.

It is essential to note that some techniques, which have been explained here, like adjusting the parameters in each control loop and applying the average duty value, can only be achieved in digital control implementation. Another technique, which does not exist in analog implementation, is turning off of some of the converters at light load operation, which cause DCM operation of the converter. According to the level of load current, one, two or three of the converters may be switched of and in this case generation of the phase shifted PWM may change. For example for four converters in parallel one can turn off two or three of the stages without even changing the generation of phase shifted PWM signals. Of course for turning off of one stage or any other numbers in general in N converters in parallel the required amount of phase shift varies and it can be predetermined and stored in memory.

3.3 Comparing Specifications

3.3.1 Inductor Size

By comparing two converters at the same condition i.e. same output power, same output voltage and same amount of ripple current in the inductors it is easy to show that for single stage.

$$I_L = \frac{I_{load}}{1-D} \tag{3.5}$$

And for N converters in parallel

$$I_L = \frac{I_{load}}{N(1-D)} \tag{3.6}$$

3.3.2 RHP Zero

From the dynamical equation one can derive output to control transfer function. The results show that the RHP zero does not change because in the single stage the RHP zero equals to

$$\frac{V_g}{L * I_L} \tag{3.7}$$

And for N converters in parallel it equals to

$$\frac{V_g}{(NL)\left(\frac{I_L}{N}\right)} \tag{3.8}$$

From the dynamical equation the equality of the above result can be numerically justified.

3.3.3 RMS Current of Capacitor

One of the interesting point is the rms current of the output capacitor. With a good approximation the rms current of the output Capacitor can be expressed by

$$I_{rms} = I_L\,(ND - K + 1)(K - ND) \tag{3.9}$$

Where, K=floor(ND+1) &

$$I_L = \frac{I_{load}}{N(1-D)}$$

and " floor " shows the integer part function or equivalently it can be written as

$$I_{rms} = I_L D'(1-D')$$

Where D′ = ND − floor(ND)

3.3.4 Input Ripple Current

The input current is at higher frequency than the switching frequency and hence the EMI filter will be lighter and the peak to peak-input ripple current is substantially reduced and the magnitude of this current ripple for poly-phase boost converter can be derived as

$$\Delta I_{in} = \frac{(K - ND)(ND - K + 1)}{ND(1-D)} \Delta I_{in},1 \tag{3.10}$$

Where K=1,2,…,N

$$\frac{K-1}{N} \le D \le \frac{K}{N}$$

Or equivalently

$$\Delta I_{in}, N = \frac{D'(1-D')}{ND(1-D)} \Delta I_{in},1 \tag{3.11}$$

And

$$\Delta I_{in},1 = \frac{V_g}{L} D T_S \tag{3.12}$$

3.3.5 Output Ripple Voltage

Based on the previous analysis and the relation for output ripple voltage that is

$$\frac{\Delta V_O}{V_O} = \frac{DT_S}{R_{load}C} \tag{3.13}$$

The output ripple voltage for N converters is given by

$$\left(\frac{\Delta V_O}{V_O}\right) N = \frac{D'(1-D')}{N^2 D(1-D)} \left(\frac{\Delta V_O}{V_O}\right) 1 \tag{3.14}$$

Or in other words for the same amount of ripple in the output the size of capacitor reduces by a factor, which is equal to

$$\frac{D'(1-D')}{N^2 D(1-D)} \tag{3.15}$$

3.4 Design of PI Controller

3.4.1 Converter parameters

Po = 35 W

Vin = 12 V

Vo = 32 V

Fs = 100 KHz

D = 1-Vin/Vo = 0.625

ΔIin = 0.2(20%)

ΔVo = 0.01(1%)

R = Vo*Vo/Po = 29.257 Ω

L = (Vin*D*Ts)/ΔIin = 128.5714μH

C = (D*Ts*Vo)/(R*ΔVo) =21.3623μF

3.4.2 MATLAB program for bode plot of the Boost Converter

```
Vi=12;
Vo=32;
Po=35;
Fs=100e3;
deli=0.2;
delv=0.01;
D=1-Vi/Vo;
Ts=1/Fs;
R=Vo^2/Po;
L=D*(1-D)^2*R*Ts/deli;
C=D*Ts/(R*delv);
num=[1/(1-D)];
den=[L*C/(1-D)^2 L/(R*(1-D)^2) 1];
H=tf(num,den);
bode(num,den);
grid on;
```

3.4.2.1 Bode plot

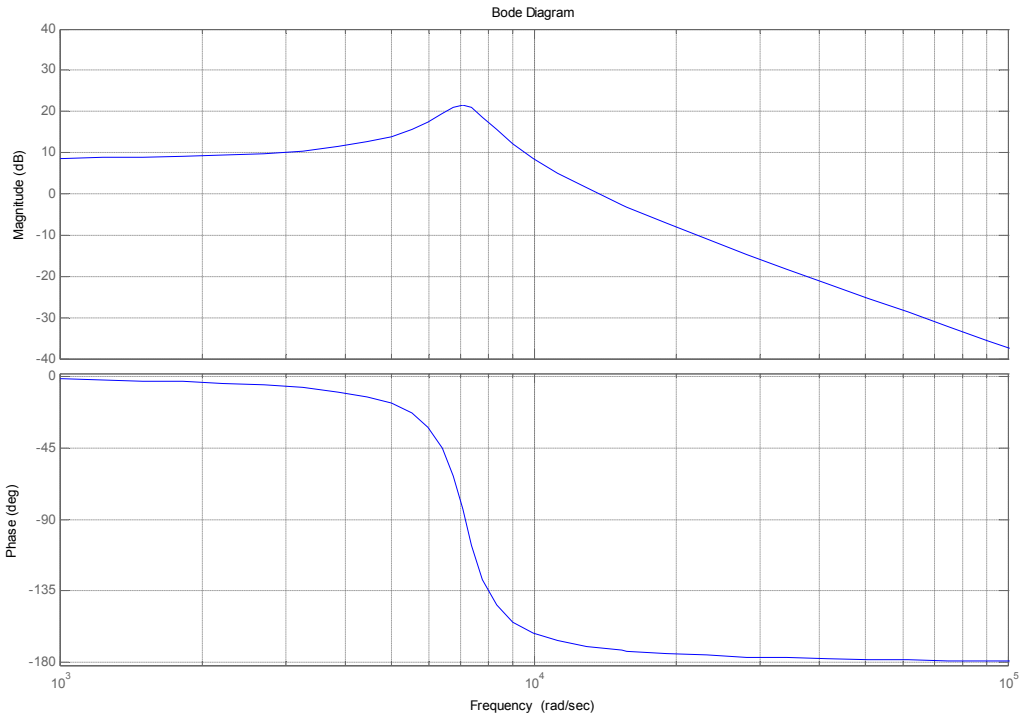

Fig 3.3 Bode plot of the boost converter

3.4.3 Calculation Kp, Ki from bode plot

$$K_P = \frac{\cos\theta}{A} \tag{3.16}$$

$$= \text{2.3792e-3}$$

$$K_i = -\frac{\omega \sin\theta}{A} \tag{3.17}$$

$$= 397.3783$$

$$\theta = \gamma_d - \gamma_u$$

$$= 60° - 87.6°$$

where, γ_d = desired phase margin,

γ_u = phase margin of uncompensated system.

CHAPTER 4

SOFTWARE IMPLEMENTATION

4.1 MATLAB Simulation of Single Phase Boost Converter (open loop)

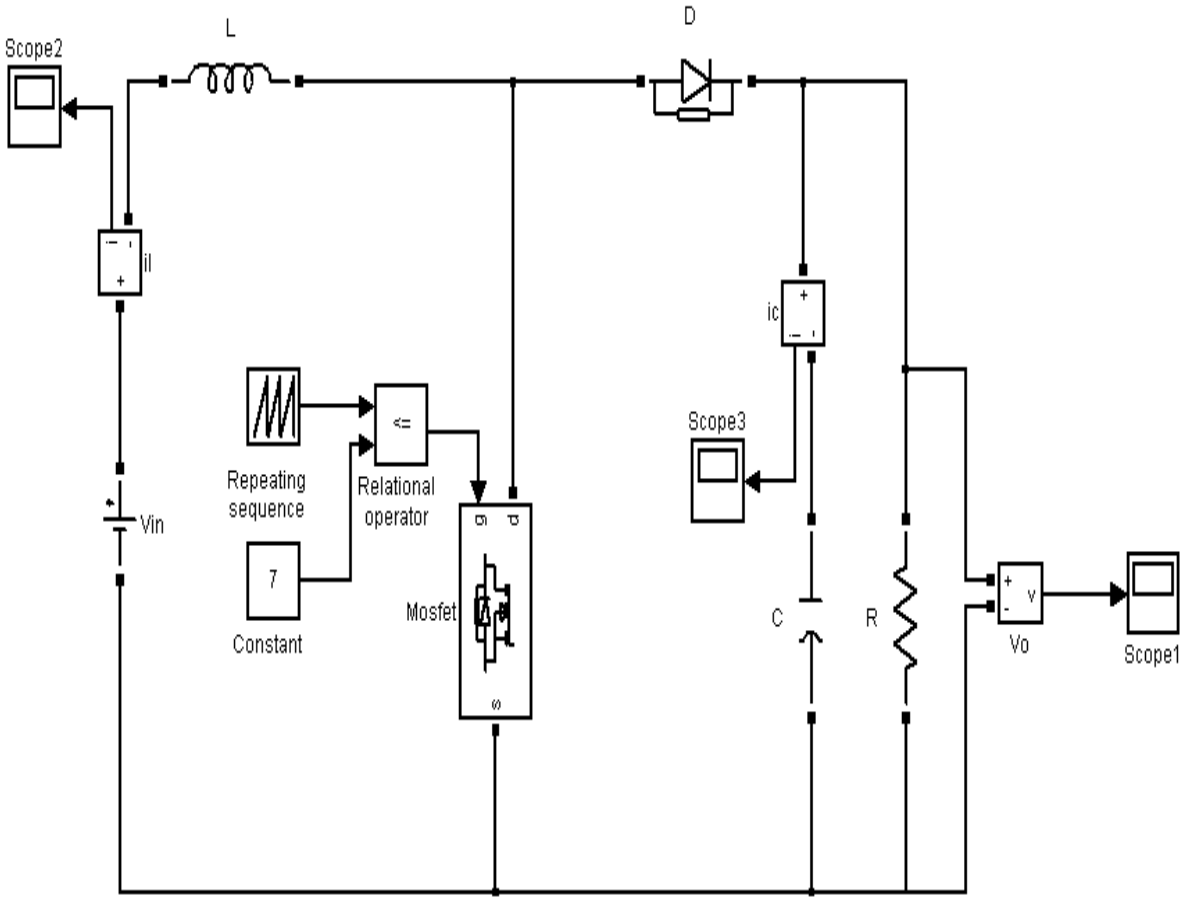

Fig 4.1 Simulink Model for Single Phase Boost Converter (open loop)

4.2 MATLAB Simulation of Four Phase Boost Converter (open loop)

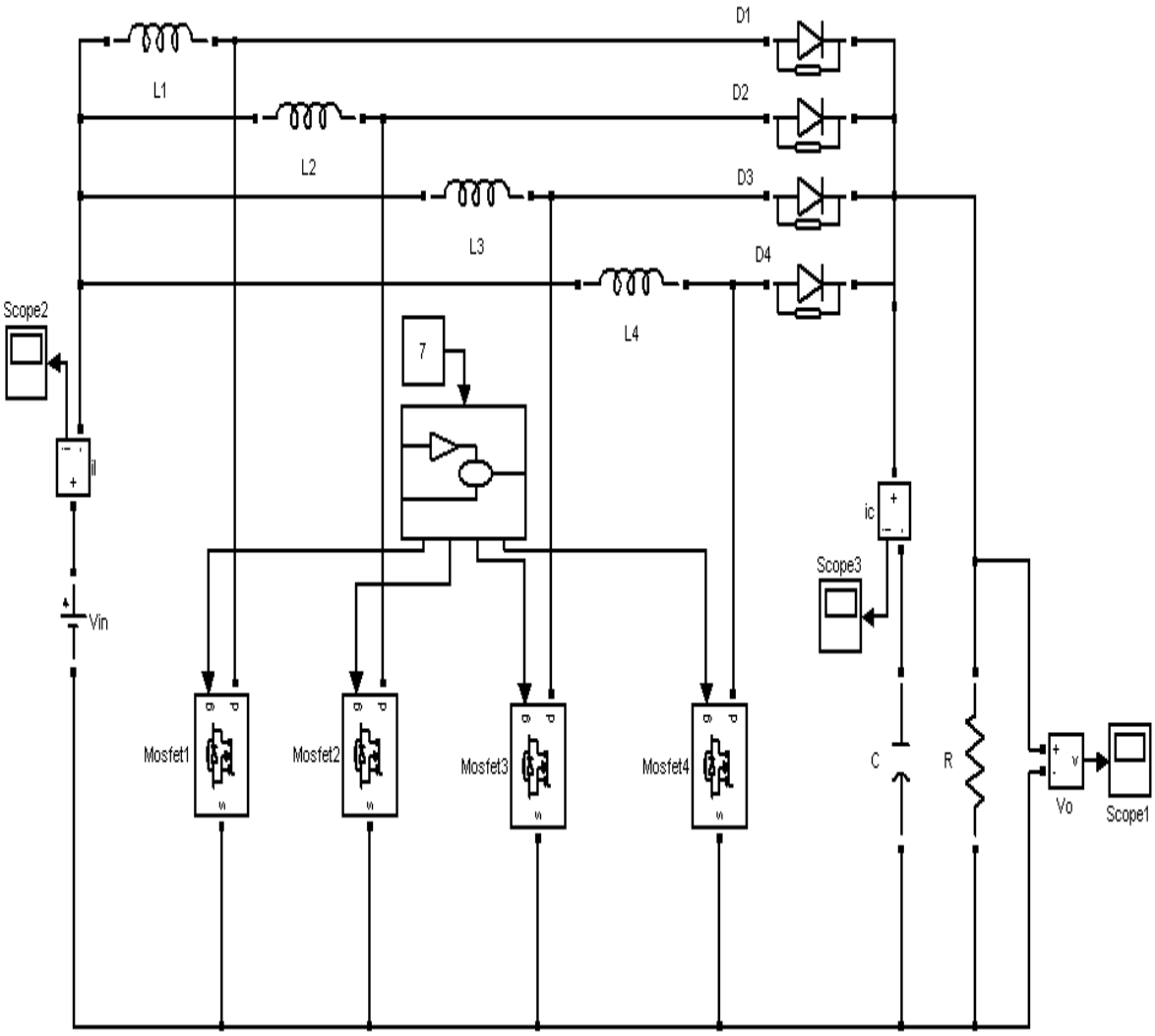

Fig. 4.2 Simulink Model for Four Phase Boost Converter (open loop)

4.2.1 Generation of Four Phase Shifted Pulses

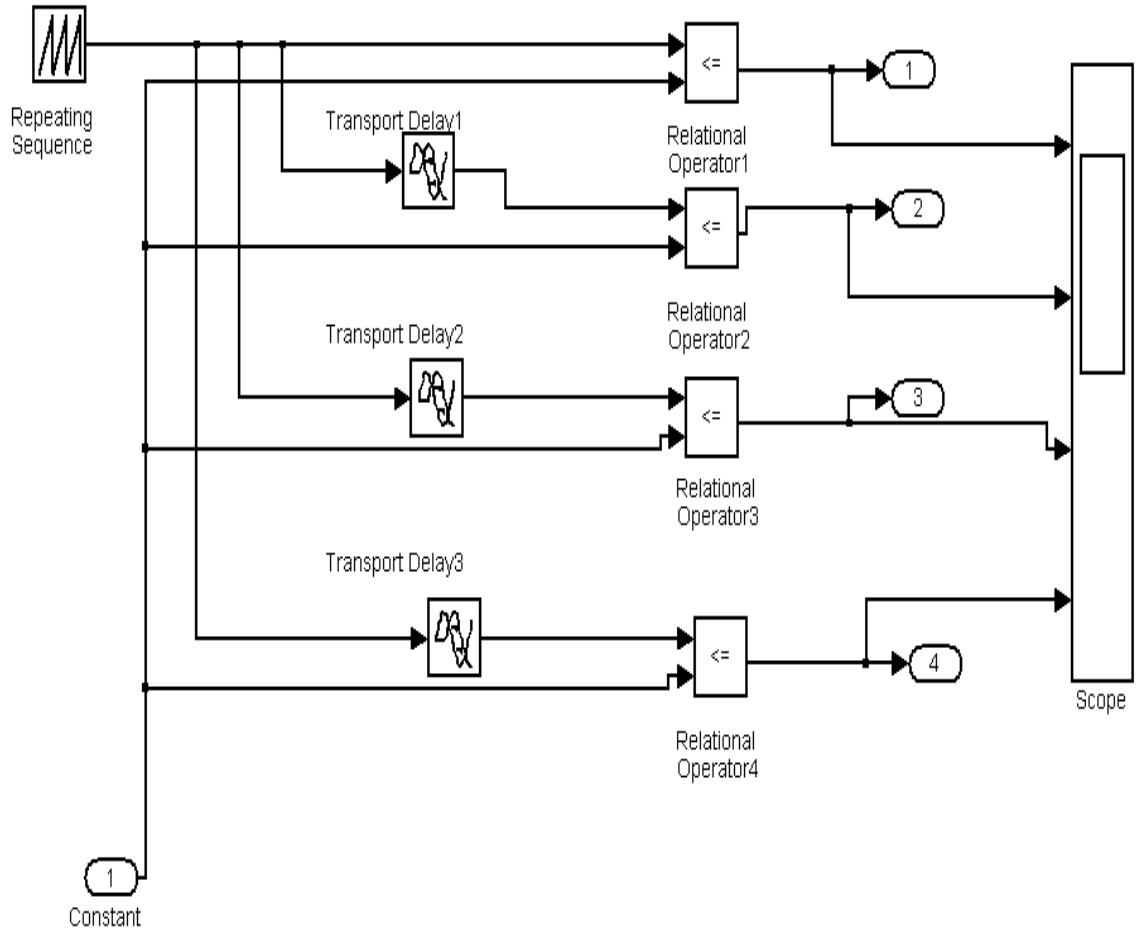

Fig 4.3 Generation of Four Phase Shifted Pulses using Simulink

4.3 MATLAB Simulation of Single Phase Boost Converter (Closed loop)

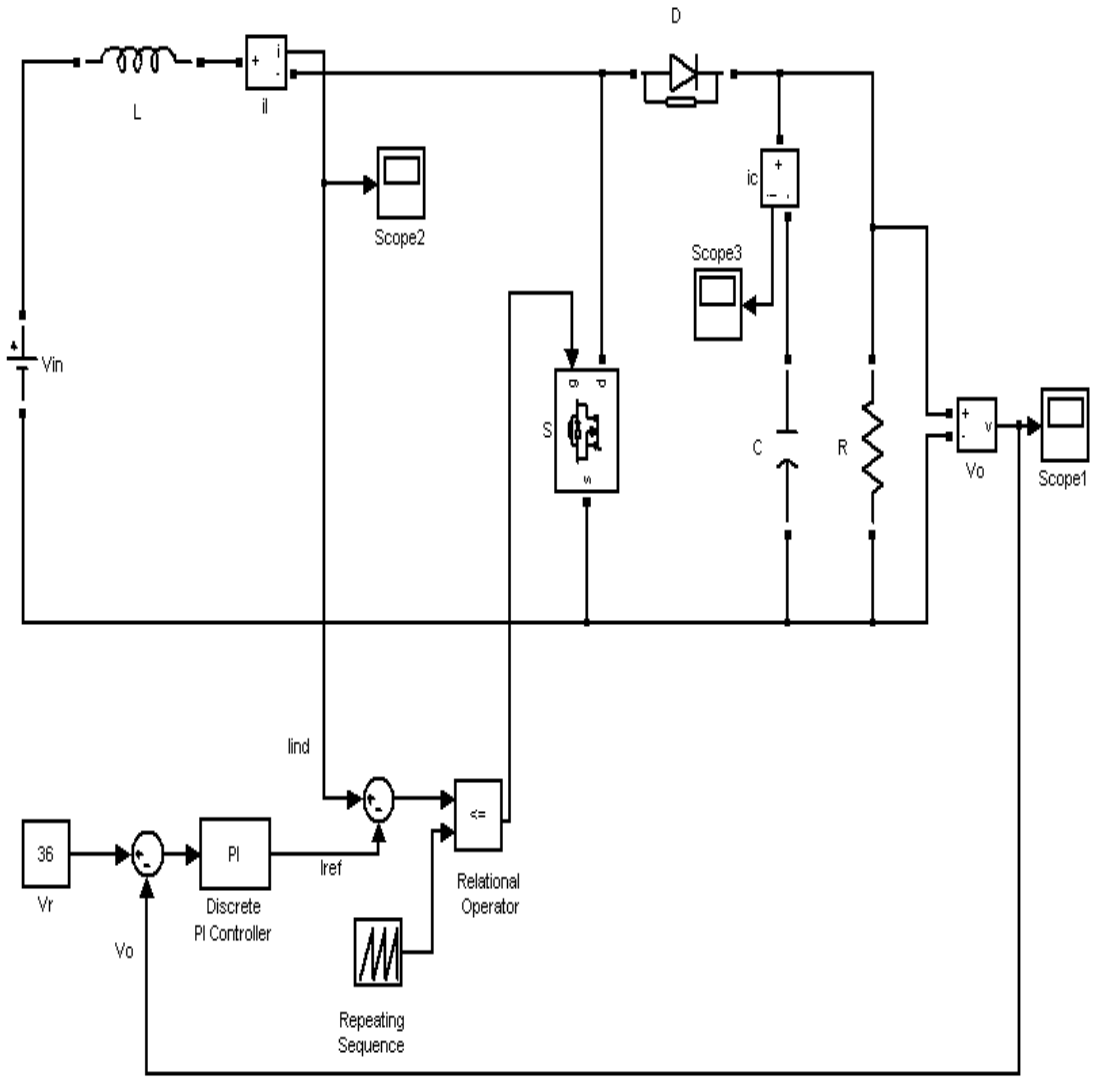

Fig 4.4 Simulink Model for Single Phase Boost Converter (Closed loop)

4.4 MATLAB Simulation of Four Phase Boost Converter (Closed loop)

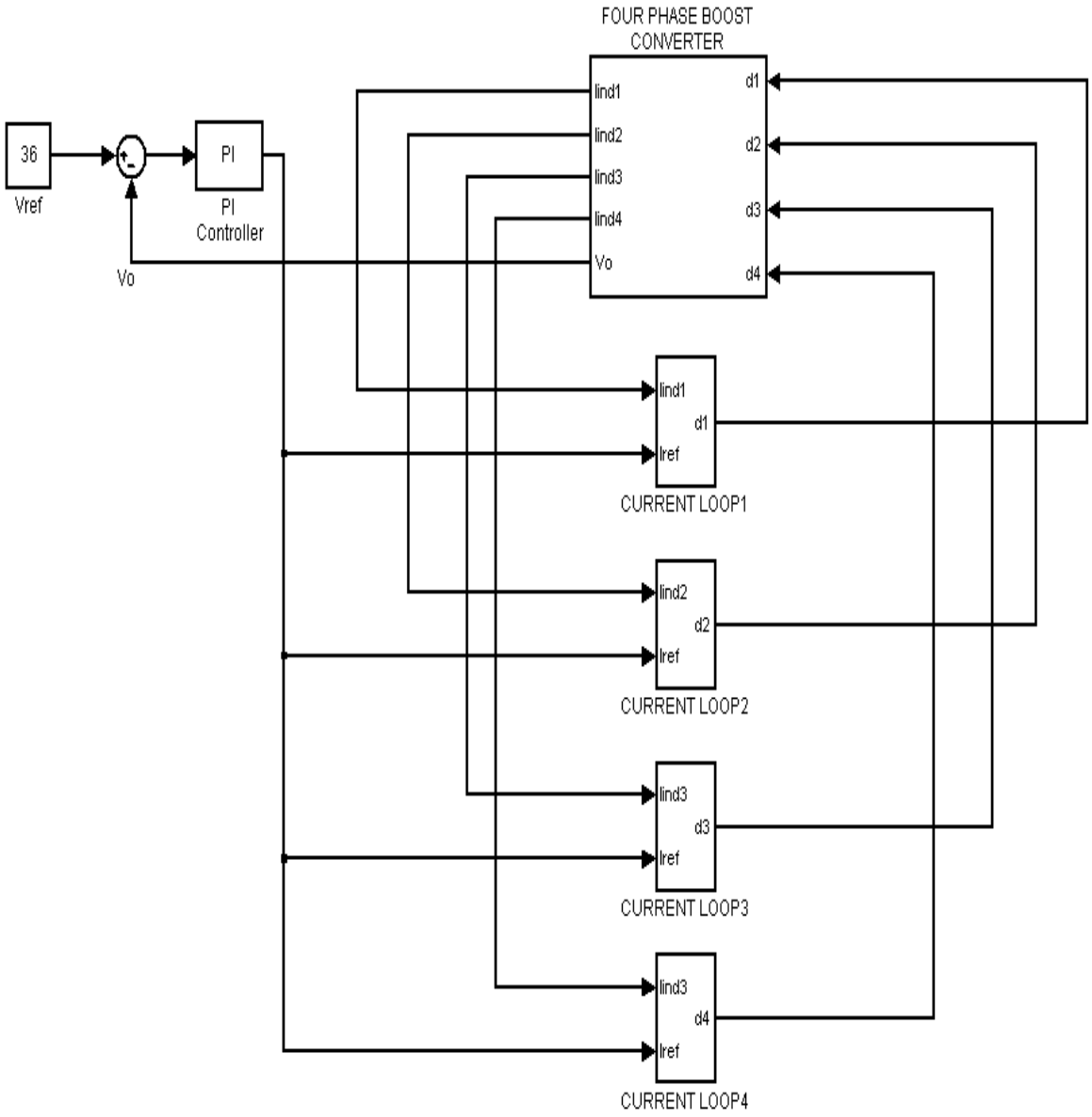

Fig 4.5 Simulink Model for Single Phase Boost Converter (Closed loop)

4.5 Sub System for Four Phase Boost Converter

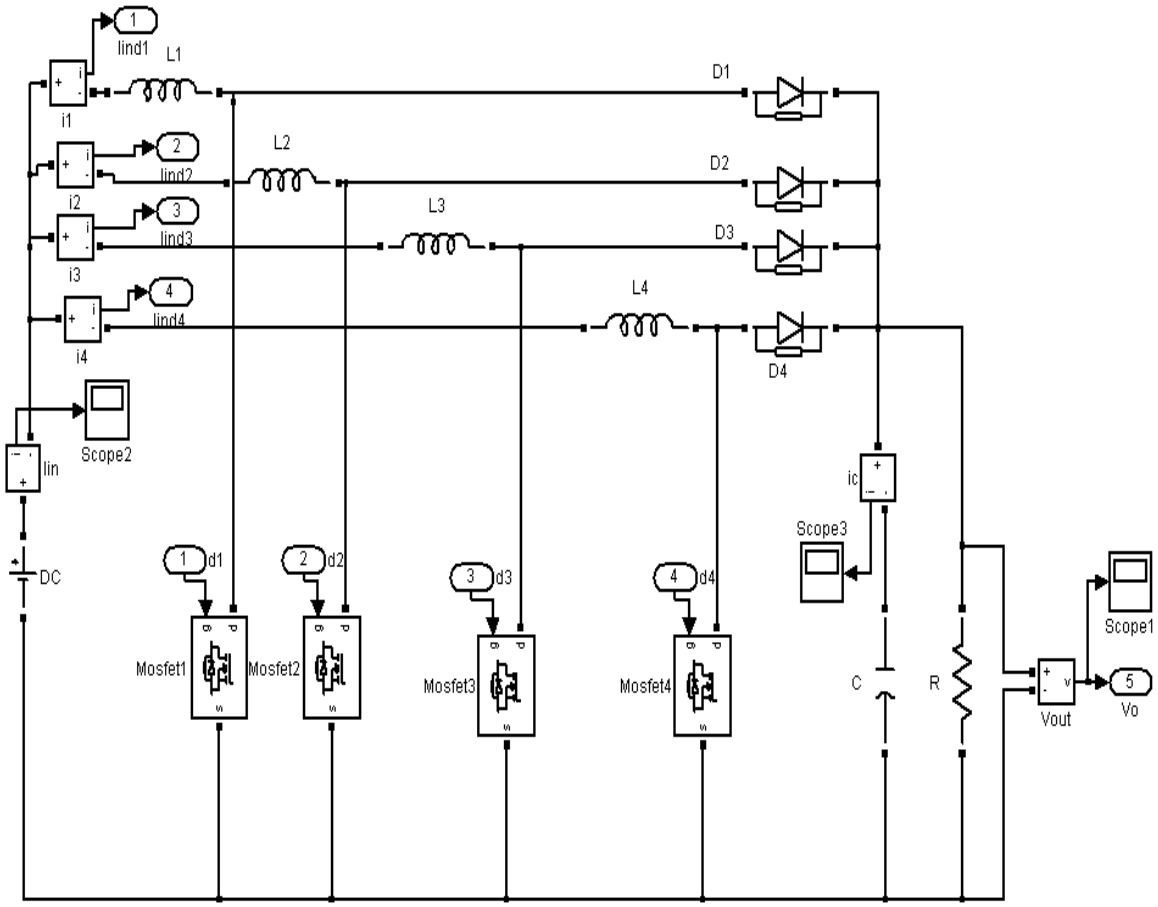

Fig 4.6 Sub System for Four Phase Boost Converter

4.6 Subsystems for Current Loops

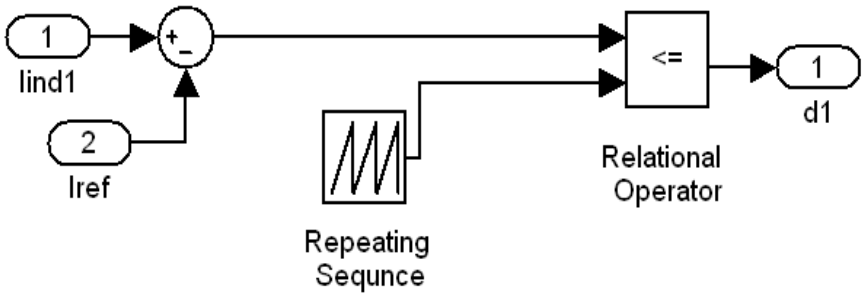

Fig 4.7 Simulink Model for Current Loop 1

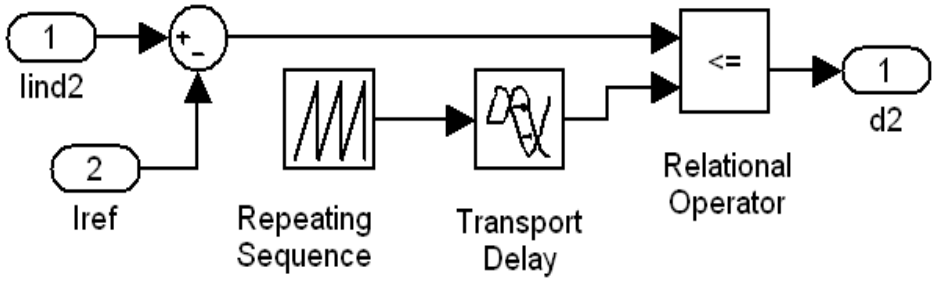

Fig 4.8 Simulink Model for Current Loop 2

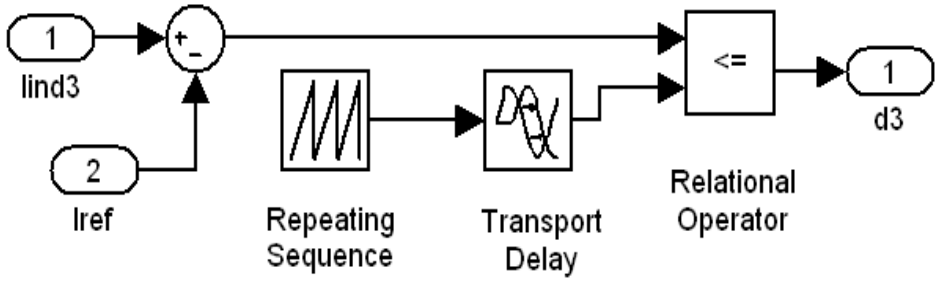

Fig 4.9 Simulink Model for Current Loop 3

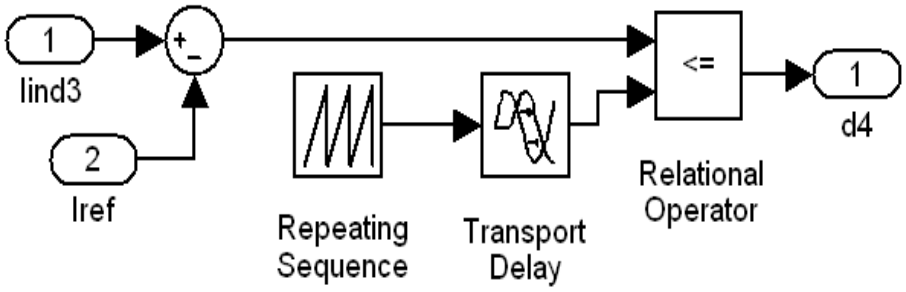

Fig 4.10 Simulink Model for Current Loop 4

4.7 Comparison of Single Phase and Four Phase Converters (in open loop)

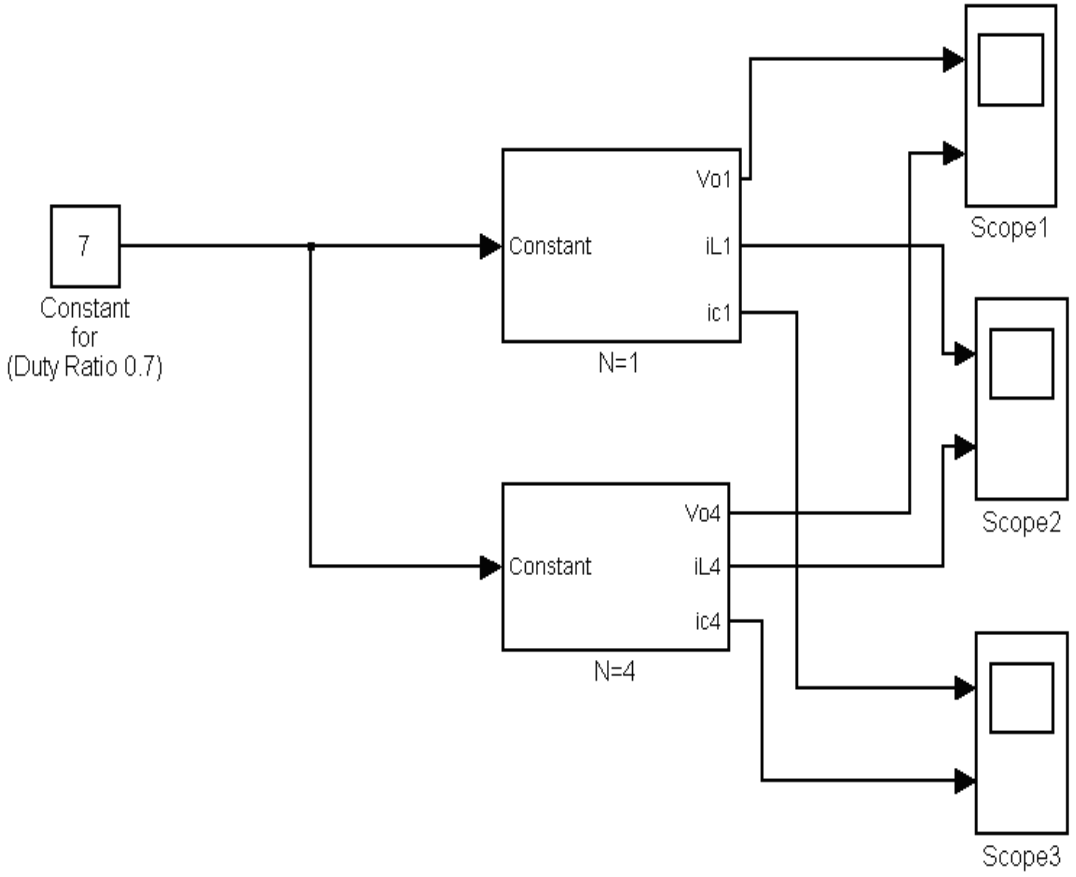

Fig 4.11 Simulink Model for Comparison of Single Phase and Four Phase Converters (in open loop)

4.8 Comparison of Single Phase and Four Phase Converters (in closed loop)

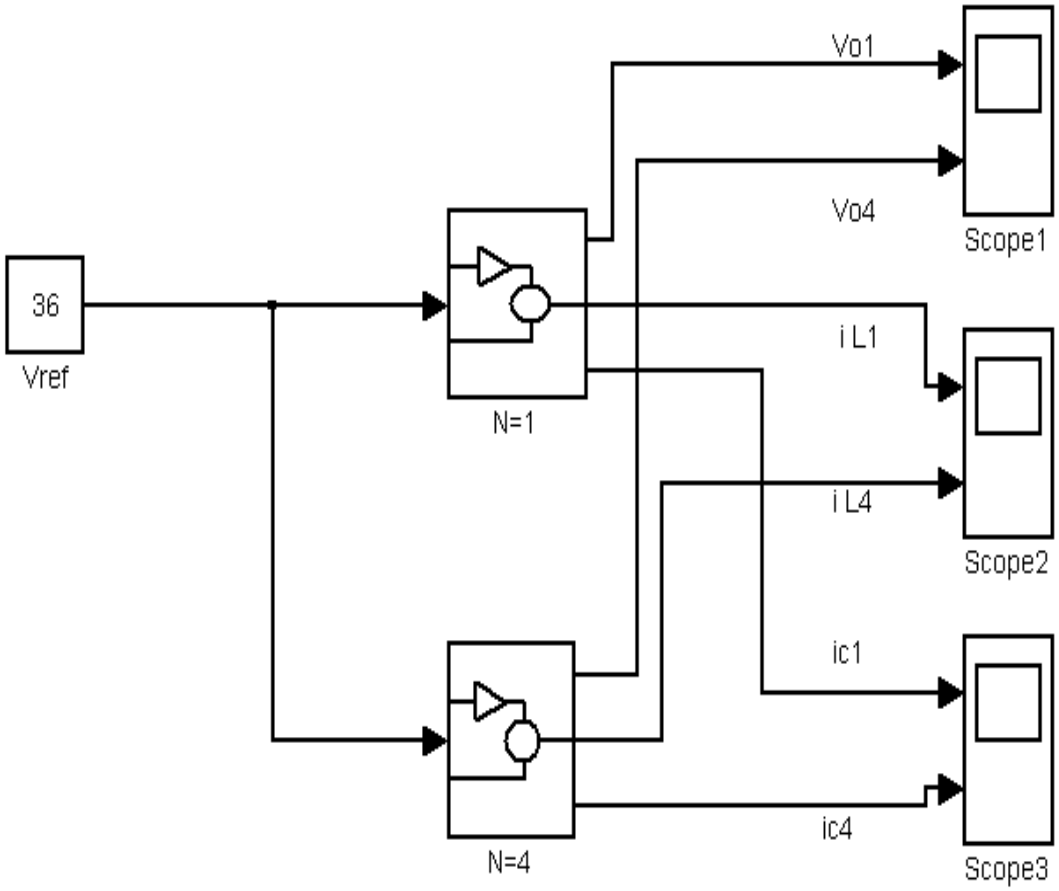

Fig 4.12 Simulink Model for Comparison of Single Phase and Four Phase Converters (in closed loop)

4.9 Step Response for Four Phase Boost Converter

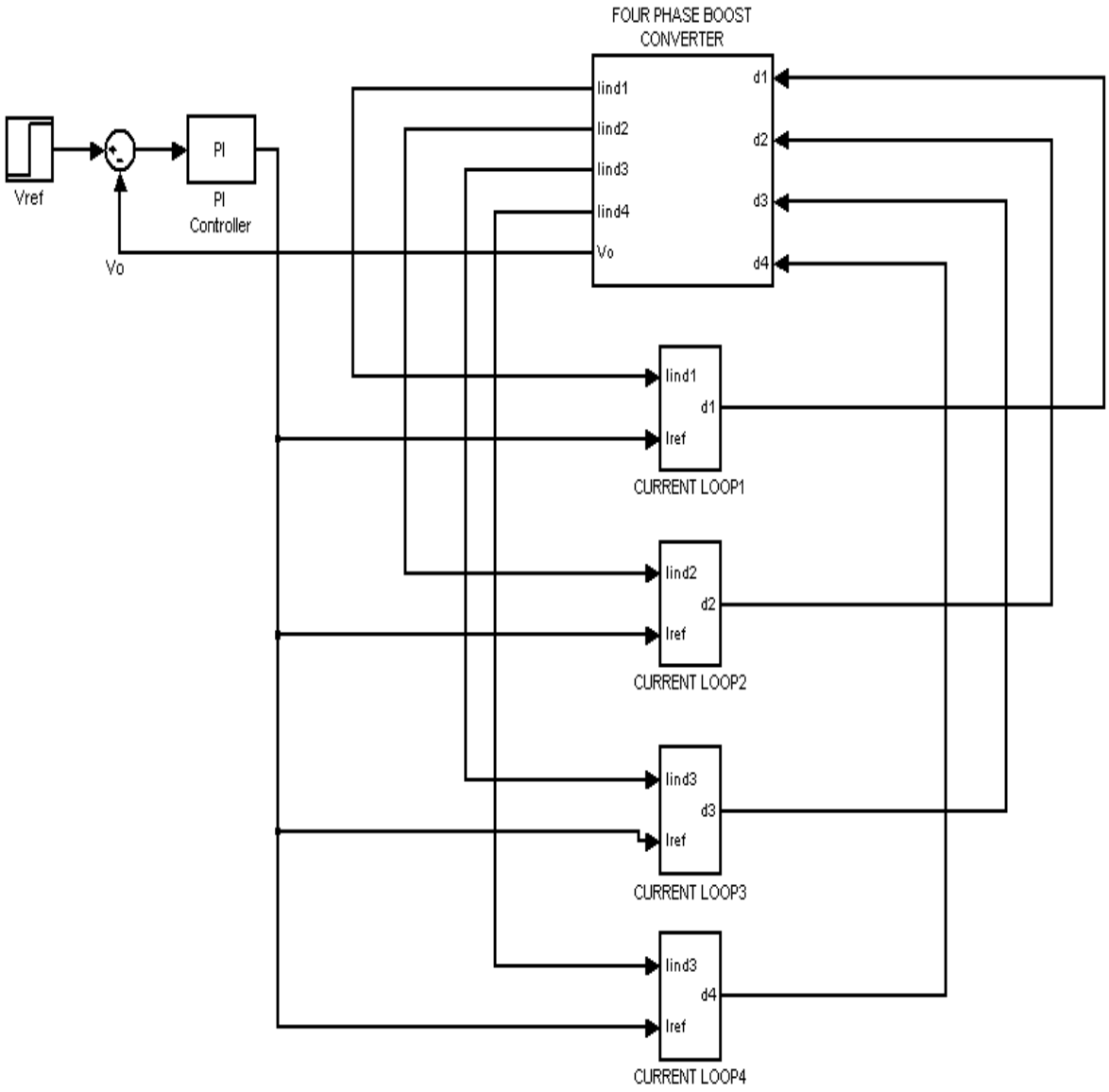

Fig 4.13 Simulink Model for Step Response for Four Phase Boost Converter

CHAPTER 5

RESULTS

5.1 Open Loop Simulation of Single Phase Boost Converter

5.1.1 Output Voltage

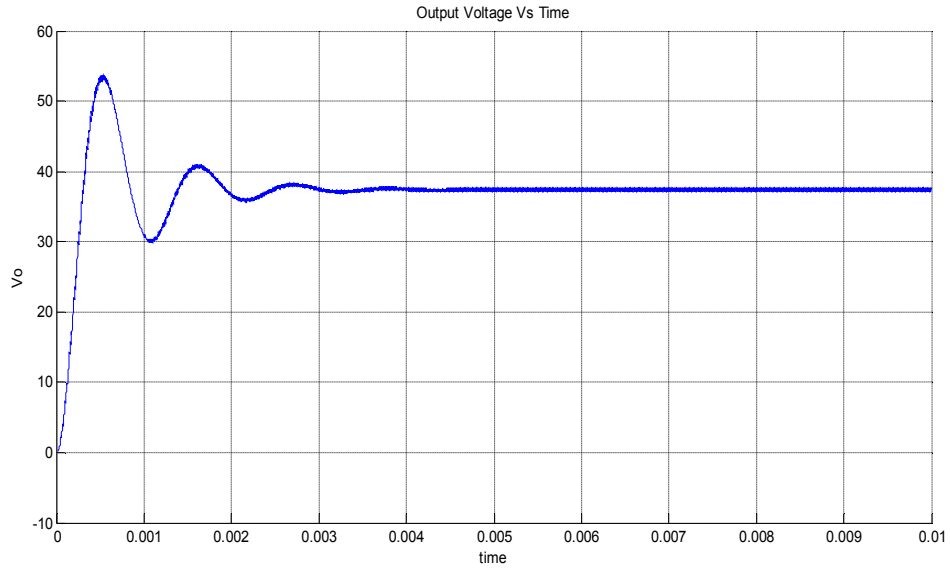

Fig 5.1 output voltage of single phase boost converter

5.1.2 Output Voltage Ripple

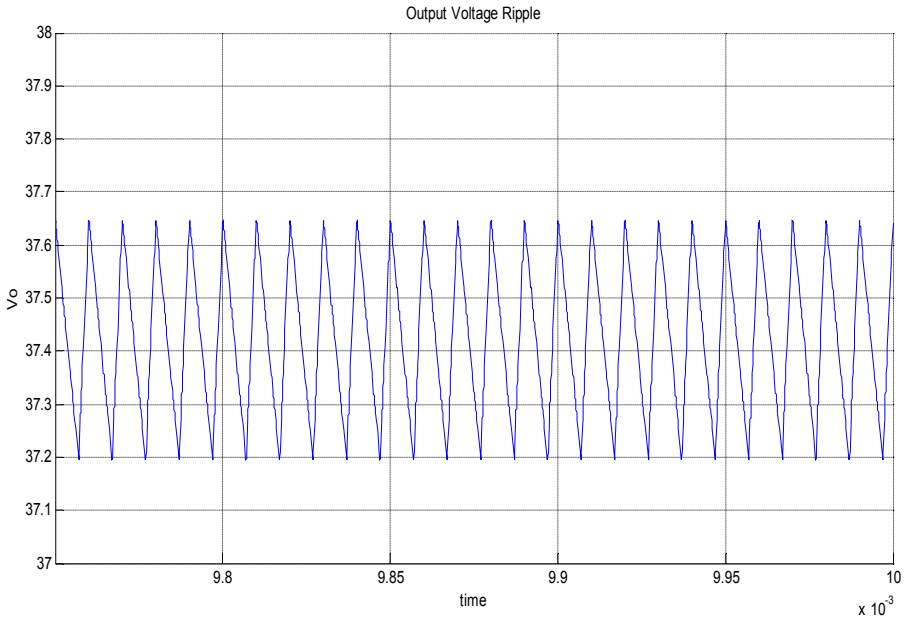

Fig 5.2 output voltage ripple of single phase boost converter

5.1.3 Input Current

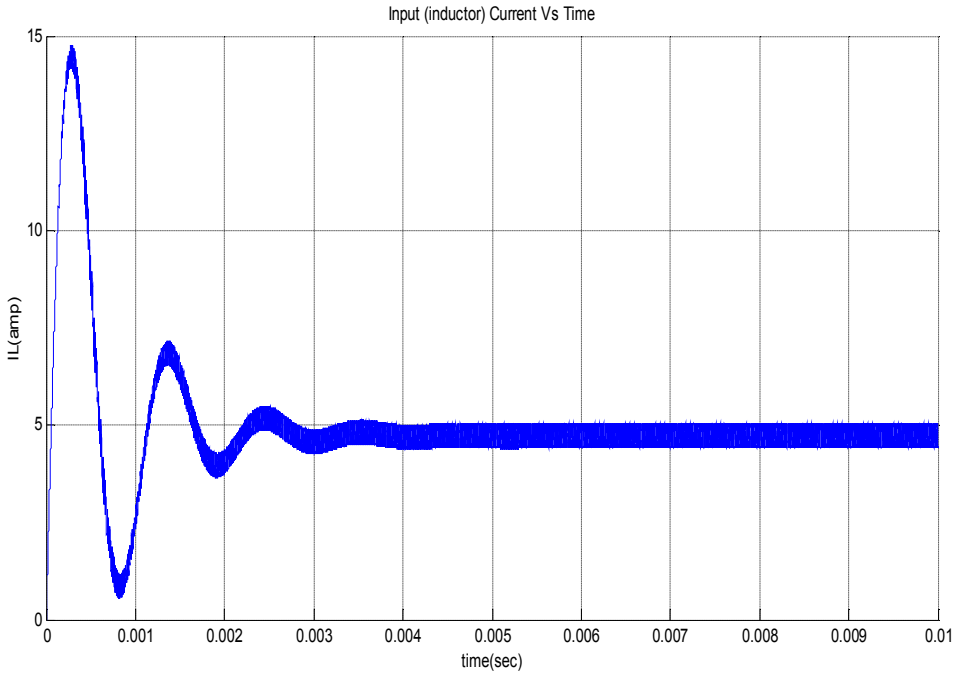

Fig 5.3 Input current of single phase boost converter

5.1.4 Input Current Ripple

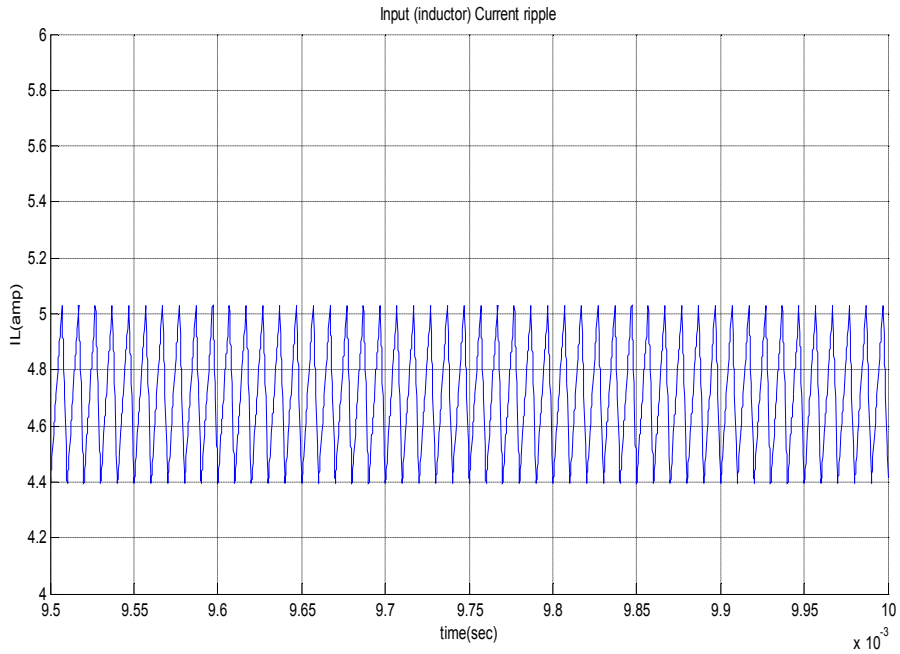

Fig 5.4 Input current ripple of single phase boost converter

5.1.5 Capacitor Current

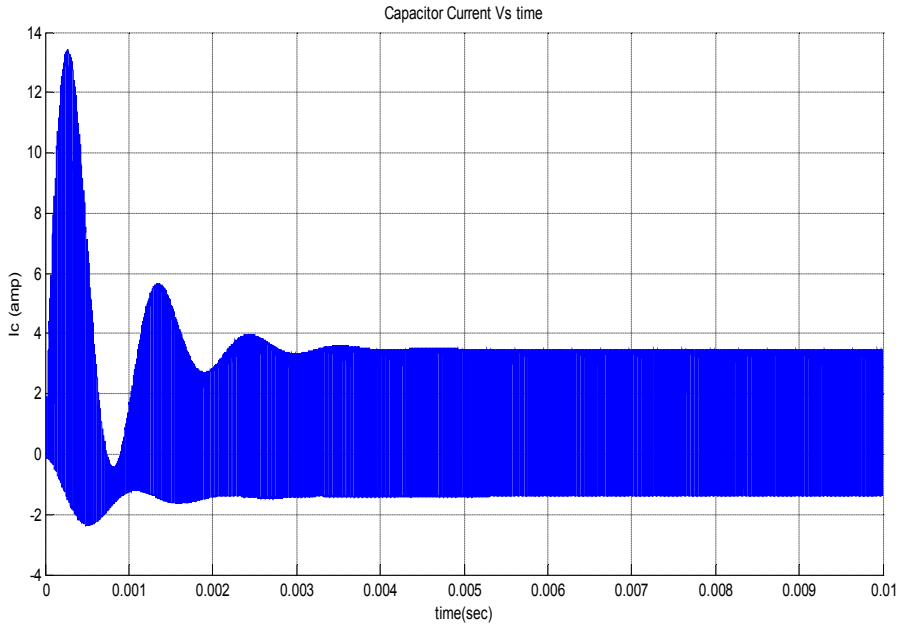

Fig 5.5 capacitor current of single phase boost converter

5.1.6 Steady state Capacitor Current

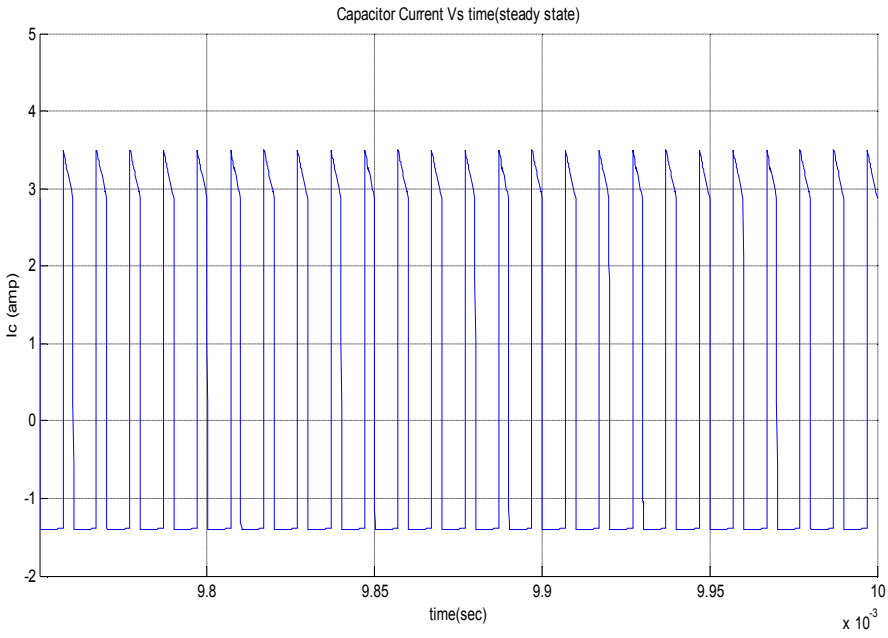

Fig 5.6 steady state capacitor current of single phase boost converter

5.2 Open Loop Simulation of Four Phase Boost Converter

5.2.1 Phase Shifted Pulses

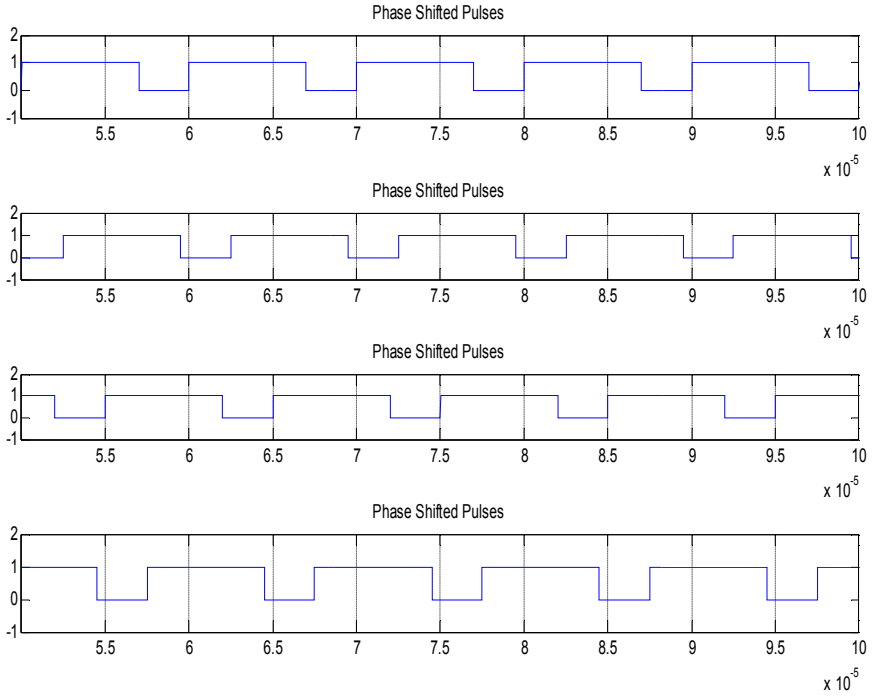

Fig 5.7 phase shifted pulses for the four phase boost converter

5.2.2 Output Voltage

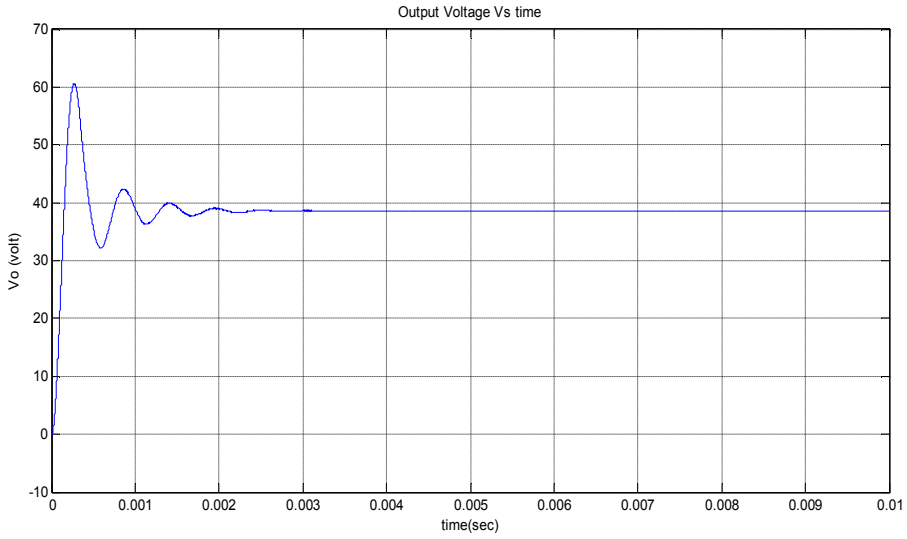

Fig 5.8 output voltage of four phase boost converter

5.2.3 Output Voltage Ripple

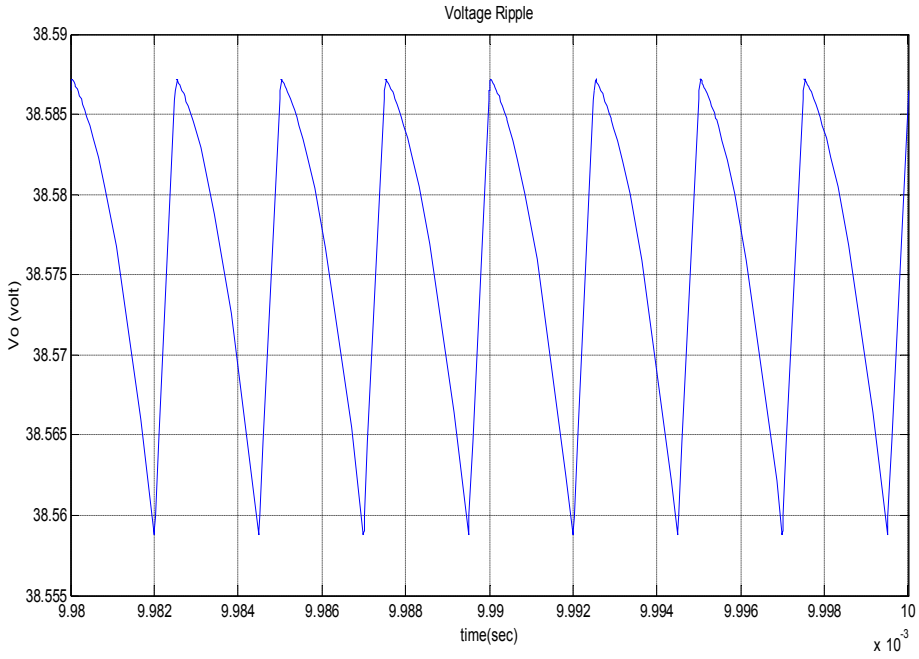

Fig 5.9 output voltage ripple of four phase boost converter

5.2.4 Input Current

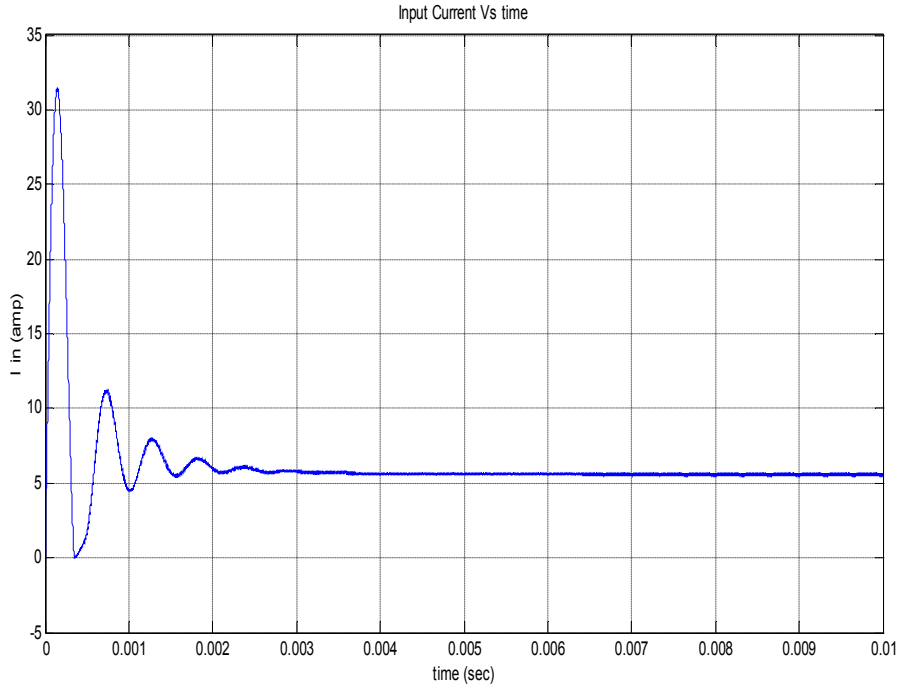

Fig 5.10 Input current of four phase boost converter

5.2.5 Input Current Ripple

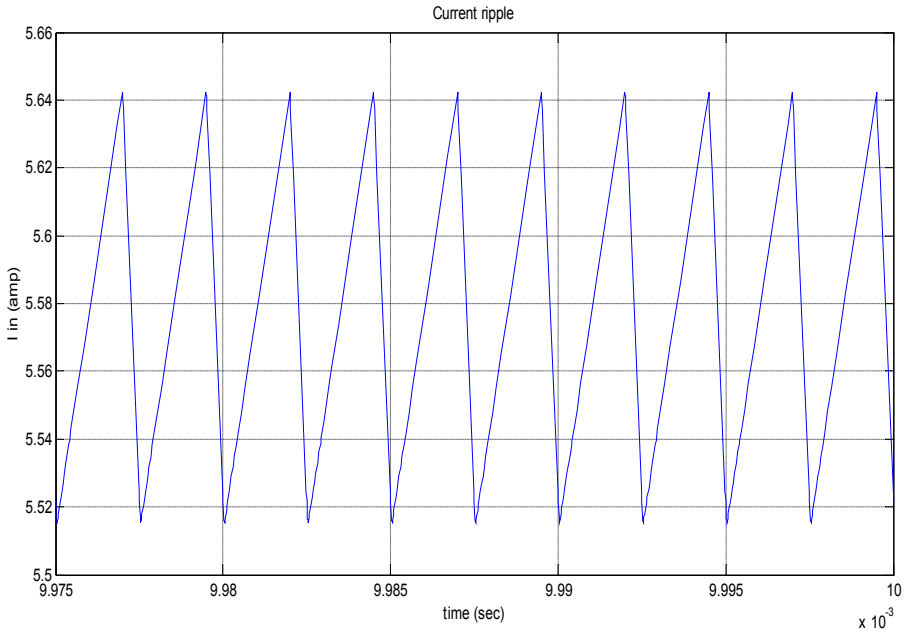

Fig 5.11 Input current ripple of four phase boost converter

5.2.6 Capacitor Current

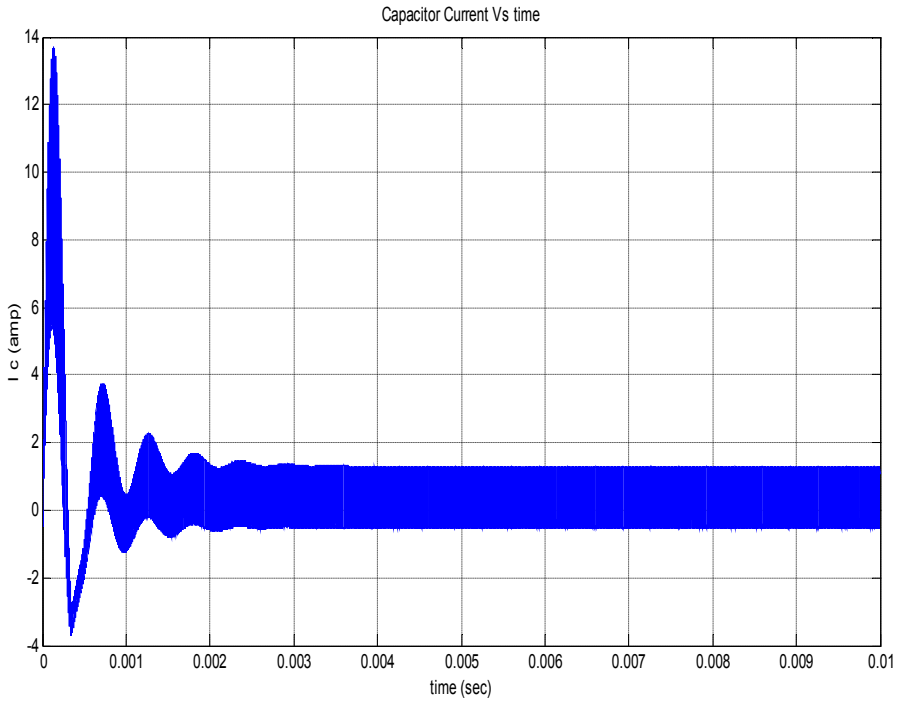

Fig 5.12 capacitor current of four phase boost converter

5.2.7 Steady state Capacitor Current

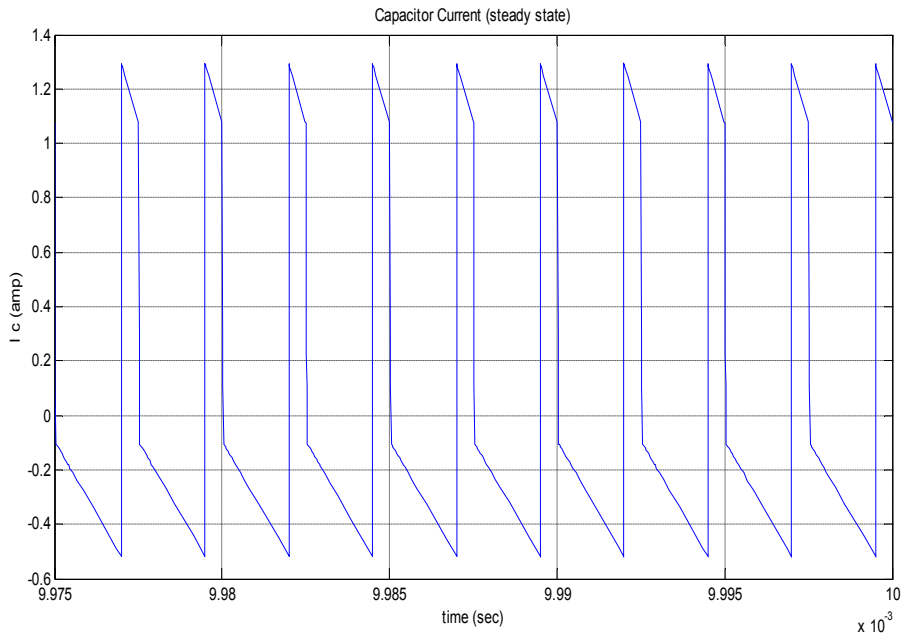

Fig 5.13 steady state capacitor current of four phase boost converter

5.3 Closed Loop Simulation of Single Phase Boost Converter

5.3.1 Output Voltage

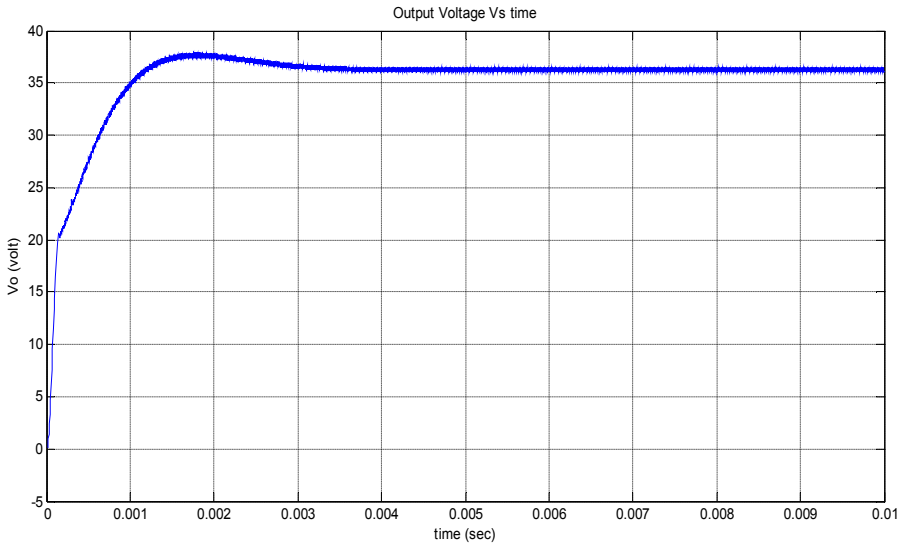

Fig 5.14 output voltage of single phase boost converter

5.3.2 Output Voltage Ripple

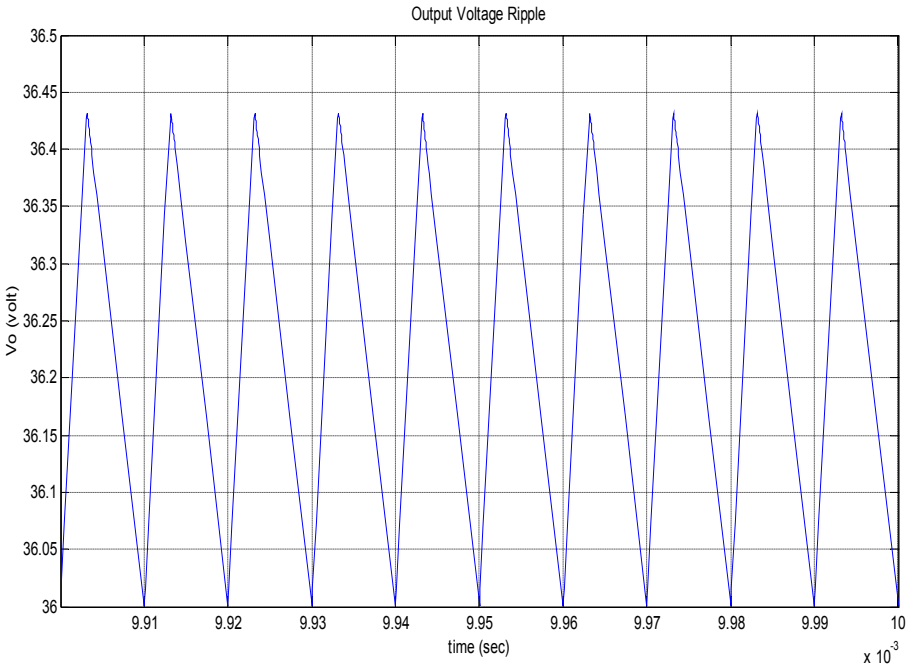

Fig 5.15 output voltage ripple of single phase boost converter

5.3.3 Input Current

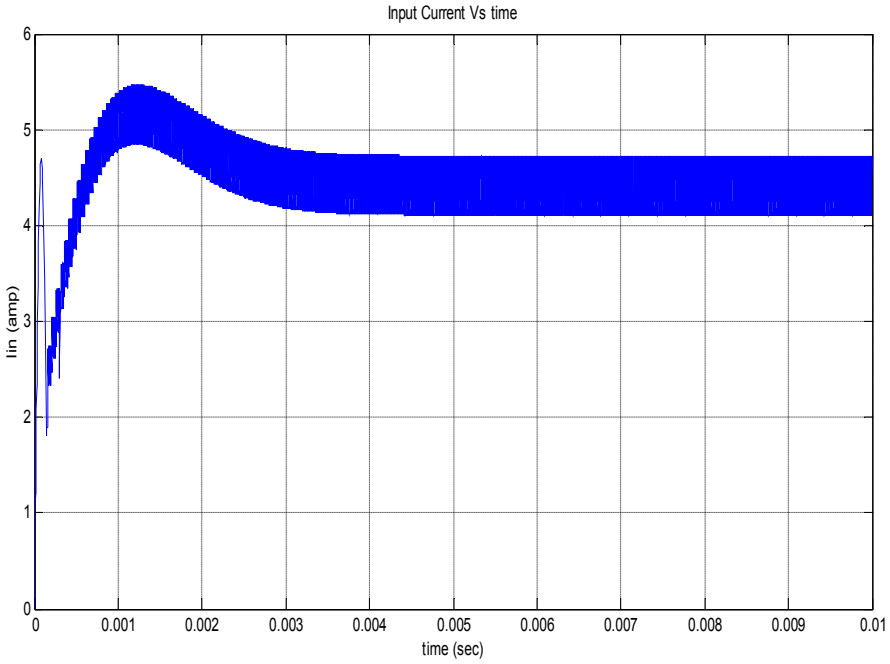

Fig 5.16 Input current of single phase boost converter

5.3.4 Input Current Ripple

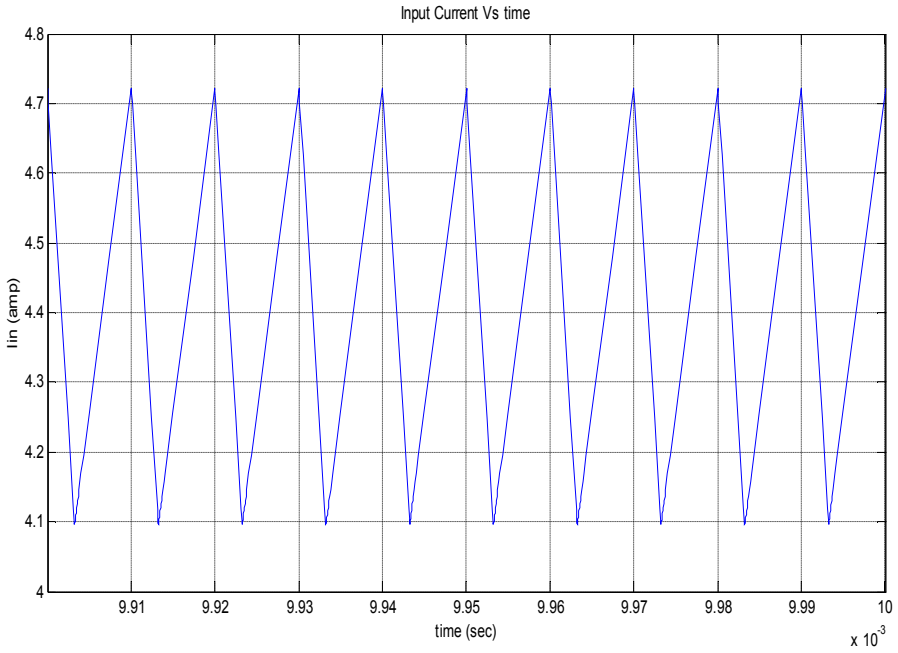

Fig 5.17 Input current ripple of single phase boost converter

5.3.5 Capacitor Current

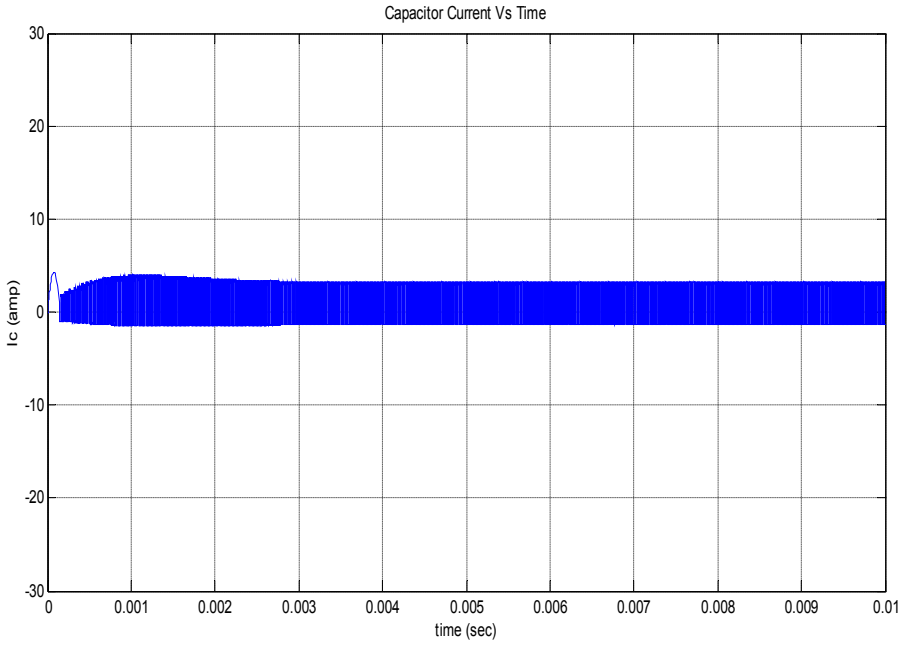

Fig 5.18 capacitor current of single phase boost converter

5.3.6 Steady State Capacitor Current

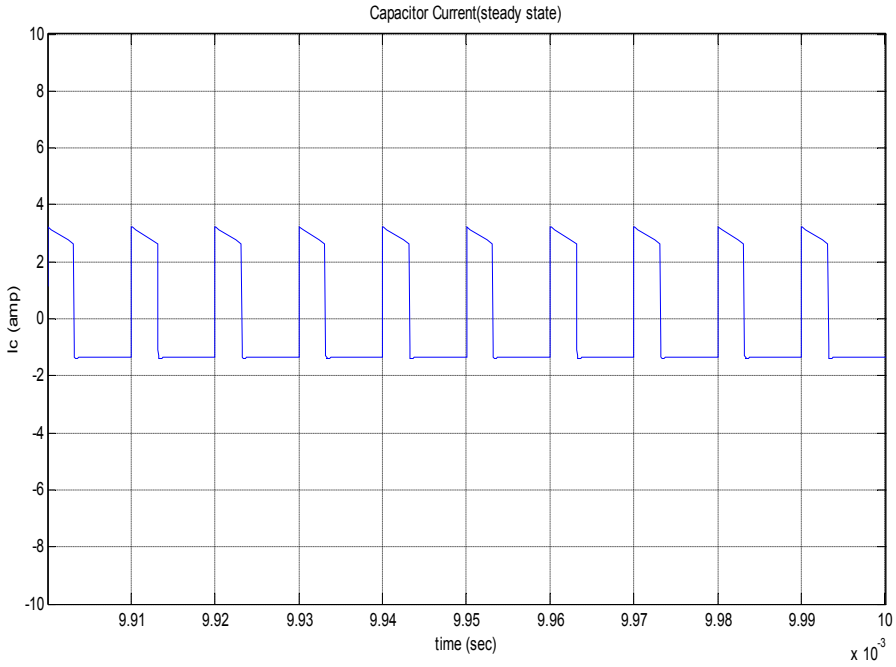

Fig 5.19 steady state capacitor of single phase boost converter

5.4 Closed Loop Simulation of Four Phase Boost Converter

5.4.1 Output Voltage

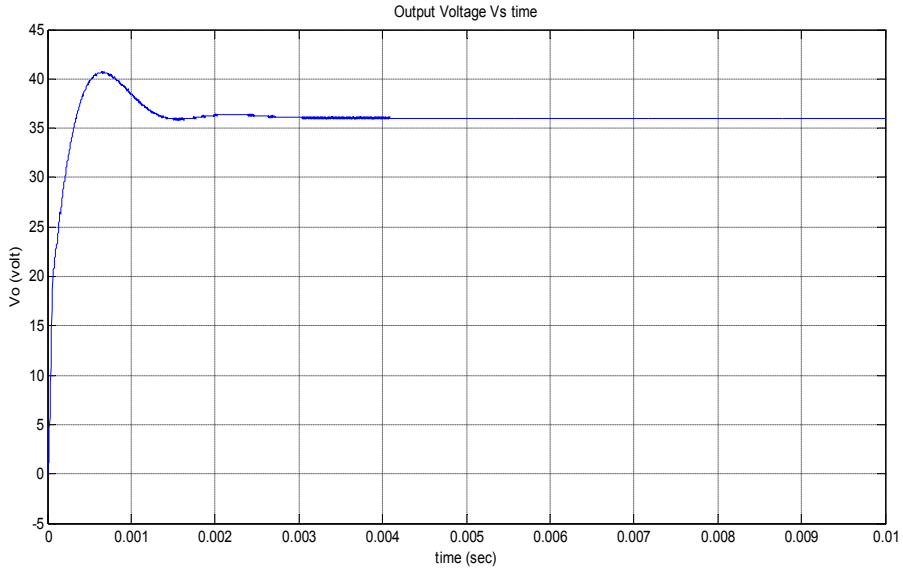

Fig 5.20 output voltage of four phase boost converter

5.4.2 Output Voltage Ripple

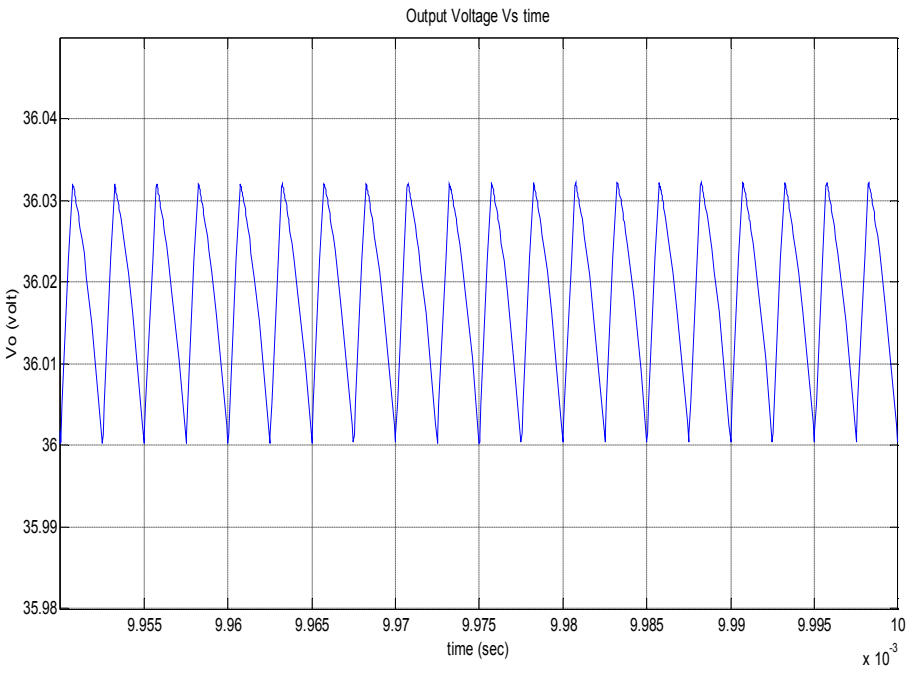

Fig 5.21 output voltage ripple of four phase boost converter

5.4.3 Input Current

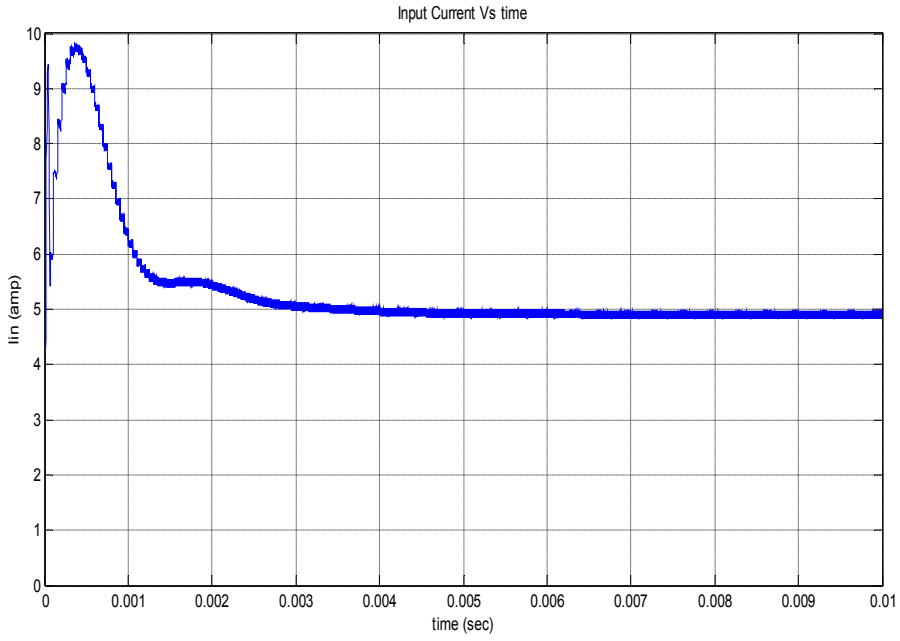

Fig 5.22 Input current of four phase boost converter

5.4.4 Input Current Ripple

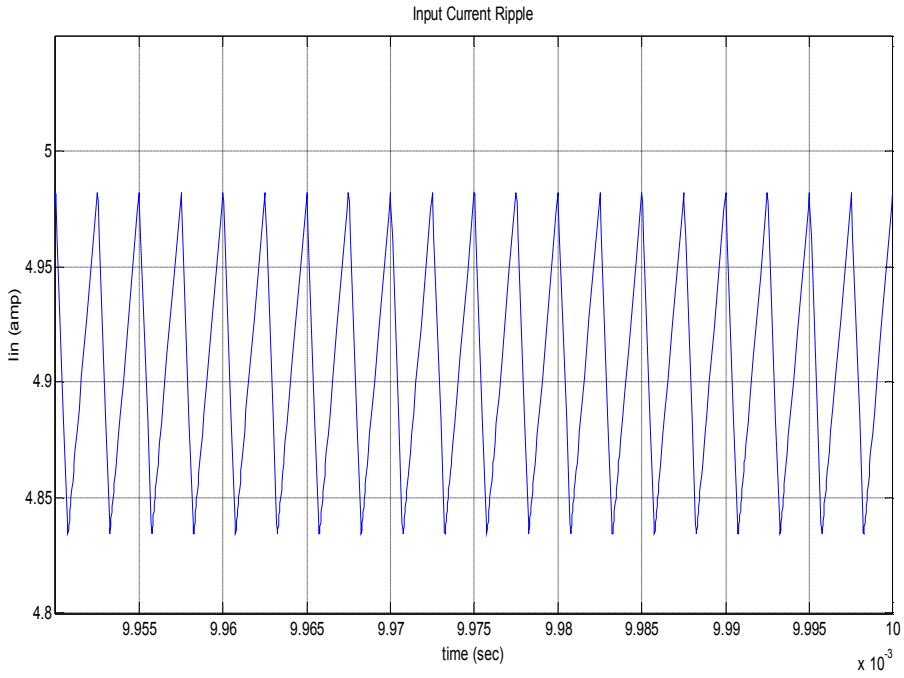

Fig 5.23 Input current ripple of four phase boost converter

5.4.5 Capacitor Current

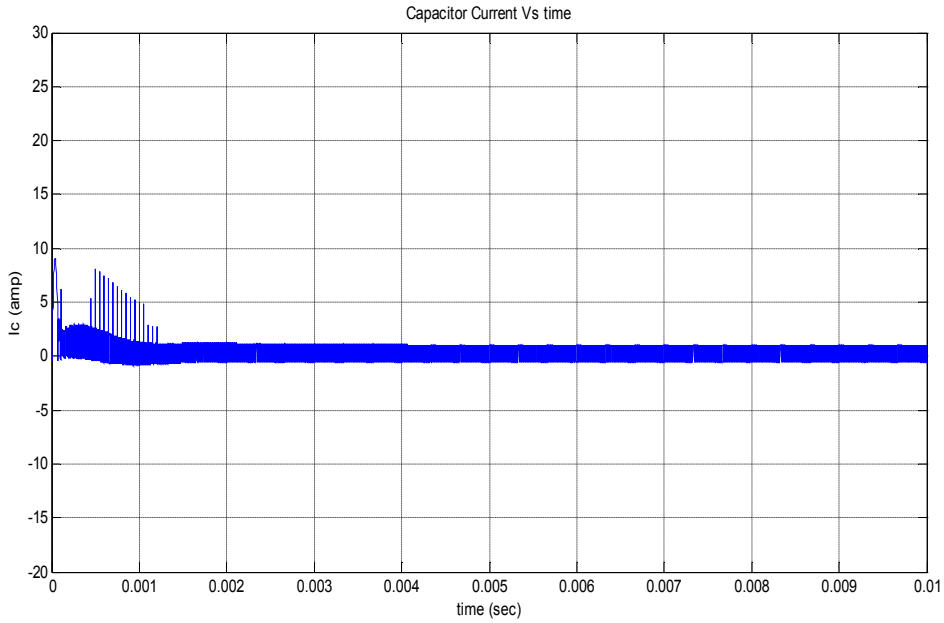

Fig 5.24 capacitor current of four phase boost converter

5.4.6 Steady State Capacitor Current

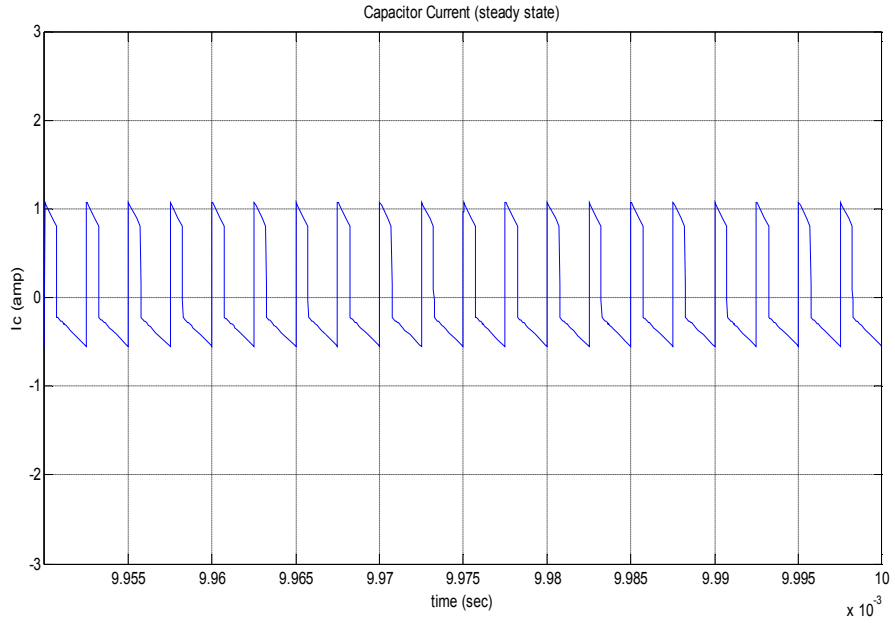

Fig 5.25 steady state capacitor current of four phase boost converter

5.5 Comparison of Single Phase and Four Phase Converters (in open loop)

5.5.1 Output Voltage Ripple

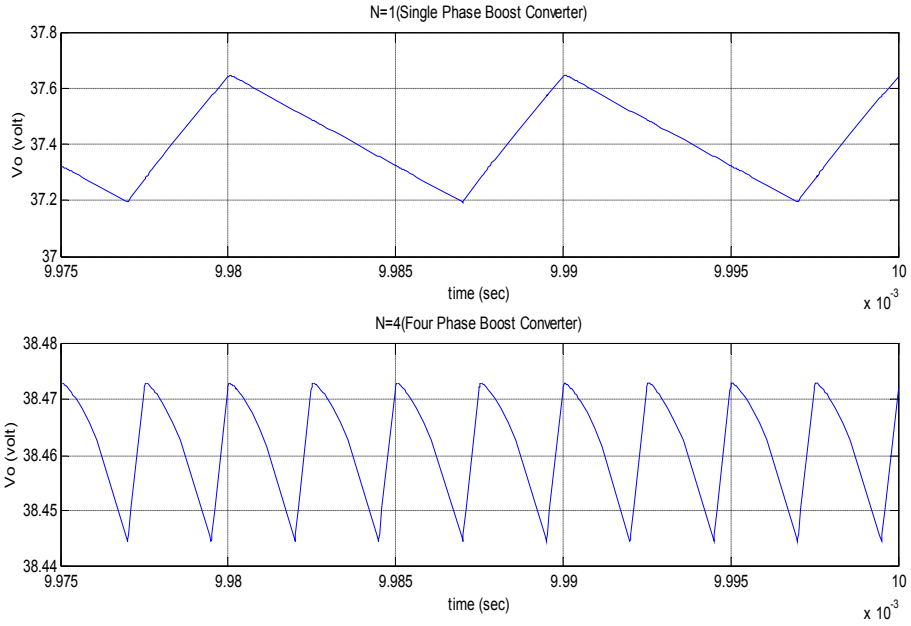

Fig 5.26 output voltage ripple of single phase (N=1) and four phase (N=4) Converters

5.5.2 Input Current Ripple

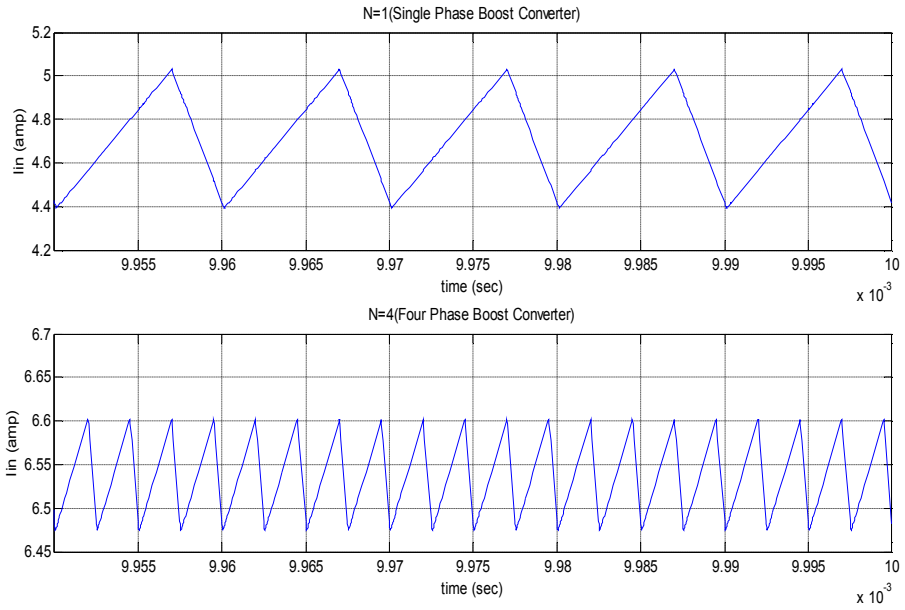

Fig 5.27 Input current ripple of single phase (N=1) and four phase (N=4) Converters

5.5.3 Steady State Capacitor Current

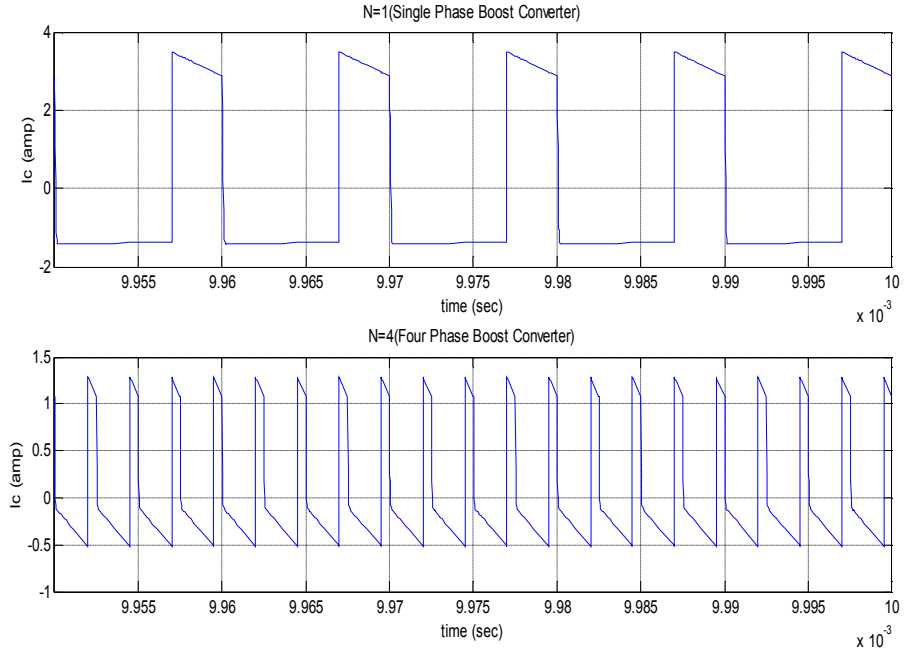

Fig 5.28 steady state capacitor of single phase (N=1) and four phase (N=4) Converters

5.6 Comparison of Single Phase and Four Phase Converters (in closed loop)

5.6.1 Output Voltage Ripple

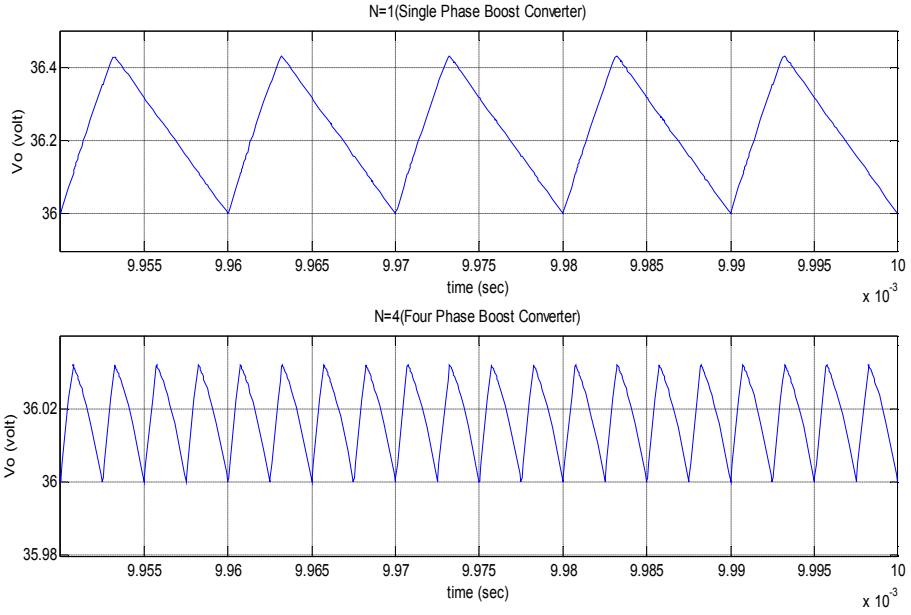

Fig 5.29 output voltage ripple of single phase (N=1) and four phase (N=4) Converters

5.6.2 Input Current Ripple

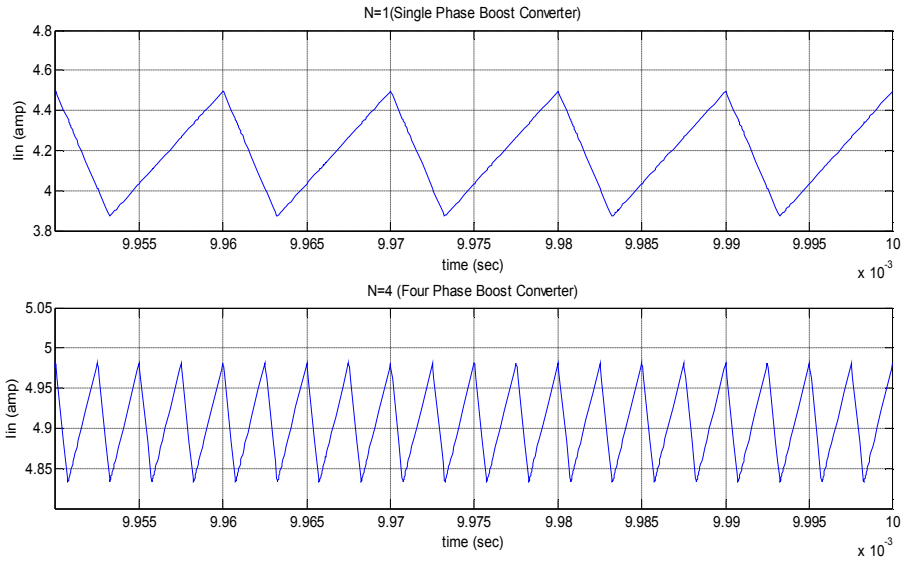

Fig 5.30 Input current ripple of single phase (N=1) and four phase (N=4) Converters

5.6.3 Steady State Capacitor Current

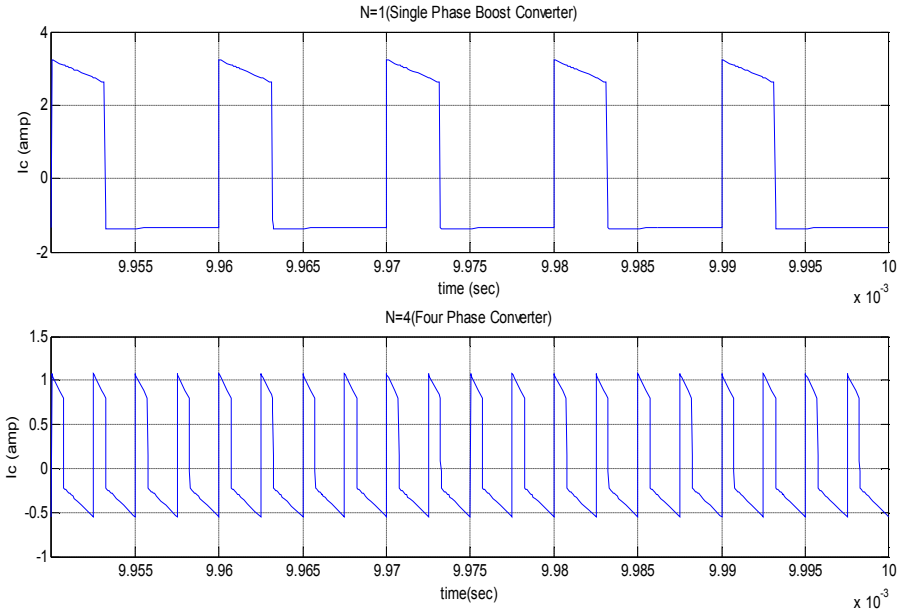

Fig 5.31 steady state capacitor of single phase (N=1) and four phase (N=4) Converters

5.7 Step Response of the Four Phase Boost Converter

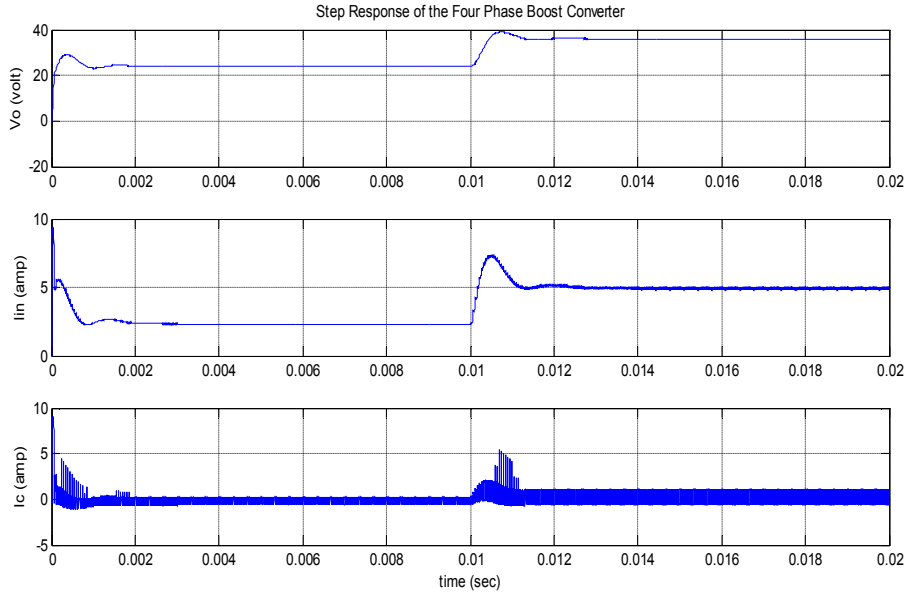

Fig 5.32 step response of the four phase boost converter

CHAPTER 6
CONCLUSION

6.1 Conclusion

This work discusses analysis and simulation for poly-phase boost converter. A modified method for determining the duty cycle corresponds to current control has been developed. The size of N boost converters in parallel is almost same as a single boost converter of the same total power because the size of main parts-inductors-almost remains same. Smaller RMS current in the energy-storage capacitor, lower input ripple current and lower output ripple voltage or smaller size of the tank capacitor are those important points, which have been considered. Moreover digital realization in control results in better performance and advantages, which cannot be achieved by Analog method. Programmability, modularity and flexibility in design and different operating conditions are major points, which have been addressed.

6.2 Future Work

The scope of future work is to implement the open loop and closed loop control of Poly-phase Boost Converter using the DSP TMS320LF2407.

REFERENCES

[1]. R. Mirzaei and V. Ramanarayanan, **"**Polyphase Boost Converter for Automotive and UPF Applications with Digital Control." NATIONAL POWER ELECTRONICS CONFERENCE, NPEC 2005.

[2]. R.Redl and L.Balogh, "Power-factor correction with interleaved boost converters in continuous-inductor-current mode." in Proc. APEC'93, pp.168–174.

[3]. R.Redl and L.Balogh, "RMS, DC, Peak, and Harmonic Currents in High-Frequency Power-Factor Correctors with Capacitive Energy Storage." in Proc. APEC 1992 pp. 533-540

[4]. R. Giral, L. Martinez-Salamero and S. Singer,"Interleaved Converters Operation Based on CMC." IEEE Trans Power Electron, vol. 14, no. 4, Jul 1999.

[5]. I. Cadirci, A. Yafavi and M. Ermis, "Unity power factor boost converter with phase shifted parallel IGBT operation for medium power applications." IEE. Proc.-Electr. Power Appl. Vol.149, No. 3, May 2002.

[6]. D. Maksimovic, R. Zane, and R. Erickson, "Impact of Digital Control in Power Electronics." IEEE International Symposium on Power Semiconductor Devices &Ics, Kitakyushu, Japan, May 2004.

[7]. J. Chen, A. Prodic, R. Erickson and D. Maksimovic, "Predictive Digital Current Programmed Control." IEEE Trans.Power Electron.,vol. 18, no. 1, Jan 2003, pp. 411-419.

[8]. S. Chattopadhyay and S. Das, "A Digital Current Mode Control Technique for DC-DC Converters" in Proc. APEC 2005, Vol. 2, pp. 885-891.

[9]. R.D. Middlebrook, S.C. Cuk, "Advance in Switched Mode Power Conversion." TeslaCO, Pasadena, USA, 1983.

[10]. P. Li and B. Lehman, “A design method for paralleling current mode controlled DC-DC converters,” IEEE Trans. on Power Electron., vol. 19, no. 3, May 2004.

[11]. Y. Panov, and M.M. Jovanovic, “Stability and dynamic performance of current-sharing control for paralleled voltage regulator modules”, IEEE Trans. Power Electron., vol. 17, no. 2, March 2002.

[12]. K. M. Smith and K. M. Smedley, “A comparison of active and passive soft switching methods for PWM converters”, Proc. IEEE PESC 1998, pp. 94–100.

[13]. G. Moschopoulos, P. Jain, and G. Joós, “A novel zero-voltage switched PWM boost converter”, Proc. IEEE PESC 1995, pp. 694–700.

[14]. G. Moschopoulos, P. Jain, Y.-F. Liu, and G. Joós, “A zero-voltage switched PWM boost converter with an energy feed forward auxiliary circuit.” Proc. IEEE PESC 1996, pp. 76–82.

[15]. C. M. C. Duarte and I. Barbi, “A new family of ZVS-PWM active clamping dc-to-dc converters: Analysis, design, and experimentation”, Proc. INTELEC 1996, pp. 305–312.

[16]. M. M. Jovanovic´, “A technique for reducing rectifier reverse-recovery related losses in high-voltage, high-power boost converters”, Proc. IEEE APEC 1997, pp. 1000–1007.

[17]. K. M. Smith and K. M. Smedley, “A comparison of voltage-mode soft switching methods for PWM converters,” IEEE Trans. Power Electron., vol. 12, no. 2, Mar. 1997.

[18]. C. J. Tseng and C.-L. Chen, “Novel ZVT-PWM converters with active snubbers.” IEEE Trans. Power Electron., vol. 13, no. 5, Sep. 1998.

[19]. M. M. Jovanovic´ and Y. Jang, “A new soft-switched boost converter with isolated

active snubber", Proc. IEEE APEC 1998, pp. 1084–1090.

[20]. T.-W. Kim, H.-S. Kim, and H.-W. Ahn, "An improved ZVT PWM converter." Proc. IEEE PESC 2000, pp. 615–619.

[21]. N. Jain, P. Jain, and G. Joós, "Analysis of a zero-voltage transition boost converter using a soft switching auxiliary circuit with reduced conduction losses", Proc. IEEE PESC 2001, pp. 1799–1804.

[22]. B. Feng and D. Xu, "1 kW pfc converter with compounded active- clamping", Proc. IEEE PESC 2002, pp. 1387–1391.

[23]. C. A. Canesin and I. Barbi, "Comparison of experimental loses among six different topologies for a 1.6 kW boost converter, using IGBT's", Proc. IEEE PESC 1995, pp.1265–1271.

[24]. M. Veerachary, ''Analysis of interleaved dual boost converter with integrated magnetics: signal flow graph approach'', IEE Proceedings Electrical Power Applications, 150, pp. 407–416, 2003.

[25]. P.A. Dahono, S. Riyadi, A. Mudawari and Y. Haroen, ''Output ripple analysis of multiphase DC–DC converter''. IEEE PEDS 1999, pp. 626–631, 1999.

[26]. M. Veerachary, T. Senjyu and K. Uezato, ''Maximum power point tracking of coupled inductor interleaved boost converter supplied PV system'', IEE Proceedings of Electrical Power Applications, 150, pp. 71–80, 2003.

[27]. P. Lee, Y. Lee, D.K.W. Cheng and X. Liu, ''Steady-state analysis of an interleaved boost converter with coupled inductors'', IEEE Trans. Ind. Electron., vol. 47, no. 4 Aug.2000.

[28]. K. C. Wu, 'Switch-Mode Power Converters: Design and Analysis" Academic Press 2005.

[29]. Kelly, A. and Rinne, K., "Sensor less current-mode control of a digital dead-beat DC-DC converter", Proc. IEEE APEC 2004, vol. 3, pp. 1790-1795.

[30]. D.S. Padimiti and M. Ferdowsi, "Review of Digital Control Techniques for Automotive DC-DC Converters." IEEE Vehicle Power and Propulsion, Sept. 2005.

[31]. C. M. Wang, "A New Single-Phase ZCS-PWM Boost Rectifier with High Power Factor and Low Conduction Losses." IEEE Trans. Ind. Electron. vol. 53 no. 2 April 2006.

[32]. C. M. Wang, "A Novel Zero-Voltage-Switching PWM Boost Rectifier with High Power Factor and Low Conduction Losses." IEEE Trans. Ind. Electron. vol. 52 no. 2 April 2005.