Photonic Interconnect based Switching and Logic Synthesis for High Performance Computing Applications

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CERTIFICATE

I, Harpreet Kaur, hereby declare that the work presented in this thesis entitled **"Photonic Interconnect based Switching and Logic Synthesis for High Performance Computing Applications"** in fulfillment of the requirement for the award of the degree of Doctor of Philosophy submitted at the Department of Electronics and Communication, Thapar Institute of Engineering and Technology, Patiala is an authentic record of work carried out under the supervision of **Dr. Rajinder Singh Kaler** (Senior Professor,ECED, TIET) during a period from Jan 2019 to Jan 2023.

The matter presented in this thesis has not been submitted either in part or full to any other university or institute for the award of any other degree.

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ABSTRACT

The widespread web-based applications are attracting extensive acceptance and deployment due to easy accessibility. The voluntary usage of social networking platforms by millions of users has forced various organizations to install extensively huge data centers (DCs). The large-scale industrial fields like health, engineering, commercial, defense, etc. employing High-Performance Computation (HPC) networks depend on these data centers. The "big data" flowing every second requires minimum possible error and faster processing to ensure high quality of service. The major issue of this multimedia transmission arises when the user-traffic is at its peak and DCs face a load-balancing problem and higher latency while switching this traffic. This questions the present DC configuration and its efficiency.

HPC systems handling complex tasks along with artificial intelligence, on the other hand, demand highly scalable structures with low latency. The current hybrid electro-optic technology entails large power consumption during electro-optic (E-O) and optic-electro (O-E) conversions. In addition, if the switching and processing of big data are continued in the electronics domain then its full potential cannot be exploited due to the increasing complexity of cables and it will eventually limit the scalability of DCs. The all-optic platforms can overrun the limitations of these challenges by offering many other positive advantages like a large bit rate, massive bandwidth, low reception-error, and reliable cost. The attractive features of optical switching technology in DCs offer promising solutions to various networking problems.

Although the extensive deployment of various optical switching technologies has proposed countless innovative schemes to overcome the challenges but the designing demands have always been an obstruction in DC switch performance. The high-radix interconnected structure utilizing MEMS-based technologies faces a large response time whereas liquid crystal-based configurations offer low power consumption but scalability remined an issue. Thermo-optic switches require large operating power and hence have a lower preference for DC applications. It is observed that SOA-based technologies have the ability to overcome their internal non-linear issues and offer solutions to the above limitations. These structures don't need any large coolants and offer low-power operation. In addition, the non-linear properties of SOA when exploited in Mach-Zehnder Interferometric (MZI) configuration can achieve many self-switching capabilities with the

inevitable speed that adds to the superiority of the structure. The employment of MZI configurations suffers various limitations like poor crosstalk and low extinction ratio but with appropriate usage of its properties, its applicability in several fields can picture future switching structures with guaranteed scalability upgradations with time. This thesis facilitates a promising photonic switching technique that can balance the incoming traffic with definite speed and offers good service quality for high performance computing applications.

Initially, the best suitable combination for photonic switching has been explored which is superior to previously reported techniques. The cross-phase modulation property (XPM) in Traveling Wave SOA i.e. TWSOA has been tested with Symmetric MZI i.e. SMZI to obtain the crossbar operation at the elementary level and power distribution in terms of gain has been presented. With the use of this elementary block, the TWSOA-SMZI photonic switch is proposed by increasing the input and output port-size to 4×4. The performance of this 4×4 crossbar switch is measured for various parameters like BER, latency, OSNR, ER, output power, eye-opening, and eye-height for ensuring scalability. In the next step, the high-radix configuration has been investigated by increasing the port-size further to 8×8. The scalability of the structure is monitored with the same parameters as 2×2 and 4×4. The performance of a three-stage 8×8 switch is examined by exploring the impact of varying injection currents of SOA. The other results are presented by decreasing the port spacing in THz to ensure the further possibility of scalability in the proposed configuration. The investigations explain the relation of carrier density with TWSOA gain w.r.t. injection current. The large values of injection current can vary the non-linearities occurring in the transmission route which further opens doors to explore the in-path non-linearities.

The optical non-linear phenomenon like noise and crosstalk can worsen the performance of switching arrangements. They are able to modify the incoming input bits traveling through the channel by affecting the refractive index of the medium. The crosstalk is considered at its peak when a crossbar switch is operated in the cross-state. The switch parametric analysis of the proposed structure is examined parallelly with non-linearities of SOA that could affect the final performance at the destination. This thesis presents analytical modelling of non-linear crosstalk and proposes a solution to minimize its effects on the output signal. The relation of the occurrence of logic ’1’ at different places in the input sequence is also observed. The high logic appearance at alternate and consecutive places affects the output due to the MZI phase shifts occurring above the

threshold. It further explains how the biasing current of TWSOA can control these phase shifts and hence the ER impairments. The other results explain the changing output effects with the length of input sequences.

The structure is explored further on TWSOA's birefringent property that certifies its polarization dependent output and further proposes a solution to remove the polarization-sensitivity by adding another type of amplifier in the middle stages. It further explains the benefits of adding EDFA-SMZI loops in the second stage and further upgrades the proposed structure to S-E-S hybrid compound amplification-based 8×8 photonic switching. This structure studies the fundamental components of polarization ellipse in terms of Stokes parameters and the Poincaré sphere. It compares the polarization sensitivity of basic SOA-MZI loop and EDFA-based hybrid structure for achieving ultrafast response.

Switching the signal to an output port and blindly sending it on a particular I/O path that is not available at the moment will only increase or add to the switching time and hence negatively contributes to the latency. Hence, the proposed S-E-S switching configuration is further explored on an innovative level of smart switching for DC applications. This level includes the incorporation of neural networks parallelly with an optical switch. Firstly, the basic introduction to the working of Artificial Neural Networks (ANN) and their various types is presented. This investigation is further explored to discover the best suitable ANN for predicting the switching path. This brings in the study of the Recurrent Neural Network (RNN) based Long-Short-Term Memory (LSTM) neural network and its activation functions. Secondly, the implementation of the LSTM network for predicting the best suited port-destination path in terms of shortest distance and minimum error is done. This process achieves a prediction accuracy of 97% and the classification of minimum and maximum error paths is done with a classification accuracy of 99.5%. The LSTM network performance is further explored on the basis of the confusion matrix and the final improved results of the switching configuration are acquired.

This investigation leaves with the exploration of the availability of port that is decided by the LSTM network based on error-rate. Hence, further upgradation is done by feeding both the current port power and error-rate at the training of the LSTM network so that it predicts and classifies the data on the basis of availability and minimum error-based shortest path. It first samples the data

for path availability by determining the average port power and calculates the minimum distance port-path combinations and then classifies those paths with BER. This solves the problem of finding an available port for switching traffic data. The training of the LSTM network is measured with batch loss and RMSE and testing parameters give a classification accuracy of 99.7%. The improved switching parametric results are obtained with a maximum throughput of 96 Tbps. Hence, it proves a better solution to switching challenges for HPC systems in DCs.

The three-stage hierarchies of DC networks also face the issue of scaling the required information and forwarding it upper level based on priority. The investigations have also been done in Control Plane Interface (CPI) routing for achieving a smart solution for scheduling the incoming traffic. The logic gating-based smart routing technique is presented that utilizes the information from the header of the incoming node requests. The priority bit in the header tells whether the immediate transfer of the message is required or it could be put in wait-status for another important signal to pass through. The proposed AND-OR logic gating-based routing allows the appropriate scheduling and controlling of incoming traffic and it further proves the excellency in terms of insertion loss and contrast ratio.

The ultrafast scalable compound hybrid amplification-based photonic smart switching structure utilizing TWSOA-EDFA-TWSOA in SMZI arrangement has been implemented in parallel incorporation of the deep learning LSTM model that provides a solution to various challenges of existing switching techniques in Data Centers. The logic-routing scheme for the Control plane Interface is also established for removing the centralized control problems.

LIST OF PUBLICATIONS

This thesis includes the following published research papers:

SCI Publications:

[1] H. Kaur and R. S. Kaler, "SOA-MZI based 4×4 interconnected crossbar photonic wavelength switching for datacenter load balancing", **SPIE**: Optical Engineering, vol. 59, no. 11, pp. 117109 (1-10), Nov. 2020. https://doi.org/10.1117/1.OE.59.11.117109

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[2] H. Kaur and R. S. Kaler, "XPoM-based 8-port photonic interconnection with low polarization sensitivity utilizing S–E–S hybridization", **World Scientific**: Journal of Nonlinear Optical Physics & Materials, vol. 32, no. 3, pp. 2350030 (1-11), Sept. 2022. https://doi.org/10.1142/S0218863523500303

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[3] H. Kaur and R. S. Kaler, "Response investigation of 3-stage 8× 8 low-latency wideband TW-SOA switch for high-performance computing applications", **Springer**: Optical and Quantum Electronics, vol. 54, pp. 1-12, Sept. 2022. https://doi.org/10.1007/s11082-022-04187-5

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[4] H. Kaur and R. S. Kaler, "Ultrafast polarization self-switching with enhanced OSNR utilizing SOA and Erbium-doped amplifier-based compound photonic amplification", **Springer**: Optical and Quantum Electronics, vol. 55, pp. 1-12, Dec. 2022. https://doi.org/10.1007/s11082-022-04414-z

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[2] H. Kaur and R. S. Kaler, "Analytical modelling and Bit Sequence Impact Investigation of XPM-AMZI-induced Non-Linear Crosstalk in 4×4 Interconnect", Journal of Nonlinear Optical Physics & Materials, 2022.

[3] H. Kaur and R. S. Kaler, “Deep Neural Network-based Low Latent 8×8 Photonic Switching Interconnect using Port-wise Minimum-distance Evaluation for Handling Big-Data”, Wireless Personal Communications, 2022.

[4] H. Kaur and R. S. Kaler, “Deep Learning-based Port-Classification approach incorporating LSTM network for High-Throughput Data Center Interconnect”, Neural Computing and Applications, 2022.

[5] H. Kaur and R. S. Kaler, “Smart Logical Traffic Routing Technique for Control Plane Interface in Data Centers”, Journal of Modern Optics, 2022.

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Harpreet Kaur

Dedicated to my Parents

for their endless support, patience and

continuous encouragement

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LIST OF ACRONYMS

HPC	:	High-Performance Computing
DC	:	Data Centers
ITU	:	International Telecommunications Union
PI	:	Photonic Interconnects
O-E-O	:	Optical-Electrical-Optical
CPU	:	Central Processing Unit
DAC	:	Digital-to-Analog Converters
ADC	:	Analog-to-Digital Converters
AI	:	Artificial Intelligence
CMOS	:	Complementary Metal-Oxide Semiconductors
IC	:	Integrated Chip
WDM	:	Wavelength Division Multiplexing
MEMS	:	Micro-Electro-Mechanical System
OCS	:	Optical Circuit Switching
OPS	:	Optical Packet Switching
EPS	:	Electronic Packet Switching
OBS	:	Optical Burst Switching
BHP	:	Burst Header Packet
SOA	:	Semiconductor Optical Amplifier
XPM	:	Cross Phase Modulation
XGM	:	Cross Gain Modulation
FWM	:	Four Wave Mixing
RNN	:	Recurrent Neural Network
LSTM	:	Long-Short-Term-Memory
TWSOA	:	Travelling Wave Semiconductor Optical Amplifier
HyPaC	:	Hybrid Architecture of Packet and Circuit
HCF	:	Hashed Credits Fair
SDN	:	Software Defined Networking
MZI	:	Mach Zehnder Interferometer
IL	:	Insertion Loss

AWGR	:	Arrayed-Waveguide Grating Router
WSS	:	Wavelength Selective Switches
HSOL	:	High-Speed Optical Layer
MZM	:	Mach Zehnder Modulator
FPGA	:	Field Programmable Gate Array
BAS	:	Broadcast and Selective
SOI	:	Silicon on Insulator
PIC	:	Photonic Integrated Circuit
MRR	:	Micro-Ring Resonator
ASE	:	Amplified Spontaneous Emission
CW	:	Continuous Wave
TOAD	:	Terahertz optical asymmetric DEMUX
BER	:	Bit-Error-Rate
EDFA	:	Erbium Doped Fiber Amplifier
CPI	:	Control Plane Interface
ER	:	Extinction Ratio
XPolM	:	Cross Polarization Modulation
FSOA	:	Fabry-Perot Semiconductor Optical Amplifier
RSOA	:	Reflective Semiconductor Optical Amplifier
EOF	:	Eye-Opening Factor
QF	:	Quality Factor
EH	:	Eye-Height
MUX	:	Multiplexer
DEMUX	:	Demultiplexer
SMZI	:	Symmetric Mach Zehnder Interferometer
OSNR	:	Optical-Signal-to-Noise Ratio
PDL	:	Polarization Dependent Loss
PRBS	:	Pseudo-Random Bit Sequence
OOK	:	On-Off Keying
NRZ	:	Non-Return-to-Zero
CT	:	Crosstalk

R-E	:	Raman–EDFA
E-R-E	:	EDFA–Raman–EDFA
R-E-R	:	Raman–EDFA–Raman
S-E-S	:	SOA–EDFA–SOA
LP	:	Linear Polarizers
PC	:	Polarization Controller
CE	:	Conversion Efficiency
ANN	:	Artificial Neural Networks
ONN	:	Optical Neural Network
MLP	:	Multi-Layer Perceptron Model
RBFN	:	Radial Basis Function
MSE	:	Mean Square Error
RMSE	:	Root Mean Square Error
CNN	:	Convolutional Neural Networks
LAF	:	Linear Activation Functions
NLAF	:	Non-Linear Activation Function
ReLU	:	Rectified Linear Unit
ROADM	:	Reconfigurable Optical Add-Drop Multiplexer
NN	:	Neural Network
BLR	:	Base Learning Rate
TPR	:	True Positive Rate
PPV	:	Positive Prediction Value
TNR	:	True Negative Rate
NPV	:	Negative Prediction Value
ToR	:	Top-of-Rack
CR	:	Contrast Ratio
DL	:	Deep Learning

CHAPTER 1

INTRODUCTION

1.1 Introduction and Motivation

The cloud-based technologies have evolved vastly in the telecommunications industry further establishing an easily accessible networking solution that is attracting extensive acceptance and deployment. The extensive surge in advanced web-based applications such as social networking, the Internet of Things, video streaming, and easy accessibility of high-speed connectivity has accelerated the generation of large data every second. This has obligated various internet service benefactors to mount massive data centers (DC). Large-scale industries employing High-Performance Computing (HPC) applications house huge Data Centers (DC) that slowly widened their roots in medical, scientific, communication, household, commercial, and many other fields.

According to a report from Mordor Intelligence [1], the widespread growth of data centers has shown an increase of 3.4 billion USD from the year 2019 to 4.8 billion USD in the year 2025 as shown in Fig. 1.1.

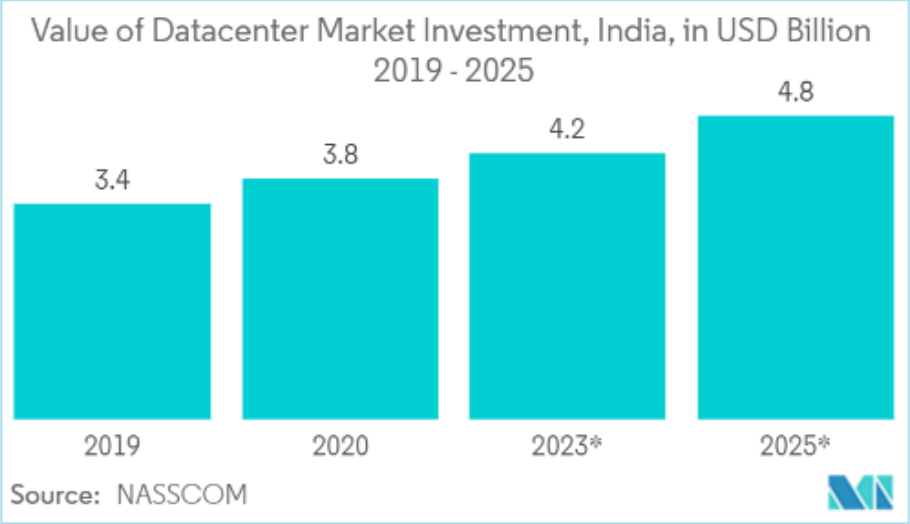


Fig. 1.1 Estimation of DC market investment in India 2019-2025 by NASSCOM [1]

According to an analysis by Precedence Research [2], with a CAGR of 6.7%, the global market size of DC construction is valued at 218.88 billion US dollars in the year 2021 and is estimated to

reach 369.6 billion US dollars by the year 2030. This estimation of the data center market is shown in Fig. 1.2.

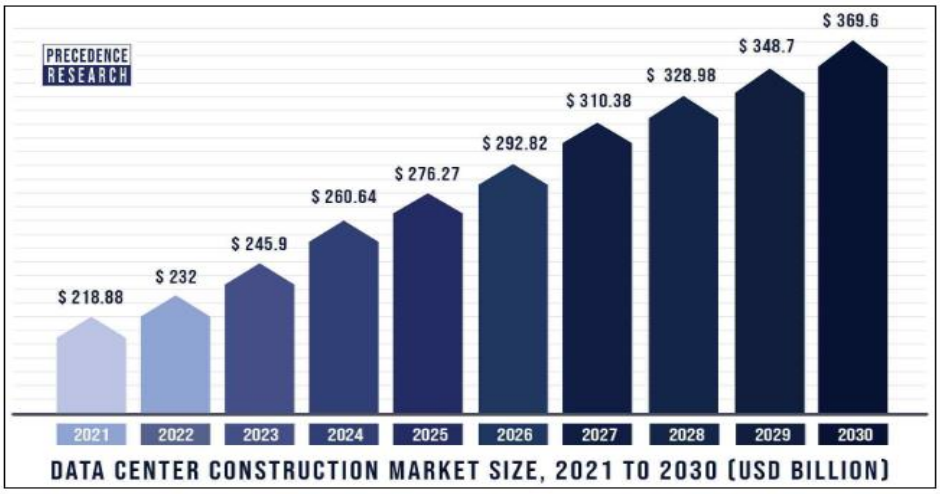


Fig. 1.2 Estimation of DC market size 2021-2030 by Precedence Research [2]

Recently, International Telecommunications Union has presented their estimation [3] of internet users and their increase from 1 billion users in the year 2005 to 5.3 billion users in 2023 shown in Fig. 1.3. This counts up to 66% of the total world's population leaving 2.7 billion people in offline status. This rapid increase in traffic makes it important for the upgradation of existing Data-Center infrastructures.

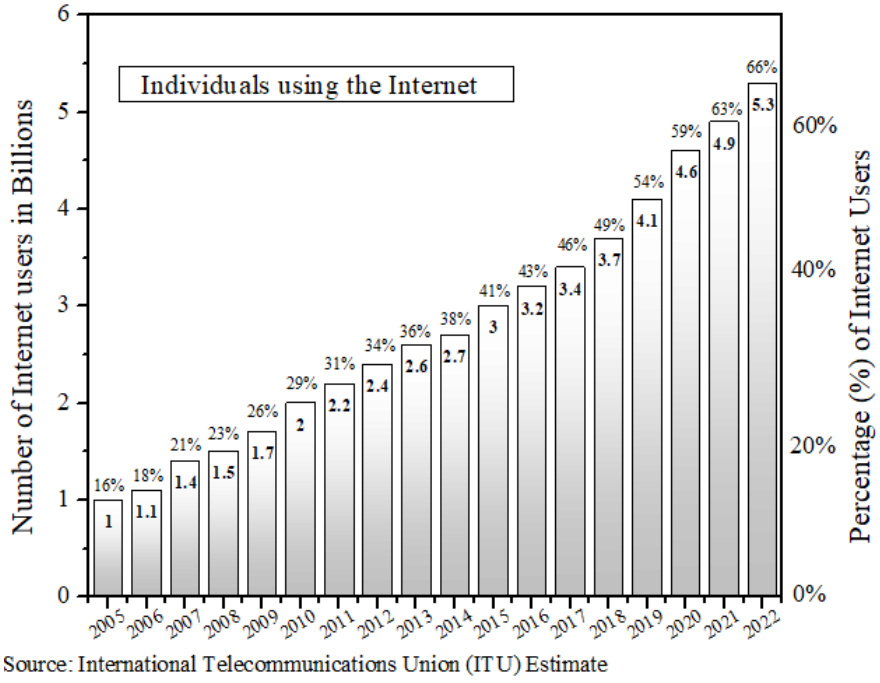


Fig. 1.3 ITU estimation of the increasing number of internet users [3]

The existing switches and servers in Facebook [4] have been upgraded to support the data rate of 10 Gbps. In other words, cloud workload and computation have been increased and more is expected in near future depending upon the number of internet users.

These data centers house hundreds of thousands, of servers on a very large scale. A complex network consisting of numerous optical links is the backbone of this intensive growth of multimedia information. These optical links process and store the floating "big data" among optical nodes established in data centers. This leads to a large amount of traffic that flows between both inter-datacenters and intra-datacenters.

In the recent COVID-19 crisis, the internet traffic jump was observed when challenges of accessing and creating online content were faced by data centers. This traffic is overtaking the capacities of DCs because of high power consumption, load-balancing problem, and slow rate of data switching which further leads to degraded system performance. These challenges questioned the present size, capabilities, power efficiency, and data rates of data centers. As the rate of data transportation is expected to match the rate of the increasing size of data centers with millions of servers, the predictable future requirement of bandwidth of internet-based applications is in order of Tera bits per second [5]. To achieve this bandwidth demand, it is necessary to provide fast access and switching of data when it comes to High-Performance Computation (HPC) where there is a critical need for highly scalable structures that offer minimum latency. The hybrid switching interconnect technology has inspired several solutions but the amount of power consumption during the conversion of data from electrical to optical (E-O) domain and via-viz (O-E) has cost performance degradation and format-dependency. On the other hand, all-optical technologies are employed in the processing of data because of their unique characteristics like enormous bit rate, high bandwidth, transparency, low power consumption, and flexibility. Hence, all-photonic switching technology is considered a promising solution for DC networking challenges.

1.2 Importance of Photonic Interconnects (PI)

Photonics is widely considered an enabling technology that offers progressive innovations with its broad spectrum of commercial applications. Photonic Interconnect (PI) approach is considered a successor to electrical interconnect technology to accomplish the future requirements of HPC systems in growing data centers. The basic purpose of interconnect may be to communicate the

data to and from sub-links present between transmitter and receiver, but for HPC systems, it has become the bottleneck between memory and central processing unit (CPU). Although the current communication links and memory interfaces are utilizing the copper/electrical approach, with the decrease in the length of copper wires, they are reaching their limit of bit-rate offerings. This further leads to power consumption and makes it more distance-dependent. Photonics interconnects are more transparent to signaling rate and also offer partial freedom of capacitive loads [6]. In addition to this, PIs provide routing flexibility by removing mechanical contacts. Their independency on the mutual coupling effect, which is a function of signal frequency, can help mitigate optical scattering and further proves advantageous in contrast to conventional interconnects. These benefits help in a compact, energy-efficient innovative fabrics which allow large stability, low cost, and high radix for optical switching.

1.2.1 Photonic Interconnect for Data Center (DC) Computation

Impressive data processing and storage capabilities have been reached through continuous technological improvement in integrated circuits. The several interconnection architectures starting from the highest level of hierarchy to its lowest [6], we have:

1) *Machine-to-machine interconnections:* These interconnections are useful in the transfer of messages attached to e-mails or coming from shared databases and that is required to cover a distance of a few meters to kilometers.
2) *Processor-to-processor interconnections:* These interconnections are utilized within the multiprocessor interfaces in a single machine where the pattern of interconnection can change dynamically while traveling a distance of a few centimeters to a few meters.
3) *Board-to-board interconnections:* These interconnections are needed when the information is required to exchange between the various electronic boards existing between a single processing unit by a data bus. The data traveling distance is as small as a few centimeters to one meter.
4) *Chip-to-chip interconnections:* These wafer-level interconnections are utilized between the chips integrated on the boards to transfer the information from 0.1 centimeters to the order of a few tens of centimeters.
5) *Intra-chip or On-chip interconnections:* These interconnections have their usage when the data connection is required between the gates and various sub-functional units embedded on a chip.

This intra-chip connection helps in transferring the data to the outside world within a few microseconds. The distance of such interconnections is a few micrometers only.

A typical DC computation utilizes the interconnection of different size switches in cascaded stages that demand low latency, high scalability with high throughput, and low power consumption. The DC on-chip interconnects comprise a large number of optical links embedded on a single chip whose multiplexing can be achieved on various levels of the cascaded unit. One of the most popular three-layered hierarchical configurations is shown in Fig. 1.4. This is also called a conventional data center network. The layer of servers is interconnected with the help of a Top-of-Rack i.e. ToR switch which locally communicates with aggregate switches [7]. Although the structure till the aggregate layer is made to support high-end nodes, it is highly dependent on over-subscription. But when there is a need of connecting more devices, there is still the requirement for a high-capacity core layer.

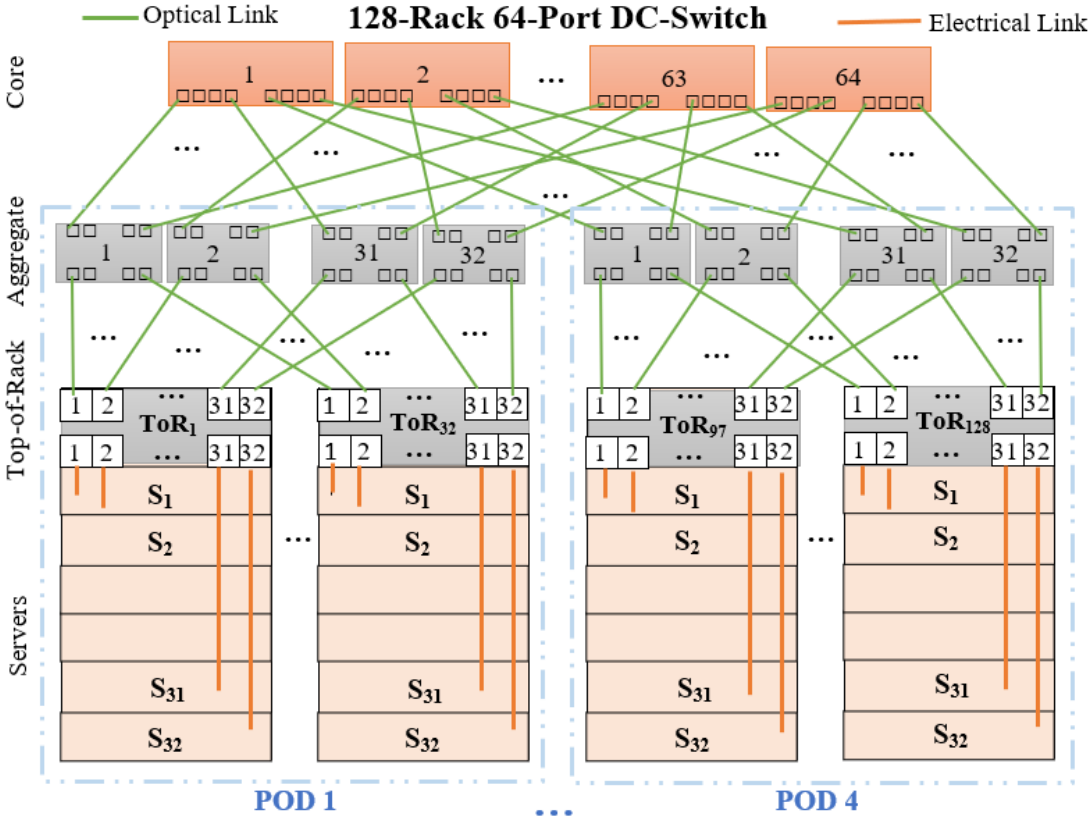


Fig. 1.4 Three-layered hierarchical DC-switch configuration with 128 racks and 64 ports

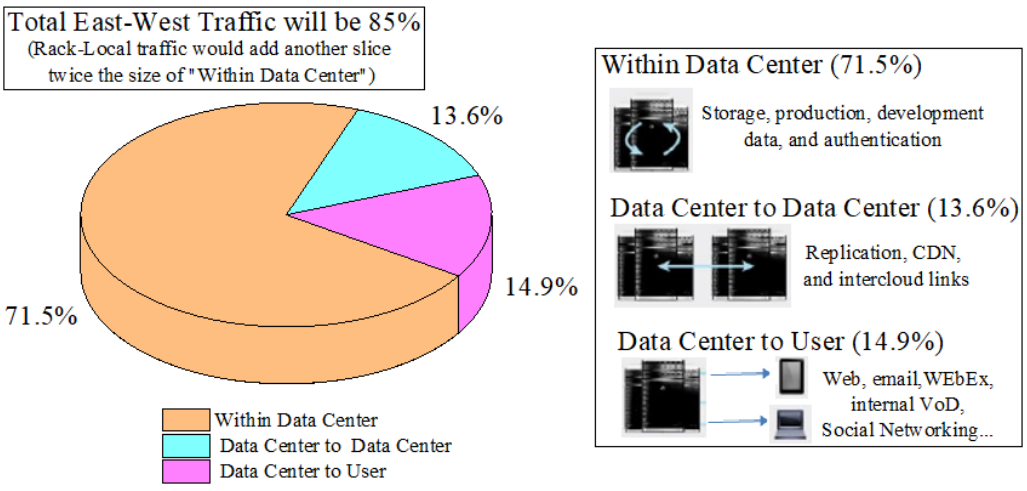
Hence these switches are further connected with high-performance core switches which usually have the aggregation of various 10GE interfaces. These various layers make the big data packets

take a large number of hops till it reaches the receiver end. This adds to the poor latency of the overall network. Hence, the existing hierarchical structure is not best suited for large traffic.

Further, the increasing traffic size requires a large network bandwidth that impacts the processors and memory. According to the Cisco Global Index DC report [8], if this traffic is categorized and studied, there are normally three types:

1) 71.5% of the traffic is within the data center and moves from a development environment to a production environment.
2) 13.6% of the data traffic moves from one data center to another using cloud computing for content distribution.
3) 14.9% of the traffic data flow from data centers to end users via emails, video streaming, and social networking sites.

The above statistics don't include the traffic that remains within the server rack called rack-local traffic. If rack-local traffic is included, Cisco estimates the distribution shown in Fig. 1.5 will change and illustrates more than 90% of traffic remaining local to DC. The big data traffic is rack-local and corresponds to 20% of all traffic within a DC [8]. Therefore, new integration platforms with innovative interconnect technology are needed at every level.



Source: Cisco Global Cloud Index

Fig. 1.5 Data Center flow of traffic statistics by Cisco Global Cloud Index [8]

The widely used DC photonic interconnection configurations are based on components utilized in optical communication. A basic point-to-point can be formed with the help of an optical source

that generates the optical signal. The modulator is utilized further to modulate the signal by the associated electrical driver. The signal further flows through an optical channel where various other optical components are present for coupling the signal to various ports present in the network on the chip. These could be couplers that couple the data according to the ratio set by the manufacturer. Passive devices like splitters and combiners help in splitting the data at the transmitter side and combines the optical wave at the receiver end. Finally, the photodetector can be utilized with appropriate filters and amplifiers for post-processing of the data. For energy efficiency, it is preferred to use photonic point links that do not require any power-hungry components like digital-to-analog converters (DAC), clock recovery, and analog-to-digital converters (ADC).

1.2.2 High-Performance Computation Challenges in Data Centers

High-Performance Computation (HPC) is dedicated to systems that demand big data processing in extremely limited time. It enables various organizations to parallel process their data while performing high-end programs like Artificial Intelligence (AI). Hence, it combines various processing units to compute complex tasks. Data centers handle various intensive responsibilities like fiscal risk modeling and resource tracking. Such tasks depend highly on AI technology that can be benefited from HPC. The accessing, and monitoring of data is expected in real-time from HPC to bring new groundbreaking innovations into the picture. According to a survey by Emergen Research [9], Amazon, Dell, IBM, Microsoft, Intel, and Atos have started to provide solutions to problems using HPC to combine AI and data analytics to achieve accuracy at faster speeds. The areas like cloud computing have been encouraged by various IT industries including applications in Oil and Gas, Media, Health, Defense, Government, Research, and Entertainment. Data centers supporting HPC technology can accommodate regularly growing requirements of fast processing. The use of photonic board-board interconnects for commercial servers and computing systems gives promising improvements [10] in crosstalk and ground noise coupling.

Several other drivers embracing HPC-based systems because of the dynamic underlying market have the following reasons:

1. Growing attractiveness in autonomous vehicles i.e. driverless vehicles proficient in sensing the environment and driving self without manual operation.

2. Appealing popular businesses like Small and medium-sized enterprises have added cloud HPC services.
3. An endeavor to promote standardization by lowering prices of HPC-based equipment.
4. Worldwide acceptance and hence country-level competition to foster HPC initiatives.
5. Frequent up-gradation of data centers for increasing the life cycle of HPC and adapting to the supporting environment.
6. Commercial strategy of on-demand cloud offering to surge business modeling.
7. Fulfilling customer technical requirements and being sensitive to green IT.

Up to this date, HPC servers operate public facilities often with big data on exascale supercomputers that require several dozens of MW of power to handle such load. On the other hand, private facilities have moderate data that can be handled with 1-2 MW of power or even less. On the public handling, the high-power issues are mitigated by cooling components which limits the number of off-premises data centers with HPC. Some of these are developing fast in European countries like Sweden, Finland, Iceland, and Norway because of favorable cool climate conditions and low cost of electricity.

In addition, big data handling requires various capabilities that have large layered embedded architectures [11-12]. One of the layered architectures proposed by NIST [11] has the following different stages:

1. *Layer 1:* Providing adaptable infrastructures like hardware resources including storage, CPU, external memory devices, and interconnects. These support various heterogeneous responsibilities that are important for the parallel processing of big data. Hence, for some systems setups like cloud computing is the key infrastructure for this layer.
2. *Layer 2:* Platform for organizing and distributing the parallel processing programs for applications like data mining and machine learning.
3. *Layer 3:* Computing and executing programs parallelly for live streaming the data batch.
4. *Layer 4:* Application stage for processing and analyzing solutions for big data and creating interacting interfaces for the real world. It also has the access to inquiring and preparing data visualizations.

5. *Layer 5:* Structure orchestrator for completing system needs of governing, monitoring activities, and resourcing.

Hence, this becomes essential to introduce either software-based approaches or infrastructure to support new developments projected for the future. This introduction of new approaches should match the programming, runtime, and compiling requirements of HPC. But the problems of bandwidth requirement, handling the increasing number of users, power efficiency, and achieving real-time speeds [13] are potentially mitigated by numerous photonic switching architectures.

1.3 Motivation for Photonic Switching in DC

As the signal processing of the flowing big data is usually carried out in the electronics domain utilizing Integrated Chips (IC) and Complementary metal-oxide semiconductors (CMOS) [14], the full potential of this technology still couldn't be exploited due to the increasing cabling complexity and limited scalability. So, the first step is designing a perfectly efficient DC interconnect is to choose the suitable switching technology. The adaption of photonic switching in data center computations will bring an evolutionary trend as it offers promising solutions to various networking problems. The research interest in DC optical switching has been increasing every year.

There is a renewed focus on photonic switching because of its other numerous advantages to match with substantial development in the transmission and processing of data. Some of these striking benefits are listed below:

1. *Ultra-high capacity:* Optical communication offers a bandwidth of nearly 10^5 GHz and supports data rates of 50 Tbps where state-of-art research is performed utilizing hundreds of wavelengths with single core fiber [15]. This usable bandwidth is affected by a single parameter of the optical carrier. So, there is a need of sending several signals at different wavelengths parallelly on the same fiber. This process of Wavelength Division Multiplexing (WDM) is also limited when the channel spacing is further decreased to accommodate a large number of users. Due to complex routing algorithms in WDM, photonic switching can exploit various areas of this bandwidth.
2. *Low power consumption:* The most imperative characteristic that photonic links and switches can provide is their capability of consuming less power [16] for long links and offering limited requirements of regeneration. Other features like data rate transparency make it a power-

efficient technology as it utilizes the power which is independent of the bandwidth for switching. Hence, low power is consumed in comparison to electronic switches.

3. *Cost:* The cost of electronic switches is highly influenced by scale economy segments of small markets but these are less dominant in markets demanding high-speed components like fifth generation i.e. 5G [17]. Another cost factor can be considered for long-haul applications where OEO conversions are required. Hence, all-optic technology provides strong competition to electronic/electrical switching links and is beneficial in its applicability in large industrial societies with an exception of cost.
4. *High-speed:* The data center switches have usually hundreds of thousands of end nodes which brings to their strict real-time requirement of low latency [18]. Even a small delay of nanoseconds in one node can add up to several thousand nanoseconds to the DC switch as a whole. The electronics switches are not capable of extending the port scalability without compromising the latency. As the all-photonic switching technology doesn't follow the store-and-forward mechanism, the data is switched in a very small time and with low latency.

On the other hand, fiber-based data propagation technologies have complex routing problems [18,195] with large-sized buffered traffic. To avoid these routing problems, optical-electrical-optical (OEO) converters are utilized so that routing could be done in the electrical domain. This conversion further adds to large switching times, complex hardware, large processing, and cost expensive challenges. So, looking at the proliferation in the number of users, the focus needs to be given to all-photonic switching which is to be adopted at the metro-level and intra-datacenter level.

1.3.1 Recent Advancements in DC Switching

In comparison to aggregate and ToR switches, core switches advancements are more prioritized because of their ability to handle large workloads. Huge market holder corporations like Amazon, and Netflix are on their way to developing new data center core switches that will help in meeting their requirement of handling growing traffic. Some of the recent advancement in DC switches has been presented below:

- The March 2021 report illustrates the introduction of [19] 32-port 200 GbE switches in Hewlett Packard Enterprise (**HPE**). These switches carry bidirectional capability with a processing rate of 12.8 Tbps.

- In April 2021, Altlanta **QTS** Data Center submitted innovative plans aiming enterprise market to construct 1.1 million square feet DC with the name 'Project Granite'. The power demands of such developments further require DC switching products.
- The three-tier DC architecture uses a virtual port channel that only supplies two active parallel uplinks; hence latency becomes the issue. To cope with this challenge, **Cisco** introduces a network-based spine-and-leaf Clos architecture that provides non-obstructive server-server connections, low latency, and high bandwidth.

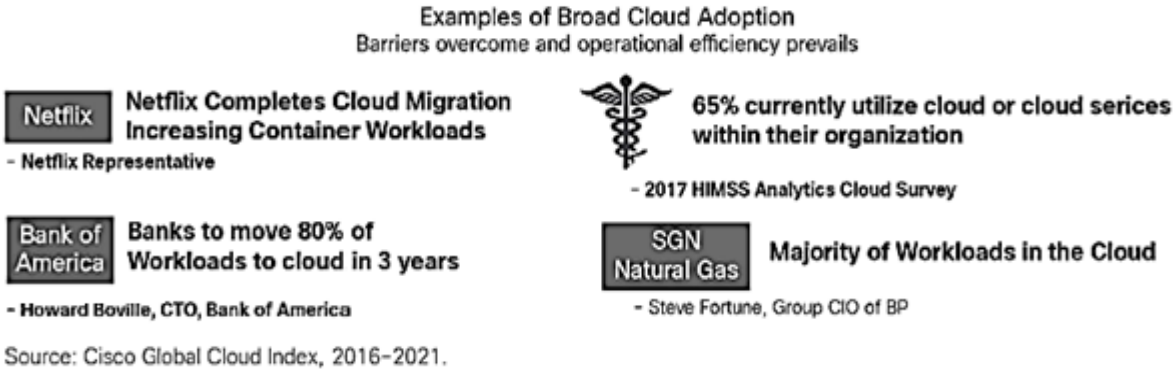


Fig. 1.6 Cisco Global Cloud Index [8] illustrating cloud adoption

- The **Cisco** plan in partnership with **PLDT** [19] operator of the Philippines has reported separate 5G platform installation in the existing TechoLab at Makati. It is expected to provide the 5G sandbox network to develop digital use cases for all-sized enterprises.
- **Netflix,** in 2016, first announced the shutdown of its traditional DC and the acceptance of a cloud-based platform. The statistics regarding the adoption of cloud by various industries are shown in Fig. 1.6. But the COVID-19 pandemic situation offered Netflix to introduce over-the-top (OTT) services [8] in the first 3-months of the year 2020 which attracted over 3.6 million subscribers across Asian-Pacific region. To mitigate interference between the signal and maintain streaming quality, Netflix removed the uppermost bandwidth streams to lessen 25% of the traffic.
- Recently in February 2022, **Meta**, the parent company of Facebook Inc., declared its intention of expanding DC markets with an $800 million investment [19] in a hyperscale campus in Idaho. The complexity and demand of networking components like routers and high-performance core switches will be critical for hyper-scale infrastructures for fast data transfer.

- Another advancement in February 2022 has been noticed when [20] **Corscale** with USAA Real Estate set up a DC expansion platform in North Virginia. Earlier development was reported in Prine Williams country with five optimized DC podiums utilizing 300 MW which fascinated 200 GbE and 400 GbE switching ports recently.
- In October 2021, [19] **HPE** also reported the distribution of server switches of the CX 10000 series to be deployed in software-defined services for easy creation and data processing while diminishing the latency issues. These switches will allow the mass software to construct the hybrid cloud required by the major IT companies these days by providing new switching solutions.

1.4 Optical Switching Architectures in DC

1.4.1 Intra-DC architectures

The data center networks are commonly classified as Clos-based topology with centralized control where product switches are ordered in multiple tier form for constructing large multi-tier switching fabric [21]. Photonic switching technologies are categorized into three basic forms based on their switching granularity:

1. *Circuit Switching Technology:* It is a coarse-grained technique that is dedicated to point-to-point links between transmitter and receiver fiber pair. It gives guaranteed bandwidth exploitation and good quality of service. For data center applications, this technology has a slow but high-capacity micro-electro-mechanical system (MEMS) that delivers straight interconnections between the access switching layer. The sluggish behavior of optical circuit switching (OCS) eventually creates traffic flow overheads like bulky datasets that require more transfer time and are less flexible for big data handling. The OCS-based switching mechanisms utilized in data centers are:
    - Hybrid c-Through Structures
    - Hybrid Helios Structures

But to embrace the structure elasticity at a higher level, the flexible OCS and optical packet switching (OPS) architectures are employed in data centers with various modulation formats, security codes, and dynamic spectrum allocation mechanisms to increase the channel capacity of

attaining more users with limited burst traffic issues. This efficiency is also increased by including sub-channels to construct a super-channel for large data processing.

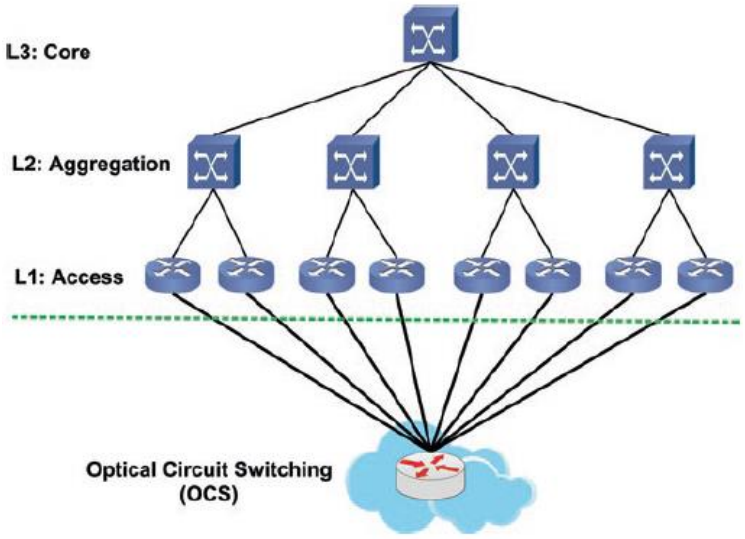


Fig. 1.7 Illustration of a hybrid c-Through network [22]

The basic system-level types of the hybrid packet and circuit switching structures are c-Through and Helios. The c-Through network [22] shown in Fig. 1.7 uses three staged tree-topology whereas the Helios network [23] illustrated in Fig. 1.8 has two-staged networks with several roots.

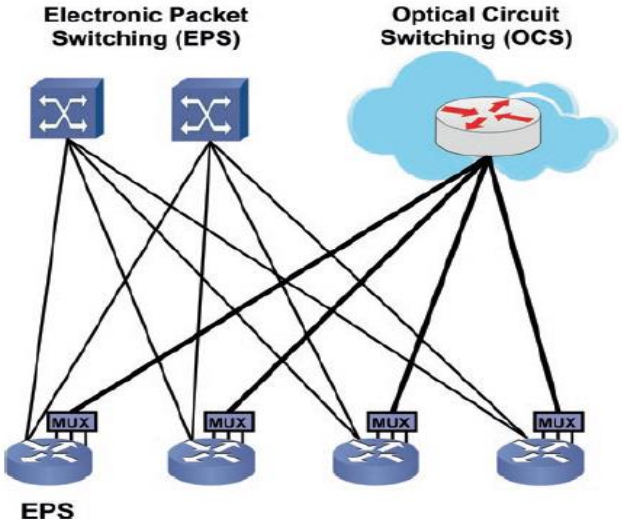


Fig. 1.8 Illustration of hybrid Helios network [23]

The alone circuit-switching configuration can provide [24] identicality at the rack level. This photonic switch is configured with high-bandwidth racks and the rest of the communication is examined with Ethernet switching.

The hybrid structure incorporates the conventional electronic packet switching (EPS) for the supervision of small traffic with circuit switching bandwidth advantages for large volumes. Like OCS has direct interconnections, similarly, the Helios in Fig. 1.8 has Wavelength Division Multiplexing (WDM) units that help in expanding the capacity of the system. The EPS is kept for all-to-all communication links and the photonic switching part is utilized for monitoring high-bandwidth changes between the pod switches. The vital implication of hybridizations in DC switching is to provide optimized resources from the collaboration of different switching fabrics. This further helps in the estimation of traffic.

The above-mentioned hybrid structures propose an outlook on efficient DC networking with the help of EPS and OCS mechanisms, they can provide reliability and increase capacity to some extent without requiring the complete replacement of hardware. But with the requirement of low and low switching time, shorter-span traffic needs to be switched in a pure optical domain to lessen the energy consumption, reduce cooling constraints of EPS, and mitigate overloading. Eventually, large-radix fabrics with low switching time in the order of nanoseconds are considered the future of DC networking above the EPS systems.

2. *Packet Switching technology:* In contrast to OCS, the packet switching technology shown in Fig. 1.9 is flexible as it supports a faster switching process with huge data or burst traffic. Optical packet switching (OPS) is expected to exploit all the features and advantages of DC switching.

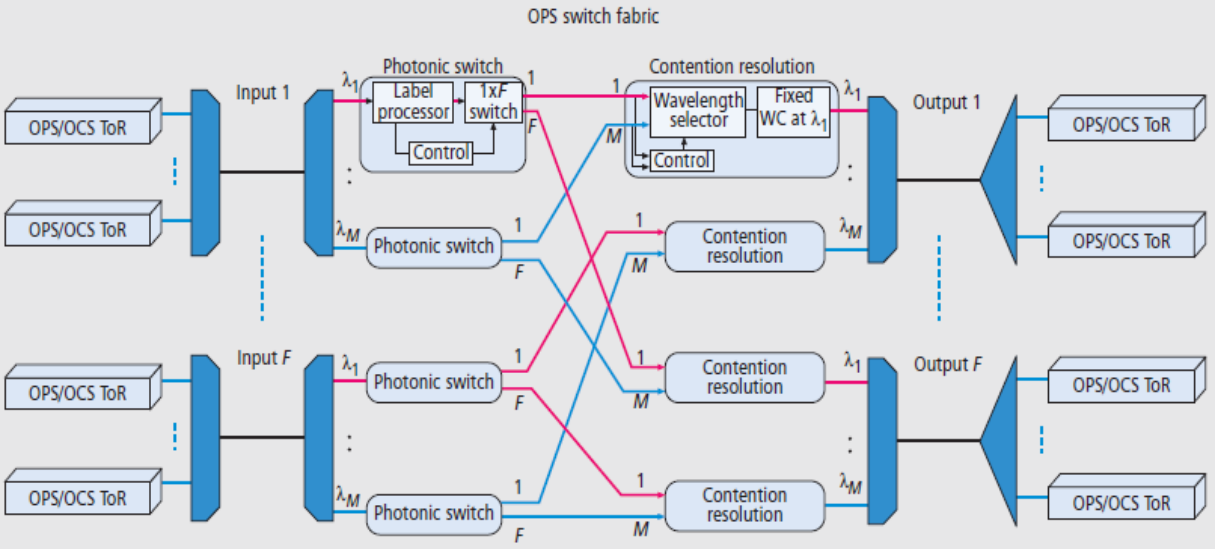


Fig. 1.9 OPS-based switch fabric assembled with discrete photonic components [24]

The major issue in OPS is that it requires the processing of packet header at a very high speed and due to the lack of proper buffering mechanisms, it seems that the commercial deployment of OPS is difficult and also cost expensive. But the connection is not required to be reserved in advance before the data is transferred and bandwidth is utilized more efficiently. These features of OPS are a good example of providing on-demand dataset transmission and hence making it a promising candidate for DC applications.

3. *Burst Switching Technology:* The third type of switching mechanism that is considered to mitigate all the above-mentioned issues is optical burst switching (OBS). These switches have promising features like flexibility, are highly adaptable, measured the consumption of resources, and are capable to cope with burst traffic conditions [197]. It uses burst accumulation duration in the range of several 1000 microseconds. The header of burst control is created and transferred to the receiver in a distinct channel before the transmission of the payload. The header further notifies each node of the coming burst data and adjusts the required end-to-end link. Hence, OBS only reserves the bandwidth for a short duration during the transfer of data.

The burst switching in the optical circuit for a core is shown in Fig. 1.10 [25] where Burst Header Packet (BHP) is sent via an n-channel dense wavelength division multiplexed network. The demultiplexer separates the BHP and burst packets to be fed to the processing unit.

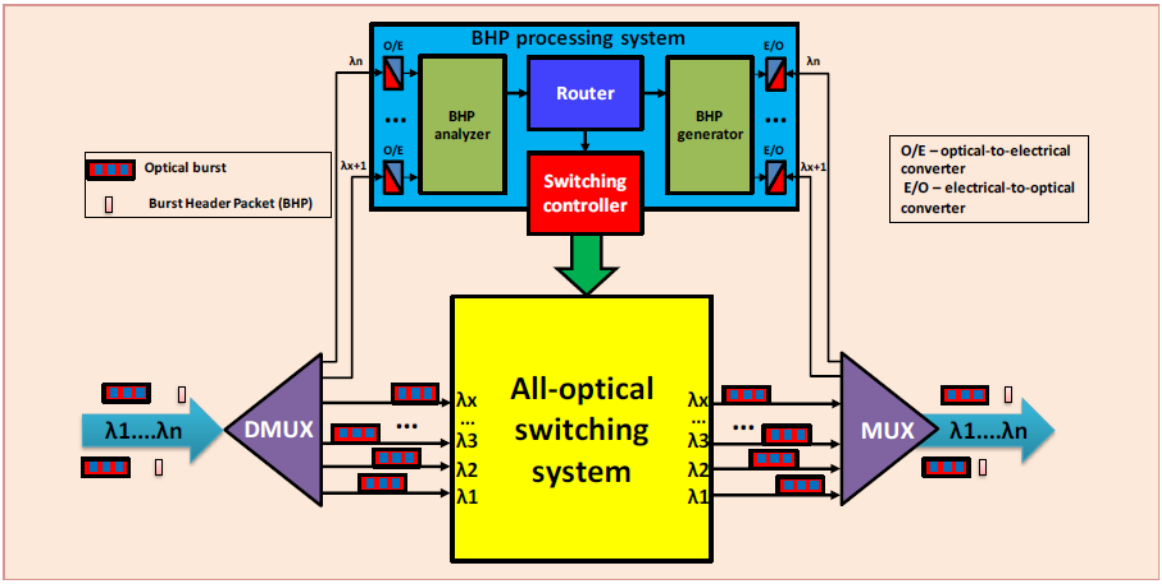


Fig. 1.10 Core node burst switching method in OBS Network [25]

This unit routes, schedules, and switches the signal in corresponding time slots. A routing algorithm allotted by the router helps in computing the complex channel w.r.t. desired quality of service and user demands within that allotted time slot. The optical switching controller reorders the information based on the router algorithm and generated BHPs are converted into their optical domain from digital to hop them to the nearer neighboring node.

1.4.2 Technologies for Photonic Switching in DC

Photonic switches can be comprehended in various ways according to the area of applications. The basic dimensional based switches can be categorized into photonic time, wavelength, and time domain switches. The types of data center switching can be realized utilizing the fabrication properties also. There can be fiber-based, crystal-based, electro, mechanical, and thermo-optic effects, as polymer and semiconductor-based switching components for commercial deployment in telecom networking. The following are the major categories of photonic switching technology:

1. *Microelectromechanical i.e. MEMS-based photonic switching*: This technology is largely implemented in fields like sensors, telecom, aeronautic, and biochemistry. MEMS are formed by tiny micro mirrors attached at an angle with moving parts organized on a particular substrate.

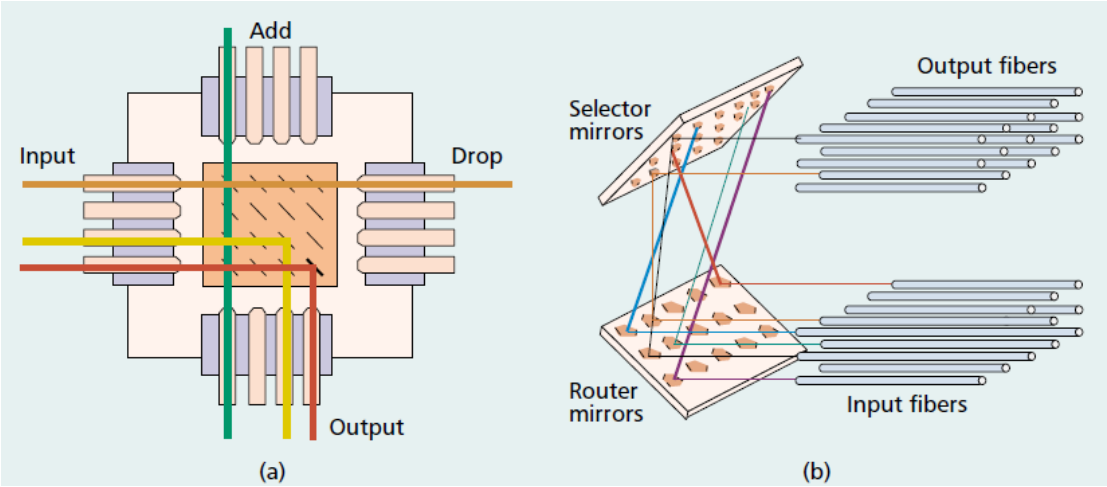


Fig. 1.11 Photonic switching structure utilizing (a) 2D digital MEMS (b) 3D analog MEMS [26]

For commercial applications, single chip integration with proper driving circuits and software is attached to the system where light from the ports on one side is steered to the ports on the other desired side. Based on the requirement of scalability, MEMS switches can be either 2D (two-

dimensional) or 3D (three-dimensional) as shown in Fig. 1.11. 2D configurations are easy to control but the scalability is limited as 16×16 2D MEMS has been commercially reported [26]. The 3D structures, on the other hand, provide freedom in size but the bulky and complex structure also requires complex software to control the operations of widely employed micro-mirrors in the system.

2. *Direct Light beam-steering technology for switching*: This is another 3D solution to scalability challenges. It is Polatis's patented switching-method shown in Fig. 1.12 which utilizes fiber collimator-based arrays straightly coupled to each other, further supervised by 2D piezoelectric actuators for angular steering of beams.

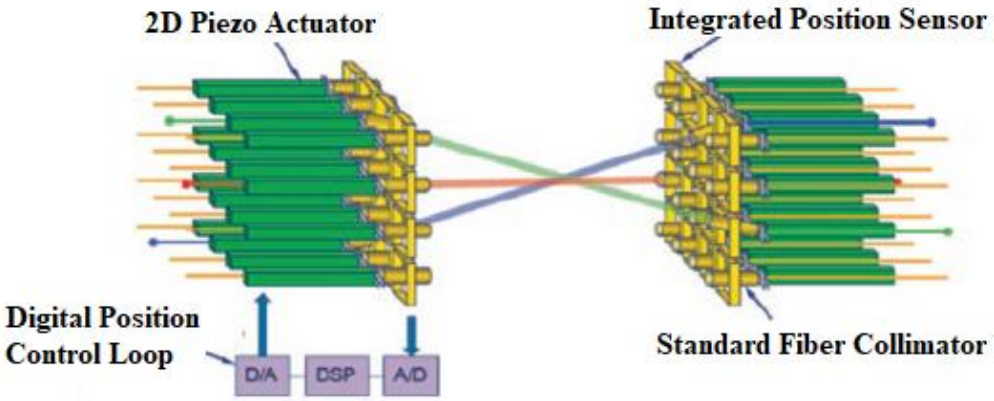


Fig. 1.12 Polatis's patented Direct Light Switch utilizing beam-steering [27]

The actuator's pointing angles are maintained by position sensors which also deliver feedback to the control loop for optimizing the destinations. The major problem of such switching techniques is their large switching time and high cross talk values.

3. *Crystal-based switching*: The crystal-based technologies include both liquid and solid-phase crystals. The solid crystals are periodic dielectric structures that allow electro-magnetic waves to propagate at particularly assigned wavelengths. In the liquid crystals, molecules of material are set at predominant mean relative alignment which is controlled by the applied voltage across the liquid crystal. This mechanism also creates a variation in the photonic properties of the material like refractive index and polarization of light which can further lead to polarization dependent loss. Such switches also face high crosstalk when subjected to larger size requirements.

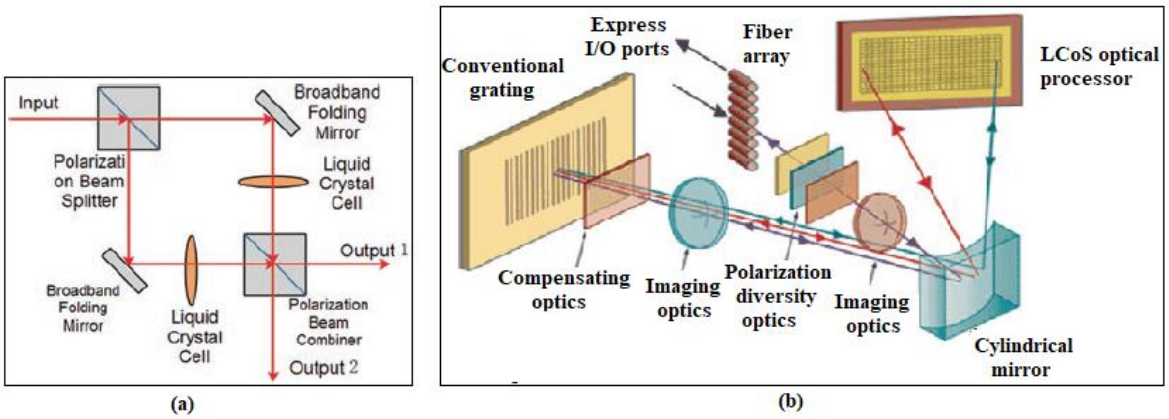


Fig. 1.13 (a) 1×2 liquid crystal optical switch (b) Liquid crystal on Silicon-based Wavelength selective switch [27]

Hence, small size crystal-based structures shown in Fig. 1.13(a) are preferred to avoid non-linear degradations. These can be formed on Silicon wafers utilizing the wavelength selective switching technologies as illustrated in Fig. 1.13(b).

4. *Thermo-optic and Electro-optic Switches*: Such switches have physical properties dependency on the thermo and electro effects employed around the material. When the refractive index of the waveguide changes with the electric field applied across materials like semiconductor optical amplifier (SOA), liquid crystals, and lithium niobite ($LiNbO_3$) shown in Fig. 1.14(a), electro-optic switching can be achieved. $LiNbO_3$ structures are preferred for their fast response times and low power consumption but the switch shows an increase in insertion loss with the increase in port scalability.

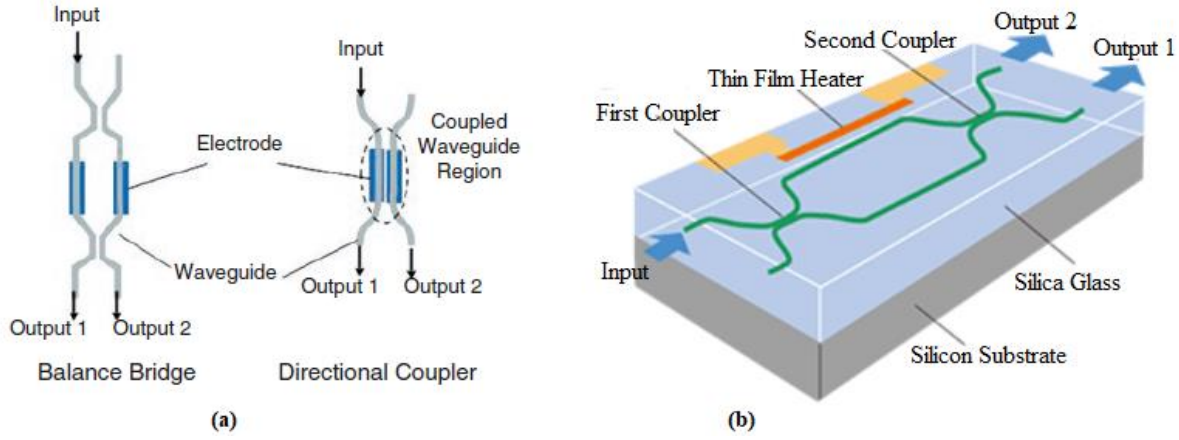


Fig. 1.14 Switches in an interferometric configuration utilizing (a) Electro-optic effect (b) Thermo-optic effect [27]

When alterations in the refractive index occur due to its temperature dependency, the switching effect so obtain is considered thermo-optic switching. Such switches are usually made on polymer or silicon wafers where waveguides are obtained with the help of chemical vapor deposition and cladding is formed by metal that further act as a heating electrode. Similar to electro-optic switches, these have interferometric configurations shown in Fig. 1.14(b).

5. *Semiconductor Optical Amplifier (SOA)-based Switches*: The studies on SOA have been gaining interest for decades and new research is proposed every time. The non-linearities of SOA like cross phase modulation (XPM), cross gain modulation (XGM) [28], and four wave mixing (FWM) [29] and its compatibility with other amplifiers [30] help gain new switching configurations.

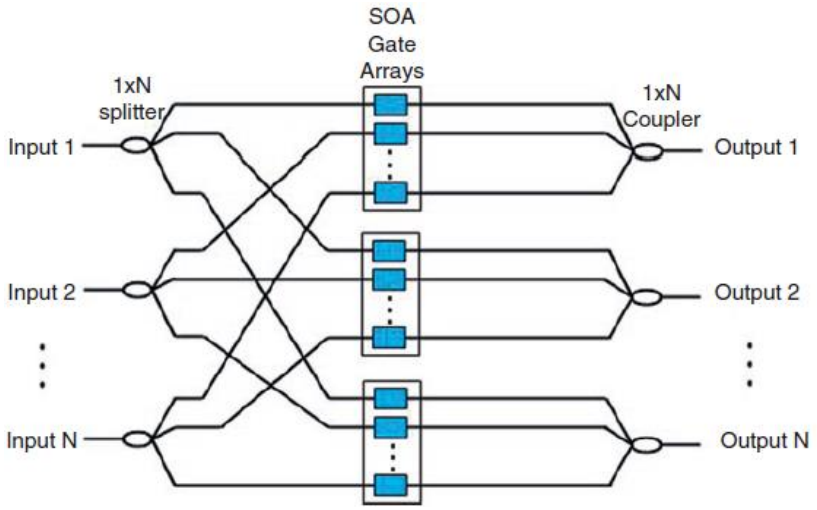


Fig. 1.15 N×N routing matrix with SOA gate arrays [26]

During its linear mode, SOA is used to amplify the signal. The SOA utilizes stimulated emission when the ray if light propagates through the active region. This area can be driven by the injected current to the positive gain regime.

In the absence of current, the signal doesn't cross through its active region, and in the presence of current, the signal passes with proper gain. Hence, usually, circuits designed with SOA are called ON-OFF gates. With attractive sizes, large routing matrices can be formed utilizing SOAs. An N×N routing matrix with SOA gate arrays has been shown in Fig. 1.15. SOA-based switching matrices are reliable, provide fast response time, less noise, and support scalability. The major concerns about designing SOA switching structures are there cost and non-linear dependency.

1.5 Conclusion

The switching technologies are designed by keeping major concerns in mind. The demands like high performance, fast response time, low power consumption, low cost, high radix compatibility, and application areas can be very challenging when it comes to designing a switch for the DC platform. The types of interconnections decide the switching configuration i.e. machine-to-machine, processor-to-processor, board-to-board, chip-to-chip, or on-chip, and their power consumption. The application area decides the further type of switch i.e. OCS, OPS, or OBS. After the type of switching interconnects is finalized, the technology for fabrication is decided based on latency, losses, radix, and cost. The MEMS-based beam-steering technologies allow large scalability but the switching speed is quite low in the range of several 10s of milliseconds. Further, the complex moving parts and driving circuits to manage the movements add more to implementation and management costs. The liquid crystals technologies give low power consumption metrics but scalability remains an issue. The electro-optic switches show small response times but the complex manufacturing limits their uses in DC applications whereas thermo-optic switches have good reliability and low manufacturing cost but the large power requirement for operating such switches stands against its preference. Lastly, SOA-based structures show low latencies in the range of nano seconds, are capable of achieving high-radix interconnections, show low insertion loss, and have low operating powers. Such attractive features of SOA make it applicable for efficient optical packet switching and wavelength selective switching circuitry for small and medium scale deployment.

1.6 Organization of Thesis

Based on the above discussion, the thesis has been organized into seven chapters.

Chapter 1 is dedicated to the keen introduction and motivation behind selecting this subject area. The proliferating demand for accommodating users in widely mounted huge data centers along with maintaining the system's quality of service has been discussed. The importance of photonic interconnects for layered embedded architectures of high-performance computations is highlighted. It also discusses various DC structure requirements and illustrates the significance of photonic switching interconnect technology. DC switching is becoming an evolutionary trend and solution to networking problems. The multiple famous leading industries and organizations are

competing to give the best possible real-time switching DC structures. Finally, it converses various photonic switching structures and their pros and cons according to intra-DC architecture.

Chapter 2 is devoted to the literature survey shown in accordance with the issues raised in chapter 1. The literature summarizes numerous throughput problems, power issues, scalability demands, and latency challenges. It further discusses gaps in the present studies reported to date. The comparison tables clarify the technologies implemented by various researchers and their constraints in the research. These remaining issues further shape the objective of the thesis. The chapter finally closes with the contribution of the thesis work.

Chapter 3 presents the proposed switching configuration for HPC applications utilizing a basic 2×2 building block. It illustrates the cross and bar state operating principle and performance is analyzed on the basis of various parameters. The major aspect of this chapter is to design a circuit that doesn't limit the increase in radix of interconnect. The 4×4 switching interconnect is achieved and its response, performance, and scalability analysis are monitored with increasing switching stages and varying injection current and input powers.

Chapter 4 further analyses the scalability of the proposed structure to increase the radix from 4×4 to 8×8. It mainly focuses on power analysis of the structure with an increase in stages of the switch. It also explains the use of the Travelling Wave (TW) configuration of SOA and presents the effect of TWSOA's injection current on the parametric performance. The switch is further evaluated on the switching time to monitor the latency with the increase in scalability.

Chapter 5 deals with two major non-linear aspects that can affect the output of the proposed configuration. It explores the non-linear crosstalk and polarization effects on the output waveform. The analytical model of non-linear crosstalk is presented and the all-port parametric evaluation has been done for both bar and cross-state operations. The evaluation is taken further by keeping a high-logic at alternating and consecutive places in the input sequence. The polarization effects are studied based on Stokes parameters and the Poincaré sphere. It also proposes an improvement in the present structure to remove birefringent effects on the output waveform by constructing the configuration utilizing hybrid compound amplification.

Chapter 6 introduces the deep learning concept in the proposed structure to smartly switch the data to the desired destination within a small response time. It first presents an introduction to the deep learning models in the optics and there working. This study is further narrowed down to choosing the (Recurrent Neural Network) RNN model called Long-Short-Term-Memory (LSTM) for the proposed configuration. It presents the proposed idea in two ways. The first way is to transmit the data to the destination port with minimum distance and low error possibility without the information of the availability of the port. In the second configuration, the network is training on the data that provides information on port-availability with small latency and low error. Thus, the implementation of deep learning improves the latency and error of reception in the proposed model.

Chapter 7 presents another smart scheme for routing the incoming traffic on the ToRs of the stack switches to direct the data according to priority. This routing technique can be applied in the control plane interface of the data center network. The structure is proposed utilizing logic-gate methodology by utilizing the priority bit information from the header of the incoming packet. This technique utilized the machine signal and priority bit as two inputs to the logic-gating-based routing configuration which proves to be reliable in terms of insertion loss, contrast ratio, and extinction ratio.

Chapter 8 in the last gives the over-all conclusion of the thesis. It presents recommendations according to the results illustrated in chapters 3 to 7. It also outlines the scope of future work.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

The rough estimate of Moore's law for scaling conventional CMOS technology [31], i.e. doubling the transistor density every two years, has helped data centers to maintain the increasing demands of subscribers while keeping low cost in the picture for a long time. But now it will not be considered an injudicious remark if it is said that the famous Moore's estimation is now ending [32-33]. In addition to extreme manufacturing challenges, it is really hard to push the lower size limit of molecules. On the other hand, the on-chip compactness has started to show its limits when an efficient energy structure is preferred. The clock frequencies have also been leveled out which puts a constraint on performance enhancement which further depends on energy efficiency. It is observed that exa-scale supercomputers that utilize the existing technology of semiconductors would consume 100MW of power. To meet this requirement, on-chip parallelism has been extensively increased. So, the end of Moore's Law can be challenged in the coming two years with two potential disruptions.

First, the need to adopt hardware-accelerated programs [34] with categorized workloads [35] to boost the removal of network latency and throughput challenges. To achieve such hard issues, there is a need for large bandwidth which will inflate costs. Second, the incapability of scaling pin density of switches, and current electrical switching configurations are expected to hit the wall in the next two generations [36]. Various new fields have explored solutions to these challenges by presenting models based on monolithic integration [37] and Silicon Photonics [38] that are ultimately becoming acceptable. But the forthcoming issues of fiber coupling, compact packaging of LASER optical source, and high manufacturing and maintenance cost has put a questionable impact on the use of above said technology in data center applications. Photonic switching presents various promising superiority in terms of power consumption, throughput, capacity, and flexibility with existing approaches. It seems to be the best solution to overcome the above-said challenges.

The optoelectronic (OE) and electro-optic (EO) conversions are not required which helps in decreasing the high cost of transceivers. In addition to this, high throughput can be supported by photonic switching because of its attractive feature of transparency to modulation formats and it

also helps in achieving low latency by offering packet inspection overhead. In conclusion, no electronics are utilized for photonic switching, thus introducing a promising enduring solution. Based on the above-said issues, the comprehensive review with present gaps in the study has been presented in the following sections.

2.2 Throughput Problems in Data Center (DC) Switching

As mentioned above, the key requirement of adapting photonic switching in DC architectures rises from introducing scalable, high throughput, and power-efficient structures to maintain the load-balancing problem. Several types of research [39-41] have been reported which promote throughput benefits to data centers for a photonic switch deployment. The first structures promoted for DC architectures were based on circuit switching.

Li *et al.* [42] showed how RotorNet netwroks are insensitive to the dynamic draffic as the switching components roatte independently with the help of a fixed optical link setup. Hence, their new architecture, called FlexNet, provides a centralized control system for traffic prediction and a topology algorithm can help in altering the topology according to the requirement. This structure showed 75% of throughput with Morida and 100% with RotorNet systems due to the innovative feature of traffic prediction and changing topology with it.

T. Kuno *et al.* [43] worked on a circuit switching network that gave high throughput for intra-datacenter applications. The structure used the combination of delivery-coupling space switches and wavelength routing switches which confirmed the feasibility of Nyquist Wavelength Division Multiplexing (WDM) and also improved the spectral efficiency.

M. Xu *et al.* [44] implemented a solution to power-hungry challenges in DC networks and high throughput outcome was ensured. The routing didn’t compromise the network performance and utilized a little power to route the data by shutting down the system or putting it in sleep mode. Hence less power was utilized. This power-aware configuration reduced power consumption for the system with less load.

H. H. Bazzaz *et al.* [45] suggested that a perfect DC interconnecting structure should be able to tolerate unusual flows occurring in the circuit to support the needs and alterations according to application. It should also be able to support the codependent and correlated flows to support

flexible routing. Keeping in view such demands of interconnects, a hybrid structure was proposed that collects statistics about the current traffic and also ensured the correct status of the network from various available sources, and finally finished with the data investigation per application semantics to configure the user-defined purposes.

A. Shpiner *et al.* [46] presented a switching-based approach to be implemented in DC networks which negligible overhead. It showed Hashed Credits Fair (HCF) algorithm with provides transparency features to end users. It illustrated that the throughput failure of minor flows is mitigated by the HCF algorithm by removing the hunger of both short and long-life TCP in a congested connection and it also avoided re-ordering of packets.

An OCS configuration was proposed by L. Schares *et al.* [47] combined with abilities to handle the transceiver's burst mode to support needed graph algorithms. The simulation mapping policy estimated accomplished great throughput for normal traffic and worst throughput when traffic is permutated with an excessive increase in frequency. This helped in minimum power consumption and hence improvement in efficiency is attained. But if the mapping was done randomly, opposite results were achieved.

Z. Huo *et al.* [48] gave a method for allocating resources across various storage servers in such a way that it provided a unified throughput for users and takes full advantage of the throughput exploitation in the DC system. This method was called Unified allocation framework i.e. UAF which fully exploitated properties like sharing incentive, envy freedom, and Pareto optimality.

A meta-model was presented in 2013 [49] which helped in predicting throughput for data center networks. The Descartes Network Infrastructure i.e. DNI Meta descriptive model could be transformed into a predictive model that defined practical situations by monitoring the traffic. The accurate prediction error of 32% on average for the worst-case scenario was reported with only two false positives. But the work on the time factor for completing the requirement of modern DC networks remained a gap.

T. kuno *et al.* in 2020 [50] proposed a cross connect technique that attained high throughput with a large port count that ensembles software defined networking (SDN) networks. To minimize the insertion loss effects, they utilized wavelength selective and delivery-and-coupling space switches.

The simulated outcomes illustrated the penalty of 3% in efficiency of fiber-utilization even with the infrequent interconnection links that also effected the routing. But the experimental results gave a throughput of 2.15 Pbps over a 700 Km distance.

M. N. Rahman *et al.* [51] mentioned optical interconnects to be the best solution for DC load-balancing problems for high throughput and low latency. The fiber links inflate the initial cost of the installation of DC architecture. To achieve high-performance computation, the power consumption was reduced with the help of coolant.

Conversely, B. G. Lee *et al.* [52] provided some switching fabrics that can help in sorting such problems. They presented a Mach Zehnder Interferometer (MZI) based switching mechanism at the chip and package level. The switch contained optical interference which was actuated utilizing phase controllers or shifters. These alter the phase delay of the active waveguide. Such controllers can be installed at either the front or back end of the line. The incident signal was 90^{o} shifted by the coupler bent cantilever waveguide that can be either vertical or lateral. This switching fabric could be utilized for low power consumption and high throughput devices but has not been implemented in DC networks.

Another MZI-based switching was proposed by C. Porzi *et al.* [53] that gave its compatibility with the high-capacity all-optic applications. They showed the Semiconductor Optical Amplifier (SOA) when utilized in MZI configuration gave the compact and flexible answer to the DC switching requirements. Transparency and reduced power penalties can be achieved by combining different coding techniques with the transmitted signals.

Following Table 2.1 shows some of the limitations encountered in the previously reported literature along with the parametric studies.

Table 2.1: Issues encountered in the literature regarding throughput problems in DCs

Ref. (Year)	**Technology/Configuration**	**Parameters Studied**	**Issues encountered**
[44] (2013)	BCube and Fat-Tree topologies	Power saving percentage, Completion time	Delay sensitive, power-aware virtual placement

[47] (2014)	Photonically Optimized Embedded Microprocessors (POEM) based throughput optimization system	Power consumption, Throughput, Delay	One-to-many, many-to-one pattern, opto-electronic control
[48] (2015)	Unified allocation framework	Throughput, Power utilization	Dynamic unequal traffic control probelm
[49] (2013)	Modelling topology, links, and routing protocol utilizing Descartes Network Infrastructure	Layer-wise throughput, traffic prediction percentage error	Compatibility with existing architecture, improved traffic prediction accuracy
[51] (2015)	Big data handling with cloud computing using OPNET	Ethernet delay, Throughput	Opto-electronic domain

2.3 Power Issues in High-Performance Switching Structures

If large throughput is expected from the highly scalable DC structures then, the expense of power and required cooling components also become vital factors for decreasing the expenditures when it comes to large-scale DC installation. It has become a zest to bring architecture into the picture that doesn't need large coolants and consumes less power. Such needs are only possible in reality if the low-power operation components are created that operate in a single domain and don't need any extra power for OEO conversions.

Q. Cheng *et al.* [54] illustrated a monolithically integrated system to create a 2×2 switching circuitry at 10 Gbps with the help of MZI modulators in place of small radix switches i.e. 1×2. This was done to achieve a higher gain and large extinction ratio of 40 dB. It demonstrated a switching time of 3 ns and a low power penalty of 0.1 dB. It also showed how the radix of such switching elements can be increased with input power rise and in comparison, to broadcast-and select switching structures, the low energy consumption of around 55% can be achieved.

Wang *et al.* [55] showed another monolithic structure utilizing the quantum well properties of SOA at 10 Gbps to gain an error-free performance. The switch showed a 2.5 dB of power penalty and had SOA saturation at the output of -7 dBm showing that the structure may reduce the

requirement of power up to 300 mW/path. But the results were only demonstrated for the negative powers. The positive power operation w.r.t. energy consumption has not been mentioned.

Chen *et al.* [56] did the work on polarization effects on silicon-based structures and presented an 8×8 broadband switch. They accomplished a wide spectral range greater than 45 dB by minimizing the port-port insertion loss near various spectral regions. A power consumption of less than 70 mW was achieved. It also mentioned the issue of the temperature dependence of the system can lead to an increase in insertion losses (IL) and polarization dependency has to be minimized by monitoring the birefringence. The second issue in the structure was to work on the improvement of IL reduction in the crossover network by employing a focus on the cross-state operation of the switching structures.

Abts *et al.* [57] showed a comparison of butterfly and folded-Clos topology for data center networks for high-performance networks. By utilizing the production traces of data centers and synthetic workloads, the authors showed an 85% decrease in power. They showed a switching capability of adaptive routing for energy conservational properties of large-scale applications.

A green computing solution was given in [58] that proposed an allocation procedure and reflected the collaboration between DC hardware and power elements for the energy efficiency of the system. The resource allocation policies and energy management of clouds were proposed and validated by CloudSim Kit. One more study in [59] showed a power consumption comparison of various interconnect technologies utilizing SOA, Arrayed-Waveguide Grating (AWG), and Wavelength Selective Switches (WSS). It illustrated the dependency of cost on the age of the type of optical component.

Huang *et al.* [60] suggested installation of built-in power monitors can consume more energy and bandwidth hungry components can degrade the system performance. Hence, installing optical switching fabrics with no such requirement can lead to low cost, less complex, and compact packaging. The scalable methodology for determining the bias state of the photonic switch in either the single-arm or push-pull stage was implemented with low complexity and reduced cost.

Dayarathna *et al.* [61] surveyed various techniques for the prediction of energy consumed by the DC components and categorized these into two states: hardware and software. The hardware

consumption at either component of the server or center level has always contributed to higher scales and software-based issues are more dominant in predictions of such DC consumptions and CPU metrics and modelling for such needed solutions.

Hirono *et. al.* [62] worked on a High-Speed optical layer (HSOL) in DC structures and mainly focused on the nano seconds switching time of the optical switch. The idea of proposing the energy-efficient structure was offered by collaborating the Micro Electro Mechanical Systems (MEMS) switching components with HSOL where 50% of power saving was observed when compared with conventional schemes.

The 8-port broadcast and select (BAS) switch was reported in [63] that utilized a trigger pulse generator in order to have low energy consumption. It showed that the consumption also occurs for a small duration when the pulse generator is interfaced with the CMOS processor. The estimated power consumption is predicted around 27.3 W i.e. 3.4 W per 100 Gbps port.

Chong *et al.* [64] suggested four key methods that were able to reduce power consumption in data centers. The first suggestion was to design the DC architectures in accordance with the requirement of the application. Secondly, designing machines that can correlate the load consumption from the data provided by the future workload prediction generator. Thirdly, improving software interfaces to show more real-time storage and runtime. Fourth, making auto-upgradation in software and improving the comparability of hardware and software so that it could allow fast integration of upcoming technologies and also doesn't stop the way to already existing operations.

Kaler *et al.* [65] illustrated a dispersion study where the power penalty for the system was calculated for the large signal analysis. The impact of line width and order of dispersion on BER was investigated. It also illustrated the significance of EDFA utilization in the system for compensating the loss in fiber periodically and hence the requirement of repeaters.

Popoola *et al.* [66] presented an analysis of the efficiency and performance of DC structures w.r.t. bandwidth usage and throughput. The basic DC configurations i.e. three-tier and fat-tree were analyzed based on the energy consumption utilizing the GreenCloud simulator. They suggested that the complete fat tree consumption was way more than three-tier. The fat-tree somewhere spent less amount of energy for sending a bit and hence better than the three-tier.

The analytical model in [67] examined various properties of hybrid systems to integrate a non-linear medium that captured ultra-low light and hence low-power operating medium. The demonstrated structure utilized photonic crystal micro-cavity for small compatible size and fast response.

Following Table 2.2 illustrates some of the power issues encountered in the previously reported literature along with the parametric studied in HPC systems.

Table 2.2: Power Issues reported in the literature for HPC systems

Author (Year)	**Technology/Configuration**	**Parameters Studied**	**Issues encountered**
[55] (2009)	Monolithic integration utilizing SOA	Power penalty, switching time, Bit error rate	High values of power penalty
[68] (2010)	Silicon waveguide resonators	Insertion Loss, Power vs Injection current	Electro-optic
[56] (2012)	Switch-selector architecture on silicon	Insertion loss, crosstalk, and switching time	Large insertion loss variations
[57] (2010)	Flattened butterfly topology	Output Power, Latency	High power consumption at data rate > 2.5 Gbps
[54] (2014)	Monolithically integration with MZI-SOA	Crosstalk, power penalty, Latency	High Latency

2.4 Scalability Requirement with Load-Balancing

The bursty traffic has motivated the inclusion of load-balancing architectures. The basic requirement of OPS and OCS switching is adopting buffer-less circuitry to avoid the delay created by the queue. It also reduces the end-to-end latency. The centralized scheduler proposal was good for fast computing but the centralized control system reduces the increasing port count possibility. Hence, the various solutions to scalability issues were proposed by many researchers reported below.

The Birkhoff-von Neumann proposed in [69] handled both unicast and multi cast traffic to reduce the average load delay. The one-stage buffering and second stage switching handled on-line complexity and were also capable of achieving 100% throughput.

The same topology structure utilizing Birkhoff-von Neumann was shown in [70] and provided resequencing of output. The structure also required the jitter control mechanism. It utilized the technique of scheduling the packets according to the deadlines of departure time. The structure didn't use segmentation and reassembly for the same packet size assumption.

A scalable switch was reported in [71] based on arrayed waveguide grating (AWG) that helped reduce the complexity of arbitration and delay. This corresponded to low latency and high throughput with bursty traffic which was far good as compared to a flattened butterfly topology-based electrical switch.

Huang *et al.* [72] implemented a single stage switching configuration based on AWG in combination with tunable lasers. The power penalty of 0.7 dB was achieved when the system is put into load balancing mode. The system was operated in two modes: switching mode and balancing mode. The high port count wavelength cross-connect could be achieved by replacing the AWG router.

Xiao *et al.* [73] utilized a distributed arrangement of photonic switching components and the arrangement of server racks is also altered at various nodes. By replacing various power components and applying cooling constraints, the authors showed that a higher scalable structure can be made. It also showed how distributed components reduce the transmission cost of DC external traffic. The inter traffic could be maintained by an integer linear program.

Duan *et al.* [74] reported a switch with the virtual framework by supporting the arbitrary traffic in virtual machines on a private cloud. The bare data were accommodated from the dynamic network environment and then adaptively applied an oversubscription which is bounded globally. The architecture preferred for such a load-balancing technique was fat-tree DC.

Rastegarfar *et al.* [75] inspected packet loss reasons in a scalable router for cloud DC by exploring the fiber delay lines when the incoming traffic was non-uniform and in large numbers. The

structure at the load-balancing stage evenly distributed the uneven traffic in time and space regions and switched to the desired location by utilizing distributed buffer architecture.

Guo *et al.* [76] demonstrated a photonic wavelength link that joined the server racks using physical wiring. This research investigated scalable structures for the load-balancing problem. The functionalities were tested for both data and SDN control plane interfaces.

SDN based networking has been attractive research when the evaluation of parameters like real-time performance, scheduling, routing, monitoring the latency, and space management is required. The study in [77] showed another SDN-based scalable and robust load-balancing topology to be applied in DC networking that employed pre-awareness of congestion by adopting a distributed control mechanism to control the congestion for making it more robust to asymmetries occurring in the topological structures.

A datacenter technology reported in [78] for RotorNet optical switches helped in decoupling the structure when large traffic was encountered. This method showed the demand for a decentralized control plane in order to have the large port count nearly a thousand. The centralized technology can decrease the demand for circuit assignment and synchronization of data but the scalability can only be solved by a control plane that does not need to monitor large port count.

Yan *et al.* [79] showed another structure for data centers utilizing flow control technology for fast optical switching and also modified ToR intra-cluster for an efficient clustering operation. The lack of optical buffering in practical applications could lead to unnecessary retransmission of packets. Hence, the investigation was focused on including ToR buffering

Zheng *et al.* [80] showed a converter to achieve more flexibility in the dynamic load balancing problem. The hybrid switching structures in DCs required optimized links to reduce the maximum link exploitation of the network. They suggested an optimization algorithm to reduce traffic congestion by up to 12% on average. The reported greedy algorithm formulated load balancing issues on the basis of ρ-approximation.

There exists another study in [81] that proposed high efficiency migration of dynamic switches to have a load balancing at the SDN controller. The load at controllers was first measured and routed

to the optimal controller that had a large resource remaining. This also minimized the cost and parallel control of all the migration switching providing highly efficient behavior.

The load balancing problem is solved by increasing the port count of optical cross connects that are utilized in the DC switching stages. The wavelength assisted switching technique was reported in [82] to observe the influence of the reconfiguration time of the switch to improve the throughput performance of the network.

Wang *et al.* [83] showed an integrated silicon photonics platform for hyper-scale DC networking as a solution to future scalability and load-balancing problem. The structures presented a two-way approach of predicting split transaction and then switching was done based on wavelength group so formed from the predictive analysis.

Following Table 2.3 illustrates some of the issues encountered in the previously reported literature along with the parametric studies enlightening the scalability requirement.

Table 2.3: Issues reported literature enlightening the scalability requirement in DCs

Author (Year)	**Technology/Configuration**	**Parameters Studied**	**Issues encountered**
[72] (2012)	AWGR-based switching	BER, Output power	To achieve high scalability, AWGR was to be replaced with large port cross-connects
[75] (2013)	AWG-based routing utilizing optical buffering	Latency	Tested at bar-layer only, High penalties
[76] (2017)	Wavelength multiplexer-based routing utilizing open flow controller	Throughput and stage-wise scalability	The latency parameter wasn't explored
[71] (2010)	Data center switch fabric based on Arrayed Waveguide Grating Router (AWGR)	Throughput, latency	Structures greater than 2×2 scalability were yet to be explored

[84] (2004)	Broadcast and select configuration utilizing wavelength space division multiplexing	BER, output Power, Quality factor	Complex control interface

2.5 Latency Challenges with High Port Switching Interconnects

Latency is an important and non-ignorable issue in the huge data centers that mounts tens of thousands of servers. The lower latencies can help in simplifying web scalability, and application developments, and open passage to the invention of new data-intensive applications. The latency has been ignored by system designers but at the application development platform, which deals with the customers and day-to-day internet users, this issue needs to be solved.

Many types of research have been reported that prefer the idea of high-performance computation but hardware achievability has still remined an issue. Hence, the architectures designed on the polling technology should be abandoned which waste the time by remining on the CPU and waiting for packets to arrive [85]. Instead, a new monitoring and predicting technology should be parallelized that an optimize the idle time of the CPU.

Schrejeck *et al.* [86] presented a switching approach to achieve fast response time utilizing the refractive index non-linearities of structure that were made from MZI. The reduced on-off ratios were observed when the switching window of sub-pico-second was exploited. They suggested the employment of SOA non-linearities in MZI configurations for 150 femtosecond pulses.

A 4×4 low latent structure was reported in [87] that exploited the features of AWG router and the loop-back buffering technology with no acknowledgement. The structure removed the complexity by maintaining the load balancing issue and provided fast switching time and also outperformed the flattened butterfly architecture. But the scalability remained an issue.

Calabretta *et al.* [88] showed a packet switching technique exploiting the statistical muxing in the virtual DC networks with a power penalty of 1 dB and latency of 500 ns. A controller was installed as a mainframe in interfacing with an FPGA control unit of OPS. The SDN approach was then provisioned for centralized control of ToR switching units and data belonging to virtual networks distributed in the DC is then multiplexed offering a low latency environment.

Alistarh *et al.* [89] proposed an approach that parallelly handled the radix and latency demands of optical switching in DC. The broadcast and selective (BAS) configuration was selected for switching purposes and passive star couplers helped tune the transceivers whereas time division muxing was employed for low latency.

Saljoghei *et al.* [90] worked on disaggregated DC protocols by embedding OCS in interconnecting architectures with transceivers integrated with silicon photonics for high capacity and low latency. The utilization of multi-core fiber in the sub-system brought down the power consumption to a level where the energy efficiency of the structure was claimed to be above 60%.

Bahadoran *et al.* [91] offered silicon on insulators i.e. SOI-based ring resonator approach for switching action in order to remove the requirement of optical pumping. This helped in achieving the closed loop bi-stable switching and low I/O power. The latency of 1.96 ps was observed for resonant mode numbers.

Yan *et al.* [92] provided a cost reduction scheme by avoiding the use of expensive transceivers in multi-stage electronic DC networks. The shown comparison in the paper proved that LIGHTNESS used in combination with electronic DC could achieve the short time transmission of packets and hence helped in achieving low latency.

A large number of connections in DC networks utilizing EPS or OCS can demand all-to-all communicating links in order to efficiency utilize the capacity and can lead to high latency. On the other hand, for OBS systems, Soni *et al.* [93] suggested that the slit between payload and BHP was increased at the entrance node due to the large queuing of traffic. This was suggested to be solved by manually setting dynamic values to the offset occurring during BHP transfer.

Terzenidis *et al.* [94] showed that AWG and BAS-based switching structures were helpful in increasing the port count of the interconnect and bringing high throughput by maintaining low latency. The feasibility of 256 ports was announced utilizing the proposed architecture at 10 Gbps with a 2.19 dB power penalty and latency of 610 ns if the incoming loads were uniform in nature with feed-forwarding buffering.

Jadon *et. al.* [95] presented the importance of multicore processors for handling load balancing problems with fast response time. The load balancing technique utilizing heuristics worked by

selecting the finest task out of all incoming tasks to fully exploit the capability of the system. The work was assigned by the priority made by the check window to decrease the effects on output due to the undesired migration of tasks. This also helped in reducing the latency and achieving faster response time.

Muranaka *et al.* [96] showed application based compatible structures to have efficient utilization of the resources. The wavelength routing-based switching was effective for higher radix networks. The BAS-based switching was preferred for systems that require low power dissipation and provided low insertion loss and compact sizes could be formed even with increased scalability.

Soliton-based structures also support heavy workloads handled dynamically. Raja *et al.* [97] proposed SOA and microcomb-based optical circuit switching utilizing a well-matched modulation scheme i.e. pulse amplitude modulation in burst-mode. The photonic integrated circuit (PIC) was embedded in Indium phosphide and the AWG array was used for creating nano seconds switching window.

The AWG based router reported in [98] was additionaly employed in switching architecture utilizing distributed control based on Field Programmable Gate Array (FPGA) to improve the scalability while maintaining the switching time. The work was performed at 10 Gbps reporting a power penalty of less than 2.5 dB. It also explained the use of Broadcast and select switches for wavelength routing as it allowed the latency of sub-microseconds.

Liu *et al.* [99] presented a multi-socket coherent network with shared memory-based ToR switching units to reduce the power consumption in the control plane. The method showed an idea of a forget-server interface utilizing the basic SOA-MZI based packet switching technique. The reduction in latency at lower incoming loads showed a 60% reduction in power dissipation as compared to conventional arrangements.

Following Table 2.4 illustrates some of the issues encountered in the previously reported literature along with the parametric study to remove latency challenges in HPC systems.

Table 2.4: Problems reported in the literature showing latency challenges in HPC systems

Author (Year)	**Technology/Configuration**	**Parameters Studied**	**Issues encountered**
[87] (2013)	Negative acknowledgment AWG router	Latency, Throughput	Electro-optic interface requiring FPGA
[88] (2014)	Optical packet switching with the label extraction process	Latency and scalability	Increased latency of 500 ns and large value of power penalty
[97] (2021)	On-chip SOA and AWG with soliton microcomb	Latency, error rate	High BER of 10^{-3}-10^{-6}
[100] (2016)	Broadcast and select switching utilizing electro-absorption modulation	Latency, insertion loss	Requirement of signal regeneration before the wavelength conversion.
[101] (2017)	Electro-absorption modulator gating array-based switching utilizing cascaded MZI configuration	Switching speed, loss, and extinction ratio	A cross-state operation couldn't be realized.

2.6 Non-Linear Challenges with High Port Switching Interconnects

The major challenge of designing the photonic switching is the requirement of robust and fast nonlinearity present in the material. It helps explore the low power operations of switching circuits. Such nonlinearities can be found in the transparent regime of semiconductors. To meet the requirements of current DC switching components, these nonlinearities should meet the energy levels of presently installed CMOS silicon transistors. Due to this reason ultra-low power operations and interactions of the nonlinear device become a critical issue [102]. Many studies listed below demonstrated different ways of constructing switching effects utilizing materials enabling nonlinear integration like microring resonators (MRR), graphene, antimonene, and SOA.

Van *et al.* [103] showed an all-photonic switching outcome utilizing microring made of GaAs–AlGaAs with the pump-probe technique. The process of variations in the refractive index of microring induced by photon absorption was used for creating a switching effect in the probe

signal. The in-out movement of the probe signal from the resonance was considered for switching the beam.

Cheng *et al.* [104] illustrated another microring-based switch-select technique utilizing thirty-two thermally-actuated MRRs i.e. Micro-Ring Resonator. The scalability of the switch was offered based on parameters like crosstalk and loss in the bypass rings present in the linear arrays. It suggested that the MRR's high crosstalk immunity of 50 dB could be achieved by dropping the crosstalk ratio in the orders of squares of the MRR component.

The graphene-based structures reported by Shan *et al.* [105] were fully synthesized for a nonlinear photonic response. The self-induced modulation and cross-phase modulation in such materials were utilized for achieving the switching effect. When the intensity of the input laser was varied to modulate the signal propagating, the changes in refractive index caused ON-OFF operation. However, the weaker modulation depth and zero band gap of graphene material limit the fabrication of light emitting [106] and logic devices [107].

The antimonene material described by Song *et al.* [108] showed an outstanding nonlinearity with long-term firmness. The device showed an extinction ratio of 12 dB and Kerr-effect showed absolute wavelength conversion of the high frequency signals of 18 GHz with high speeds.

Mizuno *et al.* [109] presented an MZI based switching structure that utilized a phase generating coupler to produce a nonlinear phase that was dependent on wavelength. This phase was acting as a virtual delay line that was not required to be manually updated. This finite value of the delay line was wavelength dependent which gave the high extinction ratio.

Mata *et al.* [110] presented a helpful suvery that declared the importance of artificial intelligence (AI) to remove noise in optical transmission systems. It addressed the significant role of AI technique for the employment of EDFA in the structure while mitigating the nonlinearities.

The SOA-based structures have gained continuous interest due to their compatibility with monolithic integration, performing signal processing with functional properties like wavelength conversion, phase [196], and intensity modulation, filtering, clock recover, pulse generation, dispersion compensation [199], and gating operation [28]. The processes of SOA that provide it extreme research interest are the optical gain with ripple [194], polarization sensitivity, and

saturation power that are able to disturb the output. This brings to discussion the fabrication of various types of switches employing SOA in the structure.

Runser *et al.* [111] reported the SOA in interferometric configuration for the purpose of achieving ultrafast optical switching operation with sampling bandwidths of nearly 1 THz. A similar structure utilizing SOA-MZI could achieve the gating operations as reported in [112].

Wang *et al.* [113] showed how SOA-MZI combinations were best for designing the D, SR, T, and JK flip-flops with all-optic operations using SOA's nonlinear polarization rotation effect. The polarization dependent rate-equations helped in forming the theoretical SOA model.

Jyoti *et al.* [114] showed the significance of encoding the user data before the transmission of the signal. The impact of intensity modulation using the OOK pattern on the encoded sequence was observed on the BER. It illustrated the increase in BER with the increase in the number of users.

Tian *et al.* [115] discussed the utilization of a genetic algorithm for attaining convergence and high computing efficiency in the two-pump switch. The switch employed nonlinear four wave mixing. The switch achieved high efficiency only for the single channel but the same had to be compromised for a multi-channel circuit.

Mehra *et al.* [116] utilized the cross-phase modulation property of SOA-MZI configuration for creating a 10 Gbps switching operation. The structure utilized two input couplers and one output coupler that were interconnected to each other by employing interferometric arms. Both MZI arms had SOA embedded with an injection current of 300 mA.

Singh *et al.* [117] proved reversible gating operations were possible with SOA structures with improved cost. The MZI was utilized to estimate the phase shift that was introduced between the arms. The blocking filters were used to remove the destructive interference wave at the output port.

Following Table 2.5 illustrates some of the issues enlightened in the previously reported literature along with the parametric studies in high port switching interconnected systems.

Table 2.5: Non-linearity challenges reported in the literature for high port switching interconnects

Author (Year)	**Technology/ Configuration**	**Parameters Studied**	**Issues encountered**
[103] (2002)	GaAs–AlGaAs microring with pump-probe technique	Input and Output signal intensity with time	The switching speed was limited by the carrier life time, improvement could be done by DC biasing. High pump energy was required.
[108] (2018)	Switching-based on antimonene material's Kerr nonlinearity	Extinction ratio and conversion efficiency	Opto-electronic operation only.
[111] (2001)	SOA-MZI configuration	Bit-error-rate	Limitations on the minimum temporal width of the switching window due to the asymmetric nature of THz optical DEMUX (TOAD) sampling window.
[115] (2007)	FWM non-linearity of SOA	Extinction Ratio	Achieves high efficiency only for single channels but the same was to be compromised for multi-channel.
[116] (2014)	SOA-MZI cross phase modulation	Contrast ratio, output power	Abrupt fall in contrast ratio when input power changed from 0 to 3 dBm.

2.7 SOA-MZI Switching: Advantages and Issues Encountered

The above literature also provides the solutions to given challenges. The idea of utilizing the inbuilt properties of non-linear elements for wavelength conversion has given a light of hope for solving the issues. SOA-based devices are reported to have great potential for integration at a monolithic level [29] which further offers high reliability, low cost, and a platform of compactness. The in-built properties like cross-gain modulation provide the inevitable operating speed with less complexity. SOA gates also deliver the sufficient amount of gain required for lossless switching operation [55]. The study in [53] showed the structures built with SOA components gave a high quality of service and lead to ultra-fast signal processing. The gain saturation region in SOA is

boosted by stimulated emission and hence low energy of the control signal is sufficient for switching operation [111]. It helps in achieving low power operation in SOA-based switches.

The structures utilizing SOA and MZI are capable of monitoring the above listed parameters and are promising configurations to handle the above challenges. The SOA component utilized in the Mach Zehnder configuration provides attractive advantages [200]. It is considered to be the best candidate for processing signals for high-capacity photonic networks [53]. These structures provide unlimited usage of fiber length as an amplifier is being employed inside the loop of interferometric arms [113] and faster state-transition can also be obtained from it. The hybrid SOA-MZI structure can reduce the absorption of power at the transmitter and hence transmitting almost all the power to the receiver.

Following Table 2.6 illustrates the comparison of various techniques followed for studying the structures with and without SOA implementation with significant parameters and issues.

Table 2.6: Literature comparison with and without SOA implementation with the significant parameters and issues

***Without* SOA**						
Author (Year)	**Technique utilized**	**Parameters Studied**	**Software utilized**	**Polarization Sensitivity**	**Non-Linearity**	**Other Issues**
[118] (2012)	Waveguide Arrangement	Gain, Power intensity	MATLAB	Yes	Two photon absorption	Guide length control
[119] (2014)	Circular Resonator Arrangement	Input and Output Power	OptiFDTD	Yes	Non-linear circular resonator	-
[120] (2012)	Add/Drop Filter with Soliton	Crossbar Output power	-	-	Delayed coupled waveguide	Incompatible with large input
[121] (2005)	Multilayer Waveguide	Electric field distribution, power density	-	Yes	Multilayer non-linear media	AND-OR operation only

[122] (2015)	Acoustic filtering in multicore fiber	Normalized power, acoustic frequencies	Comsol Multi-physics	Yes	Mode coupling	-
***With* SOA**						
Author (Year)	**Technique utilized**	**Parameters Studied**	**Software utilized**	**Polarization Sensitivity**	**Non-Linearity**	**Other Issues**
[123] (2010)	Ultra-non-linear copropagating	Output power, Extinction Ratio	OptiBPM	Yes	FWM of SOA	Conversion efficiency
[124] (2009)	Ultra-non-linear counter propagating	BER	PSpice	Yes	XGM of SOA	High power penalty
[125] (2013)	Sagnac Interferometer	Gain, output power	-	No	SOA	Unequal splitting of power
[126] (2005)	Michelson Interferometer	Output power, EOF	-	No	SOA	Low extinction ratio
[127] (2015)	MZI symmetric arrangement	Output power	Optisystem	No	XPM & XGM of SOA	Non-linear crosstalk
[128] (2010)	MZI asymmetric arrangement	Crossbar gain, ER	Mathcad-7	No	SOA	Fan-out & loop restriction
[117] (2016)	Delayed Interferometer	Power spectrum	VPI Photonics	No	XPM of SOA	Distorted outputs with delay

There are still many areas left untouched in SOA-MZI configuration as stated in [54] to bring low-latent properties in the optical switching networks. The use of MZI can overcome the splitting and coupling loss in the network but they also suffer poor crosstalk and low extinction values.

2.8 Gaps in Present Study

The effortless accessibility of home-to-home internet services and the pervasive usage of multimedia has increased internet traffic and the demand for real-time service quality is highly in need. This further unlocks the zest of existing data centers to create either topologies or device configurations that complete the insufficient demands of today's users.

Future switching structures should be able to have lower switching times to enable the real-time access possible. Such structures should also be able to accommodate a large number of users or structures should be at least guaranteed scalable such that it upgrades whenever needed. The compatibility with existing structures [49] in terms of power consumption and throughput is also a need for future DC switches. Networking organizations and optic researchers have been addressing and focusing on switching in the photonic domain for many years. Their perspective has addressed the various challenges at the system level and these are:

- The devices should have one-to-many and many-to-one [47] switching options in the fully optical domain to remove the requirement of opto-electronic-optic conversions. Such electro-optic [47, 51, 68, 87, 108] control interfaces require costly components which further limit the scalable capacity of the network.
- Communication technology has a large number of power-hungry components implanted in data centers. The major concern operating costs and their emissions. The two major requirements can be listed while dealing with a large of dynamic traffic [48]. This either requires prediction of incoming dynamic traffic within seconds before routing the traffic or power efficient structures [44, 115] to handle the high-power consumption. This also dedicates the researchers to work on parameters like power penalty [75] and power consumption.
- The basic control interface that handles the routing of traffic data has the major disadvantage of complexity [84]. The control interfaces utilizing the SDN technologies

[50, 76-77, 81, 88] prove to be promising technologies but the centralized control over the whole network limits the size and latency of the data centers.

- The signal quality and strength have been another major hindrance when it comes to the parallel handling of large traffic. This problem is called the load-balancing problem. The parameters like BER [87, 114], quality of service, and extinction ratio [101, 108, 115] assure the signal quality. The improvement in [87] BER while keeping an eye on power penalty [55, 65, 88, 94, 98] is required for future networks.
- Given the growing measure of data centers today, the hundreds of thousands of racks and servers require non-trivial ingenuity. But the process is further complex when the system faces a large cascaded system of low-radix components that adds to increasing complicated topologies. Hence, scalable interconnects are in extreme demand because future DC are expected to support millions of microprocessor cores. The present structures need to upgrade from 2×2 [71-72, 87] to N×N ports to house more users at a time. The operations in high radix switching structures also need to introduce the cross-state operation to route the traffic to any port according to the current demand of the network. The current structures [72, 75, 101, 115] with only bar-state operation limit the size of data centers. Such issues also raise an eye on another parameter to be monitored i.e. conversion efficiency. This parameter is important [108] when the cross-bar operation is achieved in high radix switches.
- The configurations with high radix should have faster responses at each port. The switching time has been compromised in many structures [54, 76, 88, 111, 93] to maintain the quality and scalability of the DC switch.
- The robust non-linearities of materials should meet the low-power requirements of the device to have a power-efficient operation. The in-built non-linearities of some materials like ring resonators with graphene [105-107], antimonene [108], and SOA [28, 111-115,117] or induced non-linearities due to the use of polarizers [27] or other birefringent components in some configurations can ruin the power spectrum of the propagating signal.

2.9 Objectives of Thesis

Based on the above literature and gaps presented in the study, the following objectives of the thesis have been framed:

1. To propose high speed scalable photonic-interconnect based switching logic for load-balance architecture.
2. To design a switching logic with high throughput to compensate losses due to high latency.
3. To synthesize the power efficient photonic-interconnect based switching logic for high performance computing applications.

2.10 Contribution of Thesis

The proposed switching structure for high performance computation in data centers is capable of extending input-output ports. The presented structure removes the scalability issues by decreasing the port-spacing to balance the incoming user traffic data. The previous assemblies utilizing the SOA-MZI have limitations in exploring this aspect of load-balancing.

There is another factor that has been explored utilizing the impact of the injection current of SOA on various performance parameters. It explains the relation between increasing carrier density and further gain with respect to the injection current. The explanation of the large value of injection current can increase the non-linearities in the propagating path further opening many doors to the solution for overcoming the in-path non-linearities.

Since the structure offers both bar-state and cross-state operations even with a high radix of 8×8 with low port-spacing, the analytical analysis of non-linear crosstalk is performed w.r.t. to the gain regime of SOA and underlines the dependency of the output power of port-signals on the crosstalk. The emphasis is put on studying the impact on logic levels occurring in the input sequence and how their occurrence in alternative and consecutive places effects the system performance.

Another innovative result presented in this thesis belongs to the parallel monitoring of non-linear effects of SOA's birefringence. The configuration is then upgraded by introducing EDFA (Erbium Doped Fiber Amplifier) for mitigating the polarization dependency of TWSOA. The evaluation is done utilizing significant factors like Stokes parameters and Poincaré sphere and hence provides a solution to reduce non-linear effects by compound hybrid amplifiers.

This thesis then further takes the proposed structure to another level of achieving smart switching. The challenge of selecting a routing path that offers a minimum load and error-free reception has been overcome by the incorporation of a neural network based on Long Short-Term Memory. This study helps in finding the shortest and minimum error path by classifying various input-output port-path combinations of switching interconnect.

This thesis also explores the issues in the centralized operation of the control plane interface in the data centers. The incoming traffic could be dynamic and randomly distributed in the server racks. This thesis presents the TWSOA-EDFA-based smart logic routing of incoming traffic to the required server rack for switching it further to the ToR switch. Hence, the logic traffic routing in the Control Plane Interface i.e. CPI has been presented for routing and switching the incoming burst traffic data onto the server racks so that further processing could be done.

CHAPTER 3
DESIGN AND SYNTHESIS OF SWITCHING CONFIGURATION FOR HPC

3.1 Introduction

In this chapter, the objective of proposing a photonic switching structure that is superior to the previously reported techniques in terms of scalability, latency, and operating power has been achieved. With this study, the first objective of designing a high-speed scalable switching configuration for load-balance architecture has been fulfilled. The basic building block of the proposed switch has been tested to increase the scalability to attain the maximum number of users. The inputs of the switching structure are interconnected to all the outputs and are capable to achieve the crossbar operation by utilizing the XPM property of TWSOA. The cross and bar-state operation of the basic building block of the switch has been presented whose response analysis is done based on various performance parameters like BER, latency, OSNR, and extinction ratio (ER). In the next step, the final proposed 4×4 photonic switching configuration has been demonstrated to test the scalability and check the reliability of the switching parameters when compared to the basic building element. The power response at various switching stages has been illustrated and the switch is also monitored at different injection currents and OSNR. Lastly, the switching time response has been presented to obtain the lowest latency possible for load-balancing architectures.

3.2 Basic 2×2 Building Block

SOA technology has been in the advancing phase recently as it can offer compatibility in the monolithic integration with low cost potential and also has a large scope in the type of optical signal processing that can't be offered by other known optical amplifiers. The deployment of SOA is evolving due to its attractive non-linearities that provide switching operation with low power consumption parallelly offering good quality of service and high-speed performance. SOA-based wavelength conversion is possible by exploiting different properties of SOA i.e. XGM [28, 127, 129], XPM [130-131], FWM [29, 115, 123], and XPolM [163,157]. The XGM based converters can be used to improve the power penalties but XPM-based switching is more power efficient and has low chirp. The other issues related to the XGM phenomenon include polarization sensitive outputs, low values of extinction ratio [132], and output dependent on input sequence patterns at

high data rates. They also have shifted blue chroma at the rising edge of the pulse and shifted red chroma on the falling which also leads to vigorous positive chirp [132]. The XPolM-based converters are utilized for exploring the effect of polarization on the output. Whereas the FWM-based conversion utilizes the frequency and phase of an afresh generated mixed wave which further is the mixture of waves existing in an active region of SOA. This generates cons similar to that of XGM [132].

The XPM-based conversions offer easy monolithic integration and are possible by placing two SOAs in interferometric arms. This deployment of SOA can be either symmetric or asymmetric. The asymmetric configurations utilize way more power than symmetric, whereas the symmetric mechanism is able to nullify the slow relaxation [86] (~100 ps) creating ideal switching windows. The input signal is divided into MZI arms and the excitation of two SOAs is done by utilizing short control pulses that have a suitable time delay.

The SOA can also be configured in various types i.e. Fabry-Perot (FP), Travelling Wave (TW), and Reflective SOA (RSOA). The FPSOA can provide good optical feedback for increasing the SOA's gain but also have a lower bandwidth that makes it not suitable for light wave communication systems. The reflective SOAs can be applied in many application areas but because of their sluggish speed, it tends to show finite modulation bandwidth. [133] On the other hand, TWSOAs provide the active region without any need for reflective facets which tends to amplify [134] the signal in a single passage through the cavity. It also provides large bandwidth and is very less sensitive to polarization effects occurring inside that makes them applicable in various application areas.

For the above listed reasons, the TWSOA in symmetric MZI has been chosen best for the designing of crossbar structure to get a minimum possible error and efficient performance. For the testing purpose whether the current configuration is good enough for scalability, the 2×2 conversion has been evaluated on the ideal conditions i.e. with ideal coupling, zero input insertion loss, no receiver noise, and zero device angle to avoid any polarization effect on output.

In the basic building block of the switching circuit, the 2×2 crossbar conversion is done by symmetrically dividing the input pulse into each MZI arm. This signal is then utilized for saturating the SOA as it is intensity modulated by the introduction of the control signal on it. The carrier

density signal creates various refractive index changes in the input signal. Hence, this technique can further induce phase shifts in the input signals coming from the two cross inputs.

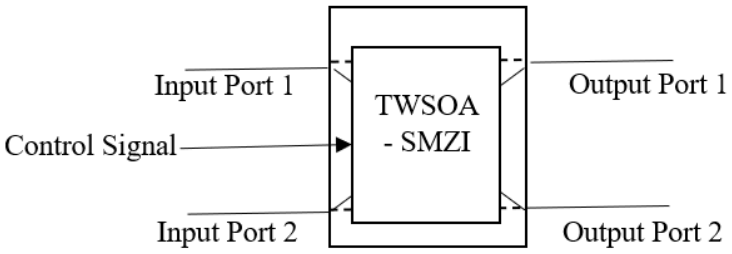


Fig 3.1 Basic assembly of 2×2 crossbar switch in utilizing TWSOA symmetric MZI arms

On the output side, the coupler is employed to recombine the two crossbar signals from the MZI arms following either constructive or destructive interference. This pattern of interference is decided by the relative difference of the phase found between the two arms of MZI at the time of recombination. This relative phase difference can also be controlled by the triggering bias current of SOA and controlling the optical power at the input side. The basic symmetric assembly can be illustrated in Fig. 3.1

3.2.1 Crossbar Power Distribution in terms of Gain

The semiconductor optical amplifier has a gain medium which generally contributes to its attractive features of switching. This gain is produced by the electron-hole pair recombination that is injected by the external circuitry. The active region present in SOA conveys this gain to the signal coming from the input side. This is the reason why SOA-based amplifies usually operate at high current densities. The optical signal having the energy of photon higher than the bandgap energy is incident on the active region of SOA, and the stimulated emission between valence and conduction band is observed. Due to this, an indefinite number of imperceptible photons have been generated that lead to the amplification of SOA. The gain medium witnesses the population inversion by regulatory injection current. This above process is more understandable with the following analysis. If 'M_g' is material gain, 'L_{soa}' is the length of SOA's active region, 'γ' is the confinement factor of active media, '*l*' is a total loss, then the final gain of SOA i.e. 'G_{soa}' in the input signal can be observed by the following equation 3.1 [135]:

$$G_{soa} = e^{[(\gamma M_g - l)L_{soa}]} \quad 3.1$$

There is a shortage of transitioning carriers if the beam is kept appropriately concentrated on the active region which further leads to saturated amplification. While on the other side, if there is the absence of an input signal and a low concentration of carrier, the gain of the SOA is estimated using the carrier lifetime directed by the earlier spontaneous emission. The presence of an input signal leads to less carrier lifetime because of stimulated emission. This effective carrier lifetime 'τ_{eff}' can be evaluated using the analysis of a small signal and the concluding lifetime evaluated is shown by equation 3.2 [135]. If the differential lifetime of the carrier is 'τ_{d}', 'υ_{group}' is group velocity, and '(D_{out})' is the output density of the photon, then

$$\tau_{eff}^{-1} = \tau_{d}^{-1} + \upsilon_{group}\left(\frac{G_{soa}+1}{G_{soa}}\right)\left(\frac{dg}{dN}\right)(D_{out}) \qquad 3.2$$

This differential lifetime is also estimated in terms of 'τ_{sp}' i.e. spontaneous recombination rate as $\tau_d = \left(\frac{d\tau_{sp}}{dN}\right)^{-1}$. When the current is not present, an incident signal is blocked by SOA and when the current is absent, an incident signal is passed by SOA with appropriate gain. The SOA has an on-off and rise-fall time of its own which makes it perfect for switching and routing applications. The output signal power i.e. 'P_o' is given by equation 3.3 [135] when the signal power before and after recombination in the upper arm is denoted by 'P_u' and the same in the lower arm is 'P_l', and the phase difference between them is 'ϕ_p':

$$P_o = P_u + P_l + 2\sqrt{P_u P_l}\cos(\phi_p) \qquad 3.3$$

The evaluation of the transfer function is done utilizing the SOA gain deployed in MZI arms. The slope of this transfer function shown in the above equation 3.1 decides the inversion of output signal w.r.t. input around an appropriate point of operation as shown in Fig. 3.2.

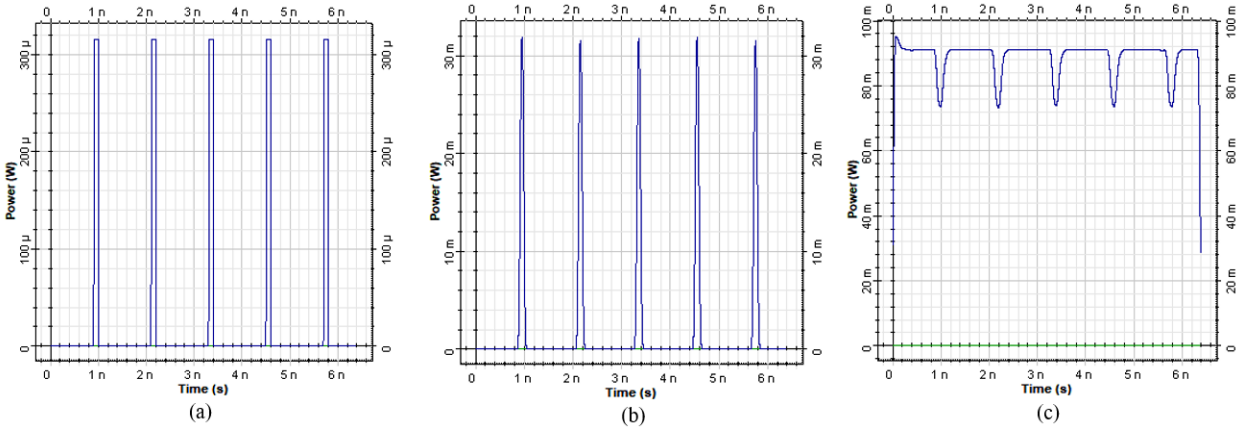


Fig. 3.2 (a) Input signal (b) Recieved signal (c) Inverted output at cross-state

In the end, the final cross and bar-state output power i.e. 'P_X', and 'P_B' can be evaluated with upper arm gain i.e. 'g_u', and lower arm gain i.e. 'g_l' as shown in equation 3.4 and equation 3.5 [135]:

$$P_X = \frac{1}{4}\left(g_u + g_l + 2\sqrt{g_u\, g_l}\, cos(\phi_p)\right) \quad 3.4$$

$$P_B = \frac{1}{4}\left(g_u + g_l - 2\sqrt{g_u\, g_l}\, cos(\phi_p)\right) \quad 3.5$$

3.2.2 Cross-State Operation of Basic Crossbar Switch

The working of the 2×2 switch is evaluated utilizing the Pseudo Random Sequence Generator (PRBS) for deterministic signial generation at the input ports. The 3 dB couplers have been employed that couple the signal equally in MZI arms with 0.5 coupling coeffients.

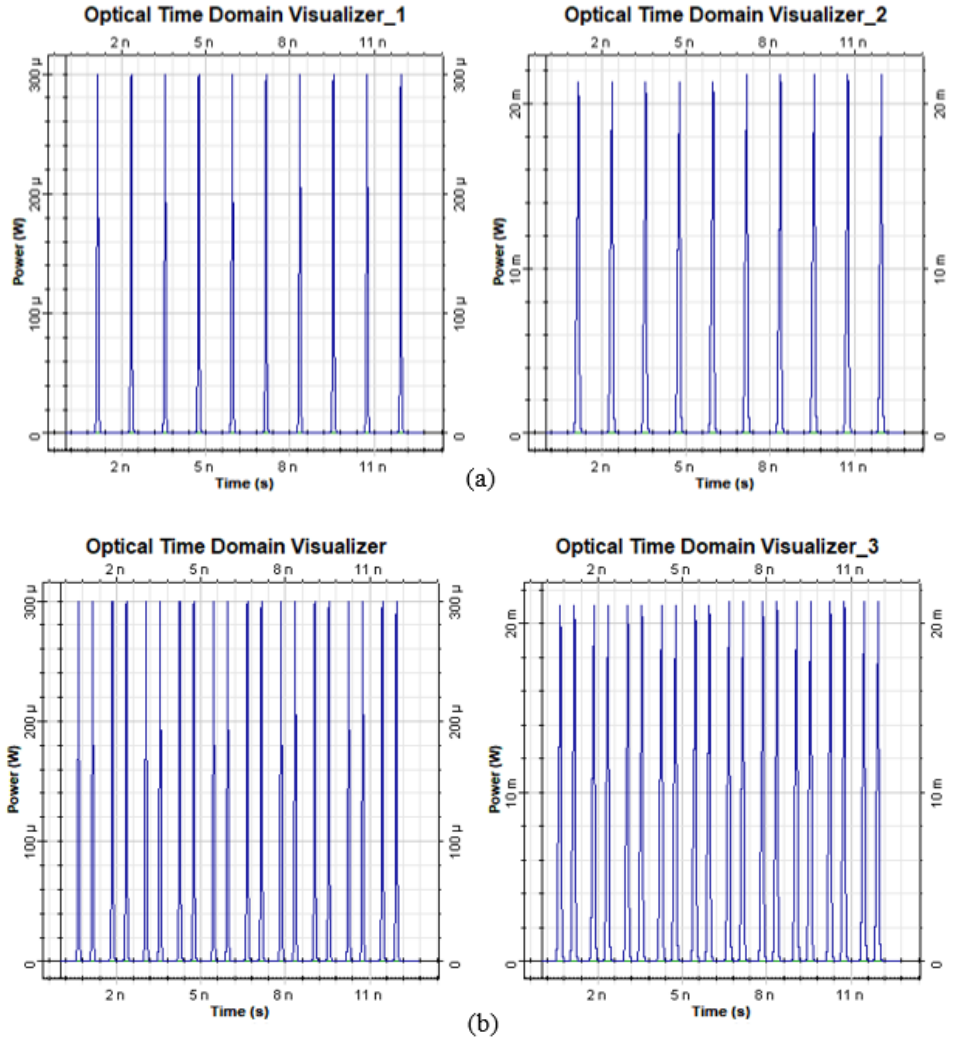


Fig. 3.3 Transmitted and received signal at (a) port 1 (b) port 2 respectively at cross-state

The PiN photodiode is utilized to detect the waveforms at the receiver end. The simulations are attained in Optisystem 7.0 at the data rate of 10 Gbps. The results obtained for cross-state operation show good quality of service with Q-factor (QF) of 22.4246 dB and 30.4555 dB on the first and second output ports respectively.

When the polarization sensitivity conditions of TWSOA are not considered, the output signal identically matches with input as shown in Fig. 3.3. Since the control signal power gets modulated with a signal transmitted by the input source, the probe power at the output also gets modulated which gives the correct data transfer to the desired port.

The study of the power spectrum of received optical output also has significance for learning the power distribution over particular transmitted wavelengths. There is a small noise spectrum under the control signal that can be observed from the input and output power spectrums shown in Fig. 3.4 (a) and (b) respectively that occurred due to the non-linearities occurring in the TWSOA-SMZI loop. This added noise further lowered the output signal strength in comparison to that of the input.

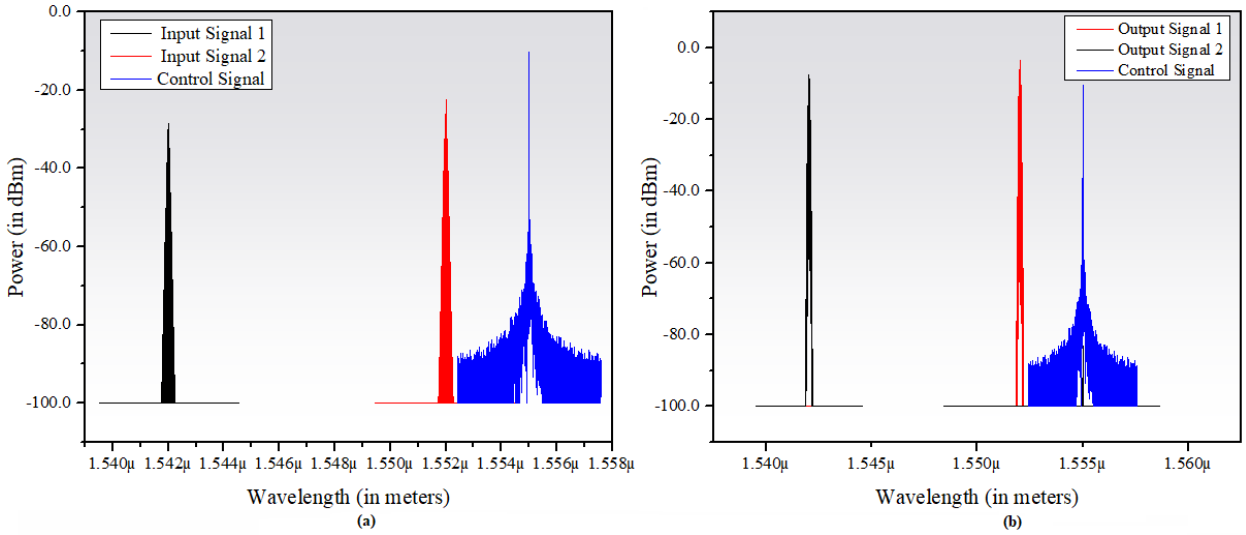


Fig. 3.4 Power spectrum of transmitted, received, and control signals at (a) input (b) output ports

3.3 Response Analysis of 2×2 Building Block

The response analysis of the above structure is perceived at the data rate of 10 Gbps. The large overshoots and noise factors that correspond to weak outputs can be perceived by an eye diagram.

The important factors from an eye diagram i.e. Eye-Opening Factor (EOF), Quality Factor (QF), and Eye-Height (EH), also illustrate the performance of the switch as shown in Fig. 3.5.

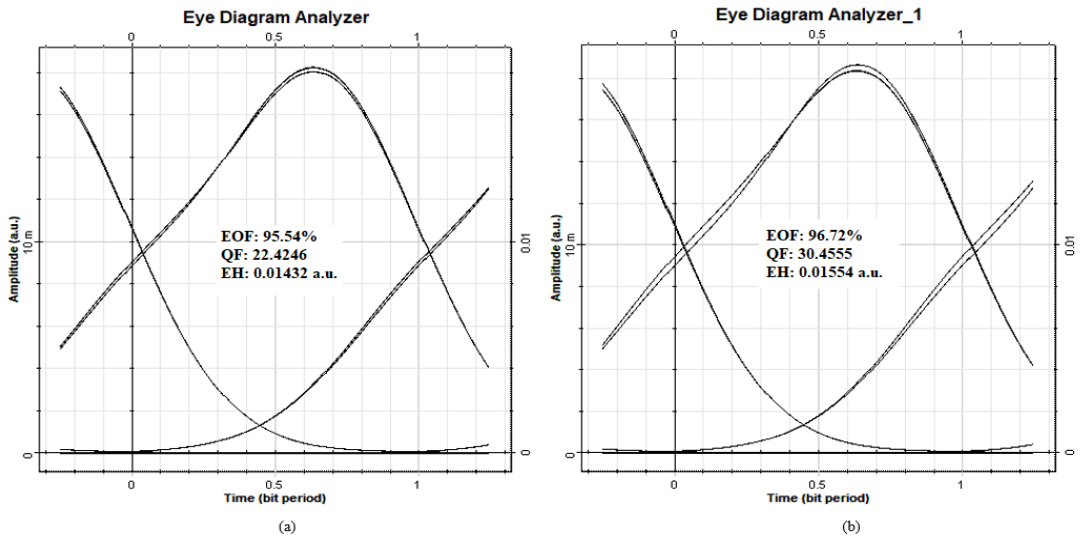


Fig. 3.5 Received eye-diagram with EOF, QF, and EH at (a) Port1 and (b) Port2

1. *Eye-Opening Factor (EOF):* The eye opening illustrated by EOF corresponds to distortion due to inter-symbol interference evaluating the overall performance. This EOF factor is evaluated by utilizing the average and standard deviation values of logic '0' and '1' i.e. 'μ(0)', 'μ(1)', 'σ(0)', and 'σ(1)' respectively as shown in equation 3.6 [141]. It is observed that EOF of 95.54% and 96.72% has been achieved at output ports 1 and 2.

$$\mathrm{EOF} = \frac{[\mu(1) - \sigma(1)] - [\mu(0) - \sigma(0)]}{[\mu(1) - \mu(0)]} \qquad 3.6$$

2. *Eye-Height (EH)*: The next parameter defines the vertical height of an eye obtained in the eye-diagram that determines the closure of the eye due to noise given by equation 3.7 [135] measured in a.u. as:

$$\mathrm{EH} = [\mu(1) - 3\sigma(1)] - [\mu(0) + 3\sigma(0)] \qquad 3.7$$

3. *Q-factor (QF)*: It is the qualitative measure of noise present in the signal for analytical purposes. It can be evaluated from equation 3.8 [135]. The Q-factor of 22.4246 dB at output Port1 and 30.4555 dB at output Port 2 for cross-state operation is achieved.

$$\mathrm{QF} = \frac{|\mu(1) - \mu(0)|}{\sigma(1) + \sigma(0)} \qquad 3.8$$

4. *Latency:* Latency of the switch is evaluated in terms of Switching time (T_s). It is measured as the delay corresponding the translating the data and switching it to the destination nodes over

a network. It is observed that for an elementary 2×2 switching configuration with the cross-state operation, the time taken to switch the data from port 1 to 2 is 0.227 ns, and from port 2 to 1 is 0.243 ns. This proves the superiority of the structure for faster responses.

5. *Extinction ratio (ER)*: This factor is the most significant in determining the performance of the system.

$$ER = \frac{\mu(1)}{\mu(0)} \qquad 3.9$$

A very small alteration in the ER can lead to the large relative difference in power level that is needed to maintain the Bit-error-rate of a system constant. The ER also contributes to penalties in an optical link and is evaluated by equation 3.9 [141]. The ER during transmission of data from Port 1 to 2 and viz-a-viz is 15.2033 dB and 18.5129 dB respectively.

3.4 Proposed 4×4 Switch Configuration from 2×2 Block

The proposed design of a 4×4 photonic interconnected switch is obtained by utilizing five elementary 2×2 TWSOA-SMZI loops as discussed above and the illustrated 4×4 configuration is given in Fig. 3.6. The signals at the input ports are identified as I_1, I_2, I_3, and I_4 and the output port signals are denoted as O_1, O_2, O_3, and O_4.

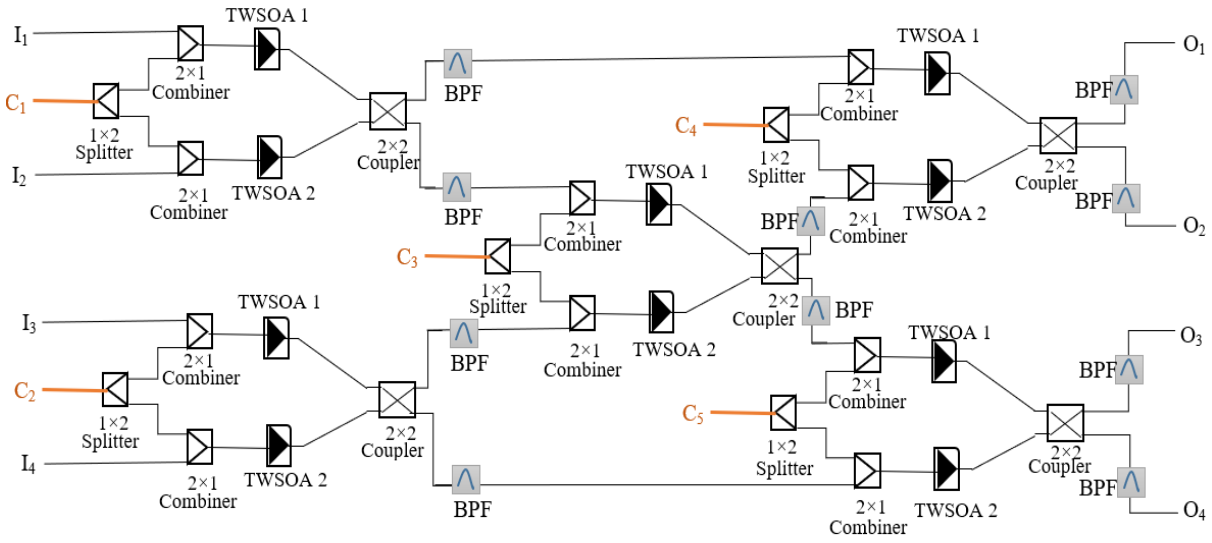


Fig. 3.6 Proposed 4×4 interconnecting switching structure using five 2×2 TWSOA-SMZI loops

As the intensity modulation of input occurs when the control trigger is induced on it that further introduces phase shifts, each loop utilizes the control trigger as C_1, C_2, C_3, C_4, and C_5 for the

switching action to occur. The output stage in every loop also requires blocking filters (BF) to block out the interference of the control pulse in the switched signal. The four input ports are fed with Continuous Wave (CW) pulses with a Pseudo Random Bit Sequence (PRBS) generator. The SMZI-based cascading assists in maintaining the same level of input power at all stages.

3.5 Scalability and Latency Analysis with Performance Monitoring

The scalability of the proposed structure can only be guaranteed if there exists consistency in parametric values with the increase in TWSOA-MZI loops and stages. The proposed structure provides consistent values of QF, EOF, EH, T_s, and ER in increasing the radix from 2×2 to 4×4. This implies the capability of the proposed design to handle the proliferation of users while maintaining the quality of service. The consistency comparison of these parametric values can be observed in Table 3.1. The average values of parameters for 2×2 and 4×4 configurations are measured as EOF: 96.13% and 96.185%; EH for same are 0.014943 and 0.011375 a.u.; QF: 26.44 and 26.58; ER: 16.858 dB and 16.7122 dB; and T_s: 0.151169 ns and 0.2038 ns respectively.

Table 3.1: Consistency Evaluation of various parameters of 2×2 and 4×4 switching configurations

Config. ↓	**O/P Ports ↓**	**Parameters of Proposed Method**						
		P_{in} (dBm)	**P_{out} (dBm)**	**EOF (%)**	**EH (a.u.)**	**QF**	**ER (dB)**	**T_s (ns)**
2×2	Port 1	-18.763	4.889	95.54	0.0143262	22.4246	15.2033	0.193935
	Port 2	-15.752	1.982	96.72	0.0155428	30.4555	18.5129	0.108404
4×4	Port 1	-18.763	4.995	95.75	0.0146194	23.5266	15.1394	0.227609
	Port 2	-15.752	1.994	96.71	0.0155639	30.3341	18.5221	0.146790
	Port 3	-18.349	4.982	95.73	0.0145654	23.4363	15.1284	0.243706
	Port 4	-15.752	1.256	96.55	0.0153721	29.0246	18.0591	0.197238

1. *Power Response*: The power distribution of input and output signal at four ports can be observed in Fig. 3.7 (a) and (b). Due to the non-linearities occurring in five loops, the noise spectrum at 1550 nm can be easily observed in the power spectrum and these can be filtered out by utilizing appropriate gaussian filers. Another important observation from power response is the received output power. Since HPC systems are complex and go through various

power losses, it becomes necessary to receive high output power to guarantee a good reception of the signal. It is observed from Table 3.1 that the input power is amplified due to the use of TWSOA in the configuration and positive power is received.

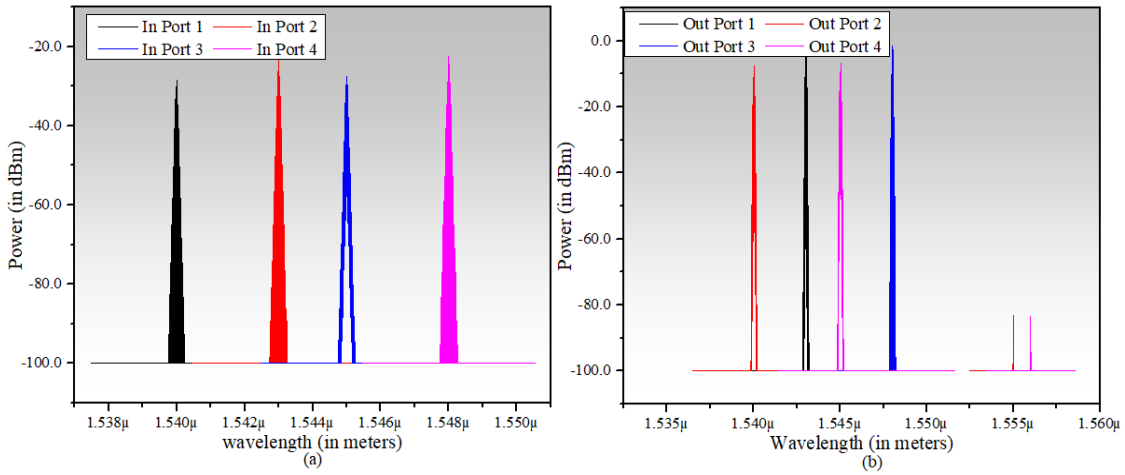


Fig. 3.7 (a) Input and (b) Output Power spectrum of 4×4 optical switching configuration

2. *Eye-Diagram and Quality of Service*: It is observed from Fig. 3.8 that the eye-diagrams at four ports have wide openings and good eye-height corresponds to noise-less switching operation.

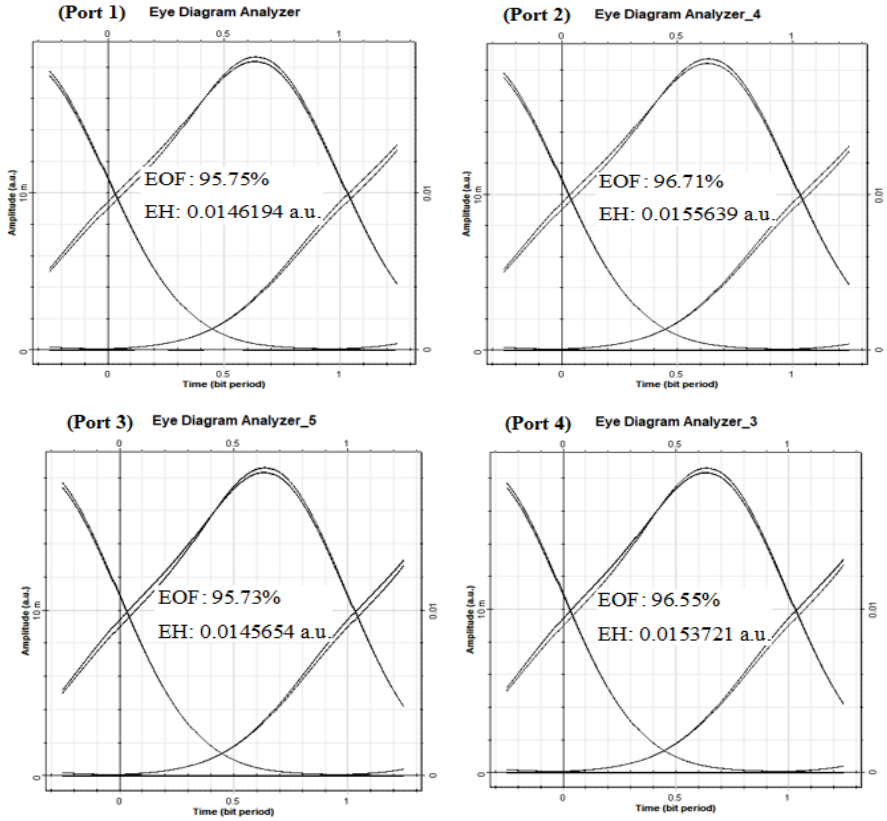


Fig. 3.8 Cross-state Eye-Diagrams at four output ports of 4×4 switch

The graphs in the following Fig. 3.9 illustrate the QF curve against amplitude and bit period for corresponding output ports proposed 4×4 switch. The high values of QF at each port in cross-state operation make the configuration suitable for data center applications.

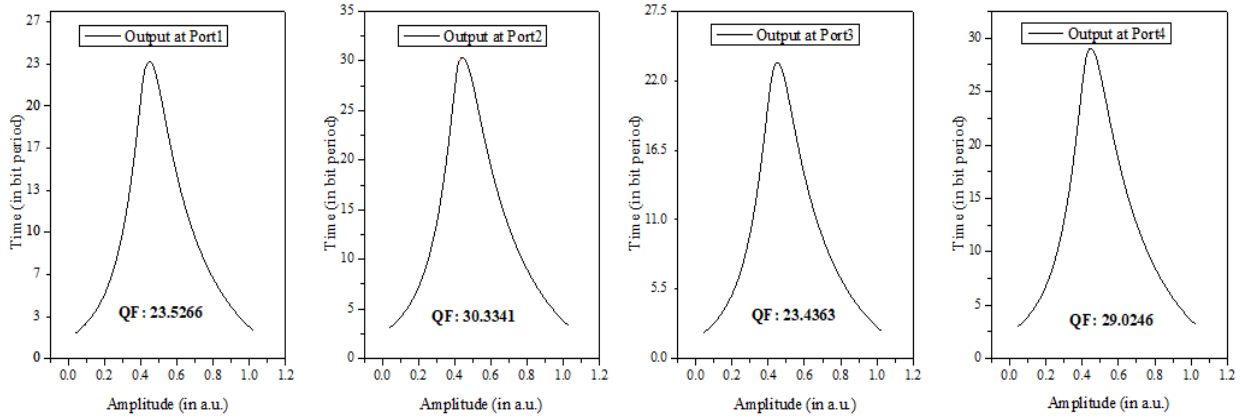


Fig. 3.9 Quality factor curves at four output ports

3. *Latency:* It can be observed from Table 3.2, the switching time at four different ports is 0.2038 nano seconds and the consistency in values to that of the 2×2 configuration stands a proof that the proposed configuration is suitable for scalability applications.

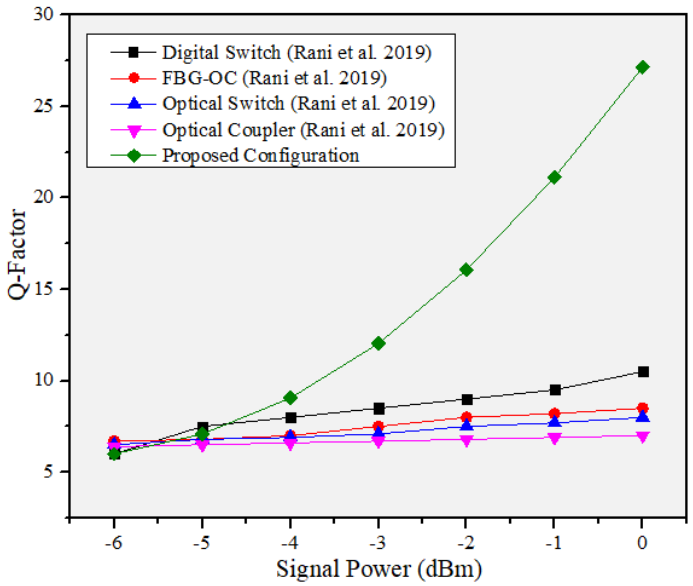


Fig. 3.10 Comparison of QF w.r.t. I/P power with reported techniques in (Rani et al. 2019) [136]

The superiority of the proposed technique for switching purposes has been guaranteed based on the quality factor comparison shown in Fig. 10 with previous reported methods by Rani et al. [136]. The comparison results show that the implemented method can offer a better quality of service as

compared to digital switches whose QF is 10.5, the Fiber-Bragg-Grating-Optical coupler based method have a QF of 8.5, single optical coupler based technique achieved the same at 7 and optical switch is 8 whereas as the implemented results have highest quality factor of 26.58. Hence, the method proves to be capable of being scalable and also maintaining a high quality of service and good solution for the data centric applications.

3.6 Conclusion

In this chapter, a 4×4 TWSOA-SMZI-based photonic interconnected switching configuration has been presented. It is designed by utilizing a basic elementary switching loop of 2×2 interconnections. The performance is checked on ideal conditions that if the structure is capable of scaling to the higher radix. The performance is monitored using numerous parameters like QF, EOD, EH, ER, and latency. The switching operation is checked for both bar and cross-state interconnections to check the effect of inter-symbol interference. The effect is monitored utilizing eye-diagrams and quality factors curves. The power distribution in the received and transmitted spectrums is also compared to check the unwanted power distribution in the output signal. The structure offers reliability in parametric values when scaled from 2×2 to 4×4. The evaluated performance at a data rate of 10 Gbps gives 96.13% and 96.185% wide-opening of an eye for 2×2 and 4×4 configurations respectively. It exhibits high quality behavior with a Q-factor of 26.44 and 26.58 for 2×2 and 4×4 radixes. A similar consistency can be seen in EH and switching time for both configurations which stands a proof of the structure being scalable. The fast response time of 0.2038 ns shows the low latency feature of the implemented method. The structure also yields large positive values of output powers that can solve power loss problems in complex HPCs. Hence, the structure can be further evaluated by increasing radix for load-balancing issues. The current structure is capable of handling a surge in users in datacenters.

CHAPTER 4
PROPOSED 8×8 SWITCH CONFIGURATION FROM 4×4 SWITCH

4.1 Introduction

In this chapter, the first and third objective of the thesis has been fulfilled by achieving a scalable and power efficient structure with low latency and offering a solution to HPC challenges in DCs. The report by E. N. Lallas [137] showed the significant features of appending switching apparatus in DCs. SOA switching techniques prove to be efficient in terms of power for long-haul applications with good cascading features but the decreasing quality [130] and high response times for high power operations have always been an issue. This chapter tries to put forward an improved switching configuration. The 4×4 structure shown in Chapter 3 is further explored for 8×8 interconnections and cross-bar operation is tested on various parameters like Bit Error Rate (BER), ER, EH, EOF, Optical-Signal-to-Noise-Ratio (OSNR), and output power. The stage-wise performance has been monitored for received powers and OSNR. It further explains the impact of injection current on error rates and quality of service and further brings out an optimization of injection current to be best operated on. The chapter also presents a comparative analysis of 2×2, 4×4 presented in chapter 3, with the proposed 8×8 interconnected switching structure to check the reliability of results. To offer it as a solution to the power consuming HPC systems, the investigation on the power penalty of the structure has also been made. The final chapter concludes finally with the comparative results from the previously reported structures where the proposed arrangement proves its excellency in maintaining the performance in terms of power penalty, latency, and quality of service.

4.2 8×8 Photonic Switch Setup

The power-hungry operations in HPC systems at various data centers prove to be expensive in terms of maintaining the quality of service that is promised to customers. The proposed 8×8 switch configuration for data centers is shown in Fig. 4.1. The commodity electrical switches called ToR are attached to server racks and ToR is further attached with optical interconnection transceiver arrangements. The ToR direct links with multiplexer (MUX) and demultiplexers (DEMUX) in between which an all-photonic switching configuration is utilized for achieving the faster routing of user data. The proposed interconnection can be utilized between mux and demultiplexer above

ToRs. The 8×8 structure has three stages where the first and third stage is built up with the help of an elementary 2×2 TWSOA-SMZI loop and the middle stage has proposed a 4×4 switching structure for making middle stage interconnections.

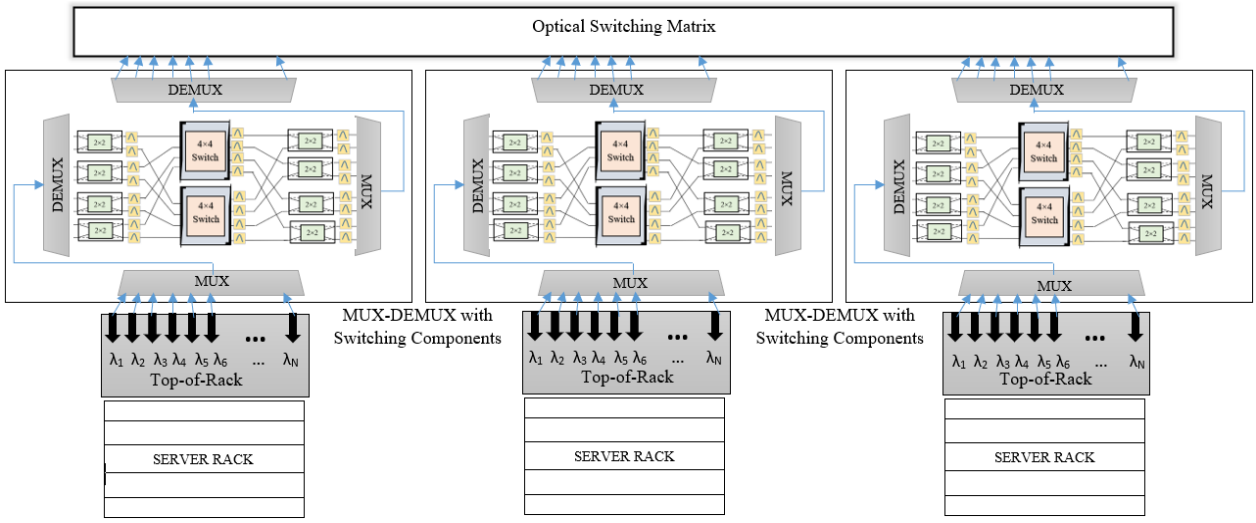


Fig. 4.1 8×8 Switching Configuration for Data Center Applications

The working of the implemented design is based on the XPM effect of TWSOA i.e. with the generation of a phase difference between SMZI arms, the effect of the control signal can be observed on the co-propagating and counter-propagating signal.

4.3 Results and Discussion

The first results are carried out to analyze the response of the system w.r.t. the power alterations with the increase in switching stages. The evaluations are also done utilizing various performance parameters like OSNR and investigation on the injection current of TWSOA shows how it alters the carrier density and hence the QF values. With the power response analysis, the latency with scalability is also monitored and the final comparison is done for low to high radix structures.

The first results presented are eye-diagrams with the EH values at each port 8×8 switch. The wide opening after three stages shows that the output is not much affected by the large overshoots. The received EH on the eight ports on average is 0.035166 a.u. which indicates good reception for a highly scalable system. The eye-diagrams port eight ports with their corresponding values are illustrated in Fig. 4.2.

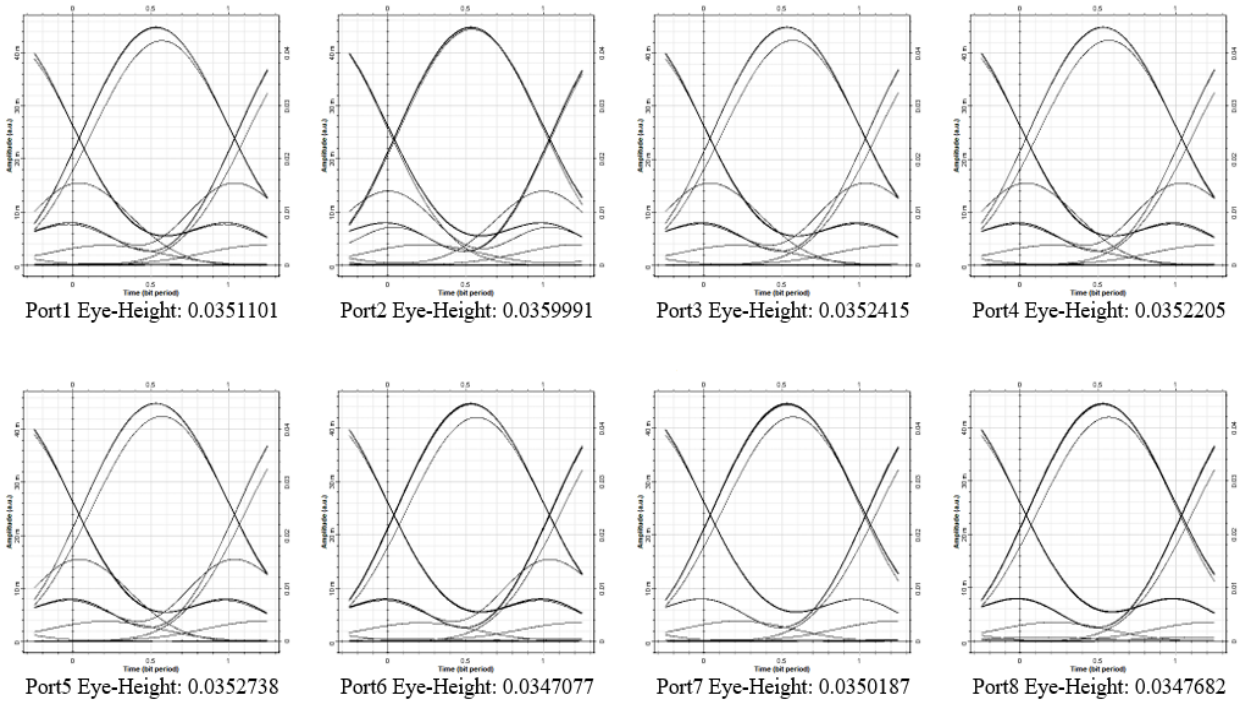


Fig. 4.2 Eye diagrams with corresponding EH value at eight ports of proposed 8×8 switch

4.3.1 Output Power Analysis

The power response analysis is done in two ways: Firstly, the output power is observed with the increasing stages to monitor the fall due to the surge in TWSOA-SMZI loops for creating 8×8 interconnections. In the later part, evaluation is done utilizing the injection current in the picture to bring out the best possible value of injection current for cross-bar operation. It is observed that the large injection currents can bring noticeable effects on the refractive index further altering the final output. On the other hand, very small values can also weaken the received signal strength.

1. Output Power vs Input Power: Since the reception of high powers w.r.t. input is desired for HPC systems to decrease the demand of post amplification and regeneration of signals at the receiver end, the proposed structure efficiently achieves this target. The signal transmission at all eight input ports is done at 0.3 mW [138]. The power at each succeeding stage can be seen as consistent with the previous one. It shows no loss during the propagation of the signal through the loops due to the use of a TW-semiconductor amplifier. The average received power at stage 2 i.e. 'P_{r1}' is 12.521 dBm, the same at stage 2 and stage 3 i.e. 'P_{r2}', 'P_{r3}' are 11.93426 dBm and 11.9342 dBm respectively. The actual variation in the power at each port can at various stages be observed in the following Table 4.1.

Table 4.1: Stage-wise power received in 8×8 proposed configuration

Stages →	**Stage 1**	**Stage 2**	**Stage 3**
Ports ↓	P_{r1} (dBm)	P_{r2} (dBm)	P_{r3} (dBm)
Port 1	12.5116	12.1360	11.927
Port 2	12.5180	13.0462	11.9201
Port 3	12.5108	12.1036	11.8990
Port 4	12.5231	12.0427	11.9332
Port 5	12.4807	12.1200	11.9389
Port 6	12.5321	12.1388	11.9040
Port 7	12.5243	12.1356	11.9892
Port 8	12.5667	12.1383	11.9627

2. Investigation of Injection Current on Output Power: The next step is to involve different injection currents to observe the power variations at the output. The study by Singh et al. [139] shows that the injection current values 70 mA, 90 mA, and 100 mA give high power penalties, and values greater than 150 mA could degrade the performance due to increased amplified spontaneous noise (ASE).

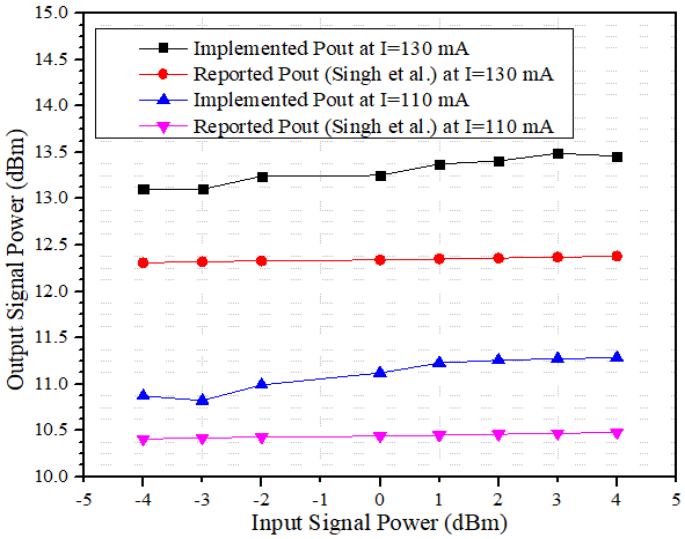


Fig. 4.3 Output power variation with input power and injection current of TWSOA and comparison with results reported in [139]

Hence, the evaluation of choosing the best injection current has been done for 110 mA and 130 mA. An observation can be made from the comparison graph shown in Fig. 4.3 that the better

output power is received at 130mA of injection current and implemented results are better than the reported structure in [139].

3. *Power Penalty:* The power penalty of the system is an important factor when non-linear devices are utilized in the switching configurations [140]. The pulses in practical scenarios suffer distortion due to various irregularities during their propagation and noise present in the system. To maintain the guaranteed quality and provide acceptable error rates, the input signal power is usually increased. This can lead to power penalty problems [141].

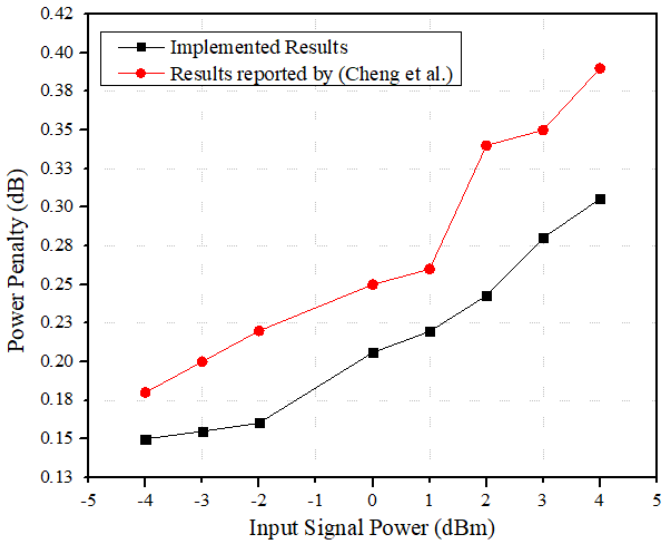


Fig. 4.4 Comparison results of power penalty reported in [54]

Hence, it is calculated by the difference between the power considered with and without the non-linear impairments of the system. It can be observed from Fig. 4.4 that the power penalty for the implemented technique lies between 0.15-0.30 dB which is quite less than the switching structure reported by Cheng et al. [54].

4.3.2 Parametric Performance Investigation

1. Bit-Error-Rate (BER): As the BER measures the error bits in the received signal, the lower values of BER are desired. From Fig. 4.5 (a), consistent values of BER of 10^{-16} are observed at all three switching stages of the proposed switching arrangement. The BER evaluation at a different injection current in Fig. 4.5 (b) shows that the BER values lie on the extreme highs when the uttermost high and low values injection current is chosen. It happens because of large refractive index changes occurring in the TWSOA due to the non-linearities induced in TWSOA-SMZI

loops. This can further degrade the system performance by inducing large error bits in the output signal. The values of injection current ranging between 0.12-0.16 A are chosen as good for witching operation. Where the value 0.15 A, the BER performance is much improved. The TWSOA operation is normally considered as low-power operation due to in-built amplifications, the proposed configuration gives the improved BER values even at higher power as illustrated in Fig 4.5 (c) which shows the structure is reliable for high-power operations in HPC applications.

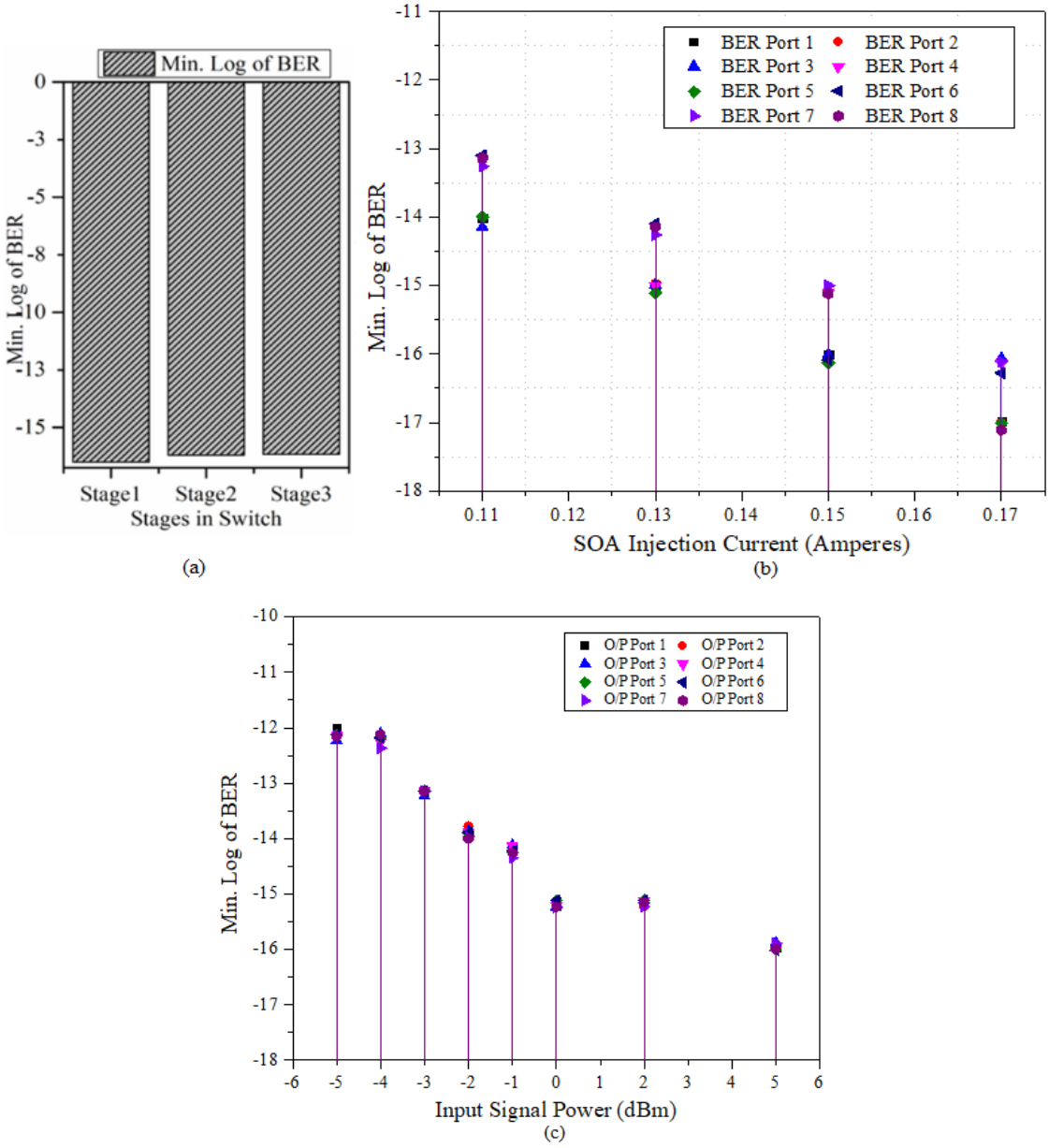


Fig. 4.5 BER performance (a) at successive switching stages (b) w.r.t. injection currents (c) w.r.t. input power at each port

2. Optical-Signal-to-Noise Ratio (OSNR): The performance measurement of a device can be evaluated by OSNR utilizing equation 4.1 [135]. The higher values of OSNR indicate the lower noise content 'P_{s_n}' in the signal '$P_{S_{in}}$'.

$$\text{OSNR} = 10\,\text{Log}_{10}\left(\frac{P_{S_{in}}}{P_{s_n}}\right) \quad 4.1$$

Due to the 3-stages of switching, it becomes important to be affirmative about the noise signal degrading the performance at each stage through the OSNR parameter. The average value of OSNR at stages 1, 2, and 3 are 21.5205 dB, 21.1076 dB, and 20.9347 dB respectively also illustrated in Fig. 4.6 (a) showing undeviating values of OSNR at three different stages. The good OSNR at three switching stages specifies the easy recovery of a received signal.

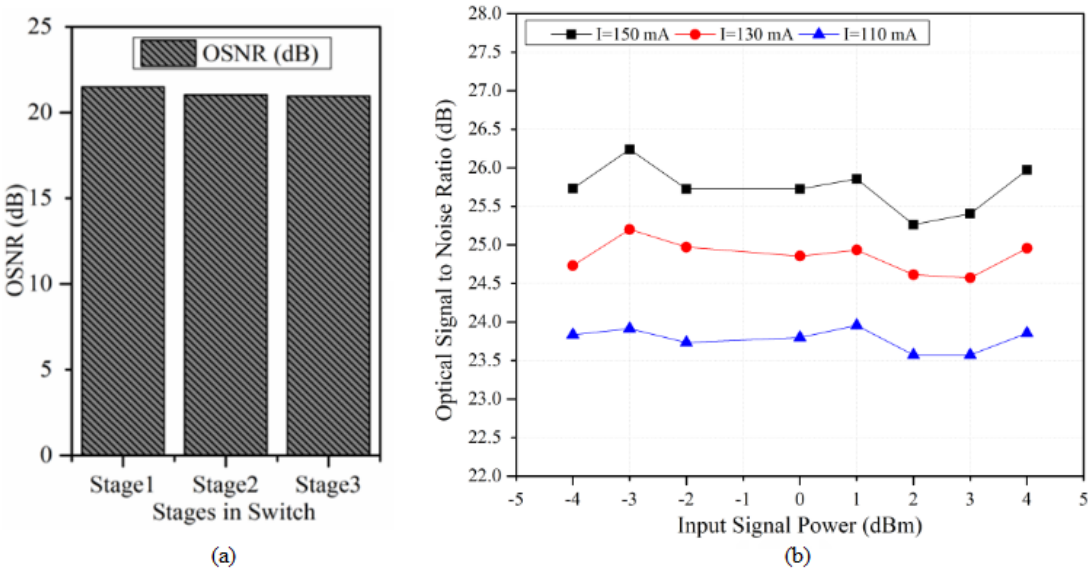


Fig. 4.6 OSNR evaluation (a) at each stage (b) w.r.t. input power for different injection currents

The evaluation of OSNR has been done at different injection current values and it is observed from Fig. 4.6 (b) that with the increase in TWOSOA injection current from 110 mA to 150 mA, the OSNR increases from 23.5 dB to 26 dB. Further effects have been seen in another performance factor to bring an optimized value of injection current for the arrangement to operate on.

3. Quality factor (QF): The QF values are noted as 24.65, 24.78, and 24.78 for successive stages in Fig. 4.7 (a) which signifies the good qualitative behavior of the proposed switch with three-stages. The QF evaluation is also done at input powers varying between -5 dBm to 5 dBm like

BER to observe the high-power operation response. The surging fashion is observed for QF of 19.29 at -5 dBm, 25.52 at 0 dBm, and 26.58 at 5 dBm.

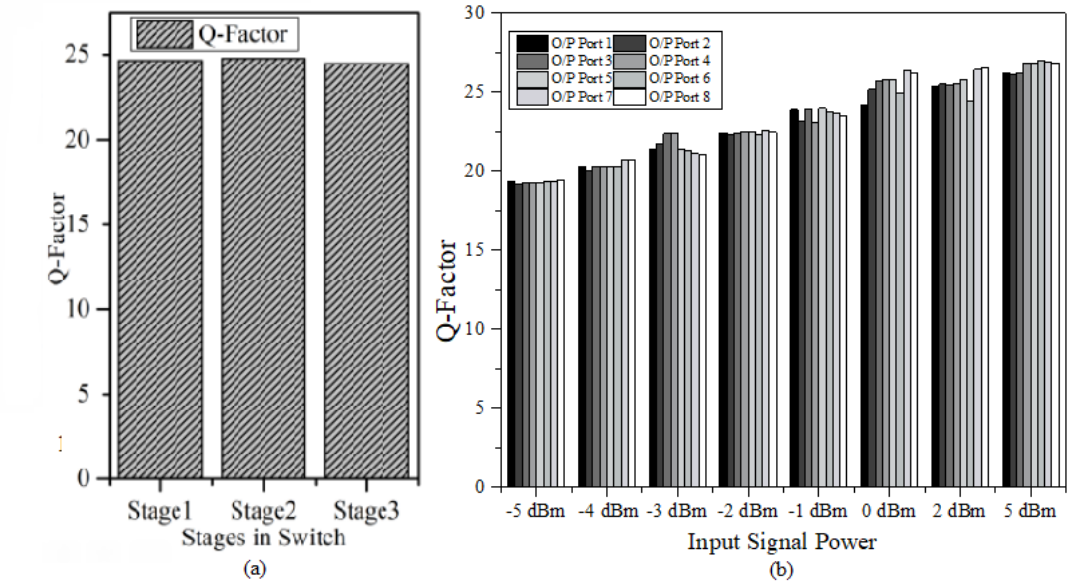


Fig. 4.7 QF evaluation at (a) various stages (b) various input powers

This shows that high-power doesn't bring an abrupt change in Q-factor and can promise a good quality of service at high powers.

4. Extinction ratio (ER): It tells how efficiently the power is transmitted to the destination by measuring the ratio of high logic average to power to that of low logic. The results in Fig. 4.8 show that the ER value improves from 14.3 dB at -5 dBm to 19.902 dB at 5 dBm.

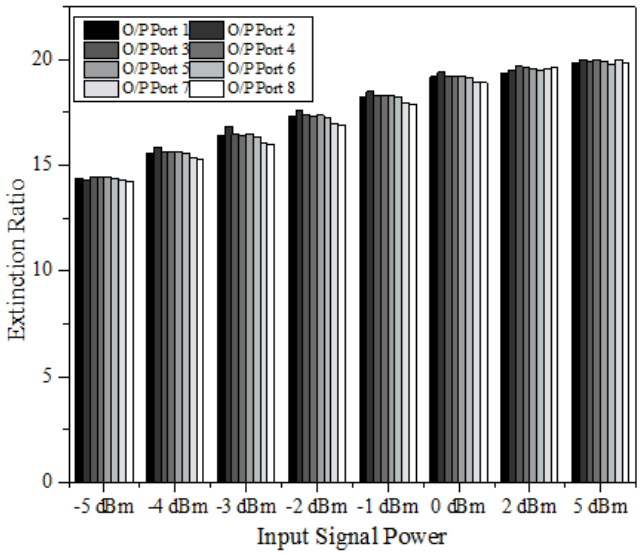


Fig. 4.8 Port-wise Extinction Ratio for various input powers

5. Eye-Opening Factor (EOF): As high values of EOF show the low noise content of the output signal, the proposed structure is also evaluated on EOF.

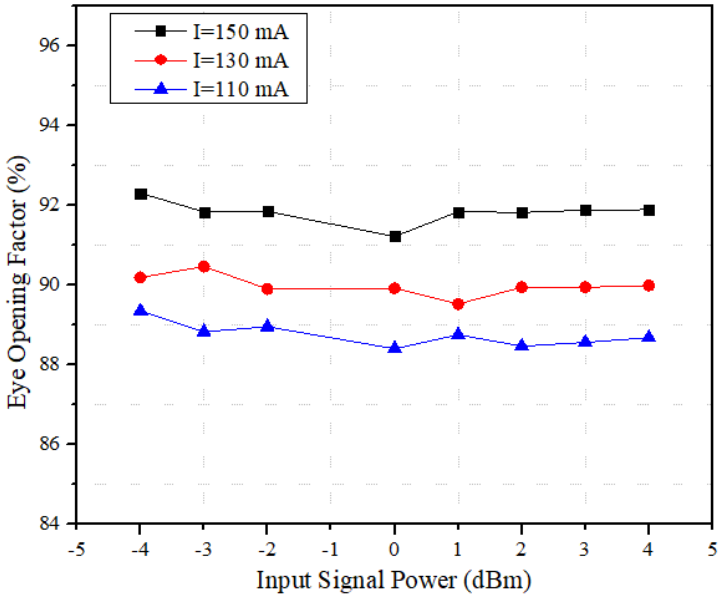


Fig. 4.9 EOF variations with injection current at various input powers

It can be observed that EOF improved from 89% to 92.5% with the increase in injection current from 110 mA o 150 mA. Whereas the structure shows consistent opening when the input power is varied between -5 dBm to 5 dBm.

The above evaluation shows that the improved values ER, QF, and BER are obtained even at high input powers. On the other hand, the reliable results with successive switching stages prove that the switching complexity doesn't disturb its performance. Hence, the proposed configuration is power efficient and also provides reliable results even with the increase in switching stages.

4.3.3 Switching Time Response

The fast response has been achieved with a switching time of 0.333 ns for the proposed 8×8 interconnected switch configuration. The regular evaluation is done while increasing the port radix from 2×2 to 4×4 and finally to 8×8. The switching time at each port of the 2×2 elementary block, the proposed 4×4 switch, and the proposed TWSOA-SMZI based 8×8 assembly can observe in Table 4.2. The lower values of switching time in nano seconds show the high-speed feature of realized configuration.

Table 4.2: Latency monitoring with an increase in scalability from 2×2 to 8×8

Config.	Ports	T_s (ns)	Ports	T_s (ns)
2×2 Switch	Port 1	0.193935	Port 2	0.108404
4×4 Switch	Port 1	0.227609	Port 3	0.243706
	Port 2	0.146790	Port 4	0.197238
8×8 Switch	Port 1	0.354916	Port 5	0.350360
	Port 2	0.381336	Port 6	0.367284
	Port 3	0.270190	Port 7	0.300952
	Port 4	0.345000	Port 8	0.296360

4.3.4 Scalability Monitoring and Comparison

For scalability monitoring, the performance of the system is evaluated on the parameters like BER, QF, ER, and OSNR during the increase in port-radix from 2×2 to 4×4, and finally to 8×8. In Fig. 4.10 (a), the radix-wise BER evaluation can be observed with the variation of input power from -5 dBm to 5 dBm. This shows the BER of 10^{-18}, 10^{-17}, and 10^{-16} are attained for 2×2, 4×4, and 8×8 interconnected switches respectively at a high input power of 5 dBm. The QF values of 25.92, 25, and 24.64 have been achieved for 2×2, 4×4, and 8×8 respectively.

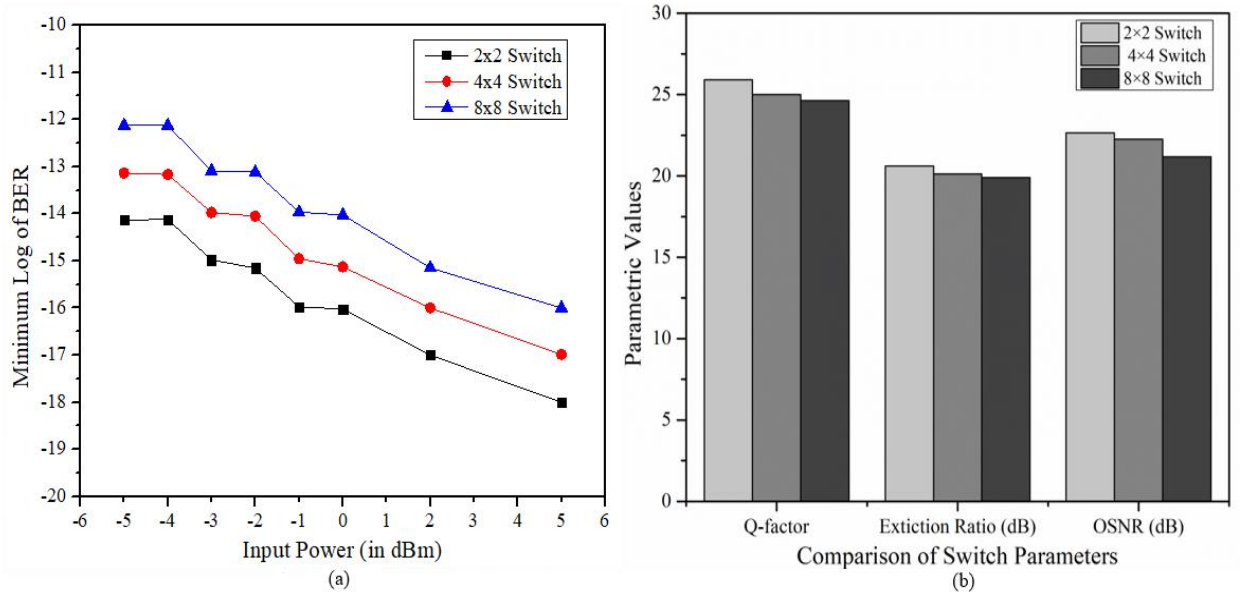


Fig. 4.10 Scalability monitoring for 2×2, 4×4, and 8×8 configurations using (a) BER (b) QF, ER, and OSNR

Similarly, for the three configurations, the value of ER is 20.1629, 20.1221, and 19.9002 dB, and the values for OSNR are 22.641, 22.26, and 21.1876 dB respectively. The consistency in the values shows that the increasing complexity of the structure doesn't have an adverse effect on the final output of the switch.

Table 4.3 Comparison of parameters with reported methods in previous literature showing superior performance of the proposed structure

Technique	**BER**	P_r **(dBm)**	**OSNR (dB)**	**ER (dB)**	T_s **(ns)**	**PP (dB)**
Singh et al. [139]	10^{-11}	10-12	-	-	-	-
Cheng et al. [54]	-	-	-	-	3	0.18-0.39
Prifti et al. [142]	10^{-11}	-	-	-	-	< 1
Mao et al. [143]	10^{-9}	-	17	-	-	< 3.4
Xue et al. [144]	10^{-9}	-	-	-	43.4	0.5
Terzenidis et al. [94]	10^{-9}	-	-	-	610	2.19
Jia et al. [145]	-	-	13-18	17.7	-	-
Implemented 8×8	10^{-16}	11-13	21.186	19.99	0.333	0.15-0.30

The values in above Table 4.3 compares the values of BER, received power 'P_r', OSNR, ER, latency in terms of switching time 'T_s', and power penalty i.e. 'PP' with the values reported in previous literature. The proposed structure obtains a BER of 10^{-16} and output power ranging between 11-13 dBm with small input powers among the eight ports which shows error free operations. The high OSNR value of 21.186 dB and good ER value of 19.99 dB shows the efficient performance of the structure with low noise content whereas the low latency of 0.333 ns stands a proof of fast response of the system. The structure also offers a low power penalty of 0.15-0.30 dB giving power efficient operation.

4.4 Conclusion

In this chapter, the scalability of the previously implemented 4×4 configuration is increased by increasing the port-radix to 8×8. This interconnected switching structure utilized TWSOA-SMZI loops for switching the data to the desired destination. To offer the structure a power efficient error-free response, the analysis of performance is done at various stages, ports, and injection

currents. Due to the utilization of TWSOA, the structure can give high output power maintaining the final signal strength. The power analysis is done at all different stages showing consistent results and hence showing reliable performance. The wide opening of an eye with an eye-height of 0.035166 au and EOF of 92.5% shows error-free operation. The error content is also evaluated utilizing the BER parameter which comes out to be 10^{-16}. The investigation shows the high-quality factor even at high values of input power. The improved values of ER from 14.3 dB to 19.99 dB with the surge in power at input from-5 dBm to 5 dBm show the structure is adaptable to high-power operations. The superiority is proved by utilizing latency results in terms of switching time i.e. 0.333 ns and high OSNR of 21.186 dB. It shows the structure is reliable even with the increase in complexity with the switching stages and is adaptable to high-power operations occurring in high-performance computing applications. The structure is also tested at different injection currents of TWSOA. The stage-wise comparison of performance parameters and final comparison with existing literature shows the designed structure can handle the surge in traffic by offering scalability feasibility and also capable to adapt the high input power operation.

CHAPTER 5

NON-LINEAR ANALYSIS IN THE PROPOSED CONFIGURATION

5.1 Introduction

Although the non-linearities of semiconductor optical amplifiers presented in previous chapters 3 and 4 are appreciated as they take part in the switching of data, the in-built non-linear effects can also leave a degrading impression on the output signal. The well-known non-linearity of TWSOA which always alter the reception is polarization sensitivity. Whereas the large intensity signals propagating through cross-bar structure with low port spacing can suffer modifications in the medium's refractive index [146-147] and hence disturbing the performance. The cross-bar arrangements of switches where each port is interconnected with the output port face high chances of crosstalk.

This chapter is divided into two sections where the non-linear effects i.e. crosstalk and polarization sensitivity of TWSOA are investigated respectively. In the first section, the analytical modelling of non-linear crosstalk is done for the cross-bar switching operation of the proposed 4×4 arrangement shown in chapter 3. The effect of the length of the input sequence on crosstalk is discussed. The appearance of high logic at alternative and consecutive places in bit sequence is investigated for cross-state operation and switch performance is evaluated based on other parameters like BER, ER, and input power. In the later section, the polarization sensitivity of TWSOA effecting the output of signal has conversed and an improvement in the proposed 8×8 structure presented in chapter 4 is achieved by the addition of Erbium Doped Fiber Amplifier (EDFA). The middle stage loops in an 8×8 structure utilize EDFA-SMZI and the first and last stage employs TWSOA-SMZI. The proposed S-E-S arrangement is evaluated on the polarization sensitive factors i.e. Stokes parameters and Poincaré sphere. The improved structure proves to be better than the basic TWSOA-SMZI structure by realizing small values of polarization dependent loss (PDL), improved ER, low BER, and good conversion efficiency.

5.2 Analytical modelling for Non-Linear Crosstalk

The cross-phase modulation is a non-linear effect of TWSOA where one wavelength can affect the phase of the signal at another wavelength. The binary '0' and '1' logics occurring in input

sequences can further increase the transmission errors [148] where the average of power of '1' logic can be affected by XPM. Since, the proposed theory is about cross-bar operations occurring in interconnected switching structures, the study of crosstalk w.r.t. input sequence becomes significant. Various theoretical analysis based on the XPM switching effect [149-150,130] and crosstalk in carbon nano tubes [151], ternary logic [152] has been reported but in-built non-linear analysis w.r.t. input bit sequence in optical interconnects has not been presented before.

The final power 'P_f' at the output of TWSOA is derived by considering the refractive index of the medium and net gain with coefficient 'G_N' with input power 'P_{in}' and can be approximated by equation 5.1 [194]:

$$P_f = P_{in}\, e^{G_N C_L} \tag{5.1}$$

This net gain is further dependent on the loss coefficient 'C_L', optical confinement factor 'C_o', and material gain 'G_{mat}' as equation 5.2 [194]:

$$G_N = C_o\, G_{mat} - C_L \tag{5.2}$$

Putting net gain in equation 5.1, we get:

$$P_f = P_{in}\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} \tag{5.3}$$

For a large number of channels in a system, the saturation of this gain occurring in the final play a significant role to add inter-channel crosstalk. If we consider there exist only two input ports with power 'P_{in_1}' and 'P_{in_2}' in an interconnecting loop, the propagation of signals in SMZI arms with the control signal can alter the final output to '$P_f(t)$', the output can change to equation 5.4:

$$P_f(t) = P_{in_1}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + P_{i_2}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + P_{control} \tag{5.4}$$

Further making the second assumption of no external interference occurring due to control signal on phase i.e. 'φ_{in_1}' and 'φ_{in_2}' and frequencies i.e. 'ω_{in_1}' and 'ω_{in_2}' of inputs propagating in the loop, the approximation of final optical field '$E_f(t)$' at the optical receiver can be given by equation 5.5:

$$E_f(t) = \sqrt{2P_{in_1}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2}}\cos(\omega_{in_1} + \varphi_{in_1}) + \sqrt{2P_{control}(t)} + \sqrt{2P_{in_2}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2}}\cos(\omega_{in_2} + \varphi_{in_2}) \tag{5.5}$$

Making the third assumption that worst case polarization is occurring between cross-port signals of MZI arms, 'η_q'as quantum efficiency, 'q' as a charge on an electron, and 'hν' a photon energy,

then the photonic current in respect of input signal energy can be approximated by utilizing square law detection as shown by equation 5.6:

$$i_p(t) = \frac{\eta_q q}{h\nu} \overline{(E_{\imath n_1}(t) + E_{\imath n_2}(t))^2} \tag{5.6}$$

$$= \frac{\eta_q q}{h\nu} (\overline{[E_{\imath n_1}(t)^2] + [E_{\imath n_2}(t)]^2 + 2E_{\imath_{n1}}(t)\, E_{\imath_{n2}}(t)})$$

Replacing equation 5.5 in 5.6, the final photon current is equal to equation 5.7:

$$i_p(t) = \left(\frac{\eta_q q}{h\nu}\right) [(\overline{[E_{\imath_{n1}}(t)^2] + 2\sqrt{2P_{\imath n_1}(t)P_{\imath n_2}(t)\left(e^{C_o\, G_{mat}\, C_L - {C_L}^2}\right)^2}} \tag{5.7}$$

$$\overline{cos((\omega_{\imath n_1} - \omega_{\imath n_2})t + \varphi_{\imath_{n1}} - \varphi_{\imath n_2}) + cos((\omega_{\imath_{n1}} + \omega_{\imath n_2})t + \varphi_{\imath n_1} - \varphi_{\imath n_2}) + [E_{\imath n_2}(t)]^2)}]$$

Utilizing time averaging over optical frequencies, the final equation of photonic current given by equation 5.8 is as follows:

$$i_p(t) = \frac{\eta_q q}{h\nu}(P_{i_{n1}}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + P_{i_{n2}}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + \tag{5.8}$$

$$2\sqrt{P_{i_{n1}}(t)P_{i_{n2}}(t)\left(e^{C_o\, G_{mat}\, C_L - {C_L}^2}\right)^2} cos((\omega_{i_{n1}} - \omega_{i_{n2}})t + \varphi_{in_1} - \varphi_{in_2})$$

Although there will not be any beat-frequency component present in the final output because the inter-channel crosstalk interferrence is coming from diverse wavelengths that are generally larger than the bandwidth of LPF, the intra-channel output from the alike sources alters the final current given by equation 5.9:

$$i_p(t) = \frac{\eta_q q}{h\nu}(P_{i_{n1}}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + P_{in_2}(t)\, e^{C_o\, G_{mat}\, C_L - {C_L}^2} + \tag{5.9}$$

$$2\sqrt{P_{in_1}(t)P_{in_2}(t)\left(e^{C_o\, G_{mat}\, C_L - {C_L}^2}\right)^2} cos(\varphi_{i_{n1}} - \varphi_{in_2})$$

From the above analysis, it can be concluded that if input ports are further increased from two to four, the final output of the system will observe worse effects. To monitor such spikes and noise arising in the output because of crosstalk, the power meters along with power spectrum analyzers are employed.

5.3 TWSOA-SMZI Switch Setup for Evaluating Non-Linear Crosstalk

The setup for evaluating the non-linear crosstalk in the proposed 4×4 interconnected switching configuration is illustrated in Fig. 5.1. to achieve the effect of random sequence coming from input ports, the Pseudo-Random Bit Sequence (PRBS) generator is first utilized that generates the input

sequence of length equal to multiplication of data rate and timing window declared globally for simulation. The PRBS generator further subtracts the number of leading and trailing zeros from the length of the sequence to generate the final input sequence. This PRBS process is followed by the pre-coding procedure that includes the On-Off Keying (OOK) Non-Return-to-Zero (NRZ) gaussian pulse generation. This coded sequence is influenced by the control signal coming from the continuous-wave (CW) because they have better efficiency than other lasers as they produce continuous high powers with a non-degrading average.

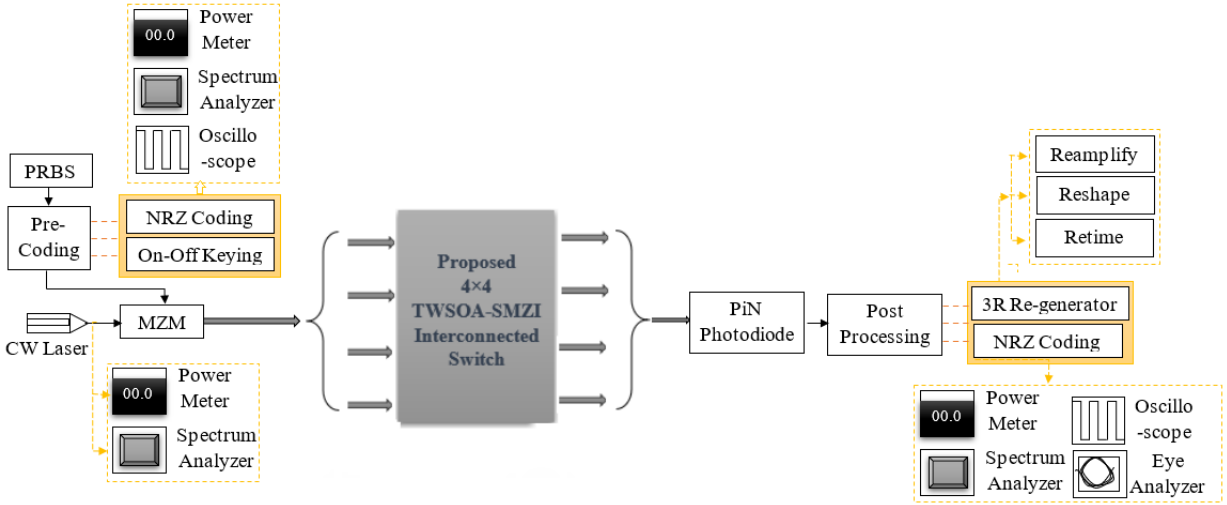


Fig. 5.1 Setup for monitoring the crosstalk in the proposed 4×4 switch configuration

The Mach Zehnder Modulator (MZM) helps in controlling the amplitude of the signal coming from the inputs. This further splits the signal symmetrically in MZI arms. At the receiver end, the PiN detector is utilized because its large depletion area provides a fast response. This detection process can be followed by post processing including 3R regeneration i.e. reshaping, retiming, and reamplifying if required for recovering the corrupted bits. The last conversion required to create of the same NRZ-coded pulse to monitor the received eye patterns.

5.4 All-port Parametric Evaluation at Bar and Cross-State

1. Evaluation at Bar-State: The noise existing in the received signal is evaluated with the help of an eye-analyzer. The wider the opening of the eye i.e. larger the EOF, the lower the noise. The performance is checked at the first bar state to observe the difference in performance when the interconnected structure actually runs for cross-ports. The results show 96% EOF on average at each port, and the quality factor also remains consistent near 27. The crosstalk measurement is

done utilizing a power meter which comes out to be -30 dB on average. The lower values of BER of 10^{-17} are observed at a bar state operation. The exact parametric values for each port of the proposed configuration operating in a bar state can be observed in Table 5.1 below.

Table 5.1: Bar-state analysis of 4×4 proposed switching structure

BAR STATE PARAMETERS			
Ports	**EOF (%)**	**Max. QF**	**CT (dB)**
Port 1	96.3892	27.7175	-30.1350
Port 2	96.4167	27.8131	-30.4148
Port 3	96.3815	27.7450	-30.1507
Port 4	96.2525	26.7239	-29.550

The measurement of crosstalk at output port 1 is done by keeping other ports other than port 1 inactive for bar state. Whereas for cross-state if the data is coming from port 2 then inputs ports other than port 2 should be inactive [148] while measuring the reading from the power meter. Mathematically, for a two-port system, if 'P_{I_1}', 'P_{I_2}', 'P_{O_1}', 'P_{O_2}' the crosstalk is illustrated in equation 5.10 [148]:

$$CT = \frac{P_{O_2}\left(P_{I_{1=\text{ACTIVE}}}\right) - P_{O_2}\left(P_{I_{1=\text{INACTIVE}}}\right)}{P_{O_2}\left(P_{I_{1=\text{INACTIVE}}}\right)} \quad 5.10$$

2. Evaluation at Cross-State: The next evaluation is done at the cross-state operation where lower values of BER are observed as 10^{-16} with port-average values of EOF as 96%, and QF of 27 and final Crosstalk of -30 dB is achieved. The exact parametric values for each port of the proposed configuration operating in a cross state can be observed in Table 5.2 below.

Table 5.2: Cross-state analysis of 4×4 proposed switching structure

CROSS STATE PARAMETERS			
Ports	**EOF (%)**	**Max. QF**	**CT (dB)**
Port 1	96.3915	27.6946	-30.1359
Port 2	96.4045	27.9074	-30.4132
Port 3	96.3957	27.6358	-30.1747
Port 4	96.2581	26.6844	-29.9532

The parametric values reported in the above two tables at both bar and cross-states stand as proof that phase alterations occurring in SMZI arms for creating a switching effect are not disturbing the overall performance of the system. Hence, the arrangement can be further tested for observing crosstalk vs input sequence effects in a system.

5.5 Crosstalk Analysis with Bit Sequence

5.5.1 Effect with Increasing Number of 'High' Logic

This effect of bit sequence is observed using the User Defined Bit Sequence (UDBS) generator in place of PRBS to observe the modifications in crosstalk done by the varying number of ones in the input sequence with a total length of 10-bits. The performance is measured in terms of BER and crosstalk. It can be seen from Fig. 5.2 that the BER degrades from 10^{-19} to 10^{-17} when the number of 'high' logics in an input sequence surges from 1 to 10.

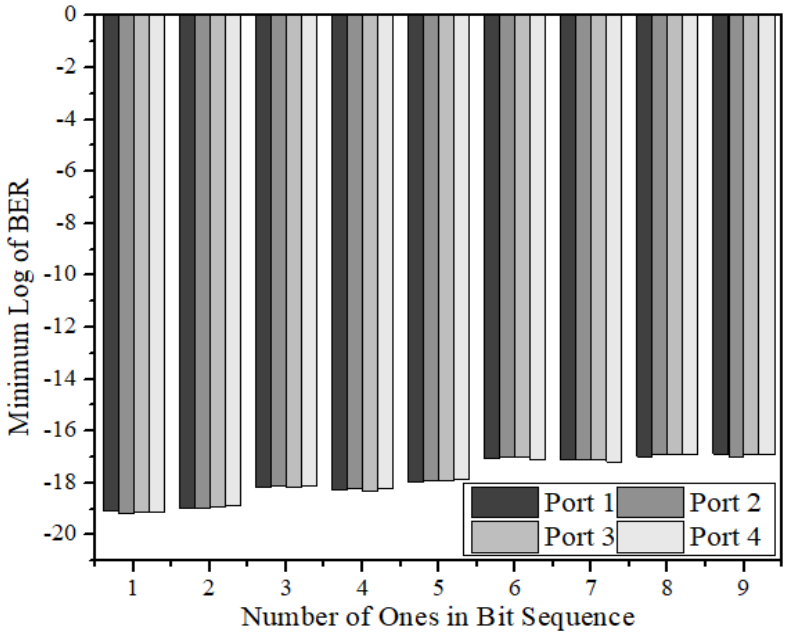


Fig. 5.2 Effect of the number of 'High' logics appearing in Bit sequence on BER

XPM effects occurring inside the SMZI loops are able to disturb the average power of 'high' logic that further modifies the switched bits coming from either that bar or cross ports. This makes the input sequence and its order during transmission and the number of zeros and ones present in that sequence more significant as it decides the final performance of the system. A similar fashion as in Fig. 5.2 is observed in Fig. 5.3 for crosstalk that also degrades from -50.13 dB to -25.3 dB.

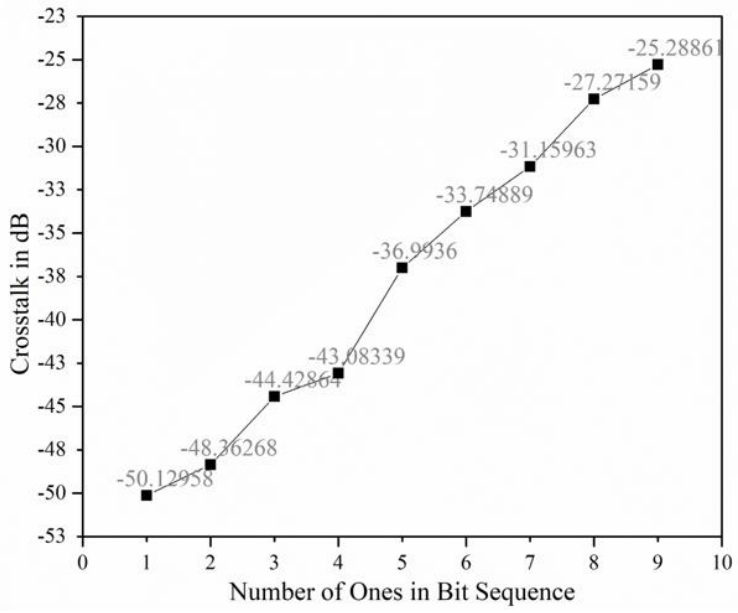


Fig. 5.3 Effect of the number of 'High' logics appearing in Bit sequence on Crosstalk

5.5.2 'High' Logic Appearance at Consecutive and Alternate Places

The next analysis is to observe how the appearance of 'high' logic in certain places can affect the output of the signal. This monitoring of performance is done utilizing BER, ER, and crosstalk. The TWSOA's anti-reflective cavity is less sensitive to polarization [28,153] which leads to a smooth gain spectrum. This property in TWSOA saves the fluctuations occurring in the output signal due to 'high' logic appearing at either consecutive or alternative places in a bit sequence. It can observe from Fig. 5.4 (a) and (b) that the performance results for the consecutive and alternative appearances of '1' are almost similar but a significant effect can be seen when the number of ones increases in the input sequence.

The results in Fig. 5.4 (a) show BER ranges between the value 10^{-14} to 10^{-16} and around 10^{-17} for the consecutive and alternative appearance of ones respectively. The degradation in ER can be observed in Fig. 5.4 (b) with the surge in several 'high' logics in the input sequence. The ER value lowered from 18.3 dB and 18.285 dB consecutive and alternate appearance of ones in sequence to 10.1065 dB and 11.6082 dB respectively. The large fall is seen due to the MZI structure in switching loops giving the large phase shifts above a certain threshold level. The impairment can be easily solved as it is observed from the results given in chapter 4 that choosing optimized values of injection current can improve the extinction ratio of TWSOA-based structures.

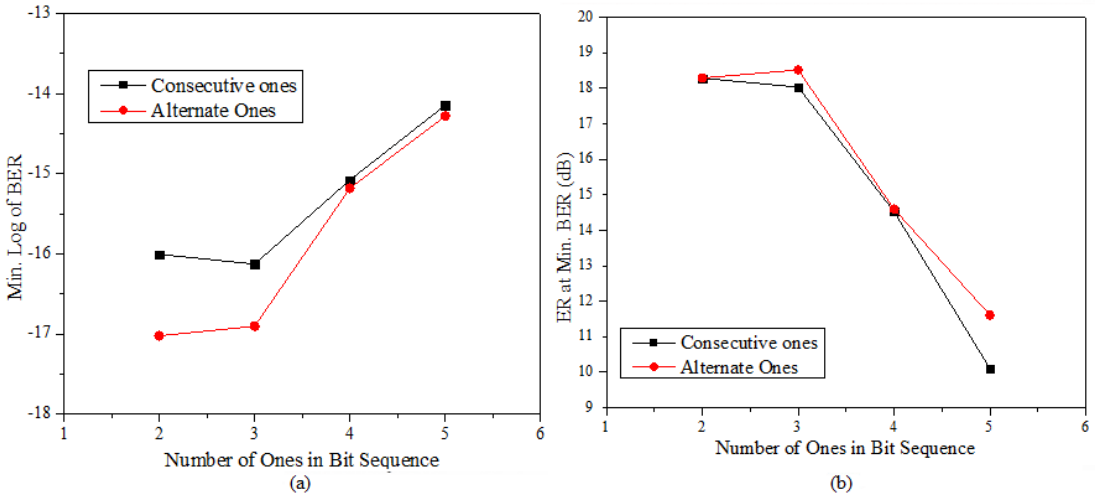


Fig. 5.4 Effect of number of ones appearing in consecutive and alternate places on (a) BER (b) Crosstalk

The crosstalk monitoring is also done for similar conditions of a number of ones in Fig. 5.5. It is observed that crosstalk can degrade from -37.7 dB and -39.2326 dB to -31.6932 dB and -31.8208 dB for the consecutive and alternative appearance of ones in an input sequence respectively.

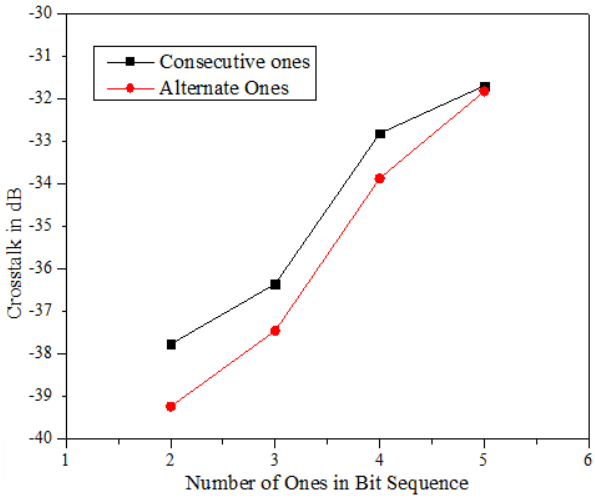


Fig. 5.5 Effect of the number of ones appearing in consecutive and alternate places on ER

5.5.3 Port-wise Crosstalk Analysis and Comparison

The non-linear crosstalk has been analyzed with the increasing length of the input bit sequence. The implmented crosstalk results are presented in the following Fig. 5.6 for each port when the length of the input sequence is varied from 7-bits to 14-bits. It can be observed that the crosstalk of -39.5 dB has been achieved when the sequence length is 7-bits. The further increase in sequence

length further degrades the crosstalk and a value of -21.5 dB can be achieved for a 14-bit sequence length which is also acceptable for switching of input data.

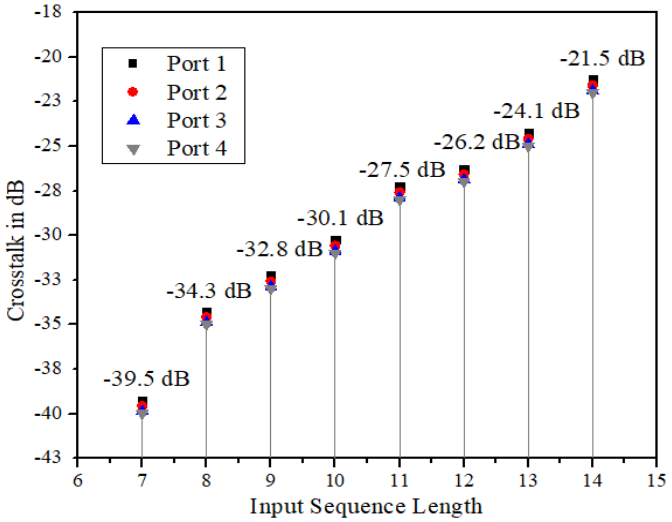


Fig. 5.6 Port-wise Crosstalk evaluation vs Input Sequence Length

It is observed that the crosstalk of -34.4 dB is achieved for minimum input power of -10 dB. The results are evaluated by varying the input power from -10 dBm to +10 dBm. The crosstalk values in Fig. 5.7 show that the proposed configuration is able to give good crosstalk of -27.8 dB for the increased input power of 10 dBm for cross-state operation.

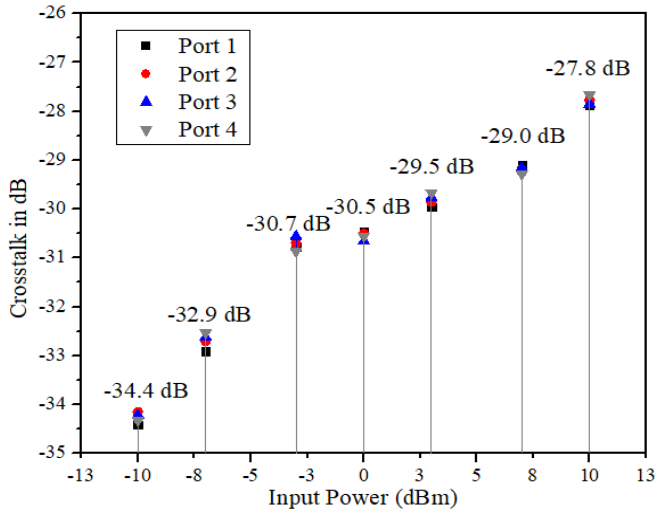


Fig. 5.7 Port-wise Crosstalk evaluation vs Input Power

The results for crosstalk shown in Table 5.3 are compared with previously reported techniques. It can be observed that the implemented crosstalk varies between -29.5 dB to -30.4 dB in all four ports at both bar and cross-state operation. Hence the crosstalk of the proposed configuration is -

30 dB on average for four ports which is far better than the crosstalk reported by Prince et al. [154] which is -25 dB and by Jeong et al. [155] which showed -20 dB of crosstalk.

Table 5.3: Crosstalk comparison of proposed switching structure with existing techniques

Techniques	**Crosstalk**
Prince et al. (2021) [154]	-25 dB
Jeong et al. (2022) [155]	-20 dB
Implemented	**-30 dB**

Hence, the comparative results prove that instead of being a cross-bar switching interconnect, the structure can achieve better performance in terms of BER, ER, and crosstalk. It is also observed that ER reduces with the consecutive appearance of '1's, it is recommended to the alternative '1's pattern can act as a fast trigger for recognizable switching. On the other hand, if the bit sequence is long enough for more switching stages, then error bits increase in output making less differentiating and requiring 3R.

5.6 Polarization Non-Linearity Effect in SOA and Significant Factors

The second non-linear evaluation is done utilizing the polarization sensitivity property of TWSOA in the proposed configuration keeping the port spacing as minimum as possible. Since the polarization sensitivity of SOA can help achieve switching and gating actions in certain structures as reported by various researchers in [156,158-159], but it also reported that unsaturated gain [160-161] of SOA, output power [162] can also be dependent on different polarization states. This leads to low latencies, higher penalties, and lower conversion efficiencies. The results obtained from the MZI structures are only reliable if the polarization dependency is not considered [163, 146] for evaluation. The proposed structure utilizing only TWSOA-SMZI loops is tested for polarization sensitivity and it is concluded that there is an area of improvement to minimize the output dependency on polarization states that effect the significance of the signal.

5.6.1 Stokes Parameters

When the signal enters TWSOA-SMZI, the birefringence effect of TWSOA alters the phase of TE and TM modes occurring in the signal and hence creating the polarization states. Since the waves are expressed as EM-components along the semi-minor and semi-major axis, the final

representation of this output wave is plotted on an ellipse to form an ellipse equation at the output. This equation will have ordinary and extra-ordinary waves i.e. have azimuth and ellipticity components. These components of the final output are also expressed as real quantities called Stokes parameters [162]. These are: S_0 shows the original signal intensity; S_1 shows the distinction between vertical and horizontal components of the intensity signal which is linearly polarized; S_2 differentiate between signal intensities which are linearly polarized 45^o and -45^o; and S_3 differentiate between right and left circularly polarized intensities.

5.6.2 Poincaré Sphere

The polarization states are represented on a sphere called the Poincaré sphere is advantageous. It tells the difference between totally polarized and partially polarized waves by representing the points 'on' the sphere and 'within' the sphere respectively [162]. A large number of points gathered on this sphere shows the effect of polarization states and intensity distribution in the output.

5.7 Proposed S-E-S Structure to Mitigate Polarization Effect

It is observed that utilization of a hybrid optical amplifier combination of TWSOA-EDFA for achieving switching operations removes various obstacles that can't be removed by basic TWSOA-based configurations like mitigating polarization effects and achieving low latency in 8-port interconnections. Hence, creating the self-switching effect in the configuration, the EDFA is utilized in the middle stage of an 8×8 interconnected structure that realizes high OSNR values, with low polarization dependent loss (PDL), good conversion efficiency, and fast response.

In the proposed 8×8 interconnected switching structure shown in Fig. 4.1, the first and third stages where made from 2×2 TWSOA-SMZI loops and the middle stage consists of the proposed 4×4 interconnection shown in Fig. 3.6 made by three-stages of TWSOA-SMZI. For the polarization sensitivity measurement, the circulator, Linear Polarizers (LP), and polarization controllers have been utilized. The middle stage in the 8×8 configuration is proposed to change from the TWSOA-SMZI combination to the EDFA-SMZI loop to minimize the polarization effects occurring in the complex arrangement. The switch is designed to operate at a 10 Gbps bit rate and the port spacing is defined at 100 GHz. The polarization meter and polarization analyzers help to observe the polarization states, stokes parameters, and Poincaré sphere distribution. The 2×2 switching loop

is designed as shown in Fig. 5.8 where the TWSOA components are replaced by EDFA for the middle stage in proposed 8×8 configurations.

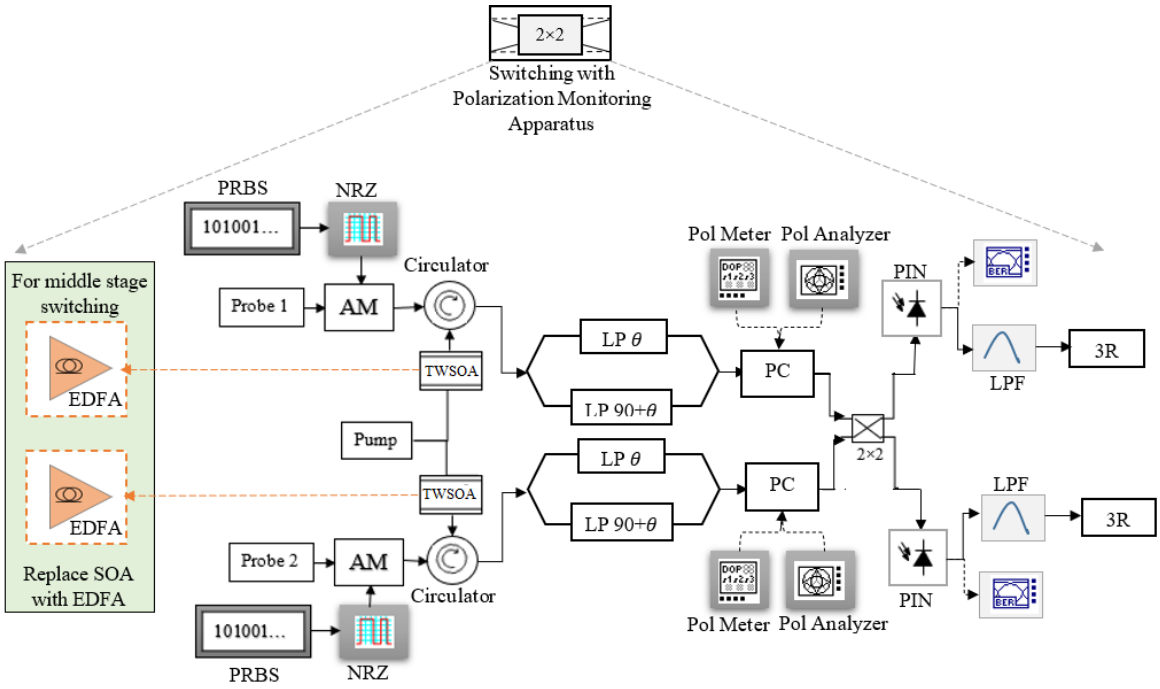


Fig. 5.8 Self-switching 2×2 arrangement monitoring polarization in 8×8 interconnection

The input of circulators is the intensity-modulated NRZ coded probe signal whereas the pump through SOA also meets from the other end of the circulator. The performance monitoring is done for various input powers with a wide range from -10 dBm to 10 dBm. The TWSOA and EDFA for the switching stages suffer the carrier density changes because of the pump signal flowing from the circulator fed symmetrically to MZI arms. This causes alterations in the refractive index and leads to phase changes in the arms. If it tends to have further refractive index variations, then it leads to the rotation of the signal coming from Port 1 and port 2 to the desired destination. The external bias voltage to the TWSOA at stage 1 and 3 also lead to an electro-optic effect causing the formation of destructive and constructive interference. For stages 1 and 3, the loops utilize polarization sensitive signals with small values of injection current and for the middle stage, the EDFA-based MZI loops are utilized that have large gain values, no polarization dependency, and low noise that helps in mitigating the negative effects of basic TWSOA-MZI based structure. The Polarization Controller (PC) at the end controls the state of polarization by setting the signal with a random polarization state. The final controlled signal is achieved depending upon the splitting ratio and difference of phase between E_x & E_y.

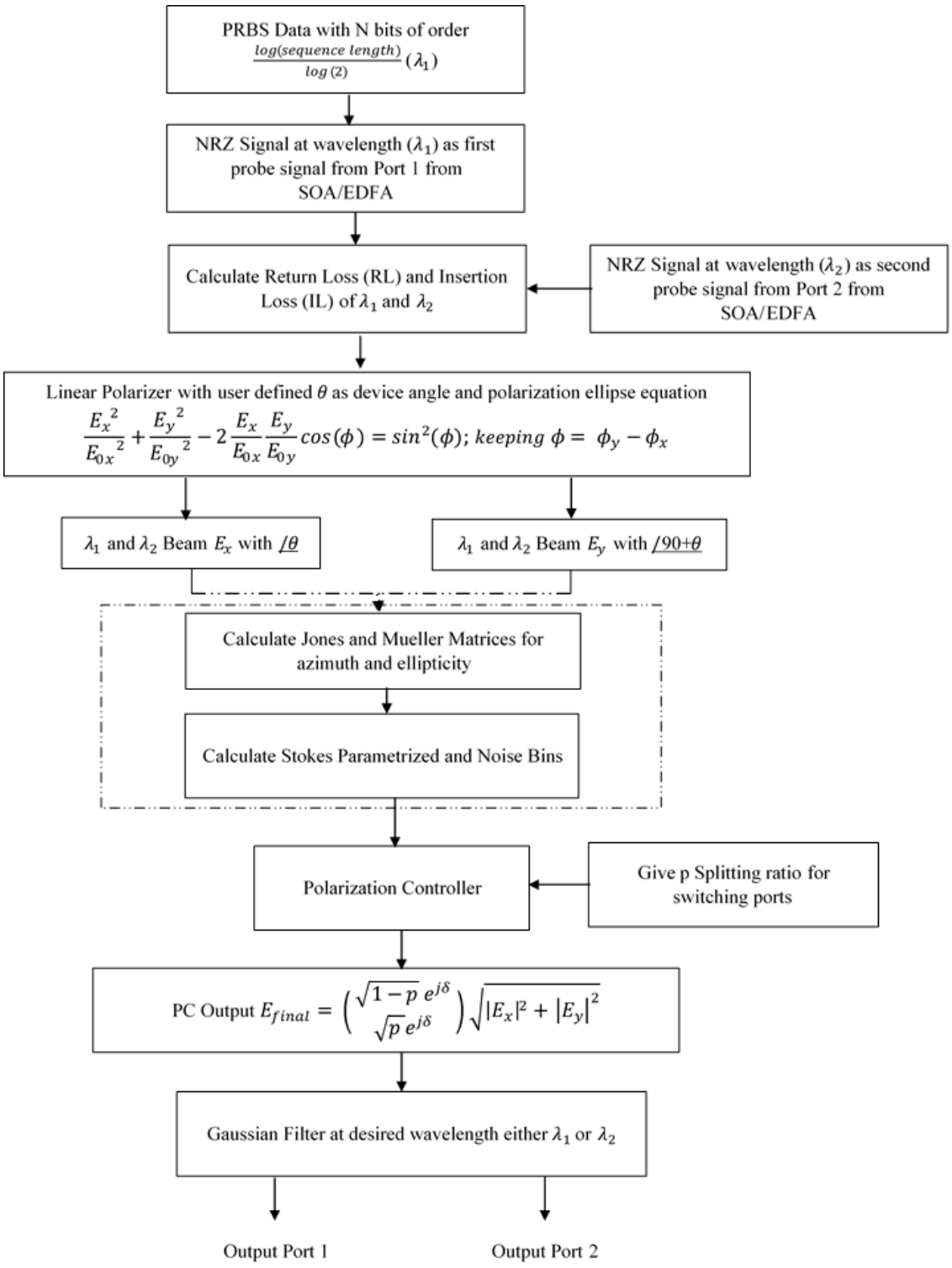


Fig. 5.9 Flow chart of proposed self-switching structure. (p: splitting ratio for PC; E_x & E_y: components of Electric field in x and y axis; δ: Phase difference; E_{0x} & E_{0y}: real amplitudes of E_x & E_y; ; ϕ_x & ϕ_y: phases along the x and y axis)

The exact flow of the signal is properly indicated by the flowchart shown in Fig. 5.9 where the 'N' number of bits are generated from the PRBS generator that is NRZ encoded. The symmetric pump signal and data from two ports meet the circulators that decide the device angle 'θ' and calculation of return loss and insertion loss is done to see the final loss in the output signal. The signal then gets split by the linear polarizers (LP) attached to the MZI arm in the 'θ' and 'θ+90' depending on the device angle. This splits the beam into the ordinary and extra-ordinary forms along the 'x' and 'y' axis as 'E_x' and 'E_y' electric field components respectively. From this, Jones and Muller's matrices decide the final transfer function of polarization. The E_x & E_y components are approximated by Maxwell equations from which the final polarization ellipse equation is obtained as shown in the forth block of the flow chart shown Fig. 5.9. The azimuth and ellipticity so obtained from the ellipse equation can now be represented as Stokes parameters. According to the phase and splitting ratio of PC, the final output is fed to the destination port that is filtered at desired wavelength by gaussian LPF.

5.8 Results and Analysis

1. Stokes Parameters: Firstly, the Stokes parameters for TWSOA and EDFA loops are compared to observe the polarization effect on the final output. The device angle is set at 45^o for azimuth rotation but it can be noticed from Fig. 5.10 that the loops made with TWSOA have ellipticity effected by the introduction of azimuth because of its sensitivity to polarization and further running the intensity of output signal. Whereas, EDFA loops have only azimuth rotation as set by the user and zero ellipticity. This shows that the introduction of EDFA in the middle can stop the polarization affecting the output.

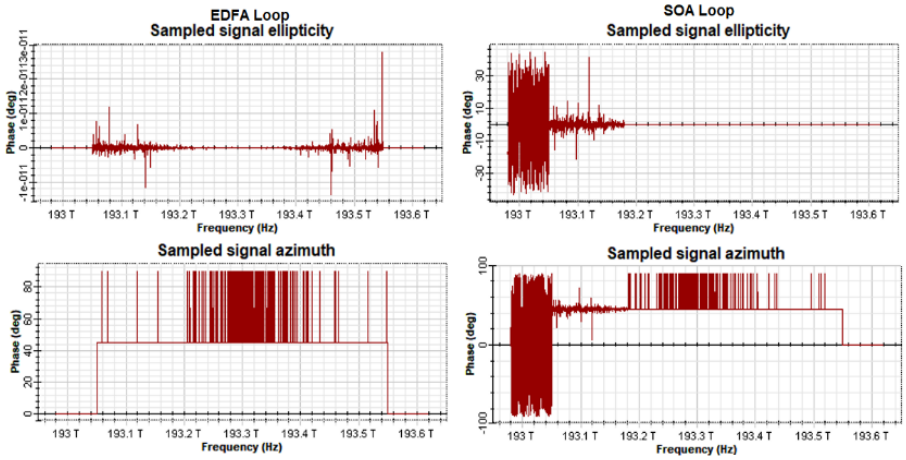


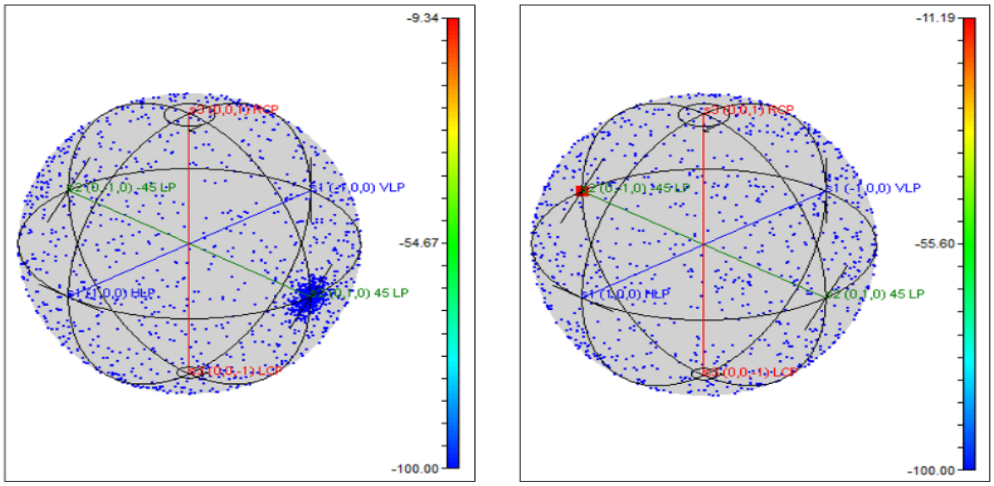
Fig. 5.10 Comparison of Ellipticity and Azimuth State for EDFA and TWSOA Loops

There exist various other parameters that decide the performance based on the Stokes theory. Table 5.3 below shows the variation in the TWSOA and EDFA loops where the exact azimuth rotation in EDFA loops is 45^{o} but for TWSOA the azimuth rotation is disturbed to 44.94^{o}. Since there was no initial ellipticity, the EDFA ellipticity parameters are valued at zero but TWSOA shows variations that disturb the final output. A similar fashion can be observed for S1 and S3.

Table 5.4: Stokes Parameters Comparison of TWSOA and EDFA loops

Parameters →	**S0 (dBm)**	**S1**	**S2**	**S3**	**Azimuth**	**Ellipticity**
EDFA	-100	0	1	0	45	0
TWSOA	-100	0.00209	1	-0.00062	43.1325	0.01038

2. Poincaré Sphere: The next observation is made on Poincaré Sphere in 3D space by representing Stokes parameters i.e. 'S_0', 'S_1', 'S_2', and 'S_3' on this sphere. It is seen in Fig. 5.11 (a) that points (0,1,0) have a large number of distributed points, unlike EDFA-based loops in Fig. 5.11 (b). which is caused by TWSOA's irregular azimuth and ellipticity rotation further creating LP states to breakdown at a single point. These spatially distributed points can be taken as a polarization dependency of the output signal in the TWSOA loop.



(a) (b)

Fig. 5.11 Poincaré Sphere Representation for (a) TWSOA-loop (b) EDFA-loop

Hence, introducing an SOA-EDFA-SOA or (S-E-S) hybrid combination of amplifiers, where SOA has TW configuration, for creating three stages of the proposed 8×8 switching configuration can help compensate polarization effects on the output signal.

3. Performance based on BER and ER: The major performance testing is based on BER and ER as the proposed configuration has three stages in which the signal suffers numerous noise and polarization effects during its propagation from input to output ports. Both of these parameters are monitored with varying input power. The observations from Fig. 5.12 (a) are clear that the proposed S-E-S structure proves better than the basic SOA-MZI configuration. The BER for the S-E-S structure stands at 10^{-16} at max where as it is 10^{-14} for the basic SOA-MZI loop.

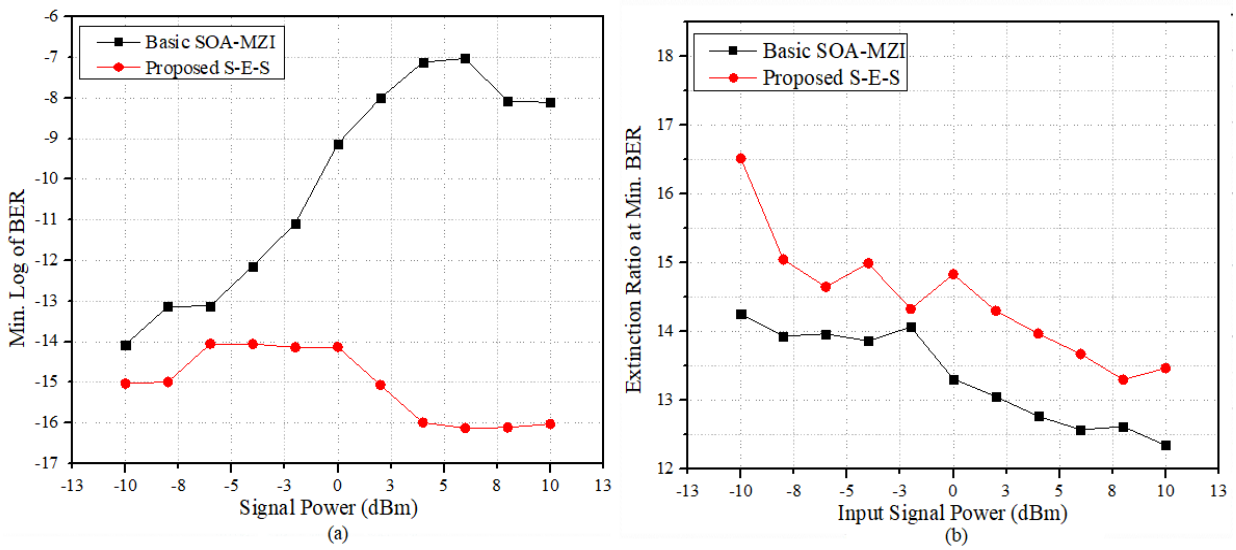


Fig. 5.12 SOA-MZI and S-E-S Comparison results for (a) BER (b) ER with varying input power

Similarly, ER at minimum BER is measured for both configurations. The maximum ER value is 14.5 and 17 dB for basic SOA-MZI and S-E-S structures. The proposed improvement in structure with hybrid optical amplifiers proof to be efficient and better than the basic switching arrangement.

4. Conversion Efficiency (CE): The measurement of CE is done w.r.t. spacing between the ports. If the power of the output port is 'P_o' and for the cross-port, the power is measured as 'P_x', then according to the formula reported in [156-157], the CE can be evaluated by following equation 5.11:

$$\mathrm{CE} = 10\, log\, (\frac{P_o}{P_x}) \qquad 5.11$$

According to the research in [156], due to TWSOA's non-linear and low frequency operation, the CE value is always expected to decrease with an increase in spacing between the propagating

channels. It is observed from Fig. 5.13 that for port spacing varying between 0.1-0.8 THz, the CE value is decreased from -7.51 to -27.13 dB.

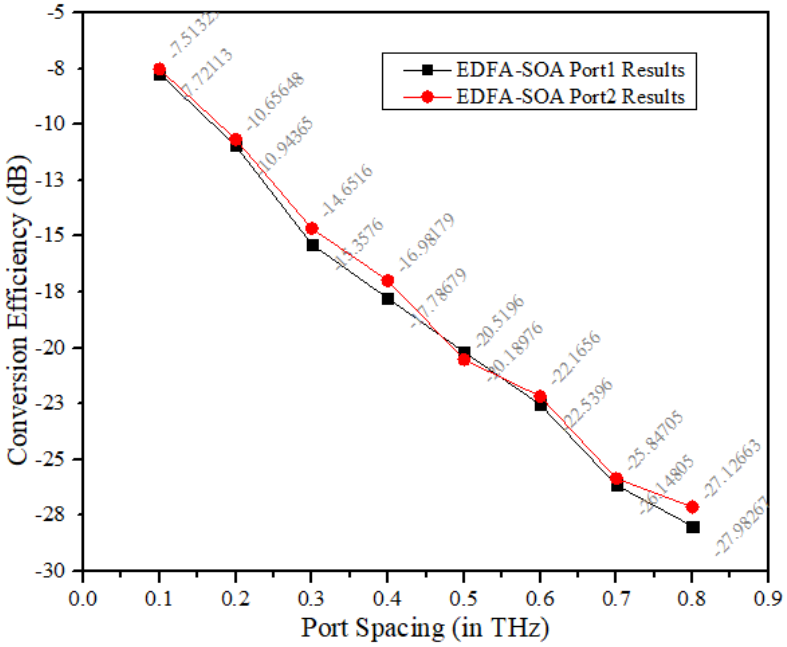


Fig. 5.13 Results of Conversion efficiency in dB vs port spacing in THz

5. Polarization Dependent Loss (PDL): PDL is evaluated by the comparative difference between the minimum and maximum intensity loss i.e. '$I_{L_{min}}$' and '$I_{L_{max}}$' suffered by a component in various polarization states as illustrated in equation 5.12 [163]:

$$PDL = \frac{I_{L_{max}}}{I_{L_{min}}} \qquad 5.12$$

The PDL for the implemented structure is 1.004 dB which proves better than the previously reported high value of 1.6 dB [165]. This proves that utilization of EDFA in the middle switching stage helps in compensating for the losses that occur owing to the polarization sensitivity of TWSOA.

6. Comparison with previously reported results: The proposed configuration is tested by varying injection current and varying OSNR of the system to check the received BER for each case and the results are compared with previous SOA-MZI and other literature work. It is observed in Fig. 5.14 (a) that for the injection currents varying between 0.15 A and 0.45 A, the BER results of basic TWSOA-SMZI configuration gets improved from 10^{-4} to 10^{-14} and 10^{-4} to 10^{-13} for Port 1 and Port 2 respectively. On the other hand, the proposed S-E-S structure yields the BER of 10^{-10} and

improves to 10^{-15} for both Port 1 and Port 2 respectively. The improved maximum values are obtained for the injection current of 0.35 A.

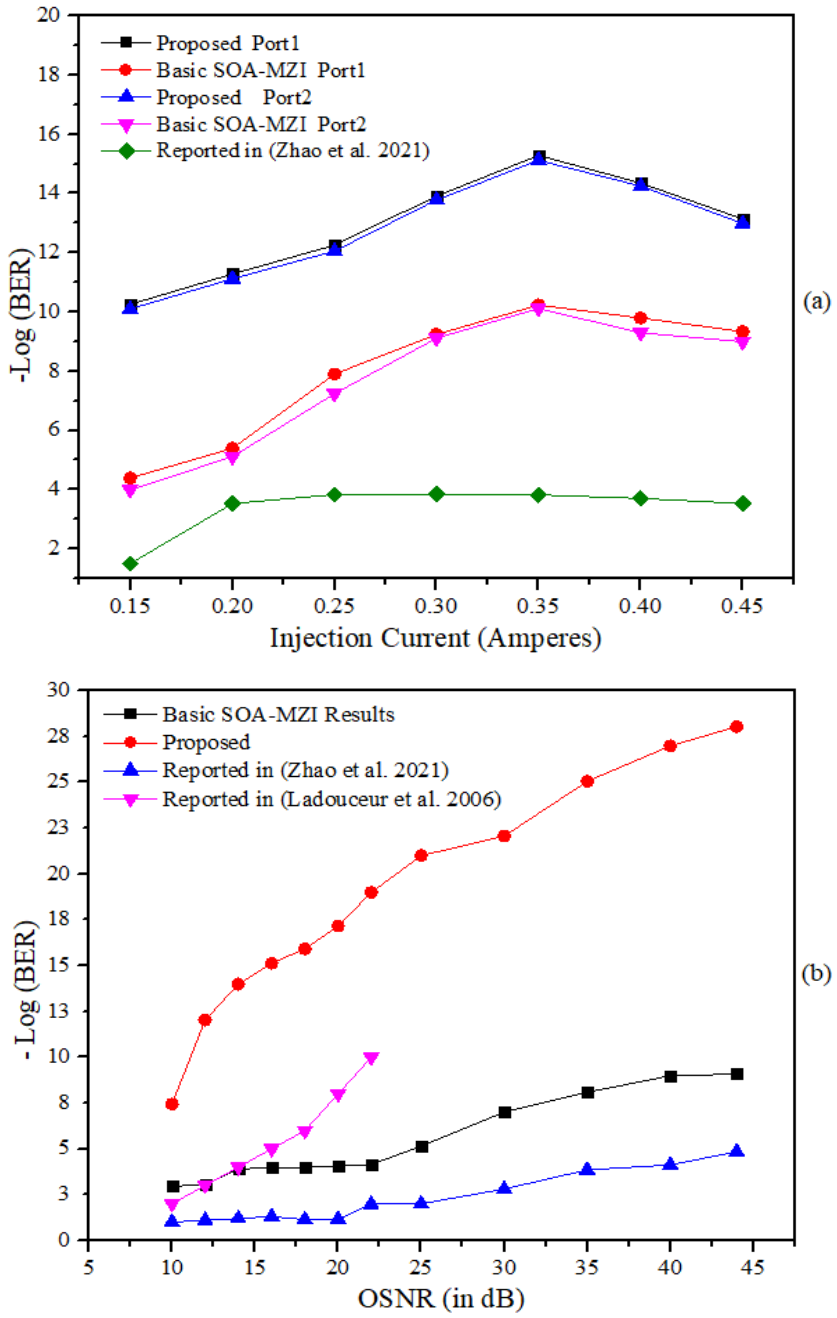


Fig. 5.14 Comparison of BER at Port 1 and Port 2 with previous literature in [159,166] w.r.t. (a) injection current (b) user-defined OSNR *(Data in [166] is only available for OSNR 10-24 dB)*

These results are also compared with the techniques shown in [159] that have a minimum BER of 10^{-1} and a maximum improvement of 10^{-4} only. The increasing and decreasing fashion of BER

with injection current is due to alteration of FWM i.e. four-wave mixing effect of TWSOA the variation of injection current [159]. This comparison shows the new arrangement offers error-free operation when the polarization sensitivity is taken into the picture.

The comparison in Fig. 5.14 (b) shows the BER of 10^{-28} can be realized user-defined OSNR and 10^{-15} is achieved for 0.35 A of injection current. This range in switches with basic TWSOA shows the variation from 10^{-3} to 10^{-9} whereas the proposed realizes the range of 10^{-7}-10^{-28} by putting the system through user-defined OSNR of range 10-44 dB. It can be concluded in Fig. 5.14 (b) that the S-E-S arrangement provides promising efficient operation when compared with the TWSOA-SMZI switching configuration.

5.9 Conclusion

In this chapter, two types of non-linearities i.e. crosstalk and polarization sensitivity of TWSOA has been studied and these results are divided into two respective sections.

Firstly, the non-linear crosstalk is modelled for TWSOA to observe the effect on output power in interconnected structures. This modelling is further analyzed for interpreting the effect of a number of '1's appearing in the input sequence and how the alternative and consecutive appearance in the bit sequence effects the output and crosstalk. The structure yields EOF of 96%, QF of 27, and CT of -30 dB an average consistently for both bar and state showing the structure is better for evaluating the crosstalk w.r.t. changing 'high' logic levels in bit sequence using UDBS generator. It is established from the results that '0' and '1' appearing in the sequence disturb the XPM of TWSOA leading to alterations in crosstalk. The performance in terms of QF, BER, and ER also degrades with a surge in '1's occurring in the input sequence. The BER degrades from 10^{-19} to 10^{-17} when the '1's increase from 1 to 10 in bit sequence. Similarly, the crosstalk degrades from -50.13 dB to -25.3 dB. It is observed that ER is extremely affected by '1's appearing on consecutive than alternate places in a bit sequence due to the MZI structure keeps giving the large phase shifts above a certain threshold level. Since ER reduces with the consecutive appearance of '1's, it is recommended to the alternative '1's pattern can act as a fast trigger for recognizable switching. On the other hand, if the bit sequence is long enough for more switching stages, then error bits increase in output making less differentiating and requiring 3R.

Secondly, it is shown that utilization of a hybrid optical amplifier i.e. TWSOA-EDFA for different switching stages in 8×8 helps in mitigating polarization effects. Hence, the new improvement in proposed by utilizing EDFA in the middle stage of an 8×8 interconnected structure that realizes high OSNR values, with low polarization dependent loss (PDL), good conversion efficiency, and fast response. The first and second stage utilizes the TWSOA-SMZI to help in creating the self-switching. This new S-E-S arrangement shows a lower BER of 10^{-16} with ER of 17 dB having a minimum spacing between ports i.e. 0.1-0.8 THz. The results are compared with the basic SOA-MZI switching configuration. The Stokes and Poincaré sphere analysis demonstrates the comparison of the effect of polarization in the TWSOA loop and EDFA loops. This helps in confirming that utilization of EDFA can lower the birefringence effects of TWSOA overall. The good BER reception of 10^{-16}, conversion efficiency of -27.13 dB, and PDL of 1.0045 dB show the superiority of the proposed S-E-S arrangement over the basic TWSOA-SMZI-based switching.

CHAPTER 6

S-E-S SWITCHING STRUCTURE INCORPORATING LSTM NEURAL NETWORK

6.1 Introduction

In this chapter, the second objective of realizing minimum latency with high throughput has been achieved. Switching the signal to an output port and blindly sending it on a particular I/O path that is not available at the moment will only increase or add to the switching time and hence negatively contributes to the latency. Hence, the proposed S-E-S switching configuration shown in chapter 5 is further explored on an innovative level of smart switching for DC applications. In this chapter, firstly the need for a neural network in the proposed switching structure is explained. Firstly, the overview of the neural network and its working is elucidated followed by the discussion of the requirement of Optical Neural Network (ONN) in switching configurations. Out of various existing deep learning models, the best model based on a regression network is chosen for applicability in the present application. The operation analysis of the Long-Short-Term-Memory (LSTM) network and the types of activations required for better prediction is described. Further, the work is divided into two parts where LSTM network-based destination prediction is made without and with port availability information. The training and testing part in both methods is tested on various parameters and a final comparison is made where the structure with LSTM prediction stands more efficient in terms of BER, switching time, and throughput than the structure without LSTM predictions.

6.2 Overview of Neural Networks

The complicated configurations that are handled employing the advantageous approach i.e. Artificial Neural Networks (ANN) proved to be a blessing by providing highly accurate and reliable results. The intensive usage of famous internet platforms has forced organizations to mount enormously large data centers. The various degrading effects of HPC systems in DC configurations can require the monitoring of the performance-impairments that can upgrade and update over time. The gradual learning of such impairments by the machine itself can make the manual process easy and stress less. Thus, the employment of ANN in the processing of such data has become a necessity of time. The ANN has been evolving day by day from machine learning

concepts to deep learning. The applicability of deep learning in the areas like image and video processing, computer vision, audio processing, alter-image, and video forensics [167-168] have proved to be a great boon in the field of medical and health, engineering, defense, and IT.

The elementary level in the ANN network is a small arithmetic computing node called a neuron. This neuron is the replica of a biological neuron. These neurons are further combined in an interconnected structure resembling the working of a biological neural network [169] as shown in Fig. 6.1.

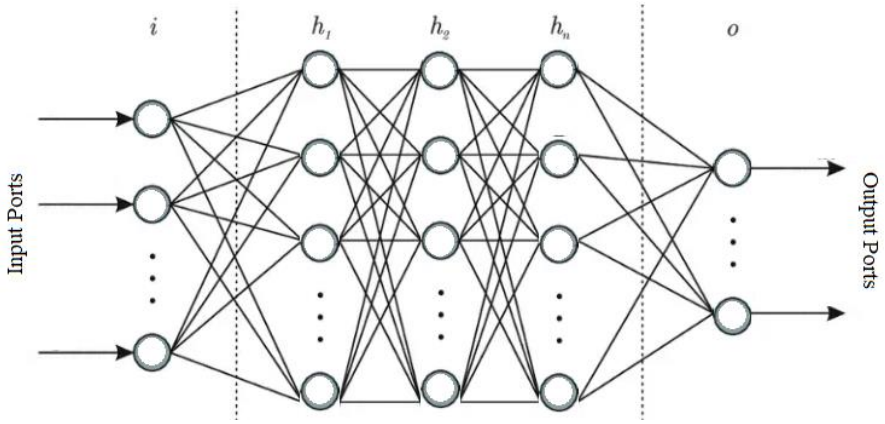


Fig. 6.1 Basic ANN structure with one input, output, and N hidden layers

These interconnections have various stages called layers and each layer is updated with bias and weights to get the desired output based on the application area. The appropriate functional mappings of the neurons in each layer lead to the learning of data fed to it. This learning and storing of data are done on a regular process of training in a manner like the biological neural network.

The purpose of the ANN study in this chapter is to explore various deep learning models and find out the best applicable model for optical switching applications.

6.3 ANN Applicability in Switching Configurations for Data Center

The all-optical approaches have been powerful encountering electrical and electronic hinderances overtime but the impairments created in the high-radix and low-channel spacing systems can be of high risk putting the quality of service in a compromising position. Hence, the implementation of ANN in data centric photonic switching configurations has become an important mission. The performance of DC switching is completely based on the high quality of service and minimum reception-error. The study in [169] has put a furnished presentation of various approaches to

understanding the difference between linear assemblage and non-linear functions of activations in ONN i.e. optical neural networks. The combination of optical configuration with artificial intelligence approaches has the capability of creating high-speed structures that compensate for all-optic impairments. The various salient features of ANN can be exploited for several other applications areas related to optical communication for prediction and classification analysis. The benefit of exploiting ANN in optics is that it can train and adapt to various environmental changes. The implantation of such a network can be easily done parallelly with the original processors running on different codes. This is why the acceptability of ANN in the optical field is obvious and enticing.

6.4 Various Deep Learning Models

The basic idea of deep learning as clear from the name is to self-learn the data it is being trained on for a while. This training of data can vary in a way the processors can vary for a particular field. The extraction of features, grouping the data into some meaningful fashion and discovering useful information out of raw data, and leaving the useless data patterns to require multiple levels of training. Similarly, different training algorithms are built to adapt to the need of an application. Some of these famous algorithmic models are listed below:

1. *Multi-Layer Perceptron Model (MLP):* This is the elementary model and is also considered the ancient model of learning. The structure is similar to simple ANN shown above in Fig. 6.1. These are also known as feed forward neural networks as the data travels in the forward direction only between the multiple layers. It can also use the backpropagation error method to increase accuracy. When the network doesn't provide the desired output with the combinations of random weights and bias and non-linear activation [169], the error in the previous layered is calculated and updated to the next layers to remove the margin between the predicted and desired output. Hence, the determination of appropriate weights in this method is the most difficult part. MLP employs the hyperbolic tangential and Rectified Linear unit (ReLU) activation functions.

These are considered good for image compression, speed recognition, and classification. Such a model has cons and difficulty in holding the probabilistic problem that utilizes the probability

density function to analyze the data. Also, the output data can be observed in logic terms of either '0' or '1' and the network can also get stuck in local minima during the weight updating process.

2. *Radial Basis Function (RBFN):* This model is an upgradation in the MLP as it can finish processing in less time by utilizing the radial basis function for activation. It is a three-layered network that works in two different stages utilizing trial and error removing techniques. Firstly, it processes the whole data based on k-means unsupervised learning. Secondly, it employs the mean square error (MSE) technique to evaluate the error and update weights based on linear regression and focus on minimizing MSE.

Such networks have their application in predicting stock market prices and ups and downs in retail platforms working mainly on time-series data. Since MSE is parallelly calculated unlike MLP, it doesn't back propagate the error. This is also the reason for its large computation time.

3. *Convolutional Neural Networks (CNN):* The problems that need deep recognition and forensics of the data are processed with CNN models. This model breaks the larger data into small overlapping pieces for learning the features rather than the whole data at once. It is mostly applied to the image and video frames [168]. The convolutional, max pooling, ReLU activation, and interconnected output layer make it more attractive for objection detection at the bigger internet platforms.

This is also applied in the fields like speed and text recognition because of its higher accuracy as compared to other ANN algorithms. But this algorithm requires high computation GPUs for training the heavy data.

4. *Recurrent Neural Networks (RNN):* Such networks brought advancement in the most widely spread platforms called google keyboards that autotypes the sentences. The RNN has feedback cycles [170] in between those interconnections that make it more accurate and bring in another element of memorizing the previous output pattern for forward processing. RNN is capable of taking a series of unlimited input patterns. This is why it is helpful in the detection of text, time series prediction, and analyzing video frames. Since it is clear from its name, it is recurrent i.e. it can take time in predicting the desired output but the accuracy is guaranteed.

There are many other types of deep learning models like restricted Boltzmann machines, self-organizing maps, Generative Adversarial Networks, and autoencoders but this chapter is mainly focused on putting a solution to prediction and classification problems that can be encountered in the optical communication field. Hence, the study of RNN is further explored.

6.5 Different RNN Models

The basic recurrent neural network can be observed in Fig. 6.2 with data cycles in a loop in the hidden layers. The layer 'x' is input which is fed to the 'h' hidden layer that can be multiple and have pre-defined functions, biases, and weights. The memoryless network with a large number of hidden layer neurons doesn't get effected by the previous layer-neuron's information and can be fed to RNN to know the previous information and get the desired output. There are standard functions for the activation of RNN and standardized biases and weights to have similar parameters for each hidden layer. This network doesn't need to create a large number of hidden layers as it revolves around the information in a loop in a particular hidden layer at each stage.

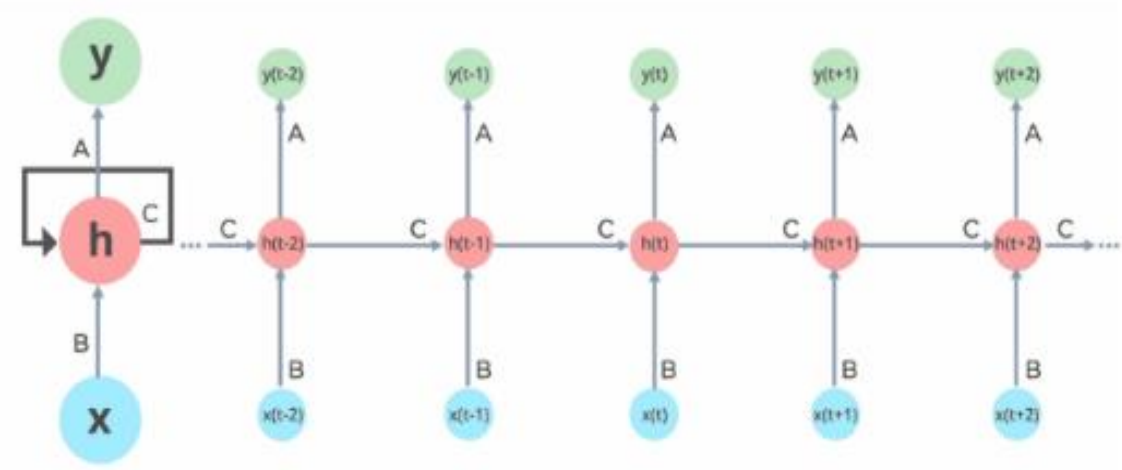


Fig. 6.2 Basic recurrent neural network structure working

There are various types of RNNs available [170]. Following are the four types:

1. *One to One RNN:* The RNNs utilized for basic machine learning problems have a single input and single output which are also called Vanilla Neural Networks as shown in Fig. 6.3(a).
2. *One to Many RNN:* The structure of this network has a single output but can have a large number of outputs illustrated in Fig. 6.3(b).

3. *Many to One RNN:* The basic structure of such RNN has many inputs but only a single output is connected to its hidden layer illustrated in Fig. 6.3(c). Such networks can be utilized for classifying the data either into positive or negative categories.
4. *Many to Many RNN:* The RNN employed for translating a particular machine have more than one input and output. The illustration of this RNN is given in Fig. 6.3(d).

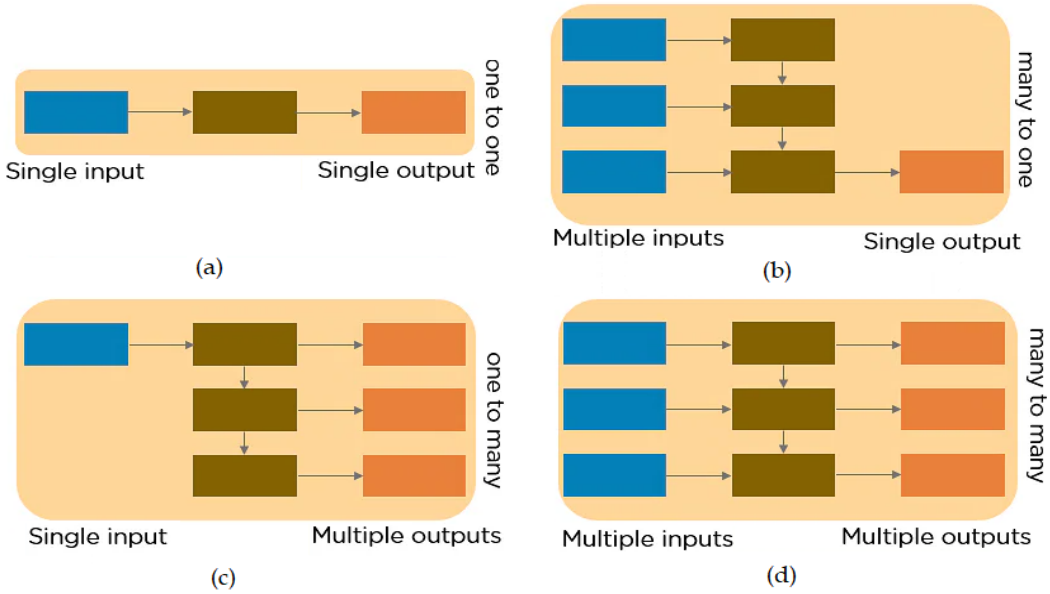


Fig. 6.3 Various types of RNN structures

6.6 Introduction to LSTM Networks

The recurrent neural networks are designed to solve the time-series and sequential problems for stock market value predictions and text generation. These networks are time-dependent and face the problem of vanishing gradients. The gradients are the elements in RNN that help in carrying the information. The gradient becomes small with time and a very small value of such a gradient can make the parameter-updating process difficult.

This problem of RNN makes the learning process difficult for long sequential data and prediction accuracy for long sentences can degrade. The backpropagation of error will again cost time and low computation efficiency. Hence, the solution to this problem is LSTM i.e. Long-Short-Term-Memory Networks [171]. These are special kinds of RNNs that are designed to handle long-term dependencies.

The design of hidden layer loops has been updated by adding activation functions like sigmoid and hyperbolic tangent as shown in Fig. 6.4.

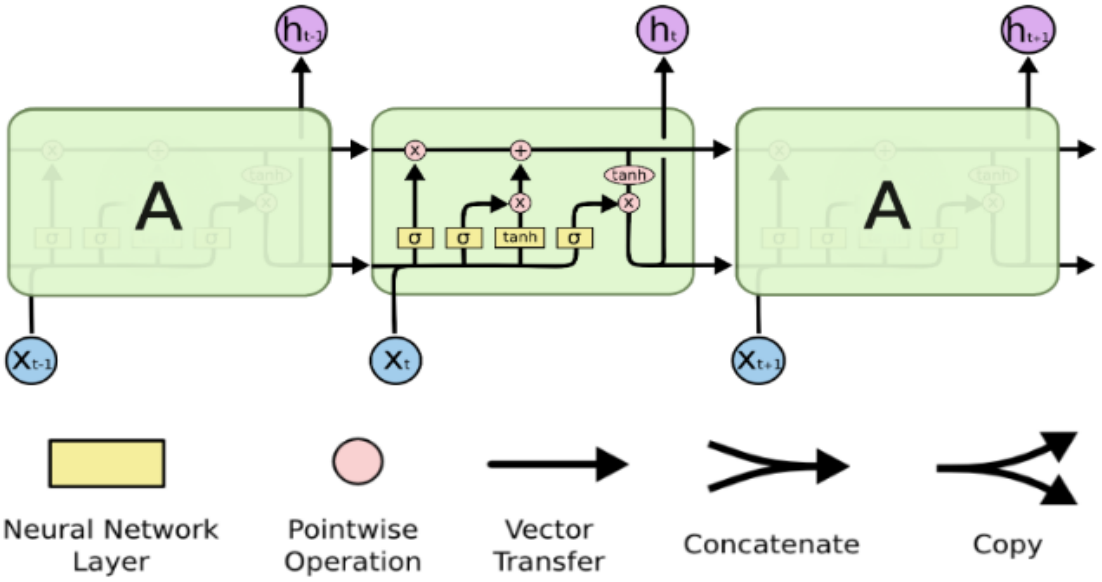


Fig. 6.4 Basic LSTM network with activation functions

6.6.1 Working of LSTM Network

The LSTM network works in basic three steps where it classifies the information to remember, forwards the required data to the current state, and decides which information should make it to the output. The basic working is written as follows:

1) *Learning the information to remember:* LSTM first remembers the information that doesn't need to be followed with the remaining information to the end. This useless information is first omitted from the basic data utilizing the sigmoid function 'σ_f' [171]. It compares the previous layer information i.e. 'h_{t-1}' with the input 'x_t' with 'w' as weight and 'b' as a bias to compute the forget function as follows in equation 6.1:

$$f_t = \sigma_f\,(w.[h_{t-1}x_t] + b) \qquad 6.1$$

This particular function 'f_t' forgets the useless information so that the chance of getting errors in the prediction of the original desired output is less.

2) *Decision making of adding the amount of the previous unit to the current layer:* This layer employs two activation functions i.e. Sigmoid function and the hyperbolic tangential function.

With the help of sigmoid activation 'σ_s', the output in terms of logic units i.e. 0 or 1 is passed to the next layer as shown in equation 6.2 whereas the tanh activation provides [171] the appropriate weightage to passed values in terms of '-1' and '1' as shown in equation 6.3:

$$s_t = \sigma_s\,(w_s.[h_{t-1}x_t] + b_s) \quad 6.2$$

$$act = tanh\,(w_{act}.[h_{t-1}x_t] + b_{act}) \quad 6.3$$

3) *Decision making of the final output from the previous layer information:* This is the final step of running the information through the sigmoid activation 'σ' as shown in equation 6.4. Hence, tanh activation from the previous state pushes the values to map to '-1' and '1' and then multiplies those values by the output of the next layer sigmoid function as shown in equation 6.5 making it to the final output 'm_t' [171].

$$out_t = \sigma\,(w_{out}.[h_{t-1}x_t] + b_{out}) \quad 6.4$$

$$m_t = out_t * tanh\,(act_t) \quad 6.5$$

6.6.2 Various Activation Functions

An activation function in any neural network decides whether the neuron of a particular layer should be activated or not. In other words, it decides the importance of information that the neuron is carrying at that time and whether it should be passed on to the neuron or not. This importance stands on the fundamentals of prediction and classification analysis using simpler arithmetic operations. Hence, the major role of an activation function is to evaluate the final desired output from the raw data fed to the layer.

In deep learning, sometimes this activation function is called as transfer function as it transfers the summed biased-weighted input to next layer neurons to derive the final output. The major purpose is to annex the non-linearity in the given neural network. This is because each layer of the linear model will behave the same way in forward propagation making it difficult to learn the complex problem. Hence, non-linear activation functions are preferred [169]. There could be 3 types of activation functions in neural networks:

1. *Binary Step function (BSF):* The threshold value of this function decides the activation of the neuron. The fed input is compared with the function's threshold value. The input value greater

than the threshold decides the activation of neurons and a lower value will make the neuron deactivated. The formula in equation 6.6 [169] is an illustration of this function:

$$BSF(x) = \begin{cases} 0 \; for \; x < 0 \\ 1 \; for \; x \geq 0 \end{cases} \quad 6.6$$

BSF is not able to deliver the outputs with multiple values. Hence, classification problems with multiple classes cannot be handled by BSF. It also has zero gradients of step function which is a further obstruction in the back-propagation technique.

2. *Linear Activation Functions (LAF):* This activation can also be considered as 'no activation' for the layer as it uses the identity function. Hence, no extra calculation is done by LAF [169] and the input is passed to the next layer as it is. Mathematically identity function can be given by equation 6.7:

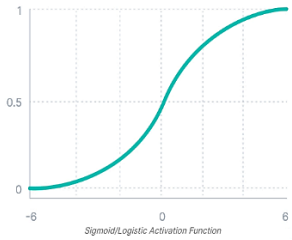
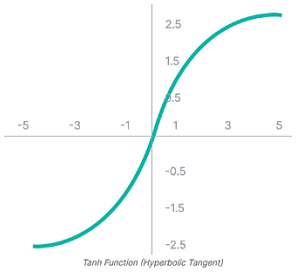
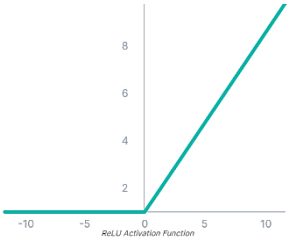
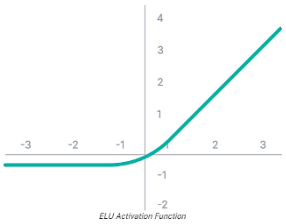
$$LAF(x) = x \quad 6.7$$

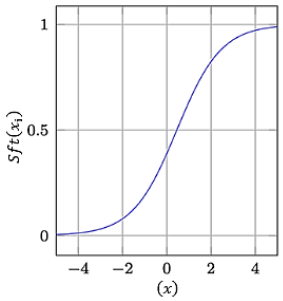
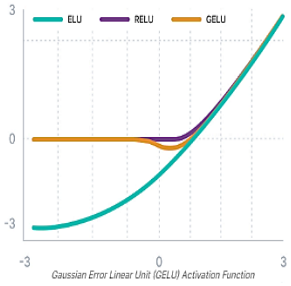
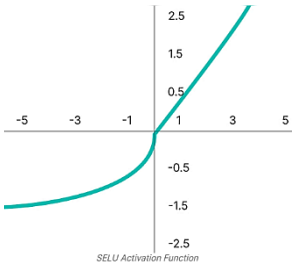
Since it doesn't have any relation to the input or any complex mapping with inputs and the derivative of such identity function is always a constant, it cannot be used for the back-propagation technique. The activation of the second layer will be similar to the first and the third will be always similar to the second which in turn matches with the first layer and so on. This means all the hidden layers are producing the same output compromising the long dynamic calculation time. Hence, it just turns the whole neural network into a single layer network despite of have more than one hidden layer.

3. *Non-Linear Activation Function (NLAF):* These functions solve the limitations of the above activation functions by allowing back-propagation analysis as they can have a meaningful derivative related to input [172]. This makes it propagate back and understand the mean difference between the predicted and desired output in order to have an accurate prediction.

The neural network with multiple hidden layers can now have non-linear relations between inputs and neurons of the next layer which helps in evaluating the final output. Various NLAFs are utilized in neural networks [172] depending upon the application which is shown in Table 6.1.

Table 6.1: Various non-linear activation functions with particular ANN applicability

Name & Scientific Notation	**Definition**	**Graphical Illustration**	**ANN Preference**
Sigmoid/ Logistic $s(x) = \frac{1}{1+e^{x}}$	I/P and O/P ranging btw 0 and 1 can be fed to it. It is differentiable and offers an even gradient and hence prevents unwanted jumps in O/P.		Regression Networks for time-series problems, RNN, LSTM
Hyperbolic Tangent $t(x) = \frac{e^{x}-e^{-x}}{e^{x}+e^{-x}}$	The S-shape is similar to a sigmoid but the O/P is mapped between -1 and 1. It's zero-centric nature makes the mapping of O/Ps close to '0' easy.		Time-series problems, CNN, RNN, LSTM
Rectified Linear Unit (ReLU) $ReLU(x) = max(0, x)$	Utilizes the derivative function to offer efficient backpropagation. It doesn't activate all neurons at once and only deactivates if linear transformation is less than zero.		CNN, Image, and Video processing
Exponential Linear Units (ELU) $ELU(x) = \begin{cases} x; & x \geq 0 \\ \gamma(e^{x}-1); & x < 0 \end{cases}$	It modifies the negative slope of ReLU so that its log-curve can be utilized for defining negative I/Ps		Accurate learning Deep CNN

Softmax Function $Sft(x_i) = \frac{e^{x_i}}{\sum_k e^{x_k}}$	It converts the raw O/P into probability vectors i.e. in a Probability distribution over I/P class. It approximates the maximum values generated by ReLU.		Deep CNN
Gaussian Error Linear Unit (GELU) $GELU(x) = xP(X \leq x)$ $0.5x(1 + tanh[\sqrt{\frac{2}{\pi}}(x + 0.045x^3)])$	O/P is observed as a combination of zoneout, dropout, and activation ReLU. The ReLU multiplies I/P by '0' deterministically whereas dropout and zoneout multiply stochastically by '0' and '1' respectively.		BERT, ALBERT, ROBERTa, and NLP, RNN models.
Scaled Exponential Linear Unit (SELU) $SELU(x) = \alpha \begin{cases} x; & x \geq 0 \\ \gamma(e^x - 1); & x < 0 \end{cases}$	The previous layer's mean value and variance are preserved by the next layer to normalize the O/P. Unlike ReLU, it can have +ve and -ve values for shifting the mean.		CNN

The major usage of these activation functions is done according to the application area and the type of problem of prediction or classification one is dealing with. As for the simplicity case, Regression Networks utilize Linear activation functions, Binary classification problems employ sigmoid or logistic activations, Multi-Class classification can use softmax activation, Multi-label type of classification can apply sigmoid, Recurrent neural networks famously employ hyperbolic tangent and sigmoid activations, and Convolutional neural networks employ ReLU and softmax both depending on the desired accuracy.

The LSTM structure is proposed for predicting the best destination port based on various parameters that help in faster switching of data. This is done in two ways:

1. LSTM prediction without the Port-Availability Information
2. LSTM prediction with the Port-Availability Information

6.7 Proposed LSTM Scheme for DC without Port-Availability Information

Deep learning neural network algorithms being a part of prediction analysis at high-end platforms, various approaches have been reported. These include the Reconfigurable Optical Add-Drop Multiplexer (ROADM) network that has ninety channels [173] for wavelength assignment, in Routing-Modulation-and-Spectrum [174] network for reducing blocking and Reinforcement learning for dispatch rotuing [175]. To handle the complex state parameters for predicting traffic and removing latency issues, RNN plays an important role in creating a system that can control the surge in users. In this section, an LSTM-based RNN network is proposed for handling big-data as RNN structures are specially modelled for sequential data. The long-term dependency problem [176] of RNN is solved by the choice of an LSTM network.

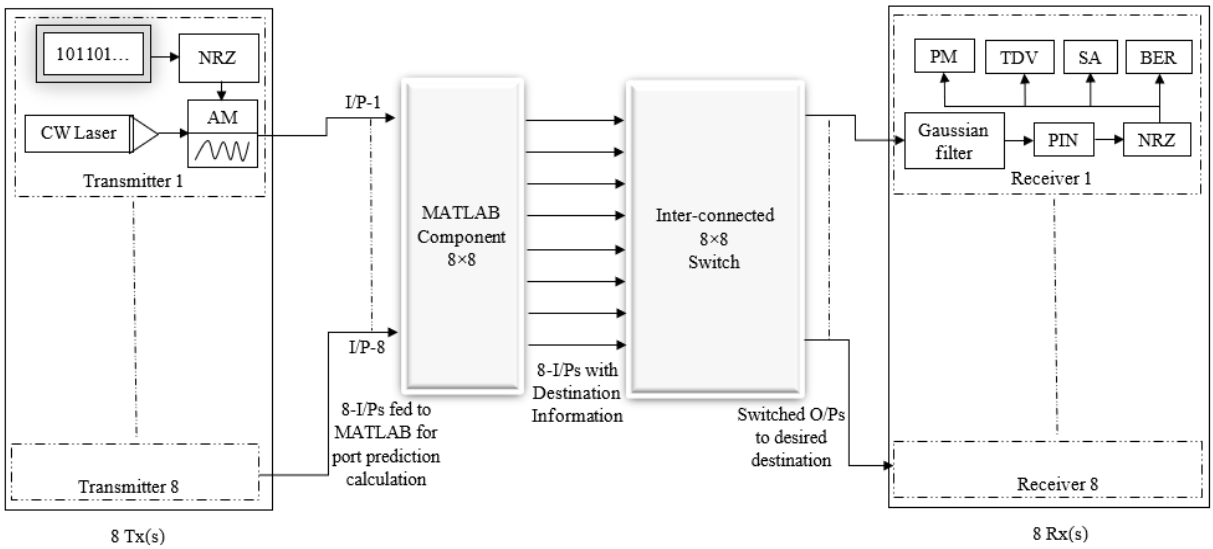


Fig. 6.5 Proposed LSTM implementation in 8×8 S-E-S switching interconnected structure with MATLAB interfacing

In the proposed 8×8 interconnected switching S-E-S structure mentioned in chapter 5, the LSTM-based neural networking is implemented as shown in Fig. 6.5. The structure has 8 input and output ports interconnected to each other making 128 different input-output paths suitable for switching

the data at 10 Gbps of bit rate with 0.1 THz of minimum port spacing. Since it is dense-channel problem for load-balancing applications, the prediction of the best switching path is needed for a fast and better quality signal. The MATLAB component shown in the above figure decides the shortest path with the minimum possible error.

The port-path combinations from the previous S-E-S structure are fed to the component. After the proper training of LSTM, it predicts the best possible route for the data to switch to the desired destination. This information is again fed to the inputs of the switching structure along with the information and accordingly the data gets switched.

6.7.1 Training of the Network and Monitoring Parameters

The LSTM network has 12 layers where the first and last are input and output layers and the rest 10 are hidden layers. The first step is to train the network so that it learns the best to predict the accurate combinations. The training is done utilizing the Milling dataset supplied by BEST lab [177] at UC Berkeley and after the network learns to find the best out of trained samples, the network is tested on the input-output path combinations possible for the 8×8 interconnected structure. Since the LSTM network is best in discarding the useless state the accuracy of prediction is high.

Firstly, the LSTM network loads the test samples of various paths where it evaluates the Euclidean distance between the paths. The average of this distance decides the minimum distance path as shown in the following Algorithm 1.

Algorithm 1. Steps for selecting the shortest and minimum error path for Switching

---

- Check the minimum and maximum port distance from training samples.
- Calculate average port distance 'D_{avg}' as a threshold for decision in test samples.
- Calculate Euclidean Distance 'D' between the test Ports.
    - If $\begin{cases} D > D_{avg} : Long-distance\ path \\ D < D_{avg} : Short-distance\ path \end{cases}$
- If the prediction accuracy is> 90%, give a classification result.
- Compare BER for the short distance paths as classified above.
- Select the path with minimum BER.

The LSTM network finally classifies the paths into two categories short-distance path and long-distance path. The last step is to take the combinations of various short-distance port-path and compare them on the basis of the minimum BER available and selects one for switching purposes.

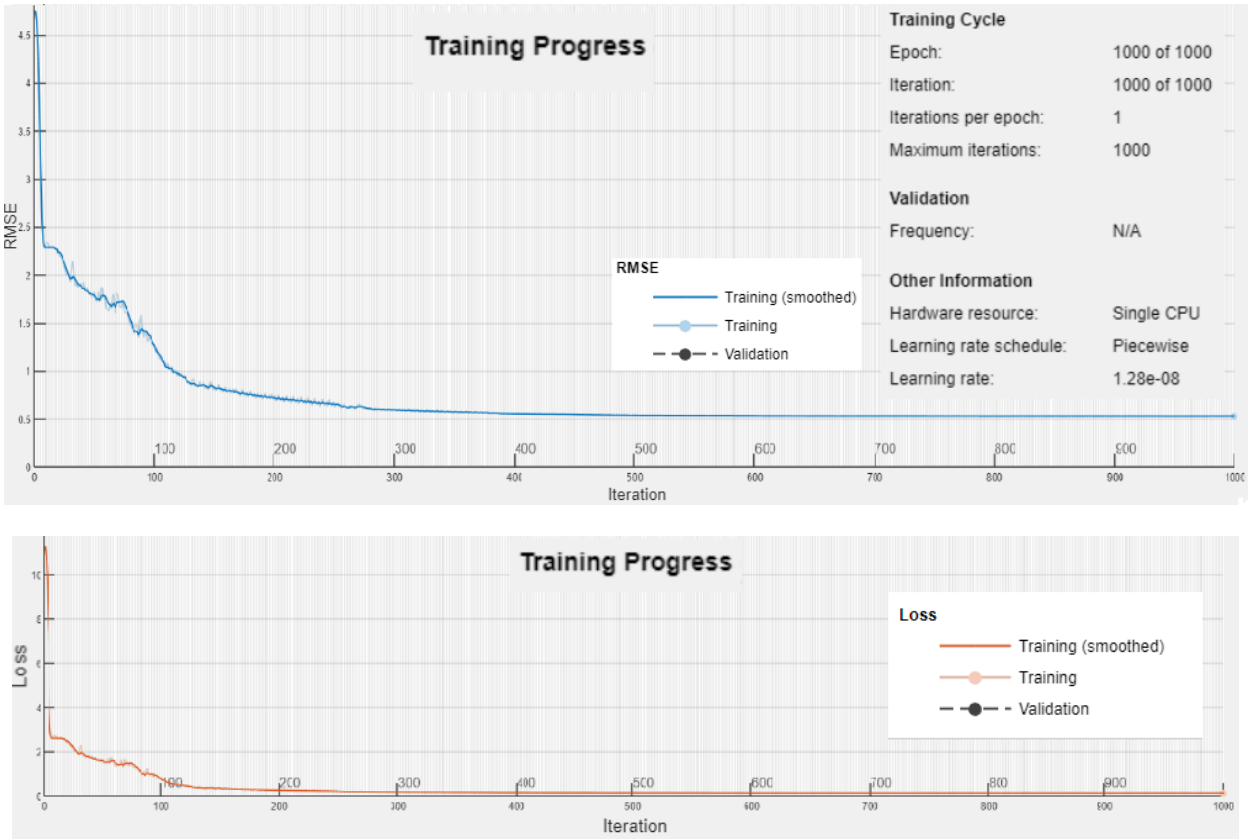


Fig. 6.6 Training progress in terms of RMSE and Batch Loss in MATLAB

The correct measure of training progress is to check the accuracy, loss, and root-mean-square error (RMSE) during the training of the network. The structure is trained for thousand epochs. Since it is an RNN network, the training progress of regression networks is evaluated by RMSE, and batch loss for the given epochs. It is observed from Fig. 6.6 that an RMSE of 0.53 and batch loss of 0.1 is achieved. It can be seen that learning of the network improved when it reaches near the 550th epoch and loss reduces from 11.3 to 0.1 and RMSE reduces from 4.75 to 0.53.

6.7.2 Classification and Testing

Since the current method is doing predictive modeling from numeric values and approximating the minimum and maximum distance paths on a basis of some algorithm, this problem is a regression and classification problem. The basic purpose of testing is to compare the NN outputs against the

required targets in particular testing instances. To remove the problems of predicting the numerical value and classifying based on that value, sometime separate prediction models are prepared but divergence in the outputs of these two models always remained an issue. Hence, only a single model has been designed for achieving the prediction and classification using multi-input and multi output NN. The proposed model is tested on the following parameters.

1. *Prediction Accuracy:* This parameter tells how efficiently the predicted value matched with the actual target value while dropping the noise and statistical fluctuations in input. The model predicts the desired switching path with 97% of prediction accuracy as shown in Fig. 6.7 which is better than previously reported 89% accuracy in [148].

2. *Classification Accuracy:* This evaluates the accuracy based on correct classification done by the LSTM model. It can be seen from Fig. 6.7 that the classification accuracy is 99.5% which is quite higher than the 89% reported in [178]. This shows the superiority of the proposed model.

3. *Confusion Matrix:* The whole model is evaluated by a confusion matrix which calculates the parameters like True Positives (TP), True Negatives (TN), False Positives (FP), False negatives (FN), Positive Prediction Values (PPV), and Negative Prediction values (NPV) [166] as shown in the confusion matrix plotted in Fig. 6.7 and also shown in Table 6.2.

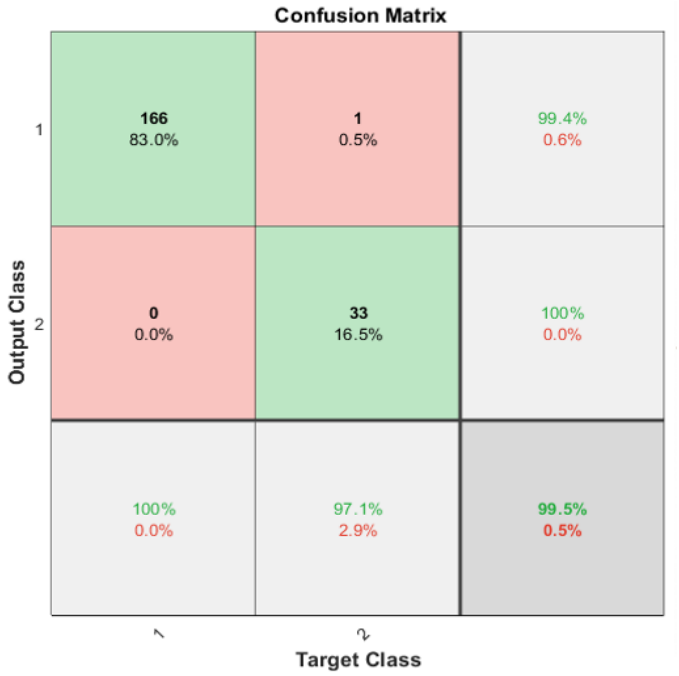


Fig. 6.7 Confusion Matrix evaluating the performance of the purposed model

Out of 200 path test samples, a total of 166 samples are correctly predicted as long-distance paths and 33 are correctly predicted as short-distance paths.

Table 6.2: Values of various parameters in the confusion matrix

Parameter	Proposed model results (%)
True Positive Rate	100
True Negative Rate	97.1
Positive Prediction Value	99.4
Negative Prediction Value	100
Accuracy	99.5

Whereas only one long-distance path has been falsely predicted as a short-distance path adding to a False Positive of 0.5% and True Positive of 83%. On the other hand, no short-distance path has been incorrectly classified as a long-distance path which has 16.5% of True Negative and 0% of False Negative being predicted as short-distance.

6.7.3 Improved Switching Parametric Results after LSTM

The BER and ER graphs show promising results after the application of the LSTM network with an S-E-S switching configuration. Another intuitive degree of performance is demonstrated by the evaluation of Eye Height (EH) and switching time.

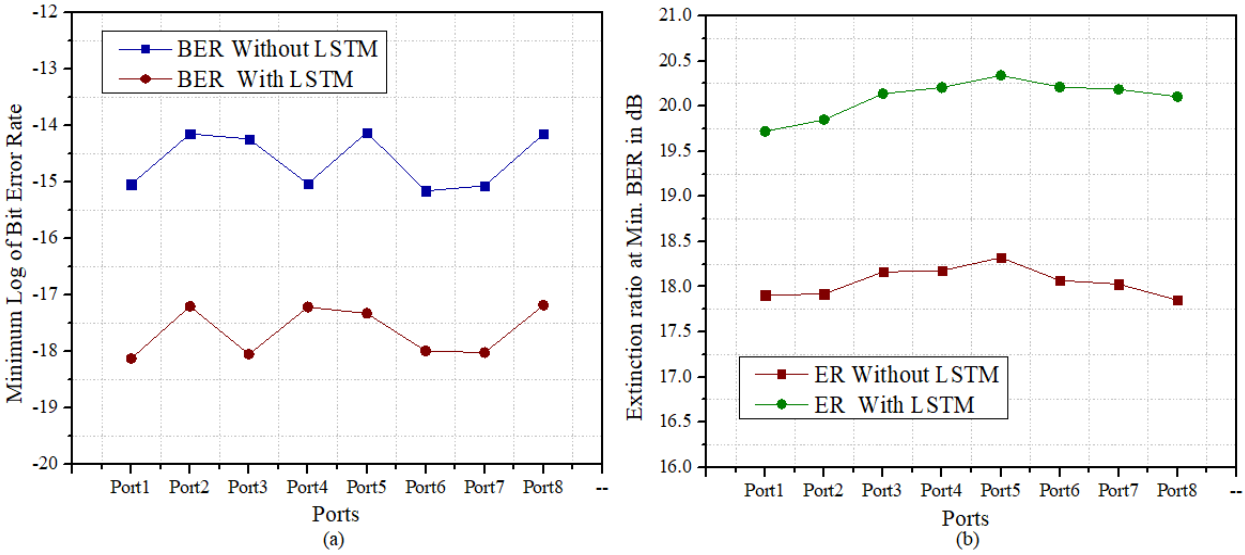


Fig. 6.8 With and without LSTM comparison of (a) BER and (b) ER

The graph in Fig. 6.8 (a) shows port-wise BER analysis in which BER improves from 10^{-14}-10^{-15} for switching without LSTM RNN to 10^{-17}-10^{-18} with LSTM network interfacing. The improvement in the structure is seen since LSTM networks are able to forget the information from the old state and keep the required data for the next level. In this way, only useful information travels to the next state.

Table 6.3: Parametric comparison for S-E-S structure with and without LSTM

Parameter	**S-E-S Without LSTM**	**S-E-S With LSTM**
BER	10^{-14} - 10^{-15}	10^{-17} - 10^{-18}
ER (dB)	17.8-18.5	19.6.-20.35
EH (a.u.)	0.005-0.008	0.0116-0.015
$\boldsymbol{T_s}$ **(ns)**	0.55-0.6	0.32-0.4

The eight port average values of various parameters are shown in Table 6.3. The improved eye height (EH) of 0.0116-0.015 a.u. and switching time of 0.32-0.4 ns can have been achieved for the structure utilizing the LSTM model that provides shorted and minimum error path to the S-E-S switching structure. It shows the latency issues can be solved by implementing deep learning in optical switching in data centers.

The factor ER has been helpful in the evaluation of the desired output power w.r.t. to undesired power loss that occurs due to either polarization effects or noise. The ER can be seen improved to 19.6-20.35 dB in Fig. 6.8 (b) showing the enhanced working operation with the LSTM network.

6.8 Proposed LSTM Network with Port-Availability Information

This chapter emphasizes removing the issue of switching the data to an unavailable path. The method discussed above in the 6.7 section shows the switching of data through a shorter path and has a minimum possibility of error. But the problem of that path being unavailable for that moment will create the input data to wait until it becomes free. Hence, the prediction of path-port availability is important.

The improvement in the proposed LSTM model is made by adding the succeding port power. The LSTM network utilizes 10 hidden layes and is trained on the same dataset for 2000 epochs to maximize the learning accuracy as much as possible. The first layer of the LSTM network takes

the data from the previous neuron and forgets the data with minimum weight. The tangential activation allots weightage between (-1,1). The information with significant bias and weights will be passed to another layer. The next ReLU activation decides the saturation level for providing good sensitivity. The final multiplication of input with old stage weights and summation of bias decides the output information. The interconnected connected of each layer supports the activation process. The following alogirthm 2 decides the best and available path for switching in S-E-S configuration:

Algorithm 2. Steps for selecting available shortest and minimum error path for Switching

---

- Check the power succeeding port in each port-path combination.
- The average power 'P_a' of testing samples with power 'P'.
  - If $\begin{cases} P > P_a : Unavailable\ Port \\ P < P_a : Available\ Port \end{cases}$
- Calculate Euclidean Distance 'D' for available paths only.
- Find the average Euclidean distance as 'D_{avg}'.
  - If $\begin{cases} D > D_{avg} : Long-distance\ path \\ D < D_{avg} : Short-distance\ path \end{cases}$
- If the prediction accuracy is> 90%, give a classification result.
- Compare BER for the short distance paths as classified above.
- Select the path with minimum BER.

If the succeeding port has a power greater than the average power of all ports, then it means there is a signal propagating through that path, and switching data on that path is not possible. It is classified as an Unavailable path by the LSTM network. Since the calculation for minimum distance is to be done for only available paths, the latency of the network can further be reduced. The path with a short distance and minimum error is selected for switching purpose.

6.8.1 Training of the Network and Monitoring Parameters

The LSTM network with 10 hidden layers is first trained on a Milling dataset supplied by BEST lab [177] at UC Berkeley so that the learning yields accurate predictions. The network is then tested for various input-output path combinations that can occur in the 8×8 interconnected structure. It is trained for 1000 and 2000 epochs to differentiate the learning progress of the

network. It is observed that with the increase in epochs, the learning rate improves which is determined by the base learning rate (BLR).

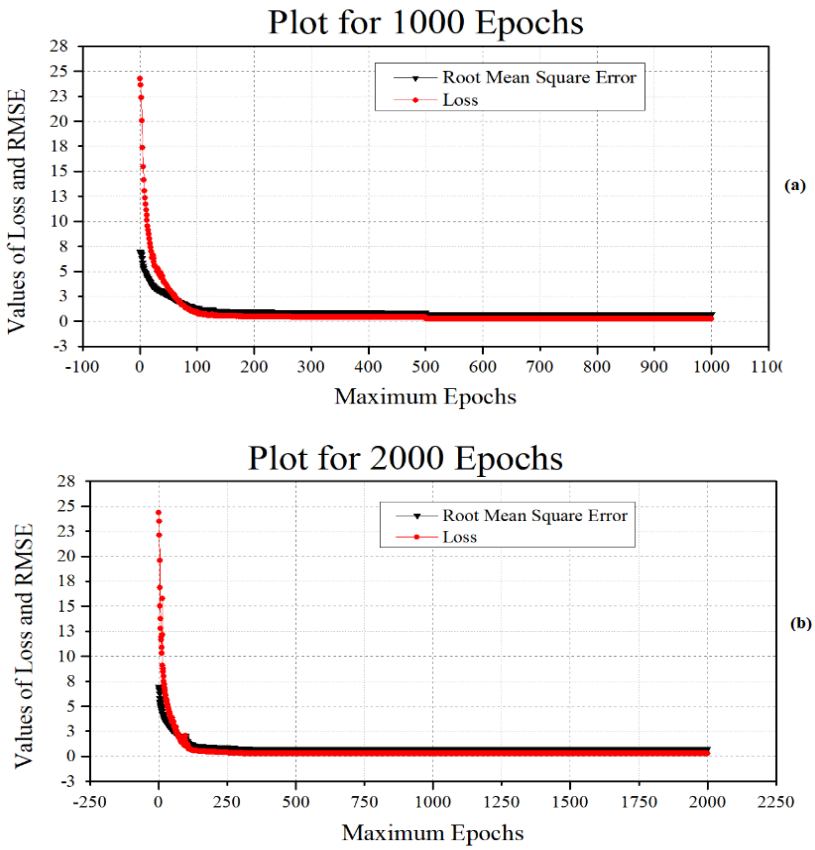


Fig. 6.9 Training progress comparison for 1000 and 2000 epochs

If the BLR value is too high, then it led to extra fast learning of sub-optimal weights which will create unstable learning. If the BLR value is too low, then either the learning process becomes too slow or it can get stuck in an infinite loop leading to no learning at all. The observation of batch loss and RMSE for 1000 and 2000 epochs can be made from the following Fig. 6.9.

For 1000 epochs, the loss, BLR, and RMSE are 0.4, 1.28 e-08, and 0.89 whereas, for 2000 epochs, it is 0.3, 3.2768 e-14, and 0.81. It can be seen that the loss stabilized at 0.3 and BLR is not undesirably low, the testing of the network is done by training the data in 2000 epochs.

6.8.2 Monitoring of Classification and Testing

1. Confusion Matrix: The significant measure of accurate classification and prediction analysis in a neural network is the confusion matrix that shows values of TPR, PPV, TNR, NPV, and Accuracy. The implemented model has two classes at first i.e. Available and Unavailable. The

available paths are then taken for another classification based on minimum i.e. shortest distance path and long-distance path. The shortest distance paths are then evaluated for minimum error path and then the best out of those is selected for switching.

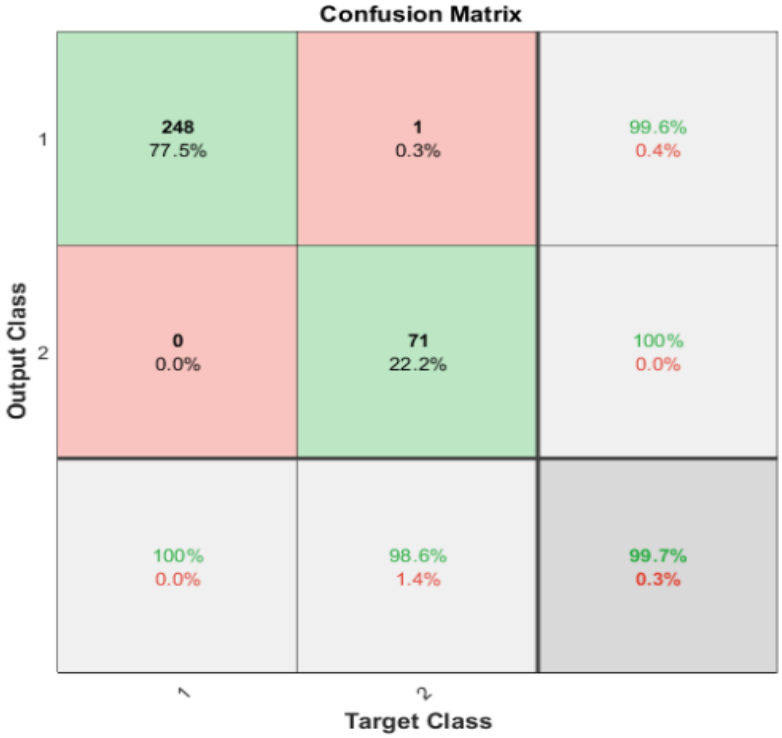


Fig. 6.10 Confusion matrix evaluating the proposed model

It can be seen in Fig. 6.10 that out of 320 test samples, 248 were short distance and are classified as short-distance paths leading to TP of 77.5%, whereas one long distance sample was classified as short distance with 0.3% FP. A total of 71 long-distance paths are classified as long distance whereas no short distance path was misclassified as long-distance. This adds to the precision of the model to 99.6%. The significant parameters are listed in following Table 6.4.

Table 6.4: Confusion Matrix Parameters for the proposed model

Evaluation Parameter	**Results of the proposed model (%)**
True Positive Rate (TPR)	100
Positive Prediction Value (PPV)	99.6
True Negative Rate (TNR)	98.6
Negative Prediction Value (NPV)	100
Accuracy	99.7

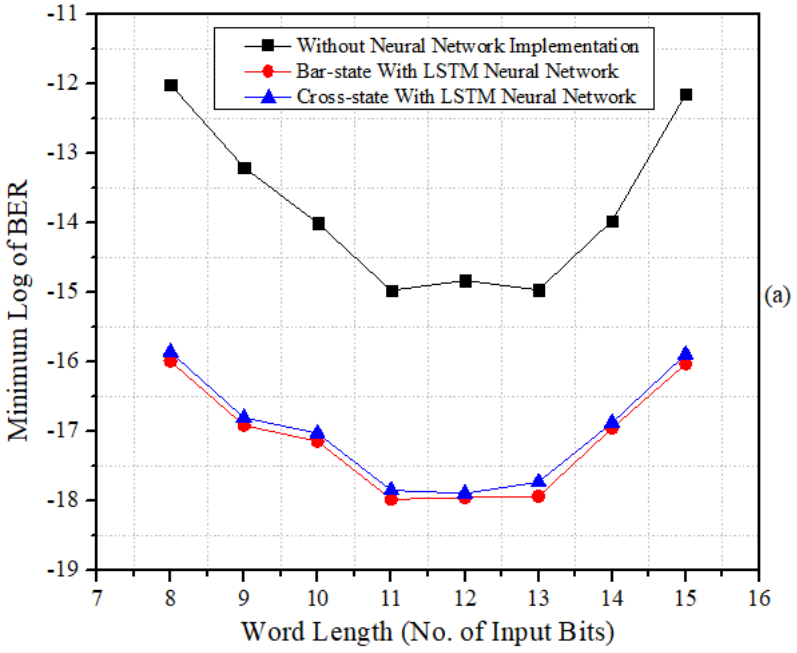
2. Prediction Accuracy: The measure of how accurately the correct class has been predicted as correct is called prediction accuracy. For the proposed model, it is 96.88% which shows that the proposed model is acceptable and efficient.

3. Classification Accuracy: The classification accuracy of 99.7% has been achieved as the model classified one of the long-distance paths as short distance adding to TP of 0.3%.

6.8.3 Improved Switching Parameters w.r.t. Word Length after LSTM

The investigation is made for various performance parameters w.r.t. word length which is an important parameter as described in chapter 5. It is observed that BER, EOF, ER, and switching time have improved with the application of the LSTM network. The BER and ER graphs are plotted w.r.t. word length i.e. number of bits present in the input sequence in Fig 6.11 (a) and (b) respectively. The graph shows that the rate of error at the reception is very low at a 13-word length i.e. 10^{-18} whereas for a 15-word length, BER of 10^{-16} is observed which is better than the acceptable BER.

The ER results in Fig. 6.11 (b) illustrate a surge with the LSTM network and a maximum ER of 19.5 dB is attained for a 15-word length. This shows the 8×8 S-E-S switching structure can operate with a 15-word length at 10 Gbps and yields efficient performance in terms of BER, ER, EOF, and switching time.



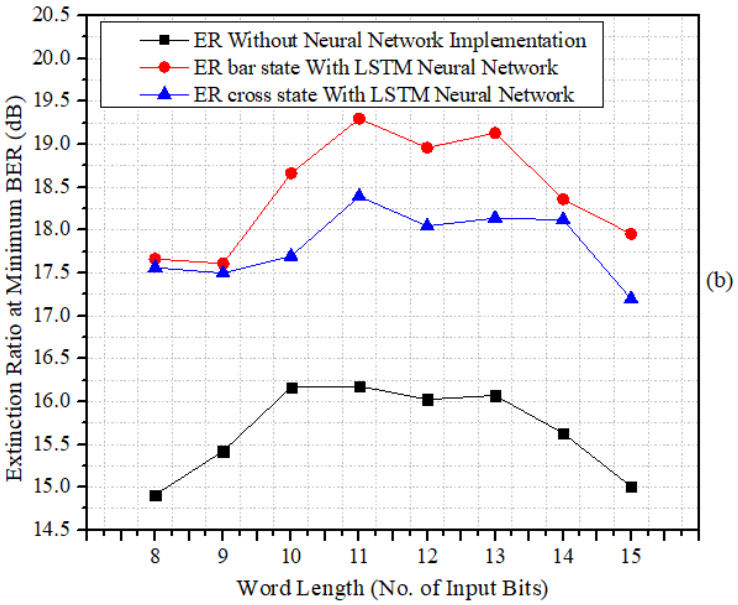


Fig. 6.11 Line graph comparison of (a) BER (b) ER w.r.t. word length

The parametric values are shown in Table 6.5. The interference at cross-ports can add to the noise in the receiver and further affect the extinction ratio. But it can be seen here in Table 6.5 that extinction has improved form 14.9-16.3 dB to 17.7-19.5 dB making it suitable for transmission purposes.

Table 6.5: Parameter values w.r.t. word length of S-E-S configuration with and without LSTM

Parameter	**S-E-S Without LSTM**	**S-E-S With LSTM**
BER	10^{-12} - 10^{-15}	10^{-16} - 10^{-18}
EOF (%)	85-87	95-97
ER (dB)	14.9-16.3	17.7-19.5
T_s (ns)	0.65-0.71	0.35-0.45

The switching time can be seen improved to 0.35-0.45 ns when the LSTM network is parallelly incorporated with the proposed switching configuration. The BER evaluation has shown improvement and lowered down to 10^{-18}. The eye-measurement evaluation has shown an improvement of 10% with 97% EOF calculating the wide opening of an eye than the structure without the LSTM network.

The throughput of the overall system is also evaluated to check if the proposed system is able to remove the throughput problems of DC-networking. With the evaluation criteria taken from research reported in [179], the capacity of the system can be evaluated based on interconnections and bit rates. The eight inputs and outputs flowing at the bit rate of 10 Gbps can make up the capacity of 640 Gbps [179]. The length of transmitting bits set at the PRBS generator is gathered as word length per user. It is observed from the above analysis that the system works efficiently with a word length of 15 showing BER of 10^{-16} and ER of 19.5 dB. The implemented structure being operated at a bit rate of 10 Gbps with a port spacing of 100 GHz and a maximum word length per port of 15 bits is said to have a throughput of 96 Tbps. This high throughput of the proposed system shows that it can excellently applicable for removing the challenges of HPC systems in DC switching networks.

6.9 Conclusion

In this chapter, the component-wise introduction to neural networks followed by their working and applicability in various areas has been analyzed. The main focus is on finding the best ANN structure for prediction and classification problems that occur in optical communication. It further explores the working of RNN models and clarifies the difference between various RNN models and brings out the best to continue for an optical domain. The introduction to LSTM networks and their working explains why is it preferred for prediction analysis. The next step illustrates the numerous activation functions and brings out their limitations. It enlightens the use of non-linear activation functions and the necessity of adding non-linearity in the complicated neural network.

To handle the complex switching operation more efficiently, the deep learning-based LSTM network has been introduced in the proposed S-E-S switching structure. The LSTM network helps in predicting the better path between input and output ports for switching useful data. This helps in improving the parametric performance by adding more accuracy to the prediction. This work is performed by two major analyses: One is to predict the port with the shortest distance and minimum error and the second is to bring out the ports which are available at that instant and then predict the shortest distance and minimum error path out of them. Hence, this chapter has been divided into two parts. Firstly, the RNN-based model utilizing the LSTM technique has been proposed for predicting and classifying the port destination for the Data Center photonic switches. In the latter part, the same model is

upgraded by adding information on the availability of ports for that particular destination utilizing the LSTM technique itself.

In the first part, the prediction accuracy of 97% and classification accuracy of 99.5% has been achieved by utilizing the enticing quality of LSTM networks to reject the futile data from the previous state. This helps to improve the errors in comparison to the structure that doesn't employ neural network models for prediction problems. The improved results of 10^{-18} of BER, 19.6.-20.35 dB of ER, 0.015 a.u. of EH, 0.32-0.4 ns of switching time are attained.

For the prediction analysis on available ports, the LSTM training is achieved for 1000 and 2000 epochs to realize the accurate and fast learning rate. The model gives 96.88% of prediction accuracy with 99.7% of classification accuracy. The performance of the structure is tested concerning the input sequence length. The ER of 17.7-19.5 dB with BER of 10^{-16} - 10^{-18} with wide eye opening of 95-97% is realized for the word length varying between 8-15 bits. The switching time of 0.35 ns shows the structure can remove the latency issue by maintaining the performance of the system. The throughput of 96 Tbps concludes that the implemented LSTM-based S-E-S structure is a potential solution to HPC in DCs.

CHAPTER 7
ROUTING SOLUTION FOR CPI IN DATA CENTERS

7.1 Introduction

In this chapter, the problem of controlling and scheduling the traffic in the Control Plane Interface (CPI) in data centers is explored and a solution has been put forward utilizing the TWSOA-EDFA-based compound amplification technique proposed in chapter 5. The scheduling of incoming connection requests has been done on a priority basis. The priority bits from the packet header and incoming request signals are taken as input to the logic-gate based proposed routing scheme. This chapter focuses on presenting error-free reception by synthesizing the AND-OR logic gating technique. Firstly, the issues in the present architectures are explored and then the importance of the implementation of optical-based structures is discussed. The gating mechanism is compared with existing literature to prove the superiority of the proposed scheme.

7.2 Problems in Existing Architecture

The 3-stage hierarchies of data centers shown in Fig. 1.3 are connected to establish the inter-communication. Since the DC structures have high-end aggregate switches but the complexity in DC configurations requires the appropriate scheduling and controlling of incoming traffic as shown in Fig. 7.1. To achieve this, data centers have CPI for controlling the routes of various protocols and managing the link [180].

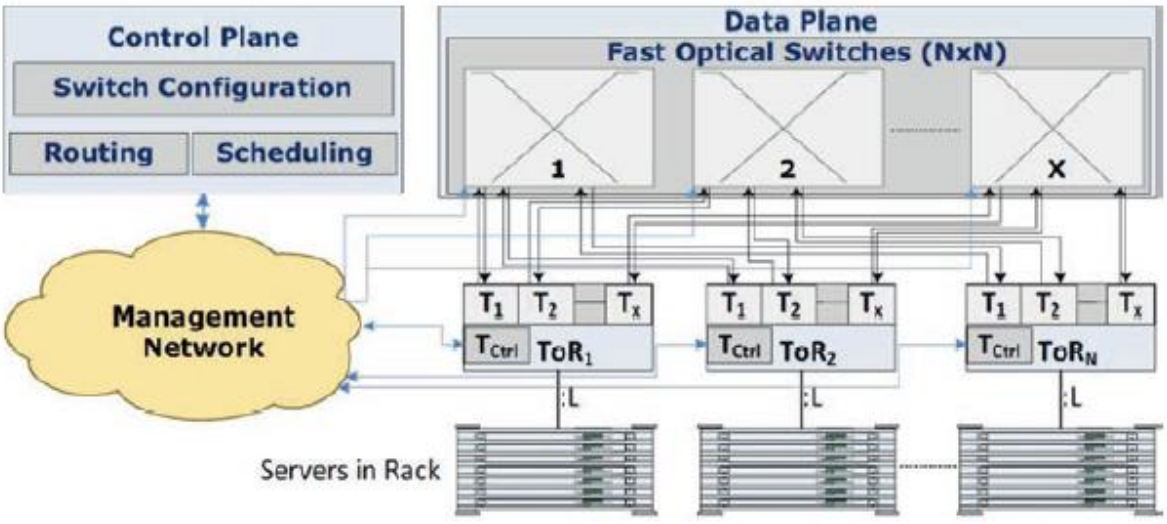


Fig. 7.1 Control Plane Interface with data plane switching structures in DC [180]

This part employs an algorithm for scheduling data flow and forwards the major flow with long and the minor flow is dealt with short bursts [181]. But the limitations of implementing it on hardware question the efficiency of DC networking. Various traffic sensitive [182] energy-aware [183] conventional techniques were presented for routing but scalability, and faultless communication has always been an issue. The structures employing plasmonic waveguides [184-185] can operate with high data-rate but the uncertain phase occurring with interfering EM waves generates a low [186] contrast ratio. The promising routing schemes utilizing software-defined network (SDN) [187] was a solution to these problems but its architecture with the centralized control limits the scalability and working speed of the present structure.

The routing operations done with the employment of logical gates proved advantageous in optical networking. The features of header recognition, encoding, data regeneration, and switching has attracted CPI applications. As shown in the above research work presented in Chapters 3 to 6, SOA-MZI-based routing can provide error-free, and power efficient operation with large optical bandwidth. The major focus on gating operations is given by utilizing SOA non-linearities but the low ER values for AND gate [190] and establishing OR operation [191] with reliable values have been an issue. The MZI operations [188,198] made it possible for achieving the AND-OR in a single structure but the parametric performance left limitations in an investigation. Apart from the fast response time, higher insertion loss [191] and low extinction ratio [184,192] also limit the proficiencies of CPI in DC applications.

When the request is made by traffic for routing, an appropriate active server is mandatory which is nearest to the end point client for handling the emergency. The path for routing is selected in such a way that it delivers faultless reception. This chapter persuades the routing features of OR-AND gates and dedicates the research to the context of the CPI for DC applications.

7.3 Proposed Gating Strategy

The header of the incoming connection request is jammed with numerous essential parameters that specify the topology, service type, destination, and others. The priority bit (PB) is a part of the header that decodes the emergency of the transfer of incoming signal. This signal is zero for no priority and one if priority is present. The incoming signal with PB is taken from the packet header and utilized for path allotment in the proposed routing architecture. The Top-of-Rack (ToRs) are

the top switches placed on the top of server racks. In Fig. 7.2, the ToR 1, j, k, and l are the ToR arranged waiting for the proper routing signal to switch the incoming traffic to the upper level of the hierarchy. This flowchart shows the stepwise proposed scheme to handle the incoming requests from different nodes. The requests are handled by dividing them in two directions: one if the signal from nodes needs an immediate transmission and the other where the node request waits for a particular time for the occupied path to become free. There is a signal that is sent on connection requests every time the path needs to be allocated. This signal is called a machine signal.

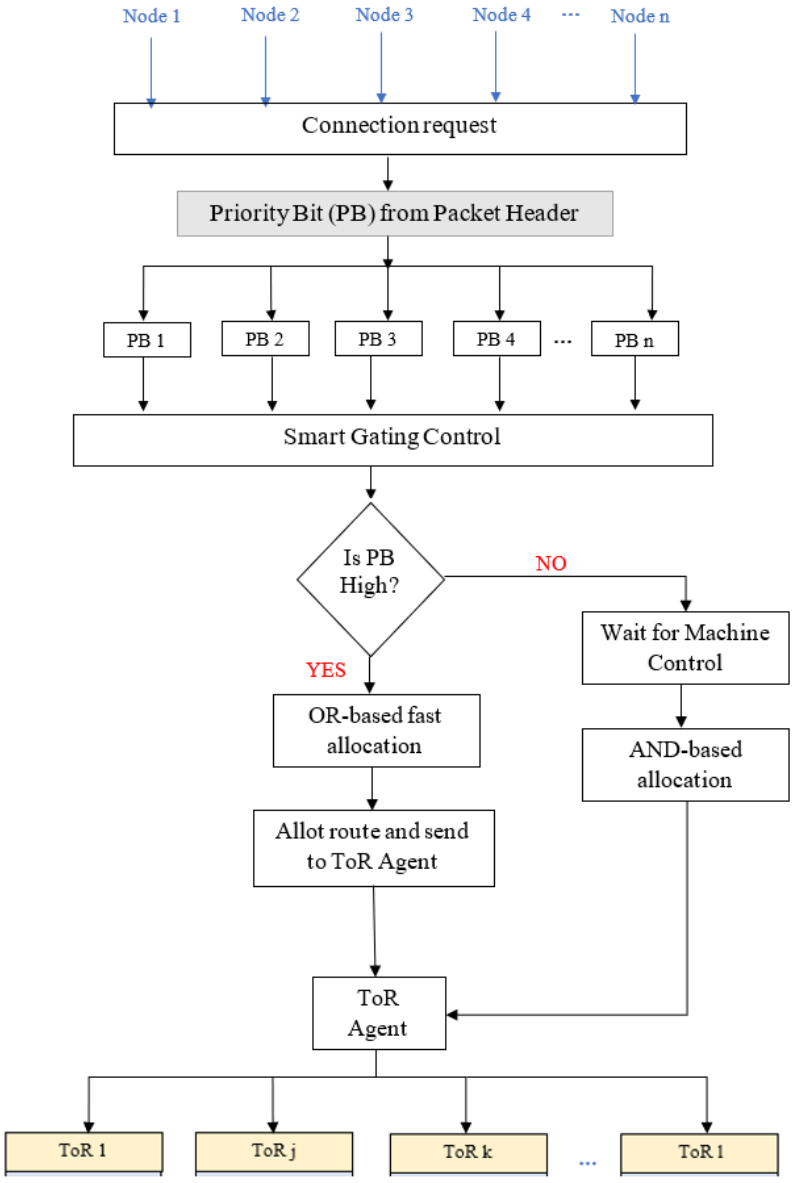


Fig. 7.2 Proposed Gating Strategy for handling various incoming requests

When the PB bit from each packet header is received, these are fed to the proposed smart gating control unit that has its second input from the machine. The machine signal is a high bit that informs the connection request. If the smart gating control takes both the inputs with the machine signal either high and request with high priority, then the signal needs to be allocated with the routing path as soon as possible. Hence, it is shifted to OR-based routing for faster path allocation. This can be directed to AND-based routing if OR-port is not available. If the PB bit is high and machine control is low, even then the smart gating control takes care of the priority of transmission and switches the signal to OR-gating allotment for reducing the latency issues. If the priority signal is low but the connection request has been made by the machine, them the signal can be made to wait for sending any other priority signal through AND-gate depending upon how much time can be spared for the signal in waiting. For low PB and MC, there is no need for the allotment. The numerical illustration of the above mechanism has been given in following Table 7.1.

Table 7.1: Numerical illustration of path allotment procedure

PB	**MC**	**Allotment**
0	0	No Need
0	1	Wait
1	0	OR
1	1	AND/OR

It can be observed that OR gating route allotment is employed for immediate allocation of the primary path to handle the emergency transmission. The AND gating route allotment is used for special secondary allocation where the node request and priority are both high. If the need for primary allocation is not discovered by the machine, then a connection request is made to wait for the time when the machine sends a signal signifying a vacant route. Utilizing the above information, once the signal is allotted with either OR-gating or AND-gating routing, the signal travels to the ToR agent that further determines the destination port by final allotment of switching path to an appropriate ToR.

7.4 Implementation of Logic Gating-based Routing

The logic gate-based routing approach has been shown in the following Fig. 7.3. The signal coming as the priority bit i.e. PB and machine control i.e. MC are fed to the implemented configuration as

input. The gaussian pulse generator helps in creating a gaussian pulse for better processing of the signal. The 3 dB coupler further employed in the structure couples these signals coming from the gaussian pulse generators and feed them to two arms of MZI that have TWSOA and EDFA on each side. This hybrid optical amplifier combination helps in mitigating the effects of polarization and other losses due to the non-linearities of TWSOA. The control probe regulates the intensity modulation of these signals during their propagation from the input to the destination side. The intensity modulation further saturates the gain of TWSOA. This alters the refractive index of the medium causing different phase shifts in the incoming signal [135]. When PB and MC are induced on a hybrid optical amplifier combination, the shifts get induced each time in the output pulse. For the OR-gating mechanism, in the presence of both PB and MC, no shift is observed and output is shifted as it is on the output port. The control probe signal that is undesired in the output can be filtered out with the choice of the appropriate filter.

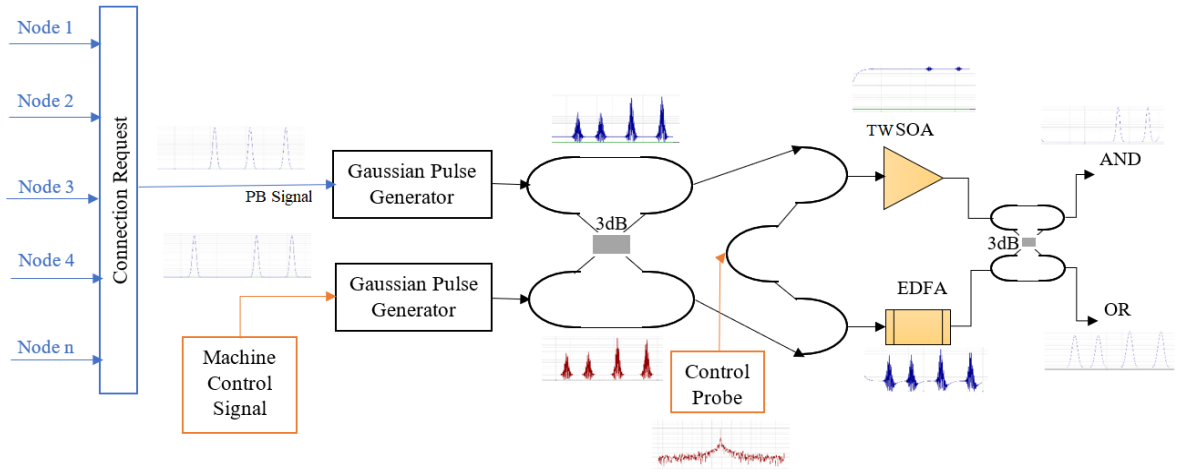


Fig. 7.3 Proposed smart-gating mechanism based on AND-OR logics for traffic routing

For the AND-gating mechanism, the output coupler combines the two pulses either destructively or constructively. With the use of the proper power of the control probe, the output phase can be controlled. During the constructive interference when the PB and MC both are high, an in-phase signal is realized and hence the AND output.

7.5 Parametric Performance and Analysis

7.5.1 Gate Routed Outputs

The designed smart gating-based routing configuration is operated on a 10 Gbps data rate for error-free reception. The pattern of data approaching from various nodes is PB and the machine signal

is MC. The TWSOA is operated with an injection current of 0.35 with $2.78\times e^{-20}$ and $3\times e^{24}$ as differential gain and carrier density respectively. The EDFA utilizes the 5 m length of erbium fiber with 2.2 m of doping core radius and applies 100 mW of forward pump power. The following Fig. 7.4 shows the inputs are Data A and Data B fed as the input to the proposed configuration. The waveforms shown in Fig. 7.4 (a) belong to the AND-logic operation whereas Fig. 7.4 (b) indicates the waveforms for the OR-gate operation.

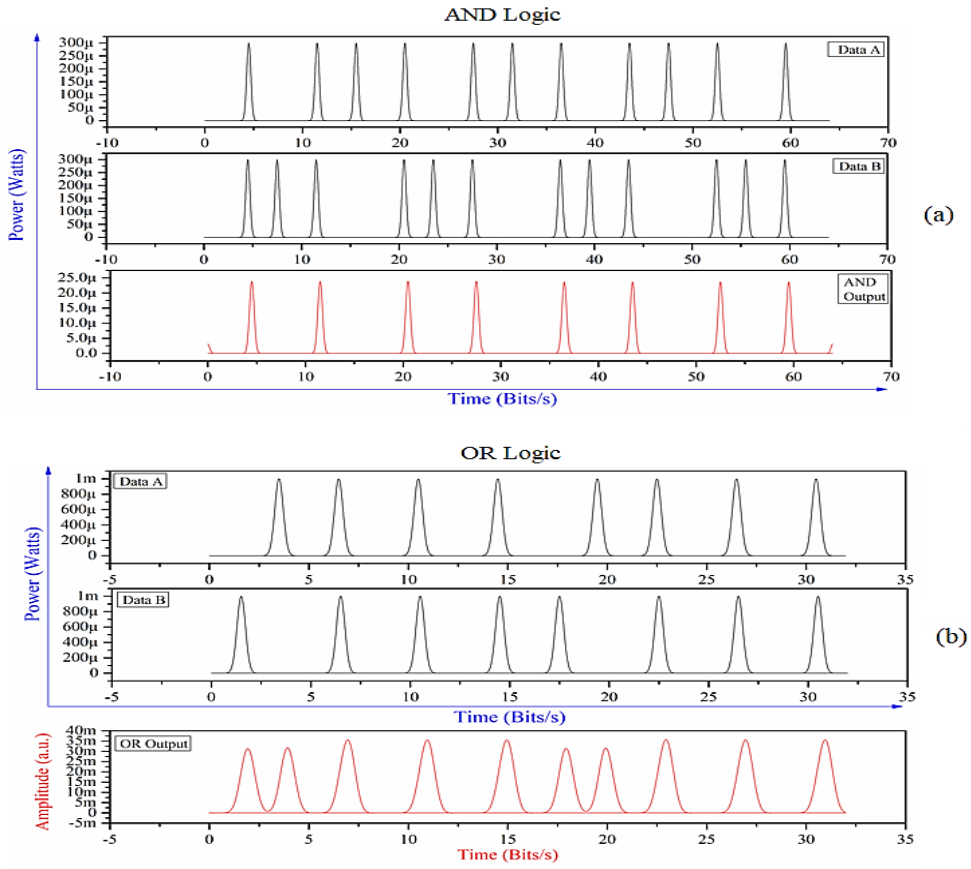


Fig. 7.4 Output illustration of proposed (a) AND logic (b) OR logic

7.5.2 Performance Parameters

The performance of the system is tested on three important parameters for logic gates i.e. Contrast Ratio (CR), Extinction ratio (ER), and Insertion Loss (IL). The parameters showed the best operation when compared with the gating-results reported in the literature. The performance is tested by varying the input power from -10 dBm to 10 dBm for both logic OR and logic AND. The following are the parametric results obtained:

1. Contrast Ratio (CR): To prevent the degradation in output power level, the CR value has to be high so that there is a perfect distinction between the 'high' and 'low' logic levels at the output.

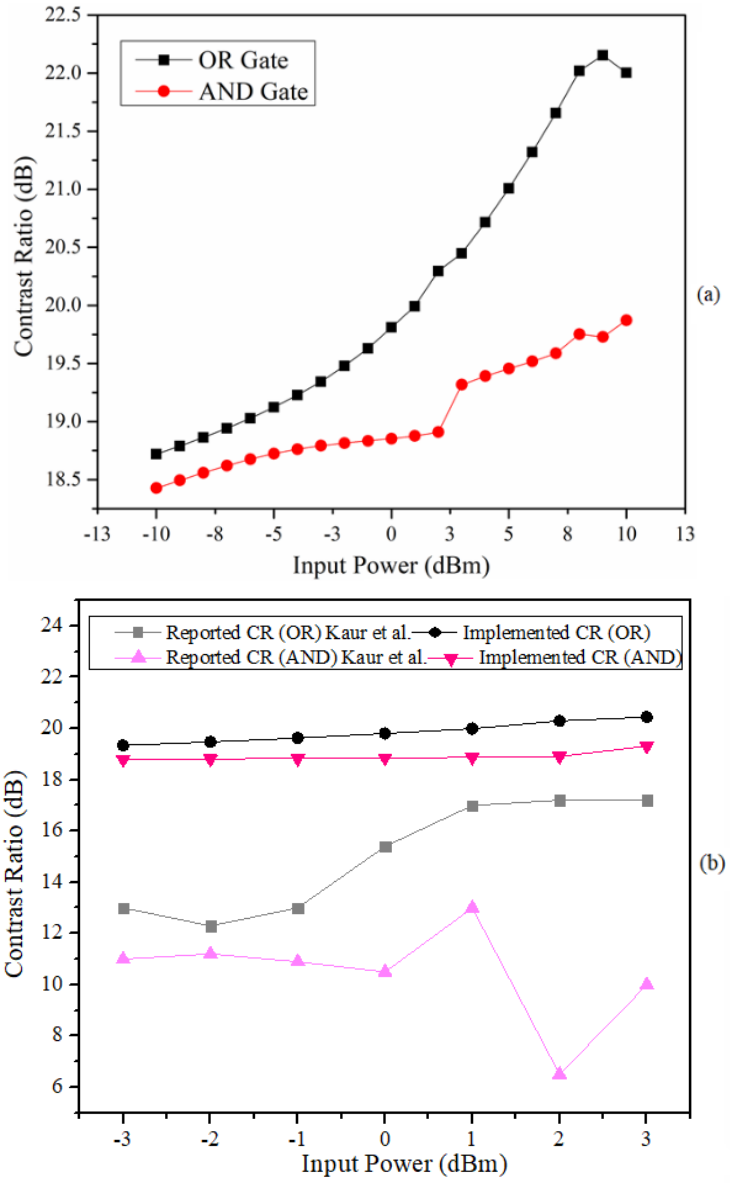


Fig. 7.5 AND-OR results w.r.t. to input power (a) CR and (b) CR Comparison with [193]

The measurement of CR is done by following the formula [191] shown in equation 7.1. Considering 'P_{out_1}' and 'P_{out_0}' as the output power of logic '1' and '0' respectively, then CR is evaluated as:

$$CR = 10\ log_{10}(\frac{P_{out_1}}{P_{out_0}}) \quad 7.1$$

It can be observed from Fig. 7.5 (a) that the OR logic CR stands at 18.72 dB for -10 dBm and 22.01 dB at 10 dBm. The same for AND logic is achieved at 18.43 dB and 19.87 dB for -10 dBm and 10 dBm input power respectively. The comparison graph plotted in Fig. 7.5 (b) has shown improvement in the CR when input power varies between -3 to 3 dBm than the results presented in [193] that utilizes two SOAs instead of EDFA. The following table gives a comparison of the latest technique reported in [191].

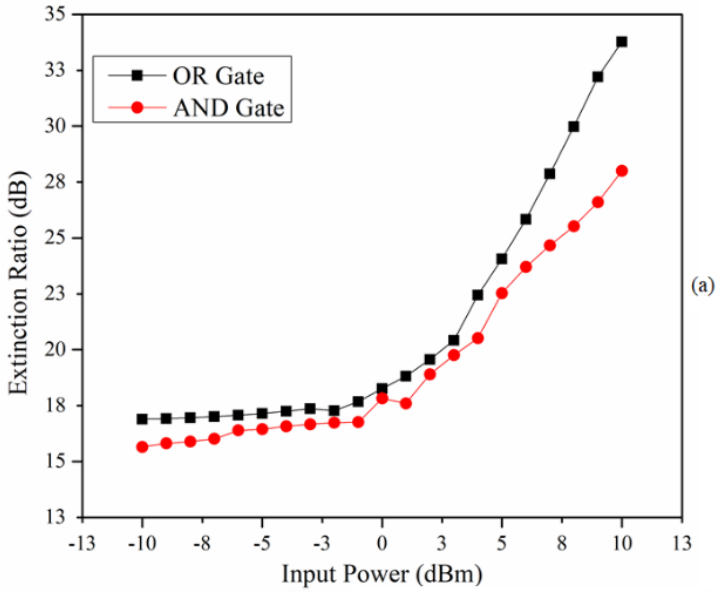
Table 7.2: Comparison of CR value for AND-OR logic

[Scheme] (Year)	**CR (dB)**	
	OR	***AND***
[191] (2022)	11.20	10.5
[193] (2012)	17	10
Implemented	**22.01**	**19.87**

The CR of 22.01 dB for OR and 19.87 dB for AND logic is higher than the reported values in [191] and [193] proves that the superiority of the proposed configuration.

2. Extinction Ratio (ER): The higher values ER has been achieved showing the efficient operation of logic gates. If the 'P_{avg_1}' and 'P_{avg_0}' are the minimum power for logic '1' and maximum power for '0' respectively then ER is evaluated utilizing the following equation 7.2 [190]:

$$ER = 10\ log\ _{10}(\frac{P_{avg_1}}{P_{avg_0}}) \quad 7.2$$



(a)

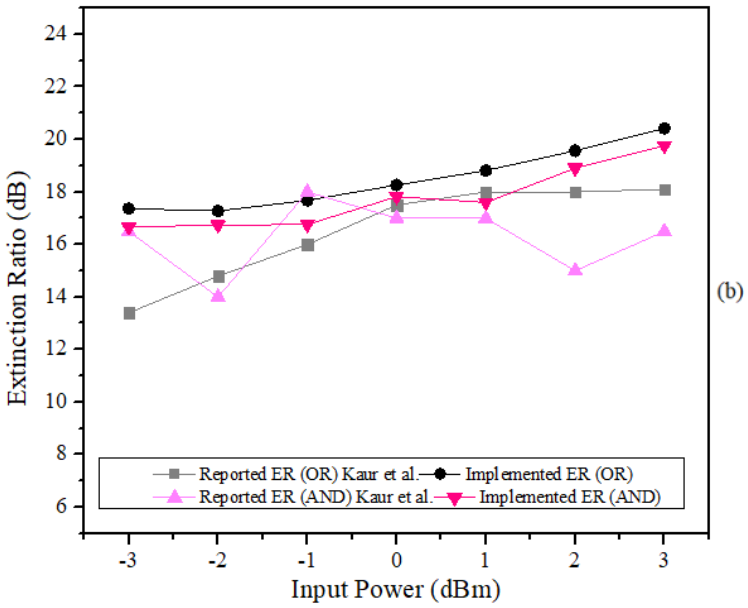


Fig. 7.6 AND-OR results w.r.t. to input power (a) ER and (b) ER Comparison with [193]

Fig. 7.6 (a) shows that the ER value for OR is 16.89 dB and 33.76 dB for -10 dBm to 10 dBm input power. The ER for AND logic surges from 15.65 dB and 27.9 dB for -10 dBm to 10 dBm input power. The further surges in power may increase ER but TWSOA's non-linearity may get worsen. This is why the observation range for input power is varied between -10 dBm to 10 dBm.

Table 7.3: Comparison of ER value for AND-OR logic

[Scheme] (Year)	**ER (dB)**	
	OR	***AND***
[184] (2021)	27.8	-
[192] (2022)	24.10	-
[188] (2015)	9	11
Implemented	**33.76**	**27.9**

The comparison in Fig. 7.6 (b) elucidates that the proposed schemes can lessen the non-linear effects of TWSOA with the incorporation of EDFA and hence bring out the higher ER values. The maximum value achieved for OR logic at 3 dBm is 20.42 dB whereas the reported value in [193] is 18.1 dB. For AND logic, the proposed structure has ER of 19.75 dB, and the reported value is 16.5 dB and 3 dBm of input power. The comparison with the latest literature is shown in Table 7.3 where the higher implemented values show the excellency of the proposed configuration.

3. Insertion Loss (IL): The IL factor gives the measure of attenuation lying between the transmitted

and received signal. This can be evaluated by input and output power i.e. 'P_{input}' and 'P_{output}' respectively as given in the following equation 7.3 [192]:

$$IL = 10\ log_{10}(\frac{P_{input}}{P_{output}}) \quad 7.3$$

It can be observed from Table 7.4 that the IL value of 1.47 for OR and 2.89 dB for AND logic has been achieved for the proposed logic which is much lower than the previously reported values in [184] and [191].

Table 7.4: Comparison of IL value for AND-OR logic

[Scheme] (Year)	**IL (dB)**	
	OR	***AND***
[184] (2021)	1.63	-
[191] (2022)	-2.076	3.059
Implemented	**1.47**	**2.89**

The lower IL values achieved for the demonstrated scheme prove that the structure is better for utilizing in the DC networking applications.

7.6 Conclusion

This chapter focuses on providing the best routing solution for CPI problems in data centers. The proposed OR-AND gates-based smart traffic routing scheme proves good in terms of CR, IL, and ER. The route allotment is made by utilizing priority signals from the received connection requests and machine control signals. The allocation decision-making is done on either a primary or secondary basis depending on the priority of the signal. It is observed that CR for OR and logic AND is higher than 19.5 dB proving to be efficient and excellent in performance. The evaluated ER for AND logic and OR logic are27.9 dB and 33.76 dB respectively while it achieves the lower values of IL as 2.89 dB and 1.47 dB respectively. This evidences the superiority of the proposed routing arrangement when compared with previous reported techniques.

CHAPTER 8
CONCLUSIONS, RECOMMENDATIONS, AND FUTURE SCOPE

8.1 Conclusions

The increasing user-traffic with the proliferated flow of big-data demand real-time switching with minimum possible error to guarantee the quality of service. The motive of this thesis is to present various existing data center switching architectures and explore their limitations and challenges to handle the increasing number of users and hence to provide a solution for the same. The photonic interconnect-based switching technology has been investigated by monitoring various performance parameters and the non-linearities that effect the final output of the system. The major parameters are focused on removing the issues of high latencies, load-balancing problems, and power inefficient outputs and hence proposing an improved switching structure for the complex HPC systems in DC networking. The significant results presented in the thesis are summarized as follows:

1. The various photonic switching structures have been explored for HPC systems in DC networks and the current requirements of DCs have been highlighted. Concerning the overall performance of the system, the use of a semiconductor optical amplifier in Mach Zehnder Interferometric configuration for switching purposes proved to be the most efficient technique despite their non-linear effects. Out of all possible SOA-MZI combinations, the XPM property of TWSOA in symmetric MZI form shows superiority in terms of BER, extinction ratio, and power efficiency. With the use of this elementary 2×2 TWSOA-SMZI block, the 4 input 4 output interconnection has been proposed for switching operations. The crossbar 4×4 structure is tested at a 10 Gbps data rate with a minimum port spacing of 100 GHz which exhibits 96% wide opening of an eye with switching time ranging between 0.146-0.243 ns. The parametric performance was consistent for 2×2 and 4×4 in terms of output power, EOF, OSNR, latency, and Q-factor which proved that the radix-increment can be tested further for attaining a large number of users.

   The structure is further analyzed for scalability by increasing the port capacity from four to eight. The proposed 8×8 crossbar interconnected all-photonic switch is designed with 3-stages where the first and last stage is designed with 2×2 elementary blocks and the middle stage

utilizes a 4×4 configuration for making all the 8×8 interconnections. The structure is also tested for power efficiency by monitoring the power penalty while switching the data. The parametric changes are observed for various input powers ranging between -5 dBm to +5dBm and the effect of varying injection current on the error rate is also explained. The results are then optimized for the suitable injection currents of TWSOA and input signal power. The highest quality factor of 26.5881 and maximum extinction ratio of 19.9 dB authenticates the proof of it is capable of handling the increasing load with high power inputs. The optimized results of BER, eye-opening, OSNR, latency and output power are observed to be consistent for 2×2, 4×4, and 8×8 architecture which indicates its scalability capability for DC networking.

2. The non-linearities in photonic networks can degrade the performance of the system by adding crosstalk, noise, refractive index modifications, and many others. This effect of non-linearities has been presented in two parts: First part shows an analysis of non-linear crosstalk and later includes the effect of in-built non-linearities i.e. polarization sensitivity of SOA in the proposed configuration. It is observed that the logic level in the signal has its significance as varying binary input sequences can add more to the error during transmission. The occurrence of '0' and '1' logic in an input sequence can have an adverse effect on the crosstalk when the system has lower port spacing. The high logic is also noticed to change the crosstalk effect with its occurrence at consecutive and alternative places in the input bit sequence. This effect is first modelled and analyzed theoretically with the gain changes in TWSOA and the UDBS and PRBS generators are utilized to present the effects of logic level on BER, crosstalk, and extinction ratio. The obtained results are compared to that of existing architectures that recommended the proposed arrangement with minimum crosstalk of -39.51 dB. The results are then optimized for various operating wavelengths to achieve high quality service.

   The later part focuses on the monitoring of polarization effects on the output signal utilizing the major factors like Stokes parameters and Poincaré sphere. It is perceived that as long as the polarization dependability of SOA is ignored, the MZI-based SOA switching configurations give reliable results. Hence, the study of cross-polarization modulation of SOA becomes an important factor. The solution to this problem is proposed and the implemented structure is upgraded for attaining improved results. The utilization of EDFA in the middle stage of the 8×8 structure provides refined results. Firstly, the effect of polarization sensitivity of TWSOA

in terms of Stokes parameters with a device angle rotation of 45 degrees is perceived. A large number of spatially distributed points on the Poincaré sphere represent the disturbance in the signal at that instance. It is perceived from the results that SOA-MZI-based structure has adverse effects that the switching is done with the utilization of EDFA in the loops. Hence, the upgraded S-E-S i.e. SOA-EDFA-SOA switching interconnected configuration provides better results when compared with basic SOA-MZI switches. The good signal strength with an output power of 14.817 dBm and conversion efficiency of -27.12 dB with 0.8 THz of port spacing is received. The structure is also evaluated on polarization dependent loss which comes out to be 1.0045 dB and such lower PDL shows the trustworthiness of improved configuration for data center switching networks for reliable results.

3. The proposed structure is further explored for smart switching purposes in DC to reduce the delays due to busy paths in terms of distance, error, and occupancy. This requires an innovative introduction of a deep learning model for predicting the best possible port-path combination out of all possible interconnections available for switching the data to the desired destination. The extended recurrent neural network (RNN) i.e. Long-Short-Term-Memory (LSTM) network is parallelly incorporated with the proposed S-E-S switching configuration. This LSTM introduction is investigated in two ways. In the first part, the LSTM network is trained on all port-path combinations possible with the knowledge of distance and minimum bit error of the path realized in the ideal conditions and the NN predicts the minimum distance path with minimum possible error for switching purposes. The testing of the neural network is evaluated on the parameters like confusion matrix and classification accuracy. This prediction analysis provides the classification of paths with an accuracy of 99.5 % proving to be better than other existing prediction models. The switching parameters like switching time, extinction ratio, BER, and eye-height are also improved when the system knows the minimum distance low error switch-path. But this method doesn’t predict if the chosen path is available for switching at that time.

   In the second part, the limitation of the above analysis is removed and the LSTM network is again trained with additional information on existing power in the path that tells the networks whether the path is available for transferring the data. It classifies the data in terms of availability first by utilizing the information of threshold i.e. average power of path, then the

final classification is followed based on minimum distance and low error. The batch loss and RMSE during the learning process are first optimized for a number of 1000 and 2000 epochs. This way of prediction gives an accuracy of 96.88% and a classification accuracy of 99.7%. The reliability of this model is further evaluated on various factors like precision, true and false positives, true and false negatives sensitivity, specificity, and negative prediction value. This DL-based approach of switching the data to a particular desired destination with the knowledge of available paths yields improved results with a latency of 0.35 ns and throughput of 96 Tbps. This structure hence shows its superiority for DC challenges of fast operation with high throughputs.

4. The DC networks with HPC computations have three-stage hierarchies with a control plane interface (CPI) that controls the flow and scheduling of data from the lower level to the upper ToR. To minimize the limitations due to centralized control, the routing mechanism is proposed for CPI in DCs. The priority bit signal from the header is fed to the AND-OR-based logic routing network and transfers the request to the next stage in accordance with the priority of the message. The OR-logic is used for priority messages and AND-logic is utilized for messages that can wait for an important message to pass through. The logic system is tested on the parameters like insertion loss, contrast ratio, and extinction ratio. The proposed routing scheme keeps SOA non-linearities to a minimum level by mitigating them with the addition of EDFA in the routing network.

Therefore, the study establishes a solution to various challenges of existing DC switching architectures employing high performance computations by introducing an 8×8 interconnecting photonic switching structure utilizing TWSOA-EDFA-TWSOA in SMZI configuration by parallelly incorporating the deep learning LSTM model. It also puts a smart routing strategy for CPI in DC for removing centralized control problems.

8.2 Recommendations

Based on the above research work presented in this thesis, the following are some of the possible recommendations:

1. The proliferated internet users have created a load-balancing problem and also escalated the demand for accommodating their data traffic with networks that have the capability to scale up accordingly. The proposed photonic switching configuration is capable of handling this increase with its potential for scalability. Since the implemented results are reliable and consistent for low to high port-radix with low port spacing, the structure is recommended for scalable data center networking.

2. With the installation of large data centers by popular social networking organizations, large production in minimum time is expected to give the best quality of service to customers. The proposed scheme mitigates all possible issues that affect the output signal in terms of error, and non-linearities, and offers high throughput, and minimum latency with efficient performance. Therefore, it can be recommended for high-speed configurations in high performance computing systems.

3. The high-power demands of high-performance core switches have always been a critical issue. The implemented design works efficiently at high power and reduces the power penalty to the minimum possible value. Thus, the applicability of structure can also be observed for power-efficient hyper-scale infrastructures for fast data transfer.

4. For mass processing of data generated every second, the introduction of an artificial intelligence-based LSTM model in parallel to the proposed switching design can offer good prediction and classification for energy-efficient routes.

5. The connection allotment feature of the proposed logic-based routing mechanism is not only for CPI in data centers, but it is also applicable for IP allotment problems in cloud-based techniques for smart-traffic management. It is applicable in WDM-based routing assignments as well.

8.3 Future Scope

The implemented research can further be explored on particular factors in the future as follows:

1. The estimations by ITU and Mordor Intelligence show that the number of users will surge and the installations of DCs will be extended to accommodate this increase in traffic. Hence, the future for the proposed structure will be to explore higher data rates of 20 Gbps or more to improve the reach of these systems.

2. The research presented utilizes the bias source for TWSOA and fiber doped pump for EDFA. This work can be further investigated for introducing a way of providing an external pump to these hybrid amplifiers from a single source to reduce the cost of the system.

3. The proposed configuration utilizes a three-stage structure for eight port interconnections which further has three stages for four port interconnections in the middle. Hence, the structure can be further explored for reducing the stage-hierarchy by keeping the feasibility of scalability monitored.

4. The number of SMZI loops in the implemented design will continue to increase with the increase in input and output ports. This loop-factor can be explored to minimize the complexity of high-radix systems.

5. The CPI routing algorithm can be further extended with a proper software-based interface that can inform about the incoming dynamic traffic per IP in an instant. This area of research will add more efficient outcomes of routing the dynamic traffic in data centers without centralized control, unlike SDN technologies.

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