Analysis of Depletion Region Width, Breakdown Voltages and Power Dissipation of Uniformly doped and Linearly Graded 3C-SiC Schottky Barrier Diode

Dissertation submitted towards the partial fulfillment of requirement for the award of degree Of

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CERTIFICATE

I hereby certify that the thesis entitled "**Analysis of Depletion Region Width, Breakdown Voltages and Power Dissipation of Uniformly doped and Linearly Graded 3C-SiC Schottky Barrier Diode**" is an authentic record of my study carried out as requirement for the award of degree of Master of Engineering in Electronic and telecommunication at Thapar University, Patiala, under the supervision of Dr. A.K. Chatterjee, Professor, Electronic and Telecommunication Engineering Department, Thapar University, Patiala.

I have not submitted the matter presented in the Thesis for the award of any other degree to any other university.

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ABSTRACT

Silicon carbide is a wide band gap semiconductor material so it is highly suitable for high temperature, high power and high-frequency device applications. Wide band gap semiconductors are capable of electronic functionality at much higher temperatures than silicon. The leakage current of SiC is many orders of magnitude lower than that of silicon due to its wide band gap.

There are different crystal structures of SiC. These are 2H, 3C, 4H and 6H; but the most important are 3C, 4H and 6H. These structures differ by band gap, carrier mobility and breakdown electric field. SiC was originally produced by a high temperature electro-chemical reaction of sand and carbon. Schottky barrier diodes (SBDs) have many benefits compared to other rectifying devices, for example fast switching speeds and relatively easy fabrication.

The present work aims at the design of SiC Schottky Barrier diode with high breakdown voltage and lower power dissipation and study the effect of power dissipation, critical electric field, breakdown voltage, specific on resistance for uniformly doping profile and linearly graded drift region. At the different value of current density Jon. By using linearly graded drift region, it is possible to design thinner devices with higher breakdown voltages and low Power dissipation.

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A	Area of the diode
A*	Richardson constant (cm-2K-2)
E_v	Valence band energy level (eV)
E_C	Energy level of the conduction band (eV)
E_F	Fermi level Energy (eV)
E_{FM}	Fermi level of the metal (eV)
EG	Band gap energy (eV)
Ei	Intrinsic energy level (eV)
E_{vacuum}	Energy of the free electron (eV)
I_0	Saturation current (A)
I_F	Forward current (A)
J_{on}	Current density (A-cm-2)
K	Boltzmann constant (J/K)
Ks	Dielectric constant
α	Gradient
N_A	Acceptor doping concentration (holes/cm3)
N_D	Donor doping concentration (electrons/cm3)
q	Electron charge (Coulombs)
R_{on}	On resistance (Ω-cm2)
Rs	Sheet resistance (Ω)
T	Temperature in Kelvin (K)
V_a	Applied bias voltage (V)
V_{bi}	Built- in potential (eV)
W	Width of the depletion region (cm)
ε_0	Permittivity of the material (F/m)
χ	Electron affinity (eV)
Φ_B	Schottky Barrier Height (eV)
Φ_m	Metal work function (eV)
Φs	Semiconductor work function (eV)
α′	angle of slope of the drift region narrowing (Degree)

CHAPTER – 1

Introduction

1.1 Introduction to SiC

Silicon carbide (SiC) is a semiconductor having very large band gap and its properties are highly suitable for devices working at high-power, high-frequency, high-temperature, and in harsh environments, with superior performances compared to silicon-based devices. SiC has high breakdown electric field strength, high velocity of saturation of electrons, and a high thermal conductivity. Moreover, SiC has a great advantage over other semiconductors like silicon (Si). It has silicon dioxide (SiO_2) as its native oxide. It opens up great possibilities for device applications utilizing a metal-oxide-semiconductor (MOS) structure. Therefore, these properties make SiC suited for a large number of applications. The main application for SiC crystals is in power electronics. Silicon is the material currently dominating the electronics industry. However, there is a demand for improved energy efficiency in power electronics, which can be satisfied by reducing the switching and conduction losses of devices, making devices capable of high temperature operation. Recently, the development of modern epitaxial techniques has led to a large improvement in the quality of material of SiC, thus leading to a constant increase in the performances of SiC based devices.

Compared with electronic devices fabricated in Si, electronic devices fabricated in SiC enable a significant reduction of electrical loses, sizes and weights of the electronics modules, with improvements in efficiency and cost.

Nowadays the main applications of SiC based electronic devices include aero-space (high temperature engines, radiation hard devices), transportation (power supply, power switching and power module), industry (power supply) as well as communications (radio frequency (RF) switching) and renewable energies (e.g., power conversion in solar and photovoltaic plants).

The advantages of SiC over Si based power devices can be summarized as follows:

- SiC unipolar devices are thinner, and they have lower on-resistances, which results in lower conduction losses and higher overall efficiency.
- SiC based power devices have higher breakdown voltages because of their higher critical breakdown electric field.
- SiC has higher thermal conductivity (4.9 W/cm-K for SiC and 1.5 W/cm-K for Si), meaning that SiC power devices have a lower thermal resistance and the device heating rate is slower, also enabling size reduction in the cooling systems of power applications.
- SiC can operate at higher temperatures (up to 1000°C compared to 150°C for Si).
- SiC is extremely radiation hard and therefore suited for aerospace applications, by decreasing the additional weight from radiation shielding.
- Because of low switching losses, SiC based devices can operate at high frequencies (> 20 kHz) which is not possible with Si based devices in power levels above a few kilowatts.[1]

1.2 History of SiC

For growing high quality crystals, Lely presented a new concept in 1955. The research in SiC became more intensified after this and the first SiC conference was held in Boston in 1958. However, the success and rapid increase of the Si technology caused the interest in SiC to drop, and the SiC research activities in the 1960 to the late 1970 were scarce. The next big break came in 1978, with the invention of the seeded sublimation growth by Tairov and Tsvetkov [2] that led to the birth of SiC wafer growth. By introducing a seed crystal and forcing material transport from the source to the seed by a thermal gradient, the growth rates could be increased and seeds of larger diameters and lengths could be made. The produced boules could be sliced and polished into wafers.

In 1987, another breakthrough came with the “step-controlled epitaxy” on off-axis substrates [3], which meant that high quality epitaxy could be conducted at low temperatures. In light of this milestone, Cree Research was founded in 1989 and became the first company sell SiC

wafers, and Cree has remained the biggest player to this day when it comes to SiC substrates. This was the beginning of a wave of interest for SiC that is yet to subside.

In 2001, Infineon launched its Schottky diode product line made from SiC and Cree also has Schottky diode as well as high-frequency MESFETs on the market. In August 2010, CREE announced 6" 4*H*-SiC wafers. In 2012 HOYA Corporation succeeded in increasing growth rate of SiC more than 50 times the conventional rate by the use of newly developed SiC fabrication process [33].

1.3 Crystal structure

1.3.1 Basic building block

Silicon carbide is a tetrahedrally bonded compound and made up by Si and C atoms (both group IV element materials) in a 1:1 ratio. Each Si atom shares electrons with four C atoms, so that each atom is 88% covalently and 12% ionically bonded to four nearest neighbors. The approximate distances between Si-C and Si-Si or C-C atoms are 1.89 Å and 3.08 Å, respectively [4,5]. The basic building block of a silicon carbide crystal is the tetrahedron of four silicon atoms with a carbon atom in the center. The SiC tetrahedron is schematically illustrated in Fig. 1.1

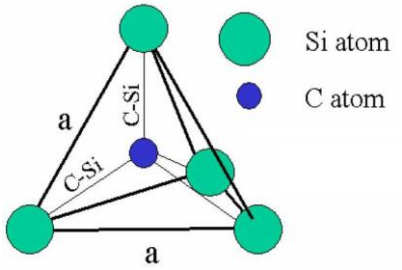

Figure 1.1- Tetragonal bonding of a central carbon atom with the four nearest silicon neighbors. Two types of tetrahedrons can nucleate, where one is rotated 180° around the *c*-axis with respect to the other.

1.3.2 Polytypism

The phenomenon of the same material crystallizing in different modifications is called polymorphism. The existence of different crystalline modifications of SiC was discovered in 1912 [6]. However, since SiC exhibits a particular two-dimensional

polymorphism, the different SiC modifications were later named polytypes [7]. The various polytypes, which can exist in cubic (C), hexagonal (H), and rhombohedral (R) crystal structures, share the same chemical composition but they have different electrical properties.

All the known polytypes of silicon carbide crystallize according to the laws of close spherical packing give structures constituted by identical layers. All polytypes have a hexagonal frame of SiC bilayers. Viewed as layers of spheres of the same radius, the hexagonal frame takes on the shape in Fig. 1.2. The SiC bilayers are the same for all planes of lattice. However, the relative positions of the adjacent planes are slightly shifted to fill the voids in the adjacent layer in a close-packed arrangement. Then, as seen in Fig. 1.2, there are three possible inequivalent positions for the spheres. Referring to the possible positions as A, B, and C, the different polytypes can be built. Thus the only cubic polytype in SiC, called 3*C*-SiC, has the stacking sequence ABCAB. The simplest hexagonal structure, called 2H-SiC, has the sequence ABA. The two important hexagonal polytypes, 6*H*-SiC and 4*H*-SiC, take on the sequences ABCACBABCACB, and ABCBABCB, respectively. The number in the notation refers to the number of layers before the sequence repeats itself [8].

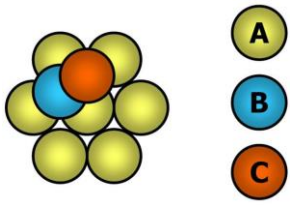

Figure 1.2- Schematic positions of atom centers for a close spherical packing. Only three possible positions exist for the SiC tetrahedron centers—A, B and C.

1.4 Outline of the thesis

Chapter-1 Introduces the reader to the world of silicon, gives the limitations imposed by silicon across a wide spectrum of applications and further suggests the new material, Silicon Carbide.

Chapter-2 Starts with the physical and electrical properties of SiC, The chapter also surveys the SiC material growth, SiC technology, its polytypes (3C, 4H, 6H etc), properties and its applications.

Chapter-3 Literature Survey

Chapter-4 In this chapter starts with the Schottky barrier diode, working of Schottky barrier diode and its limitation.

Chapter-5 The formulation for uniformly doping profile for 3C-SiC Schottky barrier diode , Calculation of $R_{on\text{-}sp}$, power dissipation, critical electric field and for the Avalanche breakdown voltage.

Chapter-6 Presents the formulation & calculations for linearly graded drift region for Power dissipation, for the depletion region width and doping concentration N_{eff} It then presents the stability in the Avalanche breakdown voltage nearly closed to the punch through voltage.

Chapter-7 Includes Results and Conclusions.

Chapter-8 Includes further improvement which is possible.

CHAPTER – 2

Properties of Silicon Carbide

2.1 Physical properties of Silicon Carbide

SiC polytypes different lattice parameters, when passing from cubic 3C – SiC to the polytypes with hexagonal structure. Different polytypes has different values of densities. The atomic density of SiC unit cells is larger than other semiconductors such as Si (together with the very short bond length between Si and C atoms and the strong bond). Thermal conductivity of SiC is very high so it is a good candidate for the fabrication of devices working in high temperature conditions and with the need of good power dissipation. SiC devices operating in harsh environments can be successfully fabricated because they have high chemical inertness of the material. A comparison between SiC and other semiconductors for what concerning the physical properties reported in Table 2.1[9,10]

Table 2.1: Physical properties of 4H and 6H – SiC polytypes compared with other semiconductors

Property	4H-SiC	6H-SiC	Si	GaAs
Bond length (Å)	1.89	1.89	2.35	2.45
Density (g/cm^3)	3.2	3.2	2.3	5.3
Thermal conduct. (W/cm K)	5.0	5.0	1.5	0.5
Melting point (°C)	2830	2830	1420	1240

2.2 Comparison of Electrical Properties

Table 2.2: Comparison of electronic properties of major SiC polytypes, Si and GaAs [11].

Property		**Si**	**GaAs**	**6H-SiC**	**4H-SiC**	**3C-SiC**
Band Gap(eV)	E_g	1.1	1.142	3.0	3.26	2.2
Breakdown Field (MV/cm)	E_c	0.6	0.6	3.2	3.0	1.5
Electron Mobility (cm^2/V-s)*	M_n	1100	6000	370	800	750
Hole Mobility (cm^2/V-s)*	M_p	420	320	90	115	40
Dielectric Constant	ϵ_r	11.8	12.8	9.7	10	9.6
Saturated Electron Drift Velocity (cm/s)	V_{sat}	10^7	10^7	$2x10^7$	$2x10^7$	$2x10^7$
Intrinsic Carrier Concentration (cm^{-3})	N_i	$1.5x10^{10}$	$1.9x10^{10}$	$2.3x10^{-6}$	$8.2x10^{-9}$	6.9
Thermal Conductivity(W/cmK)	Λ	1.5	0.5	4.9	4.9	5

2.2.1 Band gap

The band gap is a forbidden zone in the energy spectra for a crystal. For metals bang gap is zero and for insulators band is very large. A semiconductor has a band-gap up to a few eV. For some traditional semiconductors the band gaps are: 1.11eV for Si, 0.7eV for Ge, and 1.4eV for GaAs. Many of the favorable transport parameters in SiC are related to the large band-gap, which is of the order of 3eV. For such a large band gap the intrinsic carrier concentration is negligible at temperatures up to 600^0C. The intrinsic carrier concentration is responsible for the thermal noise, and also partly responsible for the leakage current, which are

both very small in large band-gap materials. The minimum energy required to create an electron-hole pair is equal to the band-gap that in SiC falls within the 3eV range corresponding to a photon with wavelength close to 400 nm. SiC devices are thus also insensitive to the main part of the visible spectrum, making SiC suitable as a detector material for UV radiation with minimal noise from the visible background [12].

2.2.2 Critical Electric Field

One of the most important properties for power-device applications is the critical electric breakdown field, E_C. This property determines maximum electric field that the material can support before suffering physical breakdown. Normally, wide bandgap materials have a high breakdown electric field because the wide bandgap leads to high impact ionization energy. Silicon carbide can withstand an electric field about ten times greater than GaAs or Si without undergoing Avalanche breakdown [13]. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors or high power microwave devices [14]. In addition, it allows close distances between adjacent devices, allowing high device packing density for integrated circuits. The breakdown voltage at a *p-n* junction is given by:

$$V_B = E_c W_d / 2$$

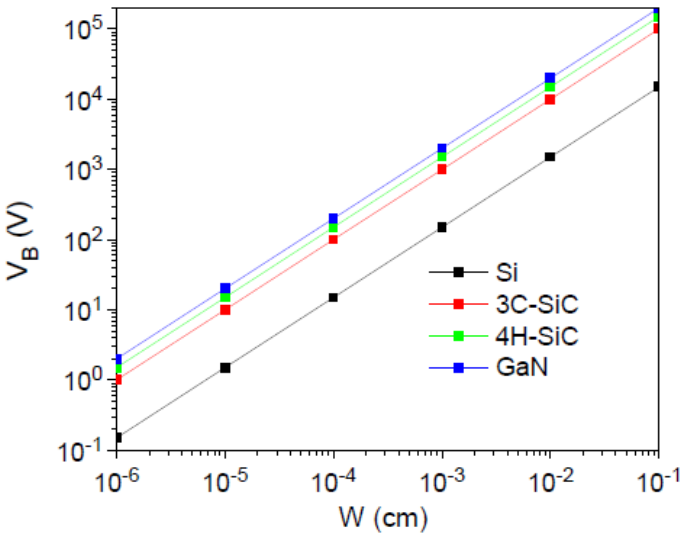

Figure 2.1- Breakdown voltage as a function of drift region width for Si, 3*C*-SiC, 4*H*-SiC and GaN

where V_B is the breakdown voltage, and W_d the drift region width. Considering the same breakdown voltage, a significantly thinner drift region can be realized in SiC compared to Si.

The relative strength of E_C for SiC compared to Si of ten times refers to devices designed for the same blocking voltage. For a doping of approximately 10^{16} cm^{-3}, E_C for 4*H*-SiC is 2.49 MV/cm. For Si, the value of E_C is about 0.401 MV/cm for the same doping [15]. In this comparison, the difference between SiC and Si is only about a factor of six and not the often advertized factor of ten. However, if one compares the critical strengths of devices made for the same blocking voltage, then a Si device constructed for a blocking voltage of 1 kV would have a critical field strength of about 0.2 MV/cm, which, when compared with the 2.49 MV/cm of SiC, amounts to the factor of ten. In Fig. 2.1, V_B is shown as a function of the drift region width for different materials.

2.2.3 Saturated Electron Drift Velocity and Carrier mobility

For high frequency devices, a very important parameter is the saturated drift velocity v_s. It is one of the key material and device properties that determine the ultimate limit of speed of response and frequency of a device, such as a transistor. In a semiconductor, carrier velocity cannot indefinitely increase with the applied electric field. Carriers speed up in response to a stronger field until the saturation drift velocity is reached. At this point, higher fields do not result in any increase. In SiC, the saturation drift velocity is 2-2.7 × 10^7 cm/sec [16], which is at least twice that of Si. A high-saturated drift velocity is advantageous in order to obtain as high channel currents and high frequencies as possible, and clearly SiC is an ideal material for high-gain, and high-speed solid-state devices. Electrons and holes are accelerated by electric fields, but they lose momentum as a result of various scattering processes, such as lattice vibrations (phonons), impurity ions, crystal defects, surface or other material imperfections [17]. The drift velocity v_d of a carrier is proportional to the electric field E, provided that v_s has not been reached. The mobility μ is defined as the proportionality factor between v_d and E as

$$\mathbf{V_d = \mu E} \qquad 1.1$$

The effects of all several microscopic phenomena are lumped into the macroscopic mobility introduced in the transport equations. The mobility is dependent on the local electric field, lattice temperature, doping concentration, polytype, crystal quality, local scattering at defects, etc. If the

doping concentration increases, the mobility decreases due to scattering. For low doping concentration, the mobility decreases with temperature due to decreased vibrational energy of the lattice phonons [18,19].

2.2.4 Impact Ionisation

For high-power devices the impact ionization process is very important. It is important for accurate predictions of the high power performance. Measurements reported a positive temperature coefficient of the impact ionization coefficient. As the impact ionization heats the lattice, so it further increases the impact ionization. This is a very serious problem, causing local hot spots, unstable operation and thermal runaway, destroying the device.

2.3 The interest in cubic silicon carbide (3*C*-SiC)

First of all, due to cubic crystal symmetry of 3C SiC it is the only polytype with isotropic properties. 3*C*-SiC has a larger saturated drift velocity than both 4*H*- and 6*H*-SiC polytypes, and more than twice that of Si, which is advantageous for obtaining higher channel currents in microwave devices [20]. Furthermore, among the three most stable SiC polytypes, 3*C*-SiC has the highest bulk electron mobility. The carrier mobility influences the frequency response or time response behavior of a device in two ways. First, the mobility is proportional to the carrier velocity for low electric field. Therefore, a higher mobility material is likely to have a higher frequency response, because carriers can move more readily through the device. Second, the device current depends on the mobility i.e. higher mobility results in larger currents. At larger currents, the capacitance charges faster, leading to a higher frequency response [21]. An interesting future device application for 3*C*-SiC is as a metal-oxide-semiconductor field effect transistor (MOSFET) for high current and high voltage switching applications. Such application requires small donor ionization energy and low density of traps at the interface semiconductor/oxide interface. SiC in general has a great advantage over competing compound semiconductors in the possibility to easily grow silicon dioxide (SiO2) by thermal annealing in an oxygen ambiance. However, in hexagonal polytypes the interface state

density is high at the SiO_2/SiC interface, which leads to low inversion channel mobility in MOSFET devices [22]. On the other hand, using the 3*C* polytype, these interface states are located inside the conduction band due to its lower bandgap [23]. It should lead to superior inversion channel mobility in MOSFETs.

In recent years, the world's interest in the fabrication and study of heteropolytype structures based on SiC has considerably increased. Palyakov *et al.* [24] has demonstrated theoretically the possibility of high electron mobility transistor (HEMTs) in a hetero polytype junction β/α (3*C*/4*H* or 3*C*/6*H*). This study predicted the formation of a two-dimensional electron gas (2DEG) at such interface with superior potential for high electron mobility transistors (HEMTs) compared to the better studied AlGaN/GaN hetero system [24,25].

The properties that make especially the hexagonal to cubic SiC interface interesting can be summarized as follows:

1. The large difference in the bandgap between cubic and hexagonal polytypes lies almost entirely in the conduction band, yielding large conduction band offsets (ΔEc 3*C*/6*H* = 0.7 eV and ΔEc 3*C*/4*H* = 1.0 eV).

2. The abrupt change in spontaneous polarization between the polar 4*H*/6*H* polytypes and the non-polar 3*C* polytype leaves fixed positive charge on the C-face of the hexagonal structure, introducing an electric field at the interface which causes an accumulation of free electrons to form a 2DEG in the zinc blende 3*C*, confined by the large band offset. 3. The next to perfect lattice matching should enable the growth of structurally perfect interfaces with no stress relaxation induced dislocation defects. These factors combine to open up the possibility for novel quantum-well heterostructures and two-dimensional electron gas (2DEG) high electron mobility transistor (HEMT) devices, based only on the different stacking sequences of chemically identical, but structurally different layers of SiC.

CHAPTER 3

Literature Survey

3.1 Literature Survey

In 1938 that German physicist Walter H. Schottky has given a theory that shows the rectifying behavior of a metal-semiconductor contact as dependent on a barrier layer at the surface of contact between the two materials. Schottky Barrier diodes are later fabricated on the basis of this theory.

In March 1993, Mohit Bhatnagar and B.J. Baliga showed theoretically that an ideal SiC Schottky rectifier can provide a breakdown voltage as high as 5000V with a forward voltage drop of only 3.85V at 300°K for a current density of 100Amps/cm^2.

In 1995, R. Raghunathan showed that breakdown voltage of 1000V can be achieved for 4H-SiC Schottky Barrier Diode.

In June 1995, Akhira Itoh et al. showed that high performance of high voltage rectifiers could be obtained by using 4H-SiC Schottky Barrier diodes. A typical breakdown voltage of 800V could be achieved.[26]

In 1997, the results obtained with limited area amorphisation with argon ion implementation at the periphery of 6H-SiC Schottky Barrier diodes.[27]

Different types of edge termination structures based upon the amorphised implanted region were studied. The termination structures were fabricated using a three-mask process which creates a high resistivity layer at the periphery of the device formed by using high dose argon ion-implantation with its position and area defined by a photoresist mask. It was established that, for obtaining a high breakdown voltage, high resistivity layer should be in contact with Schottky metal. It was showd that only 50 μm of the implant region is required at the periphery to obtain ideal plane parallel breakdown voltages.

In June15, 1998, The release of Schottky Barrier diode, the HSB0104YP containing two diode elements was announced by Hitachi. This product made possible high speed switching

at the pico-second level. It has a reverse voltage of 40V. ROHM developed the ROBOSIL-40 Schottky Barrier diode with an ultra low forward voltage having Backward voltage of 40V, which has provided an extremely low forward voltage of only 0.29V.

In July 1998, Purdue University reported, 4H-SiC SBD's using both Ni & Ti as Schottky metals. These diodes have been fabricated, and they have reverse-blocking voltages of 1720V and 1480V respectively.

In 1999, V.K Saxena et al. fabricated 1kV 4H and 6H-SiC Schottky diodes by the use of a metal oxide overlap structure for electrical field termination. In the same year 1999, Purdue University group fabricated Ni-Schottky diodes on a 50μm epilayer of 4H–SiC. These diodes have blocking voltages as high as 4.9kV.

In 2001, Matthias et.al. explained the models for the electron mobility in 4H, 6H, and 3C-SiC in a paper [28]. Experimental data on mobility and Monte Carlo (MC) results reported in the literature have been evaluated and the results serve as the basis for model development. The proposed models describe the dependence of the electron mobility on temperature, doping concentration and electric field.

In 2002 Royal Institute of Technology, Department of Microelectronics & IT, Stockholm, reported that Schottky rectifiers with SiC are able to replace Si-PIN diodes in 300-3000V blocking voltage range. On 14th May,2002 Nuremberg, Germany, Dynex Semiconductors Ltd, (a leading power semiconductor company) announced that the company has been awarded a research & development grant in a new Program (ESCAPEE) for developinf 3.3KV Schottky Barrier diode technology from SiC. Marinsz et. al. showed the results of investigation of the forward and reverse current-voltage(I-V) characteristics of 4H-SiC Schottky rectifiers with Ni as the contact metal[29].

In 2003, P.Tobias et.al. showed that Metal-Insulator–SiC devices can be used for sensing gas in automotive exhausts, because of the large band gap of SiC it can be operated at high temperature

In 2004 SiC lab of Rutgers University researchers demonstrated 1.79KV, 6.6A 4H-SiC merged PIN-Schottky diodes.In 2005, Performance of the commercially available Schottky Barrier Diode of breakdown voltage of 1.2 kV and Si diodes was compared at high temperature[30]. It was obeserved that SiC Schottky diodes gives better performances for breakdown voltage of 1.2 kV. It can provide better switching time and recovery charge than

PN-Si ultra-fast diodes, although they show slightly higher forward voltage drops. Using Ni instead of Ti for the Schottky contact lower reverse leakage current was obtained.
In 2006, It was discussed that SiC is an energy efficient wide band gap device and it was showed that SiC Schottky diodes allowed up to a 25% reduction in losses in power supplies for computers and servers when used in the power factor correction circuit. For motor control (demonstrated in 3HP motor drive), SiC Schottky allowed a >35% reduction in power loss[31].In 2007 Department of Electrical and Computer Engineering, Purdue University, put up the analysis of Schottky and PIN Diodes on epitaxial 4H-SiC wafers[32].

In 2009, a method to theoretically calculate current-voltage characteristics of Schottky barrier diode was given, using iteration method and C++ programming. The diode equation was split into two functions. Using C++ program, a set of values of current and voltages were generated. The analysis was made using 4H-SiC diode with contacts of Nickel, Titanium & Gold.

In 2012 HOYA Corporation succeeded in increasing growth rate of SiC more than 50 times the conventional rate, by the use of newly developed SiC fabrication process. With this new process, large monocrystal 3C-SiC substrates with at least 200 micro-meters thickness after removing the Si base layer, can be manufactured. HOYA's 3C-SiC substrate has the same geometry as typical Si wafers, So it can be used in conventional Silicon semiconductor device production lines without hardware changes[33].
In 2013 a novel (direct wafer bonding technique) has been reported; Si wafers to polycrystalline SiC carrier wafers. 3C-SiC epitaxial layers have been grown by using conventional chemical vapour deposition techniques above Si/SiC structures. The nature of all of these 3C-SiC epitaxial layers are highly crystalline[34].

CHAPTER 4

Schottky Diode

4.1 Introduction

The earliest systematic investigation on metal-semiconductor rectifying systems is generally attributed to Braun, who in 1874 noted the dependence of the total resistance of a point contact on the polarity of the applied voltage and on the detailed surface conditions. The point-contact rectifier in various forms found practical applications beginning in 1904. In 1931, Wilson formulated the transport theory of semiconductors based on the band theory of solids. This theory was then applied to metal semiconductor contacts. In 1938, Schottky suggested that the potential barrier could arise from stable space charges in the semiconductor alone without the presence of a chemical layer. The model arising from this consideration is known as the Schottky barrier. In 1938, Mott also devised a more appropriate theoretical model for swept-out metal-semiconductor contacts that is known as the Mott barrier. These models were further enhanced by Bethe in 1942 to become the thermionic-emission model which accurately describes the electrical behavior.[36]

4.2 Schottky Barrier Diode

SiC Schottky Barrier diodes (SBDs) or metal-semiconductor diodes are attractive since they provide rectification without significant switching loss. Switching loss occurs when a diode change from the conducting state to the blocking state [37, 38]. Schottky diodes are metal-semiconductor junctions, and conduction current in these devices consists only of electrons injected from the n-type semiconductor into the metal. Since no holes are injected into the semiconductor, there is no stored charge and no reverse recovery transient, so the SBD turns off very rapidly. The reverse current transient of the diode causes power dissipation in other components of the switching system, typically a switching transistor, and this switching loss is attributed to the diode since the current transient is caused by the diode. Substitution of a p-i-n diode by a SBD effectively

eliminates the switching loss. Although Schottky diodes are desirable because of their low switching loss, it is not feasible to build high voltage SBDs in silicon. This is because of the relatively low barrier heights between common metals and silicon. The bandgap energy of silicon is 1.12 eV and the barrier heights of metal contacts to silicon are typically less than 0.5 eV. Under large reverse bias, the barrier is further reduced by Schottky barrier voltages. This is not the case with SiC because it is easy to fabricate SBDs with barrier heights as high as 1.5 eV. Since the reverse current depends exponentially on the barrier height, the reverse leakage in SiC SBDs is orders of magnitude lower than in silicon, even at high voltages [39]. The structure of a metal-semiconductor junction is shown in Figure 4.1. It consists of a metal in contact with piece of semiconductor. Metal- semiconductor junctions are of two types: rectifying and non-rectifying. Rectifying junction forms the Schottky barrier whereas non-rectifying junction forms the ohmic contact. In an ideal ohmic contact, no potential is present between the metal and the semiconductor.

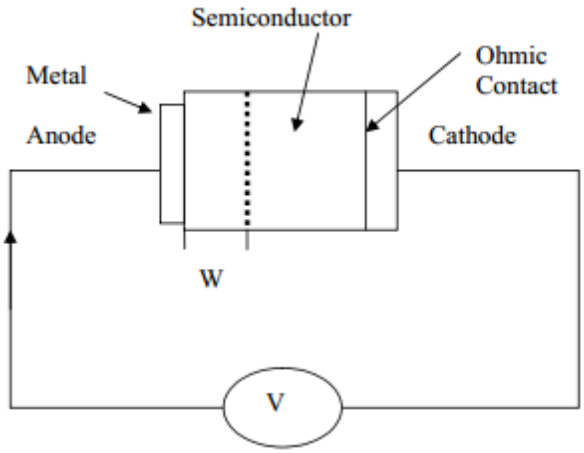

Figure 4.1 Structure of metal-semiconductor junction .

4.2.1 Schottky Barrier Formation

The formation of an ideal Schottky contact depends on the work functions of the two materials i.e. metal and the semiconductor being brought into contact with each other. When a metal and a semiconductor are brought into contact, either a Schottky contact or an Ohmic contact can be formed depending on the characteristics of the interface. Both of these contacts are highly important for solid state research. The type of the contact form is determined by the differencebetween the metal and

the semiconductor work functions. Work function of a metal is the energy required to knock a valence electron from the metal into the free space or vacuum. It is often measured through the use of the photoelectric effect. The metal's work function Φ_m is an intrinsic property and is constant assuming there is no worry of depleting the valence electrons; in other words, there are a lot of metal atoms. Thus, the metal work function Φ_m can be described as vacuum level, Eo, subtracted from the energy level where the valence electrons sit, which is known as metal's Fermi level, E_{fm}. [37]

$$\mathbf{\Phi_m = Eo - E_{fm}} \qquad 1.2$$

Work function of semiconductor Φ_s can be given as:

$$\mathbf{\Phi_s = \chi + (E_C - E_{fs})_{FB}} \qquad 1.3$$

where χ is known as the semiconductor electron affinity and is an invariant property of the semiconductor, E_{fs} is the semiconductor Fermi level with $(E_C - E_{fs})_{FB}$ the difference between conduction band edge and semiconductor Fermi level under flat band conditions. The equilibrium position of the Fermi level in the semiconductor is not an invariant value. It is positioned based on conductivity type and doping concentration meaning that $(E_C - E_{fs})_{FB}$ can be varied. This means that unlike the metal work function, the semiconductor's work function can be varied. When a metal and a semiconductor are brought in contact, the respective Fermi levels must coincide in thermal equilibrium. There are two limiting cases, one is the ideal case referred to as Schottky-Mott limit [40] and other is the practical case referred to as the Bardeen limit [31]. Figure 4.2, 4.3 shows the energy band diagram for the ideal case i.e. Schottky-Mott limit with the absence of surface states.

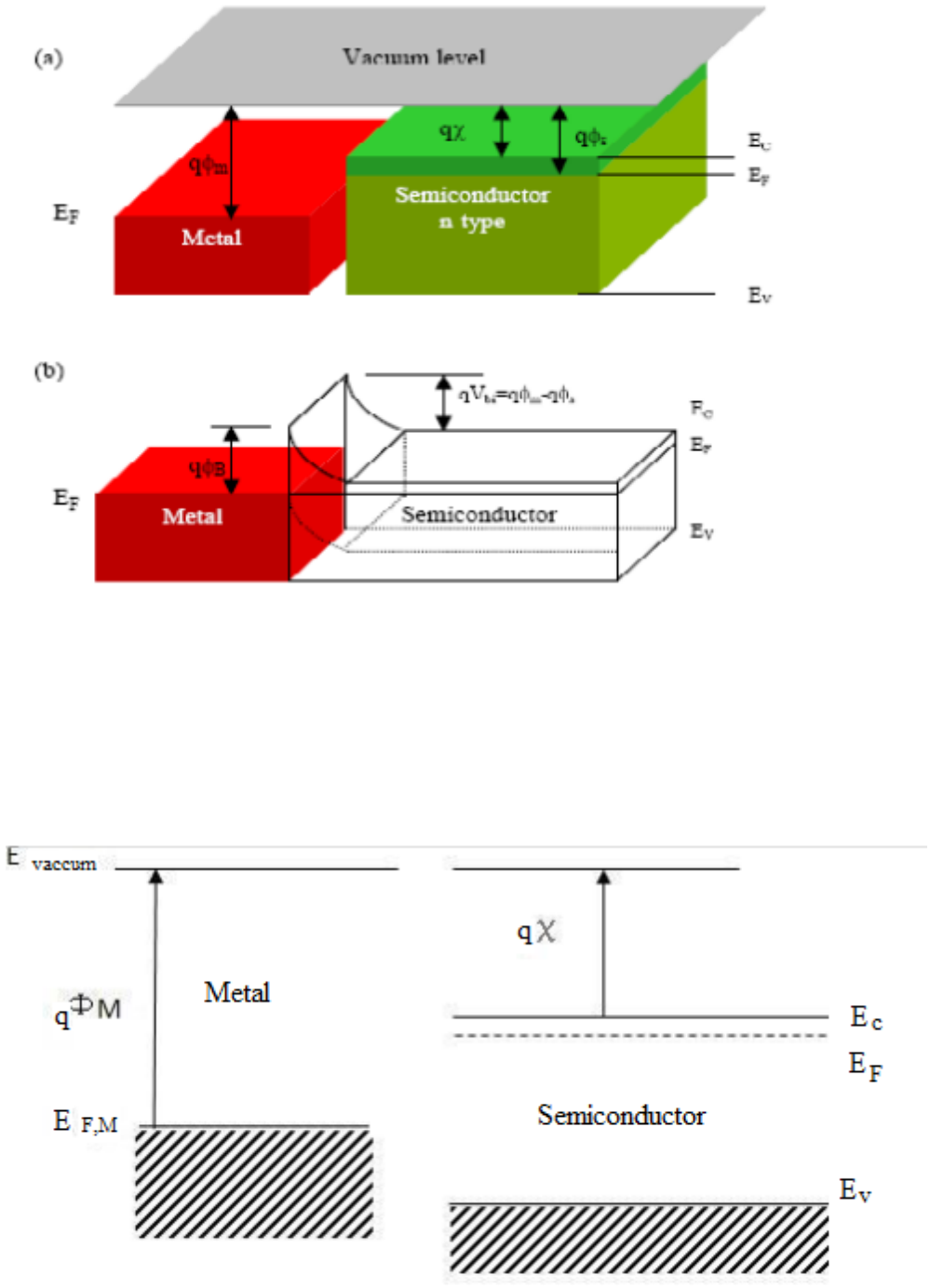

Figure 4.2- Energy band gap of M-S before contact.[40]

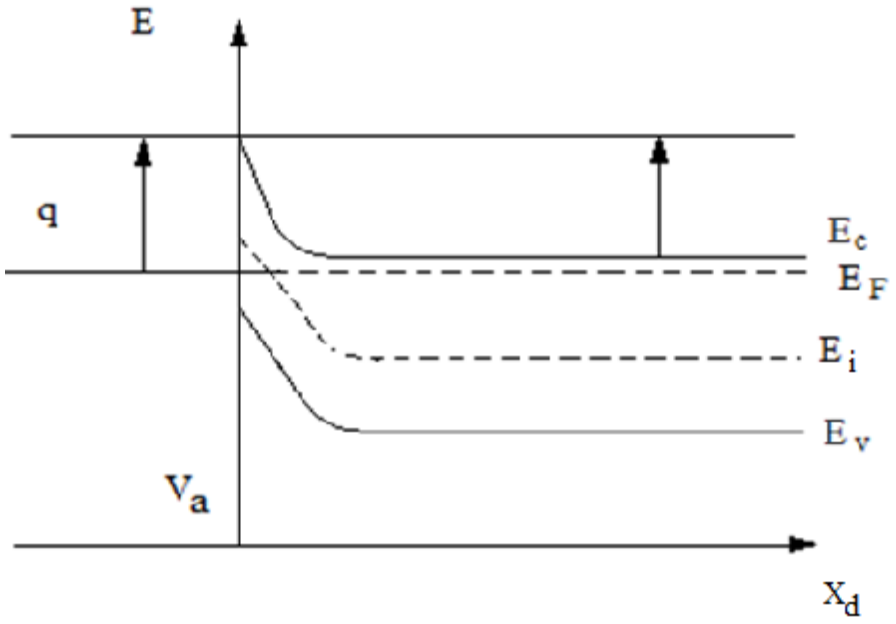

Figure 4.3- Energy band gap of M-S after contact and before thermal equilibrium

In this case the barrier height Φ_{Bn} for n-type semiconductor can simply be calculated as the difference between the metal work function Φm and electron affinity of the semiconductor:

$$q\,\Phi_{Bn} = q(\,\Phi_m - \chi_s\,) \qquad 1.4$$

For a given semiconductor and a metal, the sum of the barrier heights ΦBn of the n type and Φ_{Bp} of the p-type semiconductor results to be equal to the energy bandgap [37]

$$q(\,\Phi_{Bn} + \Phi_{Bp}\,) = E_G \qquad 1.5$$

This relationship for Schottky-Mott limit implies that the control of the barrier height is achieved by the choice of the metal. The second limiting case is the Bardeen limit where a large density of states is present at the semiconductor to metal interface. In the Bardeen limit the barrier height Φ_B is completely independent of the metal work function Φ_m in contrast to the Schottky-Mott limit and the Fermi level is said to be pinned by the high density of interface states. The Fermi levels of the two dissimilar materials do not match when the

vacuum levels of the material are set equal. The instant the metal and semiconductor are made in contact with each other, their Fermi levels still do not align. However, a splitting in

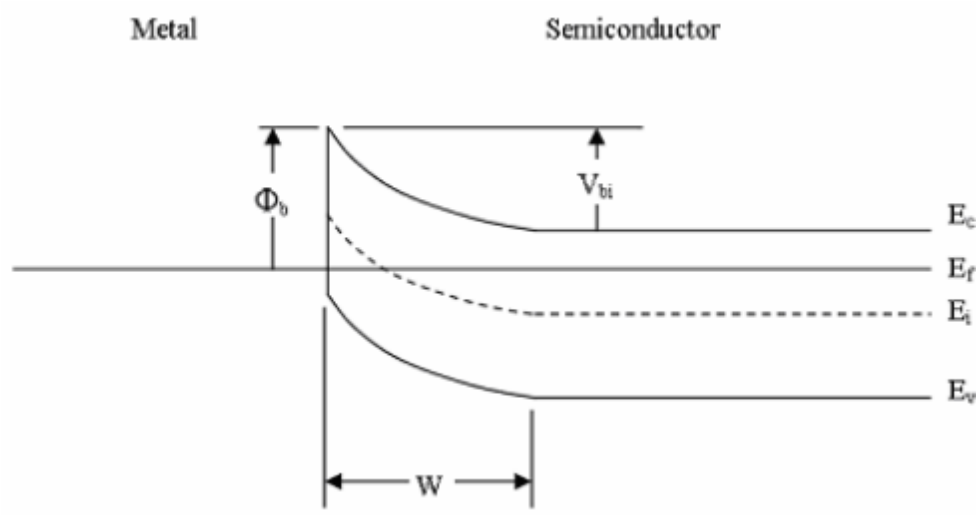

Figure 4.4- Energy band diagram of Schottky contact at equilibrium [40]

Fermi levels signifies non-equilibrium conditions exist. This is obviously not the case since no external perturbation is being applied. Therefore, to get the equilibrium conditions, transference of electrons between the semiconductor and the metal will occur. This will result in depletion region at the interface of the semiconductor and the metal. At equilibrium, the Fermi level is invariant with position as shown in Figure 4.4. Metal- semiconductor contact can either be rectifying or non-rectifying depending on the difference between work function of the metal and the semiconductor. The rectifying contact has a built-in potential, Vbi that can be equated from the Schottky barrier height and semiconductor doping level as [36]

$$\mathbf{V_{bi} = 1/q[\Phi b - (EC - Efs)_{FB}} \quad 1.6$$

where Φb = Φm – χ is the Schottky barrier height and q is the charge on an electron. Using one sided abrupt junction, such as those used for p^+-n junctions, the usual electrostatic variables can be obtained for non-punch through devices [37]

$$\textbf{Electric field, } E(x) = -qN_d(W-x)/K_s\in o \quad 1.7$$

$$\textbf{Voltage, } (x) = -qN_d(W-x)^2/2K_s\in o \quad 1.8$$

$$\text{Depletion Width, } W = \sqrt{\frac{2K_s \in_o}{-qN_d}(V_{bi} - V_a)} \qquad 1.9$$

Where N_d is the doping of the semiconductor,

Ks is the permittivity of the semiconductor,

$\in o$ is the permittivity of free space,

Va is the voltage applied to the Schottky contact and

x is the distance drom the metal-semiconductor interface [37]

4.3 Current-Voltage (I-V) Characterization

Current flows in a Schottky barrier diode because charge transfers from the semiconductor to the metal or vice versa. The four basic mechanisms by which carrier transportation can occur are:

1) Thermionic emission over the energy barrier

2) Tunneling through the barrier

3) Carrier recombination or generation in the depletion region

4) Carrier recombination in the natural region of the semiconductor

Thermionic emission is the dominant mechanism in Schottky barrier junctions. The thermionic emission is derived from the assumption that the barrier height (ϕ_B) is much larger than kT. Thermal equilibrium established at the junction determines emission and the existence of a net current flow. At the junction, there are two currents, one flow from the metal to the semiconductor and the other flows from the semiconductor to the metal. The current flow depends on the barrier height. In thermionic emission theory, the effect of drift and diffusion in the depletion region is assumed to be negligible [37, 42]. Therefore, the standard thermionic emission relation for electron transport from the metal to the semiconductor with low doping concentration is given by.

$$\mathbf{I_F = I_0[\frac{qVa-IRs}{nKT}]\{1 - exp\left(\frac{-q(Va-IRs)}{KT}\right)\}} \qquad 2.0$$

I_0 is the reverse saturation current which is dependent on the barrier ϕ_B for electron injection from the metal into the semiconductor and is given by

$$\mathbf{I_0 = AA^*T^2 exp\left(\frac{-q\phi B}{KT}\right)} \quad 2.1$$

I_0 is the reverse saturation current which is dependent on the barrier ϕ_B for electron injection from the metal into the semiconductor and is given by

$$\mathbf{I_F = I_0\ exp\left(\frac{qVa}{nKT}\right)} \quad 2.2$$

From the forward bias current equation Schottky diodes behave as rectifiers with easy current flow in the forward direction and little current in the reverse direction. Figure 4.5 shows the energy band diagram of the metal semiconductor junction under forward and reverse biased conditions.

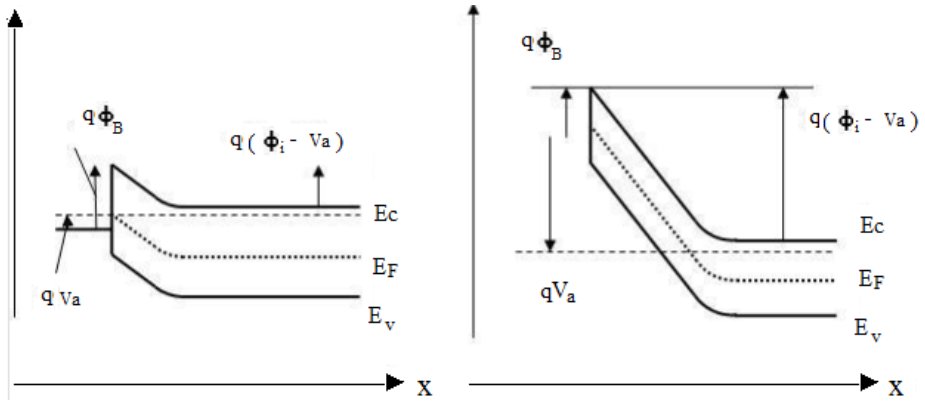

Figure 4.5 Energy band diagram of (a) forward biased (b) reverse biased M-S junction[27]

The depletion width is also dependent on the high doping density. High doping concentration makes a thin depletion width and promotes more tunneling. The depletion width is given by

$$\mathbf{W = \sqrt{\frac{2\epsilon(Vbi-Va)}{Nd}}} \quad 2.3$$

Where W = Width of the depletion region

Vbi = Built-in potential.

Va = Applied voltage.

Nd = Doping concentration.

ϵ = Permitivity [37]

CHAPTER 5

Calculations for Uniformly Doped Drift Region Profile

5.1 Introduction

Compared to silicon, silicon carbide (SiC) has certain physical properties that put it on a higher platform for use in solid-state power devices. A low intrinsic carrier concentration of the order of 10^{-7} per cc, a 10x higher breakdown electrical field, typically about 3 MV/cm, and a 3-fold higher thermal conductivity coupled with a large saturated drift velocity of $2*10^{7}$ cm/s are some of the salient features of SiC. These devices are extremely attractive in applications requiring blocking voltages ranging from 300 V to 3 kV. High voltage SiC devices are thinner and can be heavily doped if needed. At equivalent breakdown voltages, they offer specific on-resistance (Ron-sp) which may be up to two orders of magnitude lower compared to silicon devices. The forward voltage drop of SiC devices is well below 2.5 V for a 600V Schottky barrier diode (SBD) even at a current density of 4000 A/cm^2 and Ron-sp of these devices, due to the thinner drift region, is 200 times less than that of the silicon counterparts. [43].

5.2 Uniformly doped profile

The common device structure of a 3C-SiC SBD is shown in figure 5.1 and it's equivalent circuit is also drawn in figure 5.2. The SBD shown in figure 5.1 consists of a block of n-type 3C-SiC crystal with a given height 'h'. The metal contact at the top has a cross-sectional area 'A' and there is a base contact which may be formed using a metal or an alloy. Boron implant is made for edge termination on either side of the Schottky contact. An overlap exists between the top metallic contact of width 'd' and the contact length 'a'. The current flow from the top contact is considered trapezoidal in shape spreading through the drift region by an angle 'α' with the vertical at the corner edge of the boron implant beneath the contact. A standard value of '$\alpha=26^{0}$'is taken for this model, which allows a small spread of

current from the top contact to uniformly flow into the n+-substrate below. The equivalent circuit shown in Figure 5.2 of the SBD has $R_{on\text{-}sp}$ which is the sum of the series $R_{on\text{-}sp}$ of the drift region (R_D) and the parasitic series resistance (R_s) with uniform current flow. Beneath this region is the n+-type heavily doped substrate region whose resistance may be considered to be zero. [43]

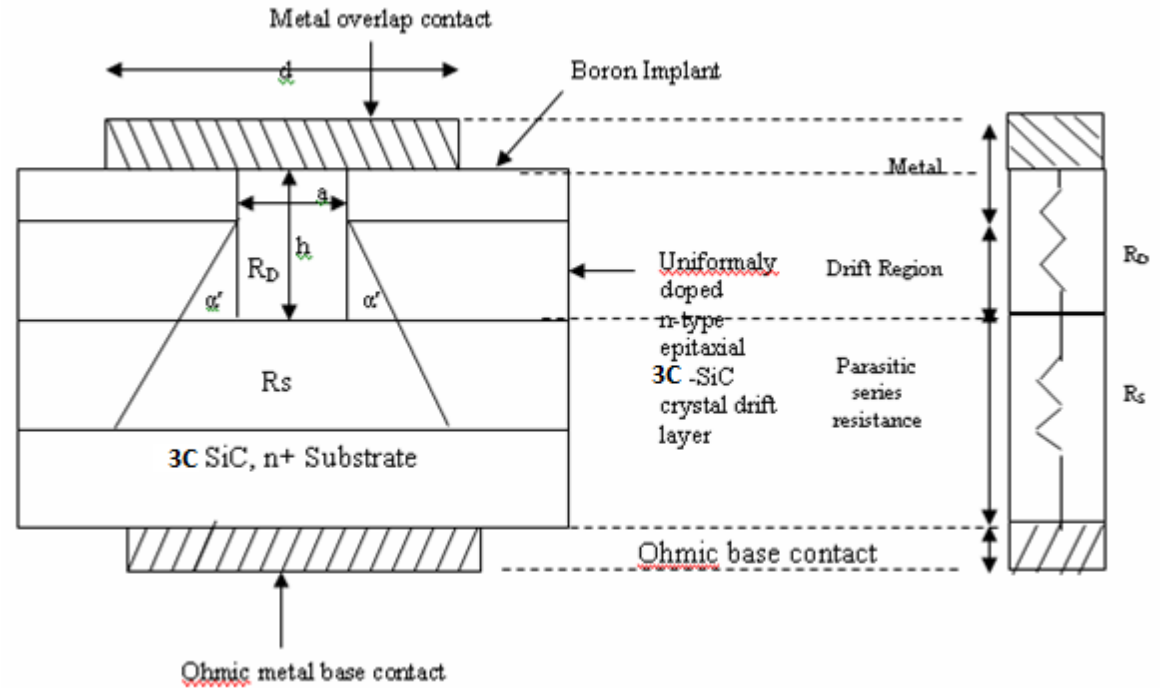

Figure 5.1-The structure and region of a SBD [43] **Figure 5.2- Equivalent circuit of SBD**

5.3 Important Relations for 3C SiC devices

5.3.1 Calculation of Breakdown Voltage

The punch-through breakdown voltage (V_{PBV}) is determined at a high reverse bias voltage (V_R) for a uniformly doped semiconductor of 3C-SiC SBD and on this voltage the depletion region width (W) is set equal to the device height (h). The avalanche breakdown voltage is obtained using the condition $\alpha_p W = 1$, to give the value of α_p. The critical field (E_c) corresponding to this value of α_p is obtained from [44]. The magnitude of the avalanche breakdown voltage (V_{AVBV}) is then obtained using the equation:

$$\mathbf{V_{AVBV} = E_C W/2} \quad \text{for uniformly doped drift region of SBD} \quad 2.4$$

5.3.2 Depletion Width

The depletion region width for uniformly doped drift region of SBD is calculated using the formula:

$$W = \sqrt{2\epsilon_s(V_{bi}+V_R)/eN_d} \quad = \sqrt{2\epsilon_s V_R/eN_d}$$

Where 2.5

V_{bi} is the built-in potential and $V_{bi} << V_R$, the applied reverse voltage which is equal to the Avalanche breakdown voltage, ϵ_S denotes the permittivity of 3C-SiC.

5.3.3 Critical Electric Field

The equation connecting the breakdown field strength E_c on the doping level N_D for a p^+-n diode of 3C-SiC has been given. Based on these result the relationship between E_C and N_D was obtained [45]

$$\mathbf{Ec(3C\text{-}SiC) = 1.95 \times 10^4\ N_D^{\ 0.131}\ (V/cm)}\ [45] \qquad 2.6$$

5.3.4 Ron-sp:

$$R_{on\text{-}sp} = \rho_D \frac{d}{tan\alpha'} \ln\left[1 + \frac{2h}{a} tan\alpha'\right] \qquad 2.7$$

$$R_{on\text{-}sp} = \rho_D \frac{a}{tan\alpha'} \ln\left[1 + \frac{2h}{a} tan\alpha'\right] \qquad 2.8$$

Where

d = a for minimum overlap of contact metal considered and

h = Device height (μm),

α ′ = Angle of slope of the drift region narrowing (Degree)

Where

$$\rho_D = 1/\mu_N eN_d \qquad 2.9$$

N_d is the donor density in the epitaxial layer (/cc)

μ_N is the electron mobility (cm^2/V.sec)

5.3.5 The Power Dissipation:

The equation for power dissipation P_D for a 50% duty cycle can be written as [43]

$$\mathbf{P_D = \frac{1}{2}(J^2_{on}AR_{on\text{-}sp}+J_LAV_B)\ Watts} \qquad 3.0$$

Where

J_{on} = On-state current density (amps/cm^2),

A = Device cross-sectional area for current flow (cm^2),

V_B = reverse blocking voltage

J_L =leakage current density, the magnitude of J_L in SiC devices is too small compared to that in silicon devices and hence the second term in equation can be neglected giving:

$$\mathbf{P_D = \frac{1}{2}(J^2_{on}AR_{on\text{-}sp})\ Watts} \qquad 3.1$$

5.3.6 Breakdown voltage

The punch-through breakdown voltage (V_{PBV}) is determined at a high reverse bias voltage (V_R) for a uniformly doped semiconductor of 3C-SiC SBD and the depletion region width (W) at this voltage is set equal to the device height (h)[43].

$$\mathbf{V_{AVBV} = \frac{1}{2}E_CW\ Volts} \qquad 3.2$$

5.4 Calculations for Power Dissipation of 3C SiC SBD with Uniformly Doped Profile

The Punch through breakdown voltage V_{PBV} corresponding to the device height 'h' is set for 15 KV, whose depletion width is calculating using 2.5. Hence the device height 'h' is set equal to the maximum depletion region width 'W' corresponding to a breakdown voltage of 15 KV for the uniformly doped epitaxial layer with the lowest doping level of 10^{15} per cc using equation 2.5. This gives a value of 130μm for the device height 'h' taking ε_s = 9.7 for 3C-SiC. The doping-dependent mobility value is obtained from Roschke and Schwierz. The magnitude of $R_{on\text{-}sp}$ is calculated using equation 2.8 with angle $\alpha' = 26^0$ and Schottky contact of

length ‘a’ equal to 100 μm. The contact width is equal to 100 μm. The device cross-sectional area ‘A’ is then 10^{-4} cm^2. Specific values of the on-state current density (J_{on}) ranging from 100 to 1000 amps/cm^2 are used and the corresponding values of power dissipation (P_D) are calculated using equation 3.1. This is repeated for doping levels of 10^{16}, 10^{17} , 10^{18} and 10^{19} per cc. The results are shown in Table 5.1

Where

Permittivity of semiconductor in free space $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm

Doping concentration $N_D = 10^{15}/cm^3$

Permittivity of SiC semiconductor $\varepsilon_s = 9.7\ \varepsilon_0$

Electron charge $e = 1.6 \times 10^{-19}$ coulomb

Calculation for Power Dissipation of 3C-SIC with Uniformly Doped Profile

Table 5.1: Calculation for Power Dissipation of 3C-SIC with Uniformly Doped Profile

Current density (amps/cm^2) J_{on}	$N = 10^{15}$ (atoms/ cm^3)	$N = 10^{16}$ (atoms/ cm^3)	$N = 10^{17}$ (atoms/cm^3)	$N = 10^{18}$ (atoms/ cm^3)	$N = 10^{19}$ (atoms/ cm^3)
	μ = 650 cm^2/Vs [35]	μ = 580 cm^2/Vs	μ = 368 cm^2/Vs	μ = 192 cm^2/Vs	μ = 109 cm^2/Vs
	$R_{on\text{-}sp} = 16.137*10^{-2}$ Ω-cm^2	$R_{on\text{-}sp} = 1.809*10^{-2}$ Ω-cm^2	$R_{on\text{-}sp} = 0.285*10^{-2}$ Ω-cm^2	$R_{on\text{-}sp} = 0.0547*10^{-2}$ Ω-cm^2	$R_{on\text{-}sp} = 0.0034*10^{-2}$ Ω-cm^2
	P_D=(milliwatts)	P_D=(milliwatts)	P_D=(milliwatts)	P_D=(milliwatts)	P_D=(milliwatts)
100	80.69	9.05	1.43	0.27	0.008
200	322.74	36.18	5.70	1.09	0.007
400	1290.96	144.72	22.80	4.376	0.273
600	2904.66	325.62	51.30	9.85	0.61
800	5163.84	578.88	91.20	17.50	1.09
1000	8068.50	904.50	142.50	27.35	1.71

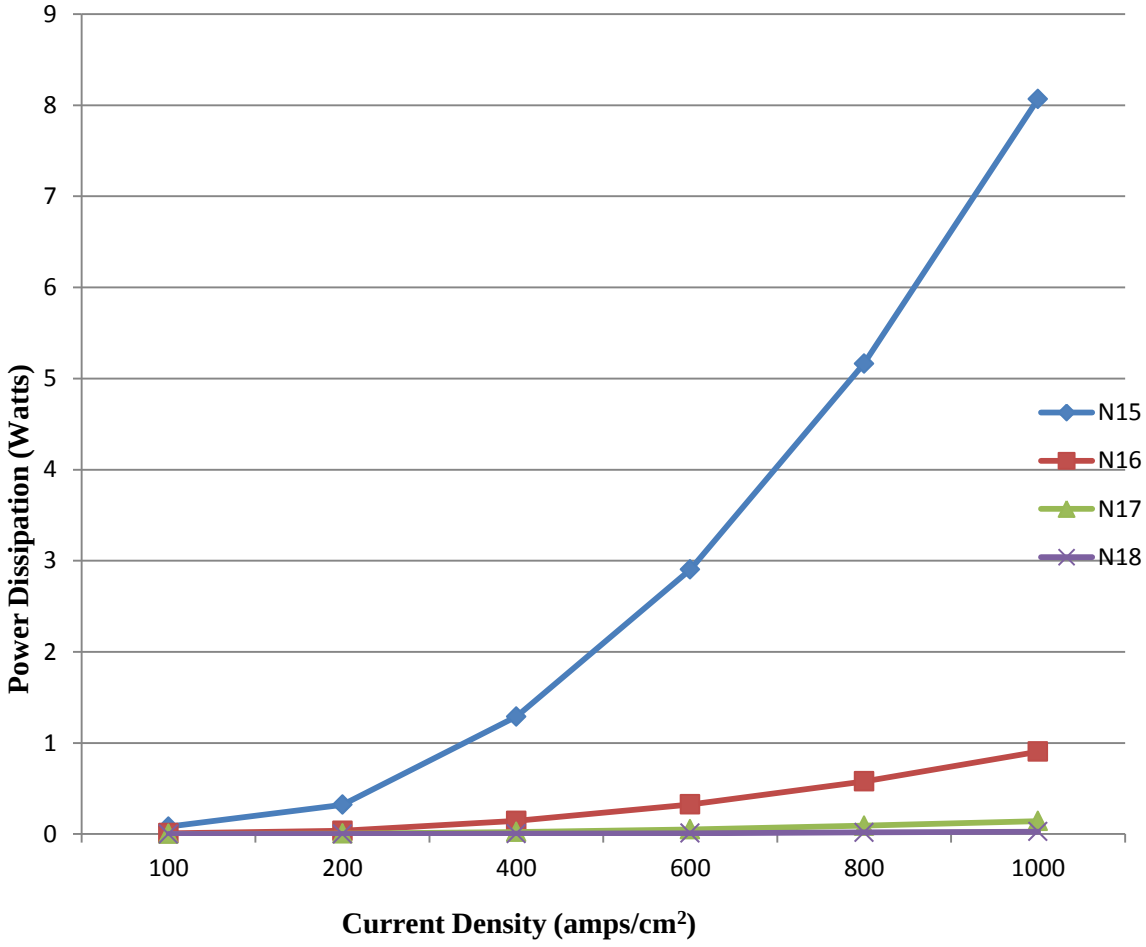

Figure 5.3- Plot between Power Dissipation and Current Density (For Uniformly Doped Profile)

5.5 Calculation for Breakdown Voltage

The punch through break down voltage V_{PBV} was set for a break down voltage 5KV for a 3C SiC SBD with a uniformly doped drift region having a doping level of 10^{15} per cc. The corresponding device height was equal to the depletion width W at this voltage the value was founded 130 μm. the Avalanche breakdown voltage is calculated for the doping level of 10^{15}, 10^{16}, 10^{17}, 10^{18} and 10^{19} per cc. The Avalanche breakdown voltage is obtained using the condition $\alpha_p W = 1$, to give the magnitude of α_p. The critical field (Ec) corresponding to this value of α_p is obtained from [44].Calculation shows in table 5.2.

Table 5.2: Calculation for V_{AVBV} & V_{PBV} for Uniformly Doped Profile

Sr. No.	Doping Level N_d(atoms/cm^3)	Depletion Width (μm)	Critical Electric Field(E_c), V/cm * 10^6	V_{AVBV} (kV)	V_{PBV} (kV)
1.	10^{15}	126.87	2.36	15	15
2.	10^{16}	40.12	7.48	15	15
3.	10^{17}	12.69	23.64	15	15
4.	10^{18}	4.01	74.80	15	15
5.	10^{19}	1.27	236.40	15	15

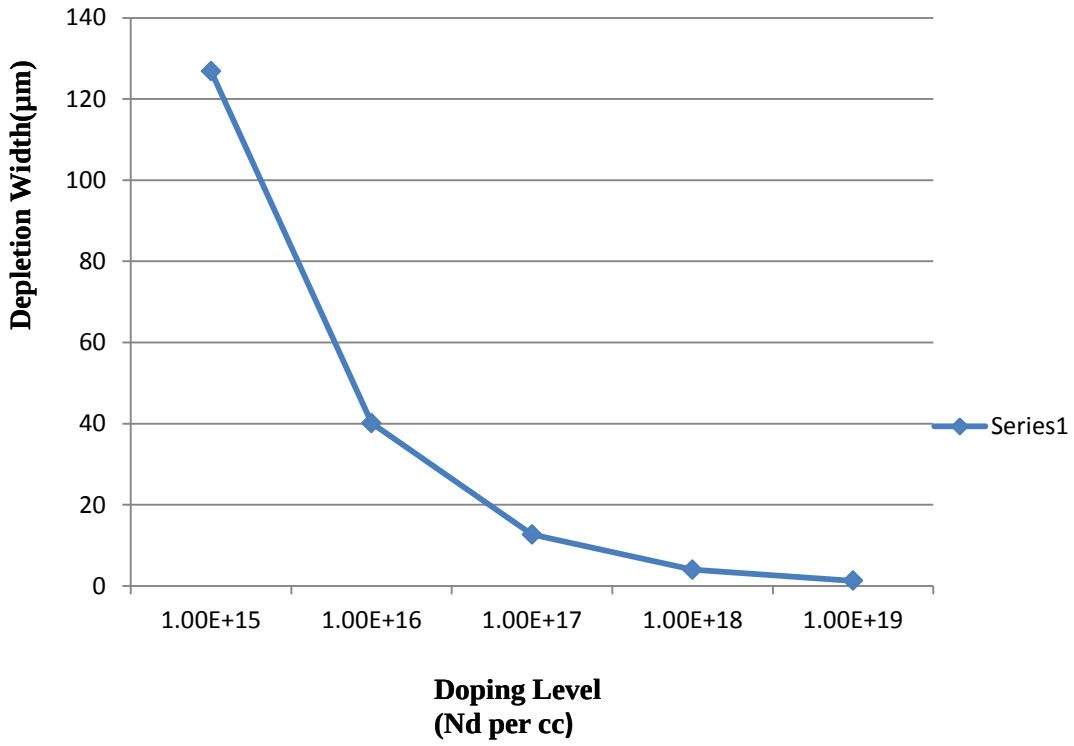

Figure 5.4-Plot between Depletion Width and Doping Level (For Uniformly Diped Profile)

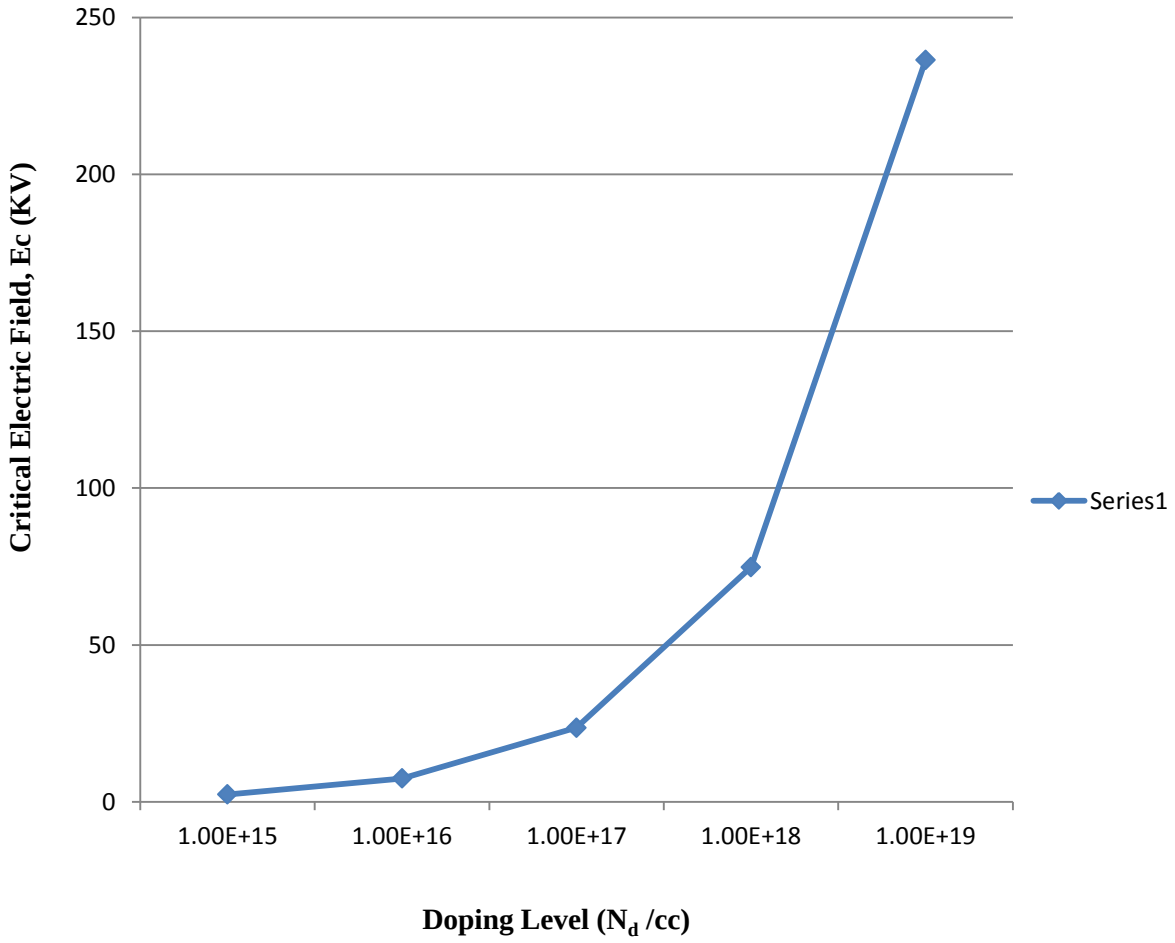

Figure 5.5- Plot between Critical Electric Field and Doping Level (For Uniformly Doped Profile)

CHAPTER 6

Calculations for 3C-SiC using Linearly Graded Drift Region

This chapter is an analysis of power dissipation, depletion region width and breakdown voltages of 3C-SiC SBD using linearly graded doped profile. In the model proposed here for the 3C-SiC SBD, the epitaxial layer is linearly graded with a gradient α. Near the contact, the device has the lowest doping level (No) and it increases with the gradient to any desired doping level (N) at the substrate. This is shown in Figure 6.1. The equivalent circuit of the device is shown in Figure 6.2, with R_D replaced by R_D' and the new Rs' (< Rs) being used. Magnitude of Rs' is lower than Rs as the doping level is nearer to the substrate than the contact at the top of the device.

6.1 Linearly Graded Profile

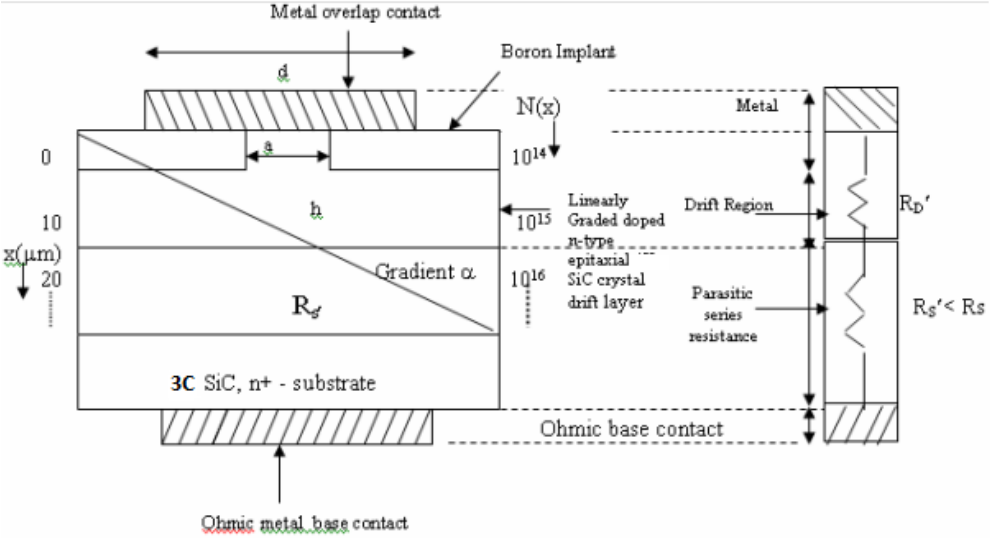

Figure 6.1- The 3C-SiC SBD with linearly graded drift region profile with gradient α [43]

Figure 6.2- The equivalent circuit of the SBD

The doping level N_D of the epitaxial layer has to be replaced by the effective doping level N_{eff} of the linearly graded drift layer. [43]

6.2 Device equations for Linearly Graded Drift Region

6.2.1 Gradient of the profile

$$\alpha = \frac{N(x)-N(0)}{h} \quad 3.3$$

Where

α = gradient of profile (cm^{-4})

N(x) = Desired doping density

N(0) = Lower doping density, used as reference doping level for calculating the gradient at different desired doping density.

h = Device height [33]

6.2.2 Ron-sp

$$R_{on\text{-}sp} = \rho_D \frac{a}{tan\alpha'} \ln\left[1 + \frac{2h}{a} tan\alpha'\right] \quad 3.4$$

Where

a = for minimum overlap of contact metal considered

h = Device height (μm),

α ′ = Angle of slope of the drift region narrowing (Degree)

Where

$$\rho_D = 1/\mu_N e N_{eff} \quad 3.5$$

N_{eff} is the effective Doping Concentration(/cc)

μ_N is the electron mobility (cm^2/V.sec) [43]

6.2.3 Depletion region width (for linearly graded drift region of SBD)

$$W = \sqrt[3]{12\epsilon_s(V_g+V_R)/e\alpha} \quad (\mu m) \quad 3.6$$

Where

Vg is the gradient voltage and $Vg << V_R$, the applied reverse voltage which is equal to the avalanche breakdown voltage. In the two equations,

Where

ϵ_S = Permittivity of 3C-SiC

e = electron charge ($1.6*10^{-19}$ coulombs)

Vg = Gradient voltage (V)

Neff = Effective doping concentration (/cc) [43]

6.2.4 Effective doping concentration given by [43]

$$\mathbf{N_{eff}} = \frac{ah}{ln\left(1+\frac{ah}{No}\right)} \quad \mathbf{(/cm^3)} \qquad 3.7$$

Where

α = gradient of profile

h = device height (μm)

6.2.5 Power Dissipation

The equation for power dissipation for linearly graded drift region devices is given as [33]

$$\mathbf{P_D = \frac{1}{2}(J^2_{on} AR_{on\text{-}sp})\ Watts} \qquad 3.8$$

Where

Jon = On-state current density

A = Device cross section area (cm^2)

Ron-sp = Specific on- resistance of the device

6.2.6 Critical electric field

The critical electrical field is given by[43]

$$\mathbf{E_c = e\alpha W^2/8\epsilon_s} \qquad 3.9$$

Where

e = electron charge

W = depletion region width for linearly graded drift region devices (μm)

6.2.7 The Avalanche Breakdown voltage

For linearly graded drift region devices the Avalanche breakdown voltage is give by [43]

$$\mathbf{V_{AVBV} = \frac{2}{3} E_c W} \qquad 4.0$$

6.3 Calculations for Power Dissipation

Power Dissipation is calculated using the set of equation of 3.3 – 4.0 for linearly graded drift region and also found the value of the Avalanche breakdown voltage and set the value of punch through voltage at 15KV.The values of power dissipation corresponding the value of current density J_{on} 100 to 1000 amps/cm^2 are shown in the table 6.1.

Table 6.1: Calculations for Power Dissipation for Linearly Graded Drift Region

Current density (amps/cm^2) J_{on}	**N_{eff} = 3.57 * 10^{15} (atoms/ cm^3)**	**N_{eff} = 1.91*10^{16} (atoms/ cm^3)**	**N_{eff} =1.27*10^{17} (atoms/ cm^3)**	**N_{eff} = 9.51*10^{18} (atoms/ cm^3)**
	μ = 650 cm^2/Vs [35]	**μ = 580 cm^2/Vs**	**μ = 368 cm^2/Vs**	**μ = 192 cm^2/Vs**
	R_{on-sp}= 40.41*10^{-3} Ω-cm^2	**R_{on-sp}= 8.46*10^{-3} Ω-cm^2**	**R_{on-sp}= 1.99*10^{-3} Ω-cm^2**	**R_{on-sp}= 0.51*10^{-3} Ω-cm^2**
	P_D=(10^{-2})watts	**P_D=(10^{-2})watts**	**P_D=(10^{-2})watts**	**P_D=(10^{-2})watts**
100	2.020	0.420	0.098	0.025
200	8.080	1.692	0.392	0.100
400	32.33	6.768	1.568	0.400
600	72.74	15.23	3.528	0.918
800	129.3	27.07	6.272	1.630
1000	202.1	42.30	09.80	2.550

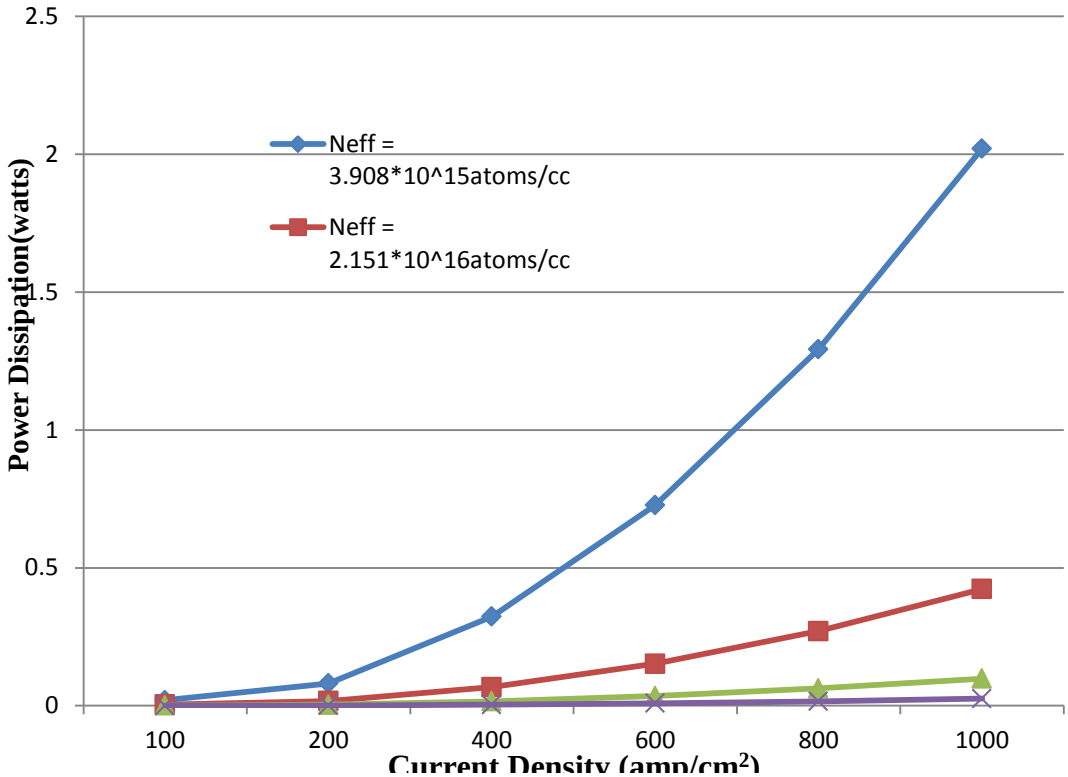

Figure 6.3- Plot between Current Density and Power dissipation (for Linearly Graded Drift Region)

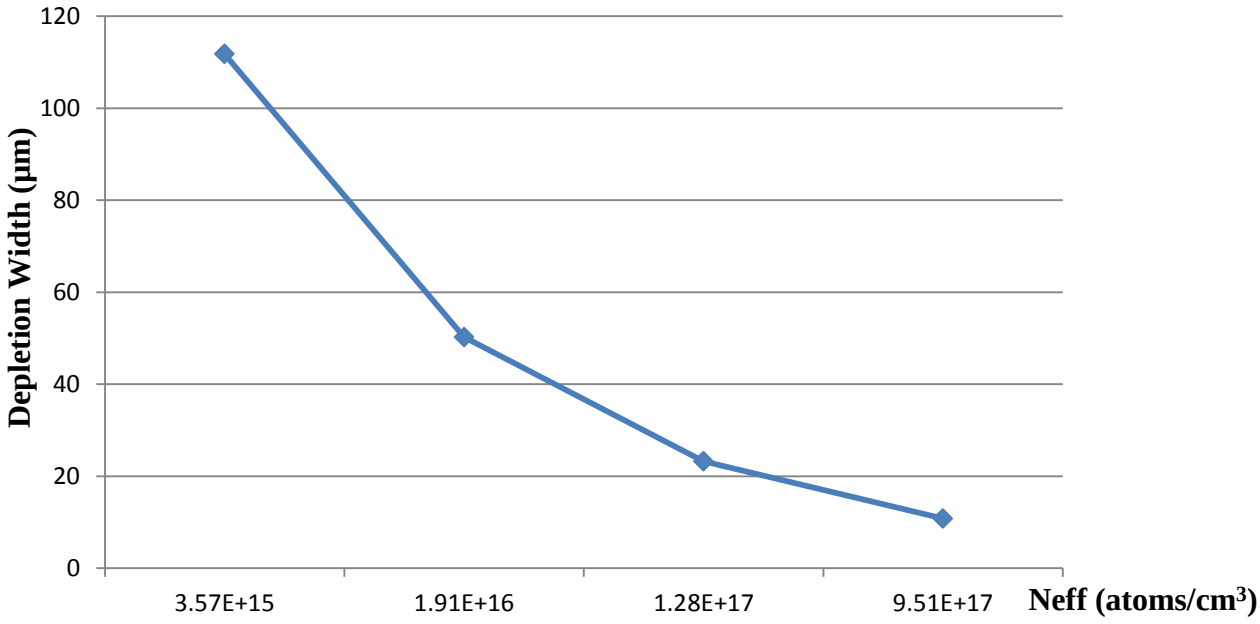

Figure 6.4- Plot between Depletion Width and Neff (for Linearly Graded Drift Region)

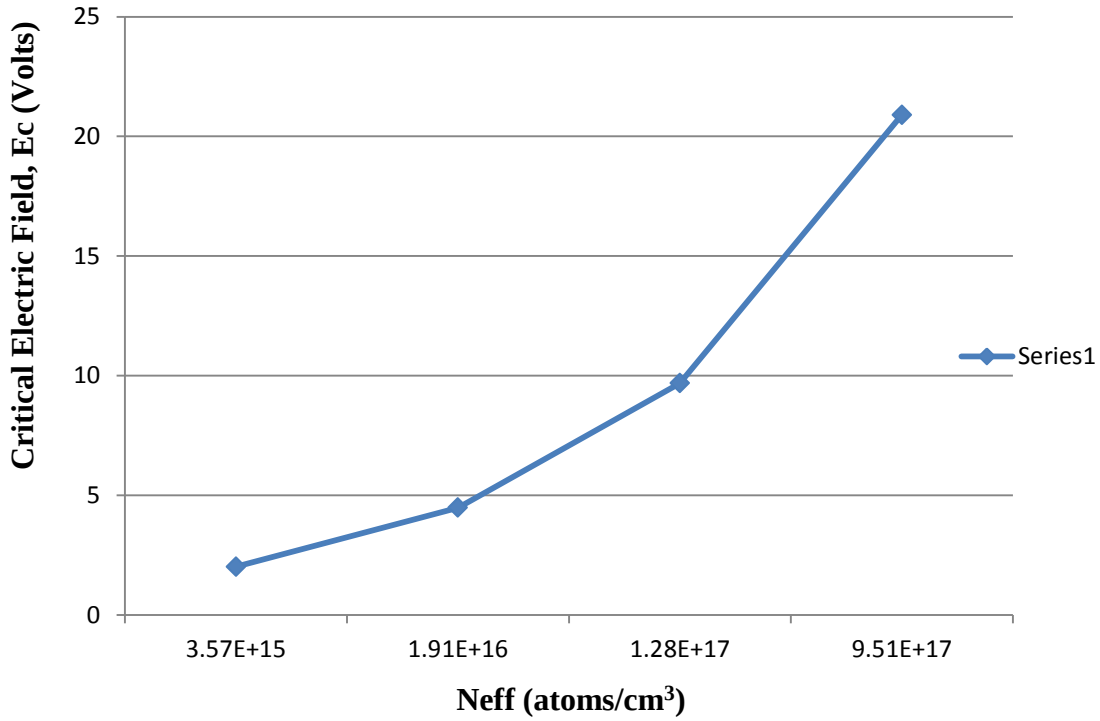

Figure 6.5- Plot between Critical Electric Field and Neff (for Linearly Graded Drift Region)

Table 6.2: Breakdown voltages VAVBV & VPBV of 3C-SiC SBD for Linearly Graded Drift Region

S.No.	$\alpha'(cm^{-4})$	W (µm)	Ec (V/cm)	V_{AVBV} (kV)	V_{PBV}(kV)
1.	$6.92*10^{17}$	111.75	$2.01*10^{6}$	14.98	15
2.	$7.62*10^{18}$	50.23	$4.48*10^{6}$	15.00	15
3.	$76.85*10^{18}$	23.25	$9.68*10^{6}$	15.00	15
4.	$76.92*10^{19}$	10.79	$2.09*10^{7}$	15.03	15

CHAPTER 7

Results

Results for the calculations for depletion region width against doping level of drift region 3C-SiC Schottky barrier diode using uniformly doped profile in drift region has been made in chapter 5. The results are reported in chapter 5earlier. Range of doping level selected was from 10^{15} donor atoms/cc to 10^{19} donor atoms/cc. The device was designed for Avalanche breakdown voltage15KV. The corresponding critical electric field ranges from $2.36*10^{6}$ V/cm to $236.40*10^{6}$ V/cm. The depletion region width however gradually decreased from 126.87μm for doping level of 10^{15} atoms/cc to 1.27 μm at doping level of 10^{19} atoms/cc. Since high power devices require substantial thickness of the drift region. It is recommended that the doping level of 10^{15} atoms/cc be used for making these devices. This would just fit into the 3C SiC wafer thickness of 130 μm.

The results for 3C SiC Schottky barrier diode using linearly graded drift region however show some change in the results reported above for uniformly doped drift region devices. In this case the doping level used has been considered as $N_{effective}$ for the linearly graded systems. It can be seen from table 6.2 that the value of doping level N_{eff} changed from $3.57*10^{15}$ atoms/cc to $9.51*10^{18}$ atoms/cc for gradients(α') ranging from $6.92*10^{17}cm^{-4}$ to $76.92*10^{19}$ cm^{-4}. The corresponding critical electric field for Avalanche breakdown voltages of about 15KV range from $2.01*10^{6}$ V/cm to $2.09*10^{7}$V/cm. The corresponding depletion region width ranges from 111.75 μm to 10.75 μm over these range of concentration gradients (α') and the corresponding values of N_{eff}. Hence linearly graded devices require wider depletion region width of 10.79 μm at 15KV for N_{eff} of $9.51*10^{18}$ atoms.cc approximately equal to 10^{19} atoms/cc. This is much larger as compare to 1.27 μm depletion region width at 15KV for uniformly doped region of 10^{19} atoms/cc. Comparing the two results, it can be inferred that linearly graded drift region devices requires wafer thickness 15 μm less as compare to those using drift region devices. This can be seen by comparing the results of depletion region width in table 5.2 and 6.2 for uniformly doped and

linearly graded drift region devices at doping level 10^{15} atoms/cc for uniformly doped devices and $3.5*10^{15}$ atoms/cc.

The variation of Ec with doping level for 15K devices are shown in fig 5.5 for uniformly doped drift region devices and in fig 6.5 for linearly graded drift region devices. It can be seen that Ec changes more than $10*10^{6}$ V/cm for a change of order of 10 at a doping level 10^{18} to 10^{19} atoms/cc. However this change reduces to only $10*10^{6}$ V/cm for a change of order of 10 from $1.28*10^{17}$ atoms/cc to $9.51*10^{17}$atoms/cc for linearly graded drift region devices. The Avalanche and Punch through voltages for these two devices have been obtained at breakdown voltages at 15KV and results are shown in table 5.2 for uniformly doped devices and table 6.2 for linearly graded drift region devices. The results are shown in table 5.2 and 6.2 respectively. Strongly enough the Avalanche and Punch Through voltages in both devices approximately match each other.

The calculations for power dissipation for uniformly doped devices and linearly graded devices have been made by taking established data for mobility dependent on the doping level to calculate Ron-sp(Specific On Resistance). The power dissipation has been calculated over a range of on state current density, Jon(ampere/cm^2) from 100 to 1000 ampere/cm^2. The results are reported in table 5.1 for uniformly doped devices and table 6.1 for linearly graded drift region devices. It can be seen that all ranges of doping levels of N and N_{Eff} atoms/cc. The linearly graded drift region devices shows substantially low power dissipation than those shown by uniformly doped drift region devices. The results are graphically depicted in figures 5.3 and 6.3 for uniformly doped and linearly graded drift region devices respectively.

CHAPTER 8

Conclusions and Scope of Future Work

The present work aims data analyzing the variations of depletion region width, Punch Through and Avalanche breakdown voltages and also power dissipation for different doping levels and On state current density. As has been stated in chapter 7, thinner devices and lower depletion region width can be achieved using linearly graded drift region devices. This could substantially reduces the device site maintaining the same breakdown voltage. Also the device height for wafer thickness can be reduced substantially by about 10% using the linearly graded profile in the drift region of 3C-SiC Schottky Barrier Diode. The linearly graded profiles have been analyzed and found to give far smaller power dissipation than those provided by uniformly doped drift region devices.

A lot of along these lines have been done on 6H and 4H SiC SBDs. It would be advisable to explore the possibility of exploring non-linear doping profiles like the Gaussian and complimentary error function doping profile in the drift region of 3C-SiC SBDDs and analyze whether or not, there is substantial change in values of depletion region width, Critical electric field, Avalanche breakdown voltages and Punch Through voltages and also power dissipation in these devices.

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