Design of a Low Power 8T SRAM Cell with Improved Stability

A Thesis Submitted in Partial Fulfilment of the Requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI Design

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DECLARATION

I, Gaurav Sharma hereby declare that the work presented in this thesis entitled **"Design of a Low Power 8T SRAM Cell with Improved Stability"** in partial fulfilment of the requirement for the award of degree of Master of Technology (VLSI Design) submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Mr. Arun Kumar Chatterjee (Assistant Professor, ECED)** from June 2017 to June 2018. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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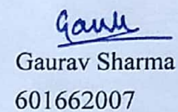

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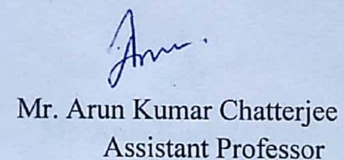

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The study has indeed helped me to explore knowledge and I am sure it will help me in my future

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ABSTRACT

SRAM is a type of semiconductor memory and typically used for CPU cache and focused on reducing power and to improve the stability of SRAM cells. The total die area of the modern SOCs is 70% covered by Embedded memories. The SRAMs are continued to be the most important part of microelectronics such as a system on chip application, high performance server processors, multimedia, wireless applications etc.

In this thesis work, stacked logic style have been employed to modify the conventional 6T SRAM cell which in turn reduces the static and total power dissipation at the cost of increase in write and read delay of the proposed cell. First of all, a conventional 6T SRAM cell has been simulated and the circuit is modified with using stacked logic style with two more transistors and the simulation results shows a significant reduction in power dissipation and improvement in stability of the cell.

The static power of a proposed cell has been reduced by 46.4 % as compared to conventional 6T SRAM cell and total power has been decreased by 30.2 %. Although the write delay and read delay of the proposed cell has been increased by 29.8 % and 8.9 % in comparison to published 8T SRAM cell, the stability of the proposed cell has been improved significantly. The stability parameters such as write trip current (WTI), static voltage noise margin (SVNM), static current noise margin (SINM) of proposed 8T SRAM cell have been improved by 27.7 %, 53.3 %, 1 % respectively as compared to the conventional 6T cell and 71.9 %, 4 %, 42.8 %, respectively as compared to the published 8T SRAM cell. The Write trip voltage (WTV) of the proposed cell has been decreased by 12.6 % as compared to conventional 6T cell and 13.4 % as compared to the published 8T SRAM cell, respectively. This shows that the proposed 8T SRAM cell is much more stable than other published 8T SRAM cells. All the simulation were have been done in Cadence Virtuoso tool at 90nm technology.

TABLE OF CONTENTS

Sr. No.	Name of Chapters	Page No.
	DECLARATION	i
	ACKNOWLEDGEMENT	ii
	ABSTRACT	iii
	TABLE OF CONTENTS	iv
	LIST OF FIGURES	vi
	LIST OF TABLES	viii
	LIST OF ACRONYMS	ix
CHAPTER 1	Introduction	1
1.1	Technology trend	1
1.2	Motivation	1
1.3	SRAM Application in Wireless Communication Devices	2
1.4	Thesis organization	4
CHAPTER 2	Literature Review	5
CHAPTER 3	Introduction to SRAM Cell	9
3.1	Random access memory (RAM)	9
3 .1.1	SRAM and DRAM	9
3.2	Conventional 6T SRAM Cell	9
3.2.1	Operations in 6T SRAM Cell	11
3.3	Architecture of an SRAM Unit	13
3.3.1	Row Decoder and Column Multiplexer	14
3.4	Different types of SRAM Cell	16
3.4.1	4T SRAM Cell	16
3.4.2	7T SRAM Cell	16
3.4.3	8T SRAM-Cell	17
3.5	N-Curve Analysis	17
3.6	Sources-of-power-dissipation	19
3.6.1	Short-circuit power dissipation	19
3.6.2	Dynamic Power dissipation	21
3.6.3	Leakage Power Dissipation	22
3.6.4	Techniques to reduced leakage and dynamic power	25
3.6.5	Static Power Dissipation	26
CHAPTER 4	Results and Performance Analysis	28
4.1	Power Analysis	28

4.2	Transient Analysis	29
4.3	N-Curve Analysis	31
CHAPTER 5	Conclusion and Future Scope	41
5.1	Conclusion	41
5.2	Future Scope	41
	REFERENCES	43

LIST OF FIGURES

Sr. No. **Figure Details** **Page No.**

Figure 1.1 Increasing of a number of transistors/chip with respect to year according to ITRS-2005........2
Figure 1.2 Two SOCs comprising SRAMs and cores presented in ISSCC'05: (a) A Video processor and (b) a Sparc processor...3
Figure 3.1 Symbols of NMOS and PMOS 10
Figure 3.2 Circuit of 6T SRAM Cell...10
Figure 3.3 Schematic of DRAM Cell 11
Figure 3.4 Read Operation..12
Figure 3.5 Write Operation 12
Figure 3.6 The concept of interleaving in an SRAM array 14
Figure 3.7 Utilization of a row decoder and a column multiplexer to activate the respective wordline and bitline according to the address...15
Figure 3.8 Schematic of 4T SRAM Cell...16
Figure 3.9 Schematic of 7T SRAM Cell...16
Figure 3.10 Schematic of 8T SRAM Cell...17
Figure 3.11 The N-curve and the butterfly curve of the Cell...18
Figure 3.12 CMOS inverter transistors conduct simultaneously a short-circuit current 20
Figure 3.13 The operation of a CMOS inverter: (a) CMOS inverter, (b) Charging phase, and (c) Discharging phase 21
Figure 3.14 The leakage current in a reverse- biased PMOS transistor 23
Figure 3.15 Subthreshold leakage with respect to gate-source voltage.......................................24
Figure 3.16 Subthreshold leakage current path in a CMOS inverter with high V_{dd}. 25
Figure 3.17 Clock Gating..25
Figure 3.18 Multi-Vt optimization..26
Figure 3.19 Degraded voltage level as input signal to an inverter results in static power consumption. .27
Figure 4.1 Schematic of 6T SRAM Cell...29
Figure 4.2 Schematic of reference Cell 30
Figure 4.3 Schematic of Proposed Cell...31
Figure 4.4 N-Curve for Conventional cell at Vdd =1 V. 32
Figure 4.5 N-Curve for reference cell at Vdd = 1V 33
Figure 4.6 N-Curve for Proposed cell at Vdd = 1V. 34
Figure 4.7 Variation in write trip voltage of SRAM cell different temperatures.........................36
Figure 4.8 Variation in static voltage noise margin of SRAM at different temperature 36

Figure 4.9 Variation in SVNM of the Proposed cell with existing SRAM cell at different voltages. 37
Figure 4.10 Variation in write trip voltage of SRAM cell at different voltages. 38
Figure 4.11 Variation in SINM of the Proposed cell with existing SRAM cell at different voltages 39
Figure 4.12 Variation in write trip current SRAM cell at different supply voltages.................................39

LIST OF TABLES

Sr No. **Table Details** **Page No**

Table 4.1 Comparison of power with the existing and reference cell 28
Table 4.2 Comparison of write and read delay for the improved cell with the existing cell.......................30
Table 4.3 Stability factor in the proposed cell compared to existing SRAM cell 33
Table 4.4 Comparison of Stability parameters of 6T SRAM Cell with different Supply Voltage (Vdd)......34
Table 4.5 Comparison of Stability parameters of 6T SRAM Cell with different temperature range. 35
Table 4.7 Comparison of Stability parameters of reference cell at different Supply Voltages(Vdd) 37
Table 4.8 Comparison of Stability parameters of Proposed cell at different Supply Voltages(Vdd)..........38
Table 4.9 Comparison of Stability parameters of Proposed SRAM Cell with a different temperature range 40

LIST OF ACRONYMS

RAM	Random Access Memory
SRAM	Static Random Access Memory
SOC	System on Chip
DRAM	Dynamic Random Access Memory
SVNM	Static Voltage Noise Margin
SINM	Static Current Noise Margin
WTV	Write Trip Voltage
WTI	Write Trip Current
RSNM	Read Signal to Noise Margin
WSNM	Write Signal to Noise Margin
CMOS	Complementary metal oxide semiconductor
WWL	Write wordline
GND	Ground
SNM	Signal to Noise Margin
Vdd	Supply Voltage

CHAPTER 1

Introduction

1.1 Technology trend

A system-on-chip (SOC) is an integration of all the components for a computer or other electronic system into a single integrated circuit (IC). The total die area of the modern SOCs is 70% covered by Embedded memories. The SRAMs are continued to be the most important part of microelectronics components such as a system on chip application, high performance server processors, multimedia, wireless applications etc. It is also predicted that the percentage of the enclosed SRAMs in the system on chip products will increase from the present 84% to 94% by the year 2014 according to the International Technology Roadmap for Semiconductors (ITRS).

1.2 Motivation

The memory is an important part of modern VLSI systems. Developments in embedded memory technology have made large SRAMs and DRAMs common place in today's System on Chips (SOCs). Semiconductor memory acts as single memory chips and also as an essential part of complex VLSI systems. Over the past few years, with the explosive growth of battery operated devices such as wireless communication units, portable multi-media devices, and implantable bio-medical chips the demand for low-power integrated circuits has been significantly increased. Static power dissipation occurring in these idle components responsible for the huge percentage of total power dissipation in any system. Therefore, minimization of this leakage component becomes crucial for effective power management. Because of technology scaling of MOS devices, an affected enhancement in the performance of MOS devices has been attained. Figure 1.1 shows increasing in a number of transistors/chip with respect to year according to ITRS-2005. [1]

Therefore power dissipation have been increased due to increase in leakage current. Till now, the drain to source subthreshold current has been the dominant leakage component.

Besides this, there is a number of reasons, for the motivation of this research work, viz., Shrinking of device size, Growth of Portability, Reliability and Battery size. Every digital system nowadays is strongly dependent on the memory. We can also say that no digital system nowadays can be built without memory. It is also the heart of any microprocessor; that is why most of the research works are in low power design of memory circuits. Herein work concentrates on the statistical analysis of SRAM cell which will consume lesser power for various temperature conditions.

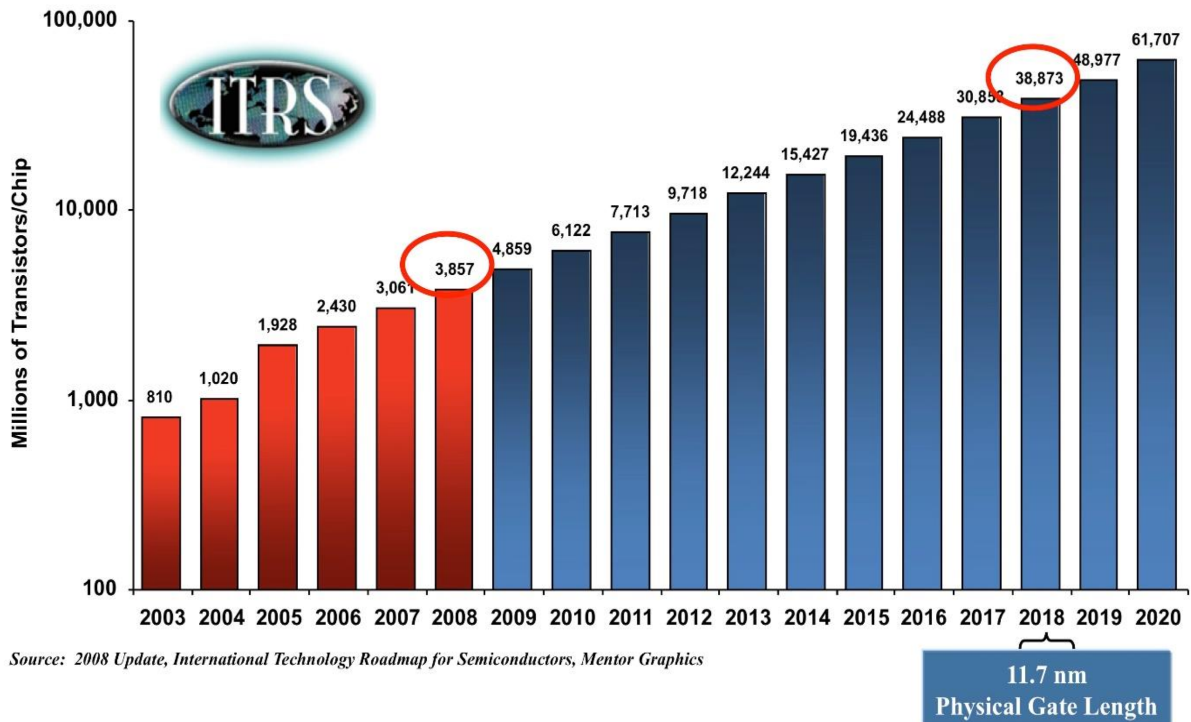


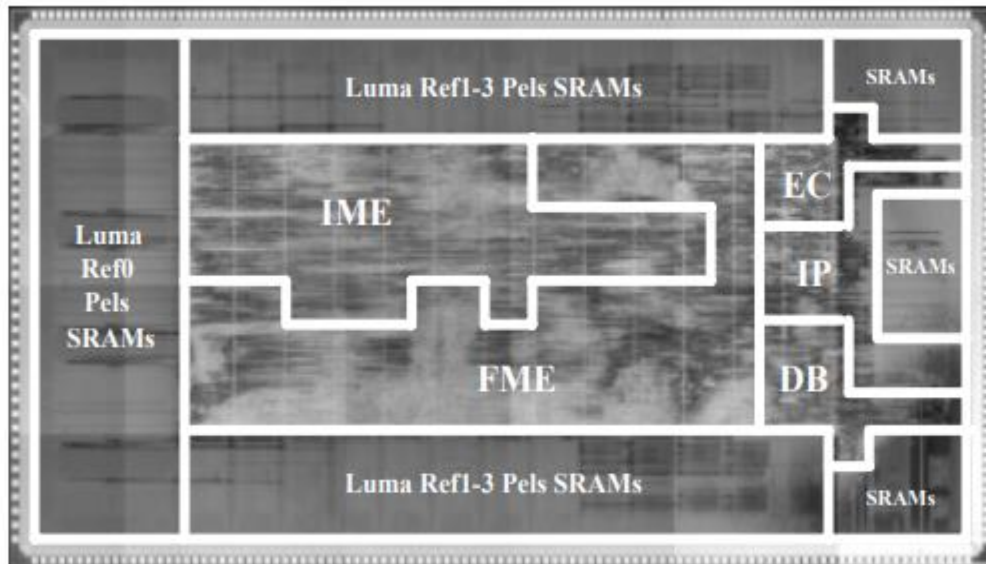
Figure 1.1 Increasing of a number of transistors/chip with respect to year according to ITRS-2005 [1]

1.3 SRAM Application in Wireless Communication Devices

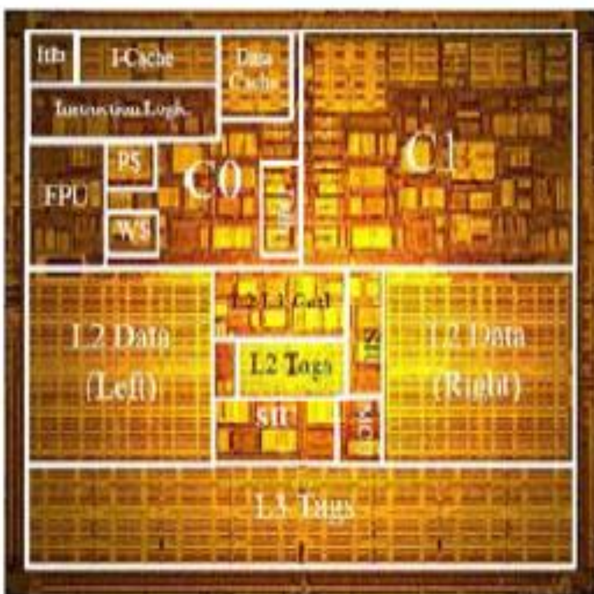
The integrability of embedded SRAMs has made it a prominent choice for the digital signal processors (DSPs) that operate along with the over-sampling digital to analog (D/A) and analog to digital (A/D) data converters. Over-sampling data converters are the most popular choices for the low-power applications where the accuracy of the conversion is a demanding requirement.

Amplitude and phase/frequency domain over-sampling data converters have been widely used in the wireless communication systems. These types of data converters are based on the noise shaping property of a closed loop system. Hence, the accuracy of the conversion is being traded off by the sampling rate of the data converter. This feature makes the sampling frequency to be several times that of the Nyquist frequency of the signal bandwidth. In return, the accuracy of the samples is relaxed [2], [3]. In the over-sampling data converters, the quantization noise is shaped such that the noise is pushed out of the signal bandwidth after its being digitized using a filter. After the signal is being digitized, it needs to be down-sampled (decimated) to the Nyquist frequency of the signal bandwidth. In order to avoid aliasing in the

down-sampling process, out of band noise needs to be suppressed. This purpose is served by decimation filters.



(a) A Video processor



(b) A Sparc processor

Figure 1.2 Two SOCs comprising SRAMs and cores presented in ISSCC'05: (a) A Video processor [4] and (b) a Sparc processor [5]

1.4 Thesis organization

The outline of the thesis is as follows. Chapter 2 discuss the literature survey. Chapter 3 discuss the basis of conventional SRAM cell operation, leakage current components inside an SRAM cell and concept of N-Curve in SRAM Cell. Chapter 4 describes the simulation result and comparison of the proposed cell with conventional 6T SRAM cell. And finally, Chapter 5 concludes the thesis and future work.

CHAPTER 2

Literature Review

Koichi-Takeda*, et al.* [6] The RSNM free SRAM cell has been proposed which have seven transistors in year 2006. The proposed cell has 23 % less area as related to conventional SRAM cell. They have fabricated a 64kb SRAM macro using CMOS 90nm technology and they have been obtained it with the minimum Vdd of 440mv with 20ns access time.

In year 2007, there is a single ended 6T SRAM cell with the write assist feature was proposed by **Richard F.hobson, *et al*.** [7]. This will reduce the problem of writing '1' through an NMOS pass transistor. Leakage and active power were also reduced and leakage power was reduced by 27 % of the conventional cell by pooling bitline charge. Standby leakage current also decreased by this method. The write power was decreased with a typical value of one-fourth and read power is reduced by the typical value of one-third as compared to standard architecture. **Govind Prasad, *et al*.** [8] an 8T SRAM cell was proposed in year 2015 to decrease the total and static power dissipation with an increase in stability by comparison to conventional SRAM cell. In this technique there was reduction of gate leakage current and the total power dissipation was reduced by 31.2 % and 40.4 % of the reduction in static power reduction by comparison with the traditional cell. The stability metrics such as SINM, SVNM, WTV, WTI also improved by 52.30 %, 11.17 %, 2.15 %, 59.1 % as related to conventional cell. Here also write delay of the proposed cell was increased due to increase in transistors. The simulation is done on Cadence Virtuoso tool using 90nm CMOS technology.

R. Niaraki, *et al*. [9] proposed a low power 9T SRAM cell in year 2016 which was compatible with bit interleaving structure. By isolating the writing and reading paths the size of access transistors was adjusted in write mode and uses the weak inverter for a better write operation. For the read operation, access buffer is used that separate the storage node transistor. The concept of virtual ground is used to prevent the leakages. The write power of the proposed cell was improved by 70 % as related to conventional SRAM cell and there was an improvement in the read power by 90.45 %.

Ruchi, *et al.* [10] There is an analytical model of WSNM for 6T SRAM cell in the subthreshold region was created in year 2018. Their results are verified and compared with simulation in different technology, i.e. using GPDK - 45nm of Cadence Virtuoso, UMC - 65nm and UMC - 130nm and their variation with supply voltage and different cell ration also analysed. This is the first model for calculating WSNM using traditional Butterfly curve and this model was authentic for all of the technology nodes. The simulation results and the model's WSNM are closely matched and give a minimum error of 0.8 % and it is also

analysed that as cell ratio increases WSNM decreases and with decreasing in supply voltage WSNM also decrease.

Vikas Nehra***, et al***. [11] As technology is scaled down the major concern was performance and stability of SRAM cell used in memory devices. There is the advancement of the microprocessor, the SRAM size increases on the chip. So to improving the SRAM cell stability, an 8T SRAM cell was proposed in this paper in year 2012 with improved stability factor at various process corners. The simulation was done on 65nm CMOS technology. In this, it is concluded that the cell with eight transistor has improved SNM as related to the conventional cell.

Rasoul Faraji, ***et al***. [12] For the low power and the high speed applications an static random acess memories cell was proposed with body biasing effect in year 2014. The control circuit is used for controlling body bias. In this cell, two wordlines are used which vary between the positive and the negative voltage level for controlling the body bias of cell's transistor. In the proposed cell the static power was decreased by the 82 % and the read performance was increased by the 40 %. The write performance is also improved by 27 % by comparison with the conventional cell.

Liang Wen, ***et al*****.** [13] proposed cell with eight transistor for low power application in year 2013 which perform the write and read operation using a single bitline. There was increase in the read stability and write ability of proposed cell. In this the feedback loop between inverter pairs are cut-off. The standby and write power is also decreased. From the simulation results, there is a 4.66 times increase in write ability of the proposed cell as related with conventional cell. The read noise margin was increased by 2.33 times and there was a reduction of 28 % in write power and standby power dissipation is reduced by 3.3 times as related to the 6T cell at 0.5 V. The simulation is done using TSMC 65nm technology.

Sayeed Ahmed ***et al*****.** [14] Based on the Schmitt trigger, a single ended 11T SRAM cell was proposed in year 2016. The purpose is to provide preferable write and read signal to noise margin and low power consumption. The variation of temperature, process, and the voltage on various parameters i.e read SNM, write SNM and hold SNM is also analyzed. The simulation is done using 45m technology and the layout is drawn for the proposed cell. It is shown that there is 2.02 times greater area of the proposed cell related to conventional cell.

Kevin Zhang ***et al*****.** [15]. In this paper, an SRAM was designed for leakage reduction with dynamic sleep transistor in year 2005. The simulation was done using 65nm CMOS technology. A chip of 70mb SRAM was fabricated using this technology. The SRAM design was optimized for performance, area and for balancing the write and read margins. The virtual ground control of the SRAM is obtained by programmable bias transistor in standby mode. The analysis shows that the SRAM leakage at 1.1v is decreased by 3-5x in data retention mode.

In year 2010, **Ming-Hsien *et al.*** [16] proposed a single ended 8T SRAM cell. There is an asymmetrical write-assist technique is used with the virtual ground and the positive feedback sensing keeper circuit to provide better write SNM and RSNM (read signal noise margin) and speed. The implementation was done using 90nm CMOS technology and implemented a 94kb SRAM test chip. From the test chip results, there is 0.2V Vdd with an operating frequency of 6.0MHz was achieved. The power consumption was 10.4μW. During post-layout simulation, the chip achieved 6MHz and 24MHz operating frequency at 200mV and 600mV.

Roghayeh Saeidi *et al*. [17] A differential 8T SRAM cell was proposed in this paper in year 2014 for the subthreshold application with improved read and write stability. To maintain the data stability in read operation the two transistors disengage the cell storage nodes. The data stability was increased at the cost of read delay. The simulation was done using 45nm CMOS technology and the worst corner Monte Carlo simulation was also done. The proposed cell have read noise margin of 74mV as compared to a 6T cell which has an 18mV. The write noise margin of the proposed cell was 92mV whereas of the conventional cell was 27mV. The cell area was increased by 1.57 times to the conventional 6T cell.

As we know that due to scaling the stability and leakage power was affected. In year 2014, **Vikas Kumar *et al.*** [18] proposed an SRAM cell to provide better stability and decrease the leakage power. There is two technique for reducing subthreshold and gate leakage current. There was a reduction in gate leakage by decreasing supply voltage and the subthreshold leakage current was decreased by increasing the voltage of ground node. From the simulation results, there is a 60-70% reduction in power dissipation for write and read operation in the proposed cell as compared to conventional cell and 40 to 60 % decreasing in leakage power. The speed is decreased by 30 to 40 %. The simulation was done using Tanner EDA tool with 180nm and 45nm at a voltage of 1.8V and 1V.

An 8T SRAM cell with dynamic feedback control was proposed by **C.B. Kushwah *et al.*** [19] in year 2016. The cell consists of single wordline to improve data stability. The comparison of the proposed cell was done with 6T and read decoupled 8T SRAM cell and it achieves WSNM of 1.4x as compared to 6T and 1.28x compared to RD - 8T at 300mV. There is a reduction in standard deviation of write SNM of the proposed cell by 0.4x compared to 6T and 0.56x as compared to RD - 8T. The read SNM was increased by 2.33x, 1.23x, 0.89x as related to 5T, 6T and RD - 8T cell. The hold noise margin was increased by 1.43x, 1.23x, 105x related to 5T, 6T and RD - 8T. The proposed cell consumed less read and write power related to 5T, 6T, and RD - 8T SRAM cell. The write power was reduced by 0.72x, 0.6x , 0.85 compared to 5T, 6T, RD - 8T and read power was reduced by 0.49x, 0.48x, 0.64x as compared to 5T, 6T, and RD - 8T.

A.Islam *et al.* [20] A technique is used for designing a variability aware SRAM cell in this paper in year 2012. The circuit was same as that of conventional SRAM cell but the access pass gate is replaced by a transmission gate. The proposed cell achieves 1.4x narrower spread in read current (I_{read}) at the

cost of 1.2 times increase in read delay. The write access time is 1.1x with 1.3x times write delay. It provides high RSNM of 1.3x at 100mv related to 6T at 75mv. The SINM of the proposed cell was 1.6x the conventional cell. The standby power was increased by 1.5 times the 6T cell.

In year 2008, **Tadayoshi Enomoto *et al.*** [21] presented a low leakage power 180nm CMOS SRAM in which the power gating technique is employed with the help of a Self controllable Voltage Level circuit by which the supply voltage level and the ground level is controlled during active and during stand - by mode. The results reported show that the measured write margin was increased and standby leakage power of the 1Kb SRAM memory cell array significantly reduced to 5.4% related traditional SRAM memory cell array at a VDD of 1.8V.

Jaydeep P. Kulkarni *et al.* [22] In this an SRAM cell was proposed in year 2007 which was based on Schmitt Trigger and that incorporates a built-in feedback mechanism, achieving 56 % improvement in SNM. The data retention capability was improved at low voltage related to conventional cell, low voltage/low power operation, and improvement in process variation tolerance lower read failure probability. They report that at iso area and iso read failure probability the proposed memory bit cell operates at a lower (175 mV) VDD with 18% decreasing in leakage and 50 % reduction in write/read power related to the conventional 6T cell. As per their simulation results, the proposed memory bit cell retains data at a supply voltage of 150 mV. The simulation of SRAM with the proposed memory bit cell was done at 160 mV in 0.13µm CMOS technology.

From the above literature survey it is clear that lot of research has been done and still going on in the area of low power SRAMs.

- The techniques reported in literature are not efficient to reduce the power with improved stability.
- They involves the voltage measurement, it does not give any information on the cell currents.
- There cannot be a single technique that will guarantee the best static and total power reduction.
- In lowering the power dissipation it is necessary to maintain the performance parameters acceptable.
- Voltage scaling causes bottlenecks in memory system.

CHAPTER 3

Introduction to SRAM Cell

3.1 Random access memory (RAM)

RAM is a form of computer data storage that stores data and machine code currently being used. A RAM device allows data to be read or write in almost the same amount of time irrespective of the physical location of data inside the memory. RAM contains multiplexing and demultiplexing circuitry, to connect the data lines to the addressed storage for reading or writing the entry. Traditional RAMs have been subdividing into the static RAMs (SRAMs) and the dynamic RAMs (DRAMs). The DRAMs consist of a single transistor and a capacitor and data are stored as a charge on a capacitor. SRAMs use bistable element such as an inverter loop to store the cell state as a voltage differential. These elements can hold their state without the need for refreshing as long as power is applied. The term dynamic refers to the need to periodically refresh the charge on non ideal storage capacitors. The basic SRAM cell is more complex than DRAM cell. They consume more area as related to DRAM cell. In system design it is important to use SRAM or a DRAM due to following design challenges include cost, volatility, density, speed and other features. All of these circumstance should be considered before the selection of memory to the system. This research work focusses on the design of write/read SRAMs.

3.1.1 SRAM and DRAM

BASIS FOR COMPARISON	SRAM	DRAM
Used in	Cache memory	Main memory
Density	Less dense	Highly dense
Construction	Complex and uses transistors and latches	Simple and uses capacitors and very few transistors.
A single block of memory requires	6 transistors	Only one transistor
Charge leakage property	Not present	Present hence require power refresh circuitry
Power consumption	Low	High

3.2 Conventional 6T SRAM Cell

The 6T SRAM cell [17] used to store one-bit information. It has two access transistor (M6 & M5) and the core cell is formed by two CMOS inverters (M1, M4, M2, M3) as shown in Figure 3.2 [23]. The transistors

(M6 & M5) are connected with the word line (WL). One of the terminals of the access transistor is attached to the bit lines (BL & BL_BAR) to perform the read & write operation. The storage cell is composed of two back-to-back inverters (M1 and M2, M3 and M4). PMOS transistors M2 and M4 are known as the load transistors. NMOS transistors M1 and M3 are known as the drive transistors. The transistors M5 and M6 is used as the access transistors.

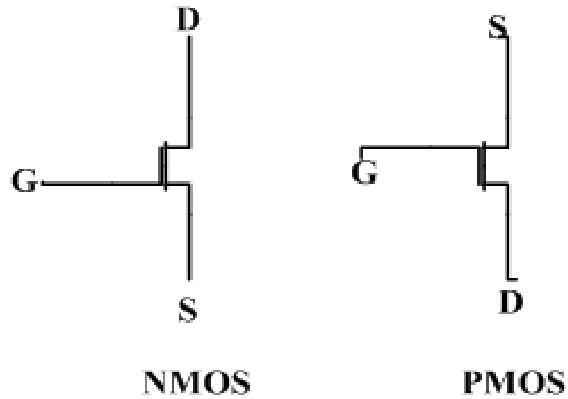


Figure 3.1 Symbols of NMOS and PMOS

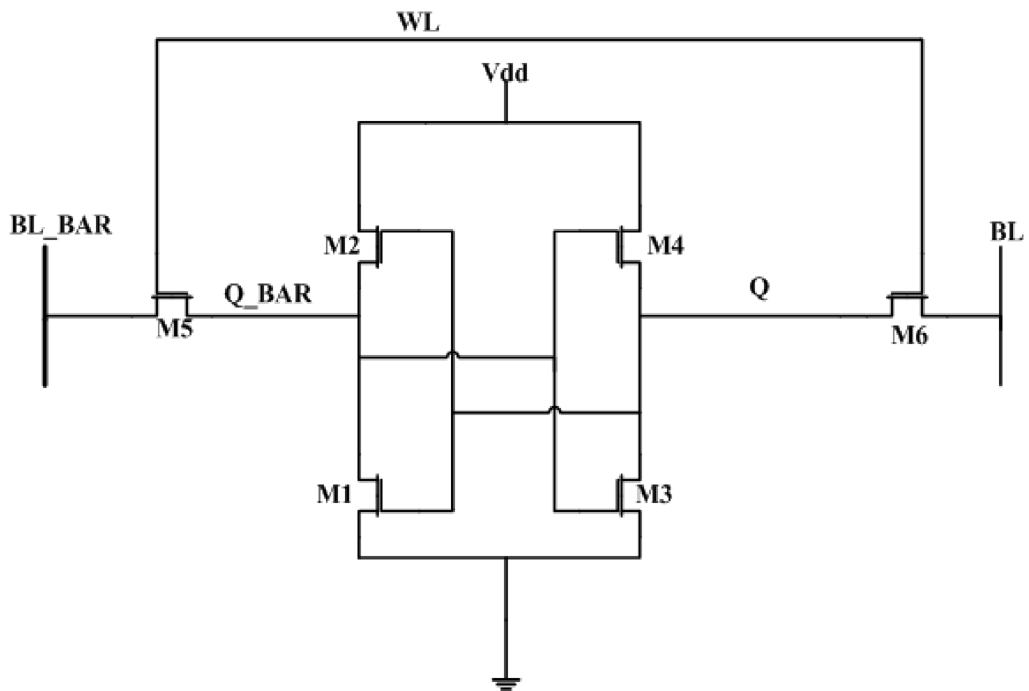


Figure 3.2 Circuit of 6T SRAM Cell

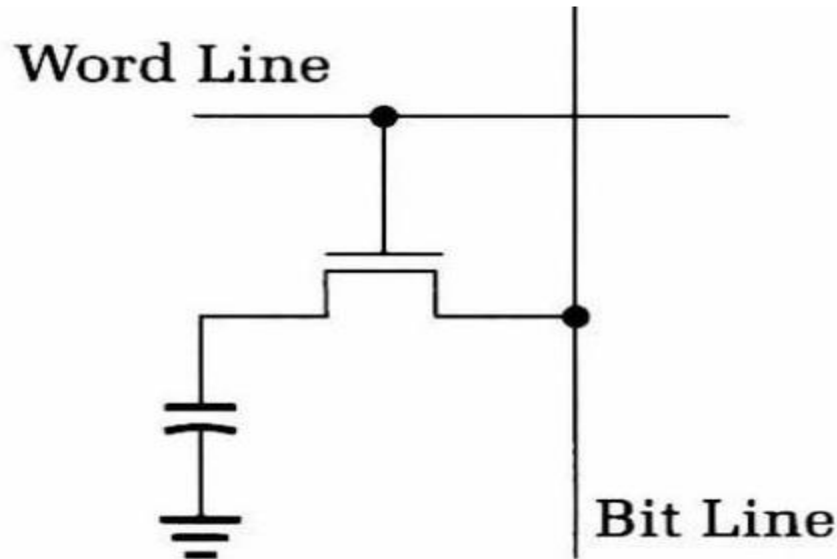


Figure 3.3 Schematic of DRAM Cell

The 6T SRAM cell has three operation modes i.e. read, write, and hold. Since an SRAM array contains many thousands (sometimes millions) of cells, and only one word can be accessed at a given time, an SRAM cell will typically be in the unaccessed retention mode for the vast majority of the time. In this operation the wordline (WL) is turned off, isolating the complementary bitlines (BL/BLB) from the storage cell.

3.2.1 Operations in 6T SRAM Cell

A Read operation

Consider a data read operation, shown in Figure 3.4 assuming that logic '0' was stored in the cell. The transistors M2 and M5 are turned off, while the transistors M1 and M6 operate in linear mode. Thus internal node voltages are V1 = 0 and V2 = VDD before the cell access transistors are turned on. The active transistors at the beginning of data read operation are shown in Figure 3.4. After the pass transistors M3 and M4 are turned on by the row selection circuitry, the voltage CBb of will not change any significant variation since no current flows through M4. On the other hand, M1 and M3 will conduct a nonzero voltage and the current level of CB will initiate to drop slightly. The node voltage V1 will increase from its initial value of '0' V. The node voltage V1 may exceed the threshold voltage of M2 during this process, forcing an unintended change of the stored state. Therefore voltage must not exceed the threshold voltage of M2, so the transistor M2 remains turned off during the read phase. The transistor M3 is in saturation whereas M1 is linear.

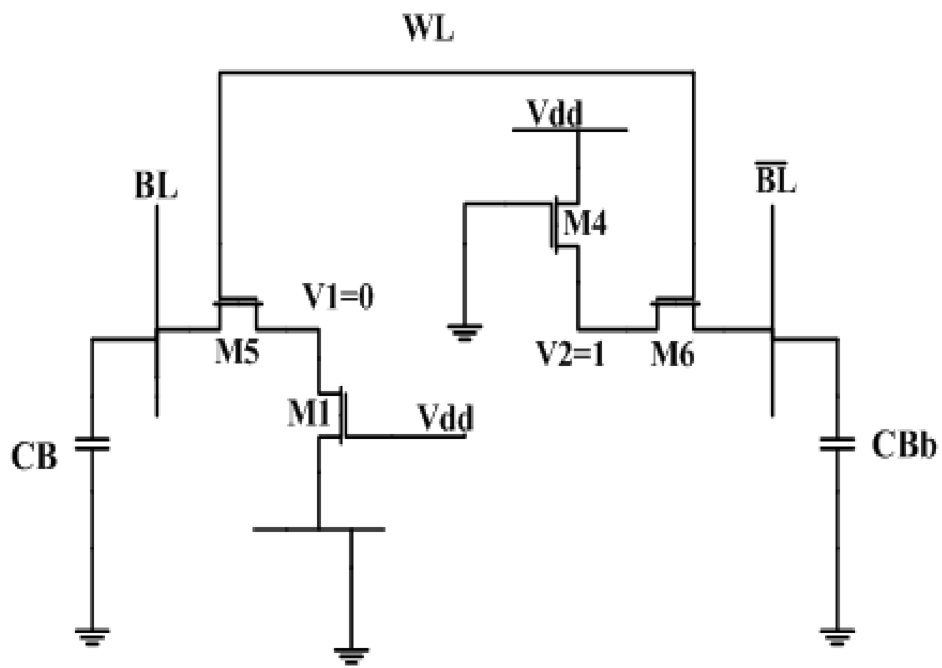


Figure 3.4 Read Operation

B Write Operation

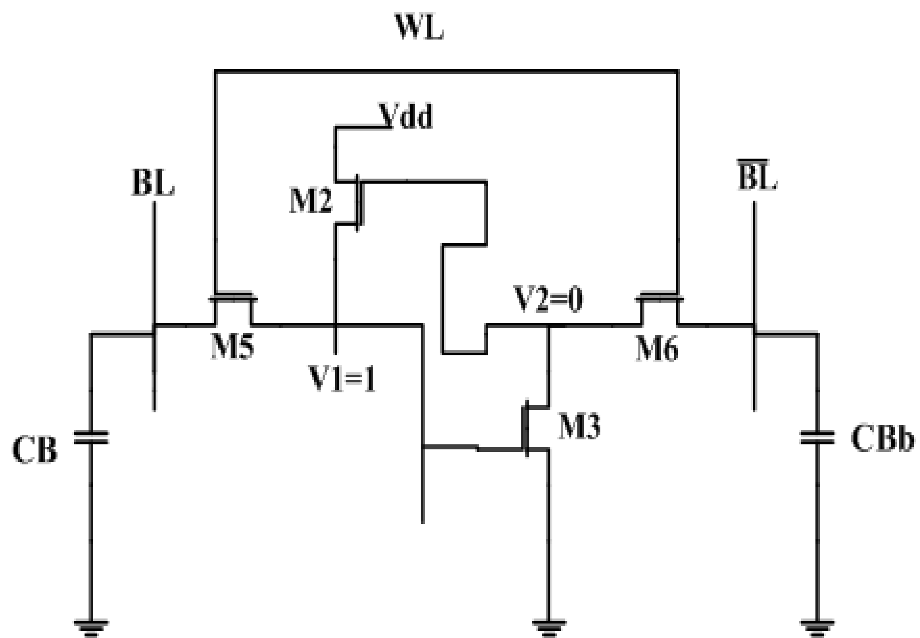


Figure 3.5 Write Operation

Consider the write '0' operation let logic '1' is stored in the SRAM cell initially. The transistors M1 and M6 are turned off, while M2 and M5 are operating in the linear mode. Figure 3.5 shows the voltage levels in the CMOS SRAM cell at the beginning of the data write operation. Thus the internal node voltage V1 = VDD and V2 = 0 before the access transistors are turned on. The column voltage Vb is forced to '0' by the write circuitry. Once M3 and M4 are turned on, we expect the nodal voltage V2 to remain below the threshold voltage of M1.

The voltage at node 2 would not be sufficient to turn on M1. To change the stored information, i.e., to force V1 = 0 and V2 = VDD, the node voltage V1 is to be reduced below the threshold voltage of M2, so that M2 turns off. When $V_1 = V_{tn}$ the transistor M5 operates in the saturation region while M3 operates in the linear region.

C Hold Operation

The circuit is in standby mode when the wordline (WL) is off and the access transistors (M5 &M4) are also off. The data is held in the latch.

3.2.3 Pull up ratio and Cell ratio

To assess the stability of the stored data during a read operation, cell ratio is defined as the ratio of the size of driver transistor to the size of the access transistor.

$$CR = \frac{W_1/L_1}{W_5/L_5}$$

Pull up ratio is related to the stability of write operation, it is the ratio of the size of load transistor to the size of the access transistor.

$$PR = \frac{W_4/L_4}{W_6/L_6}$$

3.3 Architecture of an SRAM Unit

The periphery blocks in an SRAM unit facilitate access to the cells for the read or write operation. In practice, multiple bits are accessed for the write or read operation at the same time. The group of bits that are accessed at the same time forms a word. Depending on the application, the word size, M, usually varies from a dozen bits to 64 bits. In regular SRAMs only one word is accessed at a time. The number of words that are accommodated in the unit specifies the length of the address field, N. However, The total number of cells in an array can be calculated as M x N.

An SRAM unit consists of several periphery blocks. An array accommodates the plurality of cells. A decoder decodes the binary encoded input address to indicate the physical location of the addressed cell (or word.) Sense amplifiers (SA) and write drivers interface with the bitlines to communicate with the cell in

read and write operations, respectively. A timing control unit generates the proper timing signals for the activation of the wordline, SA or write driver during the read or write operation, respectively.

3.3.1 Row Decoder and Column Multiplexer

Multiple words are placed in one row in applications with usual word size($M < 128$). Different bits of the words on a row are interleaved to share periphery circuits such as SA, write driver and row decoder. Figure. 3.6 shows an array in which each row accommodates 2^n words and each word comprises M bits. The first bit of all the 2^n words on the same row, i.e., b_0 of all 2^n words, are placed beside each other. The next bit of all words is placed at the neighboring set of cells. Hence, only one SA and write driver serves the first bit, B_0, of all the 2^n words on the same row. A column multiplexer selects the bitline that is connected to the SA or write driver. It is clear that for a word size equal to M there are M x 2^n cells on the same row (i.e., M x 2^n columns in the block).

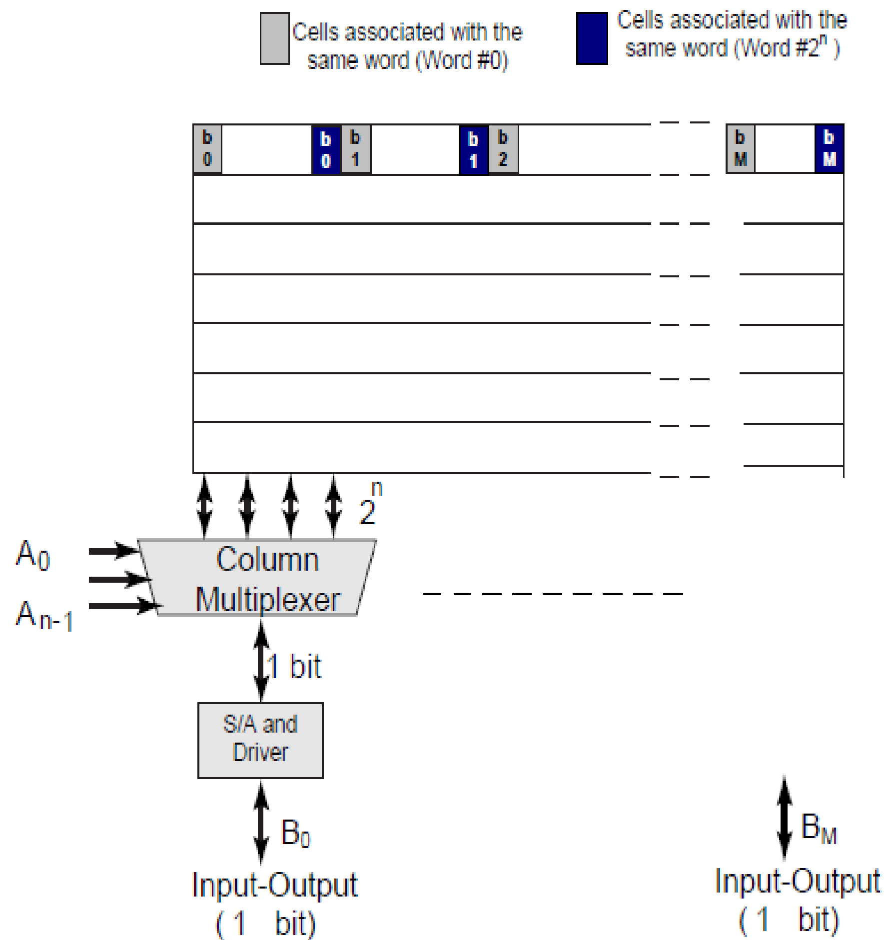


Figure 3.6 The concept of interleaving in an SRAM array [24]

The location of the accessed word is specified by the address inputs of the SRAM unit. Specified by A_0 – A_{K-1}, the address input is a binary encoded number with the bitwidth of $K = \log_2(N)$ bits. The address input is decoded to locate the word that is desired for an access. The word can be located by specifying the row on which the desired word is placed and the columns on which different cells corresponding to different bits of the same word are placed. Therefore, the K address bits are divided into column address bits A_0 – A_{n-1} and row address bits A_n – A_{n+m-1} where K= n + m. Figure 3.7 clarifies this technique. The column address bits drive the column multiplexer and specifies which word in the row is accessed. Driven by the row address bits, the row decoder specifies the row in which the accessed word is located by activating the wordline of that word

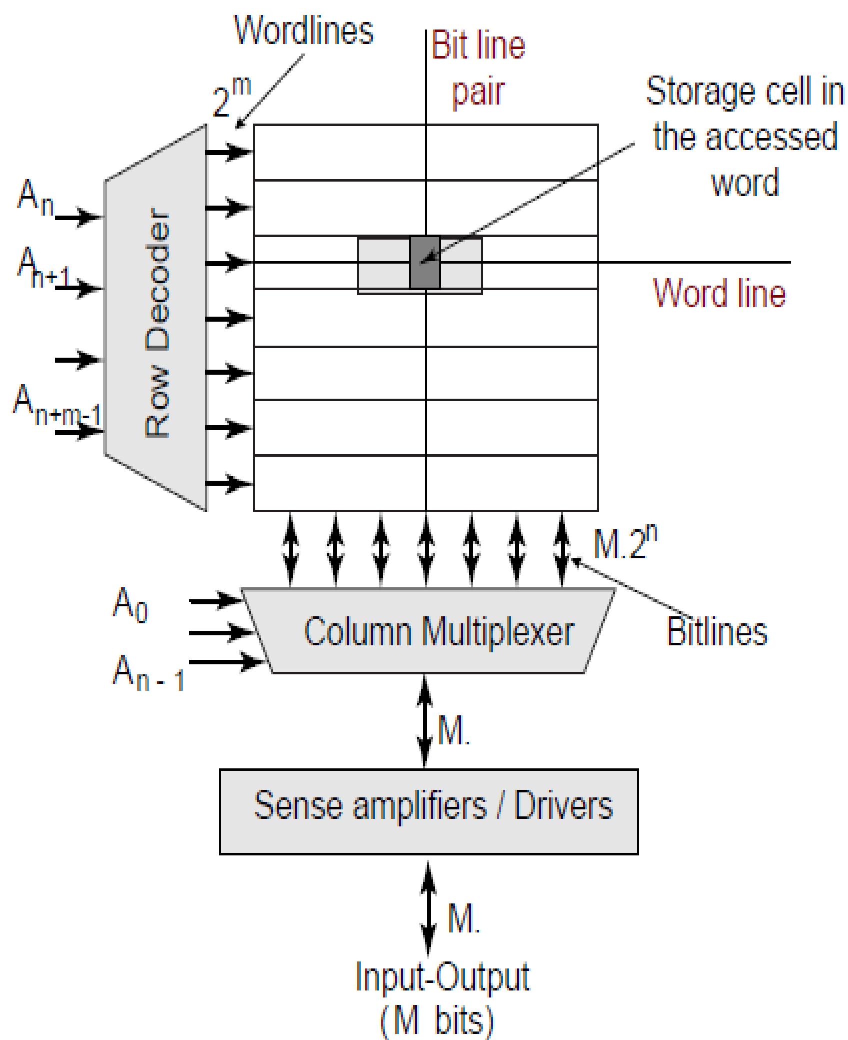


Figure 3.7 Utilization of a row decoder and a column multiplexer to activate the respective wordline and bitline according to the address [24]

3.4 Different types of SRAM Cell

3.4.1 4T SRAM Cell

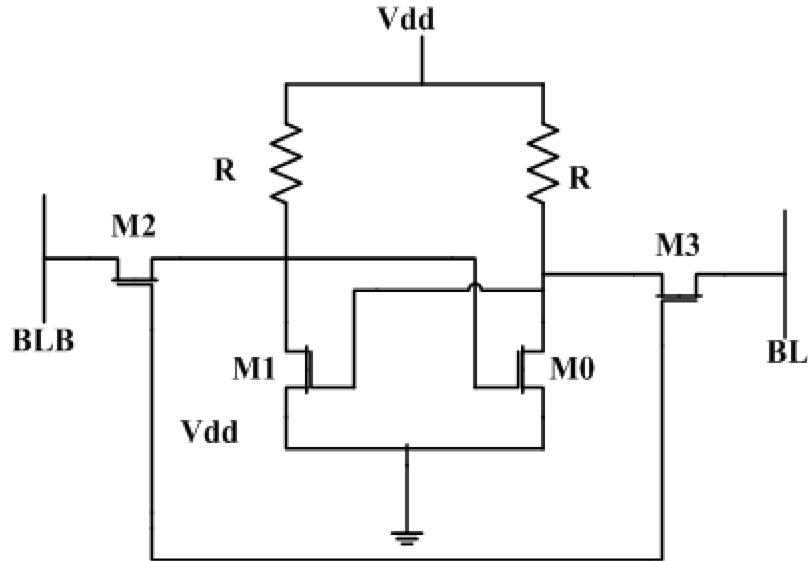


Figure 3.8 Schematic of 4T SRAM Cell

In this cell two PMOS transistors M0 and M1 are used as driver and two NMOS transistors M2 and M3 used as access transistor as given in Figure 3.8. The bitline is precharged to ground instead of Vdd. The principal drawback of using 4T SRAM is that the static power is increased due to constant current flow through one of the pull-down transistors.

3.4.2 7T SRAM Cell

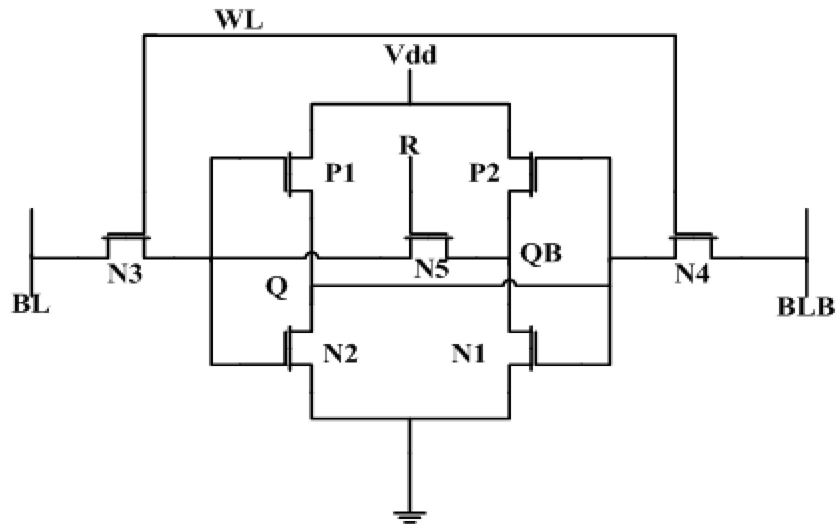


Figure 3.9 Schematic of 7T SRAM Cell [25]

This cell is basically a modification of 6T SRAM cell. Before write operation, the feedback connection between two inverters is cut off. The feedback connection and disconnection is done by using NMOS transistor (N5) as given in Figure 3.9 and bitline bar (BLB) is used for write operation [25].

3.4.3 8T SRAM Cell

In this cell, two more NMOS transistor are connected with 6T SRAM cell as given in Figure 3.10. The separated write and read line are controlled by write (WWL) and read (RWL) wordlines. During write and read operation they are used for accessing the bit cell.

Figure 3.10 Schematic of 8T SRAM cell [26]

In 8T SRAM cell, write and read operations of a standard 6T SRAM bit cell are de-coupled by creating an isolated read buffer or read port (comprised of two transistors, M8 and M7). De-coupling of write and read operations yields a non-destructive read operation or SNM-free read stability. An additional leakage current path is introduced by the separate read-port which increases the leakage current as related to conventional 6T bit cell. Therefore, an increased area overhead and leakage power make this design rather unattractive, since leakage power is a critical SRAM design metric, particularly for highly energy constrained applications.

3.5 N-Curve Analysis

For stability of cell, the N-Curve [27] is one of inline tester method for cell stability whereas SNM does not provide a simple means of its inline measurement. Signal to noise margin (SNM) is a static approach that is the butterfly curve method [28] as given in Figure 3.11 and it only involves the voltage measurement,

it does not give any information on the cell currents. The set of NC-parameters are SVNM, SINM, WTV, WTI [29].

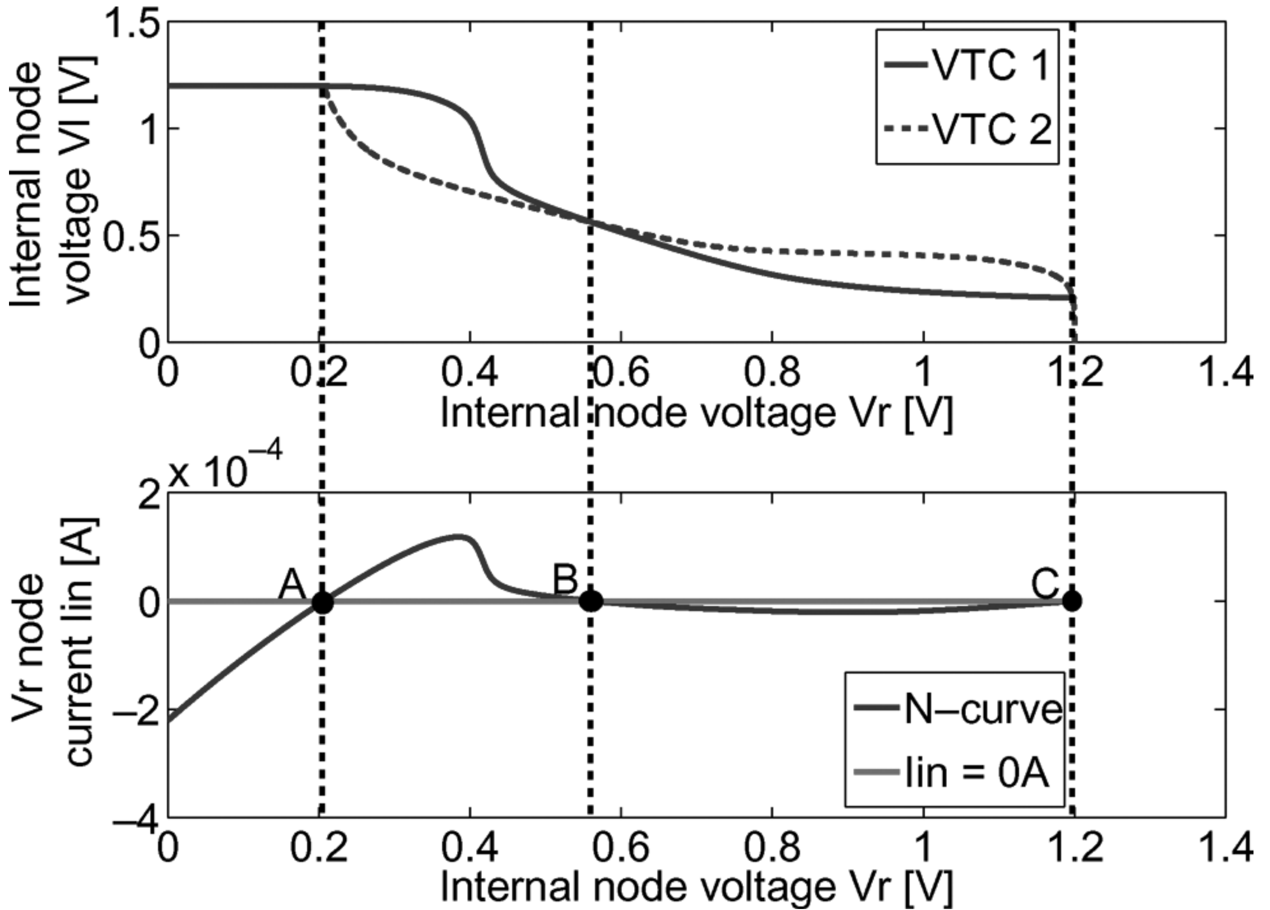


Figure 3.11 The N-curve and the butterfly curve of the Cell [26] and [27]

SVNM is defined as the DC noise voltage which is tolerable before there is a change in its content [30]. Write trip voltage (WTV) is maximum voltage required on the bit line to flip the content of the cell. Write trip current (WTI) is the amount of current which is required for writing to the cell when both lines are charged to Vdd. SINM is the required current which is needed to change the state of the cell [30]. In Figure 3.11 the voltage difference between point A and B is the Static Voltage Noise Margin (SVNM). The maximum peak current between point A and B is the Static Current Noise Margin (SINM). The write ability of the SRAM cell was also provided by N-curve. The voltage difference between point B and C is the Write Trip Voltage (WTV). The maximum negative peak current is between point B and C is the Write Trip Current (WTI). A stable SRAM cell must have high SVNM and high SINM. So SPNM which is the product of SVNM and SINM must be high for a high stable

cell. WTV and absolute value of WTI should be small for a better writable cell. Hence WTP, the product of WTV and WTI should be smaller for a better writable cell.

3.6 Sources of power dissipation

The main objective is to reduce power dissipation in digital designs. In CMOS circuits the major sources of power dissipation are described by

$$P_{avg} = P_{short\text{-}circuit} + P_{leakage} + P_{static} + P_{dynamic} \quad (3.1)$$

P_{avg} is the average power dissipation, $P_{short\text{-}circuit}$ is the short-circuit current power dissipation when there is a direct path from power supply down to the ground, $P_{dynamic}$ is the dynamic power dissipation due to switching of transistors, $P_{leakage}$ is the power dissipation due to leakage currents, and P_{static} is the static power dissipation.

3.6.1 Short-circuit power dissipation

The short-circuit power consumption, $P_{short\text{-}circuit}$, is caused by the current flow through the direct path existing between the power supply and the ground during the transition phase. Consider again the CMOS inverter shown in Figure 3.10. When the input signal changes from the logic value '1' to the logic value '0', or vice versa, there exists a very small time interval during which both NMOS and PMOS transistors are ON, and hence a short-circuit current flow between the power supply and the ground. Figure 3.12 illustrates the short-circuit current effect in a CMOS inverter. More specifically, if the rising input voltage exceeds the threshold voltage, V_{thn}, the NMOS transistor of the inverter circuit starts conducting, while the PMOS transistor conducts until the input voltage reaches to the value of (V_{dd} - | V_{thp} |). Hence, there exists a time interval where both transistors are turned on. As the capacitance C_L is discharged through the NMOS transistor, the output voltage starts decreasing. The drain-to-source voltage drop of the PMOS transistor becomes nonzero, which allows the PMOS to conduct as well. The short-circuit current is ceased when the input voltage transition is completed and the PMOS is turned off. Considering a symmetrical inverter and identical rise and fall times, a similar situation occurs for the short-circuit current component deriving from the falling edge of the input signal, where the output waveform starts rising and both MOSFET transistors are ON. The average of both the short-circuit current component of the rising edge of the input signal and the corresponding current component from the falling edge determines the total amount of power drawn from the power supply. The short-circuit current is especially dominant when the output load capacitance is small, and/or when the input signal rise and fall times are large. Consider symmetric fall and rise delays and threshold voltages, the time averaged short-circuit current drawn from the power supply and the short-circuit current power dissipation of a CMOS inverter can be approximated by [31].

$$I_{short\text{-}circuit} = K/V_{dd} \cdot (V_{dd} - 2V_{th})^3 \cdot \tau \cdot N \cdot f \quad (3.2)$$

$$P_{short\text{-}circuit} = K \cdot (V_{dd} - 2V_{th})^3 \cdot \tau \cdot N \cdot f \quad (3.3)$$

respectively, where V_{th} is the threshold voltage of the NMOS and PMOS transistors, K is a constant that depends on the transistor sizes, as well as on the technology, τ is the rise or fall time of the input signal, f is the clock frequency and N is the average number of transitions in the inverter's output.

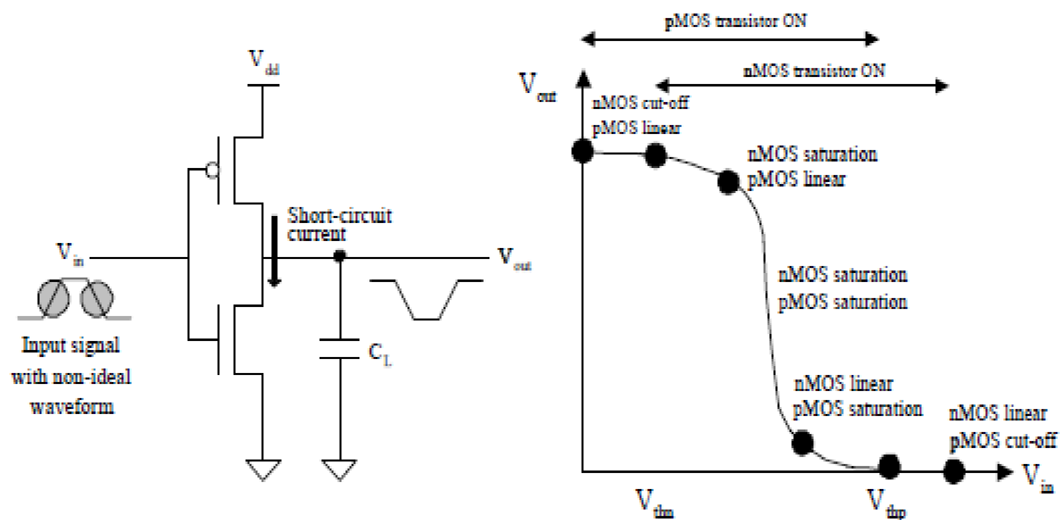


Figure 3.12 CMOS inverter transistors conduct simultaneously a short-circuit current

Reduction in the short-circuit power dissipation can be achieved by applying various techniques. From equation 3.3 it is obvious that, reducing the transistor ratio and scaling down the technology the switched capacitance and supply voltage is reduced. The $P_{short\text{-}circuit}$ is linearly proportional to the input signal rise and fall times and therefore, reducing the input transition times, the short-circuit current decreases. It should be stressed that short-circuit power dissipation exists in static CMOS logic families, but not in dynamic logic gates. Indeed, there is no direct current path between V_{dd} and ground in dynamic logic gates, because the precharged and evaluated transistors should never be simultaneously ON. Otherwise, they would function incorrectly.

3.6.2 Dynamic Power dissipation

The dynamic power dissipation $P_{dynamic}$ is caused by the charging and discharging of capacitances in the circuit. We will illustrate the computation of dynamic power dissipation through the example of a CMOS inverter driving a load capacitor C_L as it is shown in Figure 3.13. The output capacitor C_L represents the cumulative effect due to parasitic capacitances of the NMOS and PMOS transistors (source and drain diffusion to bulk), the capacitance associated with internal and external wires of the inverter cell, and the input capacitance (gate to bulk) of the circuits driven by the inverter. We consider the operation of a CMOS inverter assuming that the circuit is initially in a steady state, having as input the logic value '1' and, obviously as, output the logic value '0'. In this case, the output capacitor is discharged. When the input waveform undergoes a falling transition, the PMOS transistor conducts (ON) and the NMOS transistor turns off, as it is depicted in Figure 3.13(b).

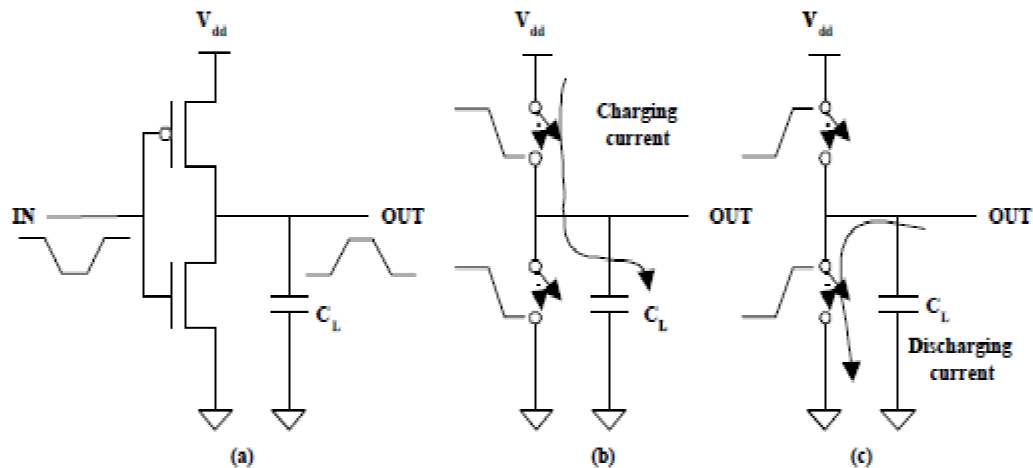


Figure 3.13 The operation of a CMOS inverter: (a) CMOS inverter, (b) Charging phase, and (c) Discharging phase

The current drawn from the power supply charges now the capacitor C_L up to V_{dd}.. During this charging process, the energy drawn from the power supply is $C_L \cdot V^2_{dd}$,, of which half is stored in the capacitor C_L and the other half is dissipated in the parasitic capacitances of PMOS transistor and the interconnect. When the input waveform undergoes a rising transition, the NMOS transistor conducts and the PMOS transistor turns off, as it shown in Figure 3.13(c). Now, there is a current path directly from the output capacitor to the ground and, thus, a discharging current flow through this path. The energy $\frac{1}{2} C_L . V^2_{dd}$ stored in the load capacitor is dissipated into the NMOS transistor as well as in the interconnect. Therefore, the dynamic power dissipated by a CMOS inverter over a time interval [0, T] can be computed by:

$$P_{dynamic} = C_L \cdot V^2_{dd} \cdot N_{0\rightarrow 1} \cdot \frac{1}{T} \quad (3.4)$$

Where $N_{0\rightarrow 1}$ is the number of rising transitions at the inverter's output, or equivalently the number of times C_L is charged, over the period [0, T]. Without loss of generality, we assume that the inverter operates in a clock frequency f, and that the number of rising transitions is half the total number of transitions. Thus, equation 3.4 may be rewritten as follows [32], [33] :

$$P_{dynamic} = C_L \cdot V^2_{dd} \cdot N \cdot f \quad (3.5)$$

where N is the average number of transitions per clock cycle at the inverter's output, and it will, henceforth, be referred to as the switching activity.

The dynamic power dissipation is the dominant factor compared with the other components of power dissipation in digital CMOS circuits. For technologies up to 0.35 µm, the dynamic dissipation is about 80% of a circuit's total dissipation. As the technology scales down, i.e. for submicron technologies, the contribution of dynamic power dissipation also increases because of increased functionality requirements and the clock frequencies [34]. Consequently, the majority of existing low power design and power estimation techniques focuses on this dynamic component of dissipation.

- **Power Reduction Approaches of Dynamic dissipation**

Equation 3.5 derived for the average switching power dissipation of CMOS logic gates indicates that. $P_{dynamic}$ is proportional to the load capacitance C_L, the square of V_{dd}, the switching activity and clock frequency f. Consequently, the power reduction can be achieved by various manners:

- Reduction of output capacitance (C_L)
- Reduction of power supply voltage (V_{dd})
- Reduction of the average number of transitions per clock cycle (N) (or switching activity) and reduction in the clock frequency.

A very popular low power strategy aims at the reduction of the effective capacitance or switched capacitance, which is defined as the product of output capacitance times switching activity, i.e. $C_L \cdot N$.

3.6.3 Leakage Power Dissipation

The NMOS and PMOS transistors used in a CMOS logic circuit commonly have nonzero reverse leakage and subthreshold currents. Having a CMOS integrated circuit, which encompasses a very large number of transistors, these currents can contribute to the total power dissipation even when the transistors are not performing any switching action. The magnitude of the leakage currents depends mainly on the used technology parameters.

The leakage power dissipation $P_{leakage}$ is caused by two types of leakage Currents [32]:

- the reverse-bias diode leakage current at the transistor drains, and
- the subthreshold current through a turned off transistor channel.

However, these current components are technologically-controlled and, thus, the designer can do a number of things their minimization. Diode leakage current occurs when a transistor is turned off, and the other transistor ON charges up/down the drain of the former respect to its substrate potential.

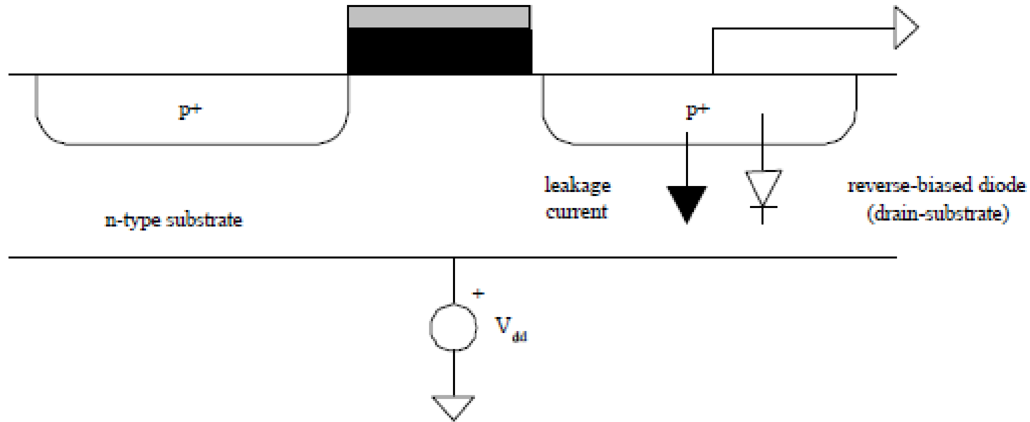


Figure 3.14 The leakage current in a reverse biased PMOS transistor [32]

Figure 3.14 is shown a PMOS transistor with a negative gate bias V_{dd} in respect to its substrate. Hence, the diode formed by the drain diffusion and the substrate is reverse-biased. We know from diode's theory that the reverse bias current is given by:

$$I_{leakage} = I_S\left(\frac{v_{dd}}{e^{v_t}} - 1\right) \tag{3.6}$$

where I_S is the reverse saturation current, V_{dd} is the bias voltage, and $V_t = kT/q$ is the thermal voltage. For engineering purposes, we may assume that the leakage current is equal to the reverse saturation current.

The reverse saturation current is given by [35]

$$I_S = q\, \eta^2_i A\left(\frac{D_p}{N_d W_n} + \frac{D_n}{N_a W_p}\right) \tag{3.7}$$

where q is the electron charge, η_i is the intrinsic carrier concentration, A is the area of pn junction diode (actually the drain area), D_p and D_n are the electron and hole diffusion coefficients, respectively, N_d and N_a are the donor and acceptor concentrations, respectively N_d and N_a are the depletion layer widths of the p and

n sides of pn junction diode, respectively. For example, assuming an average drain of 10 μm, the total leakage current for one-million transistors is about 25 μA.

The second current component is the subthreshold leakage current, which occurs due to carrier diffusion between the source and the drain of MOS transistor, when the gate-source voltage V_{gs}, exceed the weak inversion point, but it is still below the threshold voltage V_{th}, above which the carrier drift mechanism is dominant. The behavior of a MOSFET transistor in the subthreshold operation region is similar to a bipolar transistor, and the sub-threshold current is exponentially dependent on the gate-source voltage (Figure 3.15). The magnitude of the subthreshold current may increase significantly when the gate to source voltage is smaller than, but very close to, the threshold voltage of the transistor. This phenomenon results in a power dissipation due to subthreshold leakage, whose magnitude is comparable with the dynamic power dissipation.

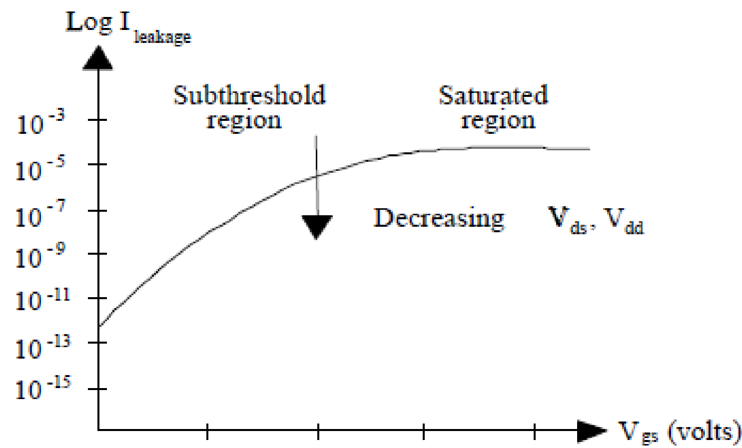


Figure 3.15 Subthreshold leakage with respect to gate-source voltage

The concept of subthreshold leakage current is illustrated in Figure 3.16. The current in the subthreshold region is given by [36]:

$$I_{ds} = Ke^{(Vgs-Vth)/\eta VT}(1 - e^{-\frac{Vds}{VT}}) \quad (3.8)$$

Where K is a function of the technology, V_T is the thermal voltage, Vth is the threshold voltage and $\eta = 1 + \Omega t_{ox}/D$, where t_{ox} is the gate oxide thickness, D is the channel depletion layer width, the quantity $\Omega = \varepsilon_{Si} / \varepsilon_{ox}$. For $V_{ds} >> V_T$, the quantity $(1 - e^{-Vds/VT}) \approx 1$; i.e., the drain-to-source leakage current does not depend on the drain-source voltage for V_{ds}, for $V_{ds} \approx 0.1$ volts.

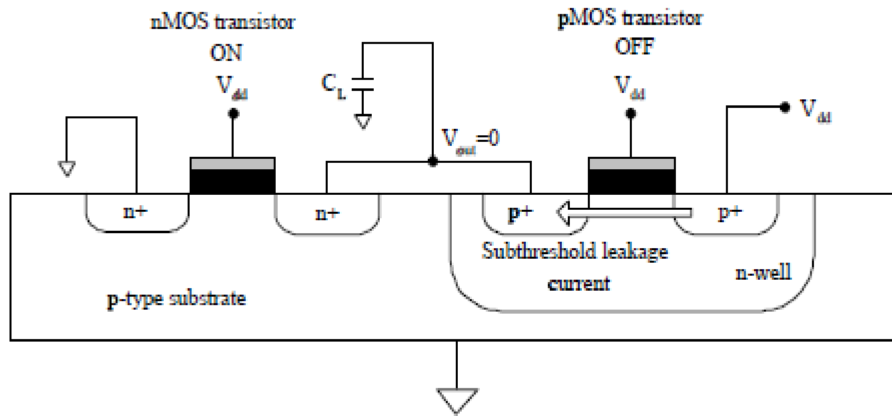


Figure 3.16 Subthreshold leakage current path in a CMOS inverter with high Vdd [36]

3.6.4 Techniques to reduced leakage and dynamic power

- Clock gating: Clock gating is a methodology of turning off the clock for a particular block when it is not needed and is used by most SoC designs today as an effective technique to save dynamic power [37].
- Multi- Vth optimization: In this technique there is replacement of cell i.e. cell with faster low-Vth which consume more leakage power by cell which consume low leakage power i.e. cell with slower high Vth. Since the High-Vth cells are slower, this swapping only occurs on timing paths that have positive slack and thus can be allowed to slow down (Figure 3.17 [37])

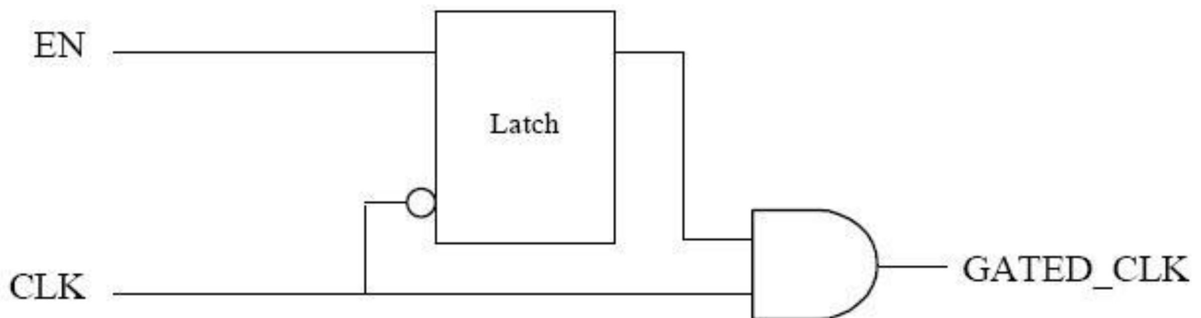


Figure 3.17 Clock Gating [37]

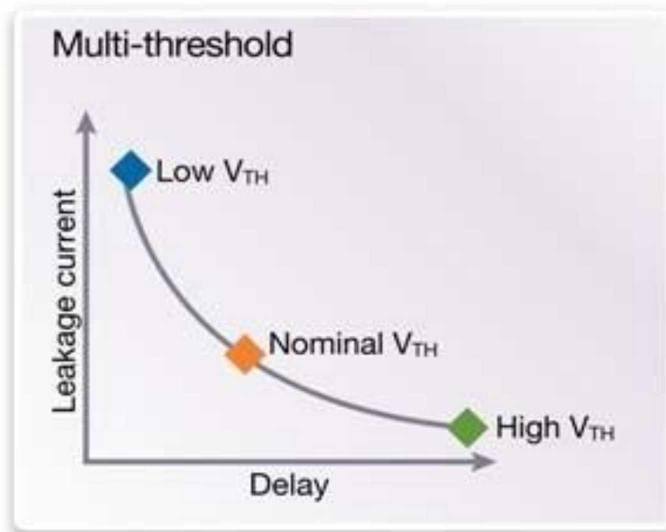


Figure 3.18 Multi-Vt optimization

As technologies reduces, leakage power consumption has increases exponentially, therefore power reduction techniques to be used. Similarly, clock frequency increases have caused dynamic power consumption of the devices to outstrip the capacity of the power networks that supply them, and this becomes especially acute when high power consumption occurs in very small geometries, as this is a power density issue as well as a power consumption issue.

- Dynamic voltage and frequency scaling: In this method when the devices is in operation, then the operating voltage and/or frequency at which a device operates is modified such that the minimum voltage and/or frequency needed for proper operation of a particular mode is used.

3.6.5 Static Power Dissipation

When the CMOS circuit is in steady state there was no power dissipation in the device. This is the most striking feature of CMOS technology. The actual operation of a CMOS circuit is slightly different. More specifically, we will deal with degraded voltage levels feeding into static complementary gates and pseudo-NMOS logic families. We will illustrate the phenomenon of static power dissipation due to degraded input signals through the example shown in Figure 3.19.

A pass NMOS transistor drives an inverter. From basic CMOS circuit theory, we know that the voltage value at the node A is $V_{dd} - V_{thn}$, i.e. it is degraded. Since the inverter's input is high, i.e $V_{dd} - V_{thn}$, its output should be low.

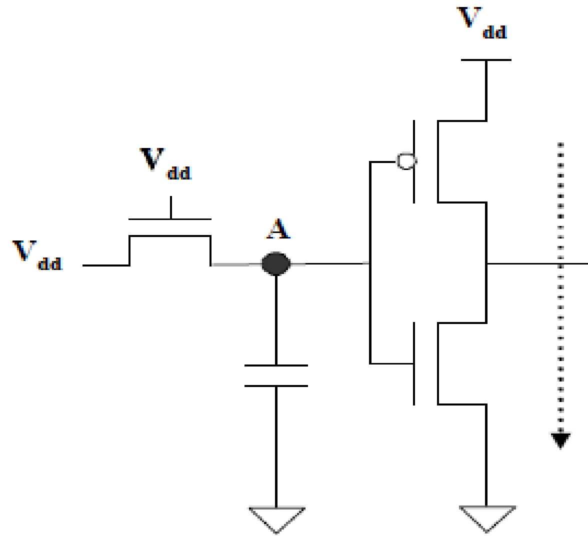


Figure 3.19 Degraded voltage level as input signal to an inverter results in static power consumption

However, the PMOS transistor will be weakly ON ($|V_{gs} - V_{thp}| \approx 0$) and, thus, conducting static current from power supply to ground rails. The associated static power dissipation might be significant if the inverter operating frequency is low.

CHAPTER 4

Results and Performance Analysis

4.1 Power Analysis

Static power essentially consists of the power used when the transistor is not in the process of switching and is essentially determined by the formula

$$P_{static}=I_{static}* V_{dd} \quad (4.1)$$

In CMOS circuits the power dissipation is described by:

$$P_{average} = P_{dynamic} + P_{shortcircuit} + P_{static} \quad (4.2)$$

$P_{average}$ is the average power dissipation, $P_{dynamic}$ is the dynamic power dissipation due to switching of the transistor [38], $P_{shortcircuit}$ is the short circuit current power dissipation when there is a direct current path from the power supply to the ground and the P_{static} is the static power dissipation.

The schematic of traditional cell has been shown in Figure 4.1 The whole circuit has been analysed with 90 nm CMOS technology with a supply voltage of V_{dd} = 1V. The length and width are L = 100 nm and W = 120 nm respectively. The power analysis has been shown in Table 1. There is a reduction in total power and static power dissipation by 46.4 % and 30.2 % respectively as comapred to traditional SRAM cell. When compared with the reference cell, the static power and total power of proposed cell have decreased by 43.9% and 21.9 % [8] respectively as shown in Table 4.1. The circuit diagram of the reference cell and the proposed cell has been shown in Figure 4.2 and Figure 4.3.

Table 4.1 Comparison of power with the existing cell and reference cell

SRAM Cell → **Power Dissipation ↓**	**6T Cell**	**Reference Cell**	**Proposed Cell**
Static power dissipation (nW)	50.56	50.15	27.09
Total power dissipation (nW)	68.56	61.24	47.84

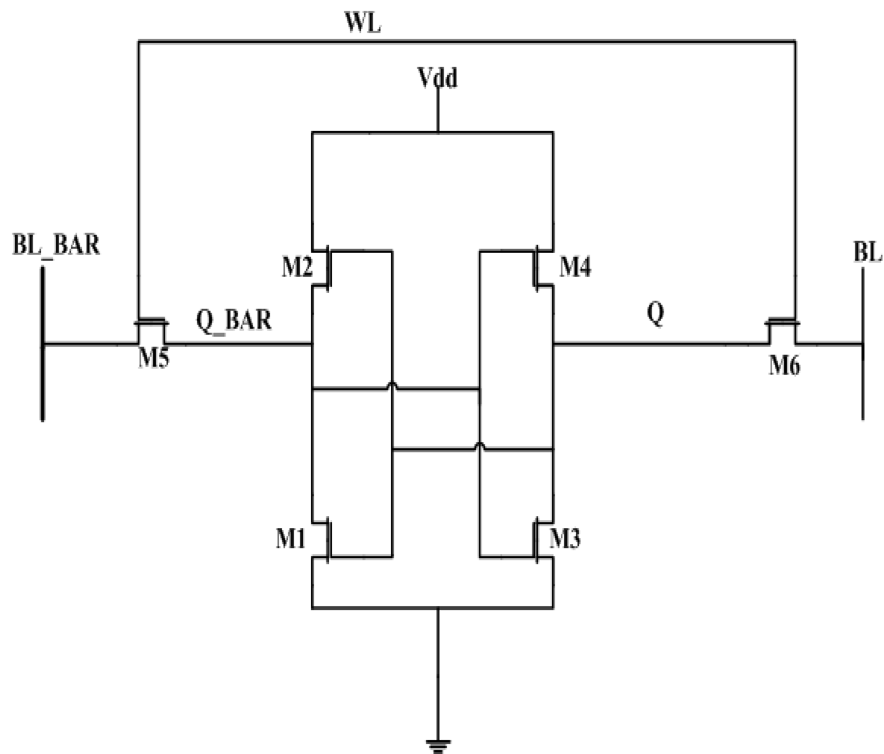


Figure 4.1 Schematic of 6T SRAM Cell

4.2 Transient Analysis

The transient response is discussed for the proposed SRAM cell. The comparison of write and read delays of proposed cell, conventional cell and reference cell is shown in Table 2. From the table, it is observed that the write delay of proposed cell has been increased by 67.5 % and 29.8 % as compare to conventional cell and reference cell, respectively. The read delay has also been increased by 10.6 % and 8.9 % when compared with conventional cell and reference cell, respectively. This increase in delay is due to the use of two extra NMOS transistors (M6, M7) in the proposed cell. But stacking effect of M6, M7 also offers advantage in reducing the leakage current [39] of proposed cell.

Table 4.2 Comparison of write and read delay for the improved cell with the existing cell

SRAM Cells ⟶ Delay ↓	6T Cell	Reference Cell	Proposed Cell
Write Delay (ps)	43.81	94.80	135.06
Read Delay (ns)	12.13	12.36	13.57

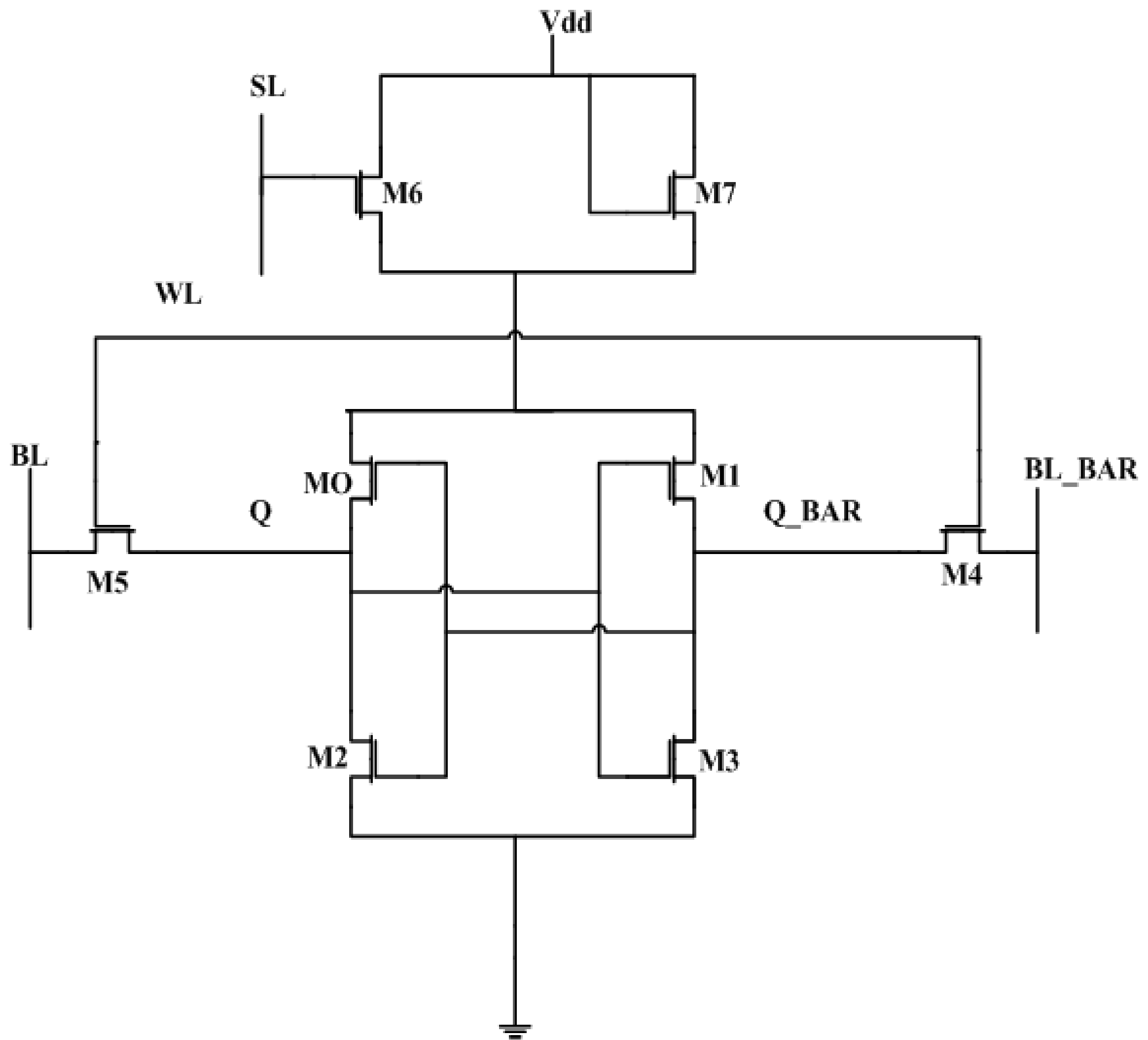


Figure 4.2 Schematic of reference Cell

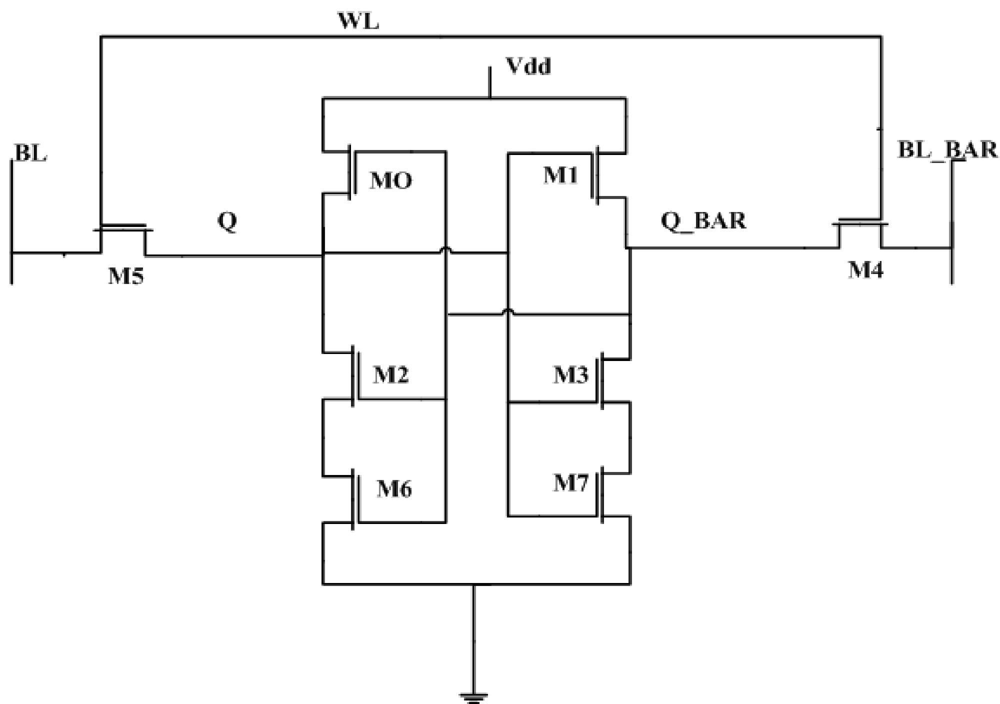


Figure 4.3 Schematic of Proposed Cell

4.3 N-Curve Analysis

The cell stability is defined by traditional SNM method, but they have the limitation that it does not provide a simple inline tester measurement and it only involves the voltage measurement, it does not give any information on the cell currents during the cell access and hold states. The greatest common method to measure SNM uses butterfly curve [40]. So the noise curve (N-curve) is one of practical inline tester technique used to determine cell stability. The N-curve parameters are SVNM, SINM, WTV, WTI [41]. The improvement in the parameters has been shown in Table 4.3. The N-curve analysis of traditional, reference and proposed cell has been shown in Figure 4.4, Figure 4.5 and Figure 4.6. The variation in the SVNM and write trip voltage (WTV) for the stability of 6T, reference cell and improved cell with temperature has been shown in Figure 4.4 and Figure 4.5 and comparison of stability parameters of 6T, reference and proposed cell with different Voltage Supply (Vdd) has been shown in Table 4.4, Table 4.7 and Table 4.8. As the temperature increases from (0 to 37) ºC there is a reduction in SVNM and WTV as shown in Figure 4.4 and Figure 4.5 and evaluation of stability parameters for 6T, reference and proposed SRAM cell with different temperature range has been shown in Table 4.5, Table 4.6 and Table 4.9. The increase in the temperature from 0 to 37 ºC affects the threshold voltage of the transistors which in turn reduces the noise tolerance of the circuit. As the voltage (Vdd) increase from 0.6 V to 1.1 V the stability also increases and hence the voltage margins (SVNM, WTV) also increase as shown in Figure 4.6 and Figure 4.7. Therefore as the supply voltage Vdd reduces, the cell tolerance was also reduced according to

the definition of SVNM. In sub threshold region of operation the noise tolerance improves with Vdd along with write ability as supply voltage increases from 0.6 to 1.1 V. In the sub threshold region of operation the noise tolerance improves with Vdd along with write ability current margins (SINM, WTI) for the stability of SRAM cells as shown in Figure 4.8 and Figure 4.9. The increase is due to the exponential dependence of sub threshold current on Vdd. The noise tolerance improves with Vdd along with write ability as the value of on current increases. From the calculation, the SVNM in the proposed cell has been raised by 1 % as compared to traditional 6T cell and 4% as related to the reference cell. The SINM in the proposed cell has been raised by 27.7 % as compared to traditional cell and 42.8% as comapred to the reference cell. The WTI of the proposed cell has been increased by 53.3% as related to traditional cell and 71.9 % as related to the reference cell, respectively. The WTV of the proposed cell has been reduced by 12.6 % and 13.4 % as related to traditional cell and the reference cell, respectively.

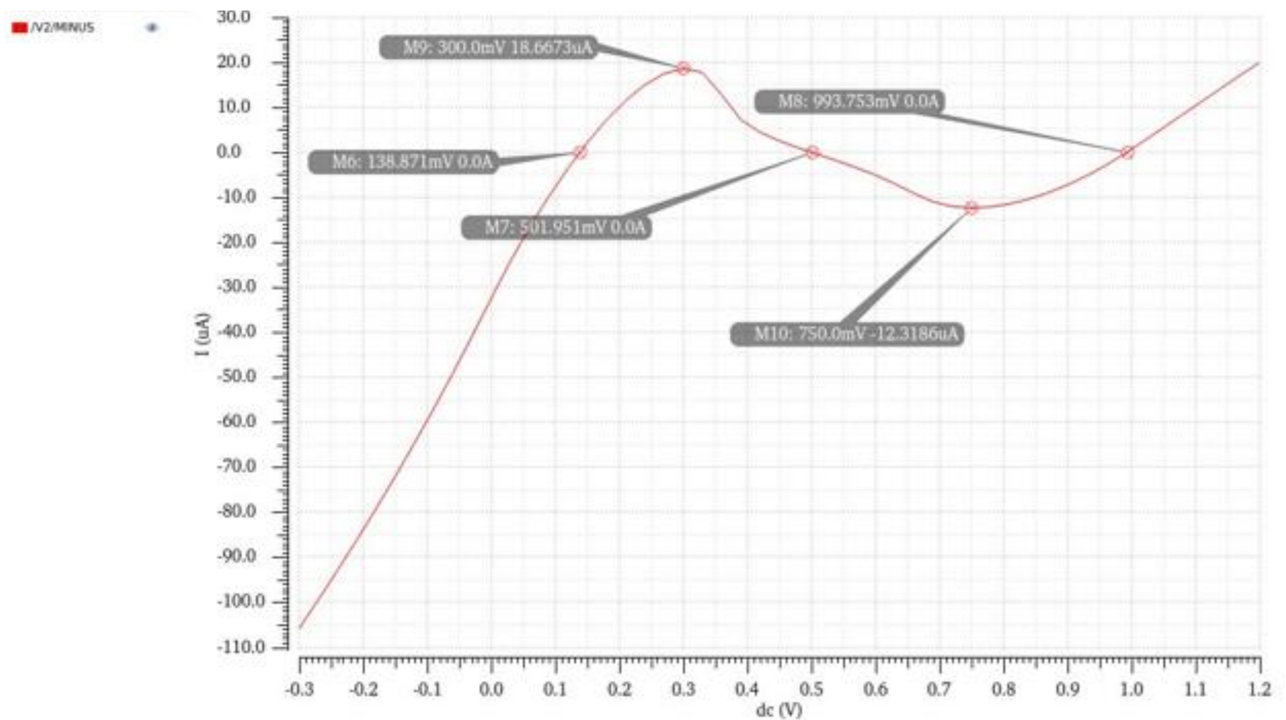


Figure 4.4 N-Curve for Conventional cell at Vdd =1 V

Table 4.3 Stability factor in the proposed cell compared to existing SRAM cell

At T=27 °C, Vdd =1 V	6T-SRAM	Reference cell	Proposed SRAM
SVNM (mV)	363.08	352.177	366.715
SINM (μA)	18.667	14.754	25.801
WTV (mV)	491.802	496.453	429.855
WTI (μA)	-12.318	-7.376	-26.283

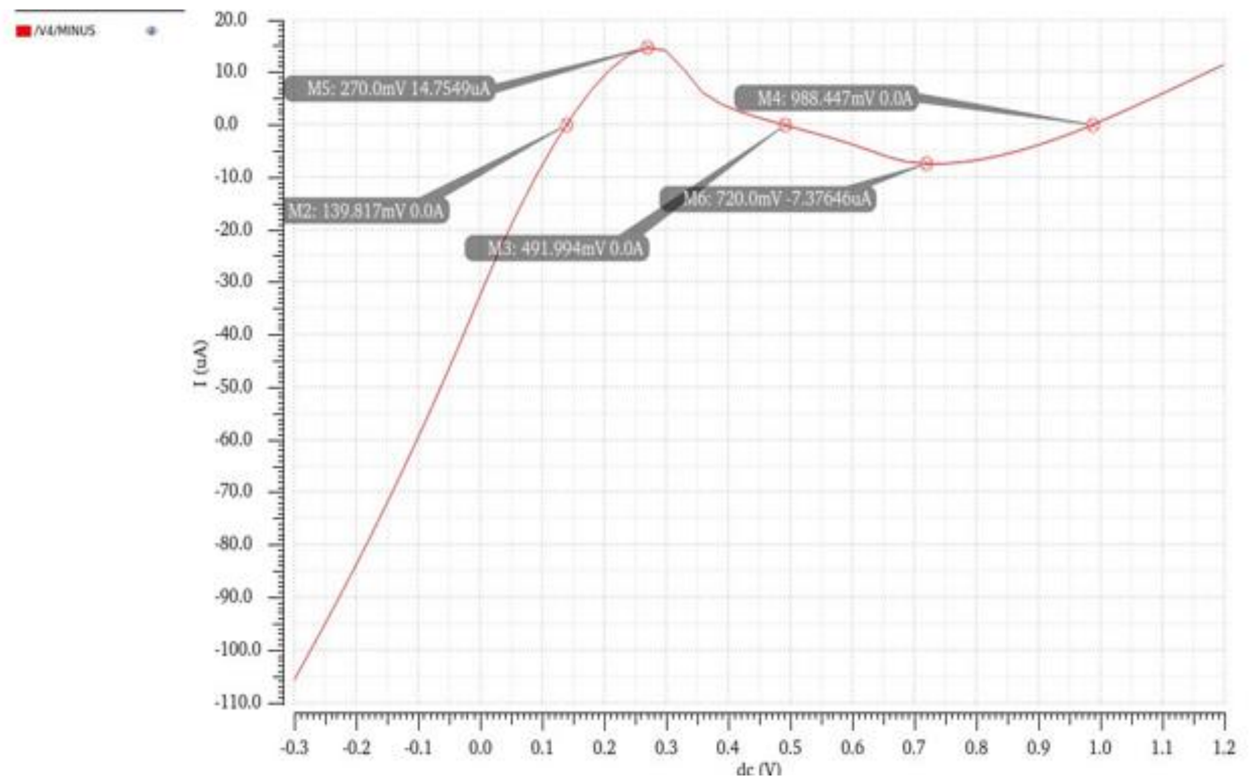


Figure 4.5 N-Curve for reference cell at Vdd = 1V

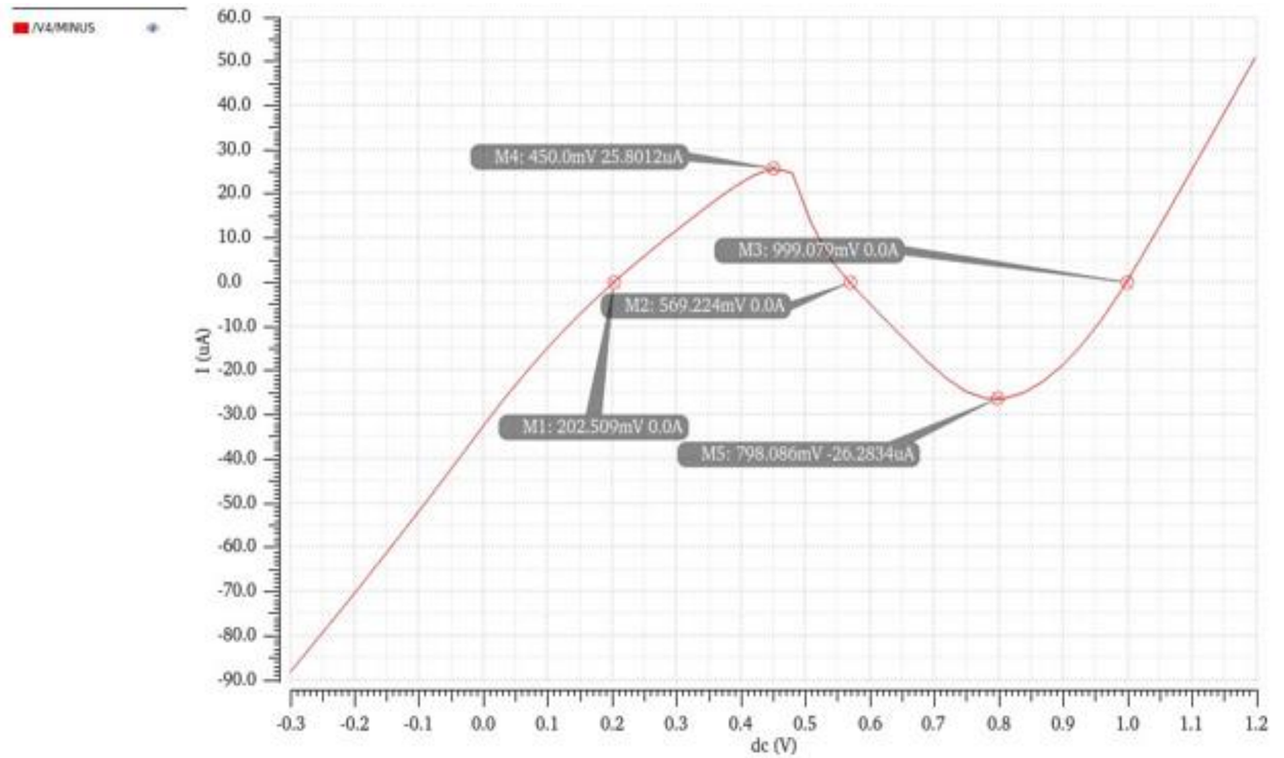


Figure 4.6 N-Curve for proposed cell at Vdd = 1V

Table 4.4 Comparison of Stability parameters of 6T SRAM Cell with different Supply Voltage (Vdd)

6T SRAM Cell Supply Voltage (V)	Vdd = 0.6	Vdd = 0.7	Vdd = 0.8	Vdd = 0.9	Vdd = 1	Vdd = 1.1
SVNM (mV)	304.089	327.051	343.745	354.323	363.08	374.206
SINM (µA)	9.862	11.919	13.436	15.738	18.667	23.567
WTV (mV)	224.086	282.44	346.637	418.55	491.802	562.931
WTI (µA)	-6.121	-8.946	-9.898	-10.314	-12.318	-15.205

Table 4.5 Comparison of Stability parameters of 6T SRAM Cell with different temperature range.

Temperature (ºC)	**T = 0**	**T = 17**	**T = 27**	**T = 37**
SVNM (mV)	375.654	367.684	363.08	358.462
SINM (µA)	22.804	20.089	18.667	17.347
WTV (mV)	495.733	493.35	491.802	490.129
WTI (µA)	-14.375	-13.072	-12.318	-11.595

Table 4.6 Comparison of Stability parameters of 6T SRAM Cell with different temperature range

Reference Cell Temperature (ºC)	**T = 0**	**T = 17**	**T = 27**	**T = 37**
SVNM (mV)	365.788	357.167	352.177	347.172
SINM (µA)	18.835	16.153	14.754	13.461
WTV (mV)	501.718	498.617	496.453	494.049
WTI (µA)	-8.990	-7.951	-7.376	-6.829

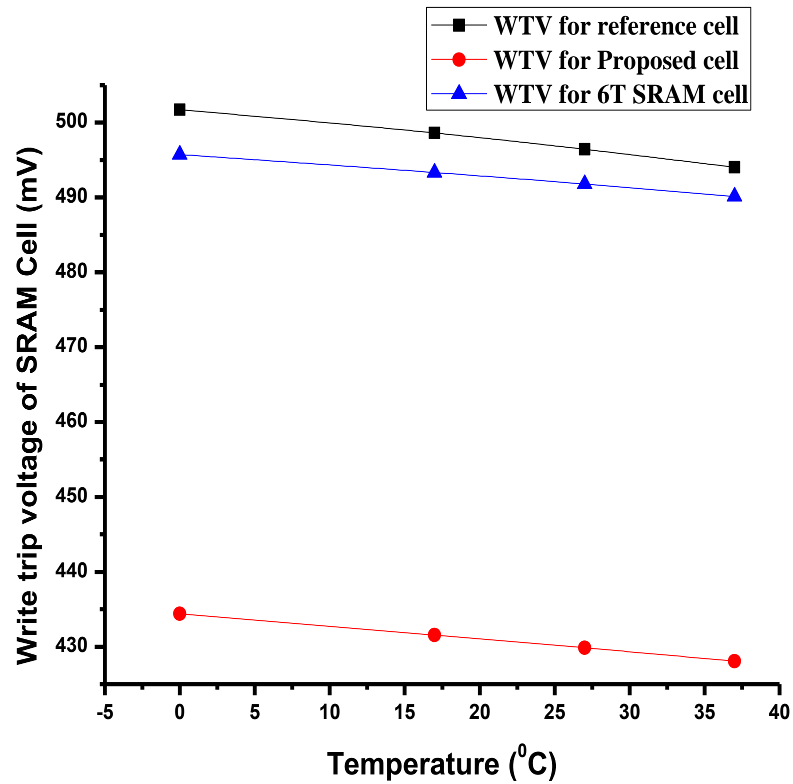


Figure 4.7 Variation in write trip voltage of SRAM cell different temperatures

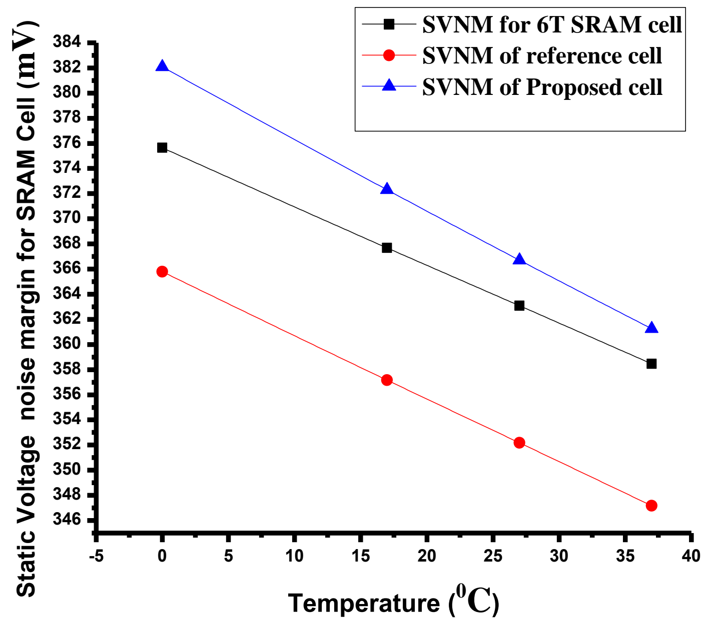


Figure 4.8 Variation in static voltage noise margin of SRAM at different temperature

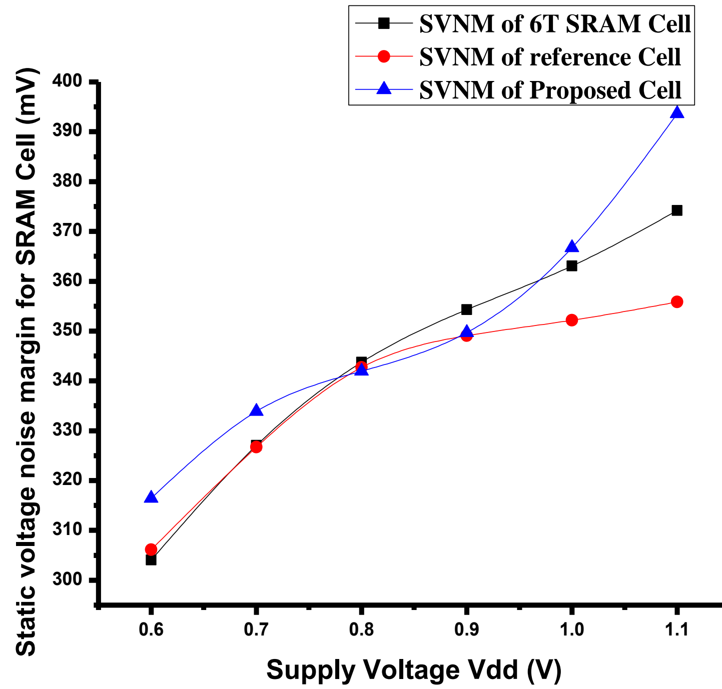


Figure 4.9 Variation in SVNM of the Proposed cell with existing SRAM cell at different voltages

Table 4.7 Comparison of Stability parameters of reference cell at different Supply Voltages (Vdd)

Reference Cell Supply Voltage(V)	Vdd = 0.6	Vdd = 0.7	Vdd = 0.8	Vdd = 0.9	Vdd = 1	Vdd = 1.1
SVNM (mV)	306.125	326.686	342.686	349.081	352.177	355.828
SINM (µA)	9.735	11.3177	11.955	12.948	14.754	17.660
WTV (mV)	223.875	282.026	346.174	419.864	496.453	571.701
WTI (µA)	-6.121	-7.792	-7.937	-6.808	-7.376	-8.946

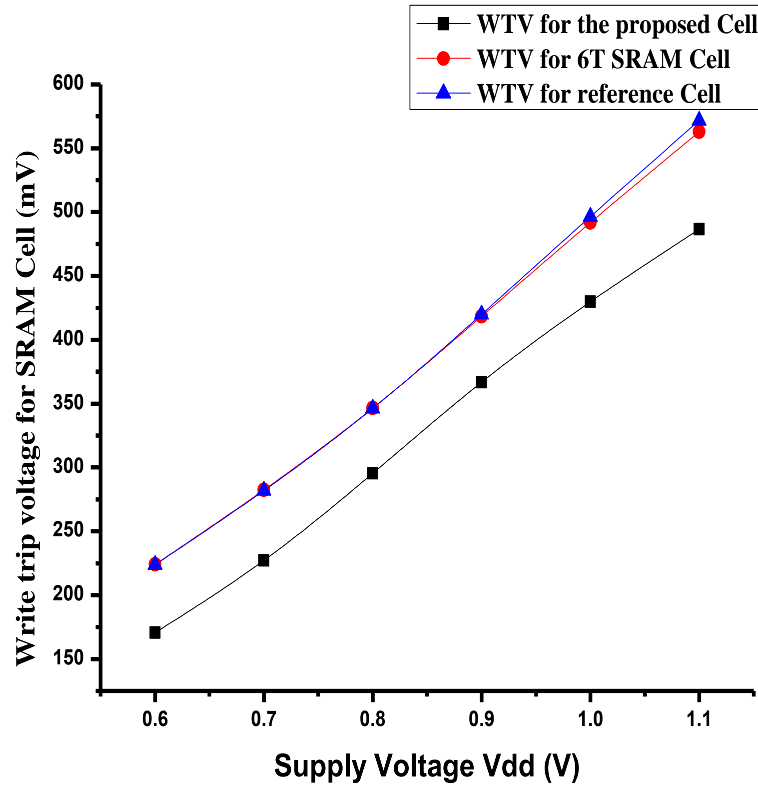


Figure 4.10 Variation in write trip voltage of SRAM cell at different voltages

Table 4.8 Comparison of Stability parameters of Proposed cell at different Supply Voltages (Vdd)

Proposed SRAM Cell Supply Voltage(V)	Vdd = 0.6	Vdd = 0.7	Vdd = 0.8	Vdd = 0.9	Vdd = 1	Vdd = 1.1
SVNM (mV)	316.45	333.853	341.988	349.725	366.715	393.643
SINM (μA)	5.736	8.168	11.416	16.699	25.801	36.809
WTV (mV)	170.601	227.279	295.495	366.682	429.855	486.542
WTI (μA)	-5.001	-8.761	-12.415	-18.253	-26.283	-37.089

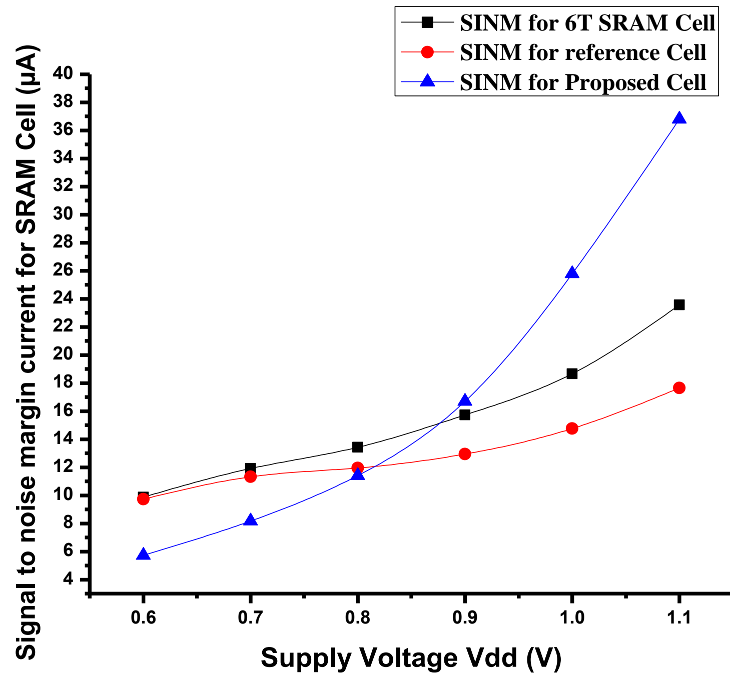


Figure 4.11 Variation in SINM of the Proposed cell with existing SRAM cell at different voltages

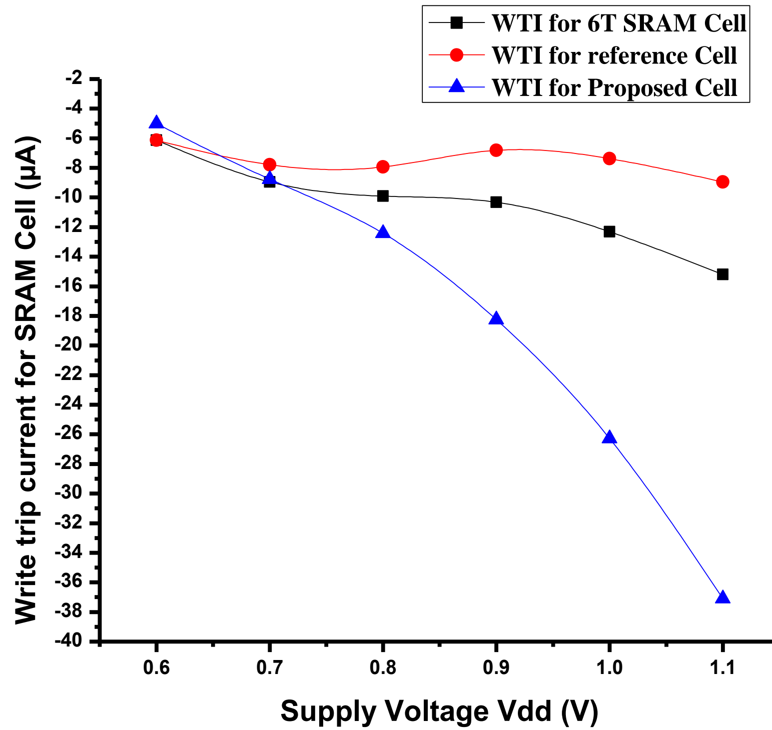


Figure 4.12 Variation in write trip current SRAM cell at different supply voltages

Table 4.9 Comparison of Stability parameters of Proposed SRAM Cell with a different temperature range

Proposed SRAM Cell Temperature (°C)	**T = 0**	**T = 17**	**T = 27**	**T = 37**
SVNM (mV)	382.089	372.308	366.715	361.251
SINM (µA)	29.661	27.144	25.801	24.537
WTV (mV)	434.38	431.532	429.855	428.068
WTI (µA)	-30.617	-27.743	-26.283	-24.987

CHAPTER 5

Conclusion and Future Scope

5.1 Conclusion

Several groups are working on developing memories with low power dissipation and high speed. SRAMs are known to dissipate high power. They are indispensable in several applications that include System on Chips (SOCs). Therefore, attention is paid towards developing low power and high stability SRAM cells and architectures. This Thesis attempts to use some technique i.e proposed cell to decrease the static and total power dissipation. The technique also used for improve the cell's stability. The performance parameters of proposed SRAM cell namely SINM, WTP, WTI, SVNM, read delay, write delay etc has been studied. The static power dissipation of proposed cell was decreased and the total power dissipation also reduced compared to other two cells existing 6T SRAM cell and the reference cell. Here read and write delay of an proposed cell has been increased due to stacking effect because of a decrease in leakage current leads to increase in delay performance. We also calculate the N-curve parameters (SINM, SVNM, WTI, WTV). There has been reduction in total power and static power dissipation by 30.2% and 46.4% as compared to the traditional cell. As related to reference cell, the static power and total power of proposed cell have been decreased by 43.9 % and 21.9 %, respectively [8]. Also, the stability parameters SVNM, SINM, WTI of proposed cell has been improved by 1 %, 27.7 %, 53.3 % as compared to traditional 6T SRAM cell and 4 %, 42.8 %, 71.9 % compared to reference cell, respectively. The WTV of the proposed cell has been decreased by 12.6 % and 13.4 % as related to traditional and reference cell, respectively. The smaller the WTV, the faster the cell is written.

5.2 Future Scope

The readability of SRAM cells remains a challenge, but the ultimate goal is to decouple the SRAM's readability and writability constraints from each other. The statistical analysis presented for the SRAM contribution was restricted to only fixed the width and lengths of the transistors and keeping all technology parameters fixed. This analysis can be further expanded to take into account changes to technology parameters as well as design parameters i.e. changing length and width of the transistor.

In this the transient analysis is based on static and total power dissipation and calculate read and write delay, we can further analyze the write and read access time of the cell. This work concentrated on 90nm technology mode and the performance obtained is with respect to this technology. However, if this concept is extended to further deep submicron technologies one can investigate the effect of the small feature size and threshold voltage sizes on performance. From the description, given in this thesis it may be noted that the effort is put in mostly to decrease the power dissipation to increase the cell stability. In the improved

cell, static and total power dissipation was decreased with the cost of increasing read and write delay. Further new topologies for SRAM cells and bit line architectures should be explored to minimize the power consumption. It may be noted that is work reported have concerns only with statistical analysis. However if this is to be realized in practice one has to draw the schematic using tools such as VIRTUOSO of CADENCE, verify the functionality, draw the layout based on specific technology libraries and carry out design rule (DRC) check, extract the circuit with parasitic components (RC extraction) and carrying out post-layout simulations. This post-layout simulation is especially important for submicron based technologies as the density of interconnects are high and their effect becomes prominent. Then the design can be prototyped by sending the design to the FAB.

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