Thesis

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"Study the performance analysis of optical based VLSI interconnects"

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DECLARATION

I Yudhvir Singh, hereby declare that the work presented in this thesis entitled "**Study the performance analysis of optical based VLSI interconnects**" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of **Dr. Mayank Kumar Rai** (Assistant Professor, ECED, Thapar University) from 2015 to 2017. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

Since decades ,performance of computer systems have witnessed a stunning growth at sustained rate .But as the technology is scaling down ,there has been a consequential reduction in dimensions. Hence, problems like increase in resistivity of Cu on-chip wires due to electron scattering start materializing. Also, due to technology scaling reduction in cross section of area of interconnect also severely demean electromigration reliability. The performance of parallel links in traditional electrical devices like Cu and CNT is also restricted by the crosstalk because of coupling . Besides this, on the demand side, the emergence of multicore architectures have placed a premium on high bandwidth density and less delay interconnect between cores. Hence ,one promising candidate to give an efficient solution to the problems associated with the global on-chip electrical interconnects is optical interconnect.

This dissertation includes the study and analysis of performance of Optical interconnects. The performance in terms of propagation delay ,power dissipation ,of optical interconnects have been analyzed at 14 nm technology node. SPICE simulations using PTM level 54 model were carried out to endorse the findings. The results acquired from the simulation are compared with the traditionally used copper interconnects and it is noticed that optical interconnects dominate the existing interconnects at distinct technology nodes ranging from 90nm to 14nm.

It is also observed that delay offered by optical interconnects follow a decreasing trend with future technology nodes whereas delay of existing copper interconnects increases. At lower frequencies ,the power dissipation in optical interconnects is more as compare to copper interconnect. But as we keep increasing frequency, the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects.

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ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ICS	Integrated Circuits
OIS	Optical Interconnects
CMOS	Complementary Metal Oxide Semiconductor
PMOS	P Channel Metal Oxide Semiconductor
NMOS	N Channel Metal Oxide Semiconductor
PD	Photo Detector
MSM	Metal Semiconductor Metal
TIA	Transimpedance Amplifier
MQW	Modulator Quantum Well
VCSEL	Vertical Cavity Surface Emitting Laser
SOI	Silicon On Insulator
CR	Contrast Ratio
IL	Insertion Loss
BR	Bit Rate
BER	Bit Error Rate
WDM	Wave Division Multiplexing
VLSI	Very Large Scale Integration
MZM	Mach–Zehnder Modulator
CNT	Carbon Nanotube
GNR	Graphene Nanoribbons
EAM	Electro-Absorption Modulator

CHAPTER 1

INTRODUCTION

1.1 Motivation

As the technology node is decreasing , the IC's are becoming more compact. The cost per operation has decreased drastically. But as the functional modules are becoming more closer than ever, the presence of crosstalk is becoming more dominant . Not only this, with scaling other problems like power dissipation, lesser bandwidth have also arisen. Many of them are due to the physical restrictions posed by copper as well as by other electrical wires.[1].This situation is called interconnect bottleneck because the performance of the chip is deteriorated by the limited capacity of existing interconnect.

As the device density increased with scaling, the current density increases in the interconnect. Due to the advantages of copper like higher conductivity , it became the preferred material interconnect in deep submicron region . As the technology scaling continued new problems were surfacing. With the reduction in cross-section area of copper interconnect, resistivity increases due to surface roughness and grain boundary scattering, causing increase in propagation delay, power dissipation and electromigration.[2].The high speeding signals are deformed because of these factors. The most imperative alternatives are optical interconnect , CNT and GNRs. Interconnects are of three types if distance is the critera : local ,intermediate and global.

1] **Local interconnects** compose of thin lines ,connecting gates and transistors inside the operational block.They usually hold the data for less then 1 clock cycle .They use only few gates and occupy either first or second metal layers.

2] **Intermediate interconnects** are broader and longer than local interconnects so that they provide relatively lesser resistance .They provide clock and signal distribution to a operational block with usual lengths that vary from 3 nm to 4 nm.

3] **global interconnects** are the ones which hold the data for more than 1 clock cycle and provide clock and signal distribution between the operational blocks .They also deliver power to each module. Global interconnects are on the top one or two layers , and they are longer than 4 mm.

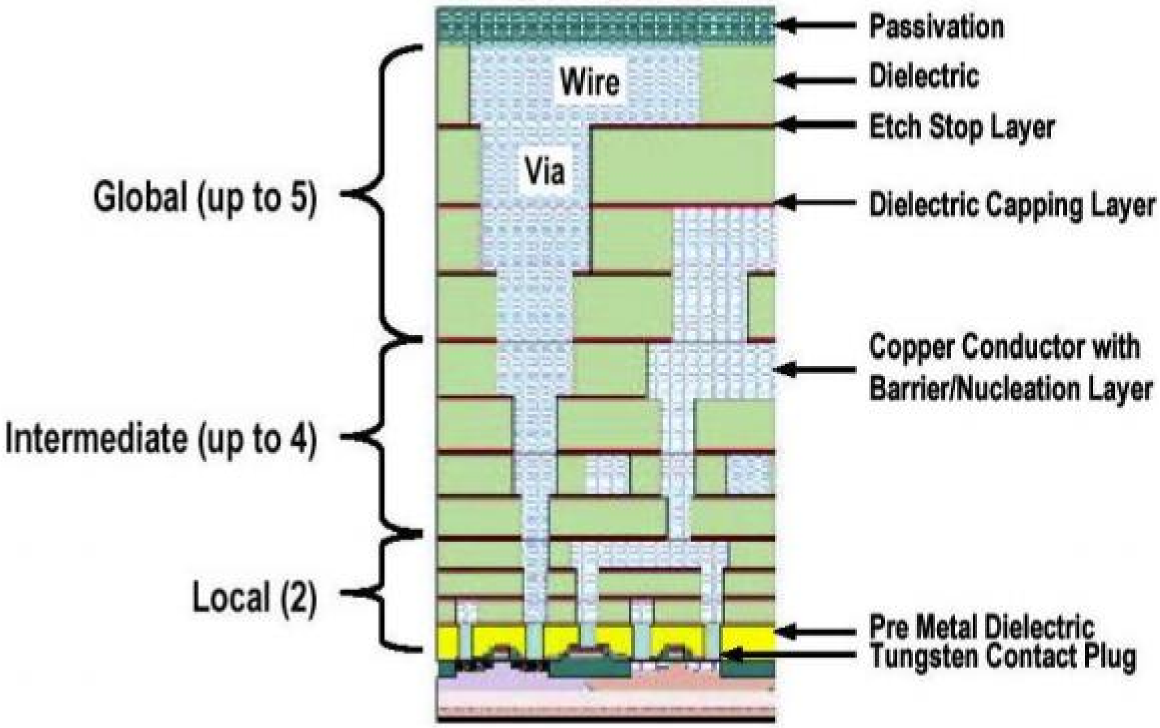

Figure 1.1: Schematic shows distribution of interconnects in modern ICs at hierarchical level [3].

1.2 Statement of problem

Following objectives have been carried out in this dissertation report :

- To study the performance of optical interconnects in the terms of delay ,dynamic power dissipation and latency.
- Compare the performance of optical interconnects with the existing interconnects that is copper interconnects.
- Comparison will be carried out in 14 nm technology node with PTM model.

1.3 Organization of report

The report is cleaved into 6 chapters which primarily focuses on comparison of the delay and power dissipation performance between optical and copper interconnects at different nodes ranging from 90nm to 14 nm. It extensively covers all possible aspects of both optical as well as copper interconnects. Simulation results have been discussed to compare both interconnects at different nodes as well as at different frequencies using different parameters.

Chapter 2 gives literature survey affiliated to the topics covered .The first and foremost step in order to pursue this dissertation is to study pertinent work which has been published formerly by various researchers working on the same topic. Research papers related to work that have been done are studied and then using that research gaps are identified. Various papers were presented which has shown the incapability of the existing copper interconnects to cope with the requirement of modern high performance ICs and also pointed out the reasons behind them. This chapter also presented the requirements for the optical interconnects and the targets that it has to achieve to overcome the problems caused by traditional interconnects.

Chapter 3 gives the description about the existing copper interconnects. It gives us information about the various facets of copper interconnects . This chapter has described what the demerit of this interconnect are and why they will not be able to cope with the requirements of future high performance electronic systems in term of various parameters. This chapter includes the basic CMOS circuit as well as the global model of copper interconnects. Equations that are used to calculate the value R,L,C parameters are given.

Chapter 4 gives us the description about optical interconnects. It is exhibited what are the advantages of using optical interconnects and why only they have the potential to cope with different challenges inflicted by the traditional copper interconnects. Optical interconnects are narrated as the potential substitute to the copper interconnects at global interconnect level. Basic optical data path at 1mm and 1 cm length is displayed

Chapter 5 gives results and discussion. Every Electrical interconnects have a equivalent RLC circuit .Physical geometries of interconnects at given technology nodes are responsible for value of parameters. The value of R,L,C parameters of electrical interconnects are evaluated. These values are calculated for various technology nodes and side by side numbers of repeaters in electrical interconnects are varied. SPICE simulations are done at frequencies 25Mhz ,50Mhz,75Mhz,100Mhz,respectively for optical as well as copper interconnect. Similarly, to analyze the power consumption aspect of optical as well as copper interconnects at same frequencies, simulations are done .

Chapter 6 gives the conclusion and the future scope of the optical interconnects. The performance of next generation CMOS based reconciled optoelectronics devices is projected.

Based on this anticipation of future technology nodes, a differentiation between electrical and optical interconnects is observed for various standard designs. The performance of optical as well as copper interconnects is collated in terms of power dissipation and delay. These comparisons are done on nodes ranging from 14nm to 90nm.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction

Researchers have found immense potential in optical interconnects. High bit rates can be achieved because data travels in form of light. For longer lengths > 10 mm,optical interconnects are more advantageous over Cu and CNT. For shorter lengths < 10mm ,optics are not preferred over GNR and CNT when it comes to smaller technology nodes. Major factors influencing the performance of optical interconnect are the delay & power dissipation of end devices that is receiver and transmitter. The main concern in optical interconnect is regarding the performance of end devices because the delay and power dissipation of optical fibre is material based phenomena and the delay is constant for constant length for a material used.

2.2 Performance analysis of electrical and optical interconnect

Guoqing Chen et al**.**[4] As the CMOS technology is being scaled , requirements of design of on-chip interconnects have become more precise because of constraints on such as delay, power, bandwidth and noise immunity. Due to various process and environmental variations new challenges are transpiring. It is extremely problematic for electrical interconnects to satisfy these requirements. Performance of CMOS based reconciled optical devices are predicted and analyzed according to the cutting edge optical technologies. Critical dimensions surpassing which optical interconnect give a potential substitute over electrical interconnect are observed to be one–tenth of chip edge length at 22nm node.

K. H. Koo et al**.**[5] To replace existing Cu-based interconnects , predictions and estimates reveals that optical and CNT's can be a potential substitute for both local(CNT) as well as global wires (optical and CNT) .For local wire, a CNT bundle manifest less latency than Cu for a given orientation ,by grasping the superior electro-migration properties of CNT, we can further improve latency .For global and semi global wires ,CNT and optical wires were compared in terms of latency ,energy efficiency ,and bandwidth density .For the future technology node ,comparisons were also carried between bandwidth density ,power density and latency .Optical wires have lowest latency and highest bandwidth using WDM (wavelength division multiplexing) among all kind of interconnects whereas Cu have more latency than CNT bundle .Considering power density comparison of interconnects which is highly switching dependent (SA) ,optics in that case favours high SA whereas for low SA optics is just power efficient compared to CNT.

Anan.A.Hamoui et al**.**[6] they proposed a model to compute the current for the supply,delay and power consumption of a submicron CMOS inverter .A nth power law MOSFET model was proposed which relates the three – terminal voltages given to drain current in submicron transistors .They followed a multistep approach to carry out analysis .First step include computing positioned references on output waveform of voltage and thus,is followed by doing linear approximations through these dots to locate the actual point of interest and desired speed. In order to evaluate and analyze voltage and current a three step process was executed done . The charging or discharging current attain its maximum value ,when the short circuit transistor changes its mode of operation .The time and output voltage are evaluated and then these are used to calculate propagation delay and characterize output waveform.

Cho et al.[7] proposed that high computational capability is very difficult to achieve in future using broad –level copper interconnects .This is because of enormous increase in high speed ,skin effect and dielectric loss ,noise ,impedance mismatch. Solutions to these problems are possible but they require complex signal processing and large are and power consumption. optical interconnect thus offer a potential substitute .This paper proposed a power comparison with respect to parameter that are bandwidth, length of interconnect and BER. They also identified a crucial device and system parameter which have a huge effect on power consumption. For optical , these were detector and modulator capacitance ,responsivity, coupling efficiency whereas in electrical interconnect parameter include receiver sensitivity and impedance mismatch. They also proposed a optimization scheme to minimize optical interconnect power and relate its performance as a function of various future technology nodes.

Arun.palanippan et al**.**[8] proposed that input and output bandwidth requirement can be addressed by inter-chip optical interconnect architecture. Several such architectures were compared to relate efficiency of power in 90 nm and 45 nm CMOS technologies. One of them is a unique architecture composed of discrete vertical cavity surface emitting lasers (VCSELs) with p-i-n photodetectors (PDs).Other architecture include wave guides formed from a metal-semiconductor-metal PDs and either EAM (electro-absorption modulator),(RAM) ring resonator modulator or (MZM) mach zehnder modulator source. An optimized current density methodology has been performed to obtain optimized circuit of driver and receiver to reduce total link power consumption .The outcome of the analysis was that performance of VCSEL based link is restricted by its bandwidth and maximum power levels rather than circuit bandwidth and thus, it attains a data rate of 24 gb/s in nodes of 45 nm and 90 nm .The other two technologies have the capacity to achieve scaled data rates more than 30 Gb/s at efficient power levels near 0.5 mW/Gb/s but are limited due to device insertion and coupling losses.MZM offers wide optical bandwidth and it can operate robustly if significant corrective measures to improve power efficiency are taken.

Pawan kapur et al.[9] proposed that the clock distribution by traditional interconnect may suffer from more power dissipation and uncertain timing with respect to optical based VLSI interconnect. They compared the power dissipation in optical based clock distribution with the electrical counterpart .Most of the power dissipation in the optical interconnect occurs in the receiver end .Important parameters were identified which were effecting its power performance was found that despite higher bandwidth requirements (higher clock frequency),the power has reduced provided a high optical power is available .They also found out that metal based interconnects used more power as compare to optical based interconnect.

Christoforos Kachris and Ioannis Tomkos [10] demonstrated that the exponential increase in the Internet traffic is because of cloud computing , rising web applications that generated the desire to have more efficient data centres. These warehouse scale data centres contains compiled racks of interconnected routing switches and thus consume significant energy. A number of optical interconnects were proposed for next generation networks used in these data centre . The paper also discusses the need to shift the systems at the data centre in the optical domain so as to get a reduced power output and meet the requiring bandwidth conditions. This paper also incorporate information about a few optical interconnects that could be beneficial for high performance data centres. The work also presents a quantitative as well as qualitative categorization of these strategies based upon their core features such as performance of the data centre, capability of getting connected and scalable level.

2.3 Optimizing Bandwidth Consideration of Optical Interconnect

Lian wee Luo et al.[11] proposed the first microring –based demonstration of WDM compatible MDM(Mode Division Multiplexing) with low loss and crosstalk .They used approach which has increased the bandwidth by many times for on-chip ultra bandwidth communications.

B.G .Lee et al**.**[12] discussed the challenges which can be faced in scaling of bandwidth within computing systems .They have considered unsustainable increase in the no of fibers per system and figured out various approaches to maximize bandwidth per fiber in future .They proposed that in future optical interconnects ,the primary goal is to increase bandwidth per fiber while only marginally increasing link cost and power .This paper reviews technologies that may add bandwidth per link in future HPC (high performance computers) system .This paper discuss and analyze the probable technologies for HPC like Flip-Chip Packaged Parallel Optical Transceivers, Multicore Graded-Index Fiber Transceivers, Optical Links Employing Planar Polymer Waveguides, and Dense WDM Exploiting Silicon Photonic Transceivers.

Yuanyuan yang et al.[13] proposed that WDM technologies has the ability to meet the demands of increasing bandwidth from bandwidth intensive computing applications .Optics is an imperative part of today's networking systems ,thus optical interconnects will play a pivotal role in the processors in parallel and distributed computing systems .This paper emphasize on the cost effective designs of WDM technique in optical interconnects for present and next generation parallel and distributed computing systems .Two different models of WDM were considered based on the specific applications .The first is wavelength based model and the other is fiber-link model .The existing WDM optical interconnect uses the wavelength based model .They also presented an optimized cost design for WDM optical interconnect under wavelength based model which used sparse cross bar switches. In the fiber-link model, the network cost can be reduced significantly .They generalized the idea that was used to design fiber-link based model to WDM optical interconnects under wavelength based model and another design was obtained that can trade off switch cost with wavelength converter cost in this WDM optical interconnect.

Po-Kuan Shen et al.[14**]** demonstrated experimentally a chip based design of optical interconnect module composed of VCSEL based chip, a photo-detector (PD) chip, a driver circuit ,and an amplifier on a silicon-on-insulator (SOI) substrate with paths for three dimensional guided-wave. Such an optical interconnect is designed for connections in processors having multiple cores or for interfaces that are used in between the memory and processor. Three dimensional guided-wave path , which consists of micro-reflectors having mirror made of silicon tilted at 45° and trapezoidal shaped waveguides, which is used to provide medium for optical information to travel between end devices. In this paper, to attain the chip level optical based interconnects ,the VCSEL and PIN PD chips are integrated on SOI substrate. Because of the distinctive design of 3-D guided-wave path , optical coupling efficiency of 2.19 dB is achieved .Not only this, but a highly aligned VCSEL/PD assembly is attained. Optical efficiency required for transmission can attain a value of upto 2.19 dB. optical power and threshold current of VCSEL can achieve a maximum value of 3.27 mW and 1 mA, respectively. For the verification of the data transmission, the commercial driver IC and amplifier IC are integrated on the silicon chip, and when data transmission of 10 Gbps can be achieved without any error.

2.4 Optimization of End devices of Optical Interconnect Circuit

N.C LI et al.[15] proposed to use super-buffer which is a sequentially connected tapered inverters and size of each inverter is more as compared to preceding inverter by the value of e(2.3).This value is selected so as to minimize propagation delay of super buffer .The parameters of given CMOS technology node are used to determine propagation delay. The transmitter end is noting but a series of inverters which can be tapered or optimally sized .The first inverter is of minimal size and the last one is used to drive the modulator .In jaeger's model ,each stage of buffer is composed of one conductor and one capacitor but in this, one conductor and two capacitors are used**.**

H.B. Bakoglu et al.[16] proposed that propagation delay of interconnect plays a pivotal role in analyzing the performance of VLSI circuits .This is because as the chip – size is increased and cross sectional interconnection dimensions are scaled ,the RC delay constant increases .This paper also proposed a model for interconnect time delay that include the effect of changing interconnect and dimensions of chip .Delays of Al,WSi2 and polysilicon lines are compared and delays in next generation VLSI circuits are proposed. Cascaded drivers which are properly scaled are investigated as probable methods for reducing propagation delay. The model discussed in paper gives most optimized cross-sectional interconnection dimensions and driver configuration which can lower power dissipation.

Ashok.V. Krishnamoorthy et al.[17] proposed that optics can be a potential substitute for electrical interconnect when the bandwidth –distance product increases more than ~100 Gb/s-m. If link power becomes lower than 1 Pj/bit/m ,then optical links are usable only for distances of 1m or below. Chip can be directly connected to Optical links so as to improve energy/bit unit .Experiments are performed on switched CMOS based VCSEL system which operates at high speed Ethernet line can gain a interconnect energy for switching activites which can be less than 19 pJ/bit for a non blocking network having 16 different ports . A cumulative capacity of 20 Gb/s per port can be achieved when operating at a line rate of 1.25 Gb/s .The CMOS –VCSEL switch can be attain optical bandwidth density of 37 Gb/s mm2 and is capable of getting scaled to higher bandwidths with 5-10 pJ which has lower link energies upto 300 fJ/bit is reviewed .This system has potential to provide optical interconnect having high switching factor at very low energy requirement.

Mahesh Kumar and K. S Sandha [18] proposed the extensive study and comparison between copper and optical interconnects in terms of delay and power consumption at global level. The traditional copper interconnects couldn’t cope with the differentiated design constraints, as the device dimensions keep on scaling down . Thus, optical links can be presented as a potential newcomer to copper interconnects. In this paper, the simulation outcome for delay and power consumption of copper and optical interconnects are displayed. The results show that optical interconnects dominates in case of delay as well as power in comparison to traditional copper interconnect if we consider the case for global interconnect length.

C.Thangaraj et al. [19] proposed that CMOS technologies having nanoscale dimensions have forced us to have a superior interconnect technology. But considering global interconnects the technology seems to have a design tailback .So the only left way is to consider optics as an alternative. If we consider prospect in future to improve upon parameters such as interconnect delay, jitter, clock skew and signal integrity ,Optics is a potential substitute to conventional electrical interconnects and has immense applications .They proposed that to successfully adjust on chip-optical interconnect ,optical components can be embedded using standard CMOS . A optical clock distribution system made of CMOS based components is described in this paper .The proposed clock recovery equipments and optical distribution system were implemented using silicon for testing purposes in 0.35 micro meter CMOS process .the experiment results illustrated the feasiabiltiy of proposed approach and the overall system functionality ,though many aspects of circuit can be improved further .No great challenges were faced in implementing the design that required more than 10 Ghz clock rates .

Mikhail haurylau et al.[20] proposed that intra-chip optical interconnects dominate electrical wires and provide an effective solution to communication tailback in high performance integrated circuits .the silicon integrated circuits must satisfy some demand so as to surpass copper electrical interconnect by using international Technology Roadmap for Semiconductors (ITRS) as a reference. the needs for optical interconnects components are identified by study of parameters such as Bandwidth density ,delay and power dissipation.

David A.B.Miller [21] proposed the comparison that was speculative but futuristic. The electrical and optical interconnects are compared depending on the predictive values and then they advocated the components usage for the optical devices, keeping in view that optics is an potential solution to the problematic challenges posed upon by various past interconnect technologies . Optics have inbuilt advantages with consideration to parameters like density, energy and timing .A very low value of photodetector capacitance is imperative .Very condensed wavelength spillters are needed to connect information to fibers .Dense wavelength are needed especially when clock rates are high or dense and one desires to avoid the usage of WDM .Optical links can cope with desired bandwidth requirements even without using fast clock or WDM.

Sung Min Park [22] suggested that large input capacitance of amplifiers is isolated effectively by amplifiers itself ,thus considerable bandwidth improvement is done by using regulated cascade configuration (RGC) for input stage .a bandwidth of 950 Mhz is shown by 1.25 Gb/s RGC TIA ,for 0.5 pF photodiode capacitance .there exist a difference of 93 MHz in Bandwidth for photodiode capacitance of 1 pF.2.5 Gb/s RGC TIA fabricated in a 0.6 um CMOS technology achieved bandwidth of 2.2 Ghz for 0.5 pF photodiode capacitance ,thus confirming RGC mechanism.

Drew Guckenberger et al. [23] presented DC-coupled TIA for optical receiver front ends with low power need. a rate of 12.5 Gb/s is attained by TIA’s which are using 0.25um CMOS technology node and 47Ghz SiGe BiCMOS technology while drawing nearly 1mA from 1.5 V and 1.8V power supplies DC-coupling of interface circuits to photodetector devices can reduce the data coding needs for system. A voltage stages uses negative feedback in TIA .thus there is a trade off between input impedance and gain ,which further relates to the bandwidth.

Guoqing Chen and Eby G.Friedman [24] demonstrated that interconnects plays a pivotal role at deep submicron level .Various potentially sound designs are investigated in the interconnect design with excellent performances in terms of parameters like delay ,bandwidth and power .The repeater insertion procedure is used to insure optimal power in RC interconnect and at same time justifying delay and bandwidth constraints .The design space restricts minimum power occurance .Solutions for minimum power requirement are given by use of delay constraints ,with average error of 7% as compare to SPICE simulations .Minimum sized drivers can be used to attain the optimal power dissipation values with the prevailing bandwidth constraints .under a bandwidth constraint the minimum interconnect power decreases as compared to RC interconnect by including inductance .

C.L Schow et al**.**[25] demonstrated a TIA fabrication using 0.13 mm CMOS process which operates at rates of 25 Gb/s .It appears to have a power consumption of 0.35 mW/Gbit.The Gain provided by TIA at a bandwidth of 15 Ghz is 42 dB .this TIA display a bit error –ratio of less than 10-12 for peak to peak input currents of 225 and 425 mA at 20 and 25 Gbits/s respectively .The TIA is dc –coupled modified version of common gate configuration design .the sensitivity of transimpedance amplifier was measured by analyzsing bit error ratio as function of input optical power .

Giovanni Anelli et al. [26] investigated the TIA design in quarter micron CMOS process Tthe amplifier can be included in any submicron CMOS process as it is composed of only NMOS and PMOS .Use of transistor replacing resistor to provide the feedback path is the main attribute of this design .To read signals from silicon strips detectors which are having few pF of input capacitance ,circuit optimizing is done. An output pulse fall time of 3ns and an Equivalent Noise Charge (ENC) of around 350 electrons rms value is evaluated for an input capacitance of 4pF,an input charge of 4fC and a Trans-resistance of 135Kohms.If the measurements are to be done at 130Kohms ,improvement is seem in the performance of chip operation .An integrated circuit having 32 channels has been designed .

2.5 Conclusion

After thorough investigation of the research papers , it can be concluded that though a lot of work has been done on optical interconnects at 180 nm ,90nm and 65nm technology nodes but a lot more work needs to be done at smaller technology nodes like 22nm ,14nm and below. The most imperative components of optical interconnect are the receiver and transmitter .Most of delay is due to these end devices, and the major source of power consumption is the receiver end. As the technology involves optics so the intermediate waveguide connecting these end devices has no equivalent RLC circuit.

CHAPTER 3

COPPER INTERCONNECTS

3.1 Introduction

A VLSI interconnect is a conducting thin film that is used to provide electrical connection between two or more nodes of the system built on the silicon chip. Earlier when electronics was emerging, aluminium was primarily used as interconnect because of the good conductivity and its adherence on silicon dioxide. Due to technology scaling , interconnect current density increased manifold. This increase in current densities produces a phenomena called electromigration. Then came the era of copper which still exist . copper was a better alternative to aluminium as it is more resistant to electromigration . Relatively , copper can handle current density about 5 times more than the capacity of aluminium. Thus ,it became preferred interconnect material, especially for submicron and deep submicron high density and high performance silicon chips. [2].Low resistivity of copper decreases the speed of interconnect and also there is substantial decrease in resistive losses as compare to aluminium. The operational frequency of the system determines the speed with which the IC's may operate . This will be decided by the delay in signal propagation delay[44].By decreasing the Resistivity of the interconnect material ,RC time constant can be reduced. Copper has a resistivity of ρ of 1.7 $\mu\Omega\ /cm$, which is very less as compared to aluminium . By integrating it with the dielectric constant material of low permittivity ,a reduction in RC delay can be witnessed . However , ,the load capacitance C_l is increases, when the aspect ratio is increased by increasing the thickness[45]. The copper interconnect has other advantageous also like it has twice the thermal conductivity of aluminium .More resistant towards electromigration [2].The usage of copper can reduce the burden of power dissipation by 30% at a specific frequency. The routing of interconnect can be simplified as there is reduction of number of interconnect hierarchical levels and thus less number of steps are involved. It optimizes both cost as well as performance[13].

The constraints posed by electrical interconnects have forced us to extensively search for potential alternative solutions such as OIs .The limitations posed by copper interconnects are considered to be time dependent ,rate dependent and energy based. Thus the comparison of copper interconnects will be done with optical interconnects at standard posed by the problematic challenges when practical implementation is the concern.

3.2 Global interconnect modelling

In electrical interconnects like copper based, CMOS inverters are used as buffer or repeaters. In this CMOS inverters are made up of PMOS and NMOS where PMOS is thrice as NMOS.

The view of cross sectional area of global interconnect cross section model is in Figure 3.1.Considering a metal layer at given technology node , variables that are needed in optimization of global interconnect are the thickness of interconnect T, the height of the metal layer above the substrate H, and width W and spacing between the signal and ground line S [42]. Various performance specifications such as power dissipation and area are not considered. The width of interconnect and spacing can be given optimal values under two scenarios: 1) value of spacing is minimal and 2) spacing has the same value as that of line width,

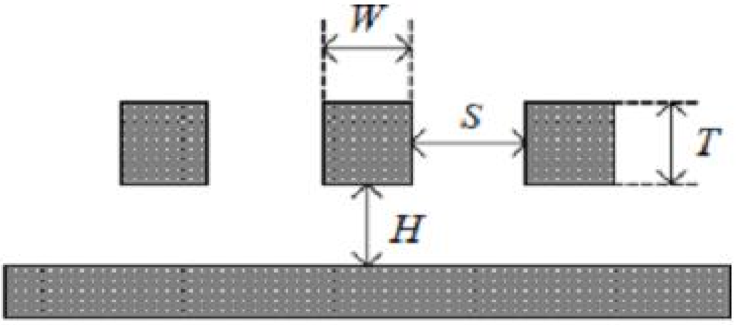

Figure 3.1 View of Cross sectional area of global interconnects [42]

Where W =width of interconnect , S = distance between the two parallel running interconnects, T = thickness of interconnect and H = height of dielectric.

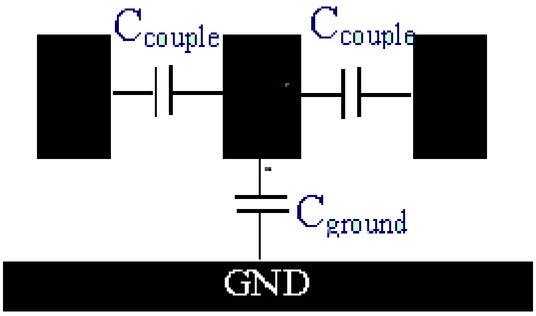

Figure 3.2 Illustration of the inter-metal and the inter-level components of capacitance.

Description of components used.

Formulas used for to calculate the values R,L,C used in equivalent circuit of copper interconnect are :

Resistance (R):

$$R = \frac{\rho \cdot l}{w \cdot t} \tag{3.1}$$

For Cu:

Value of ρ = 2.2μohm

Inductance (L):

$$L = \frac{\mu_0 \cdot l}{2\pi}\left\{ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right\} \tag{3.2}$$

$\mu_0 = 4\pi \times 10^{-7}$

Capacitance (C):

Total capacitance of the wire$(C_{\text{total}}) = C_g + 2C_c$ **(3.3)**

C_g = capacitance due to fringe flux.

$$C_g = \varepsilon\left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77}\cdot\left(\frac{t}{t+4.53h}\right)^{0.07}\right] \tag{3.4}$$

C_c**:**coupling capacitance

$$C_c = \varepsilon\left[1.41\frac{t}{s}e^{\frac{-4s}{s+8.01h}} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28}\cdot\left(\frac{h}{h+8.96s}\right)^{0.7}\right] \tag{3.5}$$

where

l= interconnect length

ρ =value of Resistivity

t = Thickness

w = Width

h= distance between metal layer and the substrate

s = distance between the signal and ground line

3.3 Insertion of Repeaters

To drive long or Global interconnects [41], or in other words if one has to drive large resistive-capacitive (RC) load present at the terminals of the gate(s) connected to it , one buffer is not an optimum solution. After all it is desired to minimize propagation delay as well as power consumption in the VLSI based interconnect system. The first and foremost purpose of inserting repeaters in the interconnect is to minimize the interconnect latency by minimizing the value of resistance and capacitance . Repeaters are necessary to operate on high RC loads. To achieve delay minimization , efficient driver circuits are desired in order to charge /discharge capacitances that are present due to large impedance present in VLSI circuits due to large drivers present at output. The repeaters can be differentiated on the basis of sizes of the CMOS inverters which act as drivers: 1] uniformly sized driver circuit. 2]optimumly sized driver circuit. 3] tapered driver .

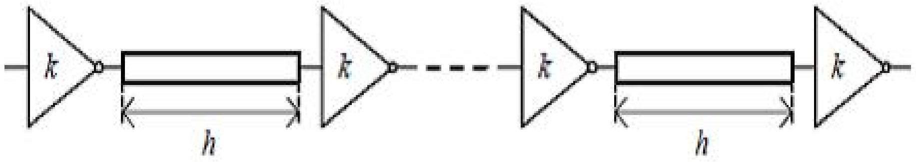

Figure 3.3 repeaters insertions in a long global interconnect [41]

As the scaling has gone up and VLSI circuits have witnessed immense increase in chip complexity .Therefore ,the running length of VLSI interconnections ,especially the power and the clock lines has increased. the main reason behind this phenomena is that parasitic capacitance and resistance of interconnects increase linearly with length. This produces high propagation delays[41].Thus ,this increases the total delay of the VLSI based electrical interconnect. An electrical interconnect with no. of repeaters can also be represented as shown in figure 3.3

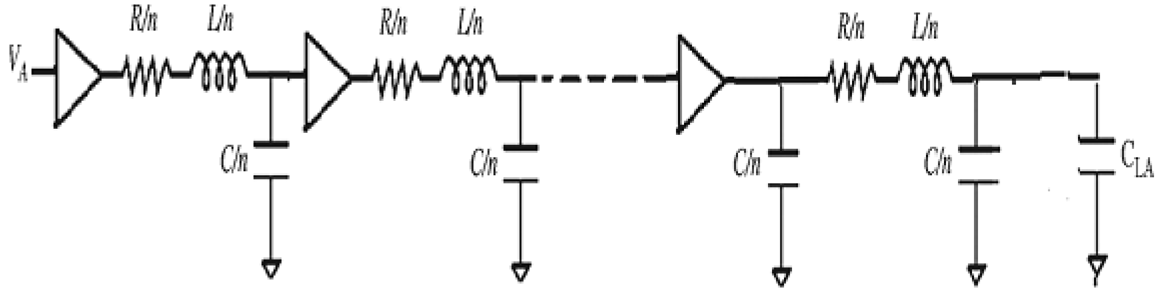

Figure 3.4 Equivalent circuit of copper interconnects[10].

3.4 Delay and Power Dissipation Analysis

The minimal delay of interconnect per unit length is given by [26]

$$\left(\frac{\tau}{h}\right)_{opt} = 2\sqrt{r_s c_0 \frac{\rho}{T}}\left(1+\sqrt{\frac{1}{2}\left(1+\frac{c_p}{c_0}\right)}\right)\sqrt{\frac{c}{w}} \propto \sqrt{\frac{c(w,s)}{w}} \qquad (3.6)$$

Value of input capacitance is= c_0, value of output parasitic capacitance is= c_p and the value of output resistance is $= r_s$.Therefore for global interconnects with repeater insertion, if length of line is= h and repeater is= k ,the time constant of the segment is as in [42].

Total delay of electrical link is given by :

$$\frac{\tau}{h}=\frac{r_s}{h}\left(c_0+c_p\right)+\frac{r_s}{k}c+rkc_0+\frac{1}{2}rch \tag{3.7}$$

The optimal size of driver and length of link segment are given by the following equation

$$k_{opt}=\sqrt{\frac{r_s c}{r_s c_0}} \tag{3.8}$$

$$h_{opt}=\sqrt{\frac{2r_s\left(c_0+c_p\right)}{rc}} \tag{3.9}$$

Thus the delay of link per unit length after optimizing the driver is given by

$$\left(\frac{\tau}{h}\right)_{opt}=2\sqrt{r_s c_0\frac{\rho}{T}}\left(1+\sqrt{\frac{1}{2}\left(1+\frac{c_p}{c_0}\right)}\right)\sqrt{\frac{c}{w}}\propto\sqrt{\frac{c(w,s)}{w}} \tag{3.10}$$

The power consumption in global link per unit length is as given by:

$$\frac{P_{total}}{h_{opt}}=k_1\left[\frac{k_{opt}}{h_{opt}}\left(c_0+c_p\right)+c\right]+k_2\frac{k_{opt}}{h_{opt}}+k_3\frac{k_{opt}}{h_{opt}} \tag{3.11}$$

Where

$$k_1=\alpha {V_{dd}}^2 f_{clock}$$

$$k_2=\frac{3}{2}V_{dd}I_{offn}W_{n_{min}}$$

$$k_3=\alpha V_{dd}I_{short-circuit}W_{n_{min}}f_{clock}\tau_{opt}ln3$$

Here,$V_{dd}$is= the given power supply ,α is= the switching factor whose value is taken as 0.15,f_{clock} is= the clock frequency,$I_{\ leakage}$ is= the leakage current that flows through the repeater,I_{offn} is= the leakage current that flows per unit NMOS transistor width,$W_{n_{min}}$is= the width of NMOS transistor used in minimum sized inverter and $I_{short-circuit}$ is= the short circuit current per unit width which is nearly equal to 65µA/µm.

CHAPTER 4

OPTICAL INTERCONNECTS

4.1 Introduction

For deep submicron VLSI based technologies ,it is extremely difficult to match the future requirements of high performance computer systems if we rely just on scaling and material innovation .These requirements are mainly bandwidth ,power consumption and delay .Clock speeds and wiring density inside systems have increased manifold ,thus electrical interconnects pose numerous difficulties not only on busses between boards but in off chip as well as on chip communication .Interconnect is one of the major consumer of electrical power .About 50% of the power is consumed by interconnect itself, which include data buses and buses used for clock distribution .Bandwidth of integrated circuits will go on increasing according to Moore’s law ,the existing traditional interconnects cannot compete even by using scaled versions.

Above complications and keeping an eye on our future requirements ,optical interconnects seem to act as potential substitute to other electrical interconnects .Optical interconnect are most suitable for global interconnects like data bus and clock networks . For local interconnects it would synchronize several on chip complex systems easily and also minimal thermal dissipation will occur in chip .The very high operating frequency of optical signals does not effect their propagation thus the modulation dependent crosstalk is avoided .Optical signals are quantum mechanically generated and detected .These signals are isolated from the other voltage signals due to process called quantum impedance conversion .This process could save us interconnect power consumption.

Unlike electrical interconnect ,where delay and power dissipation is due to resistive component present in the equivalent circuit, optical signals travel relatively faster due to absence of RLC impedances in the waveguide used. Thus the main source of power consumption .Using optics as way to communicate over a wide available bandwidth ,which could be further increased by exploiting WDM technique can attain high bit rates that are beyond the scope of any other interconnect.[21].

Optical interconnect system is primarily composed of four major modules : an off chip laser ,an optical modulator ,a waveguide to provide medium and an optical detector. Off chip laser is the light source operating at gigahertz frequency which modulators are coupled .Optical modulators are used so as to vary the property of light coming from laser source according to the data that is to be transmitted .Silicon integrated Optical modulators have been extensively studied and using two dimensional internment Optical waveguide can be constructed on a silicon strip waveguide or a rib waveguide [27].

A design based on SOI implicated optical interconnect module which uses lasers and photodetectors that are embedded on a three dimensional waveguide path can also be used for high performance system like processor incorporating multiple cores or interfaces used to link memory and processors [14].An optical receiver that has further three stages 1] first stage is that of optical detector whose primary function is to generate a current proportional to light intensity.2] A Transimpedance amplifier that convert the incoming current to voltage.3] Gain stages which provide sufficient gain so as to drive following circuit.

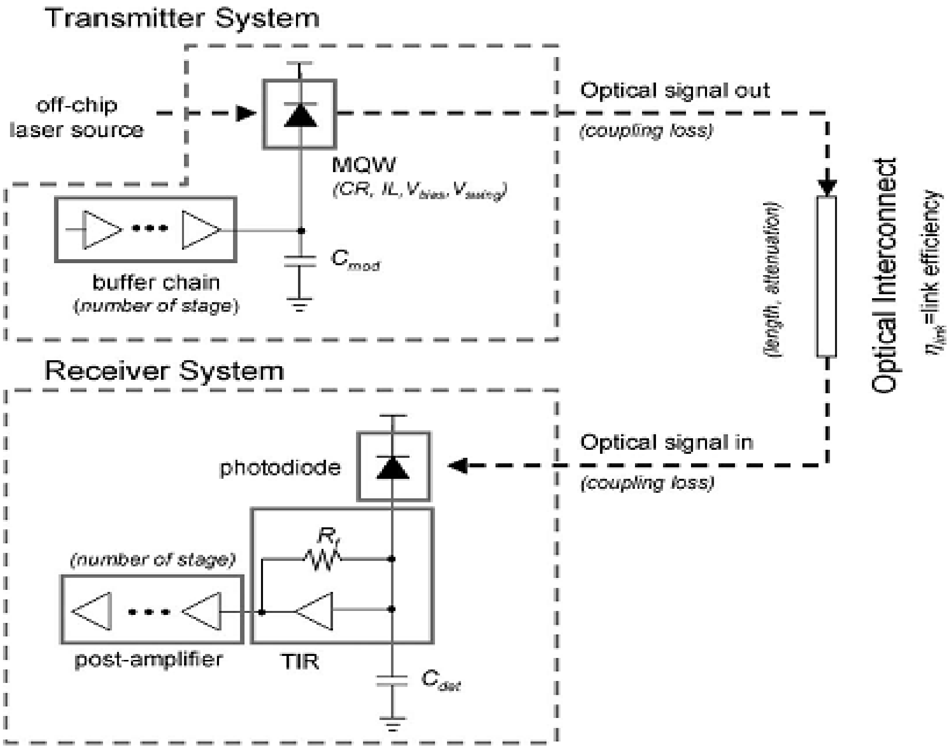

Figure 4.1: Schematic of quantum-well modulator-based optical interconnect.[28]

Optical based VLSI interconnect system firstly convert the incoming electrical signals to optical one. Waveguide is used just for routing purposes .Photodetector that converts light to current followed by TIA so as to get output voltage to drive the gain stages[29].Coupling among the modules of interconnect can be performed through waveguide gratings or 45 degree mirror as done in[14].

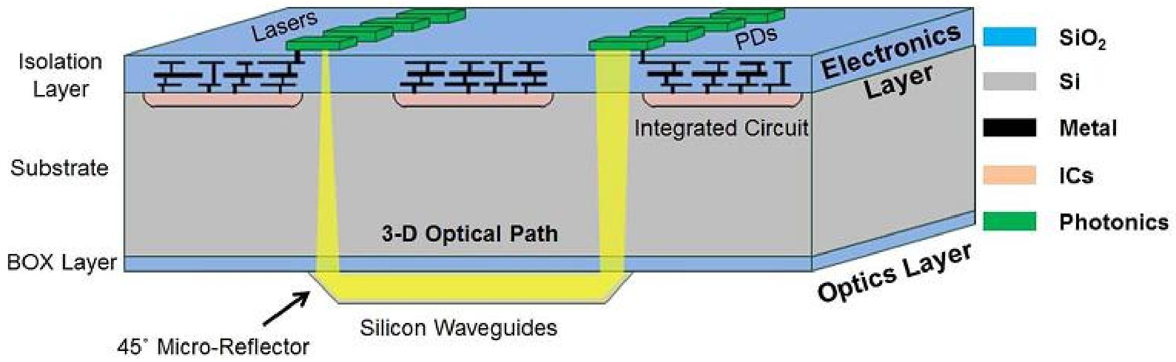

Figure 4.2: Cross sectional view of SOI-based optical interconnect[14].

Interconnects can be categorized mainly into two types that are local interconnects which typically have a propagation delay of 1 clock cycle whereas global interconnects hold on data for more than 1 clock cycle .Using OI's for long distance communication may be advantageous for global interconnection because electrical interconnect-based global interconnect suffers from large delay. The optical link offers a delay represented by

$$t_{opt} = t_{tx} + t_{wg} + t_{rx} \tag{4.1}$$

where the transmitter offers a delay t_{tx} ,and waveguide offers a delay represented by t_{wg} and t_{rx} is the delay offered by receiver end.

As far as bandwidth of optical interconnects is concerned , it can be improved further by using WDM technique ,with each new technology node,4 new channels are incorporated if this technique is used [29].

4.2 Transmitter

A transmitter used in optical interconnects system is composed of mainly two components ,electro-optical modulator followed by a driver circuit stage .One of the most difficult task is to embed optical interconnects on-chip using efficient CMOS compatible electro-optical modulator .Modulation in case of this interconnect system is a two–step process .First, some characteristic related to optical medium are varied according to electrical signals. Secondly ,modulation of optical signal is done which can be either by varying amplitude or phase .This is accomplished by varying optical characteristics of waveguide .To achieve modulation in crystalline silicon is quite demanding due to the reason that it does not have pockels effect and very weak kerr effect.Very few suitable mechanisms are available using which varying of refractive index in pure silicon either can be achieved .One of them is effect caused by free carrier plasma .There are two ways ,by which can change the concentration of carrier in silicon devices .One method is to put carriers into intrinsic region of p-i-n diode and extract carriers [30]. A notable change in concentration of carrier can be attained by above.

The other electrical structure is MOS capacitor [31].In this structure the modulation speed is high because the carrier concentration is changed by process of redistribution of carrier concentration rather than injection and extraction of carrier. Capacitance of current Si modulators is of the order in picofarads which is quite large.Thus tapered electrical devices are needed to drive the capacitance load [32].The delay of transmitter is given by

$$t_{tx} = N_{opt} u_{opt} \tau_r \tag{4.2}$$

If the capacitance offered by input gate is equal to the inverter output capacitance ,then size ratio between two neighbouring inverters is 3.6.First stage inverter is of minimal size. No.of stages can be determined by using

$$N = \frac{\log\left(\frac{C_m}{C_{g_0}}\right)}{\log 3.6} \tag{4.3}$$

Where C_m is modulator capacitance whose value is taken as 304fF.

4.2.1 CMOS circuits driving MQW modulator

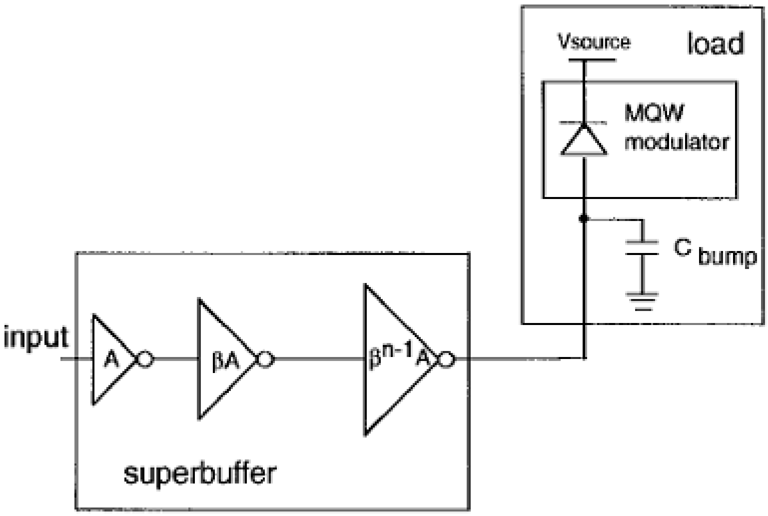

Figure 4.3: schematic of CMOS based superbuffer which is driven by MQW[33]

The above figure shows the diagram of a MQW modulator driven by a CMOS superbuffer circuit. The first stage is super buffer followed by the MQW modulator. Superbuffer is nothing but a sequence of inverters connected back to back .The size of each inverter is $\beta\ times$ the value of preceding inverter.The value of this β is between 3 or 4.Power dissipation in above figure is given by

$$P_{sb} = C_{total} \cdot \frac{BR}{2} \cdot {V_{dd}}^{2} \qquad (4.4)$$

C_{total} is capacitance offered by superbuffer .

Total capacitance is sum of input and output capacitance of inverters is of the form:

$$C_{total} = \left(C_{load} - C_{in,min}\right) + \sum_{k=0}^{n-1}\left(C_{in,min} + C_{out,min}\right) \qquad (4.5)$$

Where $C_{in,min}$ =input capacitance of the smallest sized inverter and $C_{out,min}$ is the capacitance offered at the output of imverter having same small size. C_{load} is capacitance which is driven by superbuffer circuit that includes equivalent capacitance of modulator and any other parasitic capacitance observed by inverter at the last stage of superbuffer .

Generally ,the equivalent capacitance offered by modulator is significantly low that a single inverter is enough to drive it but superbuffer which contains back to back differently sized inverters that perform a reduction in rising time from low to high of output signal which receiver consumes very less power [33].

The area used by MQW modulator is 12μm*12μm offers a capacitance of 0.2fF/μm^2. 59fF is the total equivalent diode capacitance is assumed to be applied for all CMOS technology sizes .The values of CR(contrast ratio) and IL(insertion losss) are the main parameters on which the performance of modulator are termed but at some valid supply voltage. Values of $V_h = V_l - V_{dd}$ and $V_l = V_{bias}$ are the maxima and minima of the output signal respectively.

The desired incident power at modulator is

$$P_{external} = \frac{2 \cdot F \cdot P_{opt,rec}}{\eta\eta_{link}(\eta\eta_L - \eta\eta_H)} \tag{4.6}$$

Where F is fan out and ηlink is link efficiency of system and $P_{opt,rec}$ is the required average optical power at detector input .Then, mean electrical energy dissipated due to absorption of light is

$$P_{diss,MQW} = P_{external} \cdot \frac{q}{hv} \cdot \left(\frac{\eta\eta_H V_H + \eta\eta_L V_L}{2}\right) \tag{4.7}$$

Where $P_{opt,rec}$ is equal to the mean optical power received at input ,F is the system fanout and ηlink is the optical system efficiency .Power consumed in the transmitter side is sum total of power absorbed at the input of modulator as well as the power dissipated in the subsequent stages of superbuffer.

4.2.2 VCSEL's with driver circuits

A driver circuits that are based on laser are equipped with the provision of matching the impedance at both , input and as well as output end .The adaptive stage is included so as to perform various tasks like reducing power consumption, level shifting of different kinds of signals compensating for variations in current ,eliminating jitter etc. The output driving stage is source of current to laser .The equivalent load is composed of laser diode and parasitic capacitance .

We assumed the value of current must be equal to threshold current of VCSEL's because the low current level must be 10% of the mean threshold current flowing across array.However ,the analysis specify that modulation current of VCSEL is more than threshold current at high frequency and thus contribution in overall power consumption in the link is high.

Moreover ,bandwidth of onchip VCSEL are not dependent on the ability of VCSEL's circuit which switch at high rates.this is because of the fact that ,the modulation current is more than threshold current at high switching activity .Thus the operating point of VCSEL's remains above threshold which in turn decreases the ON time.the values of modulation current and current at bias are settled at those points below which VCSEL's cannot operate.this fortify ON delay time of VCSEL's that can be ignored while reckoning the bandwidth.

CMOS driver Compatible VCSEL's :- VCSEL driver circuit comprises of two NMOS transistors (N_B and N_A) at the output stage which provide threshold and modulation respectively. The superbuffer drives gate of N_A.

VCSEL comprises of two parts of power dissipated of superbuffer given by (1) power consumption of VCSEL and two transistor because of their conduciveness .multiple driver can share single transistor because its .The bias transistor (N_c) can be shared .

Laser current (I_{total}) is the sum total of the threshold current (I_{th}) and average modulation current (I_{avg}) and average modulation current (I_m).the modulation current is assumed to have a dutycycle of 50%.As transistor N_A remains in the saturation region as the source voltage (V_{source})is equal to sum of the ON voltage of VcSEL's VCSEL(V_{th}),the voltage drop because of its series resistance (R_s) when the modulated current flows and the low source drain voltage($V_{dd} - V_{th}$) required to fortify

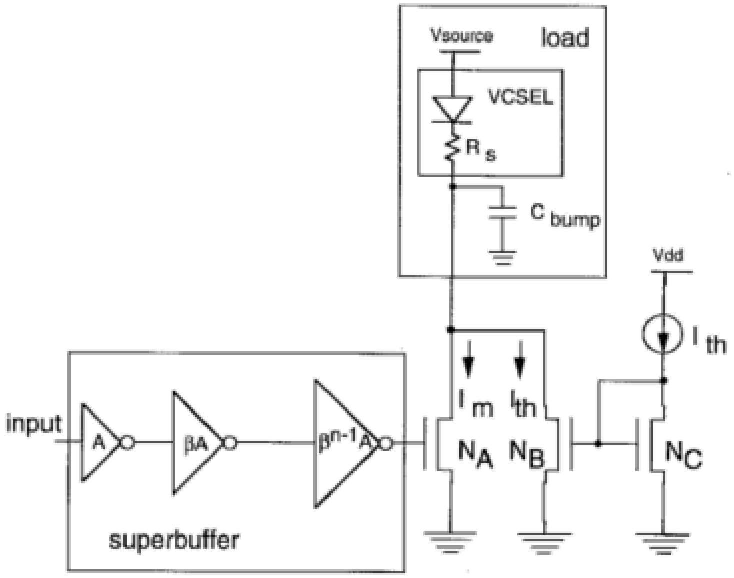

Figure 4.4: Schematic shows super buffer followed by VCSEL **[5]**

Power consume in VCSEL and in stage at output is

$$P_{CMOS,VCSEL} = I_{total} \cdot V_{source} = \left[I_{th} + \frac{I_m}{2}\right] \cdot [V_{th} + R_s \cdot I_m + \{V_{dd} - V_{th}\}] \tag{4.8}$$

For a given laser efficiency ($\eta_{,li}$) ,average output optical power is

$$P_{CMOS,VCSEL} = \frac{I_m}{2} \cdot \eta_{link} \tag{4.9}$$

The power consumed in totality in the transmitter current is thus the sum of (4.3)and (4.8)-the laser output of (4.9)

4.3 Waveguide

Wavelength of the utilized light is one of important factors which determine the performance of optical waveguides .The other factor is choice of material used to make the waveguide. While a capable waveguide like atomic crystal waveguide reduce the pitch of waveguide but it results in optical losses.

Waveguide material is primarily of two types which can be distinguished on basis of wavelength used for operation and applications for on-chip optical interconnect .Applications that require dense and short waveguide arrays uses silicon-on-insulator(SOI) based structure because it has a low valued pitch .In order to have less propagation delay and smaller losses inside the waveguide ,Low loss polymers are used[36][37].Polymer waveguide have refractive index of low value. The index varies from material to material but it usually have value of 1.43[37].The delay offered by optical waveguide is represented as following:

$$T_{wg} = \frac{N_{eff} \cdot L}{C} \tag{4.10}$$

Where N_{eff} is the effective index of waveguide medium ,C is the speed of light in the vaccum and L is length of waveguide as shown in figure 4.6

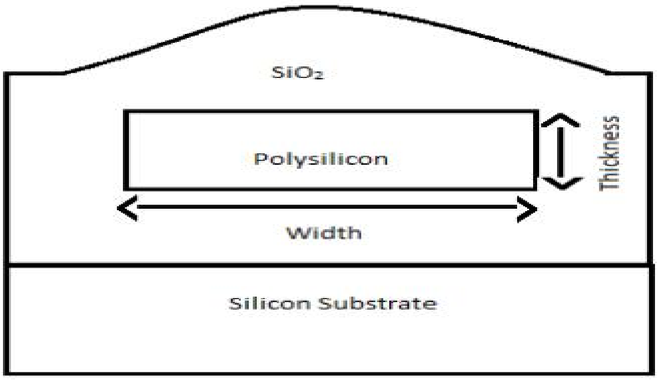

Figure 4.5: Polysilicon Waveguide

Waveguide on the as illustrated above are fabricated on Si/SiO2 as a substrate. The high dielectric constant confinement diminish the wavelength of light to dimensions of $\frac{\lambda}{n}$.the variations in the polymer waveguide material due to various factors can lead to clock skew situation.

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4.4 Optical Receiver

Optical receivers used in the interconnects are primarily having a configuration of transimpedance type due their high bandwidth ,low noise and easy to bias configuration.

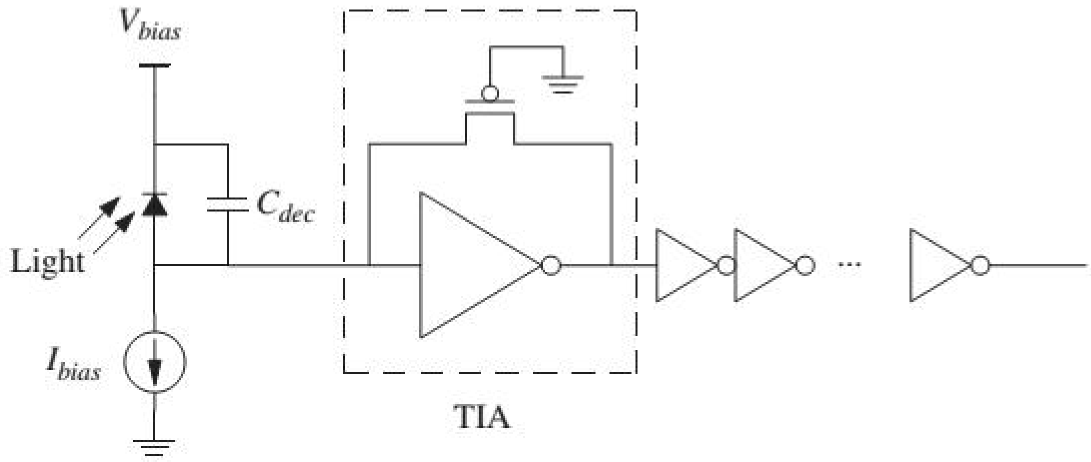

Figure 4.6: Schematic of optical receiver.[29]

The working model of a Transimpedance receiver is composed of four components (fig4.6) which are : the detector,the TIA (Transimpedance amplifier) and the decision making circuit. The photodetector firstly absorbs the light and correspondingly produces the photocurrent which depends on the responsivity and the intensity of optical signal ,an MQW photodetector with a 60fF total capacitance (including diode and bump capacitance)is supposed .Reduction in photodetector capacitance increase the optical to electrical efficiency for the receiver and improves the overall link performance [38] but the improvement of system parameters is not dependent on transmitter ,thus it can be kept fixed as scale down CMOS technology ,and compare the two transmitters.

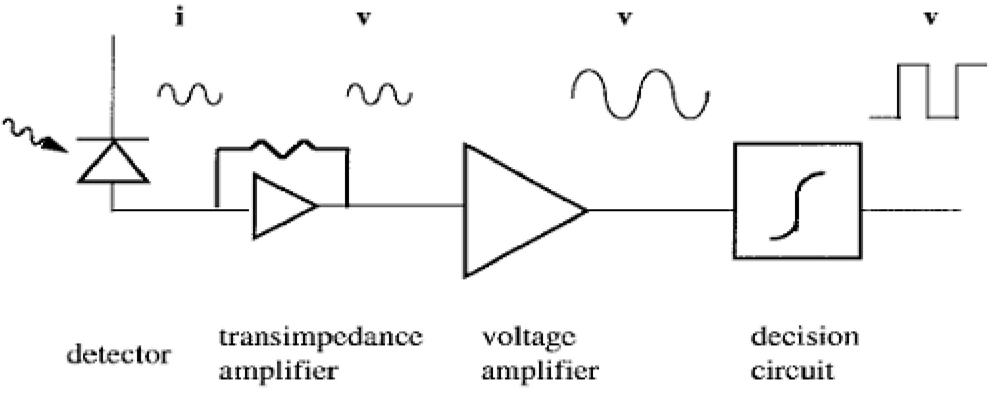

Figure 4.7: Stages of Optical Receiver.[33]

TIA converts photocurrent from the photodetector to an analog voltage which drives further driver stages .This voltage then fed to decision circuit which gives a output in binary form that are usable for computational logic circuits. The main purpose of optimizing the circuit of receiver is to minimize the same parameters that we have been discussing.One of the potential design used as TIA are differential cascade TIA in fig 4.7. The cascade and common source amplifier have almost equal gain ,but the cascade configuration have a less input capacitance. The cascade configuration has a drawback that a relatively higher voltage is needed to maintain the same gain as the common source topology, and there will be some noise due to common gate transistor.

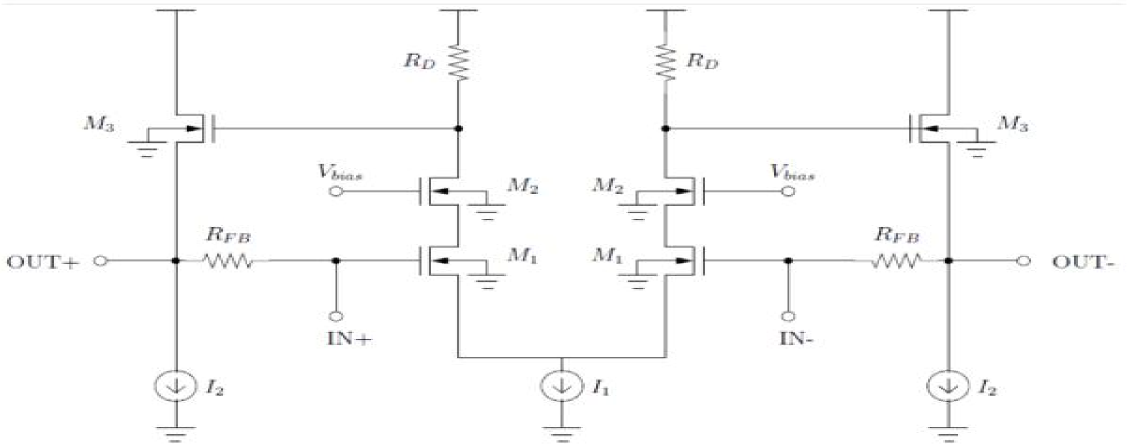

Figure 4.8: Differential Cascode TIA.[39]

There are various kinds of photodetectors used such as photodiodes with a p-n or p-i-n structure ,M-S-M photodetectors, photomultiplier and avalanche photodetector .Among all mentioned above M-S-M photodetectors has been the fastest and most efficient of all. Transit time of carrier and RC time constant required to charge equivalent detector capacitance are factors responsible for the latency of M-S-M based photodetectors[29].

$$T_r = ({\tau_{tr}}^2 + {\tau_{RC}}^2)^{1/2}. \tag{4.11}$$

Where

$$tr = \frac{x}{v}$$

$$\tau_{RC} = 2.2RC$$

Where v is the velocity with which carrier drift and x is the distance covered by the carrier in form of drifting through the medium .τ_{rc} is the time required by photogenerated carriers to travel to the electrical end driftly and the delay of M-S-M photodetector is expressed as [29].

$$T_D = 0.315T_r \tag{4.12}$$

The time required by the photodetector to produce a corresponding light reduces as the electrode size or area decreases. However there is an optimized value of area at which detector produces corresponding current is minimal [29].this because of the reason that when the electrode size is too small ,the latency of detector is dominated by RC time constant and when it is too broad ,the latency is dominated by the travelling time of carriers. Optical link delay must be composed of the delay required by TIA to produce an amplified output voltage. The delay of TIA is calculated to be (4.13)

$$T_D = \frac{0.693}{2\pi\Delta f} \tag{4.13}$$

While calculating above it has been assumed that the system is one-pole .Δf is bandwidth requirement. Equation of cumulative delay given by the receiver is given by the following :

$$t_{rx} = 0.315\sqrt{(2.2RC)^2 + (X/v)^2} + \frac{0.693}{2\pi\Delta f} \tag{4.14}$$

The circuitry of receiver are mostly based on current source inverters made of CMOS.For any node ,it gives us an idea of about the imperative factors involved in circuit designing.These include factors like rise time ,fall time ,mean energy consumed and electrical power comsumption .it also include number of stages like TIA ,voltage amplifier decision making circuits.[40].

The rise and fall time of output pulse are assumed to have values that are equal to some percentage of period to fortify an acceptable BER. The most error rate that acceptable is given by.

$$BR = \frac{\zeta}{\sqrt{t\Gamma_{in}^2 + t\Gamma_{rec}(s,p,w,v)^2}} \tag{4.15}$$

Where $t\Gamma_{in}$ is given by rise time of optical input pulse and $t\Gamma_{rec}$ is the rise time of the receiver amplifiers .

The mean optical power value desired at the detector input is represented as

$$P_{opt} = \frac{V_{dd}}{2.A_{dc} \cdot R_{pd} \cdot [A_v \cdot (w,v)] \cdot p \cdot Z_f(s,w,v)} \tag{4.16}$$

Where A_{dc} is the voltage gain of decision making circuit in the receiver ,R_{pd} is responsivity of detector ,A_p is the voltage gain of the voltage amplification stages and Z_f is the transimpedance of the amplifier. The efficiency of transmitter and fanout of transmitter determines the optical power at the detector end of the receiver and thus electrical power consumption is represented by

$$P_{elec,receiver} = (s + p) \cdot I_{ds}(w, v) \cdot V_{dd} \tag{4.17}$$

Where I_{ds} is the current used for biasing and is a function of variables w and v.

4.5 Conclusion

The optical interconnect has the potential to replace copper as well as other interconnects at the global level due to variety of reasons. The first and foremost reason is that optics operate at high frequency efficiently and the future high performance systems will be compatible at those high frequencies .Enormous amount of bandwidth is available if we use optics as mode of communicating. Optical interconnects are free not only from any capacitive loading effects but also it does not have any equivalent RLC circuit, which further makes it immune to resistive loss. Optical interconnects do not suffer from crosstalk also. Various transmitter and receiver where tested using TANNER TOOL AND T SPICE simulations where conducted to calculate delay and power dissipation of the optical interconnect.

CHAPTER 5

Results & Discussions

5.1 Parameters Of Copper Interconnects

The equivalent circuit of interconnect is represented by a RLC circuit and the values of each parameters that is value of R,L and C are to calculated by using physical geometries of the interconnect. For a given technology node and a given layer, the interconnect thickness is represented by T, the height of the metal layer from the substrate is given by H, the width W and spacing between the signal and ground line S are the most common variables used to optimize the global interconnect. The width of interconnect and spacing between interconnects are optimized under two situations, 1) spacing between them is kept minimal and 2) spacing is kept equal to the width line , for various International Technology Roadmap for Semiconductors (ITRS) technology nodes. Various parameters w, s, t, h and dielectric constant k are shown below in table 5.1 for various technology nodes.

Table 5.1 Equivalent parametric values of top layer of metal at different technologies

Technology Nodes	**Width(µm)**	**Space(µm)**	**Thickness(µm)**	**Height(µm)**	**Dielectric Constant - K**	**Length(µm)**
90nm	0.5	0.5	1.21	0.29	2.7	10000
65nm	0.48	0.58	1.18	0.19	1.9	10000
32nm	0.058	0.058	0.139	0.0904	1.95	10000
14nm	0.024	0.024	0.0692	0.0498	1.95	10000

R, L and C parameters are calculated using Shyh- Chyi Wong’s TSM model which uses values given in Table 5.1.The values of different parameters is calculated at different no of reapeaters used. The values of resistance are in ohms, the values of inductance are in nH and value of capacitances are in fF.

Table 5.2: Calculated values of R, L and C parameters at 14nm node at 10mm.

Quantity of repeaters	**R**	**L**	**C**
1R	89.67K	25.83	155.96
3R	30.22K	8.89	51.96
5R	18.12K	5.43	31.39
7R	12.91K	3.65	21.96
9R	9.89	2.91	17.31

Table 5.3: Calculated values of R, L and C parameters at 32nm node at 10mm

Quantity of repeaters	**R**	**L**	**C**
1R	30.67	24.01	200.27
3R	10.65	8.01	63.39
5R	6.33	4.89	40.43
7R	4.56	3.42	27.89
9R	3.51	2.72	22.43

Table 5.4 : Calculated values of R, L and C parameters at 65nm node at 10mm.

Quantity of repeaters	**R**	**L**	**C**
1R	391.41	18.65	2296.89
3R	136.96	6.35	742.67
5R	80.42	3.32	444.89
7R	58.21	2.72	327.43
9R	46.19	2.13	243.99

Table 5.5 : Calculated values of R, L and C parameters at 90nm node at 10mm.

Quantity of repeaters	**R**	**L**	**C**
1R	365.96	19.67	2548.79
3R	120.8	5.59	832.32
5R	67.89	4.01	522.80
7R	49.96	2.45	355.97
9R	38.62	2.09	279.93

5.2 Delay analysis of optical and copper interconnects

Delay of the optical and copper interconnects increases with the decrease in frequency .Delay in case of transmitter can be optimized by using tapered driver circuits in which each of the inverter is of size 2.3 (value of e) times the preceding inverter. For aspect ratio of 80, the delay was at its minimum when working on 14nm technology node. So aspect ratio of 80 was used through out the analysis when calculating the delay of receiver too. The delay per unit length value of global Cu wires using optimized repeaters , is shown. Uncertainty in delay is caused due to the geometric variations and changes that occur in environment that include. We have not considered the delay due to environmental factors .Crosstalk coupling exists only in electrical interconnects but not in optical interconnects. In future technology nodes it is expected that uncertainty in delay because of situations like clock skew will reduce in case of the optical interconnect . Whereas ,in case of copper ,the delay uncertainty will increase with increase in number of repeaters. To attain minimal delay ,optimal size and number of repeaters must be known.Time duration for which data is through waveguide is assumed to be equal. The delay of some components of the transmitter and receiver of optical interconnects is determined using TSPICE simulation,while some of them were calculated using equations. Following are the table at different frequencies. Delay of optical and copper interconnects is shown at 25 MHz frequency in Table 5.3.

Table 5.6: Distribution of delay in various parts of optical interconnect vs Cu interconnect at 25 Mhz.

Technology Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Modulator driver	84.63	74.93	60.29	54.27	44.92
Modulation	73.24	64.32	52.32	46.52	38.28
Detection	22.16	17.34	18.92	16.67	13.89
Receiver Amp	80.62	69.32	55.82	48.69	35.81
Waveguide	47.3	47.3	47.3	47.3	47.3
Optical delay	308.95	274.11	235.65	214.45	181.2
Copper delay	1820	2010	2200	2640	2810

Performance of optical links and copper links on the basis of delay(ps) for different technology nodes at 50 Mhz is given in Fig.5.2.

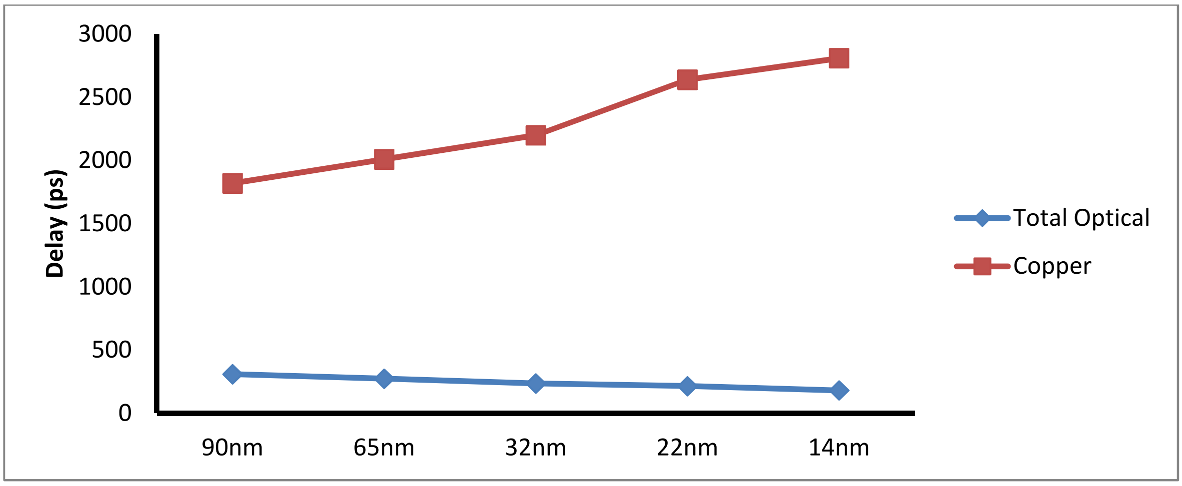

Figure 5.1: Delay comparison between Optical interconnects and Cu interconnects(at 25 Mhz).

Table 5.7: Distribution of delay in various parts of optical interconnect vs Cu interconnect at 50 Mhz.

Technology node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Modulation driver	73.59	64.32	46.79	43.82	31.29
Modulation	59.12	51.26	42.39	31.73	25.26
Detector	12.96	10.73	8.96	7.32	5.59
Receiver Amp.	71.32	60.23	46.96	36.85	24.96
Waveguide	47.3	47.3	47.3	47.3	47.3
Total Optical	265.29	234.84	193.4	168.02	135.4
Copper	1280	1450	1730	2120	2410

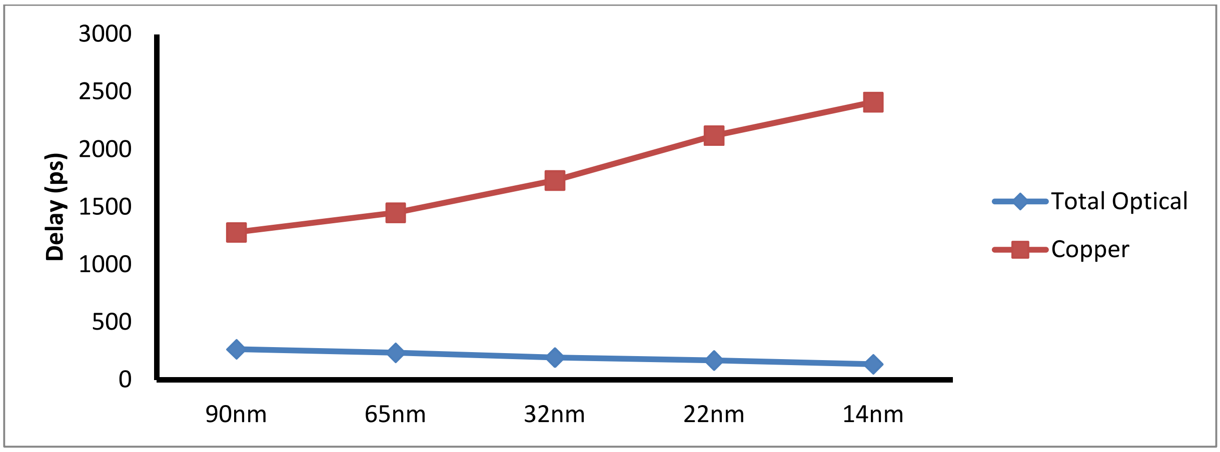

Figure 5.2: Delay comparison between Optical interconnects and Cu interconnects(at 50 Mhz).

Table 5.8: Distribution of delay in various parts of optical interconnect vs Cu interconnect at 75 Mhz.

Technology node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Modulation driver	69.2	55.62	43.23	37.45	24.13
Modulation	56.9	44.28	37.54	29.16	20.89
Detector	9.61	7.72	6.43	5.92	2.9
Receiver Amp.	65.52	56.42	44.12	33.1	22.33
Waveguide	47.3	47.3	47.3	47.3	47.3
Total Optical	249.53	212.34	179.62	153.93	118.55
Copper	990	1150	1440	1810	1900

Performance of optical links and copper links on the basis of delay(ps) for different technology nodes at 75 Mhz is given in Fig. 5.3.

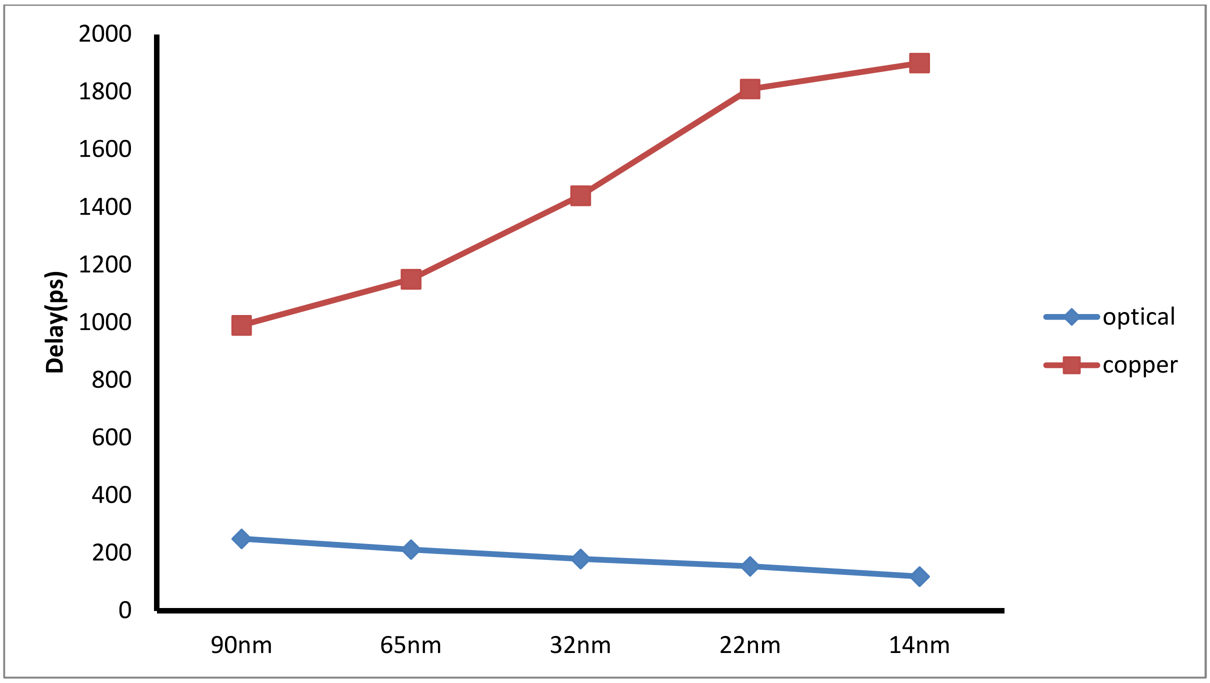

Figure 5.3: Delay comparison between Optical interconnects and Cu interconnects(at 75 Mhz).

Table 5.9 Distribution of delay in various parts of optical interconnect vs Cu interconnect at 100 Mhz.

Technology Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Modulator driver	69.7	53.1	42.1	35.67	21.29
Modulation	58.6	42.1	53.9	26.93	19.87
Detection	8.13	6.85	4.15	2.87	195
Receiver Amp	64.3	54.89	41.97	31.67	20.67
Waveguide	47.6	47.6	47.6	47.6	47.6
Total Optical	249.33	205.54	172.72	145.74	112.38
Copper	970	1150	1140	1850	2060

Performance of optical links and copper links on the basis of Delay(ps) for different technology nodes at 100 Mhz is given in Fig. 5.4.

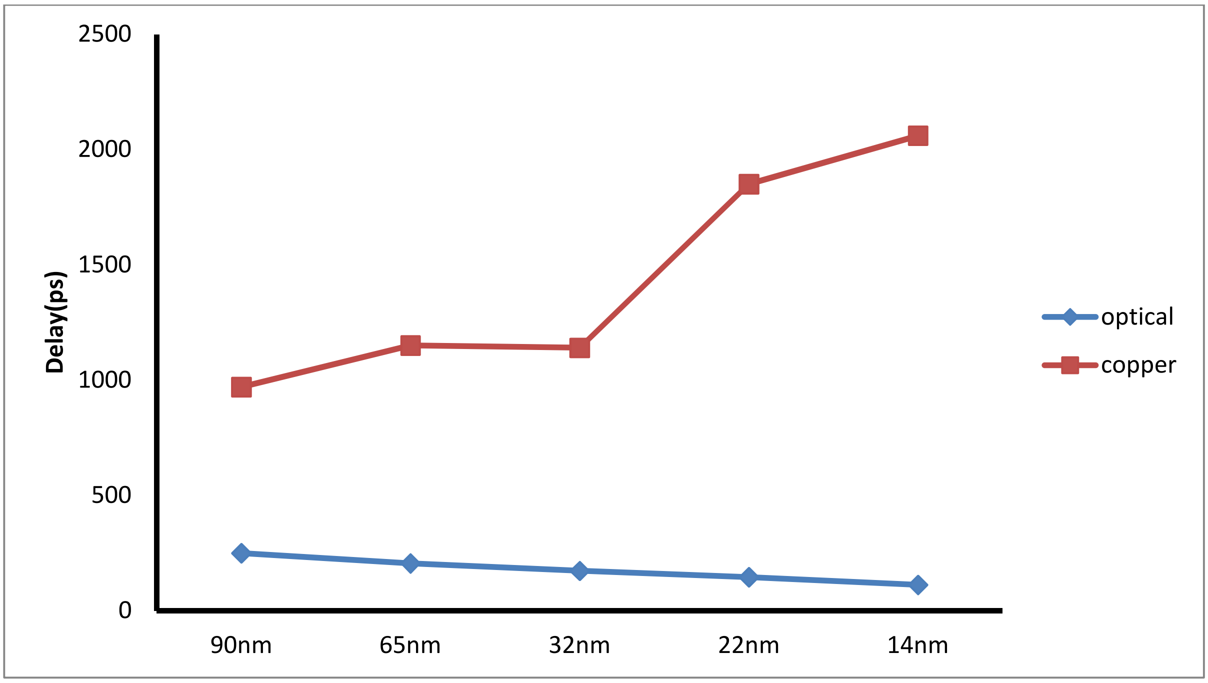

Figure 5.4: Delay comparison between Optical interconnects and Cu interconnects(at 100 Mhz).

As frequency increases the delay of both the interconnects decreases. Optimized results are obtained at 100MHz in case of optical interconnects.

5.3 Power Dissipation analysis of optical and copper interconnects

In electrical interconnects, analysis of power is to be done under some particular design constraints , such as delay and bandwidth. A wire without any repeater circuit cannot survive at global interconnect level because of the substantial delay involved and low bandwidth offered on the line. The optical power loss in the waveguide is so small that it can be ignored. Work has been done precisely is comparison of electrical interconnects with that of optical interconnects. The power consumption of transmitter is more than that of receiver side. Power of both show an increasing trend as we move towards future technology nodes. Simulations are carried out on TSPICE and they are carried out for different frequencies. Power dissipation by various components of optical receiver and transmitter at 100 Mhz is shown in the following table at 100 Mhz

Table 5.10: Distribution of power among the components of optical link vs Cu link at 100 Mhz.

Tech. Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Transmitter	0.86	1.42	3.92	7.32	8.95
Receiver Amplifier	0.48	1.22	2.56	4.25	5.36
Optical	1.34	2.64	5.48	10.57	13.31
Copper	2.81	4.62	9.56	17.29	21.39

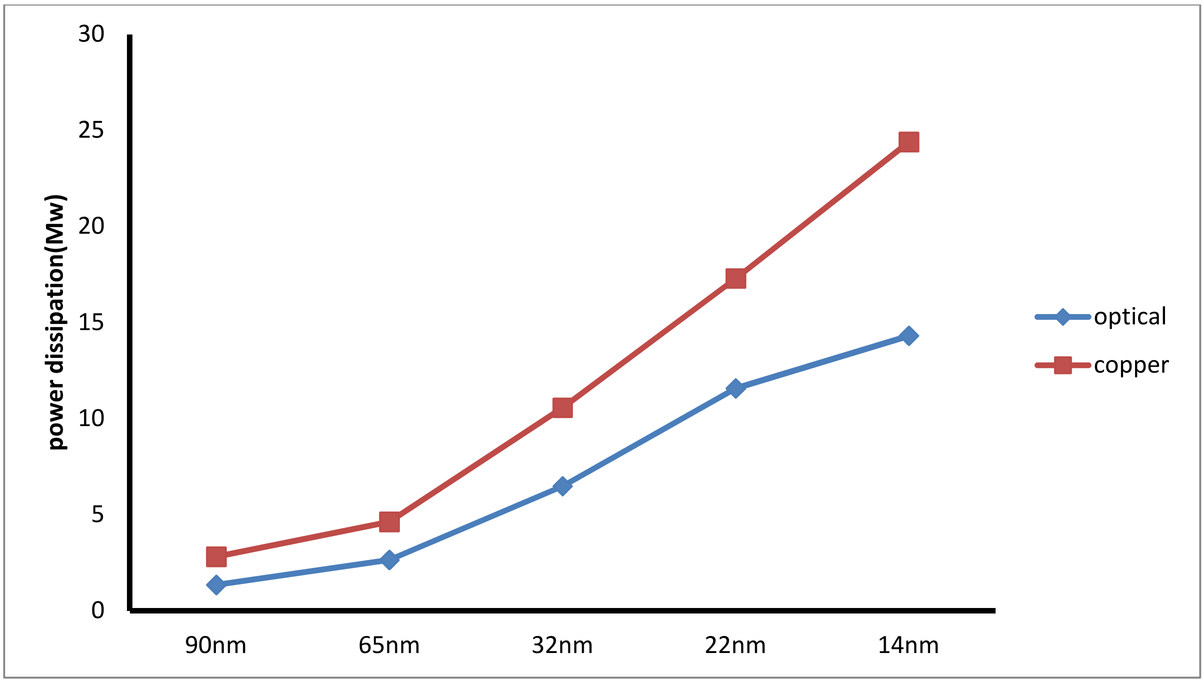

Figure 5.5: Power dissipation comparison between Optical interconnects and Cu interconnects(at 100 Mhz).

Table 5.11: Distribution of power among the components of optical link vs Cu link at 75 Mhz.

Technology Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Transmitter	0.12	0.67	1.53	2.43	5.73
Receiver Amplifier	0.069	0.43	1.21	1.52	3.12
Total Optical	0.189	1.1	2.74	3.95	8.85
Copper	0.92	2.63	5.46	13.1	17.27

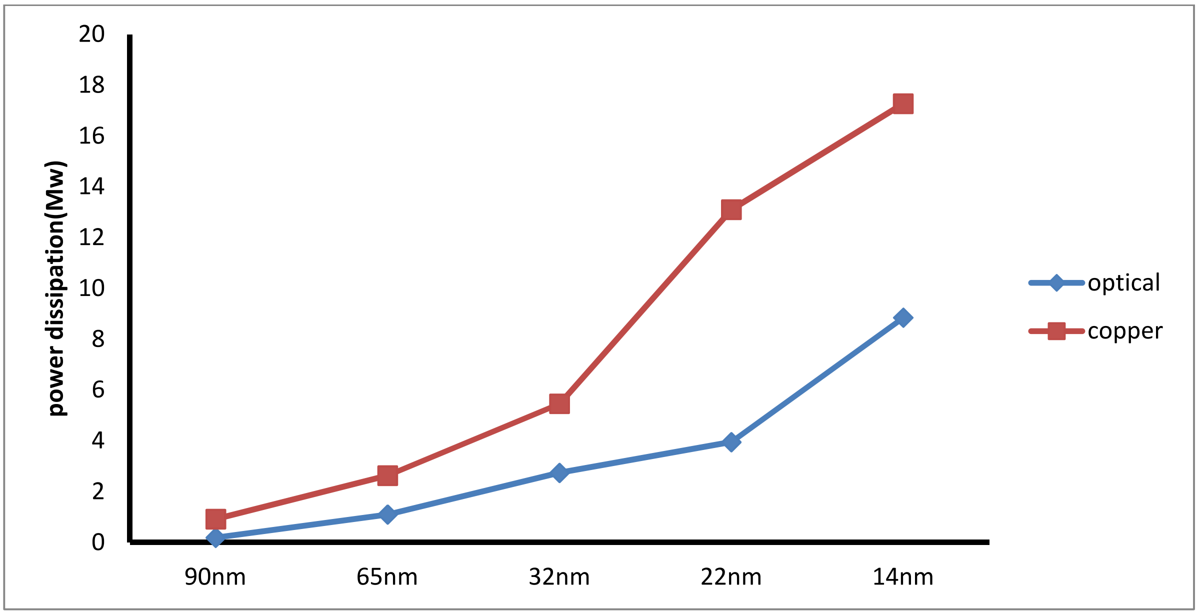

Figure 5.6: Power dissipation comparison between Optical interconnects and Cu interconnects(at 75 Mhz).

Table 5.12 Distribution of power among the components of optical link vs Cu link at 50 Mhz.

Tech. Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Transmitter	0.068	0.18	0.56	1.25	2.36
Receiver Amp	0.0042	0.09	0.13	1.01	1.25
Total Optical	0.0722	0.27	0.69	2.26	3.61
Copper	0.092	1.12	2.45	5.13	9.82

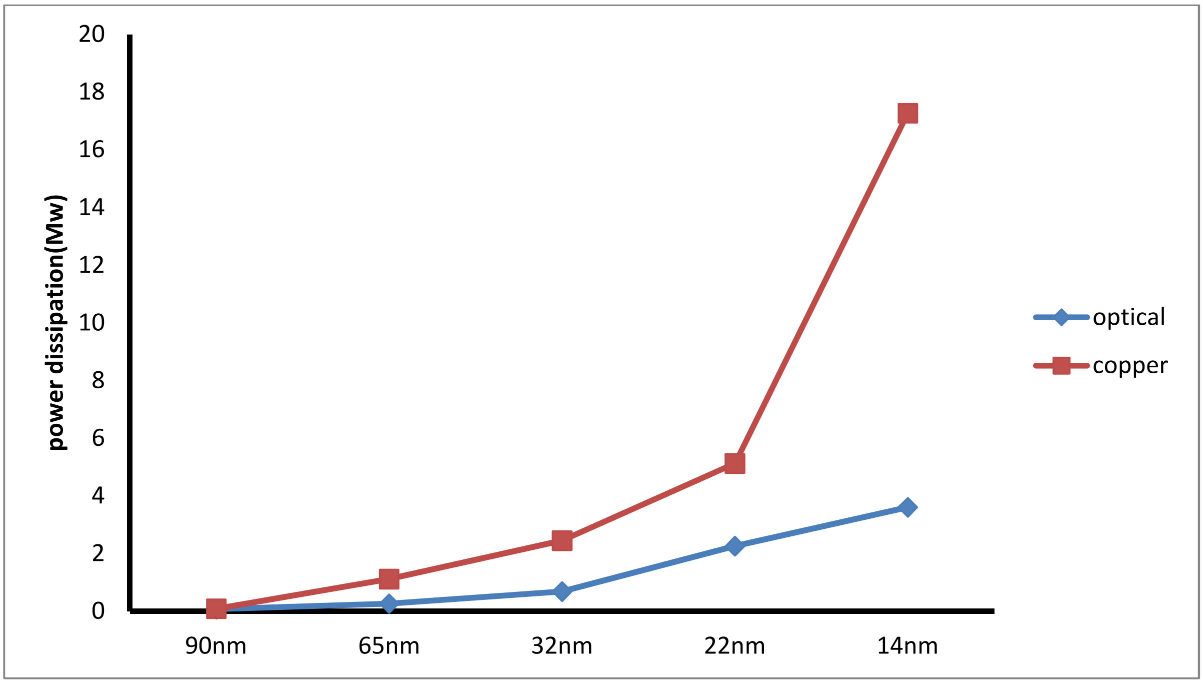

Figure 5.7: Power dissipation comparison between Optical interconnects and Cu interconnects(at 50 Mhz).

Table 5.13 Distribution of power among the components of optical link vs Cu link at 100 Mhz.

Tech. Node	**90nm**	**65nm**	**32nm**	**22nm**	**14nm**
Transmitter	0.0003	0.00012	0.072	0.091	1.1
Receiver Amp	0.00062	0.0016	0.021	0.053	0.092
Total Optical	0.00092	0.00172	0.093	0.144	1.192
Copper	0.0009	0.002	0.3	0.92	1.83

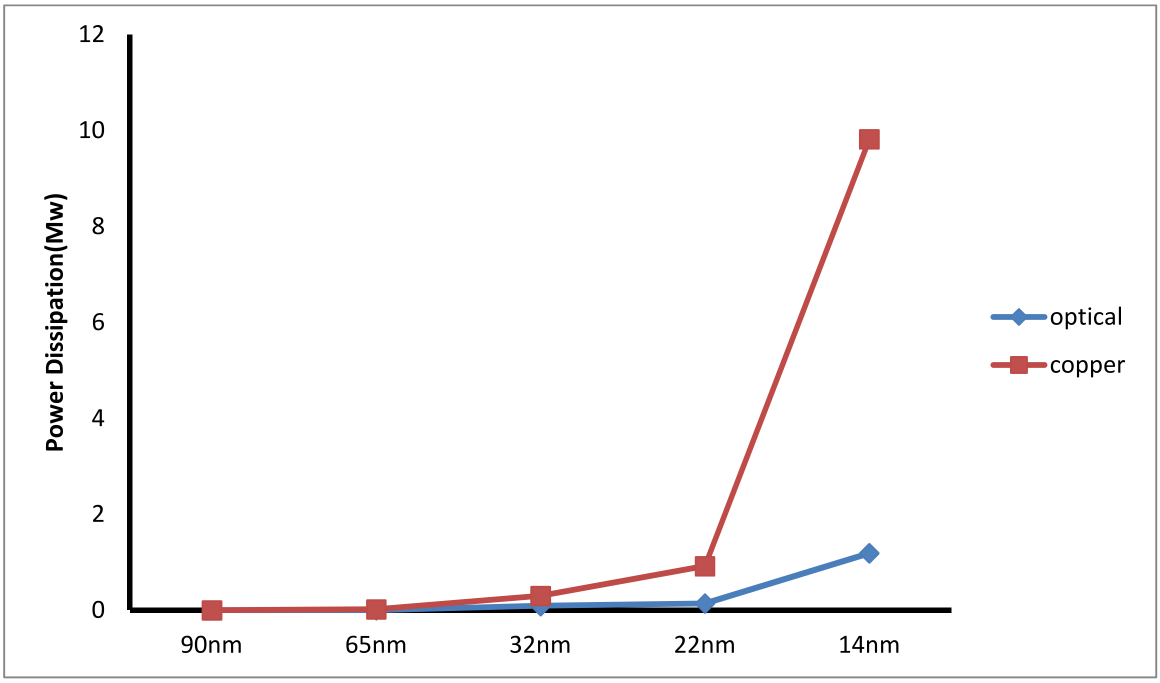

Figure 5.7: Power dissipation comparison between Optical interconnects and Cu interconnects(at 25 Mhz).

Dissipation of power in both interconnects increases as we move towards smaller technology nodes. The power dissipation in optical interconnects is comparable to copper interconnect at lower frequencies but as we keep on increasing the frequency , the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects resulting more efficient operation in terms of power also. So it can be said that optical interconnects suffers from a tradeoff between power and density.

5.4 Bandwidth and Gain of TIA

Gain of TIA is an important factor which influence the performance of optical receiver .Gain of the TIA used in this dissertation came out to be 86dB and had an optimized bandwidth of 2.1Ghz. Thus ,it can be seen that if bandwidth is an important factor, a single optical link may not serve the purpose of efficient optical transmission. Therefore to increase the bandwidth density of the optical link , incorporation of WDM into system is recommended.

CHAPTER 6

Conclusion and Future scope

6.1 Conclusion

This thesis studies the performance of Cu and optical interconnects for off-chip communications on the basis of two main parameters i.e power dissipation and delay. It studies various aspects of optical interconnects. As applications associated with external sources are concerned , fast optical and electrical interconnects are compared on the basis of above relevant metrics. As far as bandwidth of optical interconnects is concerned, it highly depends on the type of TIA used. We can increase bandwidth density by incorporating WDM . But one must be careful to optimally analyze the trade off between the gain of TIA and the bandwidth offered by that Trans-impedance amplifier. Choosing a optimal aspect ratio is also an important factor, when it comes to delay . Optical interconnects when optimized in terms of power sometimes may offer disadvantages because of the fact that delay may start increasing beyond certain length. Beyond the 32nm technology node, with its proportional bandwidth requirement, optical interconnects becomes favourites for communication when distances are as little as 10 cm. In addition, we have also scrutinized two types of optical transmitter technologies for global link:1] the vertical cavity surface emitting laser (VCSEL) and 2] the quantum well modulator (QWM). For power efficient systems VCSEL-based links are commendatory as compared to QWM-based links provided that bandwidth is large and the distance is long . However, if we see the practical scenario, it is difficult to drive current VCSELs are beyond 15-20 Gbps and they are prone to reliability problems particularly in at high temperatures. Thus, While working on lower detector and modulator capacitances , it is recommended to use The QWM. Moreover, we calibrate the design requirements desired by the modulator under which it is superior substitute to VCSEL technology as a function of bandwidth, link segment length, and transmitter and equivalent capacitances of detector. We found that QWM are more efficient as compared to VCSELs in case of power consumption, as both the modulator as well as photodetector require low value capacitances for efficient working.

We analyzed the aftermaths of scaling in technology nodes on the optimization of design of modulator. The modulator design parameters doesnot depend on the transistor parameters . The power dissipations show two conflicting trends which depend on the operating speed and capacitances of the various devices . Devices which are slow and are having small capacitances decrease the power consumption as we move towards smaller technology nodes.

.At lower frequencies ,the power dissipation in optical interconnects is more as compare to copper interconnect but as we keep increasing frequency, the power dissipation in the optical interconnects keeps on decreasing as compared to copper interconnects. This trend suggest that optical interconnects will work efficiently when incorporated in high performance computer (HPC) systems.

6.2. Future Scope

Lots of work can be done in this domain. There are varying fields of bandwidth density,noise immunity, crosstalk in which optical interconnects have to improve there performance further. The emphasize should be on modelling of end devices of the optical interconnects. Incorporating various techniques like WDM , and side by side inventing new devices and circuit designs which can efficiently optimize the future targets to be achieved . Optical interconnects will also have optical waveguides (optical fibres). Managing so many optical fibres on on-chip system modules will be a difficult task. There are various capable options relating to optical interconnects whose performances are must be explored in the relevant context of systems that involve innovations like receiver designs having no power consuming component like TIA. These solutions may naturally fasten the application of optical interconnect for small distance communications.

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