PERFORMANCE ANALYSIS OF GRAPHENE NANORIBBON AS VLSI INTERCONNECTS

Dissertation submitted in partial fulfillment of the requirements
for the award of the degree of

Master of Technology

In

VLSI Design

Submitted by

Ankit Gupta

Roll. No. 601261008

Under the supervision of

Dr. Mayank Kumar Rai

Assistant Professor, ECED

Department of Electronics & Communication Engineering

Thapar University, Patiala

INDIA

July, 2014

CERTIFICATE

I hereby declare that the work which is being presented in the dissertation entitled, **"Performance Analysis of Graphene Nanoribbon as VLSI Interconnects"** in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) at the department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Mayank Kumar Rai, Assistant Professor, ECED.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of any other degree.

Date: 30/06/2014

Ankit Gupta
Roll.No.601261008

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Dr. Mayank Kumar Rai
Assistant Professor
ECED,Thapar University

Counter signed by:

Dr. Sanjay Sharma
Professor & Head
ECED, Thapar University
Patiala-147004

Dr. S. K. Mahopatra
Dean of Academic Affairs
Thapar University
Patiala-147004

ACKNOWLEDGEMENTS

I take this opportunity to express my profound sense of gratitude and respect to all those who helped me through the duration of this dissertation. I acknowledge with gratitude and humility my indebtedness to **Dr. Mayank Kumar Rai, Assistant Professor,** Department of Electronics and Communication Engineering, Thapar University, Patiala, under whose guidance I had the privilege to complete this dissertation. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the dissertation work.

I convey my sincere thanks to **Head of the Department, Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Kulbir Singh, Associate Professor, ECED**, entire faculty and staff of Electronics and Communication Engineering Department for their encouragement and cooperation.

My greatest thanks are to all who wished me success especially my family. Above all I render my gratitude to the Almighty who bestowed ability and strength in me to complete this work.

Ankit Gupta

This work is dedicated to my father ,mother and my brother who shaped much of the way I think, instilled my confidence and technical desire, and unknowingly coined many of phrases by which I live my life.

ABSTRACT

The present work is an effort to find a solution for the problem faced by copper material in deep submicron technology node. With the advancement in technology, the resistivity of copper interconnects is increasing steeply due to surface scattering and grain boundary effect. Carbon nanomaterials like (Carbon nanotube) CNT and (Graphene Nanoribbon) GNR are considered as the attractive candidates for future VLSI interconnects due to large mean free paths and its capability to conduct high current density and high thermal conductivity.

In this thesis report, Performance of MLGNR interconnects has been analyzed at 22 nm technology node. Similar analysis is carried out for copper interconnect and results are compared with MLGNR for local, semi-global and global interconnects. SPICE simulation results reveal that MLGNR interconnects perform better than copper for local, semi-global and global interconnects. The influence of number of layers on MLGNR interconnect performance in terms of propagation delay, power dissipation and power delay product is analyzed and it has been seen that the performance improves for more number of layers. The impact of interlayer resistance on performance of MLGNR interconnect is analyzed.

The dependence of Fermi energy on impedance parameters is also critically analyzed and its effect on performance of MLGNR is examined. Finally, the effect of increase in contact resistance on propagation delay is analyzed for different lengths in MLGNR interconnect for global lengths.

List of Contents

List of Figures

List of Tables

ABBREVIATIONS

AR	Aspect Ratio
IC	Integrated Circuit
LSI	Large Scale Integration
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
EM	Electo-Magnetism
FET	Field Effect Transistor
GNR	Graphene Nanoribbon
MLGNR	Multilayer Graphene Nanoribbon
GaAs	Gallium Arsenide
GHz	Giga Hertz
MFP	Mean Free Path
MSI	Medium Scale Integration
MWCNT	Multi Walled Carbon Nanotube
RC	Resistance-Capacitance
RLC	Resistance-Inductance-Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
SWCNT	Single Walled Carbon Nanotube
VLSI	Very Large Scale Integration

CHAPTER

1

INTRODUCTION

1.1 Introduction

An Interconnect is the thin film of conducting material that provides electrical connection between two or more nodes of the circuit formed on the silicon chip. In the deep submicron technology, interconnect delay dominates the gate delays and the gap between them is increasing with more technological advancement. The resistivities of the presently used interconnect steeply increases with the dimensional scaling due to the surfaces roughness and grain boundary effect. As a result, propagation delay and power dissipation increases. To reduce the ever increasing gap between the performance of devices and interconnects, replacement of presently used interconnect (copper) can be thought with the other materials which are suitable for interconnect applications.

1.2 Motivation

Scaling of the device dimensions of the digital electronic circuits and their performance has been driven by Moore's law over many years. This led to the improvement in performance of the logic components in the microprocessor. In the earlier decades, On-chip interconnects were considered only as a parasitic load and today it became the real performance bottleneck due to its reduced cross section dimensions [1]. It is predicted that interconnects will be responsible for nearly 70 to 80% of the signal delay in high-speed systems.

With the advancement in technology, minimum feature size is decreasing and the packing density is increasing. With the decrease in the minimum feature size of interconnects, the cross

sectional area also decreases. As more and more devices are integrated in a single chip, the average length of interconnect increases which increases the propagation delay [2].

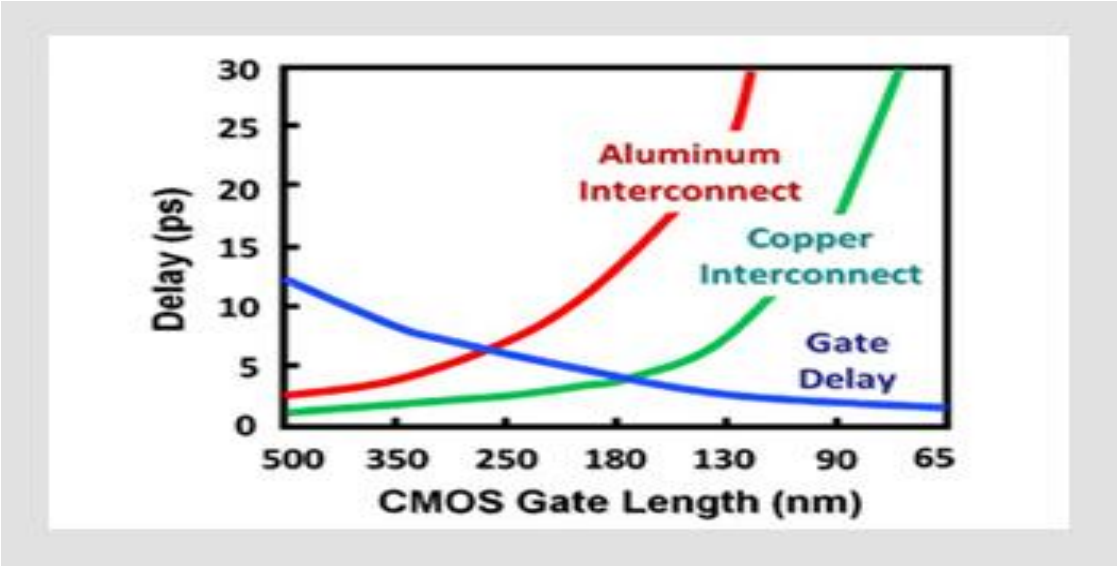

Fig. 1.1 Interconnect delay dominates gate delay in sub-micron CMOS technologies [4].

Reduction in dimensions led to the improvement in the intrinsic delay of the transistors whereas the intrinsic delays of the interconnect stay almost a constant. Thus with technological scaling, the gap between the intrinsic delays of transistors and interconnects is increasing [3]. The interconnect performance becomes important in calculating the overall performance and it becomes dominant for more advanced technology nodes.

Fig1.1 shows the comparison of gate delay and interconnect delay for different technology nodes. As the dimensions are reduced, gate delays reduces dramatically and the interconnect delays increases. Interconnect delay starts to dominate the gate delay for sub-micron technologies [4]. The delays associated to Aluminium interconnects is higher when compared to copper interconnects.

1.3 VLSI Interconnect

A VLSI interconnect is a thin film of conducting material that provides electrical conduction between two or more nodes of the circuit formed in a silicon chip. Interconnects can also be termed as wires that connect components on a VLSI chip, and these chips to other chips in a multichip module. Interconnects are important as transistors because it can affect the speed,

power and noise of a system. Based on length, interconnects are classified as local, semiglobal and global interconnects.

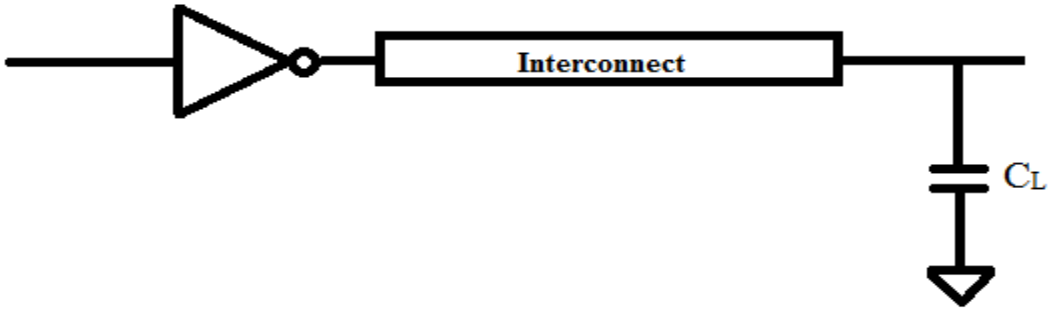

Fig. 1.2 CMOS inverter driving an Interconnect.

1.4 Statement of problems

Following objectives have been carried out in this thesis:

1. Study the performance of GNR (Graphene Nanoribbon) as VLSI interconnect at local, semi-global and global lengths.
2. Study the effect of number of layers on performance of GNR based interconnects.
3. Study the influence of Fermi energy on MLGNR (Multilayer GNR) interconnect performance.
4. Study the impact of Interlayer resistance on performance of MLGNR interconnect.
5. Compare the performance of GNR with copper interconnects at 22 nm technology node.

1.5 Thesis Organization

Chapter 2 starts with a literature review. Starting from the study of the properties of graphene based interconnects and their comparison with copper Followed by the study of different types of conductance models developed by different Authors and the RLC models proposed for the Analysis of different interconnection parameters.

Chapter 3 briefly introduces the basic concepts of interconnect analysis and its delay evaluation. The major repeater insertion techniques for improving signal delay are also discussed. The evolution of todays interconnect from the traditional interconnect is briefly explained. Later the

RLC equivalent model for copper interconnect and impedance parameters calculation has been shown.

In **Chapter 4,** applicability of GNR interconnects as VLSI interconnect is analyzed. Starting from the basics of GNR, Types of GNR and their classification on the basis of number of layers is explained. Using the RLC model of MLGNR interconnects, all the impedance parameters are critically analyzed.

In **Chapter 5,** the influence of layers on performance of MLGNR interconnects is analyzed.

In **Chapter 6,** the performance of MLGNR interconnects for local, semi-global and global length of interconnects has been analyzed

In **chapter 7**, the impact of interlayer resistance on performance of MLGNR interconnects is analyzed for global lengths at 22nm technology node.
Finally, a conclusion and future scope of the thesis is given in **Chapter 8.**

CHAPTER

2

LITERATURE SURVEY

2.1 Introduction

With the advancement in technology, gate delays are decreasing and the interconnect delays are staying almost a constant [3]. To improve the overall performance of a digital circuit, it has become necessary to improve the interconnect performance. For the copper interconnects, resistivity is rising steeply with the dimensional scaling. Future VLSI interconnects, like graphene Nanoribbon (GNR) and carbon nanotude (CNT) can be considered as a potential candidate for copper replacement [1]. Based on their properties, both CNT and GNR show much better electrical and mechanical properties than copper.

Recently much progress has been made for GNR as VLSI interconnects. Conductance has been modeled by Azad Naeemi et al [7] and Chuan Xu et. al. [33] and are widely used by other Authors for performance Analysis. Vachan Kumar et. al. [5],[28] formed a 2D resistor network for accurate estimation of resistance for top contact MLGNR interconnects. Propagation delays of different types of MLGNR's has been analyzed and found that MLGNR can outperform copper if proper intercalation doping is considered [1],[9],[33]. Performance of MLGNR w.r.t copper improves for more advanced technology nodes for global and intermediate lengths [8]. For smaller widths, GNR makes 3-4 times lesser coupling capacitance than copper which can result in lesser power dissipation, propagation delay and crosstalk noise [7]. Effective resistance of MLGNR improves with the increase in the number of layers and higher number of layers result in lesser propagation delay [15]. It is also found that CNT's can outperform copper

at global and semiglobal lengths and is comparable to copper for local lengths of interconnect [11].

2.2 Conductance Analysis in GNR based Interconnects

Vachan Kumar et. al. developed analytical models for calculation of effective resistance for multilayer graphene Nanoribbon interconnects. They estimated the decrease in the effective resistance with the increase in the number of layers. They found that resistance is not linearly proportional to length and for short lengths, the resistive coupling between the layers is very small and hence higher number of layers is ineffective in reducing the overall resistance. They also suggested that optimum number of layers should be chosen to minimize the delay and energy delay product. As the number of layers increases the resistance decreases but the capacitance increases. They observed that with increase in length optimum number of layers increases due to increase in coupling between the layers with increase in length [5],[28].

Tamer Ragheb et. al. presented a comprehensive model of the resistance for Graphene Nanoribbon (GNR) interconnects. They used experimental and theoretical results to model the impact of stacking of graphene layers in multi-layer GNR interconnects and compared the resistance of GNR interconnects with both single-walled carbon nanotube (SWCNT) bundle interconnects and conventional copper interconnects. Their simulation results demonstrate the performance superiority of multi-layer GNR interconnects over conventional copper interconnects at small widths (< 15 nm) [6].

Azad Naeemi et. al. presented compact physical models for conductance of GNR's as function of chirality, width, Fermi level, and the type of electron scatterings at the edges. Conductance of copper and monolayer single wall nanotube (SWNT) are compared with semiconducting and metallic GNR's for different Fermi energies at unity aspect ratios. They found that the resistance of metallic GNR is smaller than copper and higher than monolayer SWNT for smaller widths less than 8 nm whereas resistance of semiconducting GNR's becomes more worse for widths less than 8 nm. The advantage with GNR's is that with small thickness it makes 3-4 times smaller mutual capacitance between adjacent interconnects than copper can result into smaller power dissipation, propagation delay, crosstalk noise and delay variation. Hence they concluded that for ultra-small thickness of GNR's can provide better performance than copper wires [7].

2.3 Interconnect Performance Analysis

Chuan Xu et. al. modeled conductance using tight binding model and linear response landauer formula and focused on the conductance and performance comparisons of GNR's with other interconnect materials. The impact of various model parameters like band gap, Fermi energy, mean free path, and edge specularity on conductance is also analyzed. Resistance of AsF_5 doped zigzag multilayer GNR with smoother edges is found smaller than copper for all widths for global length interconnects whereas neutral zigzag multilayer GNR is found higher for the same case for lengths above 20 nm. They concluded that both resistance and propagation delay of AsF_5 doped zigzag multilayer GNR with smoother edges is lower than copper and SWCNT for all lengths at 11 nm technology node for global length interconnects [33].

Yuan Fang et. al. analyzed the propagation delay for intermediate length and global length interconnects at 14 nm and 22 nm technology nodes. They found that p.u.l equivalent kinetic inductance decreases with increases with number of layers and p.u.l equivalent quantum capacitance initially increases and after a few number of layers becomes a constant. They reported that MLGNR interconnects can provide better performance than copper interconnects with similar geometries in the 14 nm and 22 nm technology nodes and it is more advantageous for more advanced technology nodes [8].

Kaustav Banerjee et al, analyzed conductance and delay of graphene nano-ribbon (GNR) interconnects. The results reveal that single layer GNR's cannot match the performance of global length copper or SWCNTs, unless multiple layers along with proper intercalation doping is used along with specular GNR edge is achieved. Multi-layer zigzag edged GNRs (zz- GNRs) can be comparable to copper at the local level, and can have much better performance than that of tungsten, thus with proper intercalation doping in multilayer zigzag GNR interconnects can be used as local interconnects [9].

Atul K. Nishad et al, proposed analytical time domain models for side contact and top contact multilayer graphene nanoribbon (MLGNR) interconnects. They have designed an optimum top contact MLGNR interconnect that exceeds the performance of Cu and optical interconnects. By various model parameters like interlayer conductance, Fermi energy and line geometry, they optimized the performance of top contact MLGNR interconnects to match with that of side

contact MLGNR interconnects. The use of optimized top contact MLGNR's gives better performance than copper interconnects and can eliminate the requirement of making side contacts [10].

Hong Li et al, reported that carbon nanomaterials are better than other emerging technologies as interconnects, vias (vertical interconnects), and off-chip interconnects. They reported that both CNT's and GNR's reduces interconnect delays and power dissipation by more than 50 percent. On comparison with optical and RF technology they found that the carbon nanomaterial is better in all domains and optical and RF technology is even not applicable for local interconnects and on-chip vias [1].

Hong Li et al, presented both electrical and thermal modeling of both GNR and CNT interconnects. They compared the performance of CNT and GNR with copper. They reported that Single wall CNT, Double wall CNT and Multiwall CNT can outperform copper in terms of delay for long global wires. For GNR to be comparable to copper or CNT intercalation doping with high edge specularity is required. Due to the presence of large kinetic inductance in a CNT bundle, skin effect reduces which makes it suitable for high frequency applications. Their simulation results reveal that CNT based capacitors could provide three times more capacitance density than ITRS requirement in 2022 [11].

Prashant Kumar et al, presented closed form models for calculating the transfer function of single-layer GNR interconnects. They also present the time domain analysis of the single layer GNR interconnects to analyze propagation delay, energy and energy delay product. They observed that delay decreases with the increase in width. They analyzed the effect of quantum capacitance on propagation delay and energy and concluded that for larger widths quantum capacitance can be eliminated to make the calculations easy [12].

Azad Naeemi et al, introduced physics based circuit models for armchair and zigzag graphene nanoribbons (GNRs) and their conductance are compared with copper and CNT. They also observed that for widths larger than 4 nm, semiconducting GNR's have conductance equal to or sometimes higher than metallic. The need for chirality control can be eliminated for interconnect applications. GNR's with smooth edges can potentially outperform copper wires for widths less than 8 nm. The use of higher Fermi energies reduces the resistance due to more populated

conduction channels and larger mean free paths [13].

M.S. Sarto et al, proposed multiconductor transmission line model of multilayer graphene Nanoribbon interconnects (MLGNR) for current distribution and signal propagation at high frequency upto 100 GHz. They compared the performance of MLGNR and MWCNT interconnect. They observed that MLGNR interconnect has better current carrying capability than MWCNT interconnect with width of 10 nm and unity aspect ratios. They also observed that accuracy of ESC model is up to few tens of gigahertz for a length up to 50 μm [14].

Manoj Kumar Majumder et al, analyzed propagation delay as a function of width for MLGNR and compared with that of single layer GNR (SLGNR) interconnects. They compared the delays for different number of layers using driver interconnect load system with CMOS inverter as driver. They found that MLGNR interconnects with 20 number of layers performs better than SLGNR interconnects with a delay performance improvement of 94.5 percent. They observed that delay improves with increase in the number of layers due to the reduction of equivalent resistance with increase in number of layers [15].

Debaprasad Das et al, analyzed the crosstalk effects in graphene Nanoribbon interconnects at 16 nm technology node. They used the equivalent circuit model to calculate the circuit parameters for the crosstalk analysis. They compared the simulated results with copper and multiwall CNT interconnects and found that near end noise of GNR interconnects is found greater than copper and MWCNT and the far end noise was found lesser than copper and greater than MWCNT interconnects. They also observed that GNR interconnects has two orders of magnitude less failure in time than copper interconnects due to less overshoot/undershoot peak and width [16].

Jiang-Peng Cui et al, implemented the equivalent single conductor model for the signal transmission analysis for on-chip multilayer graphene Nanoribbon interconnects. They analyzed the output voltage waveforms of the driver interconnect load system at 22 nm and technology nodes for unity aspect ratio and different interconnect lengths and Fermi energies. The delay of the output improves with increase in Fermi energy and decrease in length. With the help of partial differential equations, crosstalk between the edge coupled multilayer GNR's has been

analyzed for different 14 nm and 22 nm technology nodes [17].

Shaloo Rakheja et al, presented the physical models of electron transport parameters such as mean free path, diffusion coefficient, mobility and p.u.l resistance for bulk and graphene Nanoribbons as a function of interconnect dimensions, edge roughness and Fermi energy. In their analysis, their have considered the finite interlayer resistivity between the layers. They analyzed the delay of MLGNR interconnects and compared with copper and found that MLGNR interconnects perform better than copper at 9.5 nm technology node. They also observed that MLGNR interconnects with optimum number of layers perform better than copper as the decrease in resistance exist only for a few number of layers [3].

Manoj Kumar Majumder, et al. analyzed propagation delay, power dissipation and power-delay product for different number of layers in MLGNR by using the equivalent RLC model for MLGNR interconnects. They used the driver interconnect load system where CMOS inverter is used as driver at 32 nm technology node. They observed that propagation delay decreases and power dissipation increases with increase in the number of layers. The optimum numbers of layers are calculated by obtaining the minimum power delay product. In their analysis, the optimum number of layers is found to be 15. They Approximate number of layers have been calculated for optimized delay and power performances at global interconnect lengths depending on their simulation results [18].

Pawan Kapur et al. modeled resistivity of copper interconnects for the future technologies. Due to the impact of surface scattering and diffusion barrier effect on resistivity of copper interconnects are found to increase with dimensional scaling. They further compared the resistance of copper with aluminium interconnects at 35 nm technology node. They found that p.u.l increase in resistance of 192%, 145% and 90% for local, semi-global and global lengths respectively. The limitation in this analysis is that they have not considered the effect of electron scattering through grain boundaries [19].

Raghunath Murali et al. fabricated the graphene Nanoribbon and the resistivity associated to it was compared with that of copper interconnects. They found that the average resistivity of GNR is three times higher than copper interconnects for narrow widths (18 nm to 52 nm). The best GNR has the resistivity similar to copper. They concluded that the moderate quality GNR's can

perform better than copper interconnects. They also observed that the resistivity decreases with the increase in width [20].

Naushad Alam et al. compared the transmission lines parameters of mixed CNT bundles with that of copper interconnects at 32 nm technology node. They found that equivalent resistance and capacitance of mixed CNT bundles are smaller than copper interconnects for semiglobal and global length interconnects and resistance of mixed CNT bundles is higher whereas capacitance was found comparable to copper for local length interconnects. They observed that the impedance parameters can be modulated by varying the tube diameters and the density of the tubes in the bundle [21].

H B Bakoglu, et al. developed a model for interconnection time delay that included the effects of scaling transistor, interconnection and chip dimensions. The delays of aluminum, WSi2, and polysilicon lines were compared. As the chip dimension increases, the minimum feature size decreases, R_{int} becomes important and delay rises rapidly. So, the major challenges were to minimize the capacitances and resistances to reduce the delay. So, two approaches to shortening the delay were to reduce the interconnection resistance by using only aluminum lines for long-distance communication and by forming multilayer of interconnections with thicker and wider lines in the upper levels and the second was to improve the driver circuit through cascaded drivers that increase in size until the last device was large enough to drive the line or by using repeaters that divide the interconnections into smaller subsections [22].

M.K Rai and S.Sarkar reported the effect of tube diameter on delay and power dissipation on CNT bundle interconnect performance and also reveal that the effect of resistance in deep submicron region for both CNT and Copper. It was concluded that resistance of Cu interconnect increases with decrease in technology due to electron migration and grain boundary effect, where as in CNT resistance increases marginally with lower technology [23], [24].

Sandeep Sharma, et al. evaluated the performance **f**or different types of carbon-nanotubes (CNTs) like Single-walled carbon nanotubes (SWCNT), Bundle SWCNT (B-SWCNT), Multiwalled CNT (MWCNT) and Copper interconnects. They showed that under the most practical conditions only the MWCNTs can give better performance in terms of delay than Copper and all other types of CNT based interconnects at local, intermediate and global

interconnect levels. The MWCNTs are easier to fabricate with less concern about chirality and density control can thus act as an replacement for traditional Copper interconnects at local, intermediate and global interconnect levels. They also found that under the most practical conditions the SWCNTs can give the best performance in terms of power. Both the SWCNT and MWCNT outperforms the copper interconnects in terms of average power dissipation at local, intermediate and global interconnect levels [25].

Ning Wang, et al. compared copper and aluminum with Graphene Nanoribbon (GNR) interconnects in sub 50 nm technology using the existing models for all materials in order to understand the physical size effects that occur when the electron mean free path becomes comparable to the IC dimensions. Using the best publicly available data and calibrating these existing models , they found that, depending on their structure, either Al or GNRs could hold advantages over Cu at line widths lesser than 10 nm [26].

Mayank Kumar Rai et al. reported that SWCNT-bundle interconnects have lower delay than copper interconnect due to its low resistance and low inductance. Interconnect delay of single-walled carbon nanotube (SWCNT) bundle was analyzed with the help different tube diameters. Delay increases with increase in tube diameter of SWCNT. They suggested that it desirable to restrict tube diameter to the minimum possible for reducing the delay [27].

CHAPTER

3

VLSI Interconnect

3.1 Introduction

The performance of an interconnect is dependent on the impedance parameters. Accurate estimation of each impedance parameters (Resistance, Inductance and Capacitance) is must in determining actual power dissipation and propagation delay. All these parasitic impedance parameters are dependent on its structural dimensions and its surrounding environment. In this chapter, initially structure of interconnect and its dimensions are explained. From the different types R,L, and C associated to it and equivalent R,L and C can be calculated based on the geometry of interconnect. Furthermore, the impact of scaling on interconnection parameters have been explained and trend of various parameters can be estimated with time. This trend differs for both local and global length interconnect. Various Repeater insertion methods have been discussed and its impact on performance has been briefly explained.

3.2 Interconnects

Interconnects serve as the streets and highways of the integrated circuit (IC) that make electrical connections between the components in the IC. Basic components in the IC include the transistors and interconnect. As the design rule shrink below 0.25 μm, interconnects have become important and cannot be ignored. The interconnect mostly used today are aluminium and copper. Depending on length interconnects can classified as local, semi-global and global interconnects and are briefly discussed in chapter 1. In the deep submicron technology, both die size and device density of the VLSI circuit increases [29]. The increase in die size and device density makes the length of the interconnect longer in VLSI circuits. With the increase in the

length of the interconnect, propagation delays also increase and the performance of the interconnect degrade. Hence, the propagation delay and the power dissipation increases of the whole circuit in the submicron technology.

3.3 Problem in existing interconnect materials

Previously, the choice of the material suitable for interconnects was based on its conductivity and adherence on silicon dioxide. As the device density increased with technology scaling, interconnect current density also increased [30]. With the increased current density the previously used interconnect aluminum faced electromigration problem. Later copper which can withstand 5 times more current density and which is more resistant to electromigration problem is started being used. As the technology advances, copper started facing the problem of increase in resistivity due to surface roughness and grain boundary scattering causing problem of increase in propagation delay, power dissipation and electromigration. The following are the problems faced by copper interconnects:

• It diffuses very fast in both oxide and Si.

• It is readily oxidized in air at low temperature (<2000C) and forms no self protective layer to stop further oxidation and erosion.

• **Grain boundary effect**: A grain boundary is the interface between two grains, or crystallites, in a polycrystalline material. Grain boundaries are defects in the crystal structure, and tend to decrease the electrical and thermal conductivity of the material. In copper volume fraction of atoms lying at the grain boundaries are more as compared with conventional coarse-grained polycrystalline materials [31].

• **Electromigration**: Electro migration is caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. It can cause the eventual loss of connections or failure of a circuit. The electro migration resistivity of copper is high. Due to continuing scaling of very large scale integrated (VLSI) circuits, thin-film metallic conductors or interconnects are subject to increasingly high current densities. Under these conditions, electro migration can lead to the electrical failure of

interconnects [31].

• **Surface scattering**: Surface scattering arises when the electron interacts from the surface and the path of electron flow deviates from the path obtained when it interacts with the ideal interface. As the dimension reduces the number of collisions from the interface increases and the surface scattering increases. Surface scatterings can be diffusive as well as elastic. An empirical parameter P which ranges between 0 and 1 shows the fraction of electrons which suffer elastic collisions at the surface. Resistivity of copper does not change when value of P is 1 and it is completely elastic type of scattering and Resistivity of copper changes when value of P is 0 and it is completely diffusive type of scattering [32]. The mobility decreases when it is diffusive scattering and remains constant for elastic scattering. The better the quality of surface, higher the value of P and lesser will be the impact on its resistivity. Fig1.3 shows the electron surface scattering for both diffusive and elastic scattering.

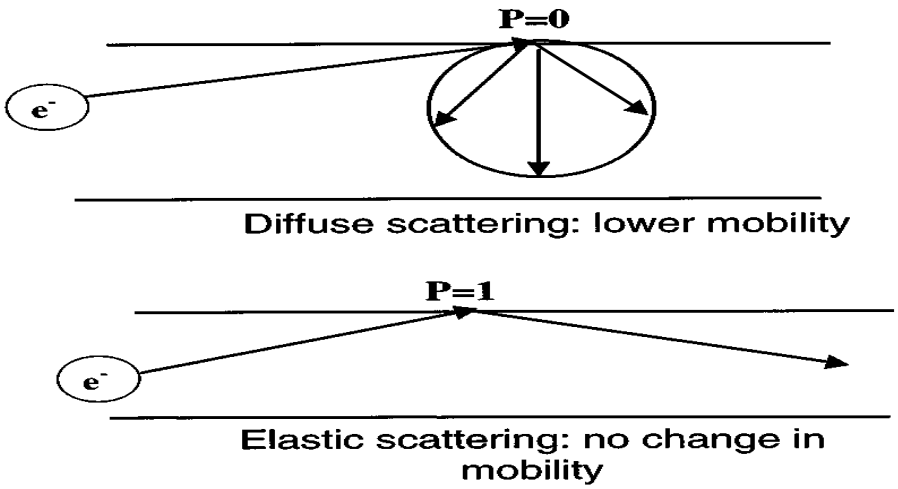

Fig. 3.1 Schematic showing electron surface scattering and the parameter P, used to characterize the interface quality [32].

With the decreasing dimensions, the problems mentioned above greatly affect the resistivity to increase steeply. Consequently resistance increases of the presently used Copper and Aluminium interconnects. Hence the performance of interconnects with low dimensions is degrading. To remove this problem the research on different materials which are suitable for interconnect in low dimensions has been started. The most promising one found was with the carbon based nano materials that are CNT (carbon nano tube) and GNR (graphene nano ribbon) [33].

3.4 Types of Interconnect

With continuous reduction of feature size there has been a parallel increase in die size. The result is more and more increase in length of some of the on chip interconnects as technology scaling continues. Based on their length interconnects are categorized as local, semi-global and global [30].

- **Local Interconnect**: Local interconnects is the first, or lowest, level of interconnects. They usually connect gates, sources and drains in MOS technology, and emitters, bases, and collectors in bipolar technology. Local interconnects can afford to have higher resistivity's than global interconnects since they do not travel very long distances.
- **Semi global Interconnect**: Used to connect device within a block. Interconnects of intermediate lengths are the semi global ones.
- **Global Interconnec**t: Used to connect long interconnects between the blocks, including power, ground and clocks. They often travel over large distances, between different devices and different parts of the circuit, and therefore are always low resistant metals. A global interconnect is very long which is connected to several nodes across the chip for example, clock lines, ground lines etc [30].

3.5 Future VLSI Interconnects

1. Carbon Nanotubes (CNT): Single wall CNT (SWCNT) and Multi wall CNT (MWCNT) are considered promising candidate for deep submicron interconnect applications due to their superior conductivity and current carrying capability [34].

SWCNT: Single wall carbon nanotubes consist of one graphene shell with diameter in the range of nanometer [34].

MWCNT: These are multi wall carbon nanotubes consisting of several graphene shells with diameter in the range of few to hundreds of nanometer. It can be fabricated using CMOS-compatible processes and its performance show significant improvement over copper. In the MWCNT's conductance is determined by number of conduction channels per shell and the number of shells. For interconnect applications metallic interconnects are useful [34].

CNT BUNDLES: They are large number of electrically parallel isolated CNT's to form a bundle. Thus by parallel connection there is considerable reduction of resistance [34]. In a CNT bundle, some CNT's are metallic while others are semiconducting. MWCNT's are mostly metallic, while the SWCNT's are semiconducting by a large fraction.

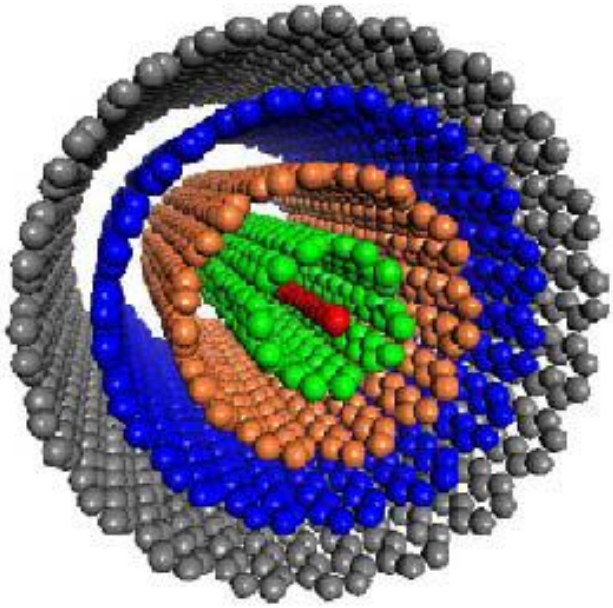

Fig. 3.2 Multiwall CNT [34].

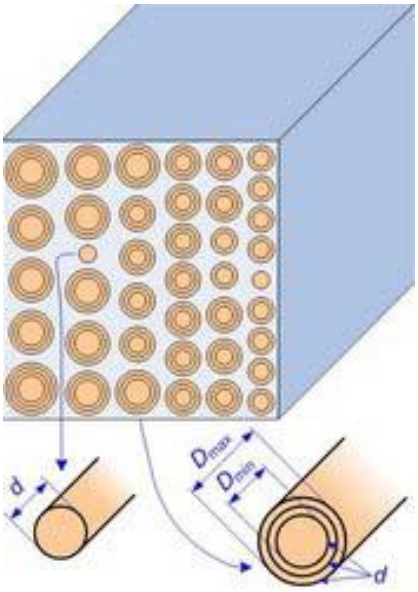

Fig. 3.3 Mixed CNT Bundle [34].

2. Graphene Nanoribbon (GNR): GNR is a strip of graphene with width in the order of few nanometers. Based on number of layers GNR's can be classified as Single layer GNR (SLGNR) and Multilayer layer GNR (MLGNR). From the technology point of view GNR is preferred due to its better controllability. High quality graphene sheets may have mean free path close to those of CNT's in the range of micro meter. Unlike CNT's whose chirality is random, there are ways to control the chirality of the graphene sheets. The major difference in the GNR and the CNT structure is the presence of the dangling bonds at the edges which are normally hydrogen terminated and have no major impact on the band structure of GNR [33]. Figs. 1.6 (a) and (b) shows the single layer GNR and multilayer GNR respectively. In the multilayer GNR, two or more number of layers are stacked in parallel to increase the conductance.

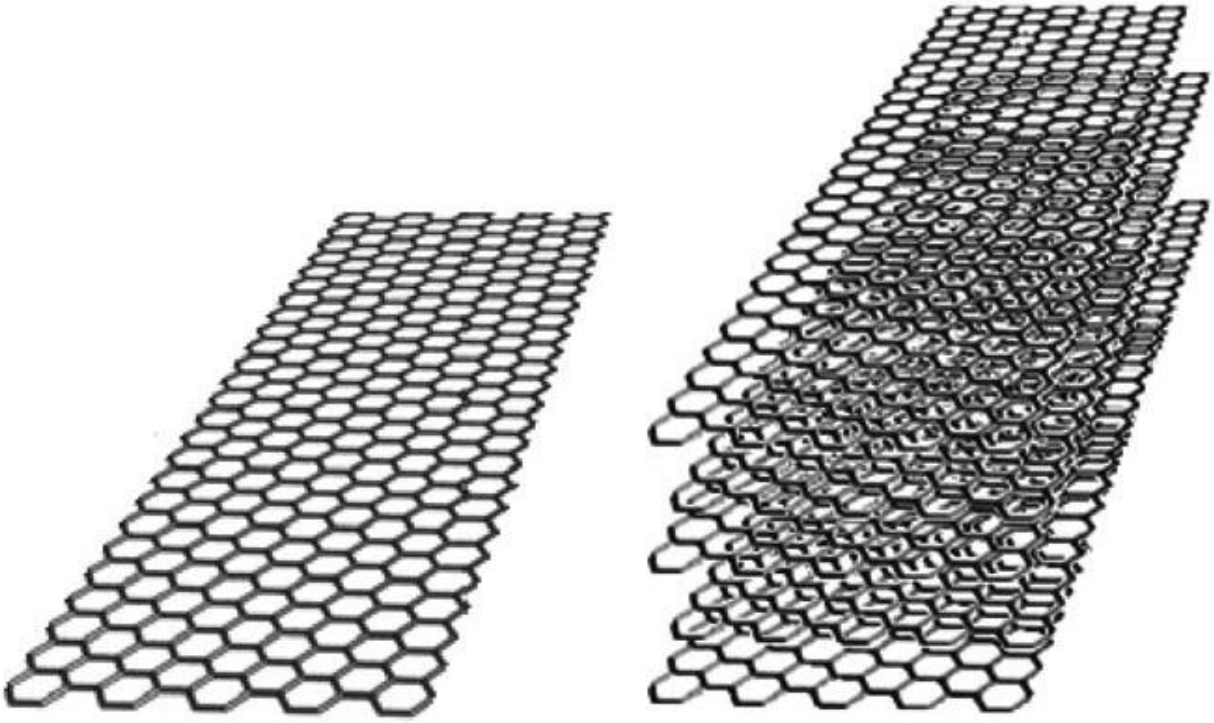

Fig 3.4 (a). Single layer GNR [33].

Fig. 3.4 (b). Multi layer GNR [33].

3. Optical interconnects: Optical interconnect is a way of communication by optical cables. Optical wires are capable of high bandwidth, from 10 Gbit/s up to 100 Gbit/s. Optical interconnects have negligible frequency dependent loss, low cross talk and high band width. Optical interconnects are not much used commercially since optical interconnects technology is incompatible with manufacturing processes and assembly methods that are currently used in the semiconductor industry [35].

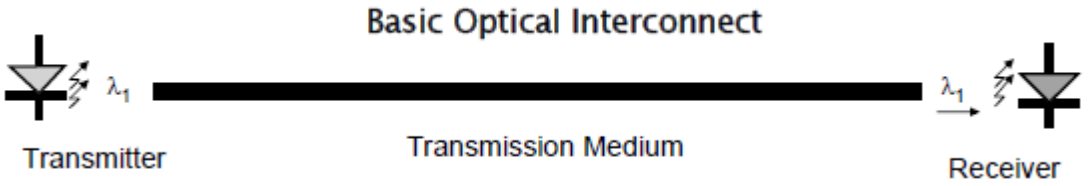

Fig. 3.5.Optical fiber interconnect [36].

Both GNRs and CNTs can conduct much larger current densities than Cu (a traditional interconnect material), due to their strong sp^2 hybridized bonds, and the absence of severe reliability problems that plague Cu, particularly for future interconnect geometries. The thermal conductivities of GNRs and CNTs are also much larger than that of Cu. Moreover, compared to

Cu, both GNRs and CNTs have large carrier mean free paths (MFPs), which lead to large electrical conductance. However, GNRs are believed to be more controllable from a fabrication point of view. This is due to the planar nature of graphene, which can be patterned using high-resolution lithography.

Properties	Copper	SWCNT	MWCNT	GNR
Maximum current density (A/cm2)	10^7	$>10^9$	$>10^9$	$>10^8$
Melting point (k)	1356	3773	3773	3773
Tensile strength(Gpa)	0.22	22.2	11-63	
Thermal conductivity(*103 W/mK	0.385	1.75-5.8	3	3-5
Mean Free Path(μm)	0.04	>1	25	1

Table 3.1. Properties Of Graphene/Gnrs, Cu, And Cnts Relevant To Vlsi Interconnect [33],[37]-[48].

The properties of GNRs, Cu, single-walled CNTs (SWCNTs), and multiwall CNTs (MWCNTs), relevant to interconnect applications, are listed in Table 1 [35],[37]-[48].

3.6 Structure of an interconnect.

Fig. 3.1 shoes the 3D view of interconnect with its cross-sectional dimensions. Here two interconnect lines are shown in parallel with width (w), Thickness (H), length (l), distance from ground plane (y) and spacing between the adjacent interconnects (s).

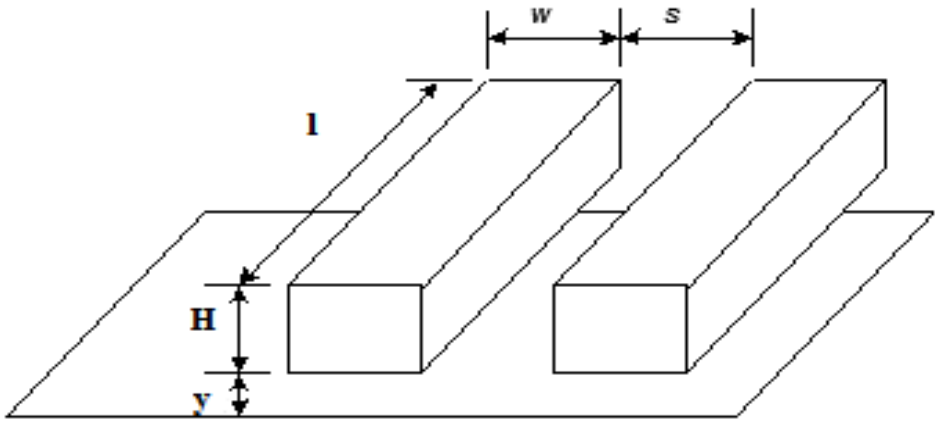

Fig. 3.6 3D view of the Interconnect.

3.7 Interconnect Parameters

Interconnect parameters are of three types -capacitive, Inductive and Resistive. These parameters affect reliability and performance of the interconnect. The increase in interconnect parasitic increases the power dissipation, propagation delay and energy consumption of the circuit. Hus degrade the performance of the circuit. They also produces noise which affect the reliability of the circuit. The evolution of interconnect and the RLC model of copper interconnect has been explained [49].

3.7.1 Interconnect capacitance

The interconnect capacitance depends on its geometry, environment and the distance of its neighboring wires. The interconnect capacitance is further classified as parallel plate capacitance, coupling capacitance and fringing capacitance. The parallel plate capacitance is the capacitance which appears between interconnect and ground plane. The coupling capacitance appears between the two interconnects. If these interconnects are on the same level then this coupling capacitance can be termed as intralevel coupling capacitance and if they appear between different levels then it is called interlevel coupling capacitance. The unwanted coupling between the neighbouring interconnects introduces an interference and are generally called crosstalk. Let us consider a single conductor model for capacitance calculation as shown in Fig.3.2(a). Here the equivalent capacitance (C_{wire}) of the wire will be the sum of parallel plate capacitance (C_{pp}) and fringing capacitance (C_{fringe}). A parallel plate capacitance is determined by

the orthogonal field between the interconnect of width (w) and the ground plane and the fringing capacitance is between the thickness (H) and the ground plane. In this model fringing capacitance is modeled as a cylindrical wire [49].

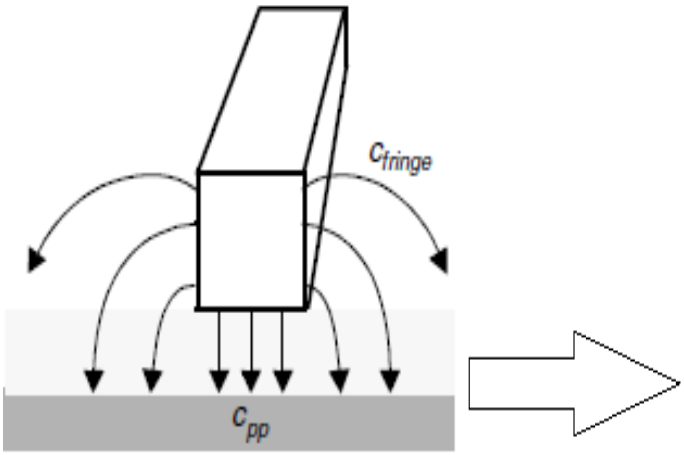

Fig. 3.7(a) Single conductor model for Capacitance calculation [49].

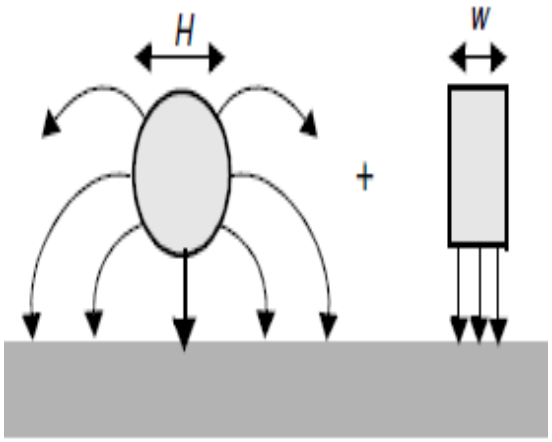

Fig. 3.7(b) Model decomposed into parallel plate components and fringing field components [49].

The following equations are used for the calculation of the wire capacitance (C_{wire}) [49].

$$C_{wire} = C_{pp} + C_{fringe} \quad (3.1)$$

$$C_{pp} = \frac{\varepsilon . w}{y} \quad (3.2)$$

$$C_{fringe} = \frac{2\pi\varepsilon}{\log\left(^{y}/_{H}\right)} \quad (3.3)$$

3.7.2 Interconnect Resistance

The resistance (R) of an interconnect is proportional to its length (L) and inversely proportional to its cross-sectional area (A). The resistance (R) of a rectangular interconnect can be expressed as [49]

$$R = \frac{\rho . L}{A} \quad (3.4)$$

Where ρ is the resistivity of the interconnect material in ohm meter (Ω.m), and A is the cross-sectional area in meter square (m^2).

$$R = \frac{\rho . L}{H . w} \qquad (3.5)$$

The area of the cross-section A is the product of interconnect thickness (H) and width (w) as shown in the Fig.3.3.

The Aspect ratio (AR) is the ratio of interconnect thickness and width. The width of the interconnect is dependent on the minimum dimensions and technology being used. From the equation (3.5), we can say that resistance is inversely proportional to its cross-sectional dimensions, interconnect thickness and width.

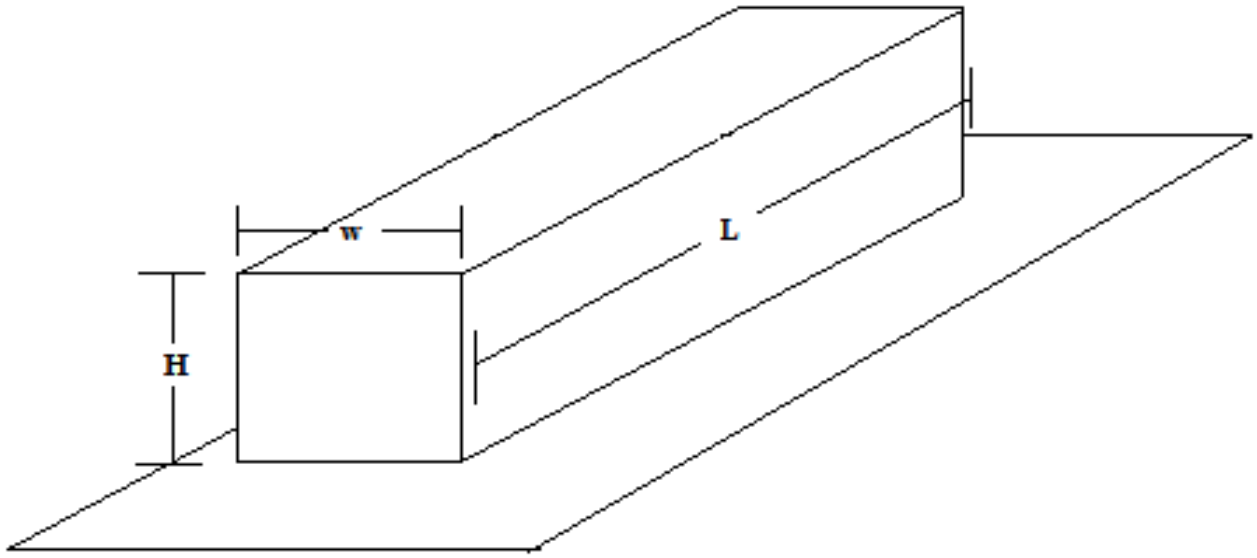

Fig.3.8 Rectangular interconnect with dimensions (H,w,L) for resistance calculation.

S.No.	Materials	Resistivity(μΩ.cm)
1	Copper (Cu)	1.7
2	Aluminum (Al)	2.7
3	Tungsten (W)	5.5

Table 3.2. Commonly used materials for interconnect and their resistivity at 20° C [49].

Resistivity of interconnects increases with the increase in temperature and scaling. Resistivity of the commonly used materials as interconnect are shown in Table 3.1 [49].

3.7.3 Interconnect Inductance

In most of the previously used models inductance was not considered. At very high frequencies in the GHz range, the inductance cannot be ignored. This impedance due to inductance increases with increase in frequency. Materials with less resistance are now adopted for interconnect applications has also promoted researchers to include inductance in the transmission line models for interconnects. The inductance of a section of the circuit can always be calculated as [49]

$$\Delta V = L\frac{di}{dt} \tag{3.6}$$

Where L is the inductance, ΔV is the voltage drop generated by the inductor, i is current and di/dt is the change in current.

Inductance can also be calculated directly from its geometry and its environment as the per unit length (p.u.l) capacitance (C) and the p.u.l inductance (L) are related by the following expression.

$$C.L = \varepsilon.\mu \tag{3.7}$$

Where Ɛ is the permittivity and μ is permeability of the surrounding material. The equation (3.7) is valid for conductors surrounded by uniform dielectric medium. Usually the conductor is surrounded by different dielectric materials. In that case, average value of permittivity and permeability can be chosen to get the approximate results.

3.8 Scaling of interconnects.

With the scaling of gate dimensions, the interconnect dimensions are also reduced. For the ideal constant field scaling, when the interconnect dimensions like interconnect thickness (H), width (w), distance between the interconnects (S), distance from the ground plane (y) and length (L) are scaled with a scaling factor (S) for local length interconnects, result in a change in impedance parameters. The resistance is proportional to length and inversely proportional to thickness and width of the interconnect and thus after scaling the resistance (R) increases by scaling factor S.
The capacitance (C) is proportional to length and width and inversely proportional to the

distance from the ground plane and thus after scaling the capacitance (C) reduces scaling reduces by scaling factor S. The RC delay for this case remains unchanged and the current density increases with a factor S after scaling [2],[49].

S.No	Interconnection parameter	Scaling factor (S)
1	Interconnect dimensions (H,w,S,y,L)	1/S
2	Line resistance	S
3	Line capacitance	1/S
4	RC Delay	1
5	Current density	S

Table: 3.3 Constant field scaling for local interconnects[49]

Based on the lengths interconnects are differentiated as local and global interconnects with scaling factor (S) greater than unity for local and scaling factor (S_c) less than unity for global interconnects. The impact of scaling on interconnect dimensions for global length interconnects has been listed in Table: 3.3. The RC delay increases with increase in length and scaling of interconnect dimensions due steep rise in resistance for scaled long interconnects. When compared to the RC delays of local and global interconnects, RC delays associated with local wires remains constant but the RC delays for global length interconnect increases with scaling [2],[49].

In contrast to the gate delays, the delays with interconnects increases or remains constant whereas gate delays reduces with the increasing years. This again shows that interconnect delays are a big reason to worry for future interconnects. This led to increasing search for new materials which can be the replacement of the presently used interconnects.

S.No	Interconnection parameter	Scaling
1	Interconnect dimensions (H,w,S,y)	1/S
2	Long interconnect length (L)	$1/S_c$
3	Line resistance	S^2/S_c
4	Line capacitance	$1/S_c$
5	RC Delay	S^2/S_c^2

Table: 3.4 Constant field scaling for global interconnects [49].

3.9 Repeater insertion

The repeaters are inserted to reduce the propagation delay and improve the performance of the interconnect. Repeaters are usually used to drive high impedance interconnects. For longer lengths, the resistive component is on a higher side and repeaters are inserted after short lengths of the total length of interconnect. To propagate the signal over a long line, repeater insertion is a commonly used technique to reduce the propagation delay. With the increase in length, propagation delay increases as quadratic function of length. The propagation delay decreases initially with the insertion of repeaters and after a number of repeaters delay starts increasing. So the optimum number of repeaters should be inserted to get the minimum delay and best performance [50]-[52]. The proper insertion of repeaters also reduces the power dissipation by reducing the short circuit current. CMOS inverter is commonly used as repeater. The sizing of the NMOS and PMOS is very important in designing a repeater. The minimum sized repeater has unity aspect ratio of NMOS and three times the size of NMOS is used for PMOS [53].The resistance of the repeater decreases with the increase in aspect ratios of NMOS and PMOS in a CMOS whereas capacitance increases with the increase in aspect ratios of NMOS and PMOS in a CMOS. To get the best performance both resistance and capacitance should be minimum. So optimized aspect ratio of the driver should be chosen for an interconnect. There are various methods for driving an interconnect and are shown in the Fig. 3.4 [54].

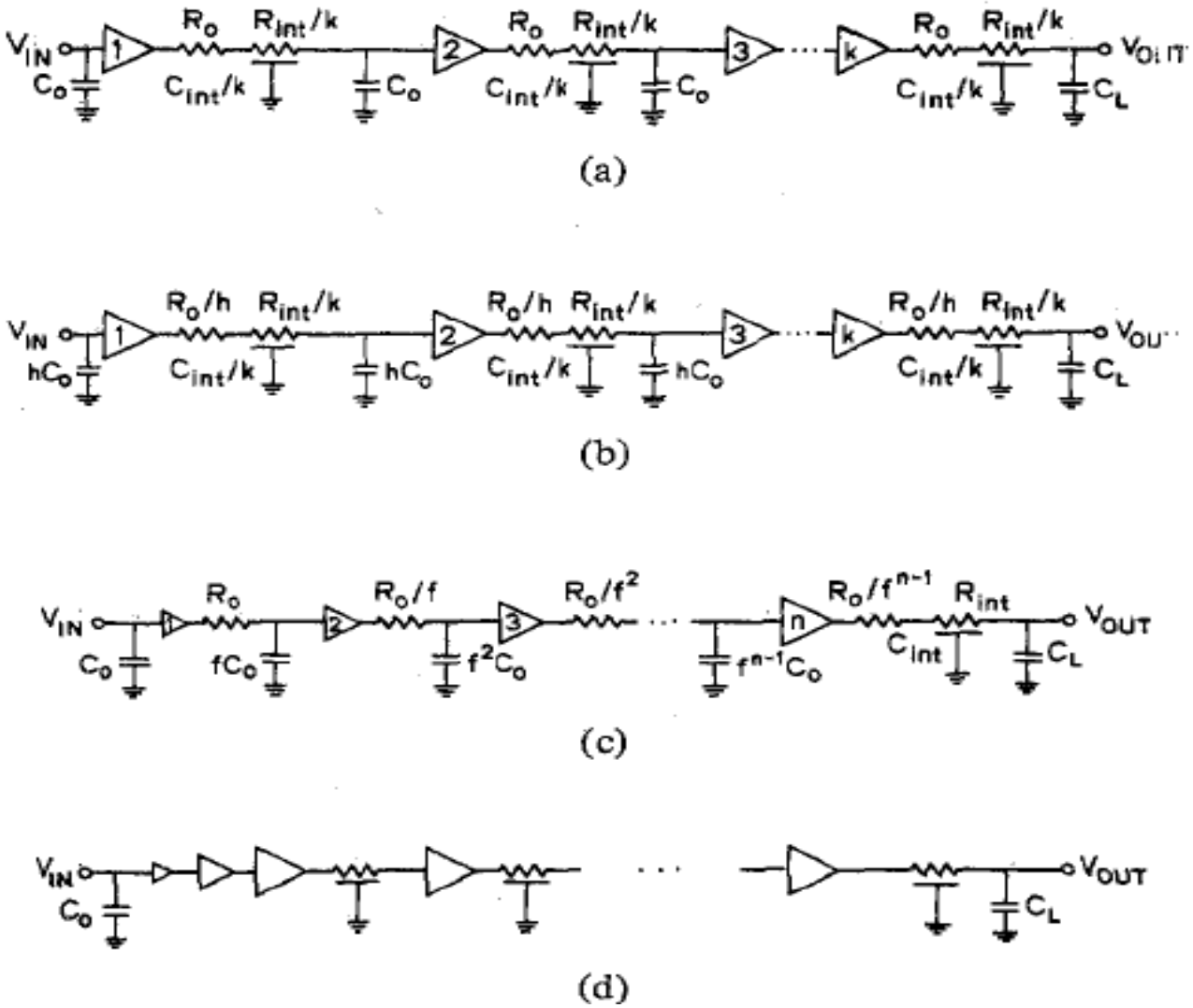

Fig. 3.9 (a) Minimum size repeaters. (b) Optimal repeaters. (c) Cascaded drivers. (d) Optimal. repeaters with a cascaded first stage[54].

3.10 Copper interconnects

For many years, Aluminium (Al) was used as the material for interconnect and silicon dioxide (SiO_2) as the dielectric between the interconnect and the ground plane. Due to rapid scaling, the gap between the interconnect and the gate delays is increasing. The interconnect is badly affected by resistive and capacitive parameters. The limitations with aluminium technology are higher RC delay, lesser reliability, more power dissipation, crosstalk noise and cost. The aluminium was lesser reliable than because it is more prone electromigration. The resistivity of aluminium is 2 to 3 times higher than copper which result in higher RC delay. Due to Higher impedance parameters in aluminium, power dissipation is also on the higher side. Due to the above

limitations of aluminium, another material copper has started being used for interconnect applications.

The resistance of copper was found to be much lower than aluminium. It was found that copper is much better than aluminium in terms of reliability. Hence the propagation delay associated to copper interconnects also is lesser. Low K dielectric has started being used. Due to the lower dielectric constant, capacitance decreased. Due to the combined effect of lower resistance and capacitance power dissipation also decreased. The impact of lower capacitance has been observed on lesser crosstalk noise. Thus it was concluded that copper is the most suitable material for aluminium replacement.

In the deep submicron technology, copper interconnects started facing many challenges. The resistivity was rising steeply due to combined effect of electromigration, grain boundary effect, surface scattering and highly resistive diffusion barrier. The problems associated to copper have been discussed briefly in chapter 1. These problems in copper limit the performance of copper interconnects. The ultimate solution found was its replacement. Last few years, the research for new materials suitable for interconnect applications are being explored and most of the researchers has focused on carbon nanomaterials. The comparison of new materials with copper on different domains has been started. For the comparison purpose the similar models are chosen with copper and other emerging interconnect material [55].

3.11 Geometry of copper interconnects

There are two commonly used geometries for calculation of impedance parameters of any interconnect technology. One is for the global lengths and another is for local and intermediate length interconnects. Coupling lines are above one metal ground for global lengths and coupling lines are between two metal ground planes. The geometries are shown in Fig 3.5(a) and (b).

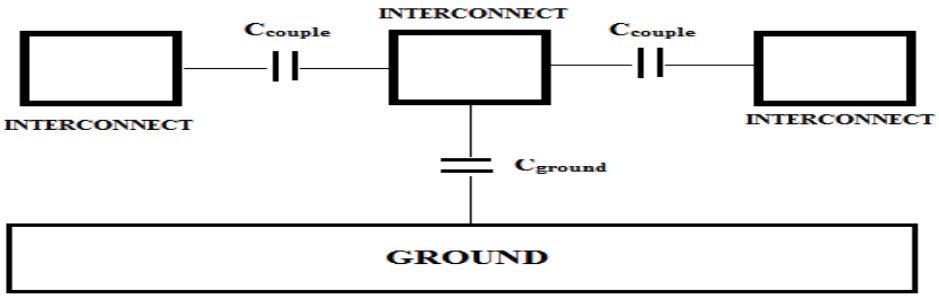

Fig 3.10 (a) Geometry of global length interconnects[53]

Three interconnects are assumed for global wires,. The impedance parameters are calculated for the interconnect between the two other interconnects. The interconnect in the center couple with the other two with a coupling capacitance (C_{couple}). The capacitance made by the interterconnect from a distance t above the ground plane is C_{ground}. In the structure of local and intermediate wires, three interconnects are considered. Here also the impedance parameters are calculated for the interconnect between the two other interconnects. The interconnect in the center couple with the other two with a coupling capacitance (C_{couple}). In this structure, interconnects are placed between the two ground planes. The capacitance made by the interterconnect with the ground plane is assumed to be C_{ground} [7].

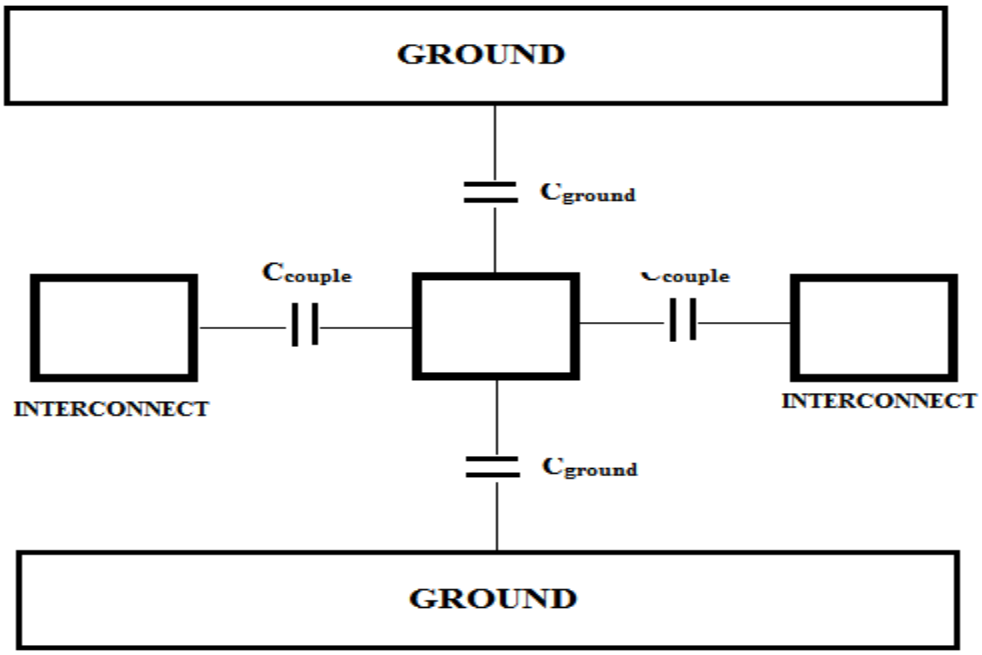

Fig 3.10 (b) Geometry of local and intermediate length interconnects[53]

3.12 Impedanance calculations of copper interconnect.

The winbond TSM model is used for calculations of equivalent resistance, inductance and capacitance of copper interconnects [56]. In this model, interconnect width, interconnect thickness ,distance from the ground plane and spacing between the interconnects are assumed to be w, t, h, and S respectively. The spacing between the adjacent interconnect (S) is assumed to be equal to interconnect width (w) [53].

The equivalent resistance (R_{eq}), equivalent inductance (L_{eq}) and equivalent capacitance (C_{eq}) are obtained from the following expressions. Fig 3.6 shows an equivalent circuit model for

copper interconnect. It contains a CMOS driver, input, output and the equivalent impedance parameters.

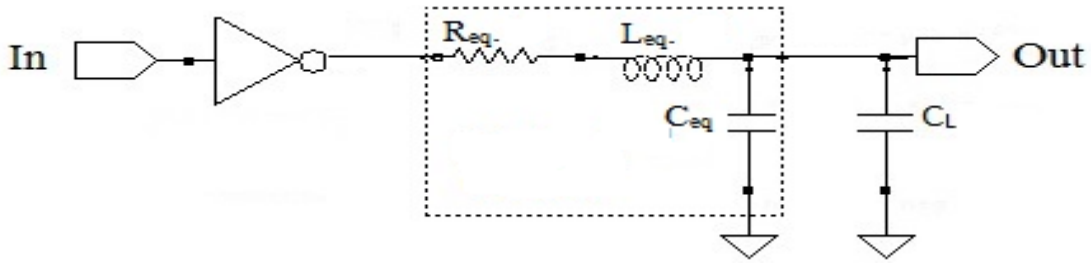

Fig. 3.11 Equivalent Circuit model of copper interconnect

3.12.1 Equivalent resistance

The resistance of the copper interconnect is proportional to length and inversely proportional to the interconnect width (w) and thickness (t). The resistivity is denoted by ρ and it increases with technological scaling. The resistance increases with increase in resistivity (ρ). The expression used for resistance calculation is [53]

$$R_{eq} = \frac{\rho . l}{w . t} \tag{3.8}$$

3.12.2 Equivalent inductance

The inductance is expressed as

$$L_s = \frac{\mu_0 . l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + 0.22\frac{(w+t)}{l}\right] \tag{3.9}$$

Mutual inductance (M) can be expressed as

$$M = \frac{\mu_0 . l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \tag{3.10}$$

μ_0 is the permeability of the free space and d is the center-to-center distance between two wires.

3.12.3 Equivalent capacitance

There are two component of capacitance (C_g and C_c) to calculate the equivalent capacitance for the copper interconnect. C_g is the capacitance with ground plane. The capacitance of the copper

interconnect for local and intermediate interconnects can be expressed as

$$C_g = \varepsilon\left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77}.\left(\frac{t}{t+4.53h}\right)^{0.07}\right] \quad (3.11)$$

Coupling capacitance (C_c) can be formulated as

$$C_c = \varepsilon\left[1.41\frac{t}{s}e^{\frac{-4s}{(s+8.01h)}} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28}.\left(\frac{h}{h+8.96s}\right)^{0.76}.e^{\frac{-2s}{(s+6h)}}\right] \quad (3.12)$$

The equivalent capacitance of the copper interconnect can be expressed as

$$C_{eq} = 2C_g + 2C_c \quad (3.13)$$

The capacitance of the copper interconnect for global interconnects can be expressed as

$$C_g = \varepsilon\left[\frac{w}{h} + 2.22\left(\frac{s}{s+0.70h}\right)^{3.19} + 1.17\left(\frac{s}{s+1.51h}\right)^{0.76}.\left(\frac{t}{t+4.53h}\right)^{0.12}\right] \quad (3.14)$$

Coupling capacitance (C_c) can be formulated as

$$C_c = \varepsilon\left[1.14\left(\frac{h}{h+2.06s}\right)^{0.09} + 0.74\left(\frac{w}{w+1.59s}\right)^{1.14} + 1.16\left(\frac{w}{w+1.87s}\right)^{0.16}.\left(\frac{h}{h+0.98s}\right)^{1.18}\right] \quad (3.15)$$

The equivalent capacitance of the copper interconnect can be expressed as

$$C_{eq} = C_g + 2C_c \quad (3.16)$$

Where ε is the permittivity of the medium and is the product of the permittivity of free space (ε_0) and the relative permittivity of medium (ε_r).

3.13 Conclusions

In the modern VLSI technology, the accurate estimation of impedance parameters is important. Based on the structure of interconnect and its environment, impedance parameters are calculated. The effect of Scaling on different interconnect parameters and the role of repeaters for improving

the interconnect performance has been discussed. Finally, the equivalent RLC model of copper interconnects for local, semi-global and global lengths has been presented.

CHAPTER

4 GNR as VLSI Interconnect

4.1 Introduction

Graphene Nanoribbon (GNR) is one of the emerging interconnect for the next generation interconnect technologies. Metallic GNR's are suitable for interconnect applications. An equivalent RLC model for single layer and multilayer GNR is presented. Due to higher resistance of Single layer GNR (SLGNR), Multilayer GNR is preferred. In this chapter, complete impedance analysis has been carried out for Multi-layer graphene Nanoribbon (MLGNR) interconnect at 22nm technology node. Similar analysis is carried out for copper interconnect and results are compared with MLGNR for local, semi-global and global interconnects. MLGNR interconnect resistance and inductance increases with decrease in Fermi energy and increase in length. On the other hand, interconnect capacitance is almost independent of Fermi energy and increases with increase in interconnect length. Impedance parameters is also analyzed as a function of width and found that resistance and inductance decreases with increase in width and capacitance increases with increase in width.

4.2 GNR interconnects

Graphene is a flat mono-layer of carbon atoms tightly packed into a two dimensional (2D) honeycomb lattice, and is a basic building block of graphite, Carbon Nanotubes (CNT), Graphene Nanoribbons (GNR), etc [9].

Graphene Nanoribbon (GNR) has been recently proposed as one of the potential candidates for both transistors and interconnects. GNRs can be either semiconducting or metallic, depending on the geometry, similar to the carbon nanotubes (CNTs). Compared to Cu,

a traditional interconnect material, both GNRs and CNTs have large carrier mean free path (MFP), and they can also conduct much larger current densities. Compared to CNTs, GNRs are believed to be more controllable from a fabrication point of view [33].

However, several issues also exist in GNRs. Firstly, GNRs have edge scattering, which reduces the effective MFP, while CNTs have no such issue. Secondly, while mono-layer graphene has large MFP and conductivity, multi-layer graphene turns to graphite and has much lower conductivity per layer due to inter-sheet electron hopping [11].

GNRs can be classified into two types on the basis of the shape of their edges viz. Armchair GNR and Zigzag GNR as shown Fig. 4.1(a) and (b) respectively. Armchair GNR show metallic properties, if the number of carbon rings along its width is 3p+2, and becomes semiconducting if the number of carbon rings along its width are 3p and 3p+1 where P is an integer. Zigzag GNR's are predominately metallic [11]. The metallic GNR has applications for nanoscale interconnects.

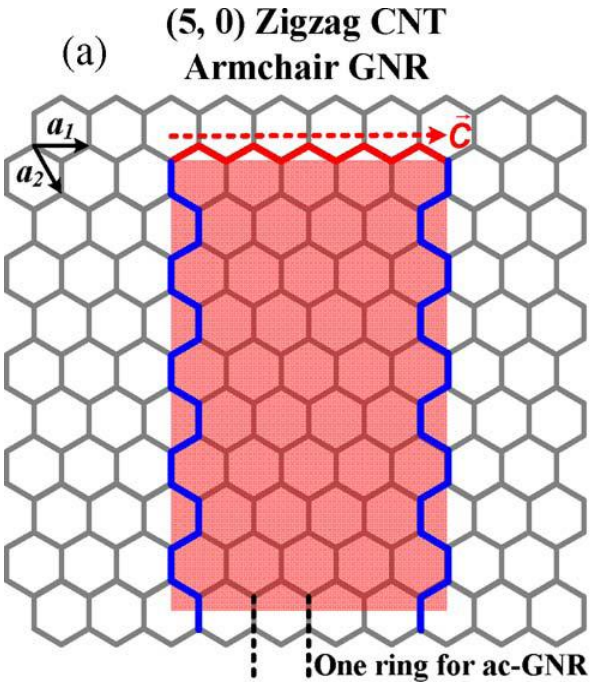

Fig.4.1(a). Armchair GNR [30].

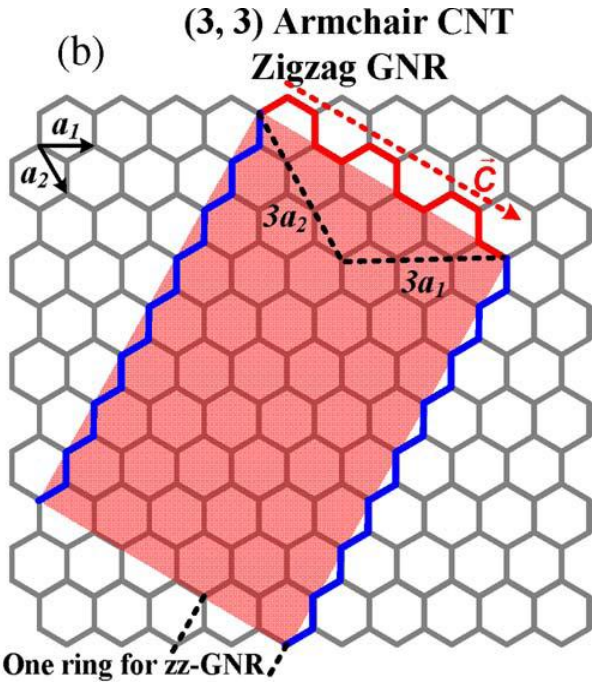

Fig.4.1(b). Zigzag GNR [30].

The dashed arrows in Fig. 4.1 (a) and (b) shows the circumferential vector C which shows the direction of a roll-up CNT. The circumferential vector is defined as

$$C = n \cdot \hat{a}1 + m \cdot \hat{a}2 \quad (4.1),$$

where â1 and â2 are the lattice vectors of graphene, and n and m are the chiral indexes. As such, the chiral indexes (n,m) uniquely define the chirality [11].

Both CNT and GNR can support large current densities and has long mean free paths [33]. However, it is difficult to control the chirality of CNT's [9] whereas in GNR's due to its planar nature chirality can be controlled using high resolution lithography [33]. The GNR's having one layer is called single layer GNR. Due to the large intrinsic resistance associated with single layer GNR, a multi-layer GNR (MLGNR) is proposed for nanointerconnects. Additionally, the conductance of GNRs can be modulated by doping.

4.3 RLC Model of Single-Layer Graphene Nanoribbon (SLGNR) Interconnect.

Fig.4.2(a). shows the geometry of single layer GNR and Fig.4.2(b) shows its equivalent RLC model. Here w is the width, y is the thickness of the substrate and ε_r is the dielectric constant.

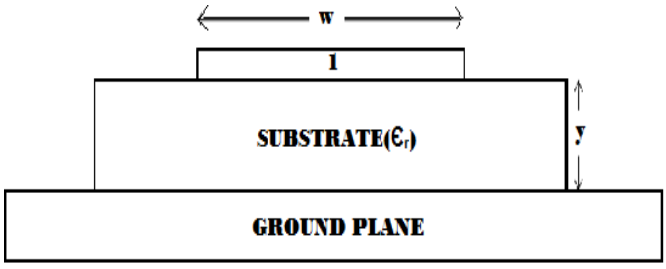

Fig. 4.2(a). Geometry of single layer GNR.

dl is the differential length, R_{mc} is the metal to GNR layer contact resistance, R_q is the quantum contact resistance and R_s, L_k, L_k, C_q and C_e are its scattering impedance parameters along its differential length.

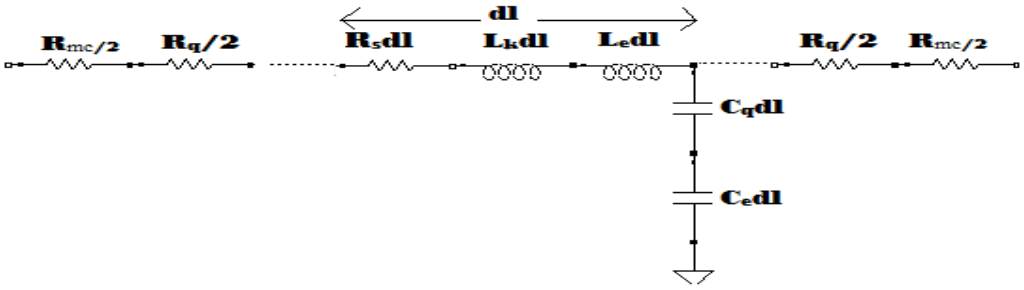

Fig. 4.2(b). RLC model of single layer GNR.

4.3.1 Conductance of GNR interconnect.

Using the linear response Landauer formula, the conductance of GNR can be formulated as [9]

$$G_n = \frac{2e^2}{h} . N_{ch} . t_{eff} \qquad (4.2),$$

where G_n is the conductance, e is the charge, N_{ch} is the number of effective number of allowed channels for transport, t_{eff} is the effective transmission coefficient. Zigzag-GNRs (zz-GNR) are always metallic and Armchair GNR (ac-GNR) can be either metallic or semiconducting, depending on the number of hexagonal carbon rings across the width (W).

The transmission coefficient (t_{eff}) is determined by both edge scattering and scattering by defects and phonons. The edge scattering is schematically shown in Fig. 5, where cot θ is the ratio of longitudinal (along the wire length) to transverse (across the wire width) velocities, and θ can be calculated from $|\sin \theta| = E_n/E$. If complete diffusive edge is assumed, transmission coefficient (t) due to edge scattering can be expressed by "w cot θ/L" where w cot θ is the average distance that electrons/holes travel before hitting the edge, and L is the length of the GNR [11].

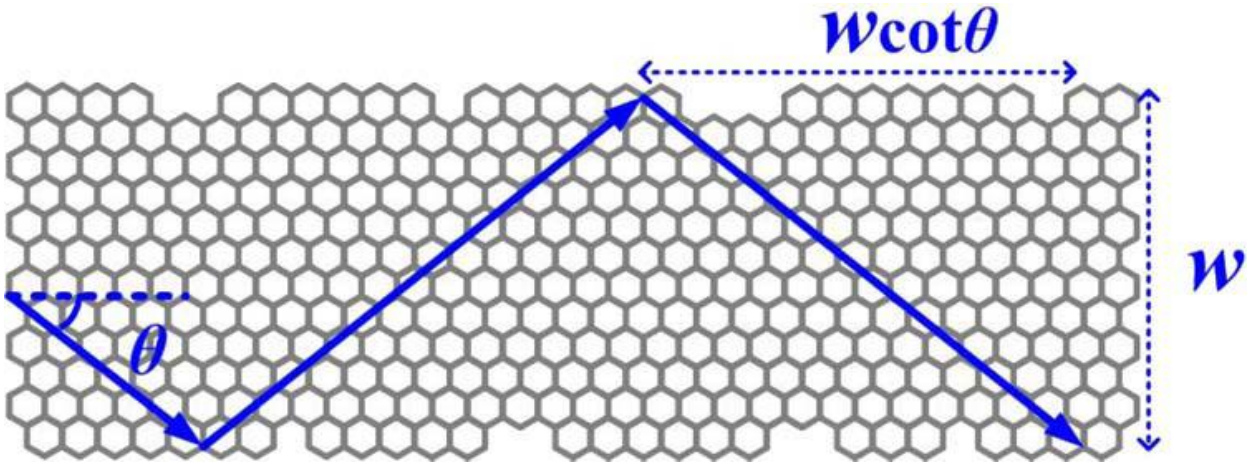

Fig. 4.3. Schematic view of edge scattering in GNRs and the definition of θ [11].

The width of the GNR is w and w cot θ is the average distance that electrons/holes travel before hitting the edge. Note that L/(w cot θ) and $L/(\lambda_{gnr} \cos \theta)$ represent the number of scattering effects due to edge scattering and defect scattering, respectively. λ_{gnr} is defined along the electron/hole transport direction (indicated by the solid arrows).

The mean free path (MFP), λ_{gnr} plays an important role in determining the conductance. Moreover, the fixed model for mono-layer GNRs is not consistent with the width-dependent l_D model for CNTs, due to the similar nature of GNRs and CNTs. The MFP of mono-layer GNR is approximately proportional to their width [11], just like the MFP of CNTs is a function of their diameter. Due to scatterings by defects and phonons (not edge scattering), the transmission coefficient can be expressed by "λ_{gnr} cos θ/L," where λ_{gnr} is the MFP corresponding to such scattering. λ_{gnr} cos θ represents the average distance that electrons/holes travel along the GNR longitude direction before collision [57].

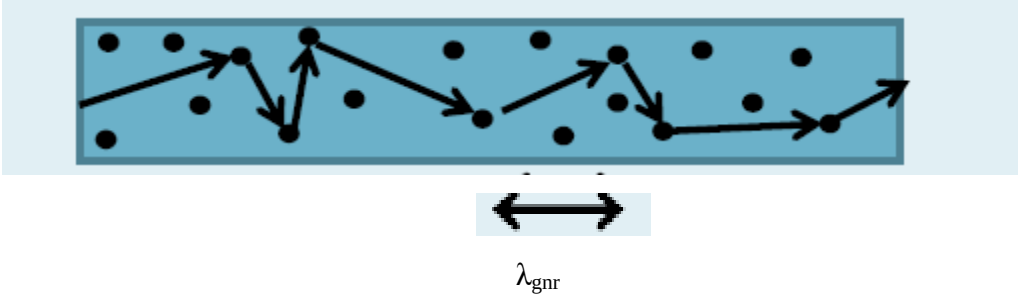

Fig. 4.4. mean free path [57].

Hence, if complete diffusive edge is assumed, using the Matthiessen's rule, transmission coefficient (t_{eff}) can be expressed as

$$t_{eff} = (1 + \frac{L}{\lambda_{gnr}.\cos\theta} + \frac{L}{w.\cot\theta})^{-1} \quad (4.3)$$

If the edge specularity is considered, the second term in equation (4.3) is modified, and the effective transmission coefficient (t_{eff}) can be formulated as [11]

$$t_{eff} = (1 + \frac{L}{\lambda_{gnr}.\cos\theta} + \frac{(1-p).L}{w.\cot\theta})^{-1} \quad (4.4)$$

N_{ch} is the number of conducting channels (modes) in one layer and is given by [10]

$$N_{ch} = \sum_{i=1}^{N_c}[1 + e^{(E_i - E_F)/KT}]^{-1} + \sum_{i=1}^{N_v}[1 + e^{(E_i + E_F)/kT}]^{-1} \quad (4.5),$$

where i is the positive integer, E_F is the Fermi energy, k is the Boltzmann constant, T is the temperature, N_c is the density of states of electrons and N_v is the density of states of holes.

$$E_i = \frac{h\vartheta_F i}{2w} \quad (4.6),$$

where E_i represents the quantized energy that corresponds to the i^{th} conduction or valence subband. The number of conduction channels increases linearly for metallic armchair GNR's which is approximated as [58]

$$N_{ch} \cong KE_F \cong \alpha w E_F \text{ (for } E_F \geq 0.1eV \,\&\, w > 10nm) \quad (4.7)$$

4.3.2 Inductance of GNR interconnect.

Kinetic inductance (L_k): GNR has kinetic inductance (L_k) in addition to magnetic inductance (L_e) as shown in Fig. 4.2(b). The kinetic inductance (L_k) is the kinetic energy stored in each conducting channel of the GNR and expressed as [36]

$$L_K = \frac{h/4e^2 v_F}{N_{ch}} \cong \frac{8nH}{N_{ch}}/\mu m \quad (4.8),$$

where v_F is the Fermi velocity. The magnetic inductance (L_e) can be calculated from the magnetic field of an isolated current carrying wire at a distance 'y' above the ground plane [10].

$$L_e = \frac{\mu_0 y}{w}\Big/\mu m \quad (4.9),$$

where μ_0 is the permeability of the free space and w is the width of GNR.

4.3.3 Capacitance of GNR interconnect.

The capacitance of GNR consists of quantum capacitance (C_q) and electrostatic capacitance (C_e). The quantum capacitance (C_q) per layer is given by [10]

$$C_q = \frac{4e^2/h \,.\, N_{ch}}{\vartheta_F} \cong N_{ch} 0.2fF/\mu m \quad (4.10)$$

The electrostatic capacitance (C_e) is calculated by using conformal mapping method with width 'w', placed at a distance 'y' above the ground plane [10].

$$C_E = \varepsilon . M\left[\tanh\left(\frac{\pi w}{4y}\right)\right] \tag{4.11}$$

$$M(a) = \begin{cases} \dfrac{2\pi}{\ln \dfrac{2.(1+\sqrt[4]{1-a^2})}{(1-\sqrt[4]{1-a^2})}}, & 0 \le a < \dfrac{1}{\sqrt{2}} \\ \dfrac{2}{\pi}\ln\dfrac{2(1+\sqrt{a})}{(1-\sqrt{a})}, & \dfrac{1}{\sqrt{2}} \le a \le 1 \end{cases} \tag{4.12}$$

where 'ε' is a permittivity of the medium and 'a' is the hyperbolic tangent of function of width 'w' and distance 'y' above the ground plane.

4.4 Equivalent RLC Model of Multilayer Graphene Nanoribbon Interconnect.

The geometry of MLGNR is shown in Fig.4.5, where H is the thickness, w is the width of the MLGNR, y is the distance from ground plane with ε_r as the dielectric constant of its medium, δ is the distance between the adjacent layers and N is the number of layers.

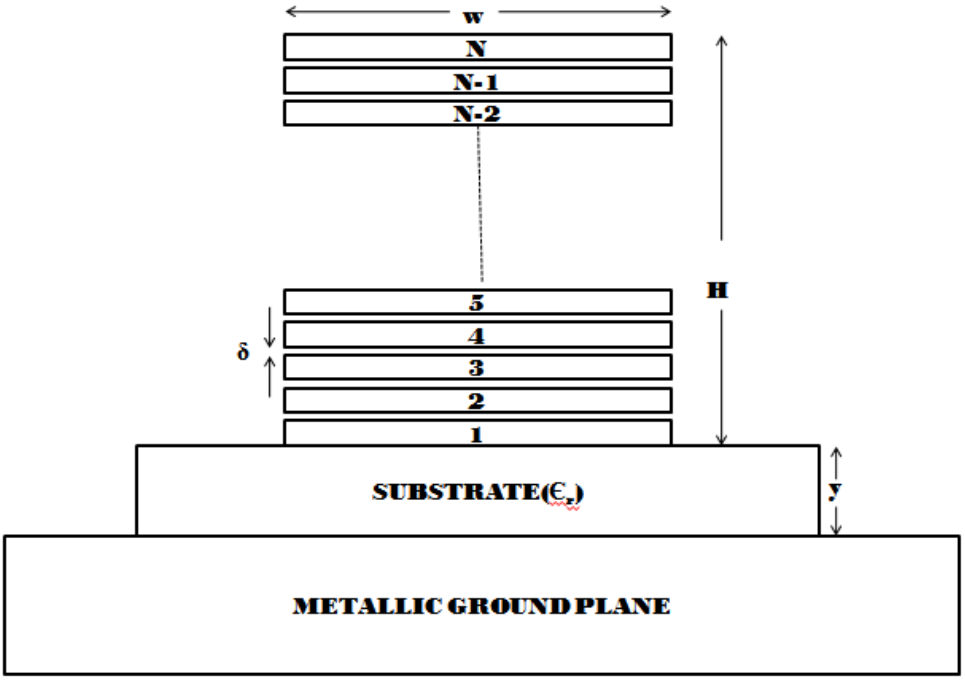

Fig.4.5. Geometry of MLGNR interconnect.

The number of layers depends on the geometry and can be formulated as [16]

$$N = 1 + \text{integer}\left[\frac{H}{\delta}\right] \quad (4.13),$$

where δ is the van der waal gap between the two layers and is numerically equal to 0.34 nm.

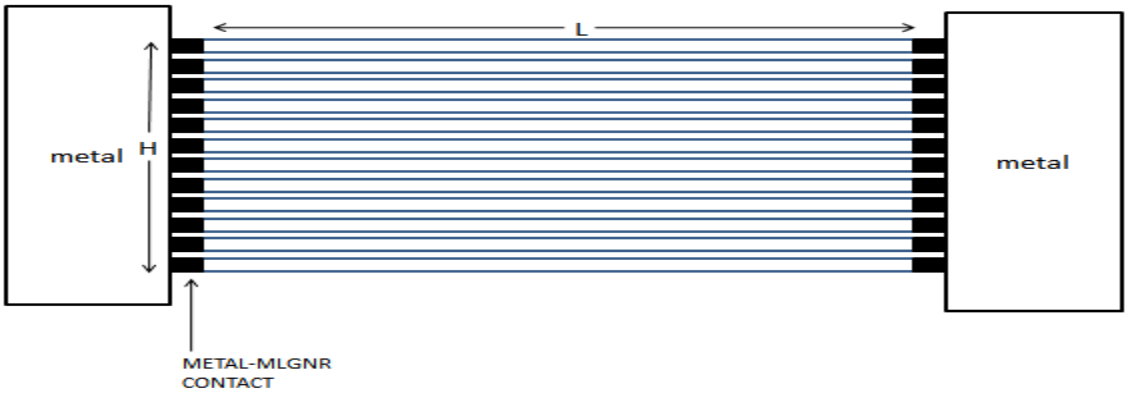

Fig.4.6. Longitudinal view of MLGNR interconnect.

Fig. 4.6 shows the longitudinal view of the MLGNR interconnect. The dimensions shown in the figure are thickness (H) and length (L) whereas the width gets hidden. Each layer of MLGNR interconnect is making metal to MLGNR contacts. These contacts obstructs the flow of electrons from the metal to MLGNR and vice versa. The contact resistance (R_{mc}) can vary from few hundred ohms to hundreds of kilo ohms depending on type of contacts and the technology being used. Its typical value is 20kΩ [17].

The RLC model of MLGNR interconnect is shown in Fig.4.7.

4.4.1 Resistance of MLGNR interconnect.

R_q is the quantum contact resistance and is defined as [10]

$$R_q = \frac{h/2e^2}{N_{ch}} = \frac{12.9k\Omega}{N_{ch}} \quad (4.14),$$

where N_{ch} is the number of conducting channels in each layer, *h* is the Plank's constant and *e* is the electronic charge. R_s is the scattering resistance along its length L and is given by [10]

$$R_s = \frac{R_q}{\lambda}\Big/\mu m \tag{4.15}$$

Hence, the total resistance of the multi-layer GNR is given by

$$R_{eq} = \frac{R_{mc} + R_q + R_s.L}{N} \tag{4.16}$$

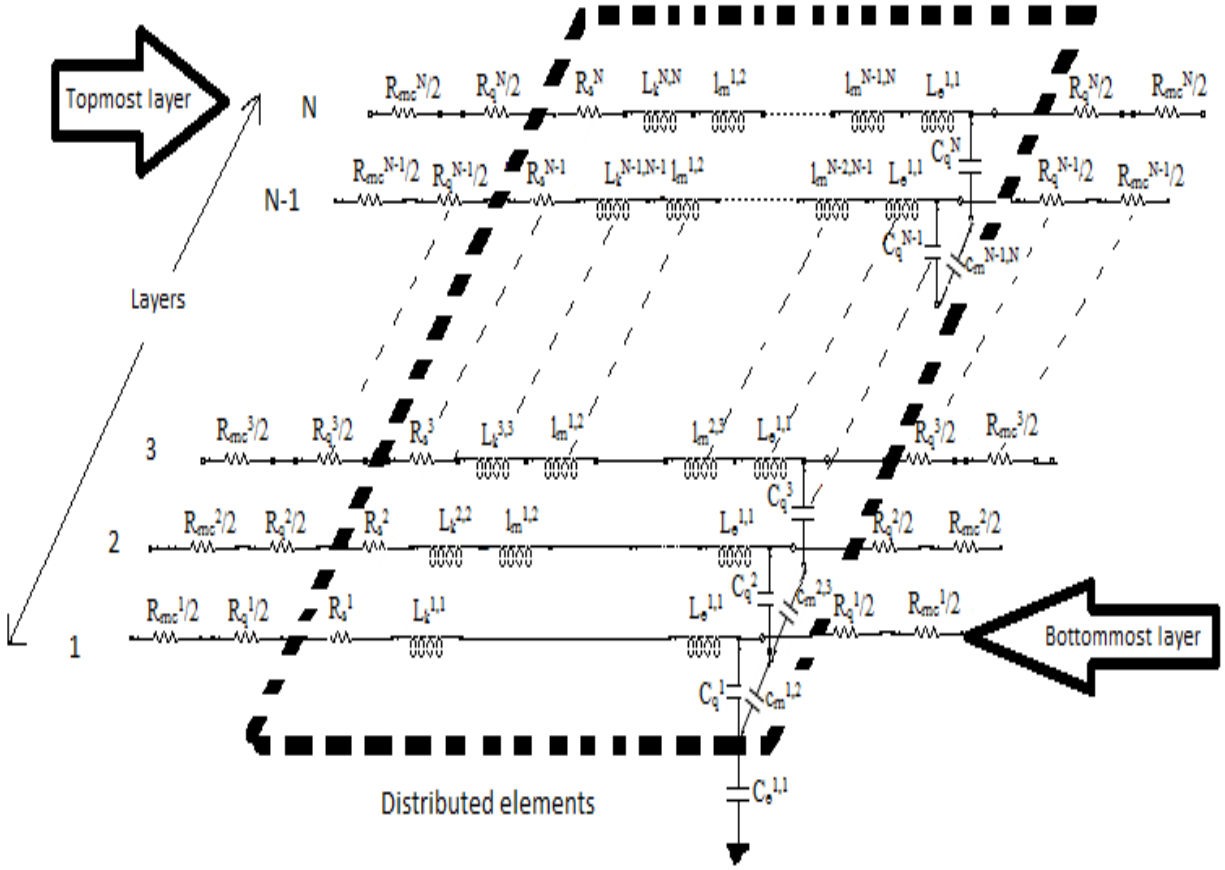

Fig.4.7. RLC Model for MLGNR interconnect.

4.4.2 Inductance of MLGNR interconnect.

GNR has kinetic inductance (L_k) in addition to magnetic inductance (L_e) as shown in Fig.4.7. The kinetic inductance (L_k) is the kinetic energy stored in each conducting channel of the GNR and expressed as [10]

$$L_K = \frac{h/4e^2\, v_F}{N_{ch}} \cong \frac{8nH}{N_{ch}}\Big/\mu m \tag{4.17},$$

where v_F is the Fermi velocity. The magnetic inductance (L_e) can be calculated from the magnetic field of an isolated current carrying wire at a distance 'y' above the ground plane [17].

$$L_e = {\frac{\mu_0 y}{w}}/{\mu m} \quad (4.18),$$

where μ_0 is the permeability of the free space and w is the width of GNR. For simplicity to calculate total inductance of MLGNR structure as shown in Fig.4.7, mutual inductance (l_m) is assumed to exist only between the adjacent layers and are equal for each pair of adjacent layers and is given by [8]

$$l_m = {\frac{\mu_{0\delta}}{w}}/{\mu m} \quad (4.19)$$

4.4.3 Capacitance of MLGNR interconnect.

The capacitance of GNR consists of quantum capacitance (C_q) and electrostatic capacitance (C_e). The quantum capacitance (C_q) per layer is given by [10]

$$C_q = \frac{4e^2/h \,.\, N_{ch}}{\vartheta_F} \cong {N_{ch} 0.2fF}/{\mu m} \quad (4.20)$$

The electrostatic capacitance (C_e) is calculated by using conformal mapping method with width 'w', placed at a distance 'y' above the ground plane [10].

$$C_E = \varepsilon\varepsilon . M\left[\tanh\left(\frac{\pi w}{4y}\right)\right] \quad (4.21)$$

$$M(a) = \begin{cases} \dfrac{2\pi}{ln\dfrac{2.(1+\sqrt[4]{1-a^2})}{(1-\sqrt[4]{1-a^2})}}, & 0 \le a < \dfrac{1}{\sqrt{2}} \\ \dfrac{2}{\pi}\ln\dfrac{2(1+\sqrt{a})}{(1-\sqrt{a})}, & \dfrac{1}{\sqrt{2}} \le a \le 1 \end{cases} \quad (4.22)$$

where 'ε' is a permittivity of the medium and 'a' is the hyperbolic tangent of function of width 'w' and distance 'y' above the ground plane. For simplicity to calculate total capacitance of

MLGNR structure as shown in Fig.4.7, mutual capacitance (c_m) is assumed to exist only between the adjacent layers and are equal for each pair of adjacent layers and is given by [8]

$$c_m = {}^{\varepsilon w}/_{\delta}{}_{\mu m} \tag{4.23}$$

4.5 Impedance as a function of length of MLGNR interconnect.

The per unit length (p.u.l) equivalent impedance parameters of MLGNR are calculated from Eqs.(4.13)-(4.23) as a function of Fermi energy. All the physical dimensions of MLGNR and copper are taken from [59],[60] and line parameters (R,L and C) of copper are calculated using appropriate expressions available in [53]. Mean free path (λ) is assumed to be 1μm for this analysis [33].

4.5.1 Resistance Analysis for Local, Semiglobal and Global lengths

Figs.4.8(a)-(c), illustrate a typical example of the dependence of MLGNR interconnect resistance on both length (L) and Fermi energy (Ef) for local, semi-global and global interconnects respectively. It shows that resistance increases with increase in interconnect length for both MLGNR and copper interconnects. Copper interconnects are of a higher resistance than MLGNR interconnects.

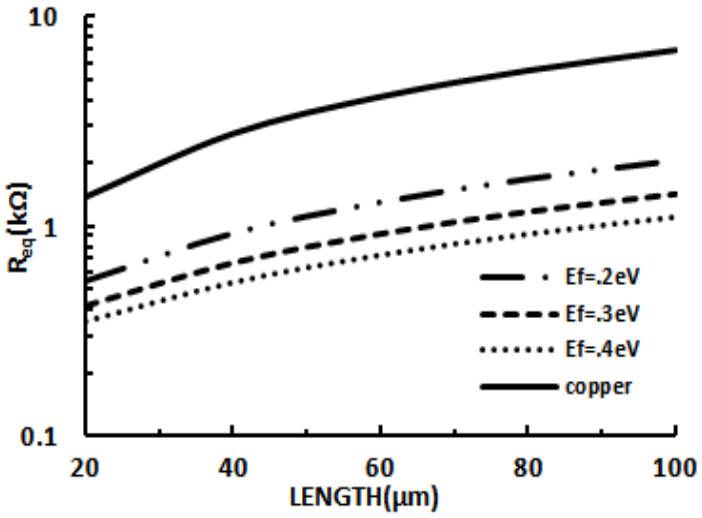

Fig.4.8(a). Equivalent resistance (R_{eq}) as a functionof Fermi energy (Ef) for local lengths of multilayer GNR interconnect.

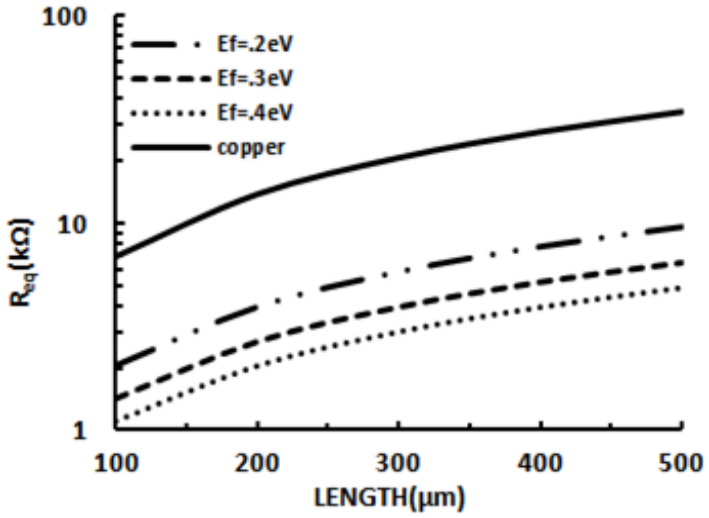

Fig.4.8(b). Equivalent resistance (R_{eq}) as a function of Fermi energy (Ef) for semi- global lengths of multilayer GNR interconnect.

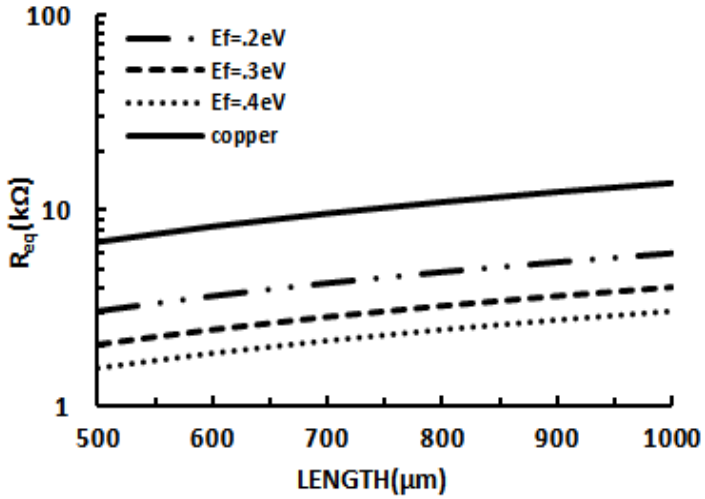

Fig.4.8(c). Equivalent resistance (R_{eq}) as a function of Fermi energy (Ef) for global lengths of multilayer GNR interconnect.

Resistance of MLGNR with smaller fermi energies (Ef) is observed more. Furthermore, the rate of increase in resistance with length for both copper and MLGNR interconnects for local and semi-global lengths (see Figs.4.8(a)-4.8(b)) is larger than global lengths (see Fig.4.8(c)).

4.5.2 Inductance Analysis for local, semiglobal and global lengths of MLGNR and copper interconnects

Figs.4.9(a)-(c) show the dependence of MLGNR interconnect inductance (L_{eq}) on both length (L) and Fermi energy (Ef). Due to the effect of inductive coupling between the adjacent layers,

Inductance (L_{eq}) in MLGNR interconnects is larger than its copper counterpart. The equivalent Inductance (L_{eq}) of MLGNR increases with increase in interconnect length and decrease in Fermi energy (Ef).

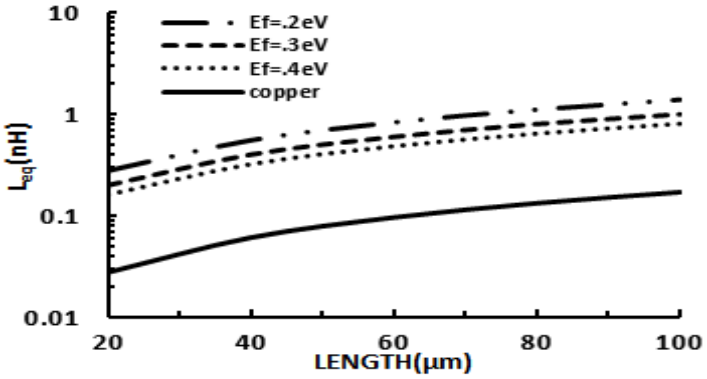

Fig.4.9(a). Equivalent inductance (L_{eq}) as a function of Fermi energy (Ef) for local lengths of multilayer GNR interconnect.

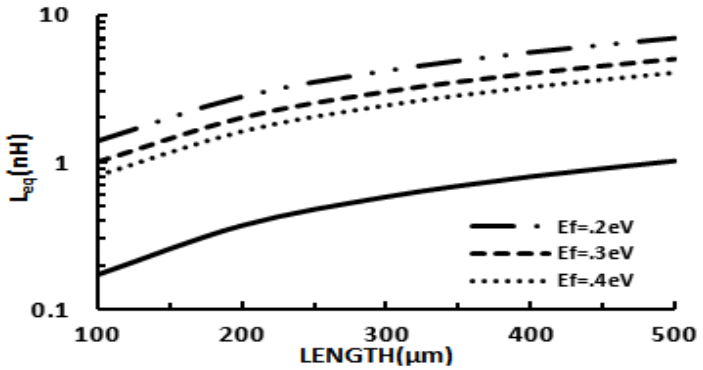

Fig.4.9(b). Equivalent inductance (L_{eq}) as a function of Fermi energy (Ef) for semi-global lengths of multilayer GNR interconnect.

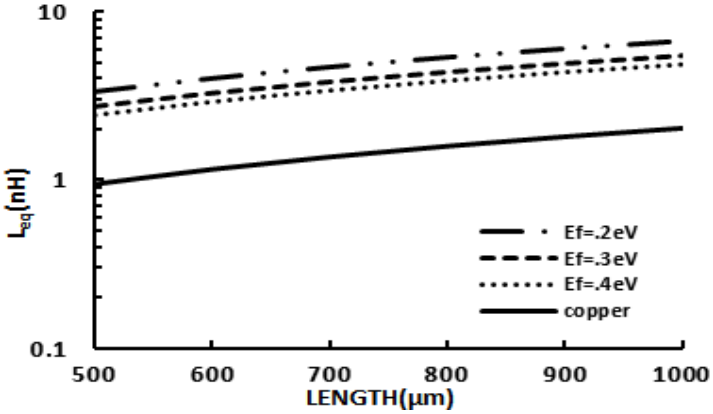

Fig.4.9(c). Equivalent inductance (L_{eq}) as a function of Fermi energy (Ef) for global lengths of multilayer GNR interconnect.

4.5.3 Capacitance Analysis for local, semiglobal and global lengths of MLGNR and copper interconnects

Figs.4.10(a)-(c) show the dependence of MLGNR interconnect quantum capacitance (C_q) on length and Fermi energy (Ef). The effect of capacitive coupling between the layers is included. The quantum capacitance (C_q) in MLGNR interconnects increases with increase in both length and Fermi energy (Ef).

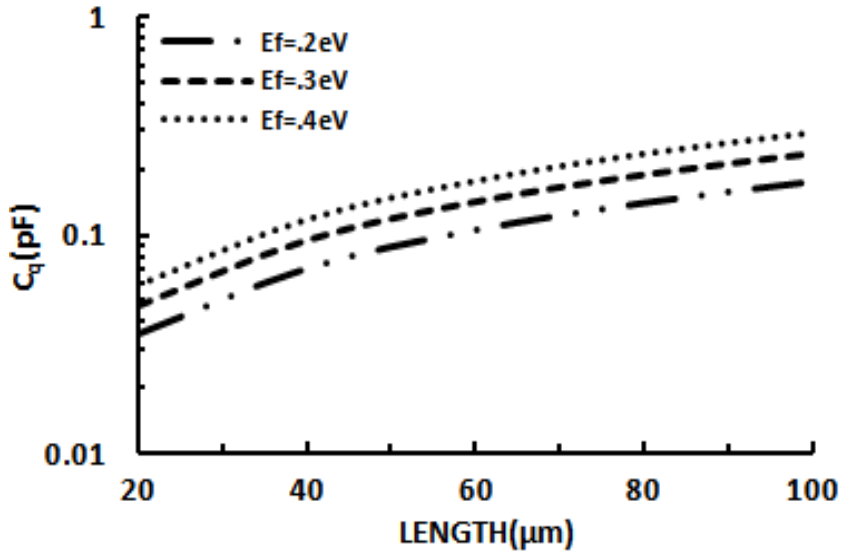

Fig.4.10(a). Equivalent Quantum capacitance (C_q) as a function of Fermi energy (Ef) for local lengths of multilayer GNR interconnect.

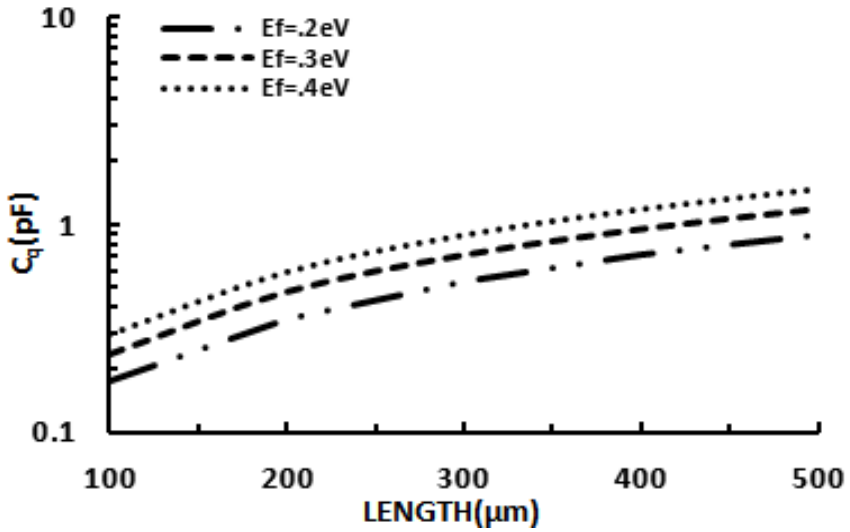

Fig.4.10(b). Equivalent Quantum capacitance (C_q) as a function of Fermi energy (Ef) for semi-global lengths of multilayer GNR interconnect.

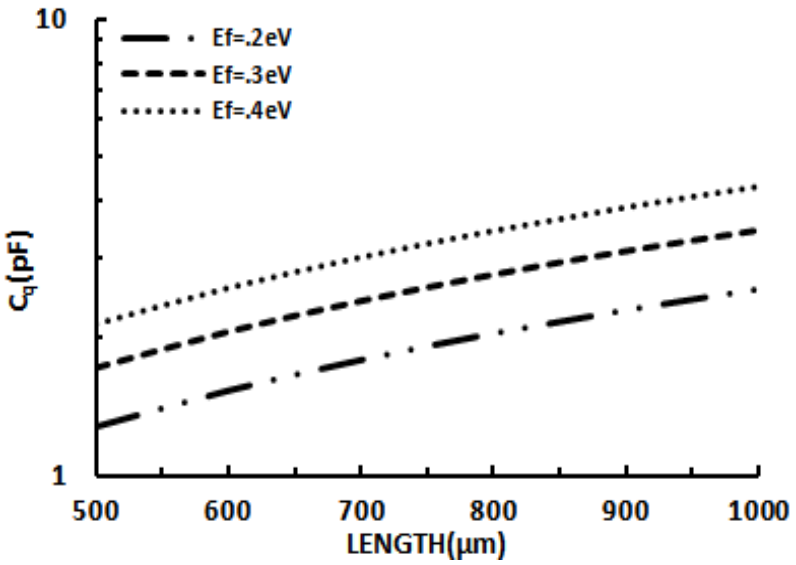

Fig.4.10 (c). Equivalent Quantum capacitance (C_q) as a function of Fermi energy (Ef) for global lengths of multilayer GNR interconnect.

The distributed capacitance is due to quantum capacitance (C_q) and electrostatic capacitance (C_e). In MLGNR interconnects quantum capacitance (C_q) is much larger than electrostatic capacitance (C_e) [9]. The equivalent capacitance is the resultant of the series combination of quantum capacitance (C_q) and electrostatic capacitance (C_e). The equivalent capacitance in MLGNR interconnect is due to the dominance of lower electrostatic capacitance (C_e) as **shown in Table 4.1**.

Table 4.1 Capacitance comparison of MLGNR with Copper interconnects

S.No.	**Lengths**	**Equivalent capacitance of MLGNR(fF)**			**Equivalent capacitance of copper(fF)**
		Ef=0.2eV	***Ef=0.3eV***	***Ef=0.4eV***	
1	Local(20µm)	0.503	0.505	0.506	0.1815
2	Semi-Global (500 µm)	12.59	12.63	12.66	4.538
3	Global(1mm)	22.48	22.53	22.56	14.82

4.6 Impedance as a function of width of MLGNR interconnect.

The per unit length (p.u.l) Impedance parameters of multilayer GNR are calculated from Eqs.(4.13)-(4.23). It is initially assumed that the thickness of the substrate y=50nm for local interconnects and y=75nm for global interconnects with dielectric constant (ϵ_r) equal to 2.05. For local interconnects thickness of GNR (H) is assumed twice of its width (w) and for global interconnects thickness of GNR (H) is thrice of its width (w).

4.6.1 Resistance Analysis for local and global global length interconnect

Figs.4.11(a) and (b) illustrate the dependence of equivalent p.u.l resistance (R_{eq}) of multilayer GNR on interconnect width for different Fermi energies (E_F) and mean free paths(λ). Equivalent p.u.l resistance are calculated for of 20 µm length of local interconnects (Fig.4.11(a)) and 500 µm length of global interconnects (Fig.4(b)).It can be seen that interconnect resistance of MLGNR decreases with increase in interconnect width and with increase in mean free path (λ).

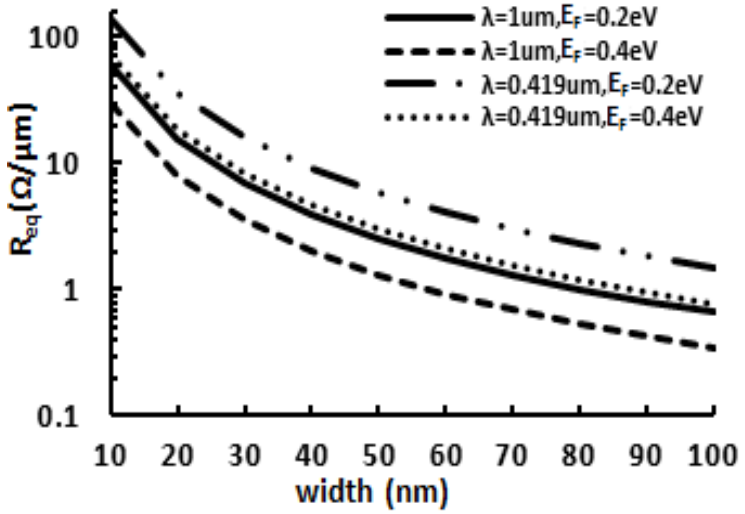

Fig.4.11(a) Equivalent resistance for different widths of local interconnect for 20µm length of multilayer GNR interconnect.

From the comparative study of equivalent resistance of Local and Global length interconnect, it is concluded that the resistance is increases with increase in length and decrease with increase in width, mean free path and Fermi energy.

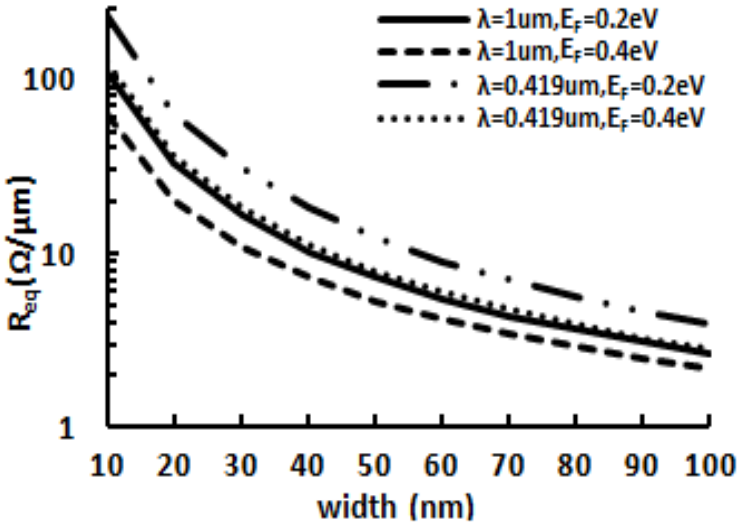

Fig.4.11(b) Equivalent resistance for different widths of global interconnect for 500μm length of multilayer GNR. interconnect.

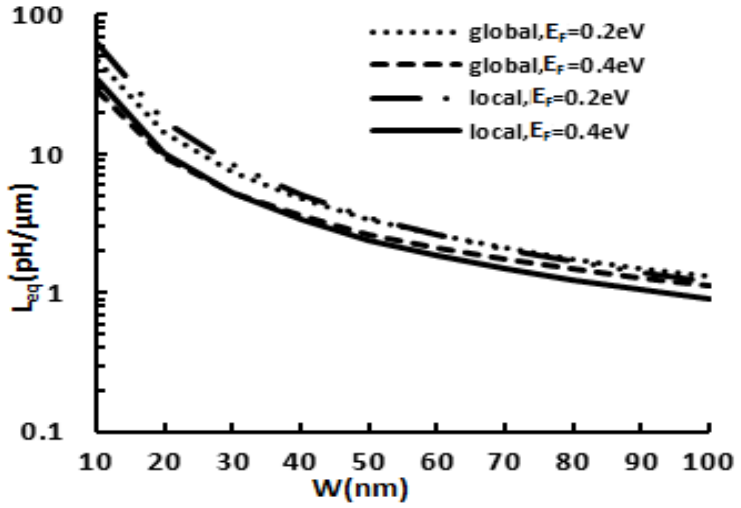

Fig.4.12 Equivalent inductance(L_{eq}) for different widths of MLGNR interconnect.

4.6.2 Inductance and Capacitance Analysis for local and global length interconnect.

Equivalent p.u.l inductance (L_{eq}) and capacitance (C_{eq}) of MLGNR based interconnect are shown in Fig.4.12 and Fig.4.13 respectively. In Fig.4.13 the effect of Fermi energy (E_F) is very weak and can be neglected. It is observed that the p.u.l inductance decreases with increase in interconnect width whereas reverse is true for p.u.l capacitance of interconnect. Results further reveal that in case of larger value of Fermi energy (E_F) the p.u.l impedance parameters are smaller than that of smaller value of E_F. Therefore, this width and Fermi energy (E_F) dependence

of impedance parameters indicates the significant effect to improve the performance of MLGNR based interconnect.

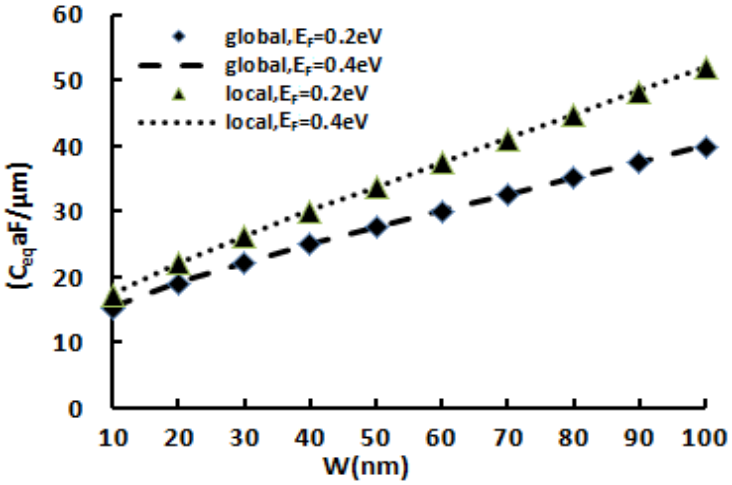

Fig.4.13 Equivalent capacitance(C_{eq}) for different widths of MLGNR Interconnect.

4.7 Conclusion

The Graphene nanoribbon (GNR) is potentially capable to replace traditional copper interconnects in very deep submicron (VDSM) technology. In this chapter, applicability of GNR as future VLSI interconnects has been analyzed. Transmission line models for single layer GNR (SLGNR) and multilayer GNR (SLGNR) has been presented using their respected geometries. Impedance parameters of MLGNR interconnects are analyzed with respect to length and width. The impact of Fermi energies has been critically analyzed. Inductive and capacitive coupling between the layers is included in this analysis. The results are further compared with copper for local, semiglobal and global interconnect lengths at 22 nm technology node.

The results of impedance analysis reveal that equivalent resistance, inductance and capacitance increases with increase in length. Resistance and inductance decreases with increase in Fermi energy and on the other hand, capacitance nominally increases with increase in Fermi energy. On comparison with copper it was found that resistance of MLGNR is much smaller than copper and the gap increases with increase in Fermi energy. However inductance and capacitance of MLGNR is higher than copper. The impedance parameters when analyzed as a function of width and it was found that Resistance and inductance decreases with increase in width and on the other hand capacitance increases with increase in width. It was also found that

resistance decreases with increase in mean free path. In addition with this we can be concluded that GNR is a is suitable alternative for copper replacement.

CHAPTER

5

Influence of number of layers on MLGNR Interconnect performance

5.1 Introduction

In this chapter, influence of number of layers on impedance of GNR is analyzed for global lengths at 22 nm technology node. Using the RLC model of multilayer GNR Interconnects in chapter 4, Power dissipation, Propagation Delay and Power delay product are analyzed for different number of layers in multilayer GNR (MLGNR) interconnects for different global lengths. SPICE simulation results reveal that performance of MLGNR interconnect improves with increasing number of layers.

5.2 Impedance Analysis

The per unit length (p.u.l) equivalent impedance parameters of MLGNR are calculated from Eqs.(4.13)-(4.23) as a function of Number of layers. All the physical dimensions of MLGNR are taken from [59],[60]. Mean free path (λ) is assumed to be 1μm for this analysis [33].Contact resistance is considered to be 20 kΩ for this analysis [17] and Fermi energy (E_F) is considered to be 0.3eV.

5.2.1 Variation of Resistance with respect to Number of layers.

The variation of equivalent resistance as a function of number of layers has been shown in Fig. 5.1. The resistance decreases with the increase in the number of layers. It is also observed that resistance increases with the increase in the interconnect lengths. The useful that can be extracted

from the above figure is that shorter interconnects with more number of layers can have the minimum resistance.

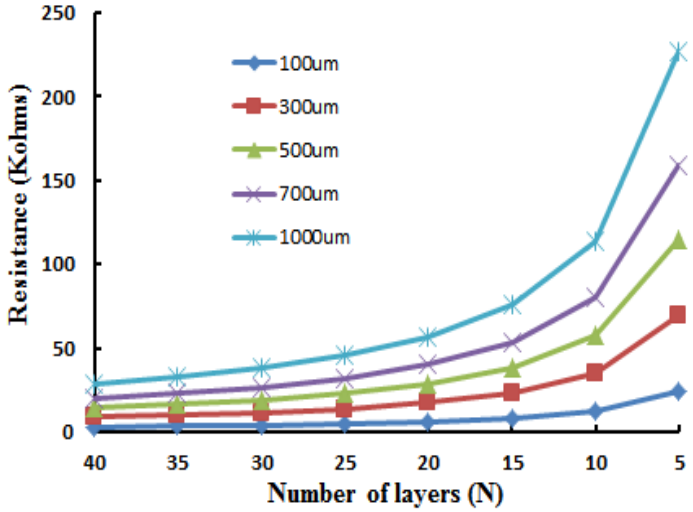

Fig. 5.1 Resistance as a function of layers for different interconnect lengths

5.2.2 Variation of Inductance with respect to Number of layers.

The variation of equivalent inductance as a function of number of layers has been shown in Fig. 5.2. The inductance decreases with the increase in the number of layers. It is also observed that inductance increases with the increase in the interconnect lengths. The useful that can be extracted from the above figure is that shorter interconnects with more number of layers can have the minimum inductance.

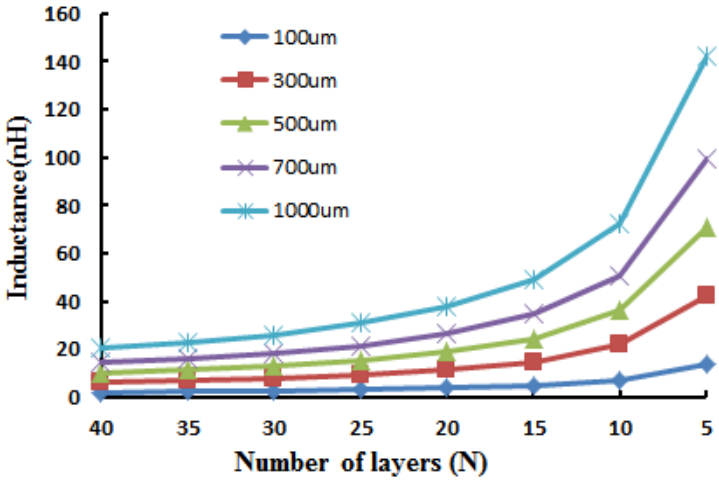

Fig. 5.2 Inductance as a function of layers for different interconnect lengths.

5.2.3 Variation of Capacitance with respect to Number of layers.

The variation of equivalent capacitance as a function of number of layers has been shown in Fig. 5.3. Capacitance increases with increase in length of the interconnect. It is also observed that there is a very nominal increase in the equivalent capacitance with the increase in the number of layers. The distributed capacitance is due to quantum capacitance (C_q) and electrostatic capacitance (C_e). In MLGNR interconnects quantum capacitance (C_q) is much larger than electrostatic capacitance (C_e) [9]. The equivalent capacitance is the resultant of the series combination of quantum capacitance (C_q) and electrostatic capacitance (C_e).

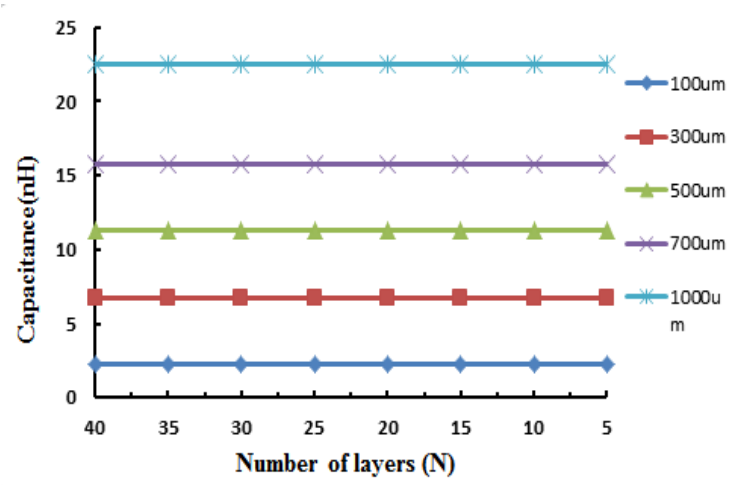

Fig. 5.3 Capacitance as a function of layers for different interconnect lengths.

5.3 Performance Analysis

The Simulation setup uses a CMOS inverter driving the MLGNR based equivalent distributed RLC based interconnect having a load of 10fF for global lengths. The input to the inverter is provided by a 0.1 GHz pulse of 1 ns rise time. The performance of this setup is studied by SPICE simulation. The predictive technology model for 22 nm is used for CMOS driver [56]. The equivalent resistance, inductance and capacitance are used for the simulation with optimum number of repeaters.

Fig. 5.4 show the variation of Propagation Delay of multi-layer GNR as a function of number of layers for different global interconnect lengths. Propagation Delay decreases with

increase in the number of layers (N). For the same number of layers, Propagation Delay also increases with the increase in length of the interconnect. For obtaining minimum propagation delay it is suggested to have higher number of layers in a MLGNR Interconnect.

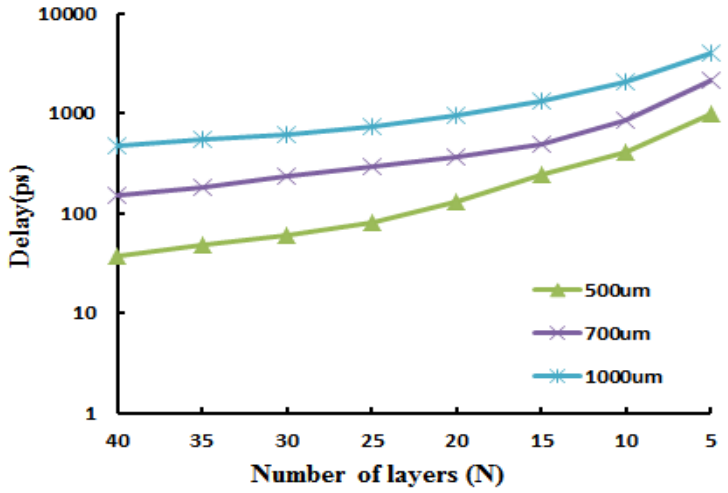

Fig. 5.4 Propagation delay as a function of layers for different interconnect lengths.

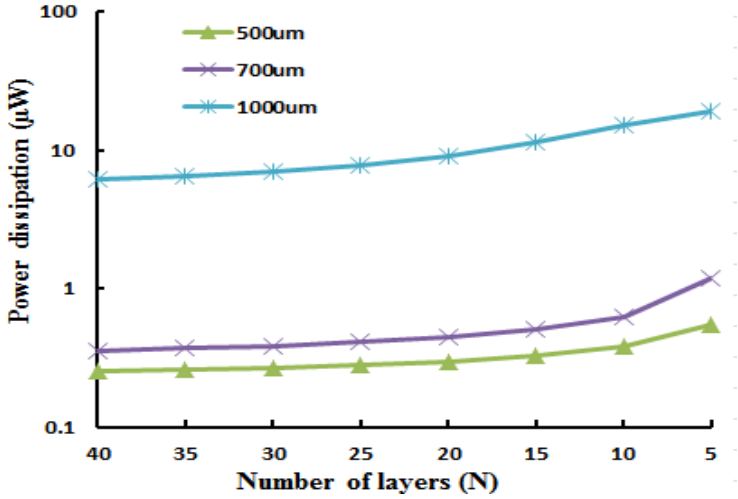

Fig. 5.5 Power Dissipation as a function of layers for different interconnect lengths.

Fig. 5.5 shows the variation of Power Dissipation of multi-layer GNR as a function of number of layers for different global interconnect lengths. Power Dissipation decreases with increase in the number of layers (N). For the same number of layers, Power Dissipation also increases with the increase in length of the interconnect. For obtaining minimum Power dissipation, it is suggested to have higher number of layers in a MLGNR Interconnect.

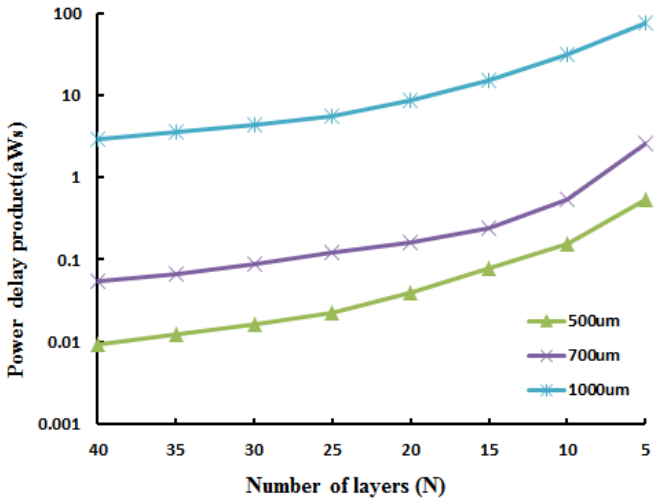

Fig. 5.6 Power Delay Product (PDP) as a function of layers for different interconnect lengths.

Fig. 5.6 shows the variation of Power Delay Product of multi-layer GNR as a function of number of layers for different global interconnect lengths. Power Delay Product decreases with increase in the number of layers (N). For the same number of layers, Power Delay Product also increases with the increase in length of the interconnect. For obtaining minimum Power Delay Product, it is suggested to have higher number of layers in a MLGNR Interconnect.

5.4 Conclusion

Using SPICE simulation, the influence of number of layers on the performance of MLGNR interconnect has been analyzed. The impedance parameters Resistance and Inductance decreases with the increase in the number of layers whereas the Capacitance is independent of the number of layers for MLGNR interconnect. The simulation results reveal that Propagation Delay, Power Dissipation and Power Delay Product decreases with the increase in number of layers. For better getting performance, it is suggested that maximum number of layers should be used in MLGNR interconnects.

CHAPTER

6

Performance Analysis of MLGNR at Local, Semi-global and Global length of interconnect

6.1 Introduction

In this chapter, the Performance in terms of PDP in Multi-layer graphene nanoribbon (MLGNR) based interconnect for VLSI applications, is analyzed. Similar analysis is carried out for copper interconnect at 22 nm technology node and results are compared with MLGNR for local, semi-global and global interconnects. The effects of inductive and capacitive coupling between the layers are considered in impedance parameters. SPICE simulation results reveal that MLGNR interconnect gives better performance compared to copper at local, semi-global and global levels.

6.2 Performance Analysis

The Simulation setup uses a CMOS inverter driving the multi-layer GNR based equivalent distributed RLC based interconnect having a load of 300fF for local and intermediate lengths and 1pF for global length. The input to the inverter is provided by a 0.1 GHz pulse of 1 ns rise time. The performance of this setup is studied by SPICE simulation. The predictive technology model for 22 nm is used for CMOS driver [56]. The equivalent resistance, inductance and capacitance are used for the simulation with optimum number of repeaters.

Similar analysis is carried out with copper using the same number of repeaters. The relative measure of multi-layer GNR is obtained by normalizing multi-layer interconnect delay by delay of Copper interconnects. All the physical dimensions of MLGNR and copper and taken from[59],[60] for 22nm technology node and line parameters of copper are calculated using [56].

Using the RLC model in chapter 4, the total equivalent R,L and C for different lengths and Fermi energies (E_F) has been calculated. The mean free path (λ) is assumed to be 1μm for this analysis [11].

6.3 Performance Analysis for Local Interconnects

6.3.1 Propagation Delay Analysis.

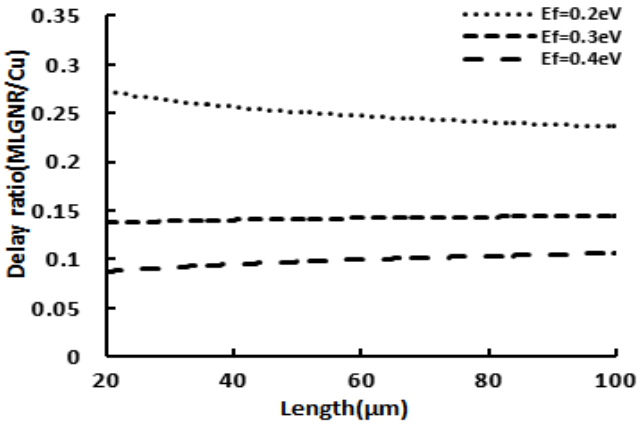

Fig. 6.1 Delay ratio (MLGNR/Cu) with varying length for local interconnects for different Fermi energies.

Fig. 6.1 shows the variation of delay ratios (Normalized delay) of multi-layer GNR and copper for local lengths of interconnects. Fig.6.1 exemplify that delay ratios decreases with increase in length nominally and with increase in Fermi energies. This is due to the dominance of higher resistance of MLGNR at local lengths. The simulation results reveal that MLGNR interconnects has much lower delay as compared to copper interconnects and the use of higher Fermi energy can reduce the delay of MLGNR even more.

6.3.2 Power Dissipation Analysis.

Fig. 6.2 shows the variation of Power ratios (Normalized power) of multi-layer GNR and copper for local lengths of interconnects. Fig.6.2 exemplify that power ratios increases with increase in length nominally and decreases with increase in Fermi energies. This is due to the dominance of higher resistance at local lengths and the equivalent capacitance of MLGNR interconnects is approximately independent of Fermi energy as explained in chapter 4 at local lengths. The

simulation results reveal that MLGNR interconnects dissipate less power as compared to copper interconnects and the use of higher Fermi energy can reduce the power of MLGNR even more.

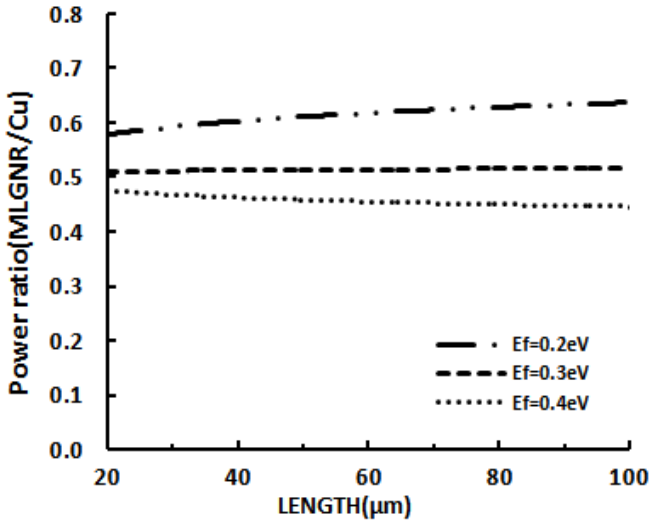

Fig. 6.2 Power ratio (MLGNR/Cu) with varying length for local interconnects for different Fermi energies.

6.3.3 Power Delay Product (PDP) Analysis

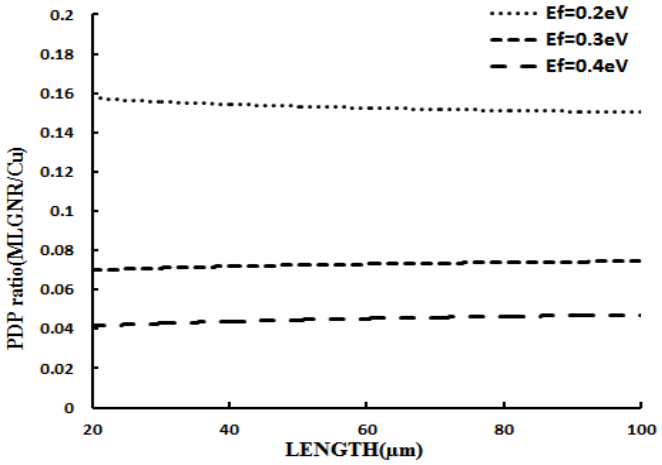

Fig. 6.3 PDP ratio (MLGNR/Cu) with varying length for local interconnects for different Fermi energies.

Fig. 6.3 shows the variation of Power Delay product (PDP) ratios (Normalized power delay product) of multi-layer GNR and copper for local lengths of interconnects. Fig.6.3 exemplify that PDP ratios increases with increase in length nominally and decreases with increase in Fermi energies. This is due to the dominance of nominally increasing power ratios over nominally decreasing propagation delays at local lengths. The simulation results reveal that MLGNR interconnects has much lower power delay product as compared to copper

interconnects and the use of higher Fermi energy can reduce the PDP of MLGNR even more. From the above analysis, it is concluded that MLGNR interconnects perform much better than copper for local lengths at 22 nm technology node.

6.4 Performance Analysis for Semi-Global Interconnects

6.4.1 Propagation Delay Analysis.

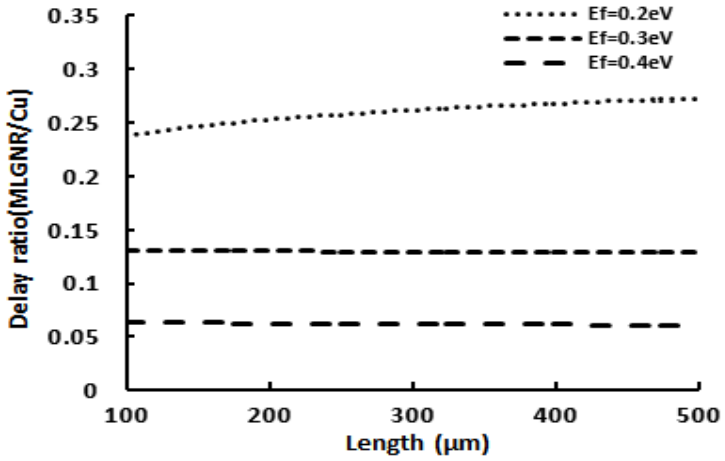

Fig. 6.4 Delay ratio (MLGNR/Cu) with varying length for Semi-global interconnects for different Fermi energies.

Fig. 6.4 shows the variation of delay ratios (Normalized delay) of multi-layer GNR and copper for Semi-global lengths of interconnects. Fig.6.4 exemplify that delay ratios decreases nominally with increase in length and decreases with increase in Fermi energies. This is due to the dominance of comparable resistance of MLGNR at Semi-global lengths. The simulation results reveal that MLGNR interconnects has much lower delay as compared to copper interconnects and the use of higher Fermi energy can reduce the delay of MLGNR even more.

6.4.2 Power Dissipation Analysis.

Fig. 6.5 shows the variation of Power ratios (Normalized power) of multi-layer GNR and copper for Semi-global length of interconnects. Fig.6.5 exemplify that power ratios increases with increase in length and decreases with increase in Fermi energies. This is due to the dominance of comparable resistance at Semi-global lengths and the equivalent capacitance of MLGNR interconnects is approximately independent of Fermi energy as explained in chapter 4 at Semi-global lengths. The simulation results reveal that MLGNR interconnects dissipate less power as

compared to copper interconnects and the use of higher Fermi energy can reduce the power of MLGNR even more.

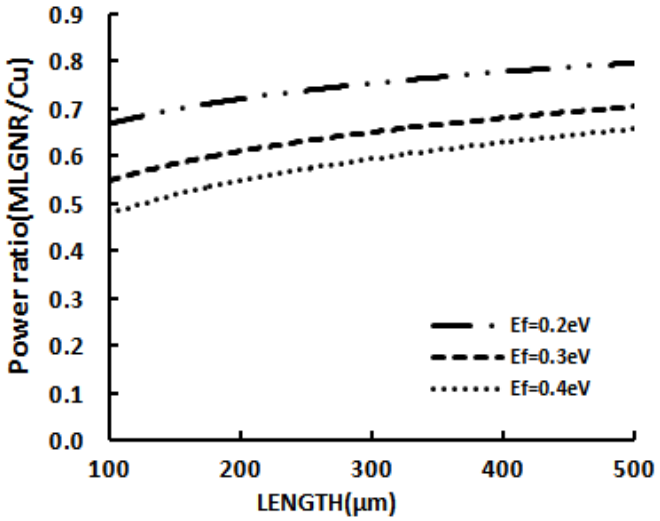

Fig. 6.5 Power ratio (MLGNR/Cu) with varying length for Semi global interconnects for different Fermi energies.

6.4.3 Power Delay Product (PDP) Analysis.

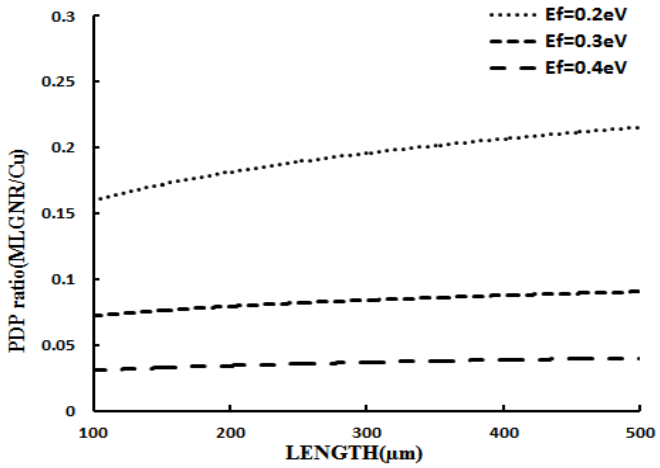

Fig. 6.6 PDP ratio(MLGNR/Cu) with varying length for Semi-global interconnects for different Fermi energies.

Fig. 6.6 shows the variation of Power Delay product (PDP) ratios (Normalized power delay product) of multi-layer GNR and copper for semi-global lengths of interconnect. Fig.6.3 exemplify that PDP ratios increases with increase in length and decreases with increase in Fermi energies. This is due to the dominance of increasing power ratios over nominally decreasing propagation delays at Semi-global lengths. The simulation results reveal that MLGNR interconnects has much lower power delay product as compared to copper interconnects and the

use of higher Fermi energy can reduce the PDP of MLGNR even more. From the above analysis, it is concluded that MLGNR interconnects perform much better than copper for Semi-global lengths at 22 nm technology node.

6.5 Performance Analysis for Global Interconnects

6.5.1 Propagation Delay Analysis.

Fig. 6.7 shows the variation of delay ratios (Normalized delay) of multi-layer GNR and copper for Global lengths of interconnect. Fig.6.7 exemplify that delay ratios decreases with increase in length and decreases with increase in Fermi energies. This is due to the dominance of lower resistance of MLGNR at Global lengths. The simulation results reveal that MLGNR interconnects has much lower delay as compared to copper interconnects and the use of higher Fermi energy can reduce the delay of MLGNR even more. It is also predicted that longer MLGNR interconnects have lesser propagation delay ratio (MLGNR/Cu) than smaller length interconnects.

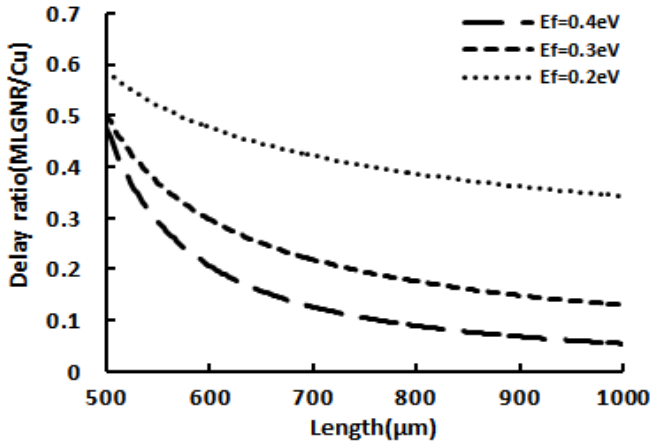

Fig. 6.7 Delay ratio(MLGNR/Cu) with varying length for Global interconnects for different Fermi energies.

6.5.2 Power Dissipation Analysis.

Fig. 6.8 shows the variation of Power ratios (Normalized power) of multi-layer GNR and copper for Global length of interconnects. Fig.6.8 exemplify that power ratios decreases with increase in length and decreases with increase in Fermi energies. This is due to the dominance of lower resistance at Global lengths and the equivalent capacitance of MLGNR interconnects is

approximately independent of Fermi energy as explained in chapter 4 at Global lengths. The simulation results reveal that MLGNR interconnects dissipate less power as compared to copper interconnects and the use of higher Fermi energy can reduce the power of MLGNR even more.
It is also concluded that the use higher Fermi energies in MLGNR interconnects can provide better results than copper interconnects.

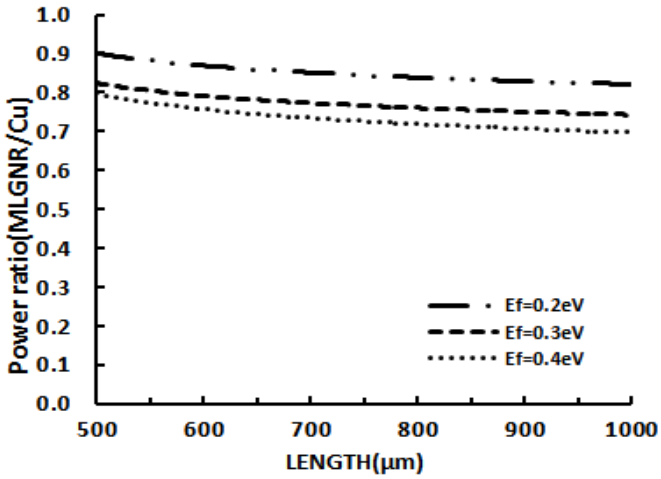

Fig. 6.8 Power ratio (MLGNR/Cu) with varying length for Global interconnects for different Fermi energies.

6.5.3 Power Delay Product (PDP) Analysis.

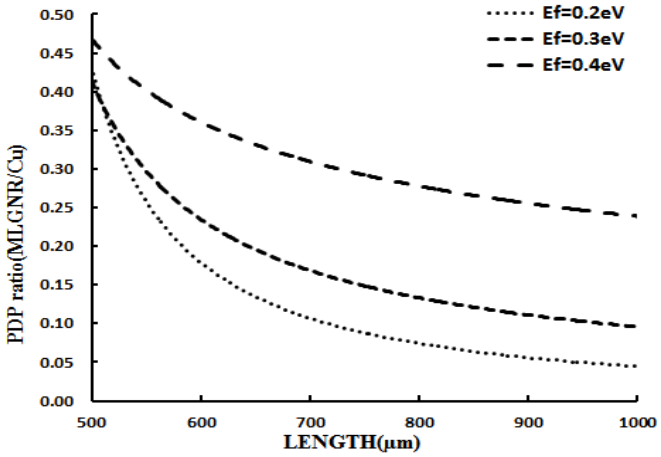

Fig. 6.9 PDP ratio (MLGNR/Cu) with varying length for Global interconnects for different Fermi energies.

Fig. 6.9 shows the variation of Power Delay product (PDP) ratios (Normalized power delay product) of multi-layer GNR and copper for global lengths of interconnect. Fig.6.3 exemplify that PDP ratios decreases with increase in length and decreases with increase in Fermi energies.

This is due to the dominance of decreasing power ratios and decreasing propagation delays at Global lengths. The simulation results reveal that MLGNR interconnects has much lower power delay product as compared to copper interconnects and the use of higher Fermi energy can reduce the PDP of MLGNR even more. From the above analysis, it is concluded that MLGNR interconnects perform much better than copper for Global lengths at 22 nm technology node. As compared to copper, the longer MLGNR interconnects are expected to perform better than smaller length interconnects.

6.6 Conclusion

The influence of length variation on propagation delay, power dissipation and power delay product of Multi-layer GNR has been investigated. SPICE simulation is used to compare MLGNR interconnect propagation delay, power dissipation and power delay product with that of copper interconnect. It has been seen that the Multi-layer GNR gives better performance in terms of propagation delay, power dissipation and power delay product than copper for different interconnect lengths. Results also reveal that the Fermi energy can control MLGNR interconnect resistance. This can be utilized to improve the performance of MLGNR.

CHAPTER

7

Impact of interlayer resistance on performance of MLGNR interconnect

7.1 Introduction

An equivalent RLC model for MLGNR interconnect including interlayer resistance has been presented in this chapter. The equivalent impedance parameters are calculated using the RLC model. The impact of interlayer resistance on equivalent resistance has been analyzed. The effect of interlayer resistance due to c-axis resistivity on performance is analyzed in terms of delay, power and power delay product (PDP) of Multi-layer graphene nanoribbon (MLGNR) interconnect. A similar analysis is performed for copper interconnect and results are compared with MLGNR at 22 nm technology node. The impact of interlayer resistance on equivalent resistance of MLGNR is critically analyzed. Inductive and capacitive coupling between the adjacent layers is included in this analysis. MLGNR, compared to copper, gives better performance in terms of delay, power and PDP with higher value of Fermi energy for global lengths of interconnect.

7.2 RLC Model of MLGNR interconnect

Fig.7.1 shows the schematic of the MLGNR interconnect, where N is the number of layers stacked one above the other, w is the width, H is the thickness, y is the height of the MLGNR from the ground plane, ε_r is the dielectric constant and δ is the distance (0.34nm) between the adjacent layers.

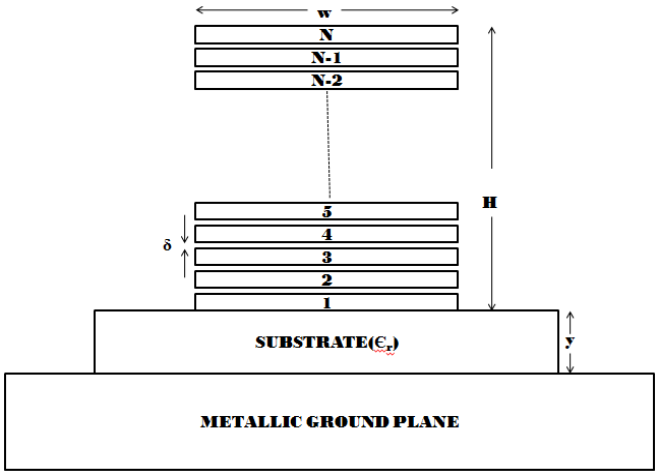

Fig. 7.1 Schematic of multilayer GNR interconnect.

The RLC Model for MLGNR interconnect is shown in Fig.7.2. R_{mc} is the resistance due to imperfect contacts. R_q is the quantum resistance and is defined as [10]

$$R_q = \frac{h/2e^2}{N_{ch}} = \frac{12.9k\Omega}{N_{ch}} (\text{for } l_{GNR} < \lambda) \quad (7.1),$$

where N_{ch} is the number of conducting channels (modes) in one layer and is given by [58]

$$N_{ch} = \sum_{i=1}^{N_c} [1 + e^{(E_i - E_F)/KT}]^{-1} + \sum_{i=1}^{N_v} [1 + e^{(E_i + E_F)/kT}]^{-1} \quad (7.2),$$

where i is the positive integer, E_F is the Fermi energy, k is the Boltzmann constant, T is the temperature, N_c is the density of states of electrons and N_v is the density of states of holes.

$$E_i = \frac{h\vartheta_F i}{2w} \quad (7.3),$$

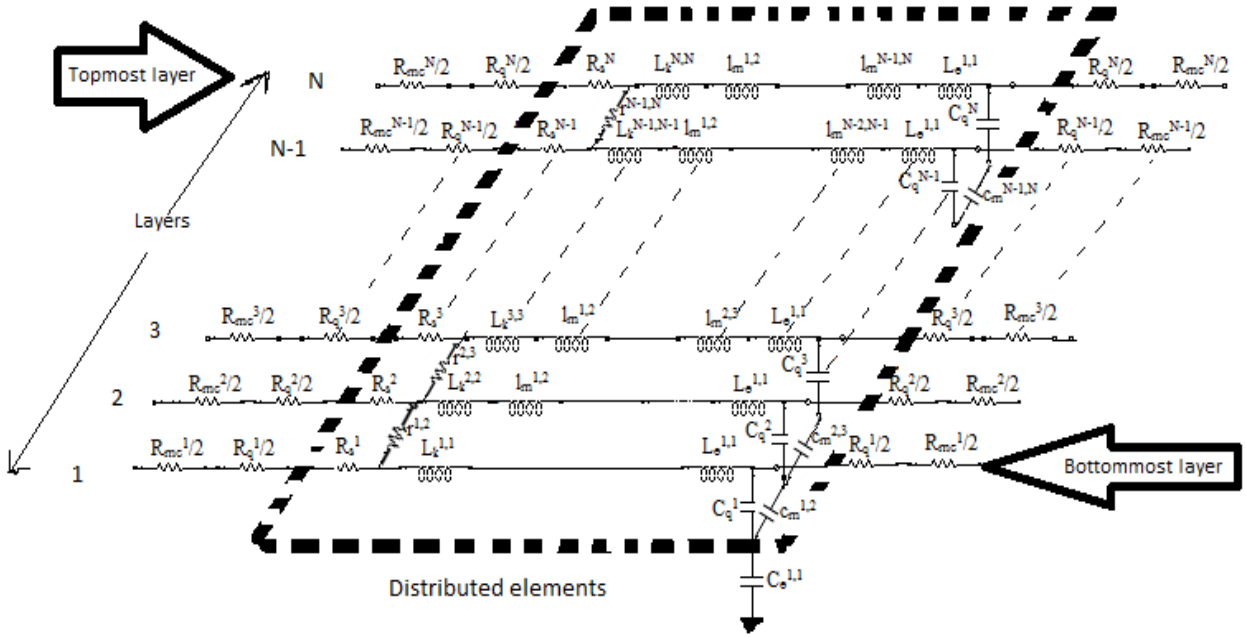

Fig. 7.2. RLC Model for multilayer GNR interconnect.

where E_i represents the quantized energy that corresponds to the i^{th} conduction or valence subband. The number of conduction channels increases linearly for metallic armchair GNR's which is approximated as

$$N_{ch} \cong KE_F \cong \alpha w E_F \text{ (for } E_F \geq 0.1eV \,\&\, w > 10nm) \tag{7.4}$$

The distributed scattering resistance of single layer GNR (R_{layer}) is defined by [28]. R_b is the layer resistance along its differential length of one partition and M is the number of partitions and is chosen to be 10 for this analysis [28].

$$R_{layer} = R_q . \frac{l_{GNR}}{\lambda} \tag{7.5},$$

where l_{GNR} and λ are the length and mean free path of the GNR respectively. If the GNR has number of partitions (M) along its differential length (l_{GNR}), then layer resistance (R_b) of single partition is defined as

$$R_b = \frac{R_{layer}}{M} \tag{7.6}$$

The interlayer resistance (r) is the perpendicular resistance between adjacent layers and defined by [5]

$$r = \frac{\rho_c . \delta}{l_{GNR} . W} \quad (7.7),$$

where ρ_c is the c-axis resistivity [61] and δ is the distance between the adjacent layers. If the GNR has M partitions, then R_a is the interlayer resistance of one partition [5].

$$R_a = M . r \quad (7.8)$$

The total resistance of single partition (R) of the MLGNR structure as shown in Fig.7.2. is given by [10],

$$R_N = \left(\frac{1}{R_b} + \frac{1}{R_a + R_{N-1}}\right)^{-1} \quad (7.9)$$

Hence, the equivalent resistance (R_{eq}) of the MLGNR is given by

$$R_{eq} = \frac{R_{MC}}{N} + M . R_N \ \ (\text{for } l_{GNR} > \lambda) \quad (7.10)$$

The equivalent inductance (L_{eq}) and capacitance (C_{eq}) are calculated using the expressions (4.17) to (4.23) in chapter 4.

7.3. Impedance Analysis

The equivalent impedance parameters of MLGNR are calculated from Eqs.(7.1)-(7.10), (4.17)-(4.23) as a function of Fermi energy. All the physical dimensions of MLGNR and copper are taken from [59], [60] and line parameters (R,L and C) of copper are calculated using appropriate expressions available in [56]. These calculations are done for global lengths at 22nm technology. In this work, mean free path (λ) and c-axis resistivity (ρ_c) are assumed to be 1μm [11] and 0.3Ωcm [28] respectively.

Fig.7.3, shows the variation of equivalent resistance (R_{eq}) under two cases (with and without interlayer resistance) of MLGNR as a function of number of layers (N) for different interconnect lengths. The rate of decrease of resistance with increasing number of layers is found to be lower for the first case (including interlayer resistance case). This effect is more dominating

for smaller lengths. This is due to the dominant perpendicular component of the equivalent resistance than the horizontal one.

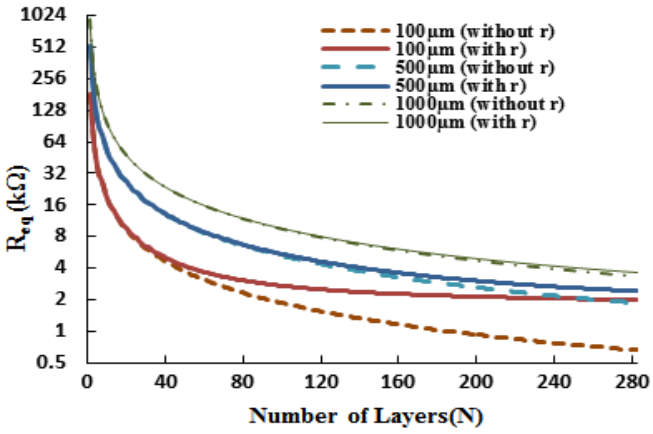

Fig..7.3 Variation of equivalent resistance (R_{eq}) with and without interlayer resistance (r) of MLGNR with respect to number of layers (N).

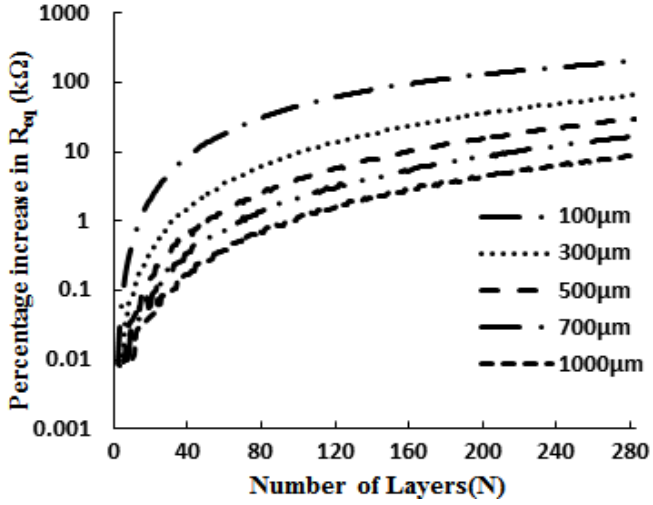

Fig..7.4 Percentage increase in resistance due to interlayer resistance for different Global lengths.

Fig.7.4, shows the percentage increase in the equivalent resistance as a function of layers for different global lengths. The impact of interlayer resistance over smaller lengths is observed to be more significant over longer lengths. This is due to the fact that coupling between the layers increases with increase in interconnect lengths.

Fig.7.5 illustrate a typical example of the dependence of MLGNR interconnect resistance on both length (l_{GNR}) and Fermi energy (E_F) for global interconnects. It shows that resistance increases with increase in interconnect length for both MLGNR and copper interconnects.

Resistance of MLGNR with smaller Fermi energies (E_F) is observed more. It is observed that the impact of interlayer resistance on equivalent resistance is significantly large for smaller lengths.

Furthermore, it is observed that the increase in resistance with length is much less as compared to the without including interlayer resistance case. It has also been seen that the impact of interlayer resistance for global lengths above (700 µm) in both cases have negligible effect on equivalent resistance. The resistance of MLGNR interconnects are further compared with copper. Resistance of copper is generally higher except for smaller lengths when interlayer resistance is included. Therefore, the influence of interlayer resistance and Fermi energy on resistance for different lengths has significant effect on performance of MLGNR interconnect.

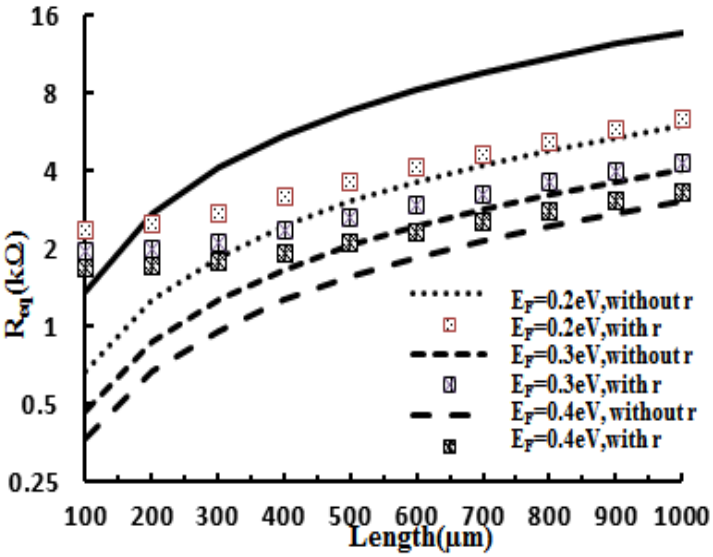

Fig.7.5 Variation of equivalent resistance (R_{eq}) with and without interlayer resistance (r) of MLGNR with respect to length (L) for different Fermi energies (E_F).

7.4. Performance Analysis

The circuit considered for analysis consist of a CMOS inverter driving the distributed MLGNR interconnect having a load capacitance of 1pF as shown in Fig.7.6. The frequency of input pulse given to driver is 0.1 GHz, having rise time of 1ns. SPICE simulations are done to study the performance of this setup. The predictive technology model for 22 nm is used for CMOS driver [56]. This simulation set up is used to study the performance with optimized number of repeaters.

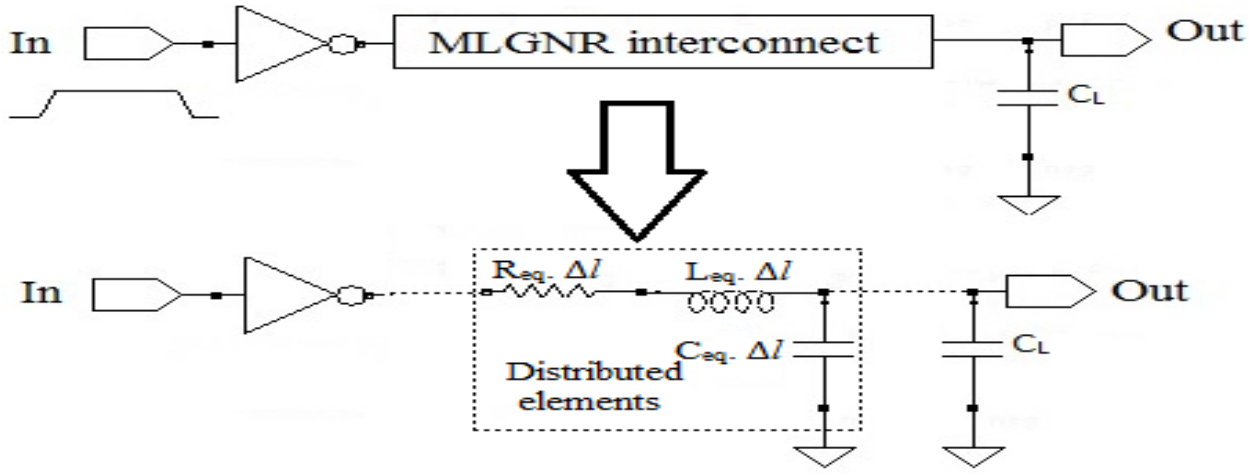

Fig..7.6. CMOS inverter driving an interconnect load.

7.4.1 Effect of Contact Resistance on Propagation Delay

Fig.7.7. shows the the dependence of contact resistance on MLGNR delay without including interlayer resistance (r) for different interconnect lengths. For accurate analysis, Fermi energy is assumed to be 0.4eV. It is observed that the delay increases with both increase in contact resistance and length.

This is due the fact that the resistance for short lengths is small and it increases linearly with length. In this case, perpendicular component of resistance doesn't exist and the total resistance is dependent only on its horizontal component. The horizontal component of resistance is directly proportional to its length. The delay for MLGNR interconnects is due to the combined effect of the impedance parameters. It is observed that the contact resistance variation has significant impact on propagation delay for smaller lengths.

Fig.7.8. shows the dependence of contact resistances on MLGNR delay with including interlayer resistance (r) for different interconnect lengths. It is observed that the delay increases with increase in both length and contact resistance.The total resistance is dependent on its perpendicular component as well as horizontal component. For shorter lengths, due to the effect of interlayer resistance (r), the perpendicular component of resistance increases and becomes dominant than horizontal. It has also been noted that propagation delay increases rapidly above a critical length (≈700μm) compared to shorter length of interconnect. This is due to the fact that horizontal component of resistance increases while perpendicular component decreases

proportionally with increase in length. The similarity in the propagation delays are observed for longer interconnects for both including and not including interlayer resistance.

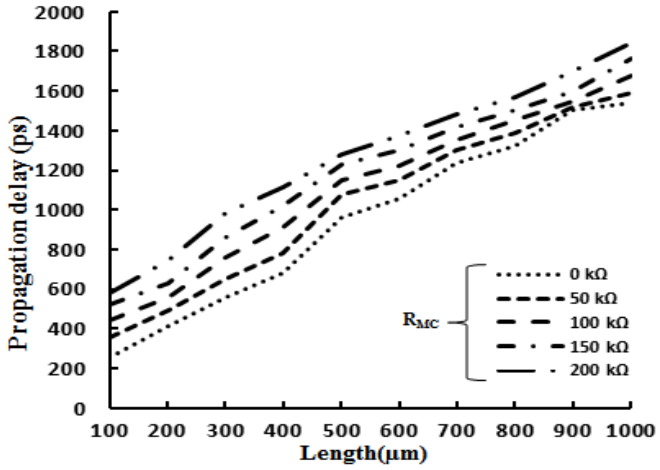

Fig.7.7. Propagation delay for different contact resistances (Rmc) of MLGNR with respect to length (L) for MLGNR without including interlayer resistance (r).

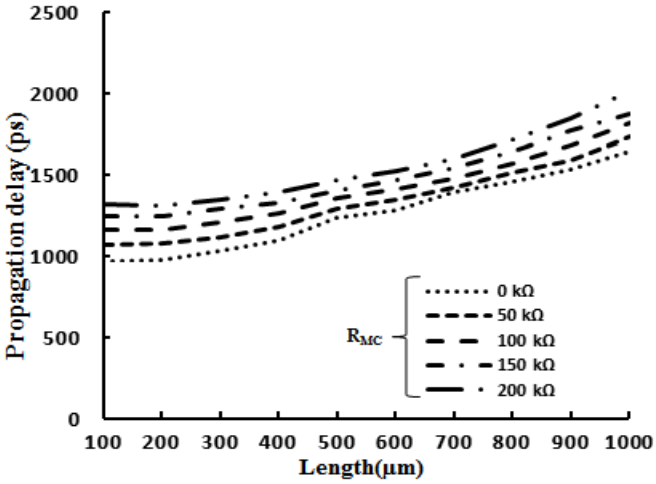

Fig.7.8. Propagation delay for different contact resistances (Rmc) of MLGNR with respect to length (L) for MLGNR with including interlayer resistance (r).

Fig.7.9 shows the Percentage increase in propagation delay with and without including interlayer resistance (r) for different contact resistances (R_{MC}) with 100µm and 700µm interconnect lengths respectively. This result is obtained from Fig.7.7 and Fig.7.8 which shows the impact of contact resistance on propagation delays under two cases viz. with and without including interlayer resistance. The contact resistance is subject to change with fabrication method and technology being used. The estimated propagation delay changes with sudden increase in contact resistance.

The results reveal that propagation delays associated to MLGNR including interlayer resistance are less sensitive to change in contact resistance (see Fig.7.9). It is also evident that shorter length interconnects are more vulnerable to contact resistance than longer length interconnects.

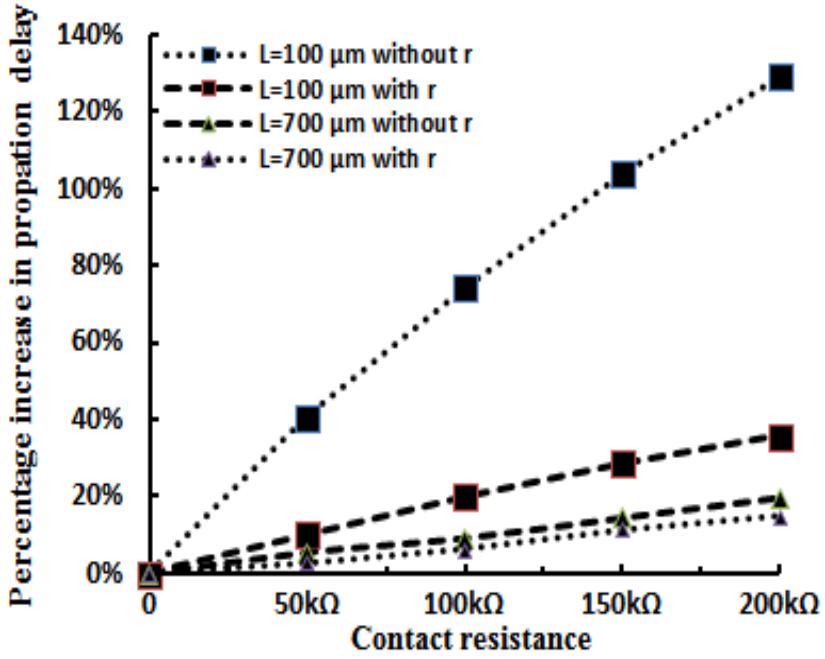

Fig.7.9 Percentage increase in propagation delay with and without including interlayer resistance (r) is calculated for different contact resistances(R_{MC}) for different lengths.

7.4.2 Effect of Fermi energy on performance.

Figs.(7.10)-(7.12). shows the variation of propagation delay ratio (MLGNR/Cu), power dissipation ratio (MLGNR/Cu) and power delay product ratio (MLGNR/Cu) with respect to length for different fermi energies of MLGNR interconnect with and without including interlayer resistance (r). For the following analysis, contact resistance is assumed to be 20kΩ [17].The analysis similar to MLGNR is done for copper using the same number of repeaters, so that the relative measure of MLGNR is obtained by normalizing MLGNR interconnect delay, power and power delay product to that of copper interconnects.

It is observed that the propagation delay of MLGNR compared to copper improves as length increases. This is due to the impact of lower resistance associated with MLGNR compared to copper. For length below 200µm, copper gives better performance, compared to MLGNR with including interlayer resistance, due to dominant perpendicular component over horizontal component of resistance. It is also observed that with the increase in Fermi energy,

delay ratio (normalized delay) decreases. This is due to the decrease of both equivalent resistance (R_{eq}) and equivalent inductance (L_{eq}) and approximately unchanged equivalent capacitance (C_{eq}) of MLGNR with increase in Fermi energy (E_F).

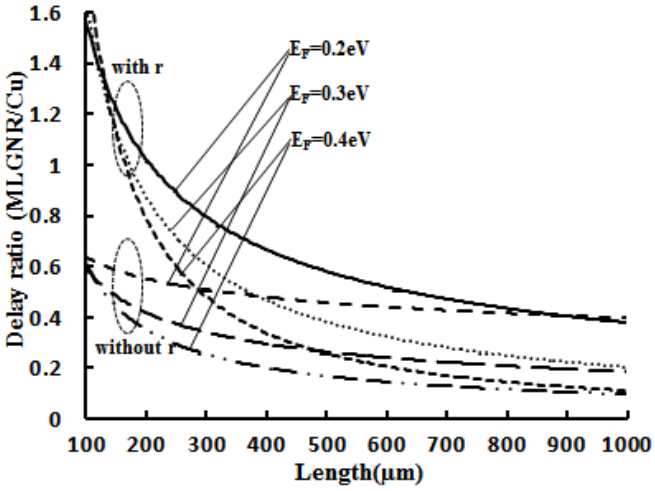

Fig.7.10. Propagation delay ratio with varying length for with and without interlayer resistance (r) for different Fermi energies.

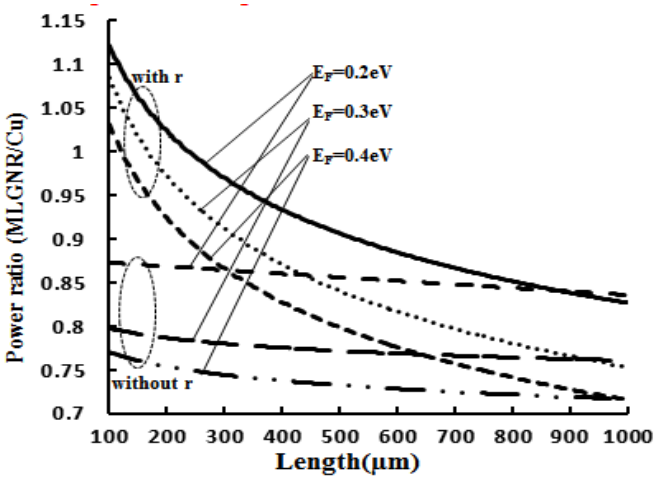

Fig.7.11. Power ratio with varying length for with and without interlayer resistance (r) for different Fermi energies.

Fig.7.11. shows the dependence of interlayer resistance (r) and Fermi energy (E_F) on power of the MLGNR interconnect. Copper generally dissipates more power than MLGNR except for smaller lengths upto 300μm when interlayer resistance is included. It is observed that Power

ratios decreases with increase in length when interlayer resistance is included and remains almost constant when interlayer resistance is not included. This is due to the fact that the rate of increase of resistance with increase in length is much lower with interlayer resistance case than copper as well as without interlayer resistance case. It is also observed that Power ratios decreases with increase in Fermi energy due to the impact of Fermi energy on the impedance parameters (R,L,C).

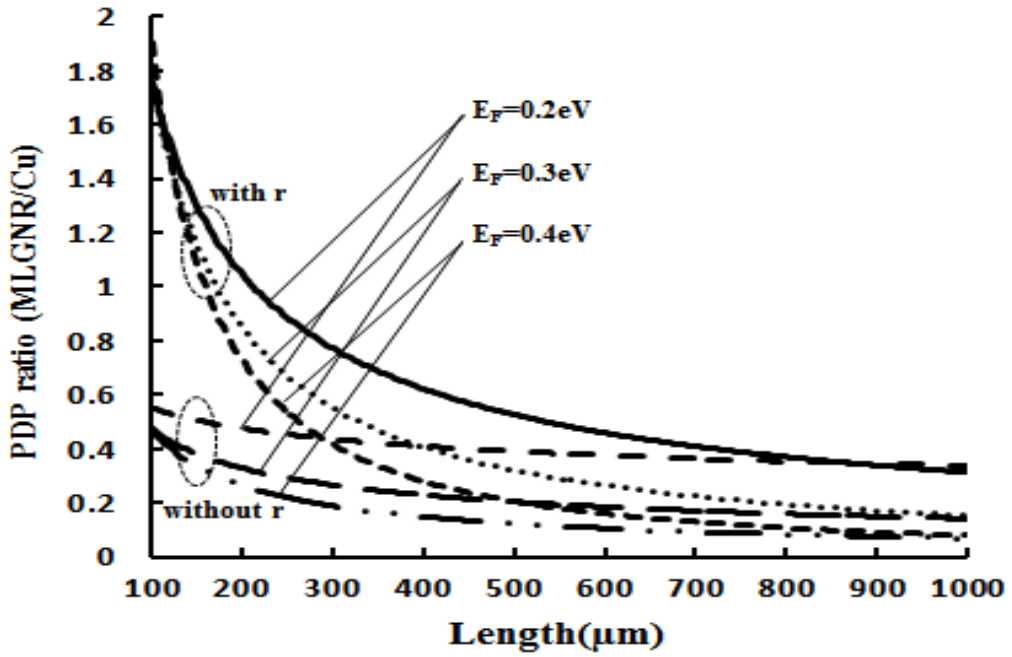

Fig.7.12. PDP ratio with varying length for with and without interlayer resistance (r) for different Fermi energies.

The overall performance of MLGNR interconnects depends on both propagation delay and power dissipation. Fig.7.12 shows the power delay product (PDP) of MLGNR compared to copper interconnects. It is evident that choice of higher Fermi energy can improve the PDP and hence the performance of MLGNR interconnects. This analysis shows that PDP improves with both length and Fermi energy and the impact of interlayer resistance can be neglected for longer interconnects.

7.5 Conclusion

The impact of interlayer resistance on performance is critically analyzed and comparison is made with the performance of MLGNR interconnects without including interlayer resistance. For short lengths, significant influence of interlayer resistance on performance is observed and with

increasing length influence of interlayer resistance is minimum. The simulated results are further compared with the performance of copper interconnects. The influence of fermi energy is analyzed for MLGNR interconnects and found that performance improves for higher fermi energies. The impact of contact resistance on propagation delay is also analyzed for MLGNR interconnects and increase in propagation delay with higher conact resistance on different lengths is analyzed.

CHAPTER

8 Conclusions and Future Scope

8.1 Conclusion

In this thesis, the performance in terms of propagation delay, power dissipation and power delay product has been analyzed for MLGNR interconnects. SPICE simulations are done to compare the performance of MLGNR interconnects with copper at 22 nm technology node. Inductive and capacitive coupling between the layers has been considered for accurate estimation of propagation delay and power dissipation for MLGNR interconnects. The following are some of the conclusions:

1. Impedance parameters of MLGNR are critically analysed and are compared with copper interconnects. The effect of Fermi energy on impedance parameters is also analysed. It was found that equivalent resistance of MLGNR interconnect is much lower than copper interconnects, however equivalent inductance and capacitance are higher than the copper interconnects (Chapter 4).
2. The performance of the MLGNR interconnects are analysed in terms of number of layers and was found that performance improves by increasing the number of layers (Chapter 5).
3. The performance of MLGNR interconnect at local, semi-global and global lengths is compared with copper interconnect. The result reveals that performance of MLGNR is better than copper at all lengths. Also it was found that MLGNR with higher Fermi energy perform better (chapter 6).
4. The impact of interlayer resistance on performance is critically analyzed and comparison is made with the performance of MLGNR interconnects without including interlayer

resistance. For short lengths, significant influence of interlayer resistance on performance is observed and with increasing length influence of interlayer resistance is minimum (Chapter 7).

8.2 Future Scope

The following are some of the future implementations that can be possibly made:

1. The performance of the interconnect can be compared by using analytical timing model.
2. Temperature dependent analysis can be done in MLGNR interconnects.
3. Performance can be examined in more advanced technologies.
4. Performance of GNR based devices and interconnects can be evaluated simultaneously.

Publications

1. Ankit Gupta, Mayank kumar rai, "Delay Analysis in Multi-layer Graphene Nanoribbon based VLSI Interconnects," *In proc. 2nd Intl. Conf. on Emerging Research in Computing, Information, Communication and Applications* (ERCICA-14), 1–2 Aug.,2014.
2. Ankit Gupta, Mayank kumar rai, "Influence of Fermi-energy on Performance of Multi-layer Graphene Nanoribbon Interconnects," *In proc. Of International Multi-Track Conference on Sciences, Engineering and Technical Innovations* (IMTC-2014), 3-4 June, 2014.

References

[1] Hong Li, Chuan Xu, and Kaustav Banerjee, "Carbon Nanomaterials: The Ideal Interconnect Technology for Next- Generation ICs,",*Design & Test of Computers, IEEE*, vol. 27, no.4, pp. 20–31, Aug. 2010.

[2] K. C. Saraswat and F. Mohammadi, "Effect of scaling of interconnections on the time delay of VLSI circuits," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 275-280, Apr. 1982.

[3] S. Rakheja, V. Kumar and A. Naeemi, "Evaluation of the Potential Performance of Graphene Nanoribbons as On-Chip Interconnects," *in Proc. IEEE*, vol. 101, no. 7, pp. 1740-1765, July 2013.

[4] Online http://www.osa-opn.org/ home/ articles/ volume_20/ issue_6/ features/ green_silicon_photonics/ U5XCIPldXEQ.

[5] V. Kumar, S. Rakheja, and A. Naeemi, "Modeling and optimization for multi-layer graphene nanoribbon conductors," in *Proc. IEEE Interconnect Technol. Conf.*, 2011, pp. 1–3.

[6] Tamer Ragheb and Yehia Massoud, "On the Modeling of Resistance in Graphene Nanoribbon (GNR) for Future Interconnect Applications," *IEEE/ACM International Conference*, pp. 593 -597, 2008.

[7] A. Naeemi and J. D. Meindl, "Conductance modeling for graphene nanoribbon (GNR) interconnects," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 428–431, May 2007.

[8] Y. Fang, W.S. Zhao, X. Wang, F. Jiang, and W. Y. Yin, "Circuit modelling of multilayer graphene nanoribbon (MLGNR) interconnects," *Asia-Pacific Electromagn. Compat.*, May 2012, pp. 625-628.

[9] C. Xu, H. Li, and K. Banerjee, "Graphene nano-ribbon (GNR) interconnects: A genuine contender or a delusive dream?," *IEDM Tech. Dig.*, pp. 201–204, Dec. 2008.

[10] A.K.Nishad and R. Sharma, "Analytical Time-Domain Models for Performance Optimization of Multilayer GNR Interconnects," *IEEE Journal of selected topics in Quantum Electronics*, vol. 20, no. 1, Jan 2014.

[11] H. Li et al., ''Carbon Nanomaterials for Next-Generation Interconnects and Passives: Physics, Status, and Prospects,'' *IEEE Trans. Electron Devices*, vol. 56, no. 9, 2009, pp. 1799-1821.

[12] Prashant Kumar, Arun Singh, Anshul Garg and Rohit Sharma, "Compact Models for Transient Analysis of Single-Layer Graphene Nanoribbon Interconnects." *15th International Conference on Computer Modelling and Simulation (UKSim)*, pp. 809-814, April, 2013.

[13] A. Naeemi and J. D. Meindl, "Conductance modeling for graphene nanoribbon (GNR) interconnects," *IEEE Electron Device Lett.*, vol. 28, no. 5, pp. 428–431, May 2007.

[14] M. S. Sarto and A. Tamburrano, "Comparative analysis of TL models for multilayer graphene nanoribbon and multiwall carbon nanotube interconnects," in *Proc. IEEE Int. Symp. Electromagn. Compat., Fort Lauderdale, FL*, Jul. 2010, pp. 212–217.

[15] Manoj Kumar Majumder et al, "Comparison of Propagation Delay in Single- and Multi-layer Graphene Nanoribbon Interconnects," *5th international conference on computers and Devices for communication (CODEC)*, 2012.

[16] D. Das and H. Rahaman, "Crosstalk and Gate Oxide Reliability Analysis in Graphene Nanoribbon Interconnects," *International Symposium on Electronic System Design (ISED)*, pp. 182-187, 2011.

[17] J.-P, Cui, W,-S. Zhao, W.-Y. Yin, and 1. Hu, "Signal transmission analysis of multilayer graphene nano-ribbon (MLGNR) interconnects," *IEEE Trans. Electromagn. Compat.* ,vol. 53, no, 4, Nov, 2011.

[18] Narasimha Reddy K. et al, "Optimized Delay and Power Performances in Multilayer Graphene Nanoribbon Interconnects," *Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, pp. 125- 125, 2012.

[19] P. Kapur, J.P. Vittie and K. C. Saraswat, "Technology and Reliability Constrainted Future Copper Interconnects-Part I: Resistance Modelling," *IEEE Transactions on Electron Devices*, vol. no. 49, pp. 590-597, 2002.

[20] Raghunath Murali et al, "Resistivity of Graphene Nanoribbon Interconnects," *IEEE Electron Device Letters,* vol. 30, no. 6, June 2009.

[21] Naushad Alam, A. K. Kureshi, Mohd. Hasan and T. Arslan , "Analysis of carbon nanotube interconnects and their comparison with Cu interconnects," *Multimedia, Signal Processing and Communication Technologies*., pp. 124- 127, 2009.

[22] H. B. Bakoglu and J. D. Meindl, "Optimal interconnection circuits for VLSI," *IEEE Trans. Electron Devices***,** vol. ED-32, pp. 903–909, May 1985.

[23] Mayank Kumar Rai, Nivedita and Sankar Sarkar, "Carbon Nanotube Based Interconnects for VLSI Application," *IE (I) Journal-ET*, vol. 91, pp. 3-6, 2011.

[24] M. K. Rai and S. Sarkar, "Influence of tube diameter on carbon nanotube interconnect delay and power output," *Physics Satus Solidi ,A 298*, No.3, pp. 735-739, 2011.

[25] Sandeep Sharma, Rajeevan Chandel, Pankaj Kr. Pal, Rituraj S. Rathore, "Performance Analysis of CNTs as an Application for Future VLSI Interconnects," *International Conference on Computer Aided Design (ICCAD),* pp. 237- 240, 2012.

[26] Ning Wang, Chris D. English, and Eric Pop "Comparison of Graphene Nanoribbons with Cu and AI Interconnects," *Device Research Conference (DRC),* pp 123 -124, 2012.

[27] M.K. Rai et al, "Control of SWCNT-interconnect Performance by Tube-diameter," *TENCON IEEE Conference*, pp. 23-26, Jan. 2009.

[28] V. Kumar, S. Rakheja and A. Naeemi, "Performance and Energy per–Bit Modeling of Multilayer Graphene Nanoribbon Conductors," *IEEE Transactions on Electron Devices*, vol. 59,no. 10, pp. 2753-2761, 2012 .

[29] Kang, S.M. and Leblebici, Y., CMOS Digital Integrated Circuits, "Analysis and Design," *TMH*, New York, 2003.

[30] Mayank Kumar Rai, Nivedita and Sankar Sarkar, "Carbon Nanotube Based Interconnects for VLSI Application*," IE (I) Journal-ET*, vol. 91, pp. 3-6, 2011.

[31] Online: http://www.stanford.edu/class/ee311/notes/InterconnectScalling.pdf.///scaling of interconnect EE311 notes/Prof saraswat.

[32] Pawan Kapur, James P. McVittie and Krishna C. Saraswat, "Technology and Reliability Constrained Future Copper Interconnects—Part I: Resistance Modeling," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 590-597, April 2002.

[33] Chuan Xu, Hong Li, Banerjee K., "Modeling, Analysis, and Design of Graphene Nano-Ribbon Interconnects," *IEEE Trans. Electron Devices*, vol. 56, no. 8, pp 1567 - 1578, Aug. 2009.

[34] Naushad Alam, A. K. Kureshi, Mohd. Hasan and T. Arslan (2009) "Analysis of carbon nanotube interconnects and their comparison with Cu interconnects," *Multimedia, Signal Processing and Communication Technologies*., pp. 124- 127, 2009.

[35] online: http://people.ccmr.cornell.edu/~cober/mse542/page2/files/Optical-Interconnect.pdf.

[36] Dr. How T. Lin,"optical interconnect and optical interconnect sensing," Endicott Interconnect Technologies.

[37] M. Radosavljevi´c, J. Lefebvre, and A. T. Johnson, "High-field electrical transport and breakdown in bundles of single-wall carbon nanotubes," *Phys. Rev. B, Condens. Matter*, vol. 64, no. 24, p. 241 307, Dec. 2001.

[38] B. Q. Wei, R. Vajtai, and P. M. Ajayan, "Reliability and current carrying capacity of carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, no. 8, pp. 1172– 1174, Aug. 2001.

[39] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[40] F. Li, H. M. Cheng, S. Bai, G. Su, and M. S. Dresselhaus, "Tensile strength of single-walled carbon nanotubes directly measured from their macroscopic ropes," *Appl. Phys. Lett.*, vol. 77, no. 20, pp. 3161–3163, Nov. 2000.

[41] M.-F. Yu, O. Lourie, M. J. Dyer, K. Moloni, T. F. Kelly, and R. S. Ruoff, "Strength and breaking mechanism of multiwalled carbon nanotubes under tensile load," *Science*, vol. 287, no. 5453, pp. 637–640, Jan. 2000.

[42] J. Hone, M. Whitney, C. Piskoti, and A. Zettl, "Thermal conductivity of single-walled carbon nanotubes," *Phys. Rev. B, Condens. Matter*, vol. 59, no. 4, pp. R2 514–R2 516, Jan. 1999.

[43] P. Kim, L. Shi, A. Majumdar, and P. L. McEuen, "Thermal transport measurements of individual multiwalled carbon nanotubes," *Phys. Rev. Lett.*, vol. 87, no. 21, p. 215 502, Oct. 2001.

[44] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Lett.*, vol. 8, no. 3, pp. 902–907, Mar. 2008.

[45] S. Ghosh, I. Calizo, D. Teweldebrhan, E. P. Pokatilov, D. L. Nika, A. A. Balandin,W. Bao, F. Miao, and C. N. Lau, "Extremely high thermal conductivity of graphene: Prospects for thermal management applications in nanoelectronic circuits," *Appl. Phys. Lett.*, vol. 92, no. 15, p. 151 911, Apr. 2008.

[46] P. L. McEuen, M. S. Fuhrer, and H. Park, "Single-walled carbon nanotube electronics," *IEEE Trans. Nanotechnol.*, vol. 1, no. 1, pp. 78–85, Mar. 2002.

[47] H. J. Li,W. G. Lu, J. J. Li, X. D. Bai, and C. Z. Gu, "Multichannel ballistic transport in multiwall carbon nanotubes," *Phys. Rev. Lett.*, vol. 95, no. 8, p. 086 601, Aug. 2005.

[48] K. I. Bolotin, K. J. Sikes, J. Hone, H. L. Stormer, and P. Kim, "Temperature dependent transport in suspended graphene," *Phys. Rev. Lett.*, vol. 101, no. 9, p. 096 802, Aug. 2008.

[49] J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits," 2nd edition, *Prentice Hall*, 2002.

[50] Adler, V. and Friedman, E.G. "Repeater design to reduce delay and power in resistive interconnect," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 45, no. 5, pp. 607-616, 1998.

[51] Adler, V. and Friedman, E.G. "Repeater design to reduce delay and power in resistive interconnects," *IEEE International Symposium on Circuits and Systems*, vol. 3, no. 5, pp. 2148-2151, 1997.

[52] Adler, V. and Friedman, E.G. "Repeater insertion to reduce delay and power in RC tree structures," *Thirty-First Asilomar Conference on Signals, Systems & Computers*, vol. 1, pp. 749-752, 1997.

[53] *Predictive Technology Model*, 2008, [Online]. Available: http://ptm.asu.edu/.

[54] Bakoglu, H.B. and Meindl, J.D., "Optimal interconnection circuits for VLSI", *IEEE Transactions on Electron Devices*, vol. ED-32 no. 5, pp. 903-909,1985.

[55] W. Zhao, Y. Cao, "New generation of Predictive Technology Model for sub-45nm early design exploration," *IEEE Transactions on Electron Devices*, vol. 53, no. 11, pp. 2816-2823, Nov. 2006.

[56] Tapan K Gupta, "Copper Interconnect Technology," *1st ed., Springer*, 2009.

[57]Online:http://tfp1.physik.unifreiburg.de/teaching/Seminar2010/talks/LandauerFormula_Presentation110510.pdf.

[58] S. H. Nasiri,M. K. M. Farshi, and R. Faez, "Stability analysis in graphene nanoribbon interconnects," *IEEE Electron. Device Lett.*, vol. 31, no. 12, pp. 1458–1460, Dec. 2010.

[59] Hong Li, Wen-Yan Yin, Kaustav Banerjee and Jun-Fa Mao, "Circuit Modeling and Performance Analysis of Multi- Walled Carbon Nanotube Interconnects," *IEEE Transactions on Electron Devices*, vol. 55,no. 6,pp. 1328-1337, 2008 .

[60] International Technology Roadmap for Semiconductors (ITRS) reports, 2006. [Online]. Available: http://www.itrs.net/reports.html .

[61] H. Kempa and P. Esquinazi, "Field-induced metal-insulator transition in the c-axis resistivity of graphite," *Phys. Rev. B*, vol. 65, pp. 241101-1–241101-4, 2002.

Appendix 1

1.1 Simulation parameters used for 22 nm technology node.

Table A.1. Simulation parameters used for the calculations [59]

Simulation Parameters	Local and intermediate	Global
V_{dd}	0.7V	0.7V
Width (W)	22 nm	32 nm
A/R(aspect ratio)	2	3
Thickness (H)	44 nm	96nm
Copper resistivity	6.01	4.2
Oxide thickness(t_{ox})	76.8nm	76.8nm
ε_{OX}(relative dielectric constant)	2.05	2.05