

Study and Design of Double-Gate Junctionless MOSFET structures

A

Dissertation

Submitted in the partial fulfillment of the requirements for the award of the degree

of

MASTER OF TECHNOLOGY

in

VLSI DESIGN

Submitted by

Saurabh Kala

Roll no. 601461024

Under the Guidance of:

Mr. Arun Kumar Chatterjee

Assistant Professor, ECED



ELECTRONICS AND COMMUNICATION ENGINEERING

DEPARTMENT


THAPAR UNIVERSITY

PATIALA – 147004 (INDIA), June, 2016

DECLARATION

I hereby declare that the dissertation titled "**Study and Design of Double-Gate Junctionless MOSFET Structures**" in the partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI DESIGN submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out as under the guidance of **Mr. Arun Kumar Chatterjee** (Assistant Professor, ECED) during 2014-2016.

Date: 15/07/16


(Saurabh Kala)


Roll No-601461024

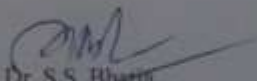
It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Date: 15/07/2016

Arun Kumar Chatterjee
Mr. Arun Kumar Chatterjee
Assistant Professor
Thapar University,
Patiala

Counter signed by:


Dr. Sarjaj Sharma
Head
E.C.E. Department
Thapar University, Patiala


Dr. S.S. Bhatta
Dean of Academic Affairs
Thapar University, Patiala

ACKNOWLEDGEMENT

This report has only been possible with the constant guidance and expertise of **Mr. Arun Kumar Chatterjee, Assistant Professor**, Electronics and Communication Engineering Department, Thapar University, Patiala and I would like to take this opportunity to express my sincere gratitude to him.

I am thankful to our Head of Department, **Dr. Sanjay Sharma** as well as **PG Coordinator, Dr. Amit Kumar Kohli** and **Program Coordinator Dr. Anil Arora, Assistant Professor, ECED**, the entire faculty and staff of Electronics and Communication Engineering Department.

I am also thankful to **Mrs. Madhu Chatterjee**, for her regular guidance and support throughout this dissertation work.

Also a big thank you to friends, family, colleagues and seniors who devoted their valuable time and helped in every way possible towards the completion of this report.

Saurabh Kala

Roll No. 601461024

ABSTRACT

In bulk MOSFET, the problem is occurrence of short channel effects as we reduce the size of the MOSFET. One of the remedies of the issues due to scaling is modification of device structures such as Silicon on insulator (SOI) based, Double gate (DG), Multi gate (MG), Fin field effect transistor (FINFET) structures. These devices help in reducing the short channel effects of the bulk MOSFET. SOI (Silicon on insulator) based devices reduce most of the leakage mechanism such as DIBL, GIDL, drain to body leakage current etc. The multi gate structure provides better controllability of the gate voltage over drain current. The problem with multi gate MOSFETs is ultra sharp doping profile between source (drain) and body region which poses a great challenge for proper operation of high speed and low power MOSFET operation. To overcome this problem, Double gate Junction-less MOSFET can be utilized.

Here, a comparative study of different nano scale JL MOSFET structures have been done. For this three JL MOSFETs have been studied. The first device structure (JL1, with uniform doping throughout the source, drain and body), the second one is (JL2, without source and drain extension), the third one is (JL3, with source and drain extension having uniform doping different from the doping of the body).

The transfer characteristics for these devices show that the drain current for uniformly doped double gate JL MOSFET (JL1) decreases at high voltage as compared to other two devices. Further due to uniform doping at the source and drain extension, there is a series resistance which further causes decrease in drain current. It has been found that with increase in gate voltage (V_{GS}), the potential at the middle of the silicon film is found higher than the potential at the surface which indicates higher accumulation of electrons at the center as compared to surface. In the second device (JL2), the centre potential is found much higher than JL1 which gives a much higher drain current. Though sub-threshold slope is increased slightly but still remains near to ideal. In the third device (JL3), the centre potential is further increased but its SS slope remains the same as JL2. Further the CMOS inverter circuit utilizing these three NMOS devices (JL1, JL2, JL3) has been simulated on TCAD tool and comparison of VTC curve has been

done. It is found that the high noise margin is much improved in JL3 as well as the transition time is much less than other two device structures.

The Visual TCAD version 1.8 tool is used for validating the results.

TABLE OF CONTENTS

Declaration	i
Acknowledgement	ii
Abstract	iii
Table of Contents	iv
List of Acronyms	Vi
List of Figures	Vii
List of Tables	Viii

Chapter: 1 Introduction **1-15**

1.1	Background	1
1.2	Technology scaling	2
	1.2.1 Why MOSFET Scaling?	3
	1.2.2 Moore's Law	3
	1.2.3 CMOS Scaling Trends	4
	1.2.4 Challenges to Miniaturization of MOSFETs	7
1.3	Current CMOS Device Technology	11
	1.3.1 Double gate FET structures	13
	1.3.2 Double gate junction-less FET	14
1.4	Organization of the Dissertation Work	15

Chapter: 2 Literature Survey **16-22**

2.1	Junction-less MOSFET	18
2.2	Review of Double Gate Junction-less (DG JL) MOSFET	20
2.3	Gaps in Literature Survey	22

Chapter: 3 Proposed Objective and Methodology **23-24**

3.1	Objective	23
3.2	Methodology	24

Chapter: 4 Results and Discussion	25-33
4.1 Transfer characteristics	25
4.2 Distribution of Electric Potential at the surface and center with Different Values of V_{GS} for JL1	28
4.3 Distribution of potential difference at surface and center of the film for different channel doping at $V_{GS}=0.2V$ and $V_{DS}=0.4V$	29
4.4 Distribution of potential difference and electron concentration at mid channel length for different channel doping at $V_{GS}=0.2V$ and $V_{DS}=0.4V$	30
4.5 VTC curve for different CMOS inverter designed by using three type of JL MOSFET	31
Chapter: 5 Conclusion and Future Work	34
5.1 Conclusion	34
5.2 Scope for future work	34
References	35
Originality Report	

ACRONYMS

IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complimentary Metal Oxide Semiconductor
ITRS	International Technology Roadmap for Semiconductor
SCE	Short Channel Effect
SOI	Silicon On Insulator
FET	Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
SS	Subthreshold Slope
PD-SOI	Partially Depleted SOI
FD-SOI	Fully Depleted SOI
DG JL MOSFET	Double Gate Junctionless MOSFET
DG MOSFET	Double Gate MOSFET

LIST OF FIGURES

Figure 1.1: Moore' Law [2]	4
Figure 1.2: Simplified demonstration of scaling of Si technology by part α	5
Figure 1.3: Reduction of barrier for the majority of carriers to enter the channel	6
Figure 1.4: Scaling movement of power supply voltage (V_{dd}), gate-oxide thickness (T_{ox}) and threshold voltage (V_{th}), as a consequence of CMOS channel length[4]	7
Figure 1.5: DIBL effect in short channel MOSFETs	9
Figure 1.6: Magnitude of carrier velocity in inversion layer vs. magnitude of longitudinal component of electric field[9]	10
Figure 1.7: Hot electron carrier effect in a region of high longitudinal electric field in inversion channel of MOSFET	11
Figure 1.8: Conventional Bulk CMOS cross sectional [5]	11
Figure 1.9: PD SOI CMOS cross –section [5]	12
Figure 1.10: Cross-sectional view of FD-SOI[5]	13
Figure 1.11: Double-gate MOSFET[5]	14
Figure 2.1: Structural view of double gate junction-less MOSFET	21
Figure 3.1: Double gate junction-less MOSFET	23
Figure3.2: Methodology	24
Figure 4.1: Double Gate Junction-less MOSFET	25
Figure 4.1(a) Transfer characteristics for 3 different symmetrical DG JL MOSFET in linear scale	26
Figure 4.1(b) Transfer characteristics for 3 different symmetrical DG JL MOSFET in logarithmic scale	27
Figure 4.1(c) Potential difference between source and drain for different structure at drain voltage of 1V	27
Figure 4.2(a) Potential along the surface for different value of gate voltage	29

Figure 4.2(b): Potential along the center for different value of gate voltage	29
Figure 4.3: Potential difference at the center and surface for different doping	30
Figure 4.4(a): Potential at the mid gate along the silicon film thickness	30
Figure 4.4(b): Electron concentration at mid gate along the silicon film thickness	31
Figure 4.5(a): CMOS inverter circuit	32
Figure 4.5(b): VTC curve for CMOS inverter of device JL1,JL2,JL3	32

LIST OF TABLES

Table 1.1: Main outcome of abnormal current	28
Table 1.2 Noise margins for different devices	33

1. Introduction

1.1 Background

The integrated circuit (IC) is the prime component of semiconductor electronics which is a combination of basic elements of electronic circuits i.e transistors, diode, capacitors, resistors on single semiconductor substrate. Transistors and memory devices play an important part of silicon electronics. MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) is used for logic applications. For ICs ,MOSFET have been the major component for past two decades. For the semiconductor chips to have better data processing and memory functions, the best choice for this is a silicon MOSFET based VLSI circuits which provides enhancing gain in performance and reduction in cost with the change in technology and scaling phenomena of device[1].

For several decades, as predicated by Moore' law[2] The semiconductor industry witnesses that the number of transistors per integrated circuits is increasing exponentially. Due to relentless progress in silicon based CMOS technology ,There is hugely evolution of electronics, (IT), and communications. Dimensional scaling is the main reason for this continuous progress. CMOS scaling technology is the main driving force for improving both device density and performance. With every new technology generation, The cost-per-function is reducing which increasing the economic efficiency. Besides scalability, There are other unique properties such as a zero static power dissipation ,simple layout, process steps, input resistance and self isolation which made the CMOS transistors a foremost components of current integrated circuits(ICs). Today CMOS ICs plays an important role in our daily life, vary from telecommunications to portable electronics and transportation. Over the last thirty years, lot of research is done in field of device design but now due to evolution of process technology brings new challenges and opportunity to device designers. Dimensional scaling of CMOS is required within the next decade in order to consider the trend predicted by ITRS (International Technology Roadmap for Semiconductors)[3], electrostatic limitations, physical dimensions faced by fabrication technologies and conventional process. For the 21st century ,as the device scaling continues, it came to consideration that the circuit density is doubled by historical growth and 40 % increase in performance with every

technology generation irrespective of Moore's Law which consider only conventional scaling theory. When CMOS technology scaling enters the sub micron region ,various serious problems come into play like short channel effects(SCEs) or the small geometry effects. Some of these effects are such as a difficulty in increasing on current, increase leakage currents, discrepancy in parameter, low yield and reliability and manufacturing cost increases etc.

In order to solve the problems to decrease the small geometry effects and sustaining historical improvements, a new device have been explored and launched. Some of the examples includes continuous A high -k /metal gate stack with continuous EOT scaling, a multiple gate MOSFET structures, Strained Silicon(S-Si) , a Si nanowire/carbon nano tube FET, etc. Many of these device have the quality to have approving device properties and current device characteristics and it requires newly fabrication technique. These device have the potential to revolutionize the traditional CMOS technology and acts as the better substitute in future technology.

1.2 Technology Scaling

Basically the device lateral dimension and interconnects are reduced. This reduction is basically called the scaling of the device. The minimum feature size(gate length or interconnect line width) is the smaller size of the object on IC. Over the past decades , the MOSFET is continuously scaling down(in channel length) specially in several micrometer but in today technology, MOSFET are scaling down upto tens of micrometer. Due to this minimum feature size (channel length), the no of transistors are increasing day by day[4]. The pace for MOSFET development is maintained by semiconductor industry by using a "roadmap", ITRS. Historically, with decreasing in the size of the MOSFET, the fabrication process becomes difficult, there is a need of very low voltages and circuit redesign is required for enhancing electrical performance(small MOSFETs having higher leakage currents, lower trans-conductance, process variations, low output resistance and a interconnect capacitance)

1.2.1 MOSFET Scaling

Several reasons are available for high desirability of small size MOSFET. The basic reason to make transistors small in size is to combine more and more no of transistors in a given chip area. This result in chip having same functionality in little area or chip having more functionality in the same area. Basically the fabrication cost related to semiconductor wafer remains fixed. How many chips per wafer that can be produced is basically the deciding factor for cost of integrated circuits. So due to this smaller ICs allow more number of chips per wafer, thereby reducing the price per chip. For the past three decades, due to new technology node introduction ,for every 23 years the number of transistors on the chip is doubling. For example the microprocessor made on 45nm technology have more no of transistor as compared to 65nm technology. Gordon Moore in 1965 first observed this doubling of transistors and is called Moore's law[2]. It is also come to know that small transistors switch faster. In order to have high speed devices, scaling of device is done. The various parameters which are scalable are channel width, channel length, and oxide thickness. They have to be scale down by the same factor in order to have no change in channel resistance but there is decrease in gate capacitance by same factor. However ,decrease in transistors size does not relate to higher chip speed because interconnections delay is more significant.

1.2.2 Moore's Law

Since 1965,the cost of 1 bit semiconductor memory is reduced by 100 million times. The miniaturization is the primary engine which powered rapid increase in spreading of electronics. In order to make circuits smaller. the transistors and interconnects are made smaller so that more circuits are fabricated on each silicon wafer. Miniaturization is the main factor for improvements in power consumption and speed in ICs. Gordon Moore made an statement in 1965 that every 18 or 24 month ,the no of devices on chips doubles and as shown in fig.1.1[2]. Each time, a new technology node or technology generation is introduced if minimum line width is reduced. Every 2 to 3 years, a new technology node is introduced. Since twice as device are fabricated on a single chip which basically reduced the cost per ICs.

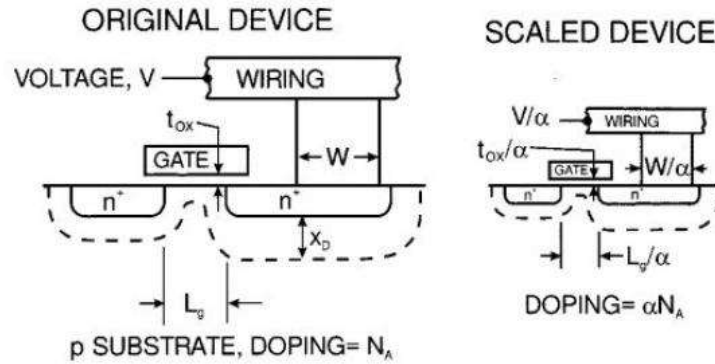


Figure 1.2: Simplified demonstration of scaling of Si technology by part α

Scaling of device is based on simple principles; performance, speed and power of the transistor is improved and also decreasing the interconnect density and size of the devices.

Device scaling predominantly depends on

- a) Scaling of supply voltage
- b) Scaling of threshold voltage
- c) Scaling of gate oxide thickness

Supply voltage of the device is to be decrease in order to have lesser power consumption under control environment. The threshold voltage of the device is also be scale down in order to have high drive current and performance. Source-body and drain-body depletion width are basically presumably based on doping due to which as we decrease the channel width ,the barrier height decreases as shown in fig 1.3[4]. Due to which threshold voltage decreases. Basically in short channel transistors, barrier height therefore threshold voltage mainly depends on drain voltage.

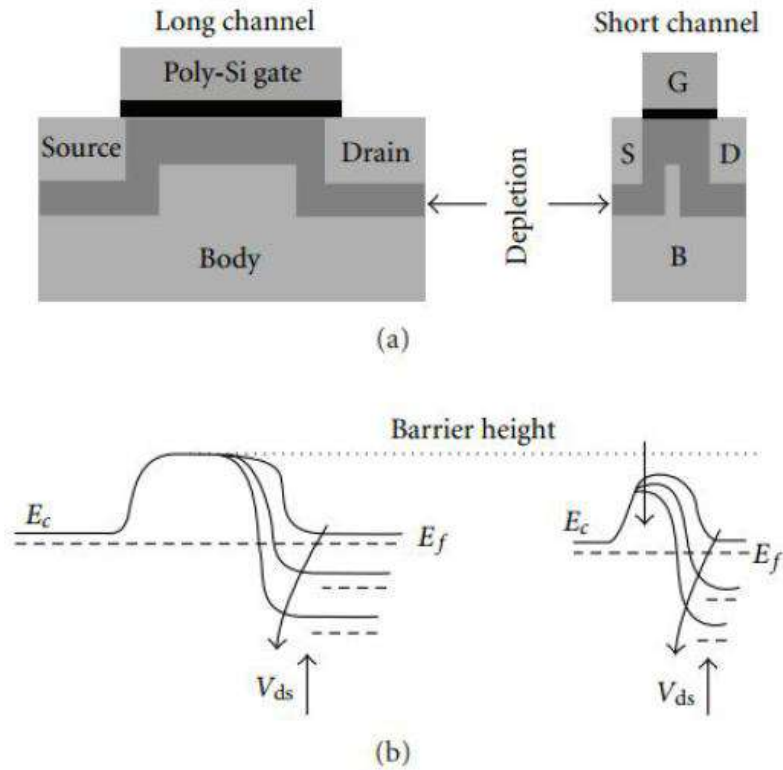


Figure 1.3: Reduction of barrier for the majority of carriers to enter the channel

Fig. shows that as we increase the drain voltage, the barrier height decreases. As we scale down the device, there is a decrease in oxide thickness of the device due to which there is transistors current and therefore increase in switching speed. fig. shows the graph is plotted channel length versus supply voltage & gate oxide thickness. As shown in fig1.4[4]. as we decrease the CMOS channel length ,the supply voltage does not decrease a comparable with oxide thickness .It is due to the win-win situation between leakage current and speed of the circuit.

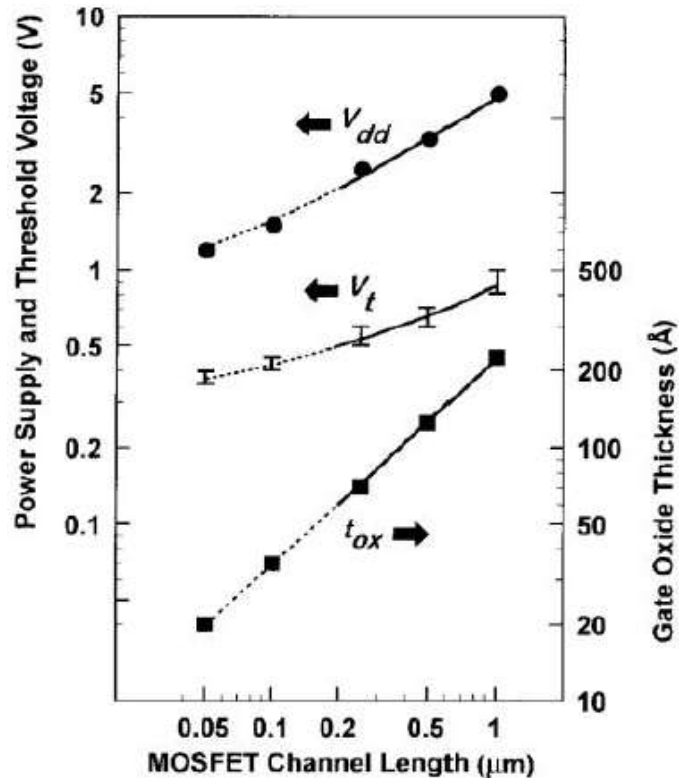


Figure 1.4: Scaling movement of power supply voltage (V_{dd}), gate-oxide thickness (T_{ox}) and threshold voltage (V_{th}), as a consequence of CMOS channel length[4]

Doping and charge density has to be increased as we decrease all dimensions and voltages by a factor α . The technology scaling rules are defined in table. α is used as the dimensional scaling factor, ϵ is used as the electric field scaling factor and α_d and α_w are the dimensional factor for different case.

1.2.4 Challenges to Miniaturization of MOSFETs

Basically this section discusses some of the difficulties facing in miniaturization and how new class of devices are helpful in solving these problems[5].

a) Larger electric fields:

If the bias voltage is applied over a short distance, it may cause avalanche breakdown due to which there is a knocking of large number of electrons from the semiconductor which increases the current and can cause damage to the devices. This type of problem occurs in nano scale devices made from bulk semiconductor.

b) Heat dissipation:

Basically the problem of heat dissipation occurs due to non availability of heat sink in the devices. this problem is further increases as device size is decreases and it limits the density of nano devices in circuits.

c) Vanishing bulk properties:

This problem can be overcome by not doping at all. Instead take the help of quantum mechanical effects. Also regular array are formed using dopant atoms.

d) Decrement of depletion regions:

Decrement of depletion regions may lead to quantum mechanical tunneling of carriers from source to drain when the device is switched off.

e) Decrement and disproportionation of the thin oxide layer below the gate:

The oxide layer prevents the electrons to leak out from gate to drain but small devices leakages electrons due to thin spots in the devices, due to tunneling effects.

Short channel effect due to the scaling of device dimensions are as follows[6]:

a) Drain induced barrier lowering (DIBL) and punch through:

When the depletion region towards the drain side extends to the source side depletion region so that the two depletion region merge, punch through occurs. It can be minimized by using thinner oxides, shallower junctions, large substrate doping, to add halo implants at source and drain junctions and using a longer channel. In order to have the current flow, there is a need of inversion layer formation under the gate region. If the voltage applied to gate is not sufficient to invert the surface ($V_{gs} < V_{T0}$), due to which electrons in the channel face the potential barrier that block the flow of the current. In order to have the current flow through the channel, the gate voltage across the channel is to increase. In short channel MOSFET, the potential obstruction is controlled by gate voltage (V_{gs}) and drain voltage (V_{ds}). If we increase the drain voltage, the potential barrier across the channel reduces. This phenomena is called Drain Induced Barrier

lowering (DIBL). This reduction eventually allows electrons flow from source to drain even if the voltage across gate is less than threshold voltage (V_{th}). This flow of current under the conditions ($V_{gs} < V_{th}$) is called sub-threshold current.

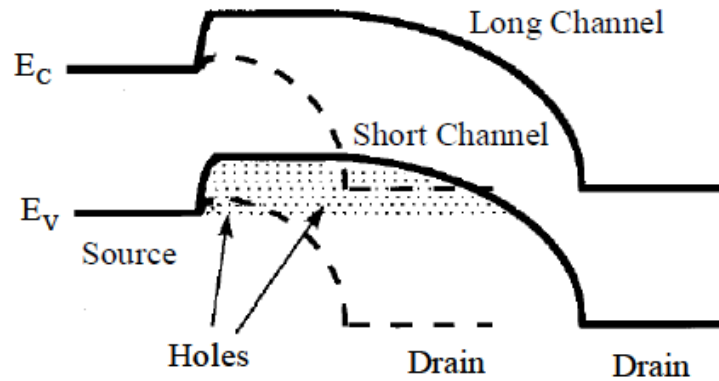


Figure 1.5: DIBL effect in short channel MOSFETs

b) Surface Scattering: Due to the sideways expansion of depletion layer into the channel region, the channel length becomes smaller so due to which the vertical electric field component E_v enhances and surface mobility becomes dependent of field. The area of inversion layer becomes narrow and scattering across the surface (electrons collided with interface when they are accelerating towards the interface) causes decrease in mobility, due to which electrons move with difficulty across the interface. So due to this, the mean mobility for small values of E_v becomes half in comparison to bulk mobility.

c) Velocity Saturation: The transconductance of the device reduces in the saturation mode which effect the performance of short channel devices. This effect is called velocity saturation. At low vertical electric field E_v , the drift velocity increases linearly with the electric field intensity in the channel. As the vertical electric field increases above the value of 10^4 V/cm, the drift velocity increases very slowly and proceeds towards a value of $V_{de}(sat) = 10^7$ cm/s around $E_v = 10^5$ V/cm at 300K. This problem is associated with short channel devices having dimensions being scaled without scaling biasing voltages.

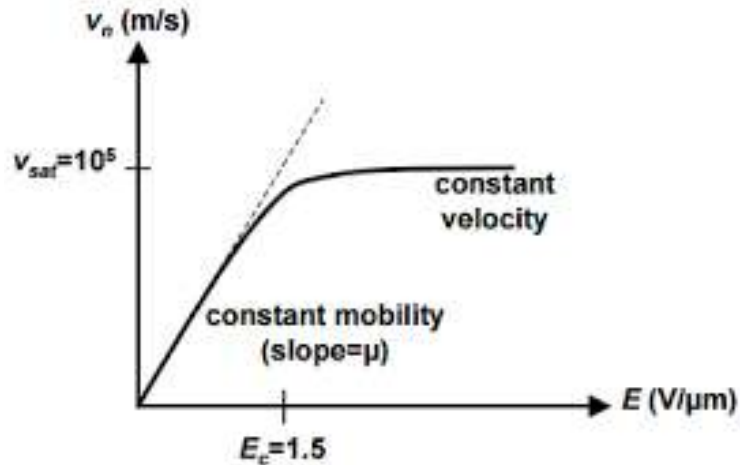


Figure 1.6: Magnitude of carrier velocity in inversion layer vs. magnitude of longitudinal component of electric field

d) Impact Ionization: One more short channel effect specially occur in NMOS causes high speed of electrons due to high horizontal electric field that causes generation of electron-hole(e-h) pairs. This effect is called impact ionization. This is basically making collision with silicon atoms and ionizing them. After that, most of the electrons flow to the drain and holes flow to the substrate forming the substrate parasitic current. If the mentioned holes around the source create a potential drop of 6 V, reversed bias p-n junction across source-substrate will conduct. Due to which some electrons travelled through the substrate. They can have enough energy to create e-h pairs. Problem is that if these electrons bypasses the drain electric field and enters the substrate, it effects the functioning of other devices on the chip .

e) Hot Electrons: One more effect related to high electric field is called hot electrons. These electrons of high energy enters the oxide and traps inside it. These electrons increases with time thereby causing oxide charging. So due to which there is a degradation in performance of device due to increase in V_{th} and reduces of gate control on drain current.

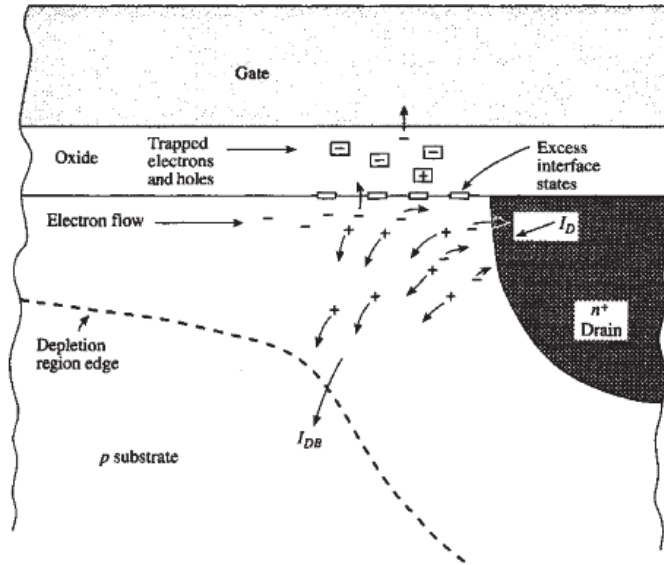


Figure 1.7: Hot electron carrier effect in a region of high longitudinal electric field in inversion channel of MOSFET

1.3 Current CMOS Device Technology

Important improvements is to be made in order to decrease the short channel effects in bulk MOSFETs happening due to scaling. The gates are of type n- and p- polysilicon, and are covered with a metal silicide, which lowers the series resistance of the gate.

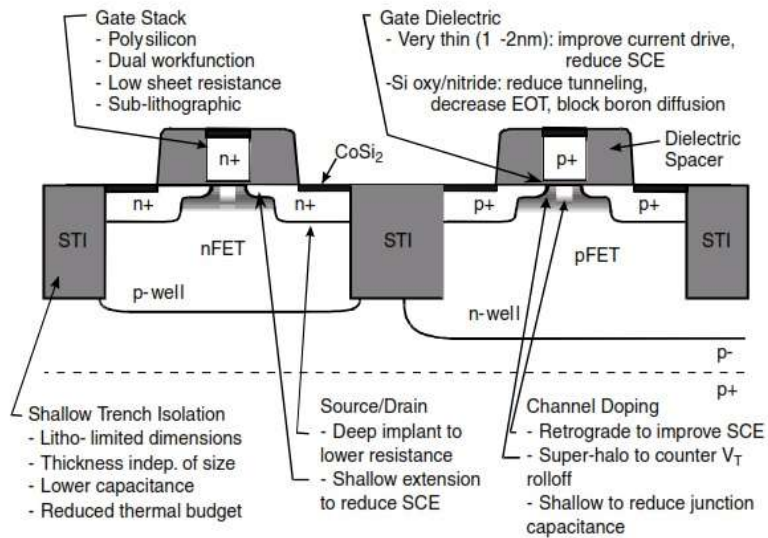


Figure 1.8 Conventional Bulk CMOS cross sectional [7]

Scaling requires these thin gate insulators in order to have low short channel effects and to increase performance, but tunneling leakage current flowing through these thin insulators is one of the disadvantage for many applications. Shallow trench isolation (STI) is used to separate the FETs, which resulted in high circuit density[7][8][9]. In order to prevent degradation of insulator of gate due to hot electrons and to reduce short channel effects, the combination of deep and shallow implants are to be perfectly engineered which are used for the source and drain. Partially depleted SOI CMOS is similar to bulk CMOS but the main difference is that PD-SOI MOSFET[10] is made in the thin silicon layer on the top of the insulating layer. In PD-SOI MOSFET, the depletion region is thinner as compared to the silicon layer due to which some undepleted silicon acts as the floating body for the device. The buried oxide (BOX) layer insulates the device layer from the substrate. This construction results in source- and drain-to-body junction capacitances that are significantly reduced, which can increase digital switching speed.

Due to floating body effect, the dependencies of bulk MOSFET body effect on source to substrate voltage eliminates.

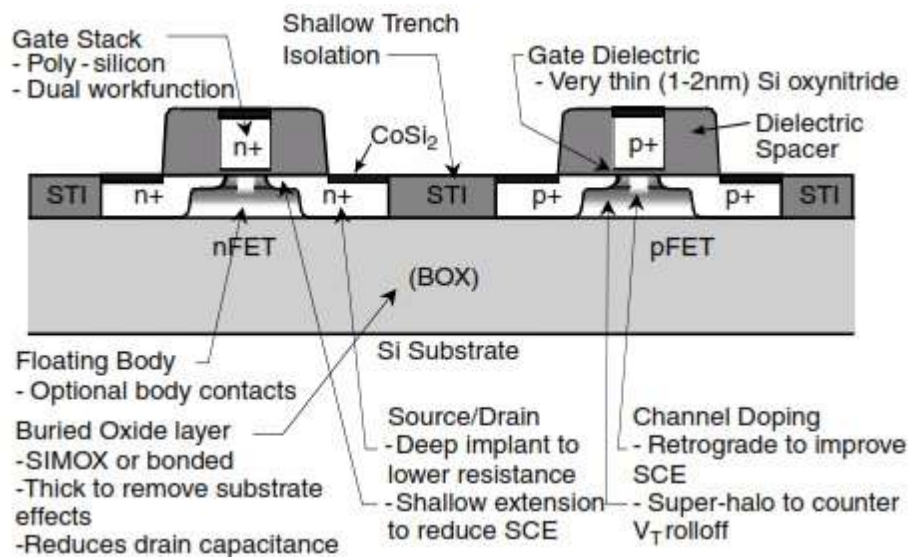


Figure 1.9 PD SOI CMOS cross –section [7]

Another more complex device approach is fully depleted SOI(FD-SOI) MOSFET. The difference between FD-SOI and PD-SOI MOSFET is that the silicon layer is thinner in FD-SOI as compared to PD-SOI MOSFET. In order to have the layer to remain fully depleted and full control on short channel effects, the layer should be half of the depletion depth of bulk MOSFET. The elimination of floating body effect, easy circuit design and drain capacitance reduction are some of the advantages of FD-SOI MOSFET over PD-SOI MOSFET.

There is a difficulty to control the thickness of thin silicon layer which leads to difficulty in controlling the threshold voltage(depends on the silicon thickness)and difficulty in achieving low resistance at source and drain contact for thin silicon layer in the case of FD-SOI MOSFET[14]. The latter problem can be solved by raising the source/drain process. There is another problem associated with PD-SOI MOSFET is that self heating of the device due to lower thermal conductivity of silicon oxide. Due to generation of heat in drain of MOSFET, this causes heating of the device due to which the mobility decreases.

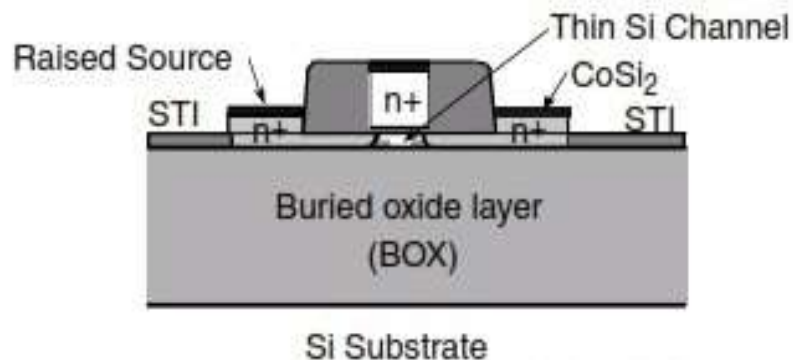


Figure 1.10 Cross-sectional view of FD-SOI [7]

1.3.1 Double gate FET structures A double gate MOSFET consists of two gates ,one on either side of the channel. The second gate is used to control the drain field and body of the MOSFET. Due to presence of two gates in double gate MOSFET, the short channel effect remain under control but the second gate can be used together with the first gate in order to double the switching current of the device. It is possible to scale DG MOSFET

more than the bulk MOSFET because the silicon layer of the device can be made thinner as compared to the depletion layer. Thus gate length can be scaled to smaller value[15]. The capacitor divider effect is negligible in DG MOSFET when we use a device with both gates switched together but this effect occurs in bulk devices between gate and body

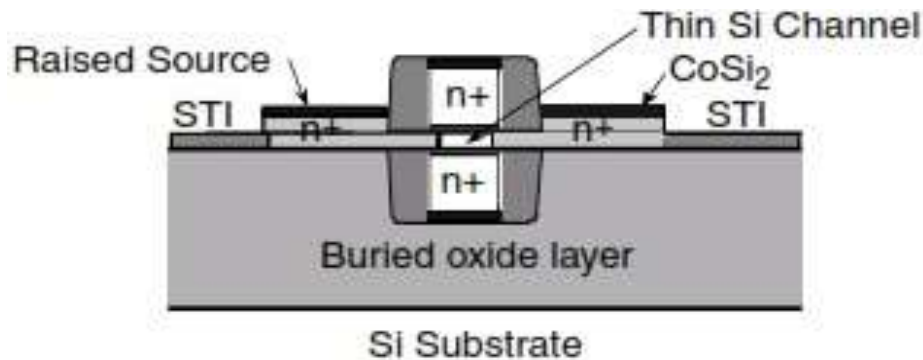


Figure 1.11 Double gate MOSFET [5]

1.3.2 Double gate junction-less FET

In order to solve the problem related to short channel effects, a device is introduced which having uniform doping from source to drain and there is no form of junction which occurs in double gate MOSFET. These device have low leakage current and simple fabrication process as compared to conventional bulk MOSFET . But due to high doping concentration in the channel , it causes reduction in carrier mobility which results in low current and trans-conductance of JL MOSFETs[16].

1.4 Organization of the Dissertation Work

Chapter i, ii describes This chapter describes the Moore's law and discuss the scaling of the MOSFET, the challenges and its remedies in form of advance MOSFET. It also discusses the short channel effects in the bulk MOSFET and how to overcome these effects. It also tells about different JL MOSFET as described by the author and also working principle of JL MOSFET and what are the research gaps in the literature survey. Chapter iii discuss about the different JL MOSFET structure and what are the different simulation done in order to define parameter variations. Chapter iv, v contains the comparison of three different JL devices simulation results from cogenda's TCAD tool and there parameter variations. It also describes the brief conclusion and improvements needed in order to better functioning of the device.

2. Literature Survey

In order to understand the evolution of integrated electronics and its developments in present day, it is first essential to understand the basic concepts of MOSFET, its history that led to the development of MOSFETs. The basic functionality of MOSFET, its different region of operation and qualitative approach of the device is studied. These paper discusses about the various characteristics of the device plotted between device current and various voltages of the device in linear and logarithmic scale. The capacitance generated between different device region and their effects is studied[1].

Proper understanding of the device gave us the idea of integrating these devices on the single wafer thereby increasing the integrity. This helps in reducing the area required for transistors in the chip doubles every 24 months but after a certain time, it is proved practically that it doubles every 18 months[2].

Basically the idea of integrating the large no of devices on the single chip leads to the idea of scaling. Scaling is the process of reducing the dimensions, supply voltage and other parameters in order to increase the integrity of the device. scaling is done on various parameters. The scaling on various parameter leads different type of scaling[3][4].

Scaling of the device leads to the reduction the dimension of the device thereby reducing the channel length, width and other parameters of the device. these reduction of parameters lead to the short channel effects which are studied[6]. These effects the performance and reliability of the device and they give the undesired results. the prominent short channel effect is leakage current. It is the current that flows in the device in the weak inversion region[8]. These leakage currents arrive due to different mechanism which need to be studied so that their reduction technique can be studied.

There are various reduction technique used to compensate these leakage current in conventional bulk MOSFET[12]. These reduction techniques can be classified on the basis of use of new materials, well engineering and circuit reduction techniques [13]. In

order to solve the problem, a new architecture is to be introduced where the architecture of the device is changed from the simple bulk MOSFET.

The new architectural devices have slight fabrication changes than that of the bulk MOSFET. These devices are Silicon on Insulator, Double Gate and multiple Gate FET structures . A brief study of these devices is being done to have an overview of these devices, their functionality, their operation, and their advantages over the conventional bulk MOSFET. These devices help in reducing the short channel effects of the bulk MOSFET. SOI improves the short channel effects by the removal of the body terminal of the bulk MOSFET, instead it has a buried oxide layer (BOX). Removal of the body reduces most of the leakage mechanisms such as DIBL, GIDL, drain to body leakage current et.al. SOI is basically categorized as Partially Depleted SOI (PD SOI) and Fully Depleted (FD SOI). The categorization of these SOIs is done on the basis of the thickness of the silicon layer compared to that of the depletion layer thickness. PD SOI has a small body region which may act as a floating terminal if not grounded. This floating body terminal gives rise to kink effect which deviates the current mechanism from its intended characteristic behavior. These kink effect is absent in FD SOI due to the absence of the body terminal [14][15].The further modification of the SOI gives rise to Double Gate MOSFET having two gates one front gate and one back gate. Due to the presence of the two gates it provides better controllability of the gate voltage over the threshold voltage (V_t). Thus increasing the number of gate terminals around the channel increases the gate controllability over V_t . This concept gives rise to the idea behind Multiple Gate FET structures and FIN-FETs .The short channel effects are present in great extent in these devices.

Therefore ,to reduce the short channel effects, a new device is introduced called Junction-less (JL) Transistors .This device having the uniform doping along the whole channel region and source/drain region to overcome the challenges face by the conventional nano devices. These device have low leakage current and simple fabrication process as compared to conventional bulk MOSFET[16] . But due to high doping concentration in the channel , it causes decrease in carrier mobility which results in low current and transconductance of JL MOSFETs. Now, in JL MOSFET as we reach the high gate

voltage, there is a reduction in drain current in saturation region. This occurs because as we have S/D implantation, it reduces the series resistance but at the same time, increases parasitic capacitance thereby causing a delay in a circuit. This problem can be solved by using JL MOSFET with source/ drain junction having non-uniform doping and also using a JL MOSFET transistors without the S/D extensions.

2.1 JUNCTIONLESS MOSFET:

1) **WuMeile, JinXiaoshi , ChuaiRongyan, LiuXi, and Jong-HoLee[16]** : In this paper, author describes the characteristics of Short Channel Double-Gate(DG) Junction-less(JL) FETs by device simulation. Threshold voltage and sub-threshold slope variation due to variations of body doping, body thickness and channel length are analyzed. As we decrease the channel length for both devices, there is a decrease in threshold voltage of both devices but the change in V_t for JL MOSFET is less as compared to IM MOSFET which lead to the conclusion that smaller channel has lesser impact on JL MOSFET as compared to IM MOSFET. Sub-threshold slope is used to define the speed of the device to open. Smaller will be the value of the SS, fast the device open. With decrease in channel length, SS increases. Smaller channel length have less impact on SS of JL MOSFET as compared to IM MOSFET. The threshold voltage of IM MOSFET is larger as compared to JL MOSFET because in JL MOSFET, there is require majority carriers to form the channel but in the case of IM MOSFET , the inversion layer formed is made of minority carriers, due to which more the doping concentration, more the voltage is required to deplete the carriers in order to form the inversion layer. With increase in drain voltage, SSs of the device increases but influence of SS of V_{ds} is smaller in JL MOSFET as compared to IM MOSFET. Conclusion obtain from these variation leads to more advantage of Junction-less MOSFET as compared to conventional MOSFET because the impact of channel length and V_{DS} on JL FETs is small as compared to conventional FETs.

2) **Mukta Singh Parihar and Abhinav Kranti[17]** : In this paper, author discusses the demand of higher channel doping($>10^{19} \text{ cm}^{-3}$) in Junction-less(JL) double gate MOSFETs. It is shown that moderately doped(10^{18} cm^{-3}) ultra low power(ULP) JL transistors achieve better as compared to heavily doped devices. In moderately doped

devices , the carriers are spread out across the entire film but in heavily doped devices, it is concentrated at the centre of the film. This increases the controllability of the gate in order to have high on-off current ratio and lower delay for sub-threshold logic applications. It also reduces the threshold voltage sensitivity to change in parameters of the devices. For the depletion of the channel, the gate work function requirement is reduced to below 5eV.

3) Elena Gnani, Antonio Gnudi , Susanna Reggiani, and Giorgio Bacarani[18] : In this paper, the electrical properties of junction-less(JL) MOSFETs are modeled. The motivation related to analytical model proposed to provide physical understanding of device behavior. In this work, authors describes the device with ideal sub-threshold slope and excellent on-current while having a lesser electron mobility due to the impurity scattering. The most important limitations of JL MOSFETs are device variability and parasitic source/drain resistances. The ideal sub-threshold slope, small DIBL and large electron mobility together with the simplified manufacturing process makes the junction-less MOSFETs as the possible candidate for the future technology. On the other hand, the value of impurity concentration cannot increase above $3 \times 10^{18} \text{ cm}^{-3}$ in order to have proper threshold voltages and good contact resistance.

4) Thomas Holtij, Mike Schwarz, Alexander Kloes and Benjamin Iniguez [19]: In this work, a two dimensional model is described in order to calculate potential in the junction-less MOSFETs valid in sub-threshold region. The comparison with 2D TCAD simulation found to be in accuracy with the 2D model. It is proved that threshold voltage is heavily effected by channel length and applied drain voltages. the threshold voltages also decreases if the doping concentration is above $1 \times 10^{19} \text{ cm}^{-3}$. Also decreasing the channel length effect the DIBL more as compared to increasing the doping concentration.

5) Mukta Singh Parihar, Dipankar Ghosh, and Abhinav Kranti [20]: In this work, double gate junction-less MOSFETs is liken with underlap DG MOSFETs for ULP(Ultra low power) applications. JL devices exhibit least reactivity to gate length as compared to inversion mode and underlap MOSFETs. The performance of the device depends on film thickness, gate oxide thickness, and doping .JL MOSFETs shows least sensitivity to gate length so they can be useful for ULP sub-threshold operation.

6) Chi-Woo Lee, Adrien Borne, Isabelle Ferain, Aryan Afzalian, Ran Yan, Nima Dehdashti Akhavan, Pedram Razavi, and Jean-Pierre Colinge[21]: The authors discuss the temperature dependence of main electrical parameters of junction-less MOSFETs. The threshold voltage and on-off current variation is analyzed. The JL MOSFETs have large variation of temperature as compared to inversion and accumulation mode MOSFETs. The drain current of JL MOSFETs increases as temperature increases.

7) Ming-Hung Han, Chun-Yen Chang, Hung-Bin Chen, Jia-Jiun Wu, Ya-Chi Cheng, and Yung-Chun Wu[22] : The characteristics and design of bulk JL MOSFETs is compared with SOI JL MOSFETs. The bulk MOSFETs exhibit a good on-off current ratio and better short channel characteristics by reducing the channel thickness. It is less sensitive to channel thickness as compared to SOI MOSFETs. The threshold voltage of bulk MOSFETs can easily be varied by substrate doping concentration.

2.2 Review of Double Gate Junction-less (DG JL) MOSFET: The scaling of channel length is a difficult process as short channel effect and leakage current increase due to less control of gate over channel. In MuGFET, the gate electrode is wrapped along the silicon film forming the multi-gate structure having better control of the channel providing full depletion of the channel. The formation of source and drain junctions in short channel devices provide quite a tough challenge and it points out the condition on doping techniques and thermal budget. The JL is basically a resistor with uniform doping. It has the constant doping from source to drain[16].

Due to the absence of doping concentration gradient, there is an elimination of diffusion of impurities and sharp doping profile formation problem. The introduction of double gate junction-less MOSFET is the best device for future technology node[16][18]. All the undoped and lightly doped double gate MOSFETs are of the same type as junction-less MOSFET if the doping of the channel is of the same type as of source and drain. The junction-less MOSFET is different because the doping in the channel is high as similar to that of source and drain. The junction-less MOSFET having high concentration of impurity within the source, channel and drain does not require junction and has advantages such as having the easy fabrication process, ideal sub-threshold

slope($SS=60\text{mV/dec}$), high on-off current ratio($I_{on}/I_{off}> 10^7$), small DIBL and low S/D series resistance. It has the property of bulk conduction instead of surface conduction. Fig 2.6 shows the structure of double gate junction-less MOSFET.

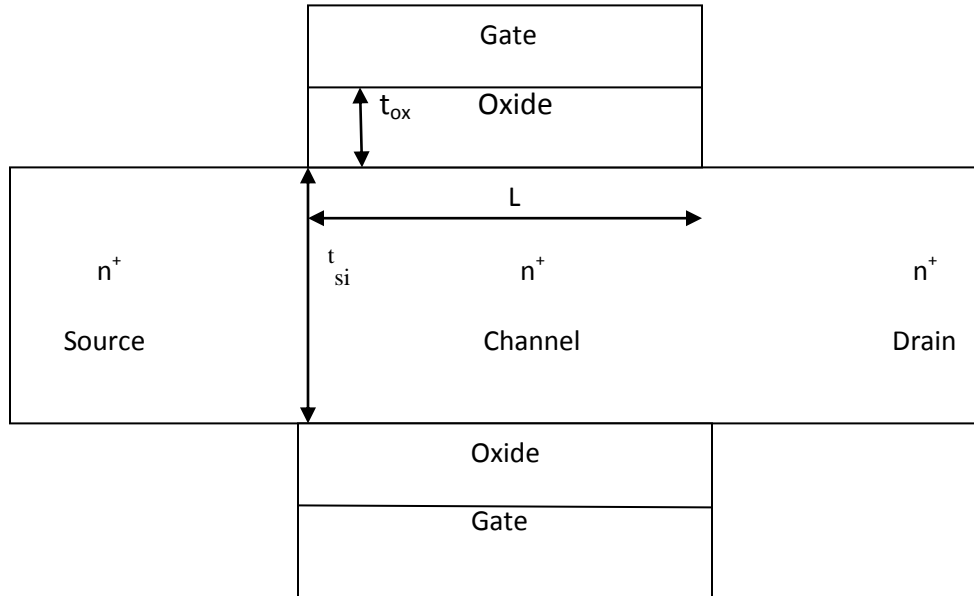


Figure 2.1 Structural view of double gate junction-less MOSFET

The operation principle of double gate junction-less MOSFET is different from double gate FET. In the sub-threshold region, there is a high electric field due to depletion of heavily doped channel. Increasing the gate voltage causes reduction in electric field, due to which there is a formation of neutral region in the center of the channel. So we can define the threshold voltage of the device because there is a gap for electron to flow in the channel. Further increasing the gate voltage causes reduction in depletion region in the channel so due to which the channel becomes fully neutral. The voltage at which this occurs is called flat band voltage. Further increasing the gate voltage causes formation of a layer of negative charges on the surface which result in surface current which is similar to the current in double gate FET. The surface current flows at higher voltage so mostly current in the JL MOSFETs is bulk current. Instead of regular junction-based devices, the principle of working of double gate JL MOSFET is based on the flow of current in the volume of silicon layer in spite of Si-SiO₂ interface. The doping density of channel is high in order to have higher current densities. On the other hand, in order to OFF the devices, the channel needs to be depleted which is difficult when doping concentration is larger.

2.3 Gaps in Literature Survey:

From the literature review it has been observed that the field of “MOSFET Devices” has been emerging a lot in the past many decades. The bulk MOSFET ruled the industry for many decades until it became difficult to scale the device to the nanometer regime in order to follow Moore’s law and obtain high performance and low voltage characteristics due to prevailing short channel effects and limitations of scaling. To overcome these problems many techniques were designed to reduce the leakage currents. New device structures or advance MOSFETs have been designed such as SOIs to have an advantage over these problems of bulk MOSFETs in terms of short channel effects and scalability issues. Recent developments have been made to develop devices having better gate controllability in short channels such as DOUBLE GATE MOSFETs, GATE ALL AROUND MOSFETs, and FINFETs.

Therefore ,to reduce the short channel effects, a new device is introduced called Junction-less (JL) Transistors .This device having the uniform doping along the whole channel region and source/drain region to overcome the challenges face by the conventional nano devices. These device have low leakage current and simple fabrication process as compared to conventional bulk MOSFET . But due to high doping concentration in the channel , it causes decrease in carrier mobility which results in low current and trans-conductance of JL MOSFETs.

In spite of these developments there are still some gaps left which need to be discussed and resolved to increase the device performance.

- In JL MOSFET as we reach the high gate voltage, there is a reduction in drain current in saturation region. This occurs because as we have S/D implantation, it reduces the series resistance but at the same time, increases parasitic capacitance thereby causing a delay in a circuit.
- In JL MOSFET , the switching characteristics obtained from the simulation is not accurate.
- Self heating and increased S/D capacitance leading to increased power density per chip in Double Gate JL MOSFET degrades its performance.

3. Proposed Objective and Methodology

3.1 Objective

Basically the problem with the double gate junction-less MOSFET having uniform doping from source to drain is the abnormal reduction in drain current in strong inversion region when gate voltage reaches a high voltage. This is basically due to the high series resistances in the uniformly doped source and drain. The large part of the voltage drop across the extended S/D, due to which the voltage obtained at the drain contact is low. This can be shown by the potential difference between S/D contact.

In order to solve this problem, the double gate junction-less MOSFET with non uniform doping of source and drain are introduced. Due to extra implantation of doping in source and drain, the series resistance decreases and there is a increase in current at the higher gate voltage.

The proposed objectives for this work are

- A) To study and simulate three different type of double gate junction-less MOSFET i.e
- 1) A device having uniform doping (N_D) throughout the source, drain & body,
 - 2) A device having uniform doping throughout source and drain (N_{Dext}) different from body doping (N_D),
 - 3) A device without having source, drain extensions,

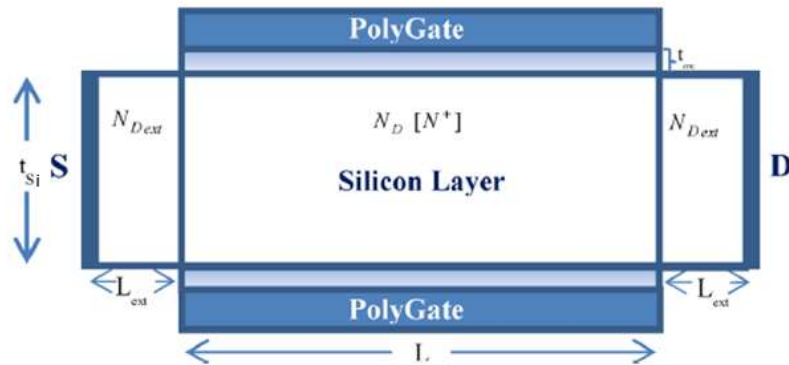


Fig.3.1 Double gate junction-less MOSFET

- B) To compare the different characteristics of these devices i.e I_d-V_{gs} curve, potential curve of the devices along the center and surface of the channel with respect to channel

length with different gate voltages , change in current, threshold voltage and sub-threshold voltage for these three devices.

3.2 Methodology

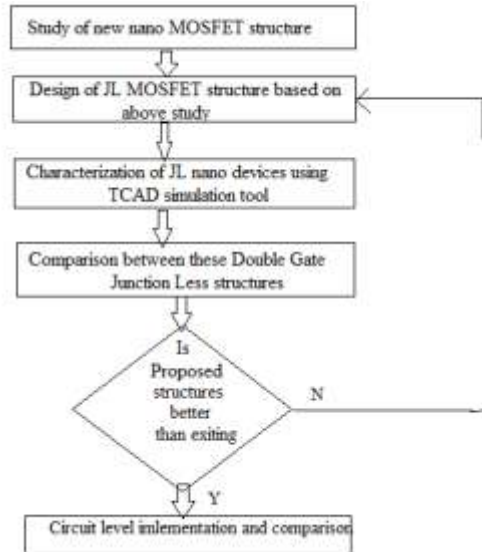


Fig: 3.2 Methodology

4. Results and Discussion

To show the effect of doping concentration at the extended S/D, two dimensional TCAD simulation is done. A traditional drift diffusion approach is used for the simulation process. The maximum electron mobility considered for the devices is $1000\text{cm}^2/\text{Vs}$. Three JL MOSFET is simulated with the following same parameters i.e channel length $L=50\text{nm}$, silicon layer thickness $t_s=15\text{nm}$ and doping concentration $N_D= 5\times 10^{18}\text{cm}^{-3}$, Tungsten gate work function which varies from 4.54-4.91eV, gate oxide thickness $t_{\text{ox}}=2\text{nm}$ and gate tungsten layer thickness= 8nm .

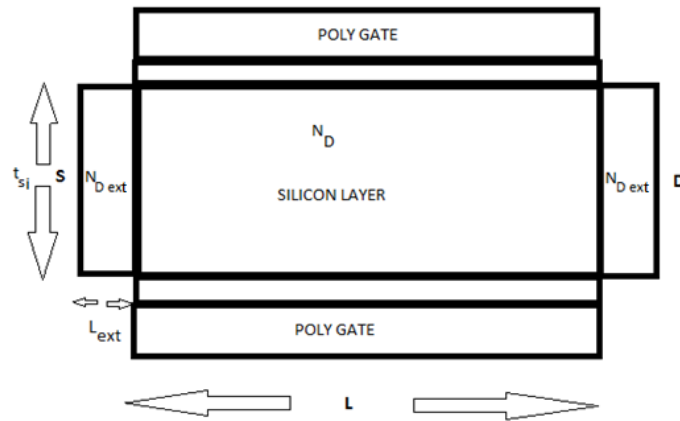


Figure 4.1 Double Gate Junction-less MOSFET

Consider three type of JL MOSFET . JL1 having S/D extensions of 30nm with uniform doping throughout. JL2 having no extension and doping concentration N_D . Third JL3 having extensions of 30nm with the doping concentration of $N_{D\text{ext}}=1\times 10^{20}\text{cm}^{-3}$.

4.1 Transfer characteristics: Fig. shows the distribution of drain current for different JL MOSFET with varying values of V_{GS} from 0.5V to 1.5V. From the graph, it can be shown that the drain current for JL1 reduces at high gate voltages and for JL2 & JL3, the current increases at the high gate voltage.

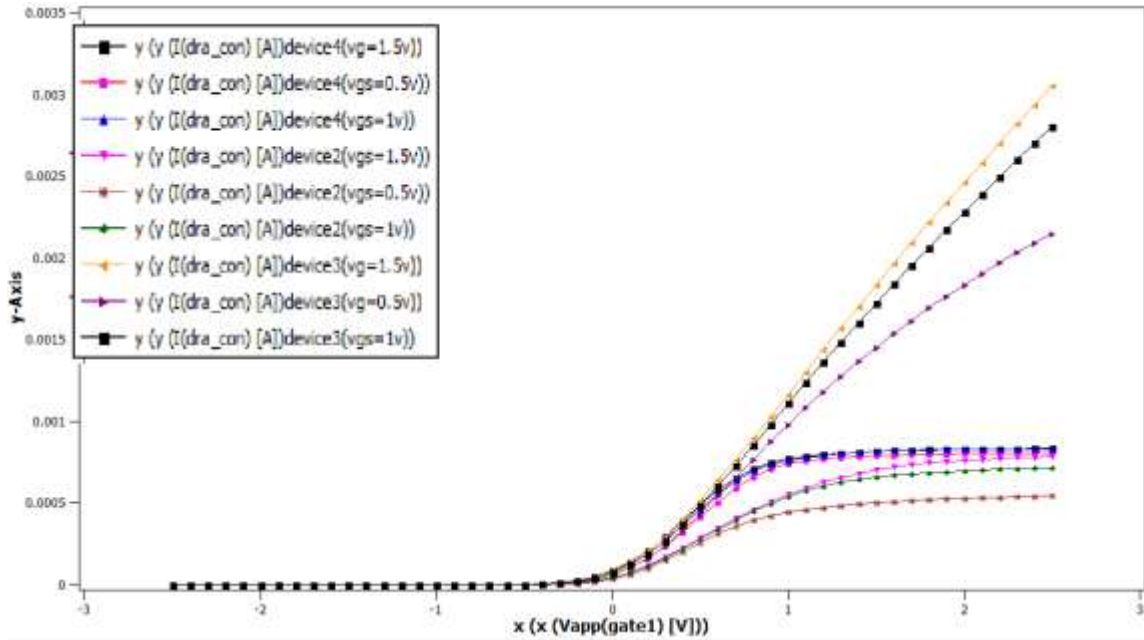


Figure 4.1(a) Transfer characteristics for 3 different symmetrical DG JL MOSFET in linear scale

This problem associated with the JL1 and advantage of JL2 ,JL3 can be understand by plotting the graph between potential difference between S&D for the surface and center V_s applied gate voltage for the drain voltage $V_D=1V$.

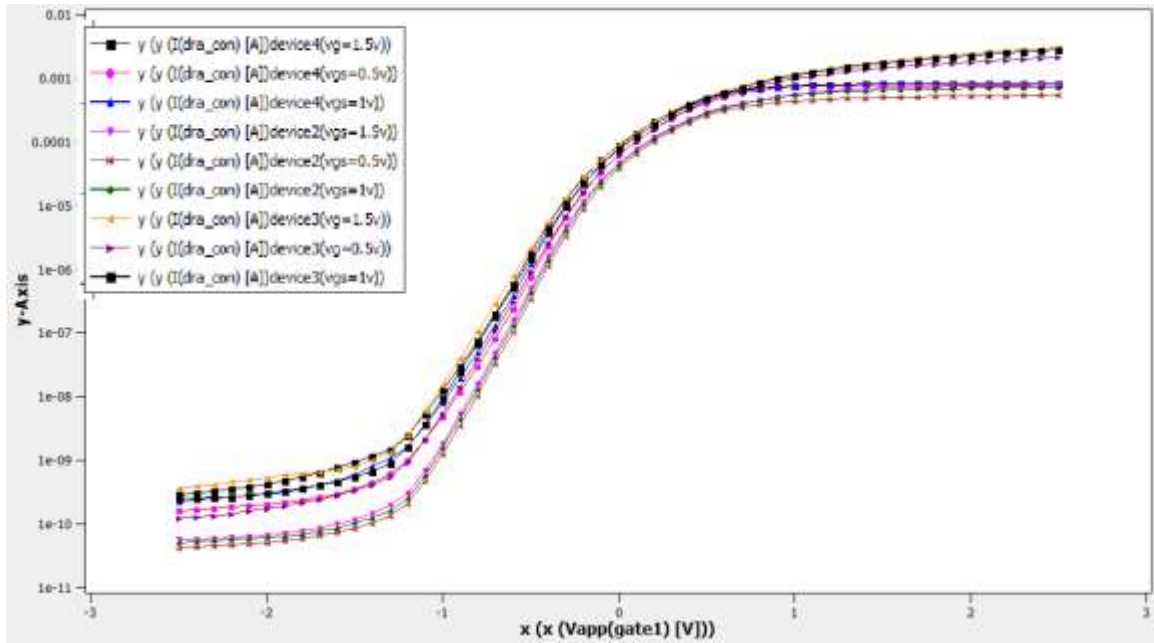


Figure 4.1(b) Transfer characteristics for 3 different symmetrical DG JL MOSFET in logarithmic scale

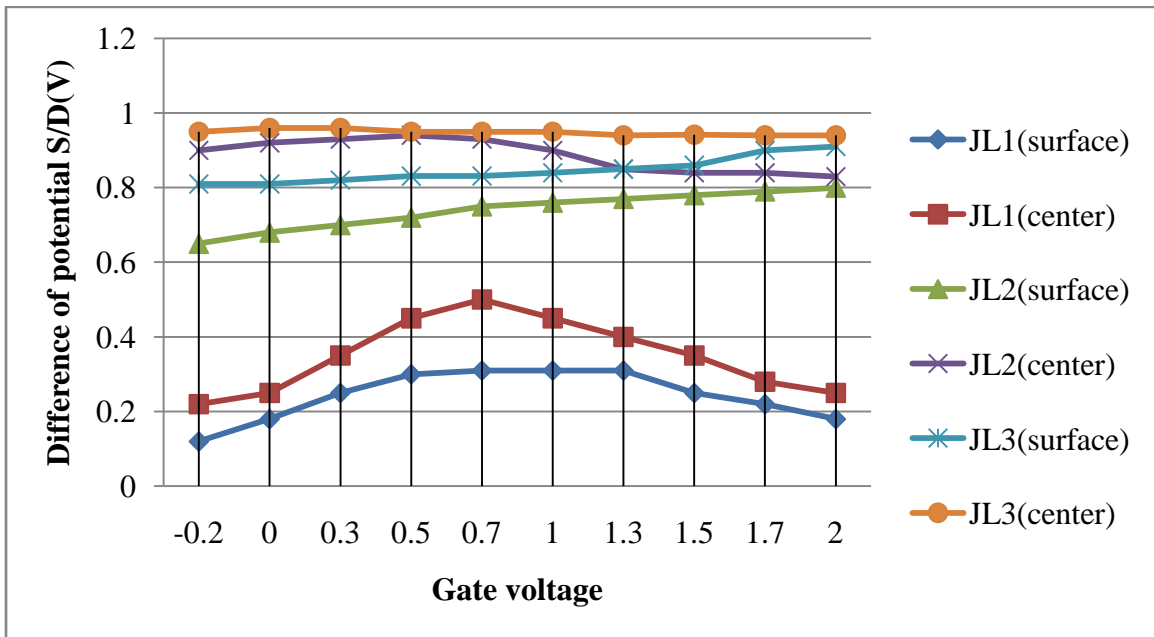


Figure 4.1(c) Potential difference between source and drain for different structure at drain voltage of 1V

From the graph, for JL1 at the gate voltage above 1V (flat band voltage), when the surface current begins to increase but due to reduction in potential at the surface and

center cause the reduction in drain current at high gate voltage. Further due to uniform doping of JL1 at the source and drain extension, there is a series resistance which further causes decrease in drain current . But in case of other two devices, the potential difference increases and also in the case of JL3, there is a non uniform doping of source and drain . Due to which ,the series resistance decreases(R inversely proportional to doping). So there is increase in drain current of the other two devices.

The following observation is made from the graph.

Table 1.1 Main outcome of abnormal current

JL Structure	Current increase w.r.t to JL1 at $V_G=1.5$ V in %	SS mV/dec of current
JL1	-	63
JL2	40	71
JL3	55	71

The current increases for JL2 and JL3 by 40% and 55% and sub-threshold slope varies. The sub-threshold variation can be understand from fig (c). The minimum potential difference at the surface is for JL1,due to which the no of electrons present at the surface is smaller. In order to off the device, we require to deplete the surface so if the no of carrier charge is smaller, more easily device can be turned off. Due to this, sub-threshold slope has better value for JL1.

4.2 Distribution of Electric Potential at the surface and center with Different Values of V_{GS} for JL1: Figures shows the plot between electric potential at the center and surface for different values of V_{GS} . At the smaller gate voltage below sub-threshold region, the highly doped channel is fully depleted, due to which there is high electric field in the channel so as EF increases, potential also increases. At the flat-band voltage, there is a formation of neutral region. Now as increasing gate voltage causes accumulation of

electrons on the surface, due to which there is increase in potential drop on the surface. So due to these factors, the electric potential increases with increase in gate voltage.

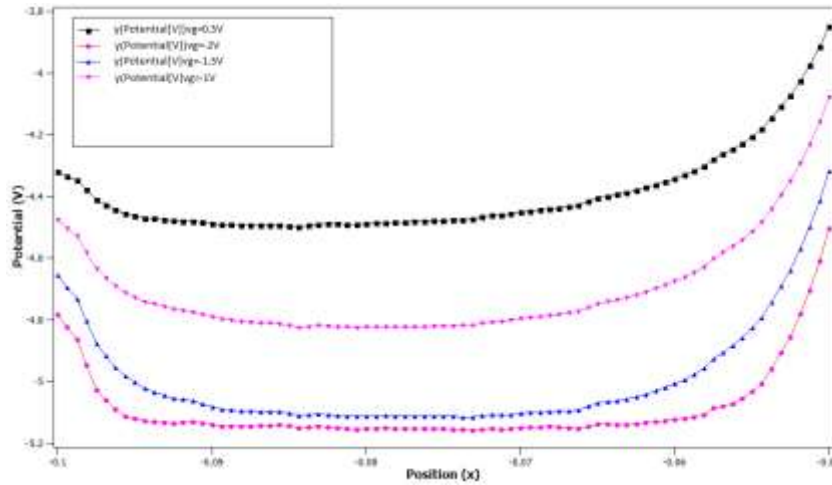


Figure 4.2 (a) Potential along the surface for different value of gate voltage

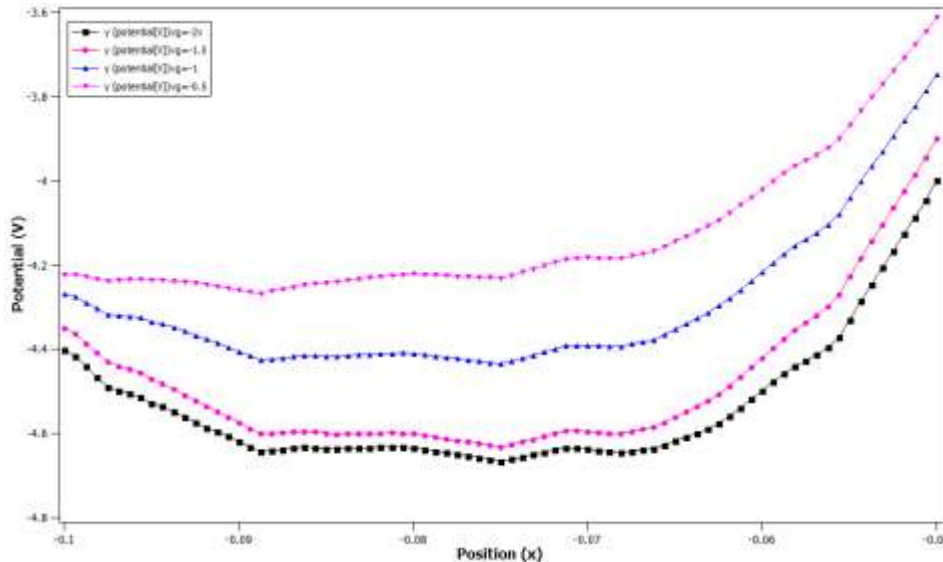


Figure 4.2 (b) Potential along the center for different value of gate voltage

4.3 Distribution of potential difference at surface and center of the film for different channel doping at $V_{GS}=0.2V$ and $V_{DS}=0.4V$:

There is a drop in potential difference between center and surface as the doping decreases from $3 \times 10^{19} \text{cm}^{-3}$ to 10^{18}cm^{-3} . Further decrease in doping does not have effect on potential difference. Inversion does not takes place in JL MOSFET. Above 10^{18}cm^{-3} ,

the current flow in the device through bulk conduction which means current flow through the center of the film. But in the case of doping less than 10^{18}cm^{-3} , the current flows through whole silicon film. Due to which the difference Between surface and center remain constant.

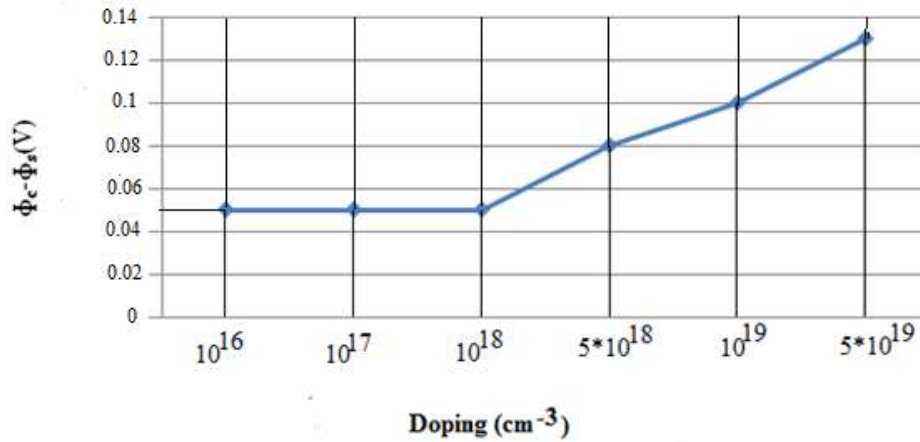


Figure 4.3 Potential difference at the center and surface for different doping

4.4 Distribution of potential difference and electron concentration at mid channel length for different channel doping at $V_{GS}=0.2\text{V}$ and $V_{DS}=0.4\text{V}$:

The graph is plotted for three different value of doping concentration of $10^{18}, 10^{19}, 3 \times 10^{19}\text{cm}^{-3}$ at the same gate and drain voltage. The electrostatic potential is

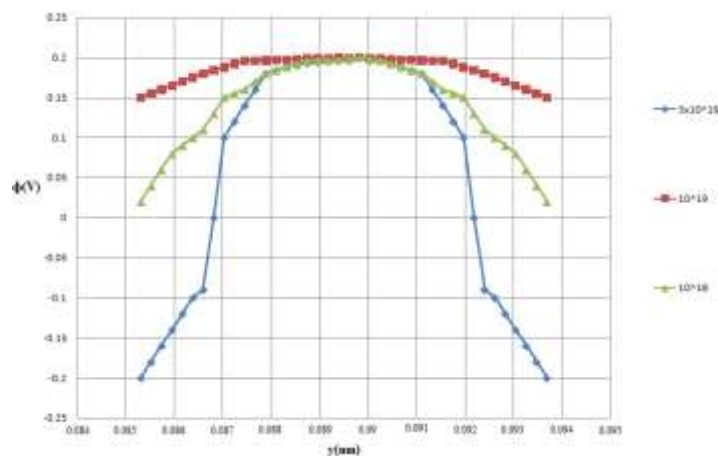


Figure 4.4(a) Potential at the mid gate along the silicon film thickness

larger at the center of channel length but the difference between center and surface decreases with decrease in channel doping because at smaller channel doping i.e $1 \times 10^{19} \text{cm}^{-3}$, the current flow through whole of the film. Also due to which, electron concentration is higher but for channel doping above $1 \times 10^{19} \text{cm}^{-3}$, the current flow through the center of the film due to this, potential is larger and electron concentration is smaller.

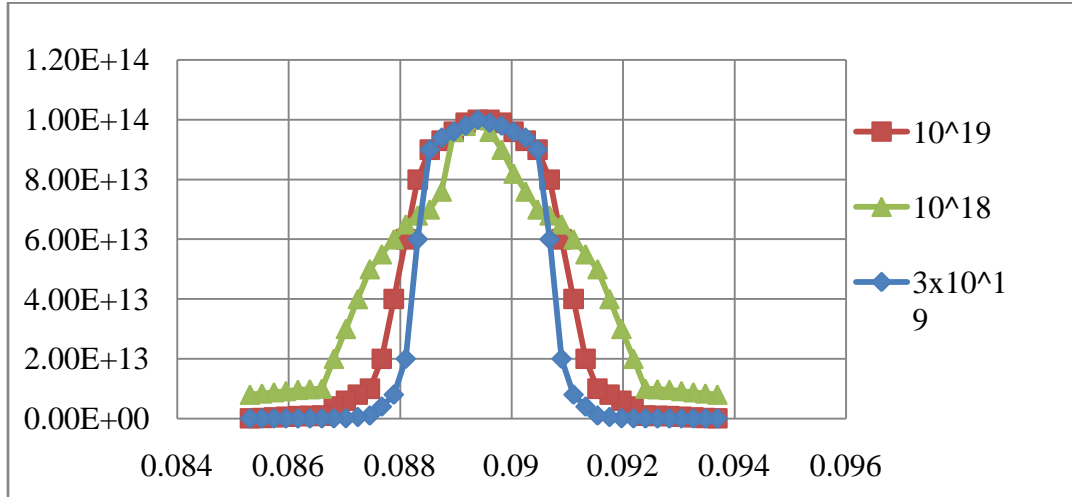


Figure 4.4(b) Electron concentration at mid gate along the silicon film thickness

4.5 VTC curve for different CMOS inverter designed by using three type of JL MOSFET : Consider the 180nm technology for JL MOSFET. Three JL MOSFET is simulated with the following same parameters i.e channel length $L=180\text{nm}$, silicon layer thickness $t_s=20\text{nm}$ and doping concentration $N_D=1 \times 10^{19} \text{cm}^{-3}$, Tungsten gate work function which varies from 4.54-4.91eV, gate oxide thickness $t_{ox}=2\text{nm}$ and gate tungsten layer thickness=8nm.

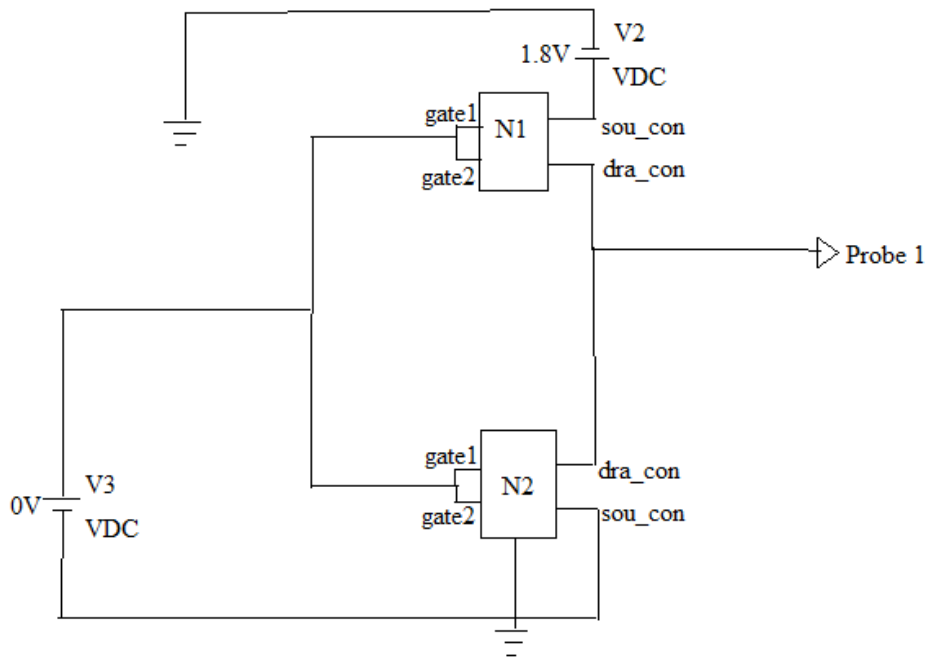


Figure 4.5(a) CMOS inverter circuit

Fig shows the CMOS inverter circuit for obtaining the different VTC curve for different devices. At the input terminal (V3), the dc sweep which varies from -0.6V to 1.8V and drain voltage of 1.8V is given.

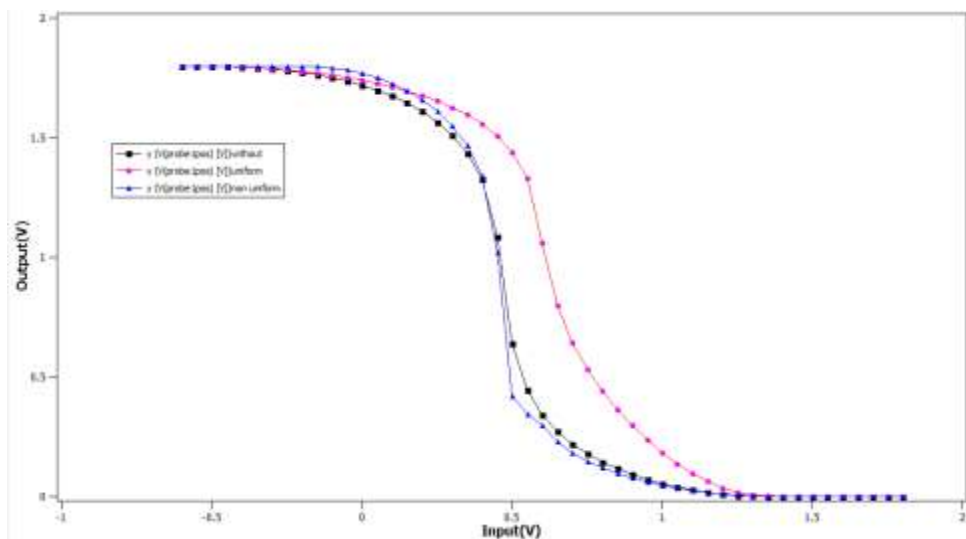


Figure 4.5 (b) VTC curve for CMOS inverter of device JL1, JL2, JL3

From the graph, it come to notice that the plot for JL3 shift to lower value among all the plot. It is basically due to the fact that in JL3 the mobility is smaller of other two devices due to the non-uniform doping .($\mu_{JL2} > \mu_{JL1} > \mu_{JL3}$). From the formula of KR ratio for the symmetric inverter i.e

$$K_R = \mu_n / \mu_p$$

Now, if the mobility is smaller (μ_n & μ_p), the value of K_R increases and it is larger among values of other two devices. Now ,if the value of K_R increases, the graph move towards the left. So this is the reason for the JL3 to shift to lower value.

Table1.2 Noise margins for different devices

Device	V_{IL}	V_{IH}	V_{OH}	V_{OL}	N_{ML}	N_{MH}
JL1	0.4V	1.05V	1.8V	0V	0.4 V	0.75V
JL2	0.2V	0.7V	1.8V	0V	0.2V	1.1V
JL3	0.2V	0.6V	1.8V	0V	0.2V	1.2V

From the table , it come to notice that , the N_{ML} is better for JL1 and N_{MH} is better for JL3.

5 .Conclusion and Future Work

5.1 CONCLUSION

The use of highly doped extensions in JL MOSFET is one of the feasible solution in order to reduce the series resistance and abnormal reduction of drain current at high gate voltage. From the simulation, it can be shown that the highly doped Source/Drain extension double gate JL MOSFET has higher current at larger gate voltage in comparison to uniformly doped double gate JL MOSFET and it can be used in high speed circuits.. The sub-threshold slope of uniformly doped JL MOSFET is smaller compared to other two devices which means that JL1 can be easily turned off as compared to other two devices. From the comparison of VTC curve for three devices, it come to notice that the transition region for highly doped Source/Drain extension double gate JL MOSFET is smaller as compared to other two devices. So this can be used as a fast switching device .

5.3 Scope for Future Work

The following recommendations can be made based on the present work

- 1.The work related to the comparison between different JL devices in terms of transfer characteristics, CMOS inverter can be extended to other multi gate MOSFET.
2. The present work can be extended by considering SCEs and compare among the devices which have the better immunity with respect to these effects.

References

- [1] C. Hu, "Modern Semiconductor Devices for Integrated Circuits", Pearson, 2009
- [2] Moore, G.E. "Cramming More Components onto Integrated Circuits", *Proceedings of the IEEE*, Vol.86, No. 1, pp .82-85, 1998.
- [3] International Technology Roadmap for semiconductors, "Process Integration, Devices and Structures Summary", 2013 Edition
- [4] Scaling and Limitation of Si-based CMOS Gang He, Zhaoqi Sun, Mao Liu, and Lide Zhang
- [5] Overview of Nanoelectronic Devices ,Vivek Venkataraman, EE, IIT Delhi
- [6] Kaushik Roy et. al, "Leakage Current Mechanisms and Leakage Reduction techniques in Deep-Submicrometer CMOS Circuits", *Proceedings of the IEEE*, Vol.91, No. 2, pp. 305– 327, 2003 .
- [7] SOI-CMOS Device Technology Yasuhiro FUKUDA*, Shuji ITO, Masahiro ITO
- [8] Yannis Tsividis, "Operation and Modelling of the MOS Transistor", OXFORD University Press, 2nd Edition, 2008.
- [9] Yannis Tsividis, "mixed analog-digital vlsi devices and technology", World Scientific Publishing Co. Pvt. Ltd. , 1st Edition,2005
- [10] K. K. Young,"Short-channel effects in fully depleted SOI MOSFETs", *IEEE Transaction Electron Devices*, Vol. 36, pp.399 -402, 1989 .
- [11] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 2001.
- [12] R.H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R.Lebanc, "Design of ion-implanted MOSFETs with very small physical dimensions", *IEEE J. Solid-State Circuits*, vol. SC-9,pp.256–268, May 1974
- [13] R. F. Pierret, "Semiconductor device fundamentals", Pearson Education India, 1996.

- [14] Vishwas Jaju, "Silicon on Insulator technology", in *Proc. IEEE Int. SOI Cont.*, 20 pp.23-24, 2002.
- [15] Chaudhry Anurag ,et.al," Controlling Short-Channel Effects in Deep-Submicron SOI MOSFET's for Improved Reliability: A Review", *IEEE Trans. on Device and Materials Reliability* , 2004
- [16] Wu Meile, Jin Xiaoshi, Chuai Rongyan, Liu Xi,and Jong-Ho Lee, *Simulation study on short channel double-gate junctionless field-effect transistors.*
- [17] Mukta Singh Parihar and Abhinav Kranti, "Revisiting the doping requirement
- [18] E.Gnani, A Gnudi, S. Reggiani, G. Bacarani, "Theory of the junctionless Nanowire FET", *IEEE Trans. on Electron Dev.*, 58 (2011) 2903-2910.
- [19] T Holtij, M. Schwarz, A Kloes and B. Iftiguez, "2D Analytical Potential Modeling of lunctionless DG MOSFETs in Subthreshold Region Including Proposal for Calculating the Threshold Voltage",ULIS 2012.
- [20] Parihar M S, Ghosh D and Kranti A 2013 Ultra low power junctionless MOSFETs for subthreshold logic applications *IEEE Trans. Electron Devices* **60** 1540–6
- [21] Lee C-W, Borne A, Ferain I, Afzalian A, Yan R, Dehdashti Akhavan N, Razavi P and Colinge J-P 2010 High-temperature performance of silicon junctionless MOSFETs *IEEE Trans. Electron Devices* **57** 620–5
- [22] Han M-H, Chen H-B, Yen S-S, Shao C-S and Chang C-Y 2013 Temperature-dependent characteristics of junctionless bulk transistor *Appl. Phys. Lett.*
- [23] Y. Taur, D. A. Buchanan, W. Chen, D. J. Frank, K. E. Ismail, S.-H. Lo, G. A. Sai-Halasz, R. G. Viswanathan, H.-J. Wann, S. J. Wind *et al.*, "CMOS scaling into the nanometer regime", *Proceedings of the IEEE*, vol. 85, no. 4, pp. 486–504, 1997
- [24] Arindam Deb Singha, Arun Kumar Chatterjee, "Simulation Study of Process Variations in Double Gate Junctionless field-effect transistors", accepted in *Journal of Semiconductor Devices and Circuits*, STM Journals, June 2015

601461024.docx

by

FILE	601461024.DOCX (1.08M)	WORD COUNT	7798
TIME SUBMITTED	15-JUL-2016 12:10AM	CHARACTER COUNT	40967
SUBMISSION ID	689636161		

601461024.docx

ORIGINALITY REPORT

16%	8%	11%	0%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	ethesis.nitrkl.ac.in Internet Source	6%
2	Frank, David. "Practical CMOS Scaling", Optical Science and Engineering, 2005. Publication	3%
3	Parihar, Mukta Singh, and Abhinav Kranti. "Revisiting the doping requirement for low power junctionless MOSFETs", Semiconductor Science and Technology, 2014. Publication	1%
4	Gnani, Elena, Antonio Gnudi, Susanna Reggiani, and Giorgio Baccarani. "Theory of the Junctionless Nanowire FET", IEEE Transactions on Electron Devices, 2011. Publication	1%
5	CMOS VLSI Engineering, 1998. Publication	<1%
6	Parihar, Mukta Singh, Dipankar Ghosh, and Abhinav Kranti. "Ultra Low Power Junctionless MOSFETs for Subthreshold Logic	<1%