Design and Analysis of All Digital PLL for Multi-Frequency Generator

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Submitted by

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CERTIFICATE

I, Jagdeep Kaur Sahani, hereby certify that the thesis entitled **"Design and Analysis of All Digital PLL for Multi-Frequency Generator"** which is being submitted by me to Department of Electronics and Communication, Thapar Institute of Engineering and Technology, Patiala in fulfillment of the requirement for award of degree of "Doctor of Philosophy". It is a record of bonafide research work carried out under the guidance and supervision of **Dr. Alpana Agarwal, Professor** and **Dr. Anil Singh, Assistant Professor.** The matter presented in this thesis has not been submitted to any university/Institute for award of degree or diploma.

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ABSTRACT

Phase-Locked Loops (PLLs) are necessary building blocks of wireless communications, Soc applications, and biomedical appliances as they are responsible for generating frequencies. The conventional PLL designs employ the LC oscillators, a charge-pump, and low pass filters. Currently, PLL designs must develop accordingly to meet the increasingly demanding requirements imposed on it by today's (and tomorrows) technology. Traditionally, PLL's design flow requires circuit techniques and analog intensive process technologies. PLL's now-days should have low-cost, low-power, improved jitter performance, and reduced noise as imposed by modern technology standards to meet specifications of low power budget and can withstand within the noisy environments of complex system-on-chip (SOC) designs. In addition to it, the low silicon area is another constraint required by the modern demands of VLSI domain. Other than above issues, the conventional PLL design suffers from circuit issues such mismatches, PVT variations, and leakage currents in the nanometer scale of technology. To meet the demands of modern day PLL key requirements, recently digital phase locked loops (DPLLs) with digital methodology and all-digital phased-locked loops (ADPLLs) are preferred over the conventional analog PLL designs especially in nanoscale the CMOS technology. It is due to their configurability, flexibility, scalability, easy portability, and small area. Further digital technology requires a low cost and requires the less design to market time. However, all digital PLL suffers from inadequately more power dissipation due to use of conventional time to digital converter (TDC) and digitally controlled oscillator (DCO) based architectures. Other than these problems, ADPLL also suffers from the quantization noise and periodic jitter issues. In this thesis work, the charge pump PLL is designed using the digital approach. The proposed design achieves low power, low jitter, and fast locking. Further to enhance these parameters, the various ADPLL architectures are proposed. TDC is major source of jitter and power consumption in overall ADPLL design. In this work, 4-bit and 3-bit flash architecture based simple, low power, and low jitter TDCs are proposed. Also in this work, ADPLL-I with 4-bit flash TDC is proposed which achieves power of 6.35 mW and periodic jitter of 6.6 ps. To further enhance the performance parameters, ADPLL-II is designed with 3-bit flash TDC and bang-bang frequency detector. This ADPLL-II architecture achieves the periodic jitter of 1.71 ps and power consumption of 5.9 mW. To achieve a low power and low jitter as compared to ADPLL-I and ADPLL-II, ADPLL-III is designed with background calibration based VCO-II. This design enhances the performance of ADPLL architecture and performance parameters

are improved. This design achieves a low power of 5.3 mW with little increase in the periodic jitter. The achieved periodic jitter is 1.83 ps. The proposed DPLLs and ADPLLs are designed in the SCL digital 180 nm CMOS technology at supply voltage of 1.8 V. These proposed ADPLL designs are suitable for high speed SoCs, battery operated devices, and wireless transceiver applications.

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Jagdeep Kaur Sahani

Dedicated to my Dearest Father

for his endless support, love and encouragement

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LIST OF ACRONYMS

ADC	:	Analog to Digital Converter
ADPLL	:	All digital Phase Locked Loop
AFC	:	Adaptive frequency Calibration
BB-PFD	:	Bang-Bang Phase Frequency Detector
BBPD	:	Bang-Bang Phase Detector
BPFD	:	Binary Phase Frequency Detector
CMOS	:	Complimentary Metal-Oxide-Semiconductor
CP	:	Charge Pump
DAC	:	Digital to Analog Converter
DCO	:	Digitally Controlled Oscillator
DCR	:	Digitally Controlled Resistor
DFC	:	Digital-to Frequency Conversion
DFF	:	D-Flip-Flop
DNL	:	Differential Non Linearity
DIV	:	Feedback Divider
DLF	:	Digital Loop Filter
DPLL	:	Digital Phase Locked Loop
DTC	:	Digital to Time Converter
EDA	:	Electronic Design Automation
FDC	:	Frequency Detection Control
FEC	:	Frequency Error Correction
FIR	:	Finite Impulse Response
FRVCO	:	Feed-forward Ring Voltage Controlled Oscillator
HDL	:	Hardware Description Language
IIR	:	Infinite Impulse Response
INL	:	Integral Non Linearity
LC	:	Inductor Capacitor
LF	:	Loop Filter
LDO	:	Low Dropout Regulator
MOS	:	Metal-Oxide-Semiconductor
PEC	:	Phase Error Correction
PFD	:	Phase Frequency Detector
PLL	:	Phase Locked Loop

PMOS	:	P-type Metal-Oxide-Semiconductor
PVT	:	Process Voltage Temperature
NMOS	:	n-type Metal-Oxide-Semiconductor
RMS	:	Root Mean Square
RTL	:	Register Transfer Logic
SAR	:	Successive Approximation Register
SCE's	:	Short Channel Effects
SoC	:	System on Chip
SS-ADC	:	Analog to Digital Converter
TDC	:	Time to Digital Converter
TSPC	:	True-Single-Phase-Clock
VCO	:	Voltage Controlled Oscillator
VDL	:	Vernier Delay Line

CHAPTER 1

INTRODUCTION

1.1 Motivation

Phase-Locked Loop (PLL) is a primary block of all electronic systems and is used in variety of applications like wireless communication, Internet of Things, and digital system. It is used for clock generation purpose in almost every electronic circuit. The high-performance digital systems use clock to sequence operation, to synchronize between functional units and ICs [1-5]. Each generation of processing technology and processor design have increased rate of data as well as clock frequencies. The proficient and synchronous clocks are designed with help of phase-locked loops (PLLs) and they are distributed on-chip with clock buffers. Internet of Things (IoT) is a concept that focuses on different objects like the devices, machines, and methods of communication using set of the standard protocols. The involving systems work over various diverse networks such as academia, business, and government. With increasing rate of data transfer and communication, there is exponential growth in the internet nodes, the electronic interface is very critical in designing high speed system [6-7]. High-performance PLLs with ultra-low power and low jitter are indispensable to synchronize their clocks at high speed with a hefty amount of data. This leads to development and growth of ultra-low power RF transceivers [1]. The current generation of PLLs consume significant amount of power in serial links and transceivers. But for the IoT operation and for battery operated applications, the power budget is very constrained [6-7]. In extremely scaled CMOS technology, the performance of PLL is constrained by the issues like device leakage and low supply voltage which cause degradation in integrated phase noise and spur levels of the PLLs. The other limitations in conventional design of PLLs are portability, scalability, and process temperature voltage (PVT) variations [6-7]. To overcome these problems, PLLs are designed using all-digital approach. All-digital PLL design can tackle above said issues as well as it gives advantages like easy maintenance of IPs, migration to newer technologies, and lower time to market [6-7]. ADPLL does not need unique devices for high frequency applications. This reduces the cost of chip. The digital blocks replace the bulky analog circuits and thus lead to significant reduction in power and area. ADPLL gives much more flexibility because the parameters can easily be modified according to design requirements. The design cycle is shortened which stimulates innovations, reduces the time to market, and lowers cost for overall systems. An all-digital PLL is favored in the wide range of applications because it gives a benefit of low power, improved jitter, and small area which

are critical parameters in IoT, wireless transceiver, and System on Chip (SoC) applications [1- 7].

1.2 Applications and Specifications of PLL

PLL is employed in a broad range of applications in the modern electronic systems [1-5]. PLL is usually used in wireless transceivers, for generating the reference clock for local oscillator (LO) in a mixer and digital circuits. PLL is also used as frequency synthesizer, jitter cleaner. It is also used for skew inhibition in the clock data recovery circuits [2-4]. The key parameters to evaluate the PLL performance are given below in the Table 1.1.

Table 1.1: Various PLL parameters

Specification List	Unit
Output Frequency	kHz, MHz or GHz
Power Consumption	mW
Tuning Step Size	MHz or kHz
Phase noise	dBc/Hz
VCO gain	kHz/mV
Supply Voltage	V
Chip area	μm^2
Locking Time	μs
Jitter	ps

1.3 Basic Operation of PLL

The block diagram of PLL, as shown in the Fig. 1.1 is a negative control feedback system. The main function of PLL is to generate an output signal with phase and frequency locked onto that of the input reference signal. PLL achieves lock when its output frequency and phase is equal to that of the input reference frequency, or equal to multiple (N) times the reference frequency [9-11]. The primary blocks of PLL are Phase Frequency Detector (PFD), Loop Filter (LF), dividers, and Voltage Controlled Oscillator (VCO). VCO is heart of PLL architectures [8]. The input reference (Clk_ref) and feedback (Clk_fd) (which is generated by voltage controlled oscillator) signals are applied to the PFD. The feedback signal is divided down by a factor of N depending on application requirements. The PFD compares phase and frequency of both signals and produce an up and dn pulses which are proportional to phase and frequency variation. The low pass filter averages the pulses produced by the PFD.

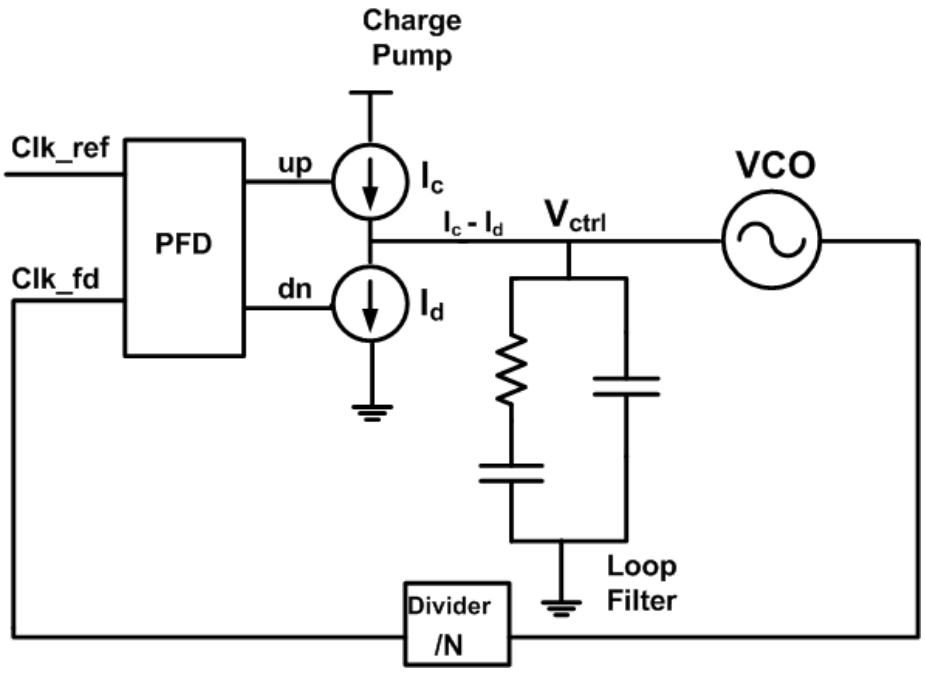


Fig. 1.1 Block diagram of PLL [9-10]

The average value produced from the low pass filter acts as the control voltage for oscillator. Voltage controlled oscillator regulate its output frequency until phase error becomes constant as given by PFD. At this point, the PLL is said to have locked onto the phase and frequency of the input reference signal. The PLL is categorized as given below depending upon the components used in architecture**.**

- Analog Phase Locked Loop (APLL)
- Digital Phase Locked Loop (DPLL)
- All Digital Phase Locked Loop (ADPLL)

1.4 Analog PLL

APLL [9-10] consists of nonlinear analog multiplier which acts as phase detector, loop filter, and the VCO. Both input reference and feedback signals are applied to the input of an analog multiplier and output signal of multiplier is extracted by the low pass filter. The output of the low pass filter varies in proportion to the input phase error between the Clk_ref and Clk_fd. The major problem with APLL is that it suffers from circuit non-idealities such as mismatch and parasitic capacitances [9-10]. APLL uses an analog filter which increases area and power consumption of overall PLL design. The analog filters are bulky and complex in design thus it slowdowns the locking process of APLL. The designing of APLL requires analog processes which cost in terms of design time and money. Further scalability and portability are other issues which restrict the porting of APLL to newer technologies. They

also suffer from PVT spreads and leakage current problems. This architecture is rarely used at the present time due to the following disadvantages:

- The maximum measurable phase error range is ± π/2 rads. This results in a small lock-in range in comparison to those achievable for a DPLL.
- Pull-in range of PLL depends upon the loop filter architecture.
- Frequency detection is not possible. This leads to delay in the locking process.

1.5 Digital PLL

A DPLL [9-11] employs a PFD consisting of logic gates with all other blocks remaining similar to the APLL. There are a range of choices of PFD which exist for this type of phase locked loop. The digital PLL is further divided into two categories: Type 1 and Type 2.

(a) Type 1 PLL: A simple PLL has digital phase detector, loop filter, and VCO. The phase detector (PD) compares the phase difference between the input (Clk_ref) and feedback signal (Clk_fd) [9-10]. Type 1 PLL is first order PLL.

(b) Type 2 PLL: It consists of a current source, current sink, and two switches with inputs directly connected to the outputs of the Phase Frequency Detector (PFD) [9-11]. Phase Frequency Detector consists of D-flip-flops (DFFs), and NAND logic gate. Both the data inputs of the DFFs are tied high and clock inputs are given the input reference and feedback signals. The outputs of the DFFs are denoted as up and dn (down) and are connected via the NAND gate back to the reset input of the DFFs. Fig. 1.2 shows a charge pump and phase frequency detector. The switches control the current from the CP where it is sourced or sinked in proportion to the input phase error.

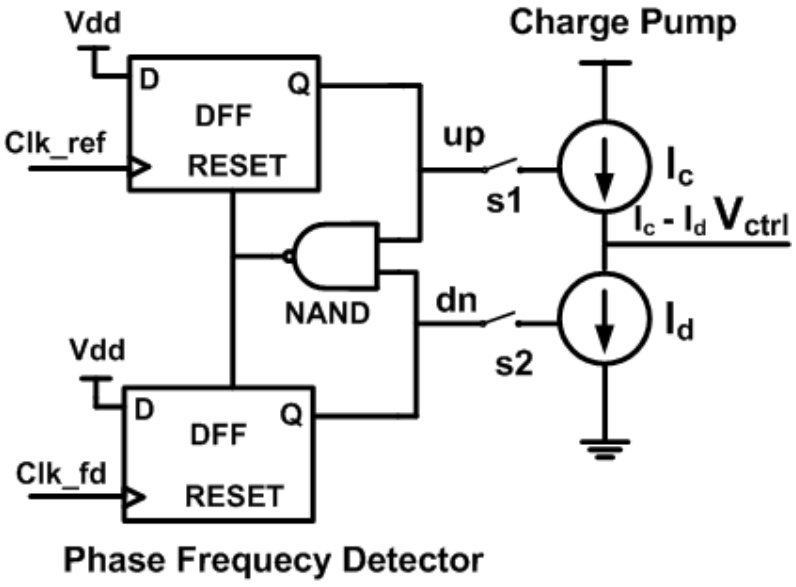


Fig. 1.2 Phase frequency detector and charge pump [9-10]

The current is sourced from supply voltage which is controlled by the up output of the PFD. This source current is thus called as the up current (I_c). The current is sinked to ground which is controlled by the dn pulse of the PFD. When the PFD detects a phase (and frequency) error between the input reference Clk_ref and feedback Clk_fd signal, its outputs *i.e.* up/dn pulses are in the states (+1/-1) in proportion to the initial error. This forces the charge pump to source (I_c) or sink current (I_d) accordingly. The gain K_{PFD} of the PFD is given by equation (1.1) [9]:

$$K_{PFD} = \frac{I_{cp}}{2\pi} \tag{1.1}$$

where I_{cp} is the current of the charge pump. Assuming the LF has as an ideal integrator characteristic and it averages a pulse generated from the PFD.

1.5.1 Loop Filter

The output of the charge pump is current which is provided to the low pass filter. A loop filter is employed in the PLL and remarkably impact on the performance parameters of the PLL [9-11]. The basic configuration of the loop filter is shown in the Fig. 1.3. The low pass filter is used to average the output of CP. The major function of the loop filter is to remove unwanted components of the phase frequency detection. The design of loop filter impacts the loop stability, bandwidth, and jitter of PLL. The impedance of low pass filter is given by equation:

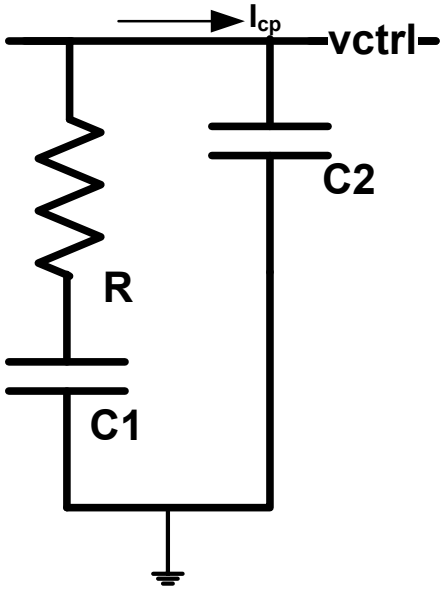


Fig. 1.3 Loop filter [9-10]

$$V_{ctrl} = I_c * \frac{sC_1R}{s(C_1 + C_2)(1 + sC_2R)} \tag{1.2}$$

where C_2 is high frequency pole. The transfer function of filter is given below [9-10]:

$$H(s)_{LP} = \frac{1 + \frac{s}{w_z}}{s(C_1 + C_2)(1 + \frac{s}{w_p})} \tag{1.3}$$

where $w_z = 1/RC_1$, $w_P = c_1 + c_2/RC_1C_2$. PLL employs a divider between the oscillator and the feedback input to the phase frequency detector which makes PLL as the frequency synthesizer.

1.5.2 Voltage Controlled Oscillator

The VCO is responsible for generating the output frequency of a PLL. As such, it is the primary high frequency block of a PLL [8-10]. The output of VCO is tied to the input stage of the feedback divider. The output voltage from the loop filter is used to control the VCO frequency. If the phase and frequency of the reference signal is higher than that of the VCO output, it speeds up the VCO and increases its output frequency. On the other hand, if the reference phase is lagging behind the VCO output phase, it forces to slowdown the VCO and reduces its output frequency. Although VCO design is simple but the high frequency operation of a VCO complicates its characteristics. It is the most challenging block of a PLL to design in terms of meeting the given specifications. The n stage VCO is shown in the Fig. 1.4. An n-stage ring oscillator is depicted with each inverting amplifier comprising one stage. The relation between the output frequency of the VCO and control voltage is shown in Fig. 1.5. For single ended VCO design architectures, there are an odd number of stages such three or five stages. For lower frequency requirements, number of stages is increased. The propagation delay from one stage to the next and the total number of stages determines the frequency of oscillation.

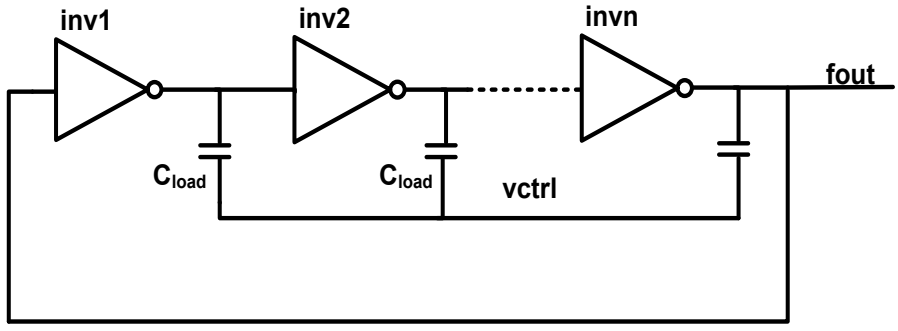


Fig. 1.4 Voltage controlled oscillator [8-9]

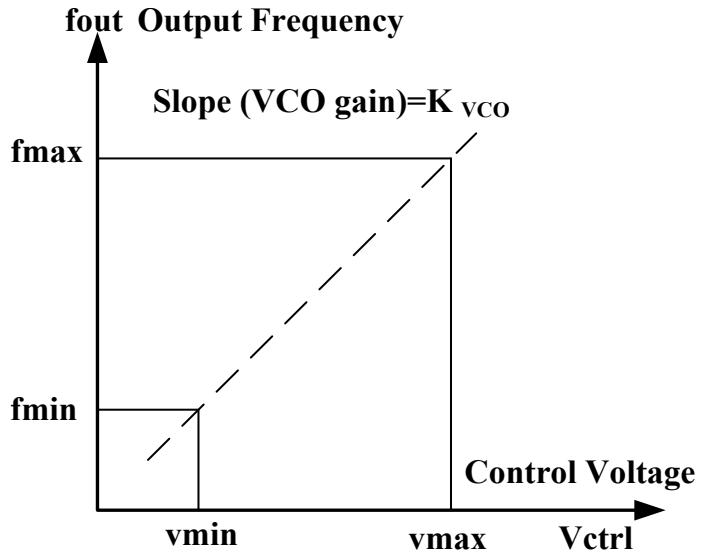


Fig. 1.5 Gain of VCO [9]

The frequency of oscillation of VCO is given as:

$$fout = \frac{1}{2n\tau_d} \tag{1.4}$$

where n is the number of stages of VCO and τ_d is the delay of each cell in VCO. Ideally, control voltage and output frequency are linearly correlated. The transfer function is given as:

$$f_{out} = f_{min} + K_{VCO}\, V_{ctrl} \tag{1.5}$$

$$H(S)_{VCO} = \frac{K_{VCO}}{s} \tag{1.6}$$

where f_{min} is the minimum frequency and V_{ctrl} is the control voltage.

Equation (1.6) shows the s domain transfer function of VCO. On the other hand, LC-tank oscillators are called the resonant oscillators and implemented using the series combination of an inductors and capacitors [9-10].

1.5.3 Feedback divider

The digital frequency divider divides the output signal of VCO by *N* times [10]. The dividers are used to divide the frequency of VCO and frequency is down converted to the value of reference frequency. The dividers are designed using single phase true clock D-flip-flops. Other than this, miller dividers are also used to divide the frequency [10].

1.6 PLL Transfer Function

PLL is negative feedback system [9-11]. The PFD, charge pump, loop filter, VCO, and divider forms a cascade system. Due to divider in system, the feedback gain Φ_{fd} is given as $1/N$. The loop filter significantly affects the gain of PLL system. The open and closed loop function of PLL is given as [10]:

$$\mathrm{G(s1)} = \frac{\Phi_{\mathrm{out}}}{\Phi_{er}} = \frac{I_{cp}}{2\pi} H(s)_{LP} \frac{K_{VCO}}{s} \tag{1.7}$$

$$\mathrm{G(s2)} = \frac{\Phi_{\mathrm{out}}}{\Phi_{ref}} = \frac{\mathrm{G(s1)}}{1 + \Phi_{fd}\mathrm{G(s1)}} \tag{1.8}$$

$$\mathrm{G(s2)} = \frac{\Phi_{\mathrm{out}}}{\Phi_{ref}} = \frac{\frac{I_{cp}}{2\pi} H(s)_{LP} \frac{K_{VCO}}{s}}{1 + N\frac{I_{cp}}{2\pi} H(s)_{LP} \frac{K_{VCO}}{s}} \tag{1.9}$$

where $\mathrm{G(s1)}$ and $\mathrm{G(s2)}$ are the open and closed loop gains respectively. I_{cp} is the current of the charge pump, $H(s)_{LP}$ is the transfer function of the loop filter, and K_{VCO} is gain of VCO. The loop filter parameters impact the stability of PLL and also affect the speed of PLL. The major issue with charge pump PLL's is current mismatch, more power consumption, and higher area requirement. To avoid these problems, recently industry and PLL designers are moving towards the all-digital phase locked loops.

1.7 All Digital Phase Locked Loop

It contains various digital blocks [3, 5, 12]. It works with discrete and digital signal only. The signal could be single or combination of parallel digital signals. It consists of three blocks: time to digital converter (TDC), Loop Filter (LF), and digitally Controlled Oscillator (DCO). Fig. 1.6 depicts basic structure of an ADPLL.

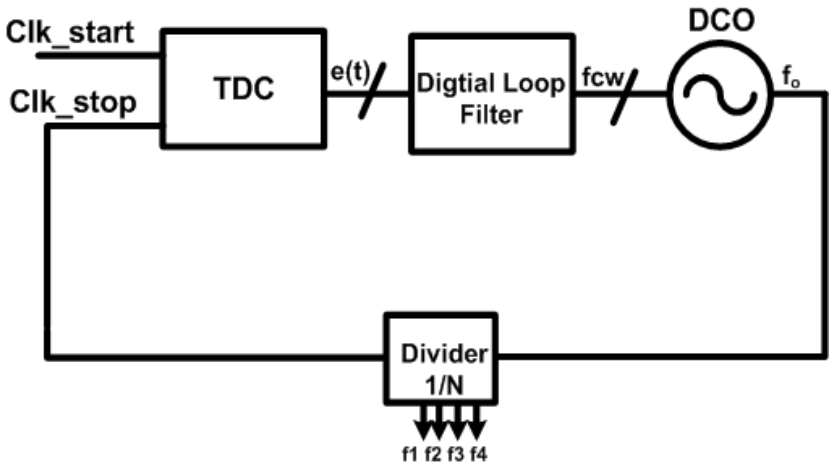


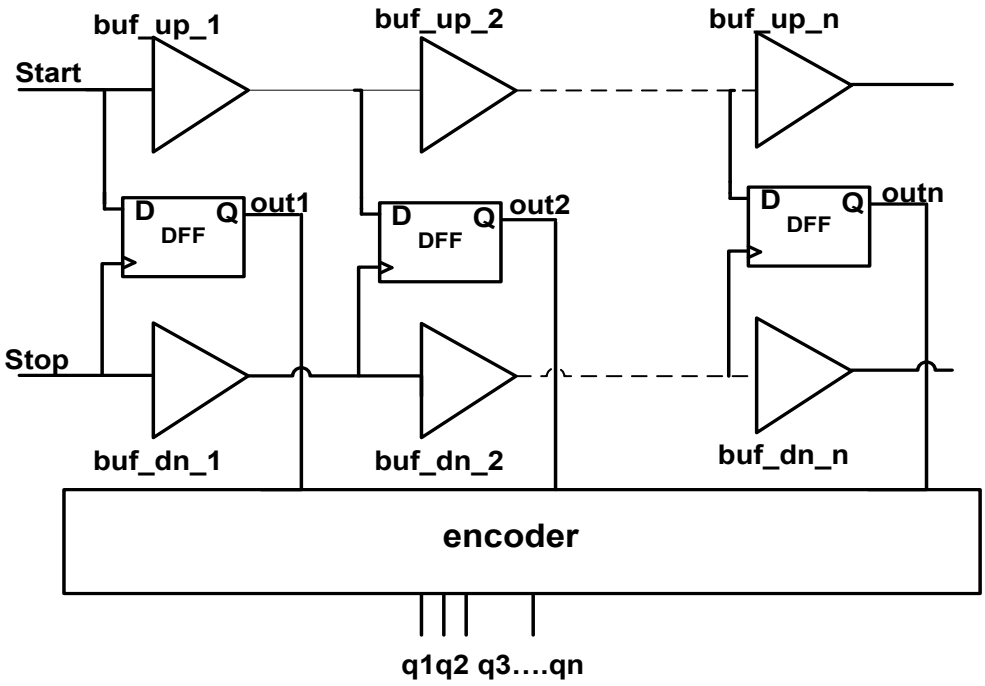
Fig. 1.6 All Digital PLL [12]

Although the CP-PLL is a predominant preference for frequency synthesis, but it faces many difficulties while integrating into nanoscale CMOS technologies. The large resistors and capacitors of loop filter in the CP-PLL architectures are required to suppress the noise issues. This impacts the area and power requirement of chip. Moreover, the analog intensive designs lack flexibility and portability to newer technologies. The other major issue with CP-PLL is the current mismatch between the charging and discharging currents which gives rise to the spurs and also degrades the jitter of CP-PLL [3]. Therefore, recently ADPLL has caught the attention from various researchers and industry. To alleviate the above said issues, ADPLL is in demand for frequency synthesis in the recent years. Unlike conventional PLL, the primary blocks of ADPLL are digital or digital-like circuits [12]. As compare to the analog loop filter that occupies more area on the chip in the CP-PLL, a digital loop filter is compact in size, fast, reconfigurable, and requires a low power. ADPLL significantly reduces the chip area and they can be easily ported and scaled to other technologies. Also, the ADPLL gives a flexibility to modify the bandwidth by changing the coefficients of digital loop filter [12]. In the ADPLL, designers are able to have intermediate signals in digital form, which is a huge advantage for analysis. Being digital in nature, it also has other benefits such as high flexibility, low power consumption, and low noise [12].

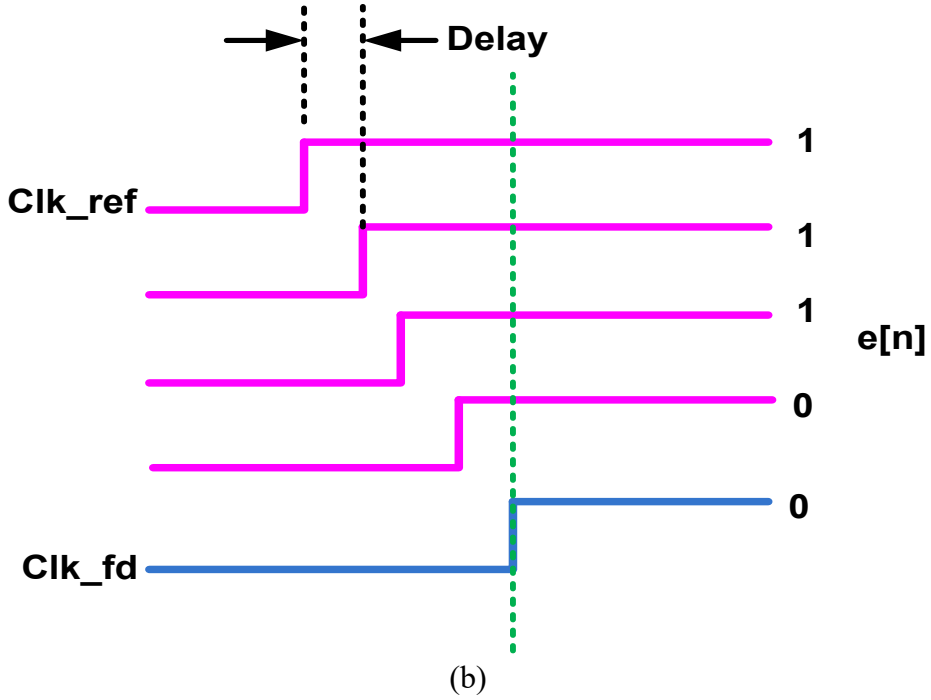
1.7.1 Time to Digital Converter

The Time-to-Digital Converters (TDC) is used have precise measurement of the time interval between two events as shown in Fig. 1.7 (a). Also experiments which involve laser ranging [13-14] use a TDC. TDC has Physics related application such as time-of-flight and lifetime measurements in atomic and high energy physics [14]. Electronic research involving the testing of integrated circuits and high-speed data transfer also requires a TDC for their operations. In oscilloscopes and logic analyzers, it gives time-related information in digital format. However, TDC is employed by ADPLL in frequency synthesis [14]. It is one of fundamental block which gives phase variation information between reference clock signal and feedback clock signal in digital format. It serves a charge pump based PD in DPLL. It acts as interface between time and digital domain. The TDC is discrete in nature and thus induces quantization error. A quantization error affects in-band phase noise and limits the loop bandwidth of ADPLL [14]. TDC impacts the performance parameters of overall ADPLL. The key solution to diminish quantization error in TDC is to improve its resolution. Dynamic range of TDC is defined as the maximum time difference that can be measured by it [14-15]. Other than resolution, the wide dynamic range is required in TDC. Thus, the ultimate goal of the TDC designers is to design a high resolution and wide dynamic range TDC. The

current process technology and refined architecture of TDC has allowed achieving the sub-gate resolution already.



(a)



(b)

Fig. 1.7 (a) Vernier TDC [14], (b) Output waveform of Vernier TDC

The Fig. 1.7 (a) and 1.7 (b) shows Vernier TDC architecture and its output waveform respectively. It consists of two chains of buffers and D-flip-flops. Start signal is given to one of the delay chain with larger unit delay of $\tau 1$. On other hand Stop signal propagates through

the delay chain with smaller unit delay *i.e.* $\tau 2$. The resolution of TDC is determined by taking the difference between two propagation delay values as shown in equation below [14]:

$$\Delta\tau = \tau 1 - \tau 2 \tag{1.10}$$

After *n* stages of delay the rising edge of Stop signal catches up with the Start signal. $\tau 1$ and $\tau 2$ are the delays of buffer elements in upper and lower arms respectively. The measurement of time interval is as given in equation:

$$\Delta\tau = n.(\tau 1 - \tau 2) + \varepsilon \tag{1.11}$$

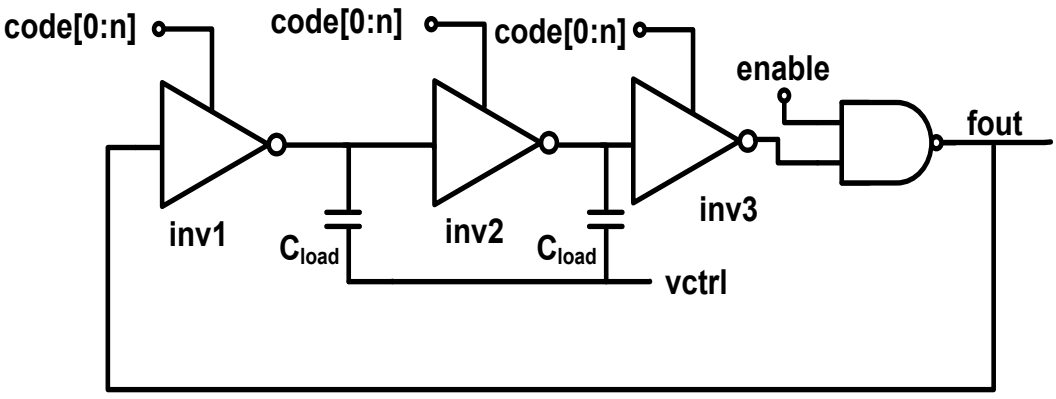
where ε is the quantization error and (n ∈ N). If the delay lines are matched properly, it provides a tolerance to the PVT variations. The dynamic range DR is limited to:

$$DR = 2^n.(\tau 1 - \tau 2) \tag{1.12}$$

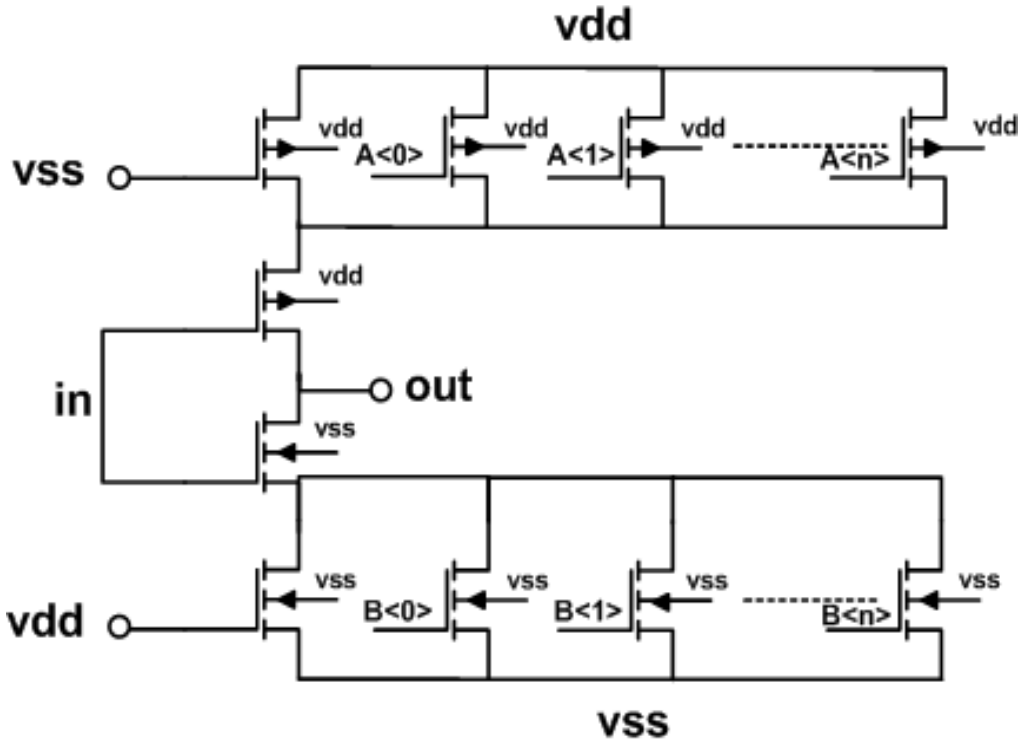
Vernier TDC architecture provides a higher resolution and wide dynamic range. Although this design has number of advantages, but achieving high resolution confines the dynamic range and also increases area and power consumption.

1.7.2 Digitally Controlled Oscillator

The digitally controlled oscillator (DCO) is used to perform the digital-to-frequency conversion (DFC) as shown in the Fig. 1.8 (a) which shows a delay cell of DCO. It is an essential block of the ADPLL. The digital control word *i.e.* code is given to delay cell which varies the frequency of DCO. It operates in the discrete-time domain [16-17]. The implementation of ADPLL is possible due to the avoidance of analog tuning controls. In ADPLL, DCO, and loop control circuitry can be implemented using the digital style. The control word *i.e.* code is input to ring DCO and fout = f (code). The supply power, uncertainty, and the PVT variations decide the instantaneous value of the frequency of DCO. There are numerous DCO architectures that can be used in the ADPLL such as LC tank-based oscillators. The discrete nature of DCO gives rise to the quantization noise which affects the performance of out-band phase noise [16]. To have low phase noise, a relatively high frequency resolution is required which costs in terms of area and power. Usually, varactors with variable capacitances are used to control frequency of DCO.



(a)



(b)

Fig. 1.8 (a) Digitally controlled oscillator [16], (b) Delay cell of DCO

The design of varactor majorly impacts the tuning range and frequency resolution [16]. At high frequency operations, parasitic, and losses in varactors significantly affect the performance of the DCO.

1.7.3. Digital Loop Filter

The digitized implementation of the phase-lock loop allows the employment of a totally digital loop filter. Fig. 1.9 shows a digital loop filter [18-19]. The avoidance of conventional analog filter significantly reduces power and area of overall chip. Apart from this, the digital

loop filter offers a high flexibility and thus provides an easy variation in the bandwidth of ADPLL. There are a number of digital filter implementations like finite impulse response (FIR) filter, infinite impulse response (IIR), and proportional integral filter that can be used in realization of the ADPLLs [18-19]. In FIR and IIR filters, proportional loop gain α is cascaded and in parallel an accumulator is used to implement the digital loop filter. FIR filters are more beneficial as they stable but takes lot of area and power. Typically, IIR filter provides stronger filtering capability and compact structure but it is more vulnerable to instability [18-20].

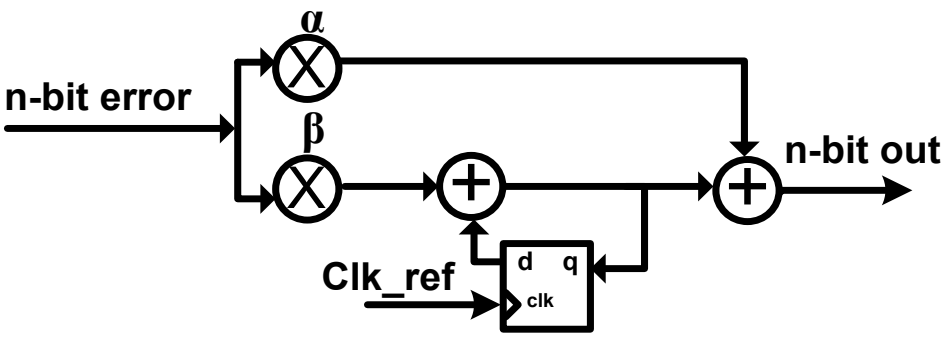


Fig. 1.9 Digital loop filter [19]

FIR filters use higher number of cells as compared to the IIR filter for given filtering capability. Generally proportional integral filters are used for filtering purpose in the ADPLLs due their easy and compact structure. The output of TDC is feed to digital filter which produces an n-bit control word (Fcw). Fcw is used to control the frequency of the DCO. The order of filter decides the accuracy and complexity of filter. The Z-domain transfer function of proportional integral filter is given as [19]:

$$H(Z1) = \alpha + \frac{\beta}{1-Z^{-1}} \tag{1.13}$$

where α and β are proportional and integral gain of digital filter. The working of ADPLL is similar to digital PLL. To realize an ADPLL, existing elements of all blocks must be designed using the digital circuits. The present standard of frequency synthesis requires a low jitter, reduced area, and power consumption. Also, ADPLL should have wide operating range of frequency with fast locking time.

1.8 Organization of Thesis

The **chapter 1** introduces the phase locked loop design and motivation behind the research in this topic. This thesis is organized as follows:

Chapter 2 shows a literature survey. This chapter starts with a review of the state-of-art of DPLLs and ADPLLs in recent years. The current trends in DPLL and ADPLL structure are studied rigorously.

Chapter 3 illustrates a design and analysis of 4-bit and 3-bit flash TDCs. The simulation results of the proposed 4-bit and 3-bit flash TDCs are shown in this chapter.

Chapter 4 gives an insight into digital PLL's. The design and analysis of two digital PLL architectures are presented in this chapter. Also proposed designs of phase frequency detectors are discussed. The inverters, buffers, and switches are used to design PFD which addresses the issues of the dead zone and blind zone. These problems impact the loop dynamics, jitter performance, and acquisition time of PLL. Then the inverter and switch based charge pump is described and analyzed in depth. The inverters based VCO for low power and low phase noise is proposed. This chapter also discusses the simulation results of proposed DPLL-I and DPLL-II designs. The various simulation results of proposed frequency phase detectors *i.e.* PFD-I and PFD-II are also discussed. The results and analysis of proposed charge pump is also shown in this chapter. The chapter ends with a pre-layout and post layout simulation comparisons of DPLL-II in 180 nm SCL technology.

Chapters 5 starts with the proposed design of ADPLL-I. This chapter presents a design and analysis of ADPLL-I. Also, the effect of TDC's jitter on performance parameters of ADPLL-I is studied. This chapter gives the details of DCO and digital loop filter. The calibration of 4-bit flash TDC is explained in the detail. Also, the need of calibration for ADPLL-I design is discussed in the depth. The major focus of proposed VCO-I is low jitter and low power. The chapter concludes with simulation results of proposed ADPLL-I.

Chapter 6 shows the hybrid architecture of the ADPLL-II. The bang-bang PFD and calibrated TDC architecture is used to design an ADPLL-II design. This chapter gives detail analysis and working of ADPLL-II design. It is concluded from this chapter that the proposed ADPLL-II achieves the low jitter and low power. The chapter also shows simulation results of proposed ADPLL-II architecture.

Chapter 7 depicts the proposed ADPLL-III design. Further to enhance the parameters of ADPLL, generic ADPLL architecture is designed. The background calibration based VCO-II is proposed to obtain low power, fast locking, and low jitter of ADPLL-III design. This chapter shows the design analysis and simulation results of ADPLL-III. Also, the simulation results of VCO-II are depicted.

Chapter 8 concludes the thesis and discusses the future scope of present research work.

CHAPTER 2

LITERATURE SURVEY

2.1 Introduction to ALL Digital Phase Locked Loop

As described in the chapter1 section 1.3, PLL is classification in different like Analog PLL, DPLL, and ADPLL [12]. The extensive literature survey on DPLL and ADPLL are carried out to find research gaps in the existing literature works. The conventional analog and Digital PPLs have shown improved performance in terms of jitter and locking time however they have issue like more area requirements, more power, PVT variations, no re-configurability, and non-scalability. To overcome the issues of Analog and DPLL, ADPLL is introduced [3,12]. ADPLLs have better performance in terms programmability, testability, lesser PVT issues, lower power consumption and lesser design effort. The prime components of ADPLL are DCO, TDC, digital filter, and divider as shown in the Fig.1.6. The reference and feedback signals are given to TDC as shown in the Fig.1.7 (a) and it to converts time to digital bits. Depending the phase and frequency difference between reference and feedback clock, the error bits are generated and these bits are given to digital filter. The output of DLF is used to modulate the frequency of DCO. Depending upon the DLF, the ADPLL can be classified as type-I and type-II. TDC is one of major block of ADPLL. Number of research papers has been published for TDC addressing issue like area, power, and PVT variations. The existing literature shows TDC have complex designs and quantization error is other major issue which degrades the overall performance of ADPLLs. DCO is heart of ADPLL. Several DCO approaches has been reported to design, low jitter, low gain, and low power DCO. DCO suffers from PVT variations which overall affects the performance of ADPLL. The various DPLL and ADPLL designs are reported in the literature. The following section shows an extensive literature survey done for DPLLs and ADPLLs which shows various research gaps.

2.2 Literature survey Digital and ALL Digital Phase Locked Loop

Wei Liu *et al.* [21] used the divider before the oscillator to keep loop bandwidth constant. The divider adjusts the control word which keeps the frequency of DCO constant. This architecture is process, voltage, and temperature (PVT) invariant but the jitter is degraded and output frequency is limited. The power consumption of 7.1mW is high and locking time of 7μs is more. Moreover, architecture contains locking monitor block, dual phase detector, and phase generator which complexes an overall design.

Richard Su, Steven Lanzisera, and Kristofer S. J. Pister [22] proposed an ADPLL which is based on standard cell library. It uses an embedded time-to-digital converter (TDC)

with multipath to increase TDC resolution and includes digital correction circuitry to resolve issues of the clock skew. The DCO is embedded in the TDC design. Therefore, delay in the DCO is directly related to quantization error of TDC. This architecture is not fully synthesizable. Also digital to analog converter (DAC) and current sources are designed using custom cell approach. The architecture has more area, locking time, and power consumption due to use of complicated Vernier TDC architecture. The usage of current source, DAC phase quantizier, and delta sigma modulator leads to complex architecture. The power consumption is 7.56 mW at the output frequency of 900 MHz only in 180 nm.

Chan-Hui Jeong *et al.* [23] used digital calibration technique to compensate the current mismatch between up and down pulses in the charge pump which results in a steady-state phase offset and generates glitches in the output current of the CP. It increases the level of jitter and reference spurs in output frequency of PLL. The additional charge pump based on AND gate, D-flip-flops, and counter is proposed which eliminates a current mismatch. This circuit generates constant 2 uA current for each step of 3-bit counter. The worst-case current mismatch is 16 uA. The locking time is increased to 32 μs due to used technique. The locking time is very high for this architecture. The frequency range is 1.15 to 1.6 GHz which is very limited.

C.H. Jeong *et al.* [24] proposed a new TDC for ADPLL which generates variable delay regardless of frequency of the DCO. The power consumption is lower as TDC turns on only at period of DCO and does not depend upon the frequency of DCO. The circuit based on D-flip-flop and NOR gate is used to control the delay of the TDC. The average power consumed by TDC is reduced. This PLL architecture consumes more area due use of complex TDC. Although the power is reduced, but it is more complex as compare other works. The PVT issue is not addressed in this paper. The high reference frequency of 40 MHz is used to produce an output frequency of 1.6 GHz.

In [25], Giovanni Marucci *et al.* designed a modified bang-bang phase detector which reduces the jitter of DCO. The paper highlights the jitter contributed by PFD and DCO. The down scaling of low pass filter relaxes a DCO resolution. The delta sigma modulator upscales the DCO resolution. This design has lower phase frequency detection range and it takes more time for locking due to use BPFD. The jitter is highly degraded and a very low output frequency of 320 MHz is generated.

Minyoung Song *et al.* [26] designed a delay cell less time to digital converter. TDC consists of the 4 phase and 8 phase multiphase clock generators along with the weighted setup time D-flip-flops. This design increases the resolution up to 4 ps without adding quantization error. The p and n latch VCO is used to further improve phase noise and PVT

variations. The DCO is designed using Digital to Analog (DAC) which is power hungry component in the system and it is not fully synthesizable. The multiphase and weighted setup TDCs are used. These TDC cause synchronization issue and power consumption of 12 mW is very high at 180 nm with degraded jitter of 4 ps.

Chung-Yi Li *et al.* [27] proposed a PLL with additional time to digital converter. This unit consists of charge pump and low pass filter which produces a narrow bandwidth for low noise. This architecture produces a variable loop bandwidth to alter the control voltage. The algorithm uses a fixed phase threshold with a delay-independent dual-slope transfer function to achieve the bandwidth control. When PLL is in locked state, it will switch to narrow bandwidth thus reduces jitter and offers more stable frequency of oscillation. This architecture uses a PD, PFD, and charge pump. The output frequency ranges from 1.2 GHz to 2 GHz and produces a degraded jitter of 9 ps at 1.6GHz. The peak-to-peak jitter is 45 ps which is more.

Ahmed Musa *et al.* [28] presented a synthesizable dual-loop and dual-VCO injection locked all-digital PLL (IL-ADPLL). This architecture addresses PVT variations using injection locking scheme. The system consists of two VCOs in which one will track frequency and other is used to calibrate the phase difference in reference and DCO clock. The main issue with this architecture is matching between the N reference frequency and free running frequency of VCOs. The use of large circuits like DAC and other circuitry leads to more area and power consumption. The reference frequency of 300 MHz is used to generate a 1.6 GHz output frequency.

Wei Deng *et al.* [29] proposed an all-digital phase locked loop which is based on the injection locking system. This architecture is fully synthesizable and all the modules are designed from standard cell library. The Hardware Description Language (HDL) language is used in this architecture. The design is based on dual loop which increases the hardware of overall system. The gated injection locking is used to decrease the spur, noise in the oscillator. Although the architecture has low area, low jitter, and high FOM factor, but the power consumption of 780 μW is high for 900 MHz. The design complexity is more.

Saman Saeedi and Azita Emami-Neyestanak [30] presented a low-power first-order frequency synthesizer architecture suitable for high-speed. This architecture uses a LC oscillator with reference injection. The PLL architecture consists of sample hold, digital coarse tuning, and phase interpolator. Reference injection is implemented via phase-interpolation. The frequency acquisition consists of digital coarse-tuning and rotational frequency detection for fine-tuning. The fine-tuning frequency detection block is made using buffers, Schmitt's trigger and oscillator. These cells are designed using resistors and standard

cell methodology. The circuits consume a more area due to use of inductors and capacitors. The frequency range of 8-9 GHz is very high for this architecture but at cost of more complexity and high input reference frequency. The area consumed is 0.044 mm^2.

Jung-Mao Lin and Ching-Yuan Yang [31] designed ADPLL consists of a bang-bang phase detector (BBPD), a digital low pass filter (DLF), DCO, a feedback divider (DIV), and delta sigma modulator. The dual loop architecture is used. The frequency detection is done first, once the frequency error is locked, and then BBPD is turned on which produces the phase error. The phase error is tracked by DAC and it produces the control word which modulates the output frequency. The DAC is present in an integral path which changes the phase error of BBPD. The architecture has jitter of 8.8 ps. The area consumption is very high. The standard cell technology is not used. The power consumption is 35 mW which is very high as compared to other designs reported in the literature.

Muhammad Faisal, Nathan E. Roberts, and David D. Wentzloff [32] proposed a low power all-digital PLL. The ADPLL features two loops: a frequency acquisition loop and a fine phase locking loop. The state finite machine is used to select the frequency and phase error. If the frequency error is more than 4K, the frequency detection is activated first, then phase loop. The power gated VCO is used to save power. The long channel MOSFETs are used to prevent the PVT variations. This architecture shows a very less power consumption but the oscillation frequency is very limited. The area consumed is 0.7mm^2 and jitter is 4.7 ns @500KHz which are worse as compare to other architectures reported in the literature.

Christian Venerus and Ian Galton [33] designed a frequency to digital converter type PLL. It has advantage of digital loop filter. It also avails the digital process benefits such as robustness and technology independence. This will also give advantage in terms of area and scalability for frequency detection control (FDC). It consists of a phase-frequency detector (PFD), charge pump, capacitor, 5-level ADC, digital block, and frequency divider. The conventional (LC) based VCO used with additional frequency control element banks for coarse and fine tuning. This architecture involves an analog process which increases an area and the power consumption. The power consumed is 31 mW @ 3.5 GHz due to use of ADC and LC DCO.

Jianhui Wu *et al.* [34] and Hsing-Chien Chu *et al.* [35] proposed a TDC based PLL. The central idea of [34] is to increase the resolution of TDC for lowering the quantization error of PLL. The frequency resolution of the LC-based digitally controlled oscillator is improved by the smaller unit capacitor. The edge interchanging circuit is used to exchange rising edge of reference and feedback clock. The output from TDC is sampled after two cycles of reference clock. The power reduction of 30% is obtained as compare to traditional

TDC for which 32 arbiters are used. For this architecture but power consumption is high. The proposed TDC is requires an additional circuitry to improve resolution which degrades power consumption with value of 9 mW. In [35], multiple TDCs are used to obtain fine resolution. The time amplifier increases the resolution 8 times but it also introduces the non linearity. This leads to phase noise degradation. The calibration technique is used to overcome this issue of non linearity. The power consumption is 18 mW @800MHz.

Long Kong and Behzad Razavi [36] showed a type1 PLL with two adjacent discrete filters. The problem with discrete filter is that it gives two voltage levels, but two filters in master-slave mode solve this problem. The PLL uses a harmonic trap circuit which is implemented in analog process with delta sigma modulator as a compact, low-power ADC to measure the ripple waveform and reconstruct it in the digital domain. The paper represents simple architecture of PLL with notch calibration to reduce spur level less than -65 dB. The paper depicts improved parameters such as area, power, and jitter. The proposed architecture is purely analog in nature which increase design effort and it is not portable and scalable.

Sung-Geun Kim *et al.* [37] proposed a PLL circuit with a supply-noise-compensated feed-forward ring voltage-controlled oscillator (FRVCO). The oscillation frequency fluctuation due to supply noise is not affected by adjusting the ratio of driving strength in the feed-forward and direct paths in FRVCO. This PLL works at 400-MHz. The PLL circuit is operating at 0.65 V and it is fabricated with 180-nm standard CMOS process. This PLL consumes only 242.1 μW. Not more than three transistors are stacked in the entire circuit for low-voltage operation. The charge pump is two-transistor-stacked gate-controlled structure and the phase-frequency detector consists of gates and D-flip-flops. The VCO has the feed-forward structure with three different frequency ranges. The delay cell employed for VCO is body biased at PMOS transistor. The divide-by-16 frequency divider consists of an extended true-single-phase-clock (TSPC) DFFs for fast operation and low power consumption. The noise sensing block is introduced which reduces the noise in supply voltage. The architecture does not show analysis for PVT variations and wide range of frequency tuning is not possible as PLL works only up to 400 MHz.

Teerachot Siriburanon *et al.* [38] and Akihide Sai *et al.* [39] showed an (Analog to Digital Converter) ADC based PLL to overcome the quantization error produced from the conventional time to digital converter. Low resolution ADC is used for less power consumption. The voltage from amplifier is converted into digital bits which controls the frequency of DCO. The voltage control oscillator with higher gain is required. The LC oscillator along with the buffers is used for isolation. The architecture is complex. The flash ADC with 21 comparators is used. In [39] TDC is proposed using single slope ADC along

with PFD and charge pump. In the TDC, the SS-ADC uses the counter for measuring the ramp-up time with that of the ADPLL for measuring DCO integer phase. High counter and ADC structure are power hungry blocks in the ADPLL. The architecture consists of many analog circuit techniques which challenges its scalability and robustness.

Susan Marya Schobar and John Choma jr. [40] and Dongil Lee *et al.* [41] designed a modified charge pump PLL. This paper [40] presented the new charge pump totally digital in nature and does not require analog circuit techniques. The proposed charge pump also compensates the ripple in ideal mode as capacitor remains charged to supply voltage in that mode. The frequency phase detector is proposed without a delay chain to incorporate new charge pump. The low pass filter is designed without the resistor which can make PLL unstable. VCO is capacitor coupled which leads to more area consumption. In [41], an additional charge pump is used to compensate the overlapping of the up and down pulses. It alleviates the problem of phase noise degradation. Further ring VCO is made which controls voltage ripple to solve mismatch problems in PD and CPs. The reference injection based VCO is used to overcome problem of PVT variations and phase noise. The proposed PFD has limited detection range of $-\pi/2$ to $+\pi/2$. Both area and power consumption are more in this proposed DPLL.

Dong Dheng Yang *et al.* [42] proposed an architecture which is implemented in the HDL language. The inductor is designed using spice tools. The inductor layout is added to automated generated layout of other blocks of system. The author focuses on design of LC DCO using MOSFETs. This DCO is pulse injection locked for low phase noise and the DAC is used to control current. The DCO is not synthesizable and standard topology is not used. Additional circuits like pulse generator, pulse width corrector, and clock distribution circuits are used.

Ching-Che Chung, Wei-Siang Su, and Chi-Kuang Lo [43] proposed an all-digital PLL design. The clock generator used in this design is capable of achieving a faster settling time and has a wider operating voltage range. In this brief, a fast lock-in all-digital phase-locked loop (ADPLL) with two operation modes (0.52/1V) is presented. The proposed ADPLL can quickly compute the desired digitally controlled oscillator control code with high accuracy. Therefore, the proposed ADPLL can achieve a fast setting time with frequency errors <5% within four clock cycles. The output frequency of the ADPLL ranges from 60 to 600 MHz at 1 V and from 30 to 120 MHz at 0.52 V respectively. The power consumption of the proposed ADPLL is 0.92 mW at (1V, 600 MHz). The frequency finder, the digital loop filter, and the ADPLL controller are designed with hardware description language. The jitter performance is very degraded due to use of TDC.

C.W. Chan, K.Y. Chang, Y.H. Chu, and S.J. Jou [44] introduced an ADPLL with power management unit in the near threshold voltage era. The power management unit consists of adequate voltage to do dynamic voltage scaling. The power management unit (PMU) engine generates control signals and the buck converter produces adequate voltage with a voltage step of 15 mV to the ADPLL for optimizing power consumption. The proposed ADPLL with power management have following: ADPLL engine consists of a phase-frequency detector, an ADPLL controller, a programmable proportional (ß), integral (α) coefficients for digital loop filter, and DCO. Further DCO system consists of varactor. The frequency adjustment is done using loading of varactors with 3 different voltages. The supply voltage is 0.5 V and the output frequency range is low.

Sebastian Höppner *et al.* [45] proposed ADPLL in which the built-in self-calibration technique is used to change the proportional coefficient (+1 to -1) of digital loop filter. The additional PFD is used to determine the jitter at input of the reference and feedback clock. This PFD works at offset time difference between both pulses. If offset time is greater than 0, the probability of occurrence of 1 at PFD is greater than 0.5. Built-In Self-Calibration algorithm compares the count values from previous cycle and accordingly, it adjusts the beta factor. The algorithm determines jitter. The noise issues due to loop filter and VCO are addressed in this paper. The jitter is 15 ps for 2.5 GHz. Although, area is reduced but jitter performance is degraded.

Omar Abdelfattah Gal *et al.* [46] proposed wide frequency range PLL from 100 MHz to 10 GHz. The paper addressed the issues related to PVT variations and noise due to wide range. This PLL has two wide range VCOs with two capacitor banks. The VCO is LC based in order to have reduced noise. The loop filter controls the oscillation frequency and binary code selects the VCOs for desired range of frequency. The dynamic PFD is used for high speed operation for frequency range of 5-10 GHz. The charge pump is modified with degenerate resistors and low v_{th} transistors to incorporate PVT variations. 6-bit counter is used along with pre-scalar for division. The power consumption is 42 mW which is very high. The issues related to process, voltage, and temperature are not addressed in this paper. The area consumed is 2.5 mm^2.

The frequency and phase error compensation technique for ADPLL is proposed by Yung-Hsiang Ho and Chia-Yu Yao [47]. The code word change is kept smooth by using coarse tuning. The proposed ADPLL can achieve fast phase and frequency acquisition, while maintaining a relatively small timing jitter. This paper employs a novel FEC to speed up the frequency acquisition process. No standard cell library is used and nor it is synthesizable architecture. The output frequency range is very limited from 860 MHz to 1 GHz.

Ting-Kuei Kuan and Shen-Iuan Liu [48] designed a bang-bang phase frequency detector ADPLL with automatic loop gain control. This technique provides an optimized jitter performance. The design uses automatic gain controller consists of FIR filter and integrator to optimize the jitter. This architecture provides a jitter with value of 320 fs and power consumption of 3.8 mW. This design consumes more area as LC oscillator is used and it is more prone to PVT variations and noise.

In [49] Amr Lotfy, Maged Ghoneima, and Mohamed Abdel-Moneum proposed the hybrid ADPLL architecture. To achieve the fast locking of 1 μs, BB-PFD and two TDCs designs are used. This architecture is bulky, cumbersome and also requires a switching between BB-PFD and TDCs. The adaptive proportional derivative digital loop filter also aids to achieve the fast locking. Though the designs show a fast locking and low jitter, the resolution of TDC is limited to 20 ps. The two TDC's consumes more area and power.

San-Fu Wang, Tsuen-Shiau Hwang, and Jhen-Ji Wang [50] proposed a DPLL with digital calibration for charge pump to suppress the fluctuations in charging and discharging currents. The proposed design reduces the ripple in control voltage. This improves the jitter performance of PLL. The proposed design limited output frequency range. As compare to other designs, the power consumption is higher *i.e.* 23 mW. Also, the proposed technique increases the locking time to 10 μs.

Junheng Zhu *et al.* [51] proposed the hybrid PLL. The proportional path is designed using phase frequency detector and DAC which drives a VCO. An analog proportional path overcomes the problem of TDC quantization error and noise bandwidth trade-off of digital PLLs. Furthermore, an analog proportional path also helps to ease the resolution requirements of the digital integral path. In this paper, the proportional path consists of PFD. Integral path consists of ring oscillator based time integrator. Further phase detector is required to convert phase error into the voltage or current signal. Both paths use duty cycle to current converter circuit to reduce jitter. The spurs are created if free frequency of VCO is not equal to reference frequency and duty cycle is not 50%. To overcome these issues, author uses differential mode integrator which increases power. Two DACs are used which increases area. The input reference frequency of 350MHz which is high.

Roohie Kaushik, G.S. Viswswaran, and Shouri Chatterjee [52] designed a LC VCO based PLL. The LC VCO is designed using CMOS inverters, inductor, and Metal-Oxide-Semiconductor (MOS) capacitors [52]. It is current controlled VCO used to design the PLL without loop filter. The output from PFD is given to VCO through tri-state buffers. This architecture is simple. These architectures consume more area and power due to use of inductors.

Yalcin Balciogluand and Gunhan Dundar [53] designed an all-digital phase locked loop using high level synthesis. The phase noise modeling of different components of PLL is done using Matlab tool. In [54], an all-digital phase locked is proposed with pseudo differential oscillator with injection locking technique by Sung woo Kim *et al.* The path delay mismatch between the injection and the phase detector remains unsolved which leads to formation of the spurs. Once the ADPLL is locked, TDC calibrates frequency error and path mismatch. The mismatch between replica and main oscillator is not addressed in this paper.

Romesh Kumar Nandwana *et al.* [55] proposed a cascade PLL which consists of delay locked loop and digital PLL to reduce division factor. This architecture uses the hybrid PLL to get advantages of analog and digital techniques. Integral path accumulates error in 18-bit accumulator. Further it is given to delta sigma DAC. The DAC is designed using MOSFETs only. The pseudo differential current starved VCO with feed-forward path is used. This architecture uses two DACs for proportional and integral paths. The jitter is 35 ps @ 2.5 GHz which very high. The system has two PLL cascade which leads to complexity and more jitter.

B. D. Kumar and H. Shrimali [56] represented a frequency synthesizer which uses current re-use VCO. The VCO circuit consists of buffers, divider, resistors, and inductors which leads to more area and power consumption. The frequency and phase are divided by N and the phase noise is improved by N^2. The power consumption is 0.52 mW. The output frequency is very small from 0.4 GHz to 0.5 GHz.

Feiran Lei and Marvin H. White [57] designed the reference injection PLL. The conventional PFD and charge pump is used along with low pass filter. The N latch VCO with variable capacitor is used. The NMOS is used as variable capacitance which is reference injected to reduce phase noise of VCO. Active load inductor is realized using the PMOS and NMOS to reduce the parasitic capacitance and it also increases the speed of delay cell. This paper also depicts the noise modeling to show the effect of reference injection. This design has improved jitter of 1.55 ps and power consumption is only 2.6 mW at 1 GHz. Although, this architecture shows many advantages but PVT variations is more than 25% on FF and SS corner.

Yuming He *et al.* [58] proposed all-digital phase locked loop for IoT applications. The TDC with 32 stages along with capacitor banks are used. The digital to time converter is used to improve the performance of ADPLL. This DTC circuit is very non linear and it introduces a fractional spur. The frequency locked loop is used along with RF counter which is highly power hungry. If the resolution of DTC and TDC is not same, it introduces the noise in the ADPLL. This design has large area and more complexity. The complex technique of phase dithering is used.

Yusong Qiu, Lei Zhao, and Feng Zhang [59] demonstrated the design of frequency synthesizer. The proposed PLL achieves ultra-low jitter of 0.35-ps with a high resolution adaptive frequency calibration (AFC) method. This scheme automatically chooses frequency-tuning curves to improve the calibration accuracy. The architecture is complex and the locking time is 20 μsec. Also, this design has higher power consumption of 20 mW.

Abdul Majeed K.K. and Binsu J. Kailath [60] proposed the DPLL which consists of 2 charge pumps, composite PFD, VCO, and variable loop filter. This architecture adjusts a gain and bandwidth during tracking and locking stages. This design uses analog processes which increases design efforts. Also, resistors and capacitors consume a more power and large area. The mismatches between the up and down currents introduce spurs in the proposed design.

Mario Mercandelli *et al.* in paper [61] presented a method to adjust the bandwidth of digital PLLs in which totally digital automatic control circuit is used to desensitize loop gain from analog components. The adaptive least-mean-square based algorithm is used to calibrate and also calibration runs in background. The design consists of DAC, DTC, and LC based oscillator which introduces a complexity and also increases power consumption. The DTC and DAC introduce an additional quantization error in the design. This design show low power consumption of 4.1 mW and better jitter performance but the locking time is 120 μs.

Jincheng Yang *et al.* [62] proposed the adaptive gain control-based BB-PFD ADPLL. This architecture works in the two loops. During the tracking process, the gain controller circuit come into picture and reduces the locking time. When ADPLL gets into locked state, the gain controller circuit is reset. The flag generated by BB-PFD is used to switch between the two loops. This design has degraded jitter of 10.3 ps. This architecture is complex.

Taeho Seong, Yongsun Lee, Seyeon Yoo, and Jaeh youk Choi [63], proposed an ADPLL based on flash TDC. To suppress the PVT variations, foreground calibration is used. The ADPLL design is fast and achieves the very low jitter of 230 fs. The output frequency range of ADPLL is very limited. The proposed flash TDC has high resolution but very limited dynamic range. The power consumption is more *i.e.* 6 mW.

J. Tao and C. Heng [64] designed an N- fractional phase locked loop (PLL). This PLL architecture is DTC-less. This architecture has complex design and requires a lot of design effort. Further, DTC based architecture introduces the quantization noise in the system. The reference phase is modulated by the combination of linear slope generator (LSG) and multi-modulus divider (MMDIV) with multi-phase generation. The phase interpolator (PI) provides a large linear phase-to-voltage from the phase detector. The LSG block provides a phase dithering and reduces the quantization noise. This proposed PLL achieves in-band phase

noise of −110 dBc/Hz at output frequency of 2.2 GHz in a 130-nm CMOS process. The architecture has many circuits and phase noise is degraded.

Na Yan *et al.* [65] proposed a low-power fractional-N all-digital PLL (ADPLL) for the applications involving narrow-band Internet-of-Things. The proposed ADPLL is complex and have DTC which introduces a quantization error. Additional delta-sigma block is used to suppress the non-linearity of DTC. The dithering block reduces a jitter in overall ADPLL design. This design has achieved the low power of 4 mW. The locking time is 20 μsec which slows the DPLL design.

Fahim Ur Rahman, Greg Taylor, and Visvesh Sathe [66] designed an ADPLL for using complex TDC and DCO, clock buffers, solver, PFD, and adaptive filter with focus on achieving low locking time. The design uses frequency and phase acquisition blocks with computational locking to obtain fast locking and low jitter. This design has more locking time of 8 μs, degraded jitter of 7 ps, and more power consumption of 10 mW.

Chen Yuan and Sudip Shekhar [67] proposed a supply insensitive DCO for ADPLL. The capacitor banks made of a 6-bit coarse tuning bank and 7-bit fine tuning bank is used adjust the delay of delay cell with high resolution. To obtain the fine tuning digitally controlled resistor (DCR) is also used. A resistor triode act as load in each stage to cancel supply sensitivity for large supply variations and it is used to improved weak latches in a 2-stage differential ring oscillator. In the ring oscillator, an inverter based delay cells are used. The proposed DCO is used in the ADPLL and this architecture achieves a phase noise of -92 dBc/Hz and power consumption of 2.45 mW at output frequency of 1.25 GHz. The proposed ADPLL is designed in the 65 nm and works at 0.8 V. The phase noise is degraded.

Arjun Ramaswami Palaniappan and Liter Siek [68] proposed the TDC-less, low power, and ultra-low area all-digital phase locked loop which is used in the biomedical implant transceivers. The ring oscillator with the circuit design technique such as fractional capacitor tuning and capacitive boosting is used to achieve better jitter of proposed ADPLL. The ADPLL is implemented in 40 nm CMOS technology and occupies an area of only 0.0186 mm^2. The limited output frequency ranges from 330 MHz to 470 MHz with a supply voltage of 0.68 V. The ADPLL consumes a power of 248.62 μW but degraded output jitter is 11.88 ps at frequency offset. This design consumes the less power but the jitter performance is degraded for given range of frequency as compare to other works reported in the literature.

Manas Kumar Hati and Tarun Kanti Bhattacharyya [69] presented ΔΣ fractional-N PLL frequency synthesizer design with new technique for phase noise cancellation and constant loop bandwidth. In this work, the calibration using the charge pump for constant loop bandwidth is proposed. The proposed DPLL have the 14 μs as locking time with LC

oscillator. The locking time of the proposed DPLL is more as compared to other works reported in the literature. This design achieves the output frequency in range of 2.1- 5.5 GHz with power consumption of 32.7 mW in the 130 nm technology. The proposed design has higher circuitry complexity and very high power consumption is reported.

R. Dinesh and R. Marimuthu [70] proposed an optimal sampling digital PLL which uses high resolution DCO and high precision TDC. The proposed novel DCO utilizes boot-strapped ring oscillator which is used to boosted gate voltage and hence it increases a driving capability. The proposed design achieves low power of 1.374 mW at 14 nm technology. The phase noise of -104 dBc/Hz is achieved and it is lower compare to other designs reported in the literature. Overall architecture is complex.

Ali *et al.* [71] proposed an all-digital phase locked loop with adaptive gain estimation and constant current DCO design. In this architecture, to overcome the issues of PFD and charge pump (CP), a frequency locked loop is introduced. This architecture uses complex algorithm to estimation the gain of DCO. The difficult binary algorithm adaptively controls capacitor banks for locking a DCO frequency closest to the target frequency channel. The LC based DCO uses a capacitor bank to change the load value and achieve fine tune step. LC oscillator consumes more area and proposed architecture is complex. The PVT variations and constant g_m in the DCO are maintained by using proposed adaptive LDO. The proposed FLL design operates at supply voltage of 1 V. This architecture consumes the total area of 0.081 mm^2. This design consumes low power of 103.32 μW but the locking time of proposed ADPLL is more.

E. Koskin *et al.* [72] developed the jitter optimization model for ADPLL and investigate the dynamics of ADPLL. This model describes ADPLL the system while it is working the in the frequency acquisition, phase tracking regions, and phase acquisition. The set of control parameters describes the structure of ADPLL. It is shown in ADPLL design that the jitter of ADPLL depends upon the gain of proportional and integral filter's coefficients. This model gives quick estimation to find the optimized parameters of filter to enhance the jitter performance. Further investigation of model can be verified by simulation on cadence tool. The model is developed for DCO resolution of 1.5 ns which more as compare to other designs reported in the literature.

The following Table 2.1 depicts a summary and comparison of various digital PLL parameters available in the literature

Table: 2.1 Comparison of various parameters of DPLL and ADPLL

Sr. No.	Year	Ref.	Tech. (nm)	Supply (V)	Power (mW)	Lock time(µs)	Area (mm^2)	Jitter (rms)(ps)/ phase noise	Jitter (ptop) (ps)	Freq. (GHz)	FoM (dB)	Spur (dBc)	Technique
1.	2010	[21]	130	06-1.6	-	-	.09	288	-	0.01-0.5	-	-	Divider to keep frequency constant
2.	2011	[22]	180	1.8	7.56	-	0.25	2.6	13.6	0.9	-	-	Embedded TDC and DCO
3.	2013	[23]	180	-	6.2	-	0.26	-	-	1.15-1.65	-	-70	Signed counter Calibration for low jitter
4.	2013	[24]	110	1.2	6.02	-	0.23	4.1	30	0.24-1.68	1.95	-	Low power TDC
5.	2014	[25]	65	1		-		13.5	-	0.3	-	-	Ring oscillator modification
6.	2014	[26]	130	1.3	15.6	32	0.4	4.06	-	1.9-3.1	-	-	Ring type oscillator modification with delay less TDC
7.	2014	[27]	180	1.8	-	1	-	8.7	-	1.2-1.6	-	-	Adaptive PLL, PVT controlled
8.	2014	[28]	65	1	0.97-1.6	-	0.022	1.8	-	0.5-1.2	-243	-57	Dual path Injection locking for low jitter
9.	2015	[29]	65	0.8	0.7	-	0.006	-	2.8	0.3-1.4	-236	-42	Injection locking and DAC for ring VCO
10.	2015	[30]	65	1	2.49	0.022	0.44	0.68	2.06	8–9.5	-	-64.3	LC VCO for low jitter
11.	2015	[31]	180	1	35	-	0.7735	8.884	-	0.25-1.367	-170	-	Adaptive loop bandwidth controlled ADPLL
12.	2015	[32]	130	0.5	0.003	-	0.07	1230	-	0.001-0.005	-	-	APRed, dual loop for ultra-low power SOC

Sr. No.	Year	Ref.	Tech. (nm)	Supply (V)	Power (mW)	Lock time(µs)	Area (mm^2)	Jitter (rms)(ps)/ phase noise	Jitter (ptop) (ps)	Freq. (GHz)	FoM (dB)	Spur (dBc)	Technique
13.	2015	[33]	1.2	1.0	21	-	0.56	-	-	3.5	-	-82	ADC based Digital PLL
14.	2015	[34]	130	1.2	9	-	0.92	4.6	25.7	2.39-2.5	-	-	LC based ADPLL
15.	2016	[35]	180	1.8	18.2	7.52	0.225	-	21.9	0.14~1.45	39.4	-	Stochastic TDC based and ring DCO for ADPLL
16.	2016	[36]	45	1	3.1	-	0.01	−114	-	2.4	-	-65	Type1PLL
17.	2016	[37]	180	0.65	0.024	-	0.0075	13.1	-	0.4	-	-	Digital PLL with feed forward ring VCO
18.	2016	[38]	65	1	4.2	-	-	0.38	-	2.2	−242	-	ADC based PLL
19.	2016	[39]	65	1.2	0.36	-	-	-106	-	0.5–10.0	-	-66	ADC based PLL
20.	2016	[40]	40	0.2–1.2	.80	-	0.0040	0.80 ± 0.05	-	0.5–1	-	-	Analog CP-PLL
21.	2016	[41]	65	1	6.1	-	0.18	0.9	17.65	1.76-2.16	-238	-48.2	Injection locking VCO with additional charge pump
22.	2016	[42]	65	-	4.8	-	0.12	0.142	-	2.8-3.2	-250.3	-	LC-DCO based synthesizable IL-PLL
23.	2016	[43]	90	0.5/1	0.92	0.8	0.0625	26.5	155	0.16- 0.6	-	-	Dynamic voltage and frequency scaling
24.	2016	[44]	65	0.58	11.9	9.5	0.045	11.2	-	0.13	−222	-	Ring DCO differential And power management unit
25.	2016	[45]	28	1	0.6	-	0.0042	2	15	2	-236	-	Jitter monitoring at PFD
26.	2016	[46]	65	1.2	42	-	2.25	0.7	-	0.1-10	-	-55	Wide range with two VCOs

Sr. No.	Year	Ref.	Tech. (nm)	Supply (V)	Power (mW)	Lock time(µs)	Area (mm^2)	Jitter (rms)(ps)/ phase noise	Jitter (ptop) (ps)	Freq. (GHz)	FoM (dB)	Spur (dBc)	Technique
27.	2016	[47]	180	1.8	5.42	17	0.78	1.31	28.75	1	-236	-	ADPLL with ring VCO and phase frequency error compensation
28.	2016	[48]	40	1.1	3.8	-	0.1	0.29	-	3.96	-290	-72	LC oscillator with BB-PFD and fast locking technique
29.	2016	[49]	65	1	5.1	1	0.013	1.37	-	4	-	-50	Proportional derivative filter and power gated DCO
30.	2016	[50]	180	1.8	22.57	10	1.68	-	-	2.27-2.88	-	-	DPLL with digital calibration for charge pump
31.	2016	[51]	65	0.6 V to 1.2	1.82	-	0.0021	3.73	-	0.4–2.6	-226.0	-	Time based integral control
32.	2016	[52]	130	1		-	0.315	-	-	3.6	-	-	LC-DCO for highly digital PLL
33.	2016	[53]	65	1.2	19.5	-		-	-	0.005	-123	-	Highly synthesizable verilog code
34.	2017	[54]	65	1.1	13.5	-	0.016	0.197	-	2.5	-	-65	Time division dual calibration for ADPLL, PVT, tolerant
35.	2017	[55]	90	1	4.76	-	0.16	4.1	35.2	2.56	-242.7	-53	Cascaded PLL and DLL topology
36.	2017	[56]	130	1.2	0.52	-	0.092	-	-	0.4 -0.51	-	–141	Current-Reuse VCO and DPLL
37.	2017	[57]	130	1.2	2.6	-	0.02	-95	-	1	-	-	Reference Injected Phase-Locked Loops

Sr. No.	Year	Ref.	Tech. (nm)	Supply (V)	Power (mW)	Lock time(µs)	Area (mm^2)	Jitter (rms)(ps)/ phase noise	Jitter (ptop) (ps)	Freq. (GHz)	FoM (dB)	Spur (dBc)	Technique
38.	2017	[58]	40	1	.637	-	-	-	1.98	1.8-2.5	-	-	ADPLL Divider less Fractional-N Digital PLL
39.	2017	[59]	55	1.2	20	15	0.33	0.35	-	4.4-5.6	-236	-67	Wide range DPLL with adaptive frequency tracking technique
40.	2018	[60]	180	1.8	6.9	2.05	0.24	-	3.41	2.56	-	-71.4	DPLL design with composite PFD and variable switch loop filter
41.	2018	[61]	65	1.2	4.5	-	0.234	0.4	-	2.9-4.0	-	-72	Background calibration technique to control the bandwidth of digital PLLs
42.	2018	[62]	65	1.2	5.3	5.6	0.61	0.18	-	3.7-4.1	-363.9	-	Automatic gain controller for loop latency reduction
43.	2018	[63]	65	1	6.0	-	-	-	0.32	2.4	-242.1	-	Optimal threshold TDC and LMS calibration for ADPLL
44.	2019	[64]	180	1.8	-	20	-	-	-	5.27-5.6	-	-	Fast locking using phase error correction
45.	2019	[65]	55	1.2	4	20	0.88	1.07	-	1.5-2.04	-233	-76.3	Low power ADPLL with spur suppression for IOT applications
46.	2019	[66]	65	1.2	10.8	-	-	3.09	7.55	1-2	-	-	Computational locking and PVT invariant ADPLL

Sr. No.	Year	Ref.	Tech. (nm)	Supply (V)	Power (mW)	Lock time(µs)	Area (mm^2)	Jitter (rms)(ps)/ phase noise	Jitter (ptop) (ps)	Freq. (GHz)	FoM (dB)	Spur (dBc)	Technique
47.	2019	[67]	65	1.1	4	-	1.89	-	-	1.25	-	-	Supply insensitive DCO for ADPLL
48.	2019	[68]	40	0.68	0.28	-	0.0186	11.88	-	0.33-0.47	-156.8	-	ADPLL with ring oscillator and no TDC for low power biomedical applications.
49.	2020	[69]	130	-	37.8	7.25	-	-	-	2.1-5.5	-	-	DPLL with calibration of charge pump for constant loop bandwidth
50.	2020	[70]	14	-	1.37	-	0.0012	-	-	0.5	-	-	DPLL with high resolution DCO and FPGA implementation
51.	2020	[71]	55	1	0.103	3.7	-	-	-	2.1-3.05	208.19	-68	Frequency locked loop with the adaptive gain estimation and constant current DCO for IoT
52.	2020	[72]	-	-	-	-	-	-	2	-	-	-	ADPLL modeling using the FPGA and jitter optimization

The table 2.1 shows a various techniques used to design DPLLs and ADPLLs. It is observed from the table 2.1 that the lowest power consumption for 180 nm at output frequency of 1 GHz is 5.4 mW. The achievable lowest jitter is 1.31 ps at 180 nm technology.

2.3 Research Gaps

The most of the research is focused on design of an efficient phase locked loop to have low jitter and low power consumption [1-7]. The limits and design issues of the control path in high-performance charge-pump PLLs has been studied. Moreover, analog/CP- PLLs require a much more efforts than the digital process for migration in to new technology. The loop filter in a DPLL needs large area and it is difficult to reconfigure. In highly scaled CMOS technology, the performance of PLL is restricted by issues like device leakage and low supply voltages. To overcome these problems, we need to design PLLs using all-digital approach. However, there are many issues related to all-digital phase locked loop designs especially when we design analog circuits with digital approach. The study is also done on an all digital approach based PLL and there are many issues like more jitter, more power consumption, not portable, more area requirement, and PVT variations are found in the current all digital PLL architectures reported in the literature. Also, TDC suffers from PVT variations, more quantization error, more area and more power consumption. Achieving a high resolution with lesser power consumption is design challenge. The present ADPLL architectures suffer more locking time and complex architectures. Again, designing a low phase noise DCO with high resolution is difficult. These issues need to be addressed and provides a room for improvement in all digital PLL architectures. The various research gaps as given below:

1. TDC is the main block of exiting ADPLL. Some of the existing digital TDCs use delay line or stochastic based approach but for higher resolution and lower jitter, the power and area are increase in these approaches. Therefore, a new approach can be developed to design TDC to achieve higher resolution with low jitter and power.
2. The existing ADPLLs use a digital to analog converter (DAC) to convert a digital word to an analog voltage. This block adds jitter to ADPLL**.**
3. To tackle the problem of higher spur level in the output clock signal, the complexity of architecture is increased.
4. For finer resolution and PVT variation immune DCO, a complex calibration algorithm is generally required which increases power and area of overall design.

2.4 Objectives

Generally, ADPLL's have power and jitter constraint for wireless transceiver applications and SoC. Jitter parameter of ADPLL defines a total jitter in the transceivers. The power budget of transceivers and SOC heavily depends upon the ADPLL power consumption so it becomes more astringent parameter for ADPLL design. ADPLL, in this work, is targeted for SoC and wireless transceiver applications with power budget of < 8mW and jitter budget of < 25 ps [5,17,47]. From the research gaps, the following objectives are formulated:

1. To propose a high resolution TDC for ADPLL with low jitter.
2. To propose an efficient All Digital Phase Locked Loop for low power (≤ 8 mW).
3. To propose an efficient All Digital Phase Locked Loop for low jitter (≤ 25 ps).
4. To attempt a generic architecture for low jitter and low power for ADPLL.

2.5 Research Methodology

The DPLL and ADPLL can be designed for applications like wireless communications and System on Chips (SoCs), and etc. The various circuit techniques are used according to required applications. The following points summarizes a research methodology adopted:

1. The study of various architectures of DPLL and ADPLL has been done. The detailed study of various blocks used in PLL has been done.
2. The research work is focused to propose and design the architecture of DPLL and ADPLL to improve the various parameters such as jitter, phase noise, lock-in range, power, and area.
3. To meet the given objectives, the DPLL is designed using digital CMOS technology. DPLL is designed in CMOS 180nm and pre and post layout simulations are done to verify the design.
4. Since DPLL suffers from the issues of more area, more power, and degraded jitter. To overcome these issues, all digital approach is adopted further to design a PLLs.
5. ADPLLs are implemented using various techniques like TDC-TDC approach, hybrid architecture having PFD and TDC. ADPLL-I is designed for low power, low PVT, fast locking and low jitter. TDC is one of major component which suffers from high power. To overcome this issue, a flash based 4-bit TDC is designed using calibration. This design achieves a power of 6.35 mW and jitter of 6.6 ps.
6. To further, improve power and jitter ADPLL-II is designed using 3-bit flash TDC and bang-bang PFD. This design achieves a low jitter of 1.83 ps and power consumption of 5.94 mW.

7. ADPLL-III is designed for further improving jitter, locking time, and power consumption. A gain calibration based low phase noise VCO-II is designed. This design achieves a low power of 5.3 mW and locking time of 1.7 μs.
8. The various Electronic Design Automation (EDA) tools like cadence virtuoso for schematics and layout, synopsis design compiler for Register Transfer Logic (RTL) coding has been used to design the ADPLL.
9. ICC complier and calibre has been used to obtain an automated placed and routed layout of proposed design.

CHAPTER 3

DESIGN AND ANALYSIS OF HIGH RESOLUTION TDC

3.1 Introduction to Time to Digital Converter (TDC)

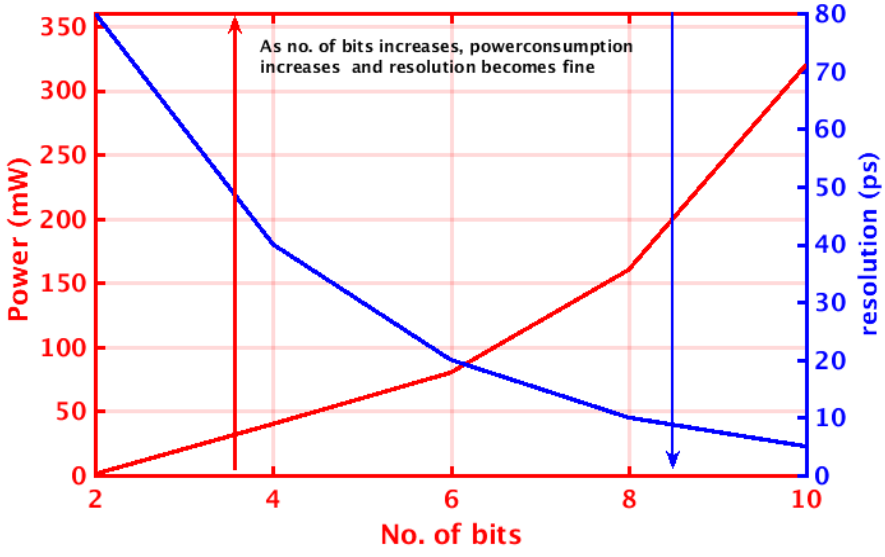
Time to digital converter (TDC) is used to measure the time difference between two clock edges and converts it into a binary digital number. TDCs are realized using the inverters, buffers, and D-flip-flops. The buffers and inverters act as the delay units and D-flip-flops are used as sampling elements. TDC has number of applications like precise time measurements, in physics for lifetime measurements in atomic and high-speed integrated circuits [13, 14, 73]. In ADPLL circuits, the TDC detects the error between the reference clock signal and the generated feedback clock signal. The resolution of TDC significantly impacts the performance parameters of ADPLL so attention is required to design a TDC architecture focusing on high resolution, wide dynamic range, lower integral non linearity (INL), lower differential non linearity (DNL), and low power. There are number of TDCs available like inverter delay line, delay line, gated ring oscillator, and Successive Approximation Register (SAR) [73].

3.2 Issues Related to Existing Vernier TDCs

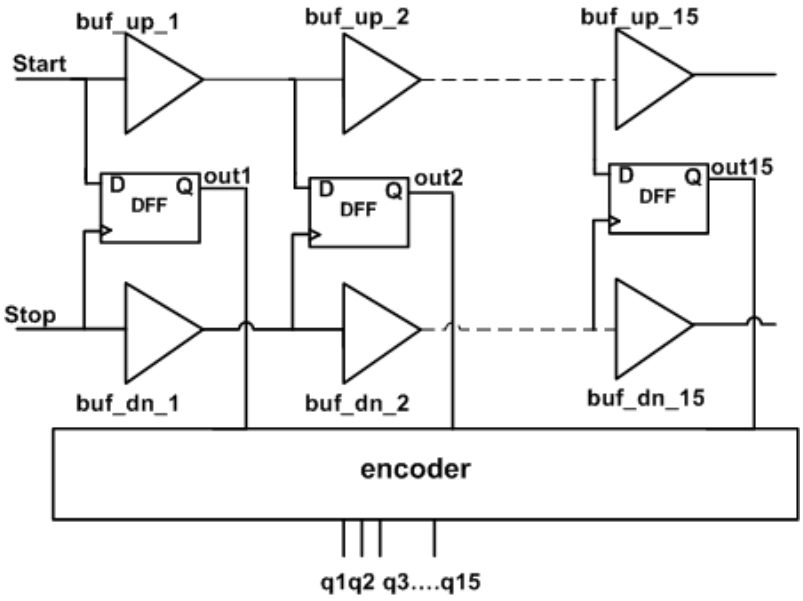
To achieve resolution lower than the single inverter delay for certain technology and wide dynamic range, Vernier TDC is designed. However, there are many issues related to Vernier TDC's [73]. To a have wide dynamic range and high resolution, Vernier TDC should have more of delay elements which costs more area and power consumption, increases quantization noise, and PVT variations. It consists of two delay chains and chain of D-flip-flops. The resolution is taken as difference of delay of two delay elements. This architecture has fine resolution but no. of bits is increased which in turns increase area and power consumption. Also, increasing the no. of bits increases PVT variations and quantization noise and needs an attention. In order to tackle this issue, a flash TDC seems to promising candidate as flash architecture is simple, compact, consumes lower area, lesser power, and easy to design. However, the flash TDC suffers from limited dynamic range. This chapter discusses the design and analysis of 3-bit and 4-bit flash TDCs in the detail. Section 3.2 explains the architecture of the Vernier TDC. Section 3.3 shows a 4-bit flash TDC and its simulation results. Section 3.4 gives the detail of 3-bit flash TDC. The conclusion is presented in the section 3.5. the following section shows a 4-bit Vernier TDC.

3.3 4-bit Vernier TDC and its Simulation Results

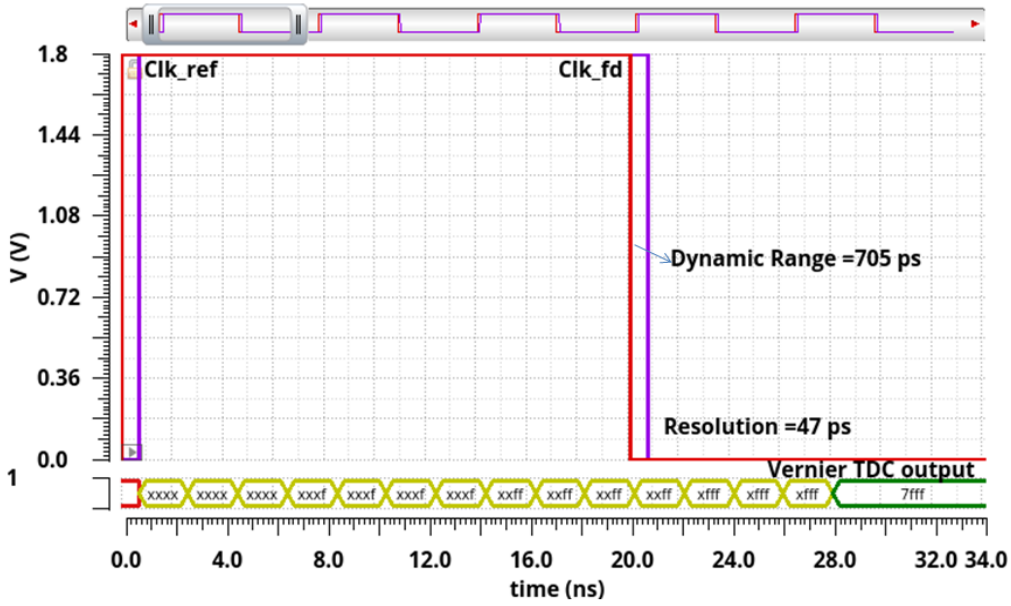
The number of high resolution TDC architectures are designed and published by many authors [73-75]. There are number of available architectures like inverter delay line, gated ring oscillator, pulse shrink, and SAR TDC [73, 75]. Vernier TDC is commonly used as it provides fine resolution and high speed. Many Vernier TDCs like 2-step and multi- step are reported in the literature [73] which solves the issue of more area requirement and higher power consumption. The researchers have work with different techniques which reduces the number of delay elements in the Vernier TDC architecture. The detail of Vernier TDC has been discussed in the section 1.7. The major issues with Vernier TDC are increase in power consumption and area with increase in the number of bits as shown in the Fig. 3.1 (a). To solve these problems, number of TDC architectures had been proposed [73-75] but the major issues with these architectures are complexity, more power, and area consumption. Typical n-bit Vernier TDC consists of 2 (2^n-1) buffers and (2^n-1) D-flips-flops. 4-bit Vernier TDC is shown in the Fig. 3.1 (b) [73]. For designing an ADPLL, 4-bit Vernier TDC is sufficient to characterize its parameters. The output of 4-bit Vernier TDC (here it is called as TDC1) is shown in Fig. 3.1 (c). It is observed from graph that it takes (n-1) clock cycles to generate output. The power consumption of Vernier TDC is 1.2 mW which is more and thus increases the overall budget of power consumption by ADPLL. The periodic jitter is calculated and it has value of 3.1 ps as observed in the graph shown in the Fig. 3.2 (a). The power consumed by the 4-bit Vernier TDC is 1.2 mW in SCL 180nm at the supply voltage of 1.8V. In order to tackle the issues of Vernier TDC like more power, area, and periodic jitter, a simple flash architecture for TDC is proposed.



(a)



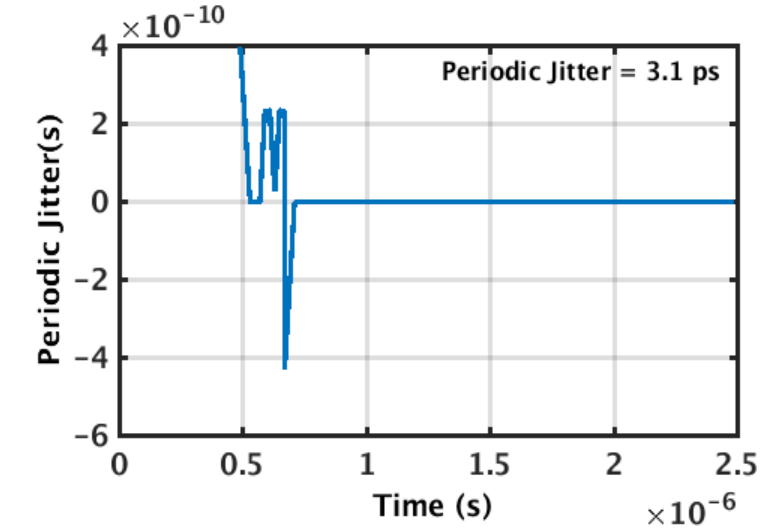
(b)



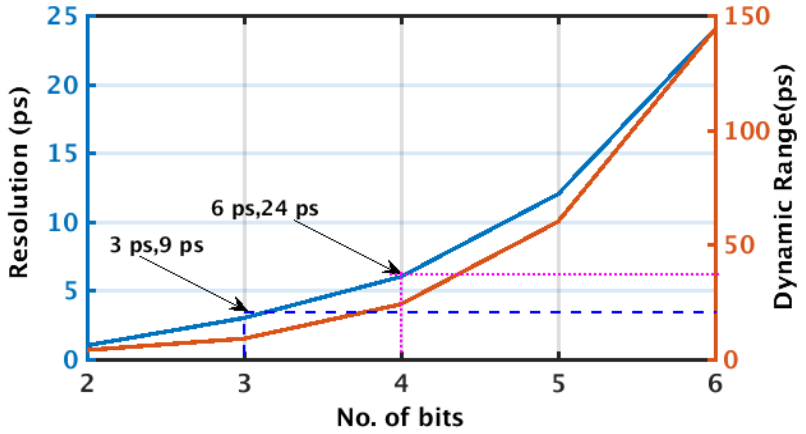
(c)

Fig. 3.1 (a) Power consumption and resolution variation with number of bits, (b) 4-bit Vernier TDC1, (c) Output of Vernier TDC1

This architecture is simple, compact, and easy to design. It solves the problems of conventional Vernier TDC. The proposed flash TDC is designed with different number of bits to achieve high resolution, low periodic jitter, and low power consumption. Fig. 3.2 (b) shows a variation of resolution and dynamic range with the number of bits of flash TDC. The 4-bit and 3-bit are designed for resolution of 6 ps and 3 ps respectively. Though these designs achieve finer resolution, low area and power but the dynamic range is very limited due to the flash architecture.



(a)



(b)

Fig. 3.2 (a) Periodic jitter of Vernier TDC1, (b) Resolution and dynamic range variation with number of bits of flash TDC

The resolution of TDC2 and TDC is determined by taking the difference between two propagation delay values as shown in equation (1.10). The relation between dynamic range, resolution, and number of bits for flash TDC is given as [73]:

$$DR = n.(\tau 1 - \tau 2) \tag{3.1}$$

$$P_{avg,core} = freq.\frac{DR}{T_{lsb}}(E_{rise}^{buf} + E_{fall}^{buf} + \frac{1}{2}(E_{rise}^{DFF} + E_{fall}^{DFF}) + C_L V_{DD}{}^2) \tag{3.2}$$

where DR is the dynamic range, n is number of bits and $(\tau 1 - \tau 2)$ is the resolution of flash TDC. $\tau 1 and \tau 2$ are the delay of consecutive buffers in flash TDC. $P_{avg,core}$ is the average power consumed by flash TDC, $freq$ is the frequency of operation, T_{lsb} is the resolution of TDC, E_{rise}^{DFF} & E_{fall}^{DFF} are the rise and fall energies of D-flip-flops, E_{rise}^{buf} & E_{fall}^{buf} are the rise and fall

energies of buffers, V_{DD} is supply voltage and C_L is load capacitance. As seen from equations (1.10), (3.1), and (3.2), dynamic range depends upon delay difference (resolution) between consecutive two delay elements and no. of delay elements. It is also observed from equations that lowering dynamic range helps to achieve fine resolution and reduces power consumption of TDC. The quantization noise of TDC is other issue which needs to be addressed [13] as it directly contributes to the phase noise of ADPLL. The resolution of TDC affects the quantization error. As the resolution becomes finer, the quantization error tends to decrease. Further, the quantization error of phase noise significantly affects the phase noise of ADPLL. The phase noise of ADPLL depends upon the quantization error, bandwidth of ADPLL, output frequency of ADPLL and offset frequency at which the phase noise is measured. The phase noise of TDC block is given as [13]:

$$PN_{TDC} = \frac{2\pi T_{lsb}}{T_c\sqrt{12}}\sqrt{\frac{f_{bw}}{f_{ref}}} \tag{3.3}$$

where PN_{TDC} is the phase noise of TDC block at output of ADPLL, f_{bw} is the bandwidth of ADPLL, f_{ref} is the reference frequency, and T_c is the clock period of output frequency of ADPLL. From above equation, it noted that resolution play key role in the phase noise of ADPLL due to TDC block. To improve the phase noise, resolution should be fine. The limited dynamic range of flash TDC is other major issue for designing ADPLL designs. Therefore, in order to tackle issue of limited range and to achieve the fine resolution, the number of bits for proposed flash architecture is taken as 4 and 3. The next section explains the details and analysis for 4-bit and 3-bit flash TDC.

3.4 Proposed 4-bit Flash TDC and its Simulation Results

For designing the ADPLL-I for SoC applications, the power consumption is less than 8 mW at output frequency in range of 0.6 GHz to1.6 GHz is desirable [17]. A 4-bit flash TDC (here it is called as TDC2) is proposed for resolution of 6 ps and periodic jitter of 0.75 ps to obtain the given specifications of ADPLL-I. The considerable parameters offered by TDC are resolution and dynamic range which impact the performance parameters of ADPLL [73-74]. Traditionally, TDC utilizes the propagation delay of buffers which act as delay elements in Vernier delay line (VDL as shown in the Fig. 3.1 (b)) [73]. The resolution of VDL TDC (called as TDC1) is taken as difference of delay between the two-unit delays lines, *i.e.* ($\Delta\tau_{ver} = \tau_{1\_}\tau_2$) as shown in the Fig. 3.1 (b). The range is resolute by the count of delay elements used in two parallel lines. Though this method gives the large dynamic range and high resolution but at the

cost of more area and power. As number of bits increases, the resolution becomes more finer but the power consumption is increasesd as shown in the Fig. 3.1 (a).

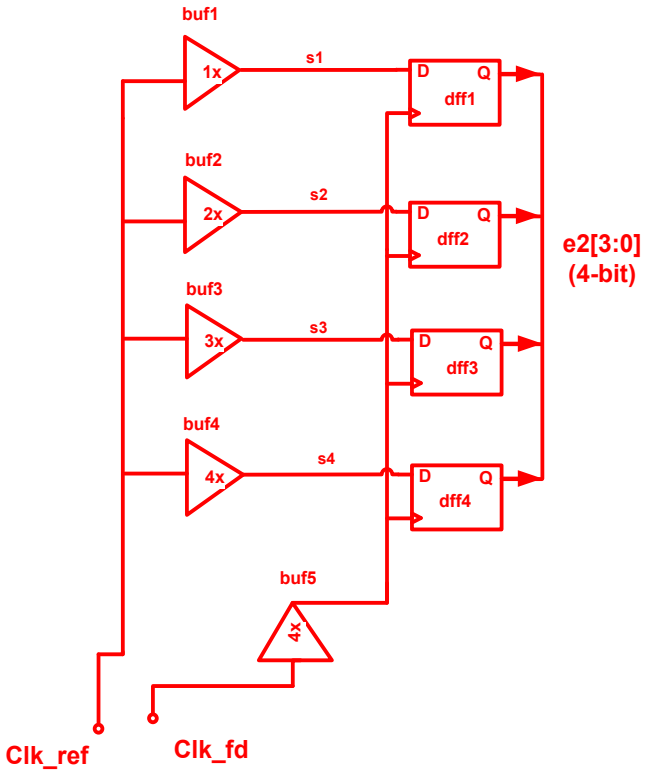
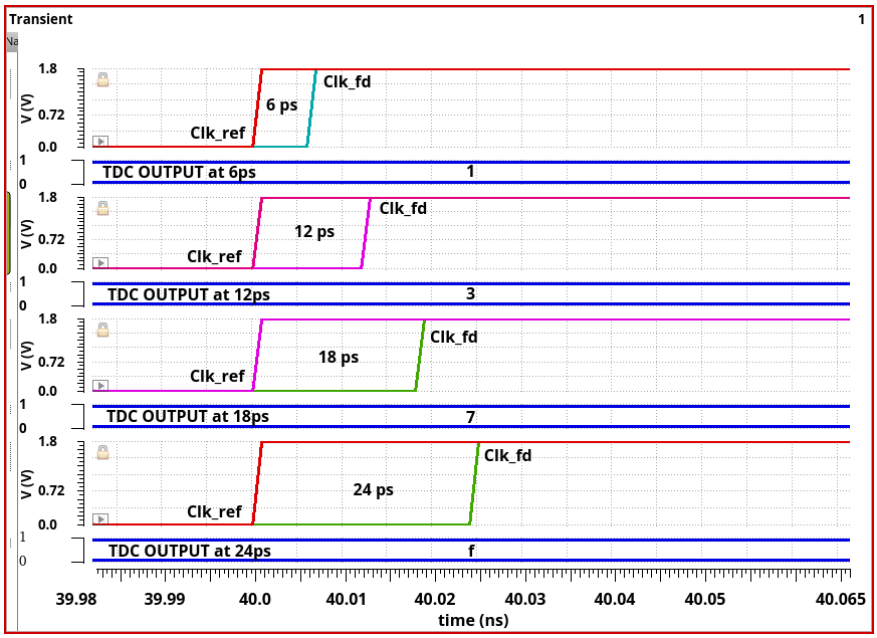
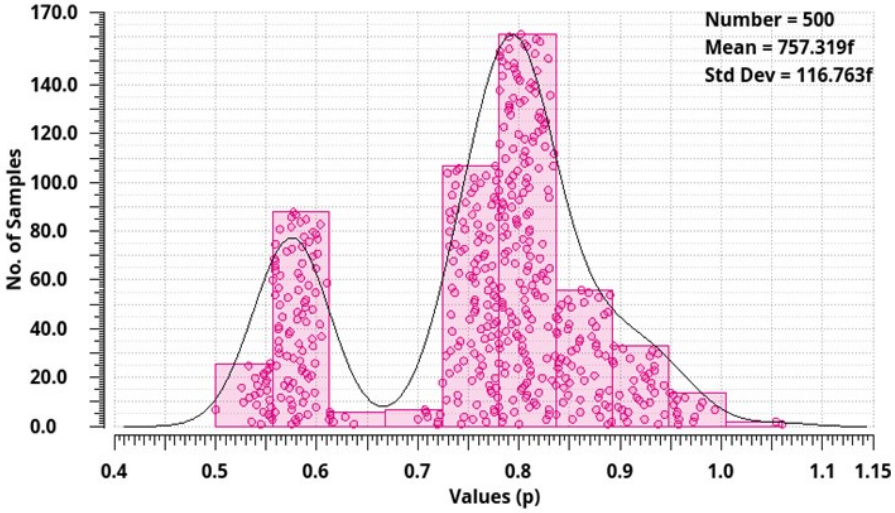


Fig. 3.3 Proposed 4-bit flash TDC2

For TDC1, since the resolution of TDC1 is prone to PVT variations [73-74], only 4-bit Vernier based TDC (TDC1) is used which gives the advantage of wide dynamic range in the range of few nanoseconds. To reduce the area, power, and also to diminish the variability in the delay cells, the 4-bit flash TDC (TDC2) is proposed. The proposed 4-bit flash based TDC *i.e.* TDC2 is simpler, fast, and consumes lesser number of delay elements as compared to Vernier delay line based 4-bit TDC (TDC1). The proposed 4-bit flash TDC2 is implemented using set of equally spaced four buffers (buf1-buf4) in addition to D-flip-flops (dff1-dff4) as sampling units shown in Fig. 3.3. The reference signal Clk_ref is given to these set of buffers (buf1-buf4). To maintain the fine resolution and measurement accuracy, feedback clock Clk_fd is given to the delay cell buffer (buf4) [73]. The delay cells buf1-buf4 with the different driving strengths are chosen in order to have decreasing delay *i.e.* ($\tau_1 > \tau_2 > \tau_3 > \tau_4$) from top to bottom. The number of bits of 4-bit flash TDC2 is limited to four for low area and power consumption. The proposed 4-bit flash TDC achieves a resolution of 6 ps. Fig. 3.4 (a) shows the output of 4-bit flash TDC. For input difference of 6 ps, the output is '1H' and for input delay of 24 ps, the output corresponds to 'fH'. The periodic jitter of 4-bit flash TDC2 is 0.75 ps as shown in the Fig. 3.4 (b).



(a)



(b)

Fig. 3.4 (a) Output of 4-bit flash TDC2, (b) Period jitter of 4-bit flash TDC2 with Monte Carlo simulation

The power consumed by proposed 4-bit flash TDC is 0.39 mW. The next section gives the insights and describes the 3- bit flash TDC.

3.5 The need to design 3-bit Flash TDC and Proposed 3-bit Flash TDC

ADPLL-II is designed for speed high application like wireless transceiver applications in which the periodic jitter and power consumption constraint is very astringent and also requires a low area, low power, and low periodic jitter TDC and DCO. TDC and DCO significantly impact the ADPLL-II parameters [73-74]. For ADPLL-II, periodic jitter < 2 ps at output frequency of 1.6 GHz is required for wireless transceiver applications [4-5]. The proposed 4–bit flash TDC2 achieves the periodic jitter of 0.75 ps and high resolution of 6 ps which are not sufficient to achieve the ADPLL-II specification. In order to meet the parameter specifications of proposed

ADPLL-II, another version of 3-bit flash TDC is proposed. The 3-bit flash TDC is designed for 0.2 ps jitter and resolution of 3 ps in order to achieve the ADPLL-II design specifications.

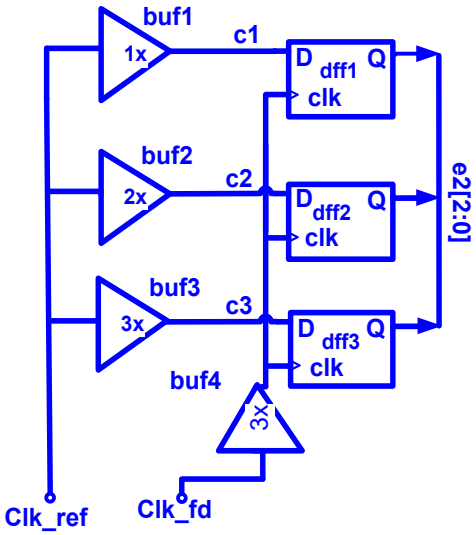
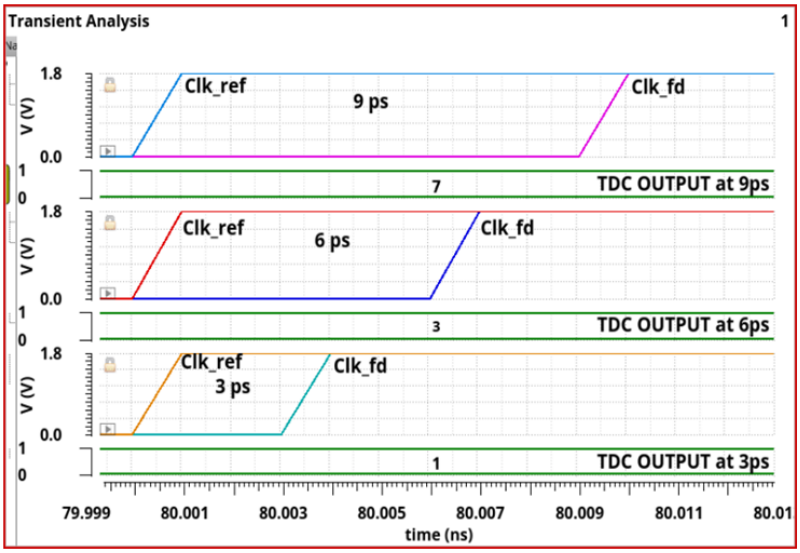
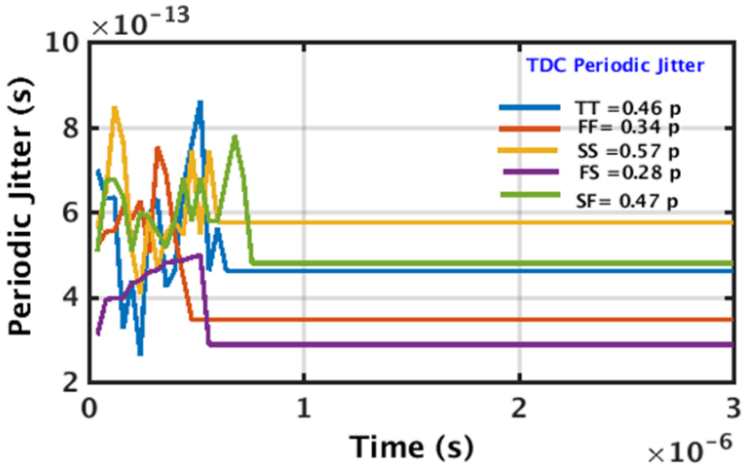


Fig. 3.5 Proposed 3-bit flash TDC

In this section, the 3-bit flash TDC is proposed which enhances performance metrics of ADPLL-II thus helps to achieve low jitter, fast locking, and low power ADPLL design. To achieve reduced the area, power, and PVT variations, simple and high-speed flash architecture based 3-bit TDC is proposed as depicted in the Fig. 3.5. The proposed 3-bit flash TDC has a set of 3 D-flip-flops and buffers. At the input of buffers (buf1-buf3), the reference clock Clk_ref is provided. The architecture of proposed 3-bit flash TDC consists of 3 buffers (buf1-buf3) of relatively equal delay difference of 3 ps between them i.e., between buf1-buf2 and buf2-buf3 and therefore they are chosen to have increased delay.



(a)



(b)

Fig. 3.6 (a) Output of proposed 3-bit TDC for different input delay difference output till 3 ps resolution, (b) Periodic jitter of proposed 3-bit flash TDC at PVT corners

Table 3.1: Relative comparison of parameters of proposed TDCs

Parameters	TDC1 [73] 4-bit	TDC2 4-bit	TDC 3-bit
Delay Elements	30	5	4
Number of Bits	4	4	3
Clock Cycles	15	1	1
Dynamic Range (ps)	Higher (705)	Lower (30)	Lower (9)
Resolution (ps)	47	6	3
Periodic Jitter (ps) (at TT Corner)	3.1	0.75	0.46
Power Consumption (mW)	1.2	0.39	0.35
Architecture Type	Vernier	Flash	Flash

The D-flip-flops (dff1-dff3) acts as sampling elements. The Clk_ref is provided at the input of buffers (buf1-buf3) and the D-flip-flops (dff1-dff3) samples the input provided to (buf1-buf3) at rising edge of clock Clk_ref. The delay cells (buf1-buf3) have relative decreasing driving strengths and thus they provide the increasing delay i.e. ($\tau_3 < \tau_2 < \tau_1$) from bottom to top [73] and this generates a resolution lower than the minimum delay of CMOS inverter in a given technology node. For an instance, delay for buf1 is 46 ps and buf2 is 43 ps respectively. The relative delay difference between them is taken as resolution of proposed flash TDC. The Vernier TDC [73] concept is used to achieve a fine resolution in this architecture.

As this flash TDC is prone to PVT variation, later in the preceding chapter 5, calibration is done to achieve low power, low area, fine resolution and lesser PVT variations TDC. The output of proposed TDC is depicted in the Fig. 3.6 (a). It is apparent from graph that the output is '1H' corresponds to minimum input delay difference of 3 ps and output is '7H' for maximum input delay difference of 9 ps respectively. The periodic jitter value after simulation for 3-bit flash TDC is 0.46 ps as shown in the Fig. 3.6 (b). The power consumed by the proposed 3-bit flash TDC is 0.35 mW. The PVT variation of 23% to 30 % is observed in the 4-bit and 3-bit proposed TDC. Table 3.1 shows relative comparison of various parameters of Vernier, proposed 4-bit and 3-bit flash TDCs. The power consumed by the 4-bit Vernier TDC is higher as compared to proposed flash TDC. The resolution of Vernier TDC is lower as compared to flash TDCs and also the number of delay elements used to design the Vernier TDC is more as compared to flash TDCs.

3.6 Conclusion

In this chapter, a 4-bit Vernier TDC1 and its issues are discussed. The two high resolution 4-bit and 3-bit flash TDCs are proposed to tackle the problems of Vernier TDC1. The section 3.3 and 3.4 shows the simulation results for proposed 4-bit flash and 3-bit flash TDC designs respectively. The 4-bit TDC2 and 3-bit TDC achieve the resolution of 6 ps and 3 ps respectively. A 4–bit flash TDC2 and 3-bit flash TDC achieves a low periodic jitter of 0.75 ps and 0.46 ps respectively. The proposed TDC architectures are high speed as they give output only in 1 clock cycle. The proposed TDC architectures are suitable for designing a low power, low area, and low jitter ADPLL. The power consumption directly depends upon no. of delay elements used in the flash TDC, as no. of delay elements reduced in TDC as compare to TDC2, consecutively, power consumption is also reduced in the TDC. Though, the proposed 4-bit and 3-bit TDC achieves the high resolution and low periodic jitter however they suffer from the PVT variations. The PVT variations in the TDC degrade the periodic jitter of ADPLLs. Therefore, in order to tackle the issues of proposed flash TDCs, the digital calibration is used which will be described and discussed in the latter chapters. The combination of 4-bit Vernier TDC1 and 4-bit flash TDC2 are used in ADPLL-I architecture. 4-bit Vernier TDC1 gives a wide range which helps to achieve wide locking range. The 4-bit flash TDC2 is fast and therefore helps to achieve fast locking of ADPLL. The flash TDC2 also consumes low power. Also, TDC2 with calibration achieves a low PVT variation and enhanced jitter. Overall TDC1 and TDC2 aids to achieve fast locking, low jitter, and low power ADPLL-I.

CHAPTER 4

DESIGN AND ANALYSIS OF DIGITAL PHASE LOCKED LOOPS

4.1 Introduction to DPLL

The digital phase and frequency detector, loop filter, charge pump, and analog VCOs are key blocks of DPLL. DPLLs are employed in number of applications like wireless transceivers, SOC, and clock recovery circuits. DPLL is smaller in area, consumes lower power as compare to analog PLL. The digital approach to design a DPLL gives number of advantages over the APLLs. This chapter presents two architectures of digital PLL.

4.2 Issues of Analog PLL

Analog PLL (APLL) [9-10, 12] consists of nonlinear analog multiplier which acts as phase detector, loop filter, resistors, capacitors, and the VCO. In deep sub-micron technologies, the performance of APLL is mostly restricted by the various short channel effects (SCE's). SCE's severely affect the performance metrics like the phase noise, jitter, and reference spurs in the PLLs [9-10]. The key issues of APLL are that it suffers from circuit non-idealities like parasitic capacitances, PVT variations, and mismatches [10, 12]. DPLL suffer from many issues like more area, leakage currents, and PVT variations. The analog filters used in the APLL and DPLL designs are complicated and large in size which slows the locking process. The scalability and portability are also problems which restrict the porting of APLL and DPLL to the newer emerging technologies. The maximum detectable phase error by APLLs is in the range of $\pm\pi/2$ rads. This result in limited lock-in ranges as compared to the DPLL designs. The detection of frequency variation is not possible in the APLL architectures. This also leads to delay in locking process.

Lately in recent years, all-digital phase locked loops (ADPLLs) have attracted interest and the attention of the industry and many researchers. This is majorly because the conventional charge pump (DPLLs) has limitations such as PVT spreads, costly analog process, more power supply voltage and other technological issues like -mismatches, leakage current in lower technology nodes. The conventional DPLLs also suffer from other issues such as slow settling time and degraded jitter [10, 22]. On other hand, ADPLL is digital-in nature and works with discrete signals in digital domain. It leads ADPLL to have many advantages. Primarily, ADPLL gives advantages of portability and scalability to newer technologies and superior performance parameters as compared to the conventional DPLLs. ADPLL design gives a number of advantages over conventional DPLL designs. In order to obtain the low power and

improved periodic jitter, DPLL architectures in this work are designed with digital approach. The digital process gives advantage of low power, low area, and less design efforts. The DPLL designs are designed with digital approach in order to obtain low power and low area. Loop filters are also designed using MOSCAPs and transmission gates which reduce the area and power consumption of DPLL. The DPLL architectures are designed to meet the given specifications of power of 8 mW and periodic jitter of 25 ps. To avail the benefits of DPLL and to overcome the issues of APLL designs, DPLL are proposed using digital approach in this work.

4.3 The need to Design DPLL

The issues related to conventional APLL and DPLL have been discussed in the section 4.1. The digital design methodology has number of advantages over analog process like portability, scalability, low cost, and reduced time to market [12]. The main disadvantages of APLL are like temperature drift and it's vulnerable to the change of voltage. On the other hand, Digital Phase Locked Loops (DPLLs) doesn't have these disadvantages and therefore it gives advantages like high stability and reliability [12]. Table 4.1 shows the comparative analysis of APLL, DPLL, and ADPLL.

Table: 4.1 Comparison of APLL, DPLL, and ADPLL

Properties	APLL [9]	DPLL [10]	ADPLL [12]
Blocks	Analog multiplier, VCO, loop filter	PFD, VCO, loop filter, charge pump	TDC, DCO, digital loop filter
Type	Type-1	Typle-2	Type-2
Loop Gain Dependency	Loop gain depends upon signal amplitude	Loop gain independent of signal amplitude	Loop gain independent of signal amplitude
Response	Non-Linear Response	Linear Response	Linear Response
Speed	slow	fast	fast

This chapter shows a design and analysis of digital PLL. Two architectures of charge pump PLL are designed in this chapter. System level architecture, different functional blocks like PFD, charge pump, and VCO-I are described. Section 4.3-4.10 illustrates the novel system level DPLL-I and its simulation results. The proposed fast phase frequency detector (PFD-I) with dynamic logic is used to design DPLL-I. The low phase noise voltage controlled oscillator (VCO-I) using the standard CMOS inverter gates is designed. The analysis of CMOS inverter

is done which is used as variable capacitor to adjust the frequency of VCO-I. The design and analysis of DPLL-II with proposed PFD-II, VCO-I, and charge pump (CP) is presented in the section 4.11- 4.16. The various blocks of this architecture are designed using digital approach and switches only. Section 4.17 discusses the disadvantages of DPLL and requirement of ADPLL design in the current applications. Section 4.18 concludes the chapter.

4.4 Design of DPLL-I

Traditionally, a PLL can be designed using analog and digital methodology. The primary blocks of DPLL are PFD, VCO, loop filter, and dividers [9-12]. As discussed earlier in above section that digital PLL gives a number of advantages over the conventional analog PLL. Therefore, to tackle the problems of analog processes involved in designing the DPLL, a digital methodology is used to design the DPLL. The charge pump is analog block which severely affects the performance of PLL. The mismatch between sources and sink currents of conventional analog CP also affects the PLL locking process, jitter, and phase noise. The separate analog circuit techniques are required to tackle these above said issues. The other design problems which require a consideration in designing the PLL are larger silicon area and more design effort, portability, and scalability to newer technologies. Fig. 4.1 shows the complete DPLL-I architecture. In this section, the proposed DPLL has simple methodology, consumes lower power, and less area with fast locking time.

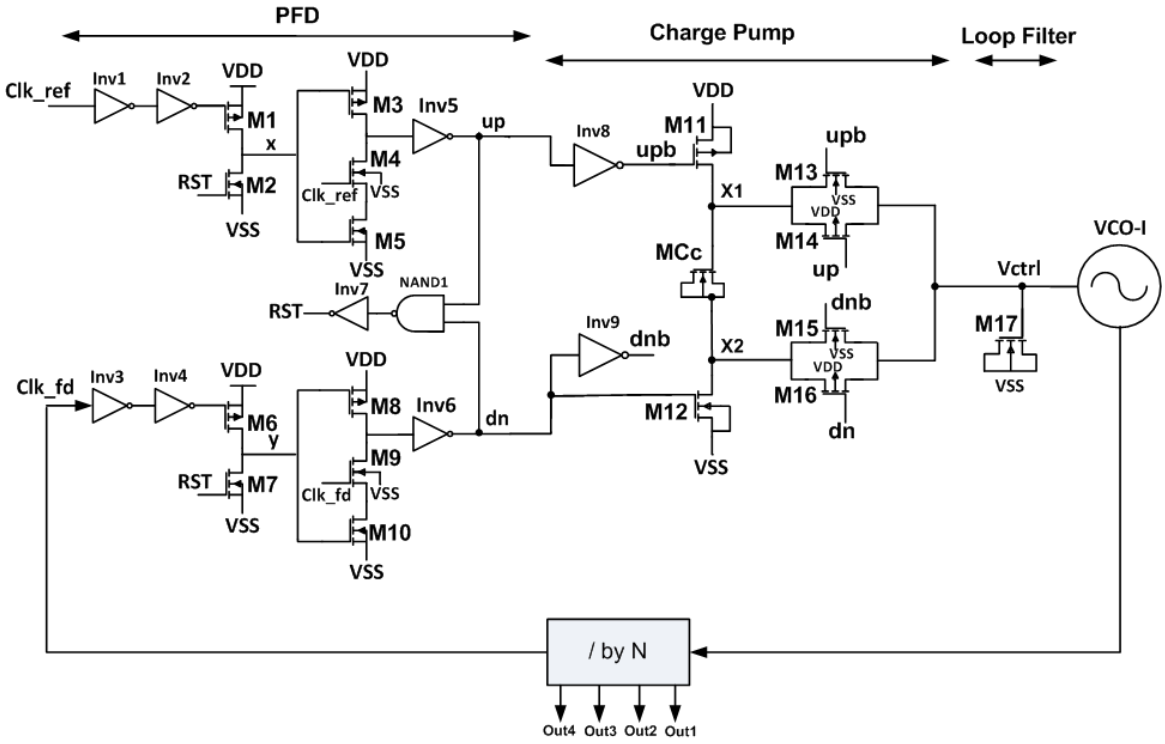


Fig. 4.1 Proposed DPLL-I design

After charge pump, PFD is other block which affects the DPLL parameters. The frequency phase detector has issues of dead zone and blind zone which degrades a performance of DPLL. In this work, dynamic logic based fast PFD is proposed. A pseudo differential VCO-I is proposed which works at frequency of 1.6 GHz. A DPLL-I is proposed which consists of fast dynamic logic-based PFD, digital charge pump, and pseudo differential VCO-I. The following section explains the design of proposed dynamic logic-based PFD for DPLL-I architecture.

4.5 Phase Frequency Detector (PFD-I)

The resettable NAND gate and D-flip-flops are the primary blocks of conventional PFD design [9-11]. The performance of PFD is degraded by the design issue such as blind zone which also affects the performance of the DPLL. When rising edge of the clock Clk_ref comes prior to the falling edge of the reset pulse, blind zone occurs [76]. Also, the width of reset pulse depends upon the up and down (dn) pulses width when they are at logic '1' and also depends upon the total delay of the circuitry from input to output in the reset path [9-10]. It leads to dead zone, if reset pulse width is narrow and therefore the PFD design requires the wider widths of up and dn signals. However, this degrades the locking time of the DPLL design. The designs of PFD reported in [76-77] are high speed and also solves the above-mentioned issues but still requires more attention. A proposed dynamic logic-based PFD-I design tackles the above said issues. The proposed PFD-I is shown in the Fig. 4.2. It comprises of two dynamic logic based fast D-flip-flops (D-FFs).

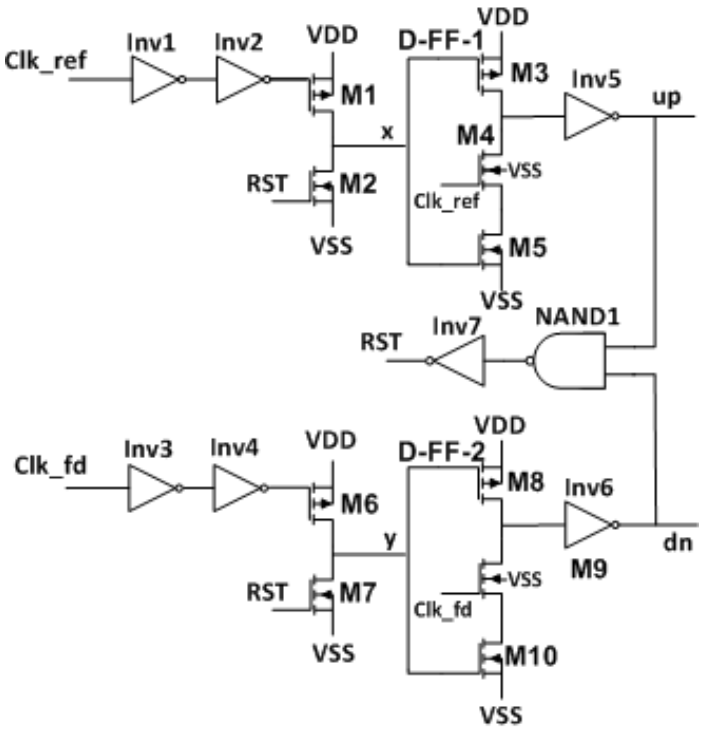


Fig. 4.2 Proposed PFD-I with W/L for M1, M6, M3, and M8 and M2, M7, M4, M5, M8, and M10 =2.96/0.18 µm and 1/0.18 µm respectively

A D-FF used in PFD-I is designed using inverter Inv5 and MOSFETs M1-M5 in upper arm, and similarly inverter Inv 6 and MOSFETs M6-M10 in lower arm. The pre-charging of node x and y are delayed with the additional delay at the input nodes of M1 and M6 MOS transistors which avoids blind zone. The τ_{pch} (where τ_{pch} is the charging time to charge the node (x or y)) from 0 to VDD which should be less than the delay τ_1 (provided by Inv1 and Inv2) or τ_2 (provided by Inv3 and Inv4) respectively. The pulse width of RST signal depends upon the total delay provided by a D-FF, NAND1, and inverter Inv7. RST pulse width is narrower because of faster D-FF-1 and D-FF-2. Hence it reduces the probability of occurrence of rising edge of the Clk_ref while RST pulse is high. Similar argument is valid for the lower arm. The reset path will be activated by M2 and M7 as the clock Clk_ref and Clk_fd comes into the phase and during this time up and dn signals are at logic '1'. This will lead to discharging of up and dn signal to logic '0'. The problem of dead zone problem comes into picture when phase difference between up and dn pulses is zero. In the case, the proposed dynamic logic-based PFD-I with inverters (Inv1 and Inv4) and gates in the reset path (NAND1 and inverter Inv7) gives an enough time for up and dn pulses to become stable and wide so that dead zone is avoided. The pulse width of up and dn signals controls the variation in the control voltage which changes the frequency of VCO-I as shown in the Fig. 4.3. It is seen from the Fig. 4.3 that control voltage increases as width of up signal increases and on other hand, the control voltage is decreased as width of dn signal increases.

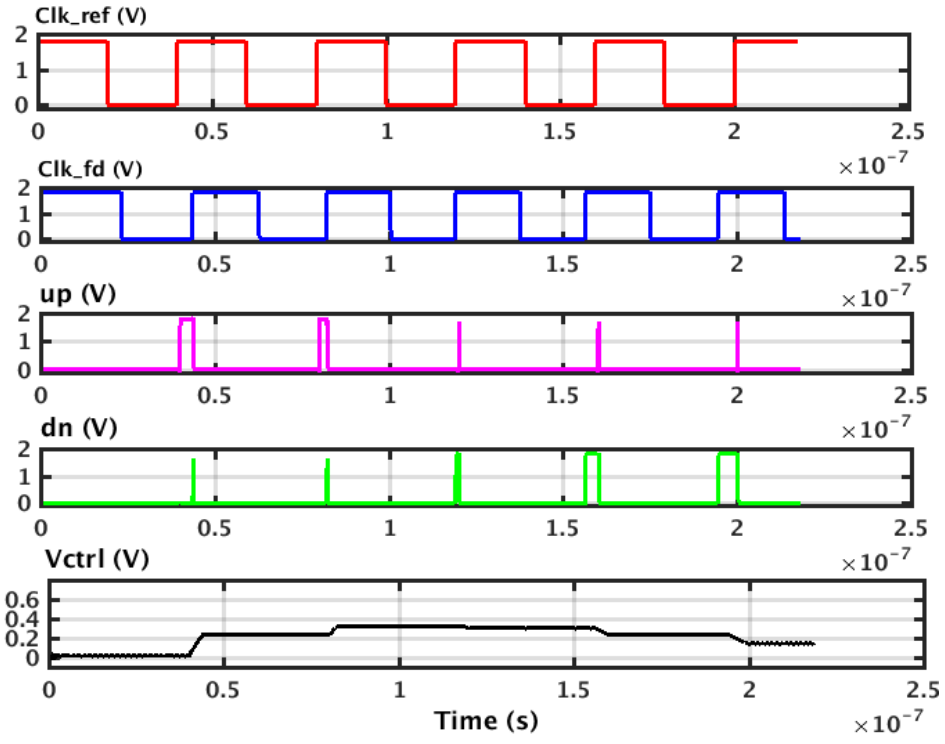


Fig. 4.3 Transient simulation of up and dn signals with control voltage

When PLL is under the locked condition, the widths of up and dn pulses become equal, the control voltage settles down at constant value.

4.6 Charge Pump

The charge pump (CP) is a most important block in the PLL architecture. The charge pump immensely affects the jitter, locking time, and phase noise of the PLL designs. Normally, the charge pump uses current mirror circuit which act as constant source of current and thus helps to avoid the current sensitivity of up and dn pulses. As the current mirror based charge pumps are analog in nature so they are prone to mismatches and PVT variations. For low jitter [9-11], the current matching between charging and discharging current is necessary as current mismatches in CP causes a ripple in the control voltage. Therefore, it will degrade in the performance parameters of PLL. Also, the charge pump block significantly affects the overall power budget of PLL. It majorly consumes the power after the VCO which also consumes the higher amount of power [78-79]. The charge pump [40] is very compact, immune to PVT variations, and consumes low power and used in DPLL-I architecture as shown in the Fig. 4.1. It consists of switches, inverters, and switch capacitors. The W/L ratio for M11 and M12 is 1/0.18 µm and 0.54/0.18 µm. The charge pump is given the up and down pulses provided by the PFD and CP generates the charging and discharging currents. The charge pump design reported in [40] shows a very less mismatch between sourcing and sinking currents because it uses a switch capacitor. The output of charge pump is fed to the loop filter which is described in the following section.

4.7 Loop Filter-I

The proposed loop filter design which is used in DPLL-I is shown in the Fig. 4.4. The values of the capacitor and resistor in loop filter drastically impacts the stability of DPLL [9-11]. In this DPLL-I, MOS based capacitor (called MOSCAP) is used to design the loop filter. To achieve the optimized RMS and periodic jitter for DPLL-I architecture, value of capacitor is determined. The output control voltage generated by charge pump is averaged by the loop filter in the DPLL.

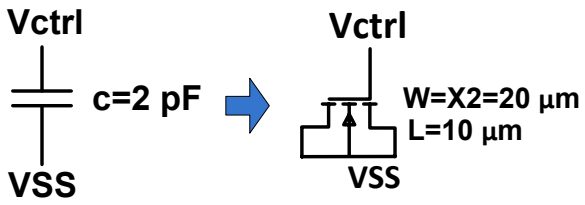
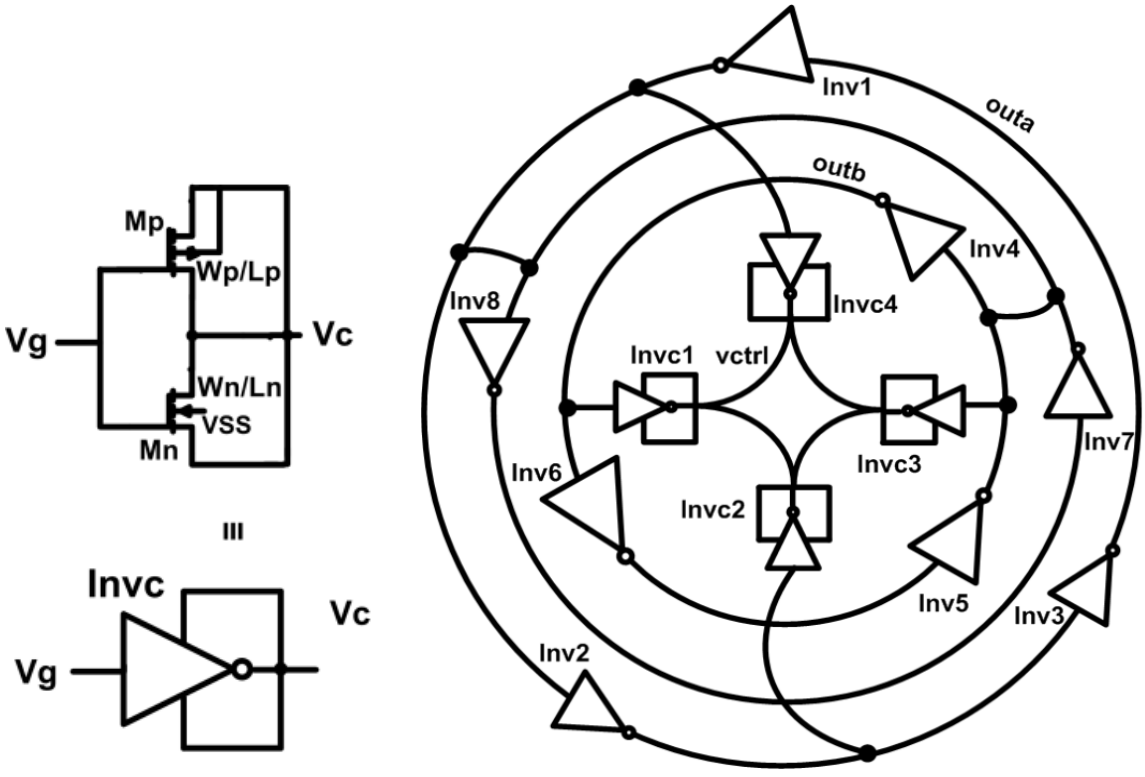


Fig. 4.4 Loop filter-I with W/L as 20/10 µm

The loop filter also controls the noise and ripple in control voltage which helps to improve the jitter in VCO output frequency. The passive resistor and capacitor in the conventional loop filter costs more area and power consumption due to their bulky size [9-11]. The proposed PFD-I incorporated in DPLL-I architecture and also reduces the locking time as compared to other PFD-I designs given in literature [76-77, 80]. The output of filter is given to VCO-I to tune the frequency of proposed VCO-I. The next section gives the details of proposed VCO-I.

4.8 Voltage Control Oscillator (VCO-I)

The VCO is heart of PLL architecture [9-10]. The MOS based ring oscillators are compact, easy to design, consumes lesser area, and power as compare to LC oscillators. Also, inductor and capacitor consume very large area and have issues like PVT variations [61,69]. Further, implementing the LC oscillator using CMOS is difficult and degrades the phase noise performance. The objective to use digital CMOS technology in PLL designs, so LC oscillator is not used. The major focus in designing a VCO is to design with inverters only and thus reduces a lot of design effort and to achieve low phase noise, low area, and low power as compare to existing VCO designs in 180nm. The control voltage generated by the loop filter is used to vary the frequency of VCO-I. Fig. 4.5 (a) shows a structure of Inverter-cap. Inverter-cap consists of PMOS and NMOS.



(a) (b)

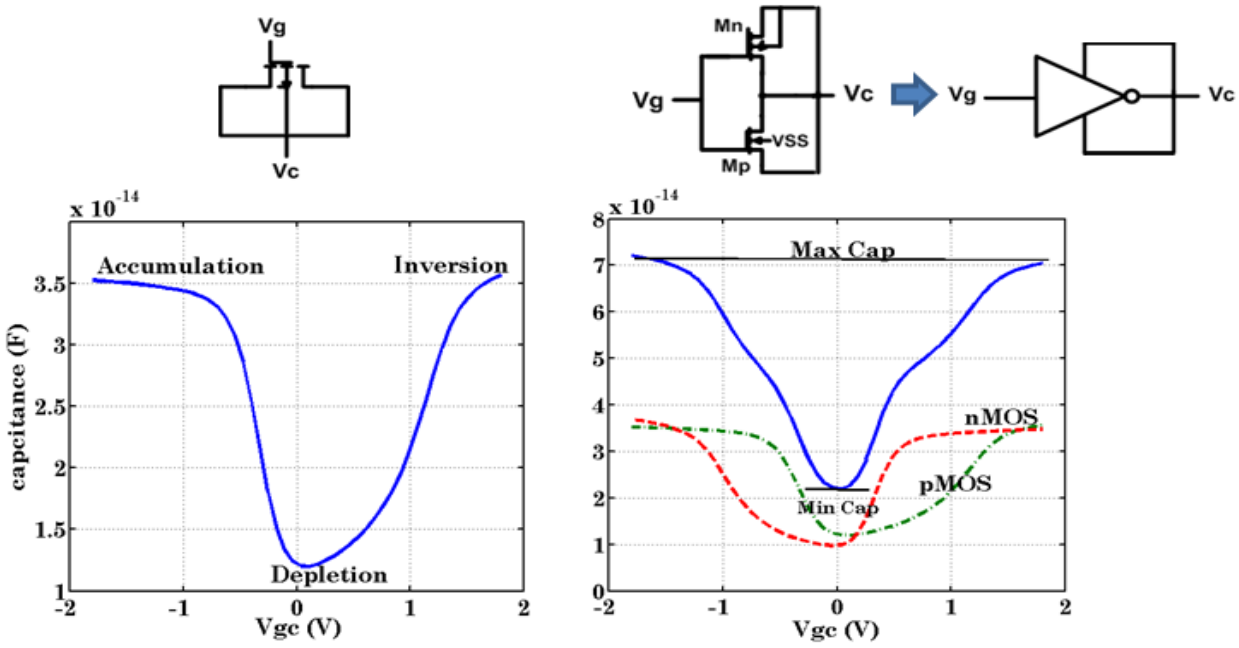
Fig. 4.5 (a) Inverter-cap with Mp and Mn W/L as 2.3/2.3 and 2.3/2.3 µm respectively, (b) Proposed VCO-I schematic design

The drain, source, and bulk terminals are connected to ground and control voltage (V_g) is given at the gate terminals of PMOS and NMOS of Inverter-cap. The novel pseudo differential methodology is followed in this work, CMOS inverter-based voltage controlled oscillator is proposed as shown in the Fig. 4.5 (b). VCO-I is consisting of 3 CMOS inverter stages and used to generate higher frequencies. The ripple in the control voltage degrades the phase noise performance of the PLL. The pseudo differential method is followed in the proposed VCO-I which offers noise immunity and improves the phase noise. The delay elements for VCO-I are CMOS inverters (Inv1-Inv6). Inverter-cap gives more linear variation in the capacitance as compared to MOSCAP. Therefore, it is used in the proposed VCO-I. The variable capacitors are used to adjust the frequency of VCO-I using other set of inverters (Invc1-Invc4) between two rings. To maintain the constant phase difference of 180˚, Inv7, and Inv8 are used which act as phase interpolator.

4.8.1 Analysis of CMOS inverter as a Variable Capacitor and Noise Analysis of Proposed VCO-I

In this section, the noise analysis of the VCO-I is done on basis of noise contributed by all the CMOS inverter gates in design. The inverter gate is used variable capacitor instead of MOSCAP. The capacitance of MOSCAP is changed immensely due to variations in VCO stages which are either 0 or 1. This will give the degradation in phase noise of the proposed VCO. To overcome this problem, inverter gate is used as variable capacitor. The output capacitance of i^{th} of VCO-I and input capacitance of next of ($i^{th}+1$) stage and load capacitance C_{load} contributes an overall capacitor at each stage. The output voltage at alternative VCO-I stages is 0 and 1.8 respectively. The V_{gc} is voltage across terminals of inverter caps Invc1-Invc4 which is changed at the alternative of stages of VCO-I. According to voltage 0 or 1.8 at output node of VCO-I, PMOS or NMOS of inverter cap turns on and capacitance value contributed by them is in range of 6-7 pico-farads. Due to this, there is less variation in the control voltage and improves phase noise of VCO-I. For given frequency of operation with lower power consumption and minimum periodic jitter, the value of width W and length L are taken as W = 2.3 μm and L =2.3 μm with t_{ox}=4 nm for MOSCAP, inverter and as well as for inverter cap at output. For '0' to '1' transition in VCO-I, at its switching threshold point NMOS contributes the maximum noise current and similarly for PMOS, for '1' to '0' transition [81-82]. In inverter cap, NMOS works in depletion region and PMOS in

minimum cap region. Fig. 4.6 (a) and Fig. 4.6 (b) show a variation of MOSCAP and inverter cap with the gate voltage respectively.



(a) (b)

Fig. 4.6 (a) Capacitance variation of MOSCAP with gate voltage, (b) Capacitance variation of inverter-cap with gate voltage

The power spectral density of noise due to thermal noise at switching point is given by following expression given below [82-83].

$$S_{vn,NMOS} = 8kTg_m\Upsilon = \frac{8kT\Upsilon \cdot I_{D,NMOS,sat}}{V_{DD}-V_{t,NMOS}} \quad (4.1)$$

where k is Boltzmann's constant, T is the temperature,Υ is the bias dependent factor, $I_{D,NMOS,sat}$ is saturation region current due of NMOS and $V_{DD} - V_{t,NMOS}$ is input and it is overdrive voltage at the input of a VCO-I node, T is the temperature. PMOS and NMOS in inverter Invc, being in different regions of an operation, the total capacitance given by them is in the order of 20-70 fF as shown in the Fig. 4.6 (b). At an output node ni with inverter cap Invci, the total capacitance is given by C_{loadi} with $i \in$(1-4):

$$C_{loadi} = C_{ni} + C_{Invci} \quad (4.2)$$

Here C_{ni} is combination of the diffusion capacitance at ni node and the gate capacitance of subsequent stage and C_{Invci} is the gate capacitance of Invci in the proposed VCO-I as shown in the Fig. 4.5 (b). The gate voltage (v_g) of Invci changes from 0 V and 1.8 V and the voltage at its output node (V_c) changes in range of 65 mV ± 2.5 mV. Due to load capacitor, the power noise spectral density is given by [81]:

$$S_{v,C} = \frac{kT}{C_{loadi}} \tag{4.3}$$

The equation (4.1) is changed and the total output noise voltage spectral density due to NMOS and C_{loadi} is given as:

$$S_{vn,NMOS} = \frac{8kT\Upsilon \cdot I_{D,NMOS,sat}}{V_{DD}-V_{t,NMOS}} + \frac{kT}{C_{loadi}} \tag{4.4}$$

The control voltage contributes a flicker noise in the VCO. Due to control voltage variation, the frequency of oscillation of VCO is changed and also it affects the phase noise of VCO according equation given [81]:

$$\frac{\partial f_o}{\partial V_{ctrl}} = kS_{vc}(f) = \frac{k^2}{4f^2} S_{vc}(f) \tag{4.5}$$

Where *k* is gain of VCO-I, f_o is the frequency of oscillation, $S_{vc}(f)$ is voltage spectral density and *Vctrl* is control voltage of VCO-I. The delay in each stage is given by pull up and down current of PMOS and NMOS devices respectively. The relationship between phase noise and jitter is given below [81]:

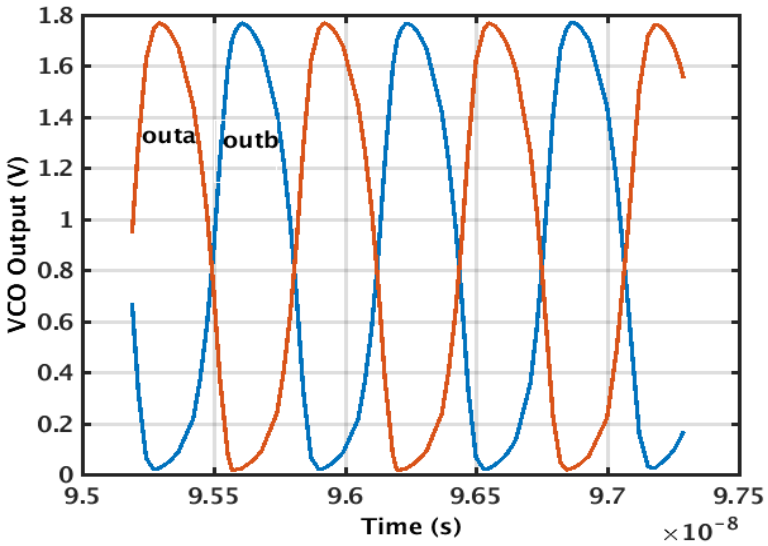
$$S_{psd}(f) = \sigma^2 \frac{f_c^3}{f_o^2} \tag{4.6}$$

where $S_{psd}(f)$ is power spectral density of phase noise, σ^2 is the jitter, f_c is the carrier frequency, and f_o is the offset frequency. At switching point, the current in both devices are considered to be equal. The glitches and perturbations in control voltage affect the propagation delay of each stage and fluctuates the frequency of oscillator. The cascade of inverters with variable load cap will contain the other noise sources in ring oscillator design. The noise at the output of first delay cell is amplified by the next stage cell's trans-conductance. For VCO, the amplification and coupling noise becomes dominant at higher frequencies which can be neglected.

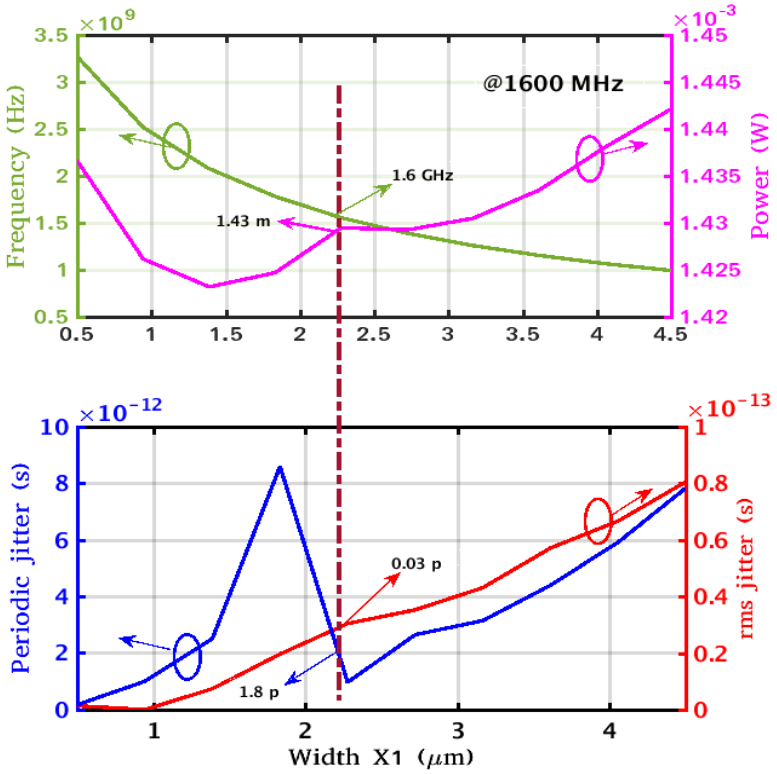
4.9 Simulation Results of VCO-I

The proposed VCO-I have tuning range from the 0 V to 0.6 V and it gives a highest frequency at 0.6 V. The transient response of proposed VCO-I is shown in the Fig. 4.7 (a). The graph in Fig. 4.7 (b) shows an analysis of proposed VCO-I at width X1of Inverter-cap =2.3 μm and control voltage of 100 mV. As X1 increase, power increases but frequency decreases. The variation of power and frequency, periodic jitter, and RMS jitter with width X1 of Inverter-cap in the proposed VCO-I is shown in the Fig. 4.7 (b). The achieved periodic jitter and RMS jitter are 1.8 ps and 0.03 ps respectively. The proposed VCO-I achieves the gain of 830 kHz/mV

approximately which is suitable to achieve the low phase noise DPLL architecture for SoC applications. The voltage variation in control voltage is up to ± 13% in the proposed low gain VCO-I which can be tolerated by it without affecting the phase noise of DPLL-I. Fig. 4.7 (c) shows the variation in output frequency of VCO-I with the width of MOS X1. The PVT variations in output frequency across the different corners are shown in Fig. 4.7 (d). The maximum variation of 3.25% is observed at FF corner whereas for SS corner, it is 2.5%. The variation of 1.25% is observed for SF and FS corner with respect to TT corner.



(a)



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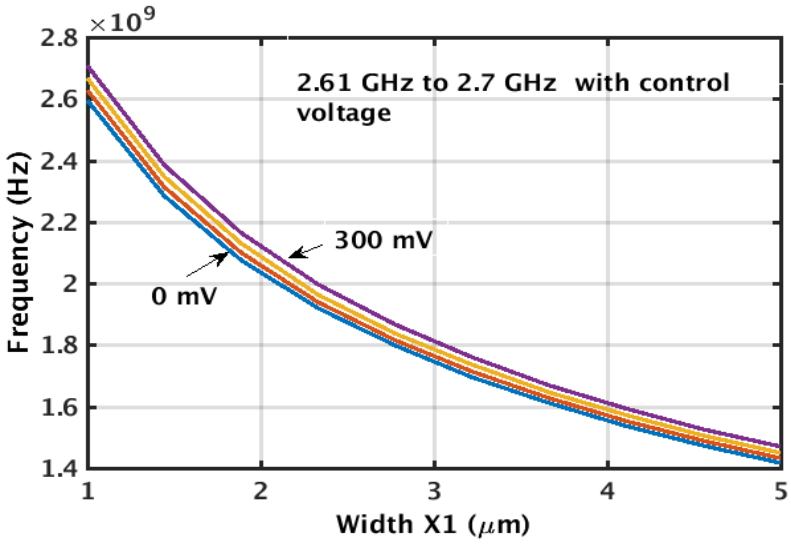
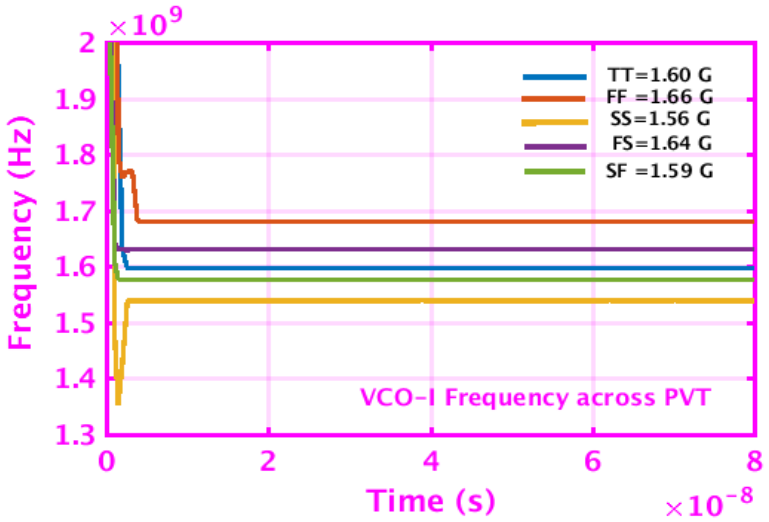
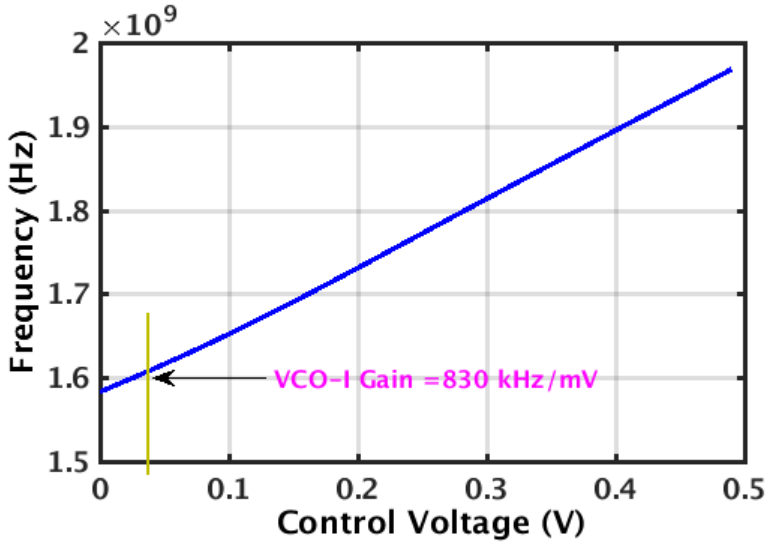

×10^9
2.8
2.6
2.4
2.2
2
1.8
1.6
1.4
Frequency (Hz)
2.61 GHz to 2.7 GHz with control voltage
300 mV
0 mV
1
2
3
4
5
Width X1 (μm)

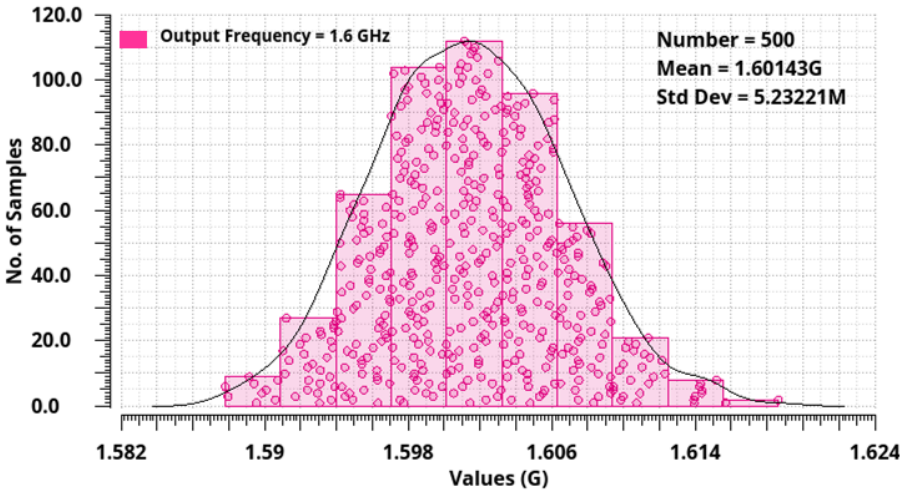
(c)


×10^9
2
1.9
1.8
1.7
1.6
1.5
1.4
1.3
Frequency (Hz)
TT=1.60 G
FF =1.66 G
SS=1.56 G
FS=1.64 G
SF =1.59 G
VCO-I Frequency across PVT
0
2
4
6
8
Time (s)
×10^-8

(d)


×10^9
2
1.9
1.8
1.7
1.6
1.5
Frequency (Hz)
VCO-I Gain =830 kHz/mV
0
0.1
0.2
0.3
0.4
0.5
Control Voltage (V)

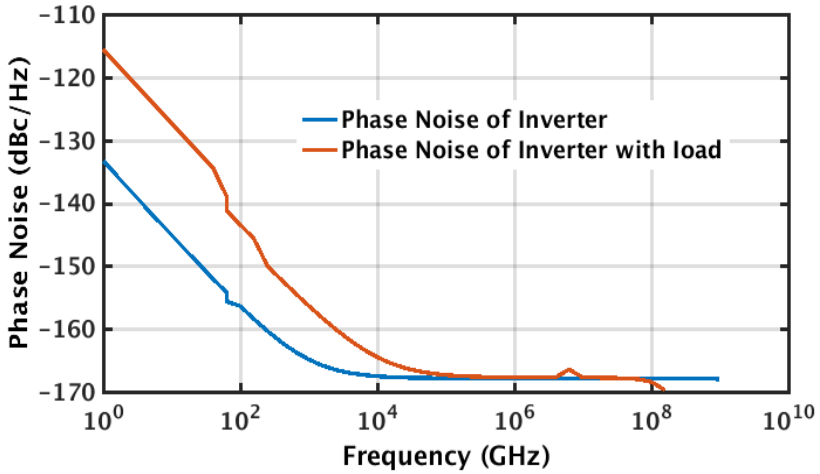
(e)



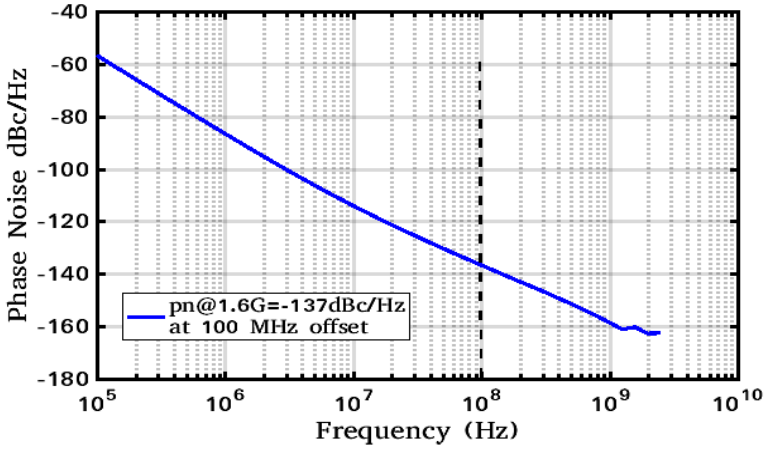
(f)

Fig. 4.7 (a) Transient response of VCO-I, (b) Periodic jitter, power, and frequency variation with width X1, (c) Variation in output frequency of VCO-I with the width of MOS X1 and control voltage Vctrl (d) Frequency variation with PVT, (e) Gain of VCO-I, (f) Monte Carlo Simulation of VCO-I

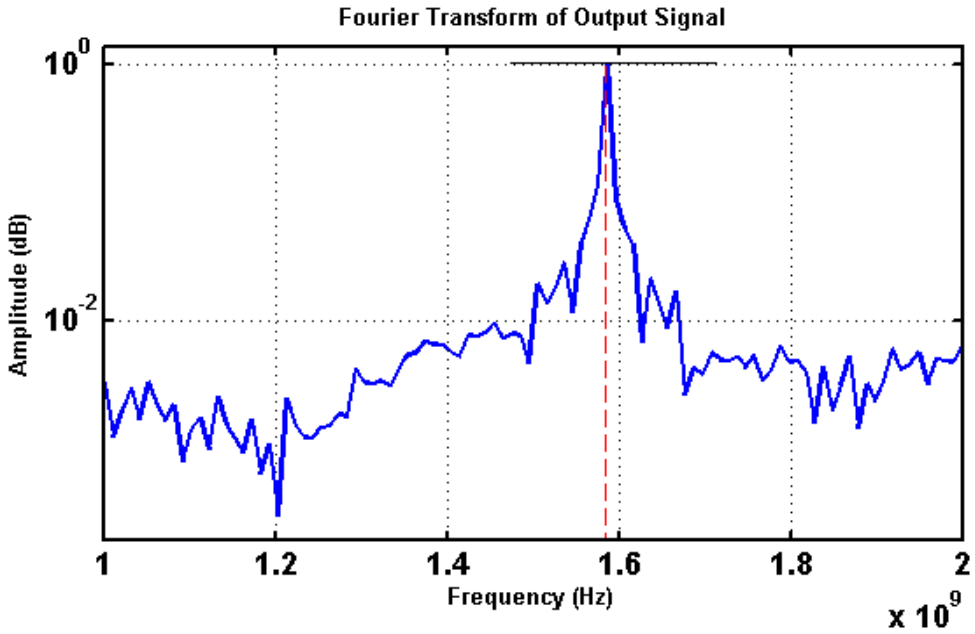
For stable operation and low jitter VCO-I in DPLL designs, the low gain of VCO-I is achieved with value of 830 kHz/mV as depicted in the Fig. 4.7 (e).



(a)



(b)



(c)

Fig. 4.8 (a) Phase noise of inverter circuit with no load and with inverter-cap (Invc) as a load, (b) Phase noise of proposed VCO-I for DPLL design, (c) Frequency spectrum of output of VCO-I

Table 4.2: Proposed VCO-I parameters

Parameters	Proposed VCO-I
Periodic Jitter (ps)	1.6
Power (mW)	1.43
Phase Noise (dBc/Hz)	-137
Gain (kHz/mV)	830
Area (μm^2)	225
W=L=X1(µm)	2.3

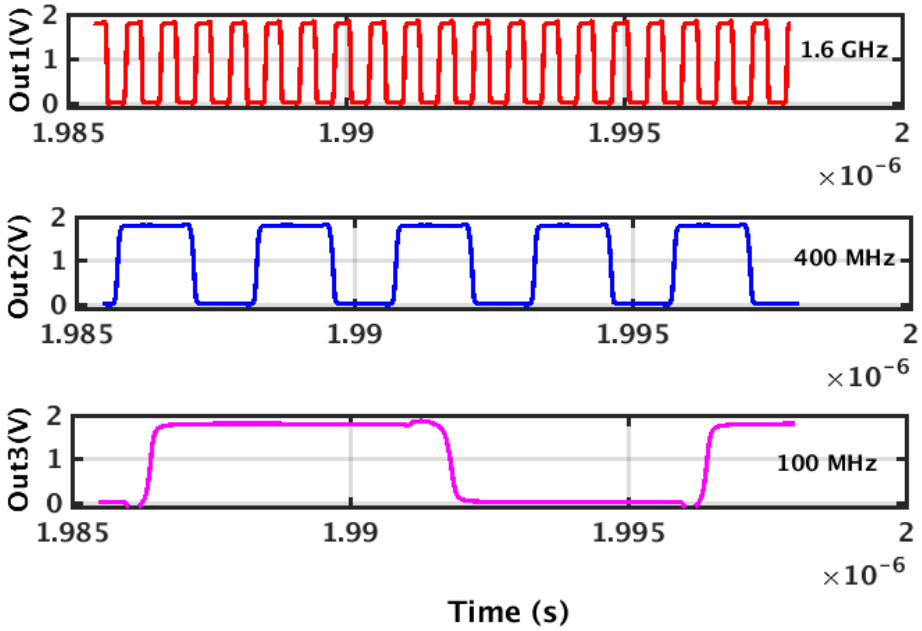
Fig. 4.7 (f) shows the Monte Carlo simulations for proposed VCO-I. It is observed that 0.325 % variation in the output frequency with process and mismatches. From the Fig.4.8 (a), it is noted that the phase noise of inverter with inverter cap Invc as load is same for target frequency range. Further extending the analysis, the graph in Fig. 4.8 (b) shows the phase noise of proposed VCO-I which comes out to be -137dBc/Hz at offset of 100 MHz and suitable for the proposed DPLL architectures. Fig. 4.8 (c) shows a frequency spectrum of output frequency of VCO-I. It is shown maximum power of carrier is observed at the frequency of 1.59 GHz which is output frequency of VCO-I. Table 4.2 shows the performance parameters of proposed VCO-I and they are optimized for DPLL architectures.

4.10 Divider

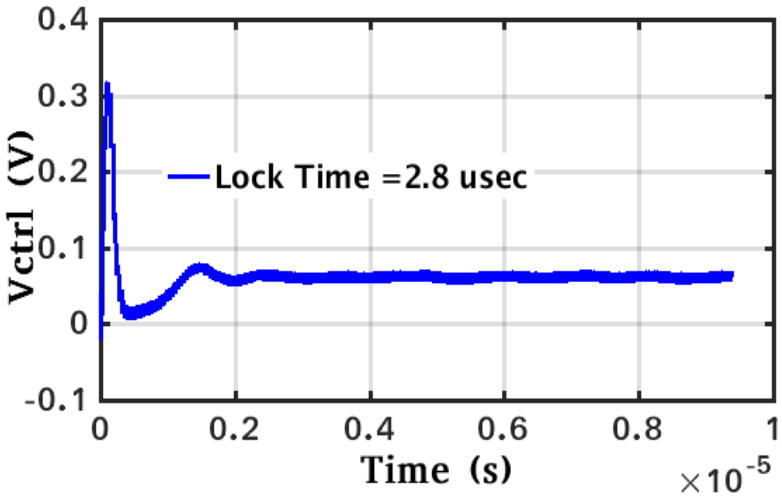
To generate the output frequency of 1.6 GHz from the reference frequency of 25 MHz, the division ratio for DPLL architectures is 64. The true single-phase D-flip-flop is used to design the divider. The divide–by-2 and divide-by-4 circuits are used to obtain the division ratio of 64. All digital design methodology is used to obtain the divider which makes it reusable for lower CMOS technologies [84].

4.11 Simulation Results of DPLL-I

Fig. 4.1 shows the complete DPLL-I design with proposed PFD-I and VCO-I. The proposed DPLL-I is simple, compact, and relatively easy to design. The DPLL-I is designed in SCL 180nm digital CMOS technology with 1.8V supply voltage. This design achieves a periodic jitter of 0.642 ps at the output frequency of 1.6 GHz. The different frequencies generated by the DPLL-I are in the range of 25 MHz to 1.6 GHz as shown in the Fig. 4.9 (a). The control voltage of proposed VCO-I settles at Vctrl $\cong$ 70 mV which produces an output frequency of 1.6 GHz. The achieved locking time of the proposed DPLL-I is 2.8 µs as shown in the Fig. 4.9 (b). The voltage variation is in range of ± 2.5 mV and is observed in control voltage. However, it does not affect the performance of DPLL-I as VCO-I can tolerate it and suppress the phase noise. The total power consumed by proposed DPLL-I is 2.3 mW. At the output frequency of 1.6 GHz and 400 MHz, the achieved RMS jitter is 0.204 ps and 0.207 ps respectively. The effect of increase in the width of MOSCAP M17 of loop filter with control voltage and variation locking time is shown in the Fig. 4.9 (c). As the width of MOS M17 (X2 in µm here) is increased, gate capacitance increases which reduces the control voltage variation.



(a)



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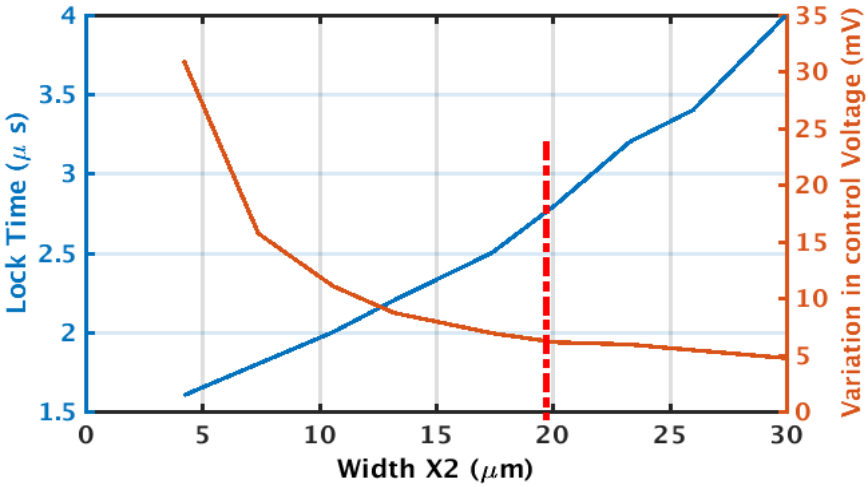
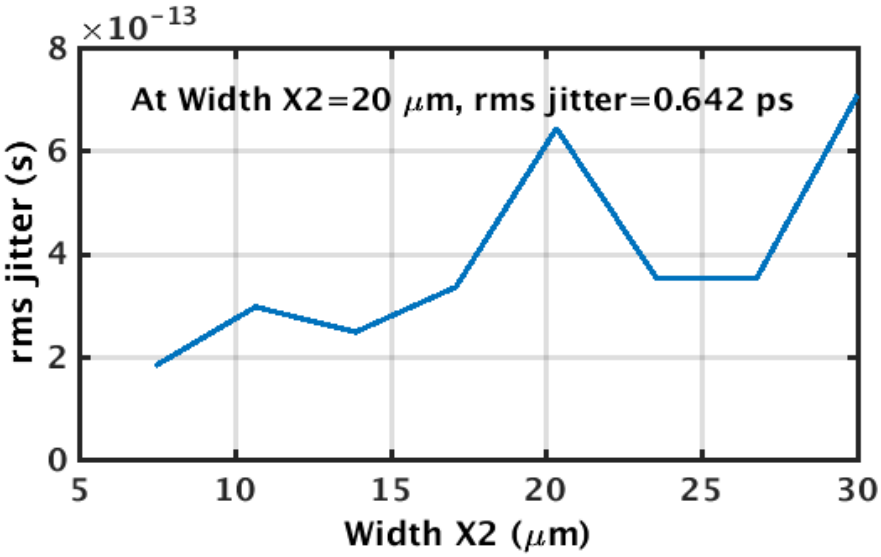


(c)



(d)

Fig. 4.9 (a) Transient response of DPLL-I, (b) Locking time of DPLL-I, (c) Lock time and control voltage variation with width X2, (d) RMS jitter variation with MOSCAP M17

Table 4.3: Achieved DPLL-I parameters

Parameters	Proposed DPLL-I
Supply Voltage (V)	1.8
PLL Frequency (GHz)	1.6
Jitter $_{(RMS)}$ (ps)	0.642@1.6 GHz
Locking Time (µs)	2.8
Power Consumption (mW)	2.3

For the locking time of 2.8 µs in DPLL-I, the variation in control voltage becomes constant in range of ± 2.5 mV (*i.e.* 5 mV in total) at X2 = 20 µm. The RMS jitter of 0.64 ps under locked condition is achieved as shown in the Fig. 4.9 (d). Table 4.3 shows the performance parameters of proposed DPLL-I. The proposed DPLL-I has loop filter, CP, incorporates the proposed VCO-I, and dynamic logic-based phase frequency detector (PFD-I A compact low jitter and low power DPLL-I with inverter based low gain and low jitter VCO-I, fast PFD-I, and transmission gate-based loop filter is proposed in this work. Overall power and area of DPLL-I is reduced due to switched capacitor based compact charge pump and proposed PFD-I reduces the locking time of DPLL-I architecture. The DPLL-I synthesizes 1.6 GHz at the output with root mean square RMS jitter of 0.642 ps. It shows that it is suitable for high speed and battery-operated devices. The simulation results of proposed DPLL-I are discussed and analyzed in this section.

4.12 Design of DPLL-II

Application-specific integrated circuits (ASICs) are also designed using standard cell methodology. Standard cell methodology is an instance of design abstraction in which digital circuits are represented by logic gates (such as a NAND gate) [22]. Standard Cell is a collection of interconnect structures and transistor that gives a Boolean Logic function (*e.g.* inverters, OR, AND, XOR, and XNOR) and a storage function (*e.g.* latch or flip-flop). The significance of standard cell library design methodology is growing with very-large-scale integration (VLSI) technology development due to its low cost, low design effort and less time to market. Fig. 4.10 shows the novel standard cell based DPLL-II. Owing to benefits of standard cell methodology, a designing of mixed signal architectures such as PLLs and ADCs using standard cell methodology has recently gained popularity [22].

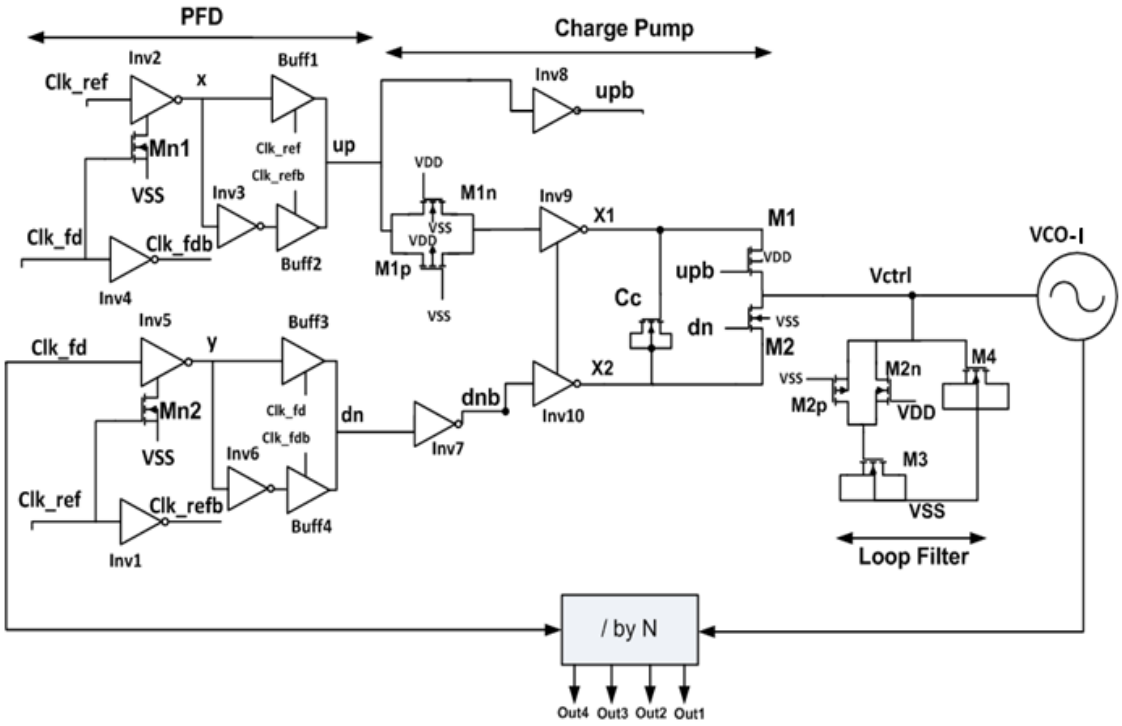


Fig. 4.10 Proposed DPLL architecture-II

In this section, another version of digital PLL (DPLL-II) has been designed using a highly standard cell-based methodology for SoC and battery-operated applications. Fig. 4.10 shows the proposed DPLL-II architecture. In this DPLL-II version, novel gated based frequency phase detector (PDF-II), inverter based VCO-I, and digital charge pump (CP) are proposed to enhance the locking and power consumption parameters. This novel DPLL-II architecture achieves a low power, fast locking, and low area.

4.13 Phase Frequency Detector (PFD-II)

Fig. 4.11 shows the proposed PFD-II design. The traditional PFD-II architecture is comprised of D-flip-flops with reset pin and logic gates such AND, OR, NOR, and NAND [9]. The major issues of earlier reported architectures are an additional delay added by the logic gates which generate the reset signal to reset the D-flip-flops. The duration of the reset path (which slows the PFD design) depend upon the widths of up and down (dn) pulses and the delay offered by the logic gates. If the process of resetting of D-flip-flops occurs during the rising edge of clock Clk_ref, at this instance, any specific edge is missed for detection of phase error difference between the reference and feedback signals. This gives rise to the issue of blind zone and it also induces the glitches in the source and sink current of charge pump [9-11]. During the blind zone occurrence, a particular edge of Clk_ref or Clk_fd is missed for the detection and thus affects the locking time of DPLL-II. This issue also induces a ripple in control voltage which degrades the phase noise of DPLL.

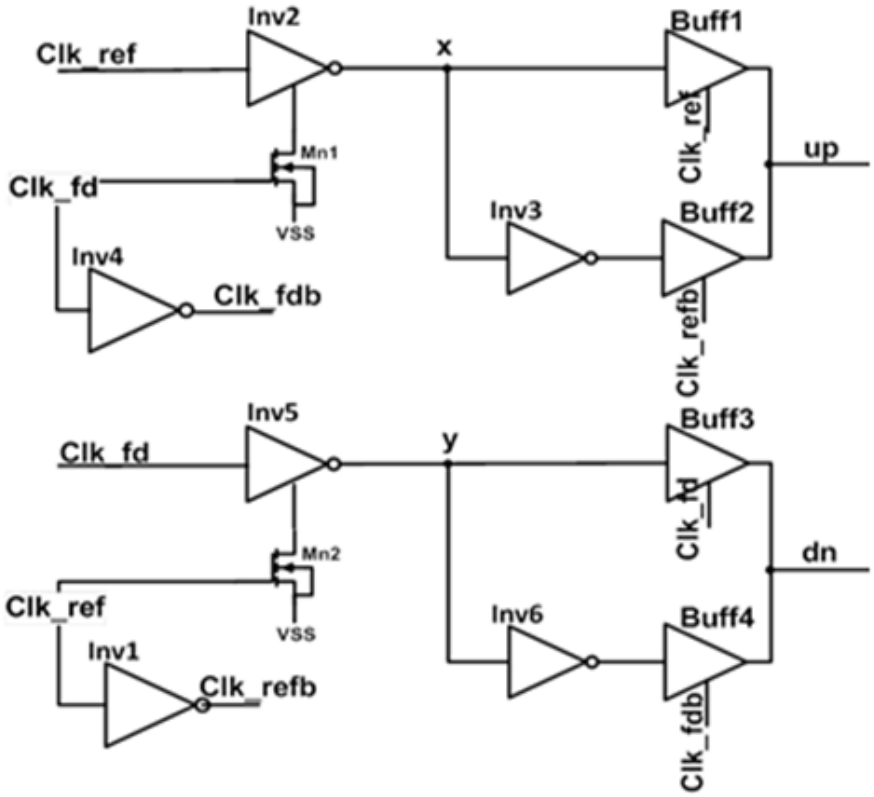
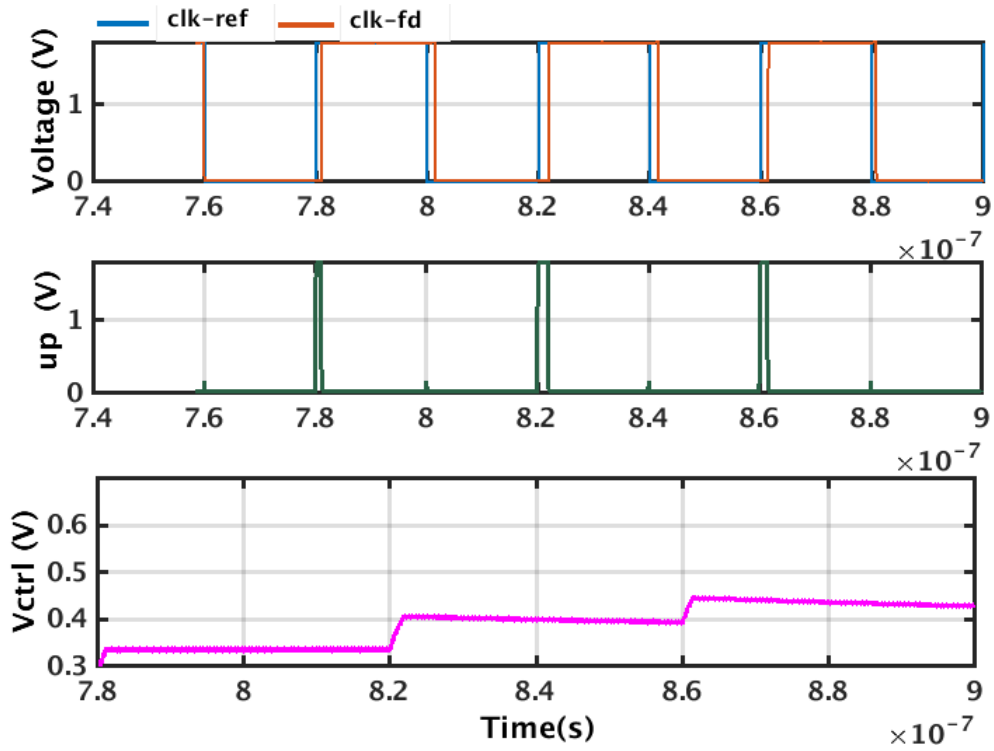


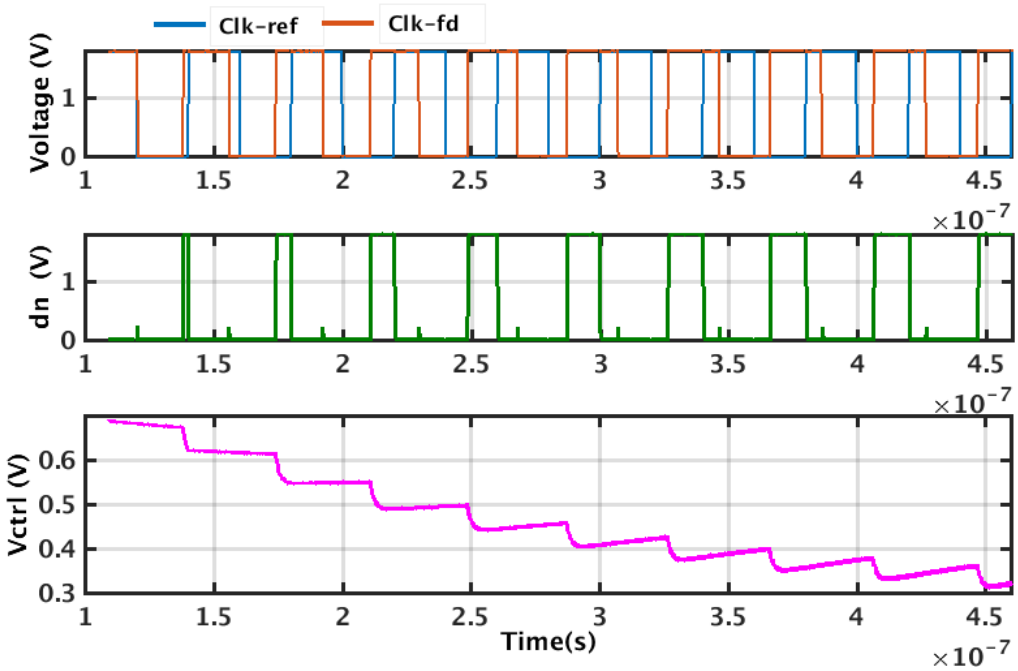
Fig. 4.11 Proposed PFD-II

Conventionally, supplementary inverter chain is used to add extra delay at rising edge of Clk_ref and Clk_fd which tackles the blind zone problem. The PFD architectures reported in literature [76-77, 85] have high speed which improves locking time but still the problem of blind zone needs to be addressed. The proposed PFD-II design avoids a blind zone because reset signal is generated by Clk_ref and Clk_fd and thus the reset path is removed from the circuit. Therefore, the locking time of DPLL-II is reduced. The proposed PFD-II consists of buffers (Buff1-Buff4), NMOS switches (Mn1, Mn2), and inverters (Inv1-Inv6). VSS node of inverter Inv2 and Inv5 are attached to the drain nodes of MOSFETs Mn1 and Mn2 respectively. The functioning of proposed PFD-II is divided into three operations. Initially, when Clk_ref is at falling edge *i.e.* '0' node x is charged to logic '1' and if Clk_ref is at rising edge and it leads the feedback signal Clk_fd, the Buff1 and Inv2 charges the up signal to logic '1' otherwise Buff2 and Inv2 discharges the up signal to logic '0'. When feedback signal Clk_fd is at rising edge and it leads reference clock and Buff3 and Inv5 charges the dn signal to '1'. When Clk_ref and Clk_fd are at falling edge, the Buff2 and Buff4 discharges the up and dn pulses to logic '0' respectively. When Clk_ref and Clk_fd are at rising edges, the intermediate nodes x and y discharges to VSS via MOSes (Mn1 and Mn2) which resets the pulses up and dn. The proposed PFD-II shows an improved lock time at the output frequency of 1.6 GHz. Fig. 4.12 (a) and (b) depicts the pre-layout simulations for up and down pulses with variation of control voltage.

The width of up pulse starts increasing which increases the control voltage when the Clk_ref behind the Clk_fd as shown in the Fig. 4.12 (a). As the control voltage increases, the frequency of the proposed VCO-I also increases.



(a)



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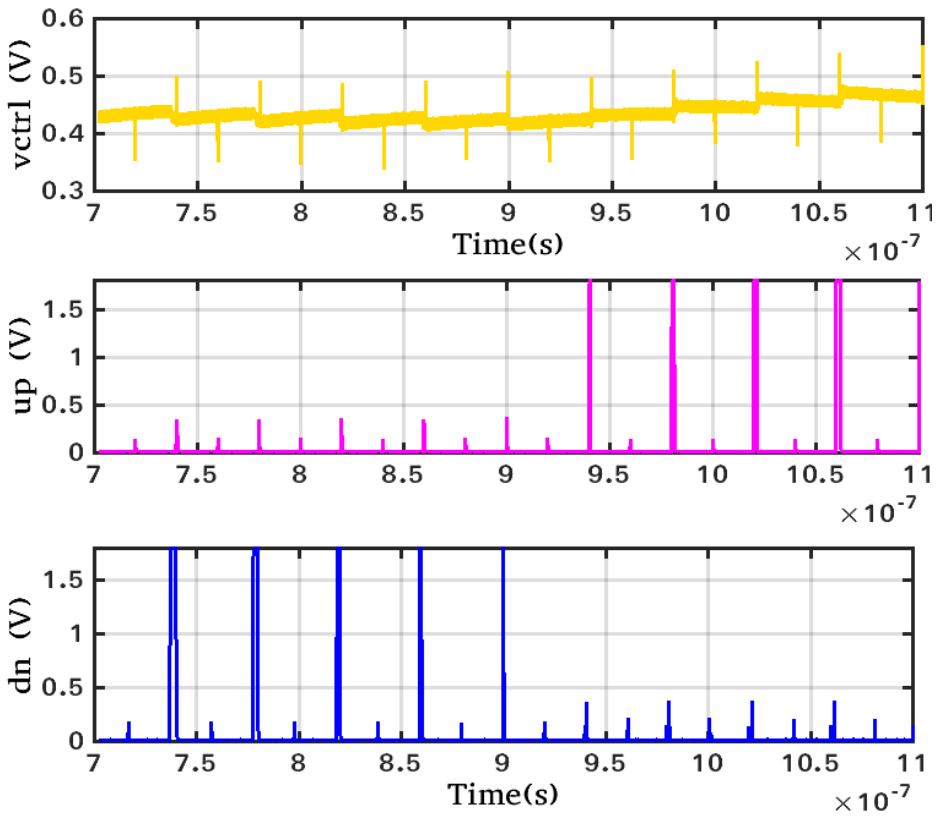


(c)

Fig. 4.12 (a) Pre-layout simulation results of control voltage variation with up pulse, (b) Pre-layout result of control voltage variation dn pulse width, (c) Post layout simulation of control voltage variation up and dn pulse width

Similarly, Fig. 4.12 (b) shows that when the Clk_fd comes after the Clk_ref, the width of dn pulse increases and the control voltage decreases which decreases frequency of the proposed VCO-I. When the phase difference between the Clk_ref and Clk_fd reduces and the widths of up and dn pulse also reduces to minimum size, the control voltage becomes constant and DPLL-II is said to be in locked state. The post layout simulations for up and dn pulses of proposed PFD-II are shown in the Fig. 4.12 (c).

4.14 Proposed Charge Pump

The charge pump (CP) is important block of DPLL architecture which is analog in nature [9-11]. The enormous amount of power in range of few milli-watts is consumed by the charge pump [40, 79, 86]. Therefore, it drastically affects the overall power budget of the DPLL architectures. The CP being analog in nature is more prone problem like leakage currents and power noise. Hence, digital design methodology is followed in this design which makes it low power and compact in size.

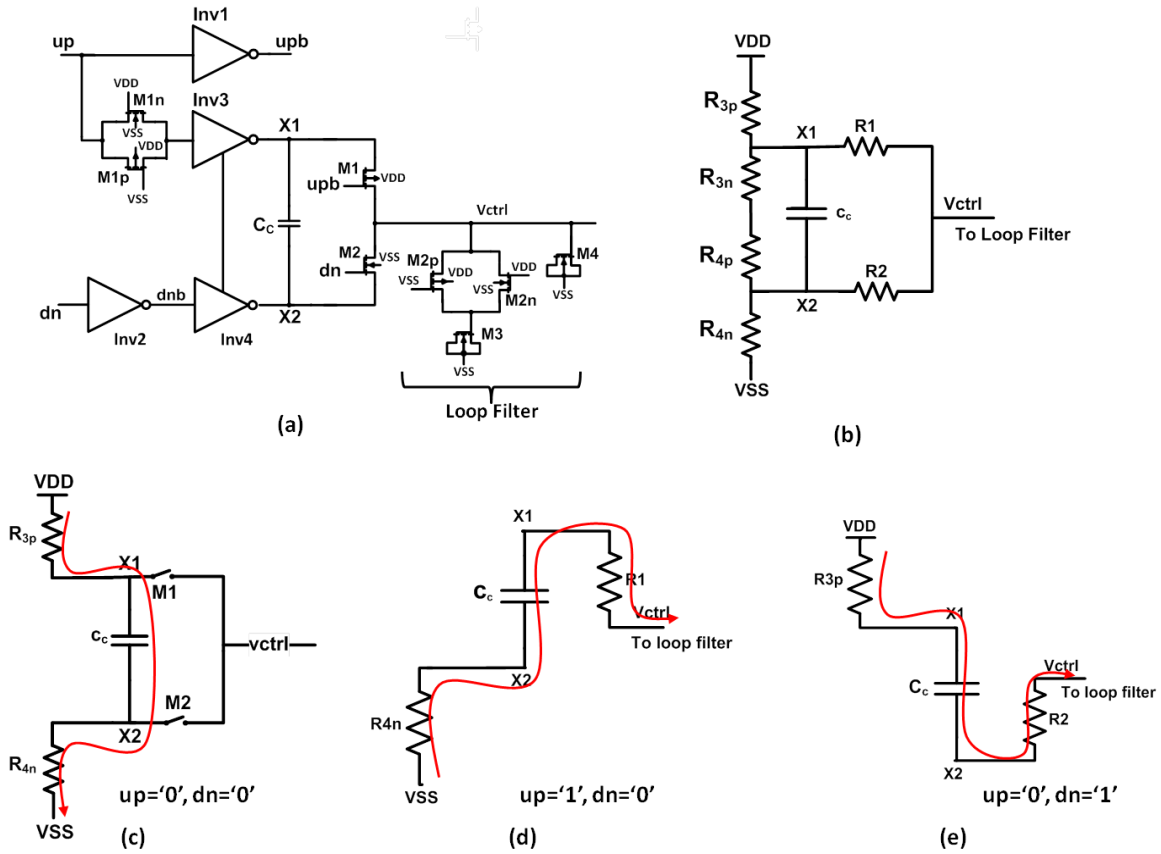


Fig. 4.13 (a) Proposed charge pump design with M1 and M2 W/L as 1.2/0.18 and0.8/0.18 µm, (b) Equivalent circuit model of charge pump design, (c) Idle mode, (d) Up mode, (e) Down mode

Many charge pumps which are designed using digital approach are reported in literature but these architectures still have problems of higher power consumption and more area requirements [40, 79, 86]. In phase locked loop, the proposed charge pump designed with digital methodology which tackles the above said issues. Only MOS transistors and CMOS inverters are used to design charge pump. MOSCAP (PMOS) is used to implement the capacitor Cc. The performance of proposed CP is not affected by the voltage variation across Cc. Since the isolation at output nodes of Inv3 and Inv4 with inputs are provided by use of capacitor Cc.

4.15 Operation of Charge Pump and Simulation Results

The PFD creates the up and down pulses and these pulses drives the CP. The charging and discharging currents are generated by it. For the low jitter DPLL designs [9-10], the matching of charging and discharging current is necessary. This proposed CP design consists of switches, inverters, and buffers as shown in the Fig. 4.13 (a). The proposed CP works in the three modes which are up mode, down mode, and idle mode. At first, when signals Clk_ref and Clk_fd are at falling edge and '0', the capacitor C_c is charged to VDD by up pulse. After that, when the Clk_ref is ahead of Clk_fd, the charge stored by C_c is shared with loop filter capacitors

implemented by M3 and M4 respectively. As charge increase across the MOS capacitor $CM_{3,4}$, the control voltage increases which in turn increases the frequency of VCO-I. This will bring the frequency of Clk_fd closer to reference Clk_ref. Similarly, when Clk_fd is ahead of the Clk_ref, the charge stored on loop filter capacitor $CM_{3,4}$ discharges through capacitor C_c and thus decreases the frequency of the proposed VCO-I. The proposed CP consumes the power of 0.35 mW. The power consumption is very low as compared to other designs realized using digital gate-based approach. For the CP in different modes, the power consumption analysis has been done in consequent section.

4.15.1 Idle Mode

When up and dn pulses are logic at '0', the charge pump is said to be in idle mode. The Inv3 and Inv4 charges the capacitor C_c to voltage V_c. The output voltage V_{ctrl} is obtained at output node of charge pump and is given to low pass filter. For charge pump, the equivalent circuit model and idle mode is shown in the Fig. 4.13 (b) and Fig. 4.13 (c) respectively.

$$p_{idle} = \frac{\alpha f_{clk\_ref} q_c V_{DD}}{2} \tag{4.7}$$

where α is switching activity factor, q_c is charge on capacitor, f_{Clk_ref} is the frequency of reference clock at the input node.

4.15.2 Up Mode

When up pulse is at logic '1' and dn pulse is at logic '0', the charge pump is said to be operate in up mode. For up mode, the equivalent circuit model is shown as in the Fig. 4.13 (d). The final voltage across the capacitor C_c in idle mode is V_c which acts as initial voltage while operating in the up-mode. In up mode the charge pump works as: voltage V_{X1} at node X1 starts falling and it will the charge MOS capacitor $CM_{3,4}$ to $V_X = V_{supply} - V_c$ in the low pass filter. The MOS capacitor is implemented by MOSes M3 and M4. The voltage V_{ctrl} is the final voltage at output of charge pump for the duration of the transient mode, and is given by following:

$$V_{ctrl} = V_c + \frac{C_c}{C_c + CM_{3,4}} V_X \left(1 - e^{-t/\tau_{up}}\right) \tag{4.8}$$

where C_c is capacitance connected across the nodes X1 and X2 of charge pump. The power p_{charge} consumed in the up mode is given as:

$$p_{charge} = \frac{f_{Clk\_ref}\ \alpha\ q_c\ V_{ctrl}}{2} \tag{4.9}$$

where $\tau_{up} = ((R_{4,n} + R1)C_c)$. The power change occur as charge pump changes its operation from idle to up mode and change in power is by adding equations (4.7) and (4.9).

$$p_{charge} = \frac{\alpha f_{Clk\_ref}\ q_c(V_{DD}+V_{ctrl})}{2} \tag{4.10}$$

$$= \frac{\alpha f_{Clk\_ref}}{2}(C_c V_{DD} + CM_{3,4}\ V_X - \frac{CM_{3,4}}{CM_{3,4}+C_c} V_X e^{t/\tau_{up}}) \tag{4.11}$$

4.15.3 Down Mode

The operation of the down mode is shown in the Fig. 4.13 (e). When dn and up are at the logic '1' and '0' respectively, the charge pump starts to operate in the dn mode initially from the idle mode. The MOS capacitor $CM_{3,4}$ discharges by R2 while operating in the down mode thus reduces the control voltage V_{ctrl} at output node of proposed charge pump. The power discharging while operating in the dn mode is given as $p_{discharge}$

$$V_{ctrl} = V_c - \frac{C_c}{C_c+CM_{3,4}} V_X \left(e^{t/\tau_{dn}}\right) \tag{4.12}$$

where, $\tau_{dn} = ((R_{3,p} + R2)C_c)$

$$p_{discharge} = \frac{\alpha\ q_c\ V_{ctrl}}{2} \tag{4.13}$$

$$p_{discharge} = \frac{\alpha\ f_{Clk\_ref} q_c\ V_{ctrl}}{2} \tag{4.14}$$

The total power consumed by the proposed charge pump during working in the all 3 modes is given as:

$$p_{cp\_tot} = p_{idle} + p_{charge} + p_{discharge} + p_{leakage} \tag{4.15}$$

$$= \frac{\alpha\ f_{Clk\_ref} q_c\ V_{DD}}{2} + p_{leakage} \cong \frac{\alpha\ f_{Clk\_ref} C_c V_{DD}^2}{2} \tag{4.16}$$

As the width of dn signal is increased, the control voltage is reduced and similarly when the width of up signal is increased, control voltage also increases. Finally, the control voltage settles at particular value when the widths of up and dn pulses become constant. The sourcing and sinking current of proposed charge pump is settled at ±192 µA. The simulated waveform of variation of sourcing and sinking currents which is the function of the control voltage is shown in the Fig. 4.14. The control voltage is in range of $0 < V_{\text{ctrl}} < 1.8$. The mismatch between sourcing and sinking current is less than 0.1% with control voltage range from 0.45 V

to 1.35 V. Owing to digital approach, the charge pump shows a better performance as compared to other architectures given in literature [79, 86].

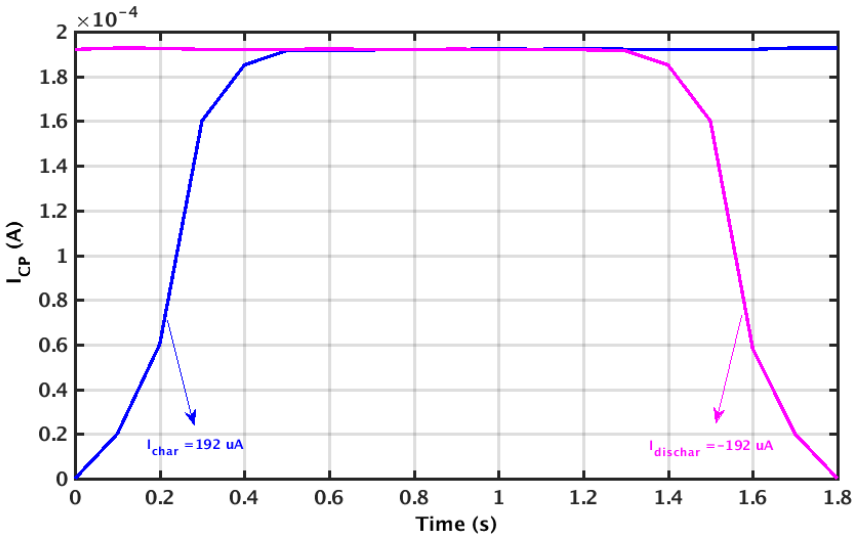


Fig. 4.14 Source and sink current variation in proposed CP

The ultimate target is to use proposed CP in the DPLLs. By using this CP, small area, and low jitter DPLL architectures can be designed.

4.16 Loop Filter-II

The stability of DPLL is maintained by the second order low pass loop filter. In this present work, MOS devices are used to realize loop filter as shown in the Fig. 4.15. As per given specification for reduced periodic jitter and cycle-to cycle jitter of PLL, the optimized value of capacitors and resistor are taken into account. The loop filter is used to have the average of the control voltage provided by the proposed charge pump. It reduces the ripple and noise in control voltage which ultimately decreases the jitter in output frequency of VCO-I.

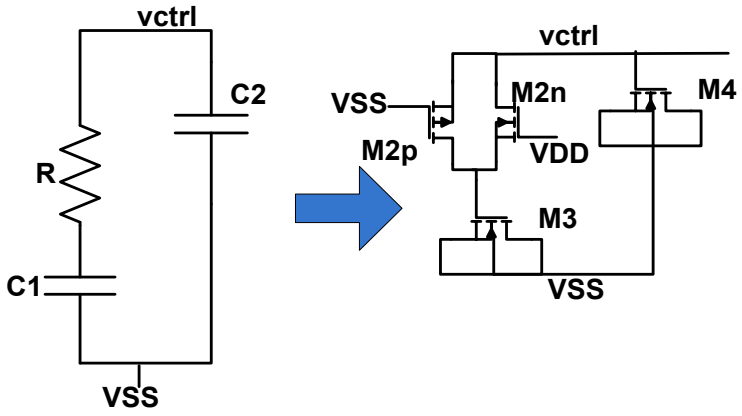


Fig. 4.15 Loop Filter-II with M3 and M4 W/L as 92/0.18 and 55/0.18 µm

The CMOS transmission gate is used to realize the resistor in low pass filter. For DPLL-II architecture, the control voltage V_{ctrl} = 0.386 V for proposed VCO-I at free running frequency of 1.6 GHz. Both transistors M2p and M2n of loop filter-II are in the saturation region for $V_{ctrl} < |v_{tp}|$. The required resistance value for stable operation of DPLL-II is obtained by transistors M2p and M2n in low pass filter. The proposed fast PFD-II reduces the locking time of DPLL-II as compared to other architectures reported in literature [76-77]. When up and dn pulses are at logic '1', Inv3 and Inv4 are turned off and the charge pump holds the prior state.

4.17 **Simulation Results of DPLL-II**

The proposed DPLL-II architecture is shown in the Fig. 4.10. This architecture uses a proposed charge pump, PFD-II, and VCO-I for frequency generation of 1.6 GHz. The VCO-I proposed in section 4.7 is used. This architecture shows low power and wide range output frequency. It is also suitable for high-speed applications.

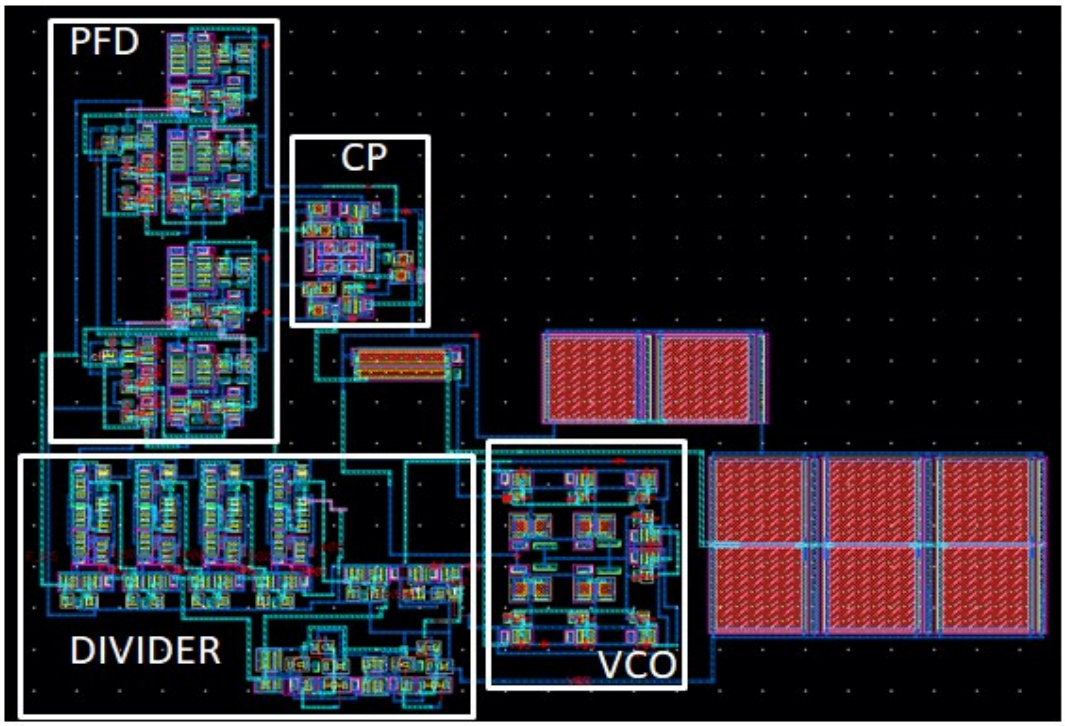
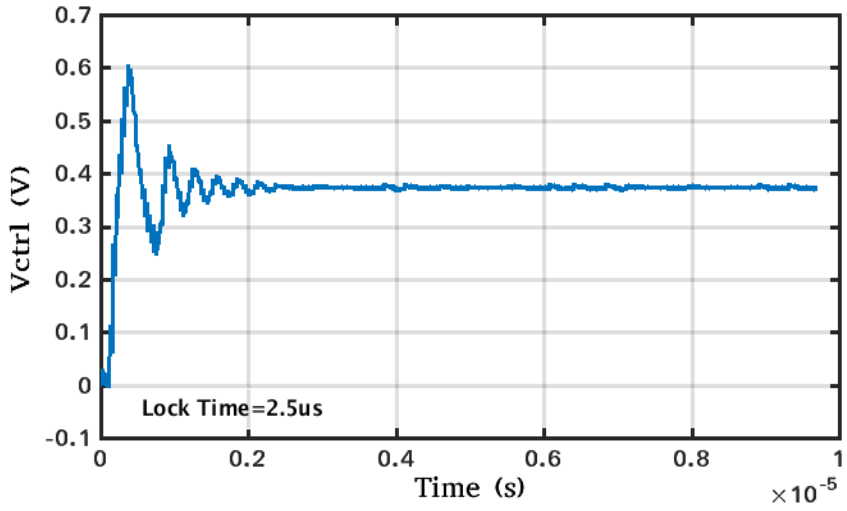


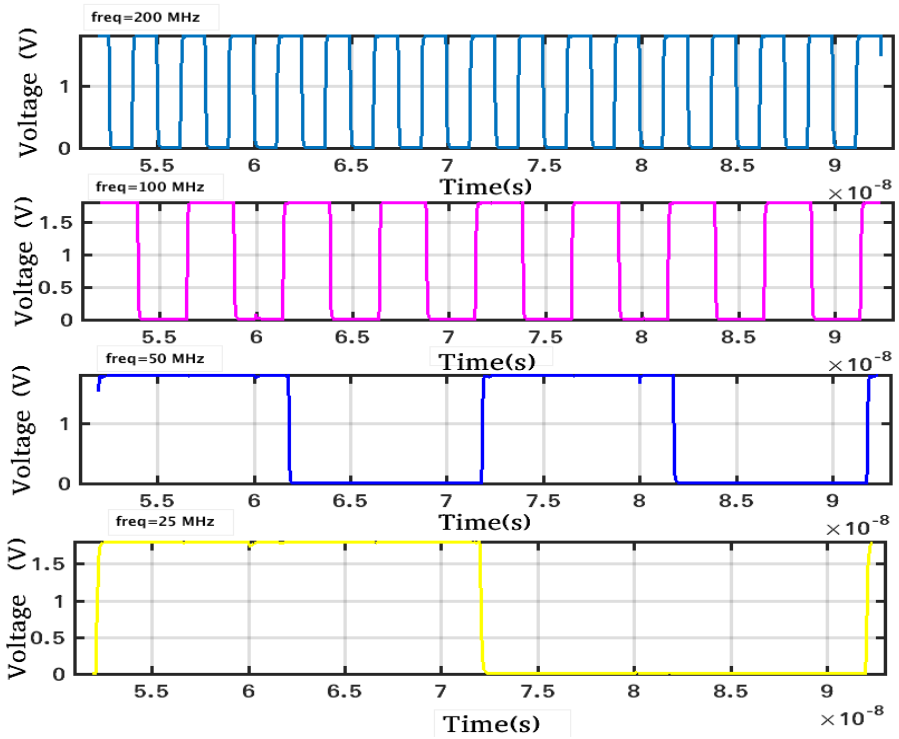
Fig. 4.16 Layout of DPLL-II

The layout of proposed PLL which contains the different blocks is shown in the Fig. 4.16. The proposed DPLL-II is designed in SCL 0.18 µm CMOS technology with 1.8V supply voltage. The locking time of proposed DPLL-II is 2.5 µs as shown in the Fig. 4.17 (a). The control voltage settles at 386 mV for output frequency of 1.6 GHz and variation in control voltage is less than ±4 mV. The proposed VCO-I can tolerate this variation and does not degrade the periodic jitter in the proposed DPLL-II. As gain of proposed VCO-I is 830 kHz/mV which is

very low and this variation does not affect the phase noise performance of VCO-I. The post layout simulations for transient response for output frequency of 200 MHz, 100 MHz, 50 MHz, and 25 MHz are shown in the Fig. 4.17 (b). The MOSCAP M3 and M4 with widths W3 and W4 respectively are used to realize the loop capacitors in loop filter is shown in the Fig. 4.15. The variation of periodic jitter with width W3 of MOSCAP M3 is depicted in the Fig. 4.18 (a).



(a)

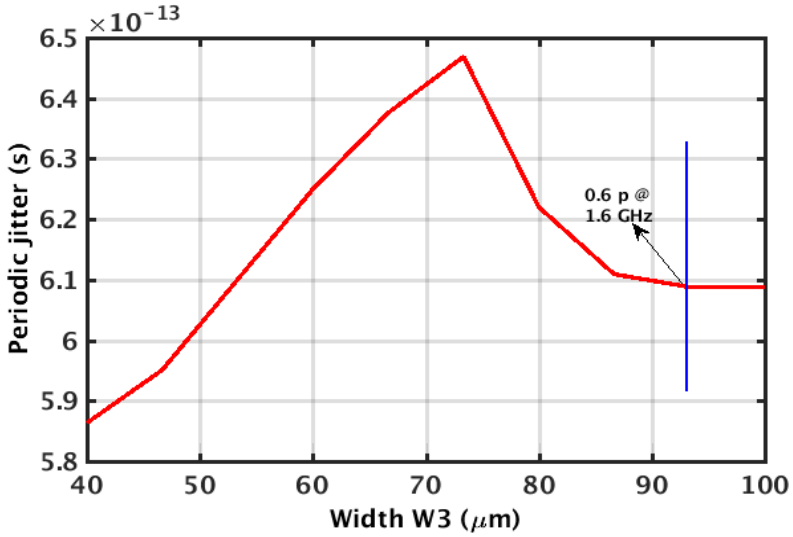


(b)

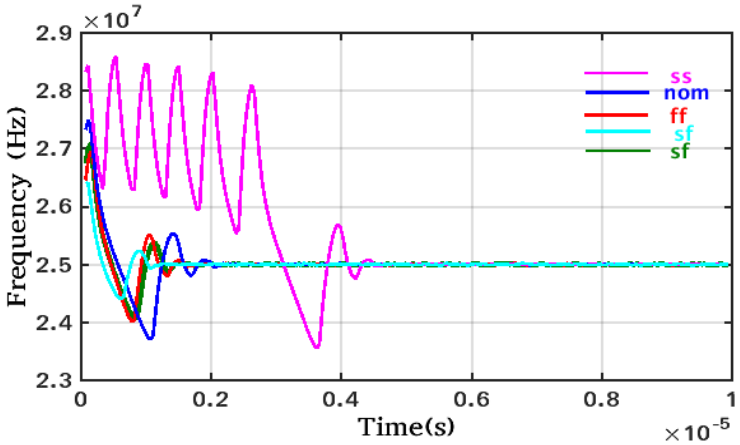
Fig. 4.17 (a) Lock time of proposed DPLL-II, (b) Transient waveform of proposed DPLL-II

The periodic jitter initially increases and then starts decreasing at 70 µm as the width W3 of MOSCAP is increased and finally becomes stable at 92 µm. This is due to variation in the width

of W3 varies and the bandwidth of DPLL-II and thus varies the periodic jitter. To have fast lock time and improved period jitter with variation lower than 1% in output frequency, best values for widths W3 are chosen as 92 µm.



(a)



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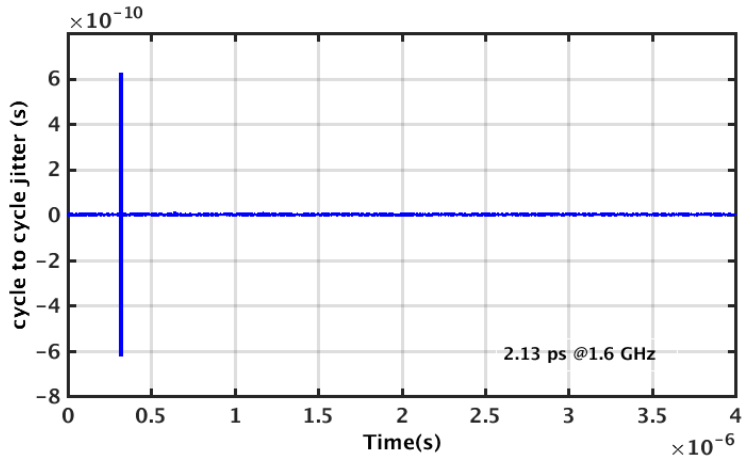

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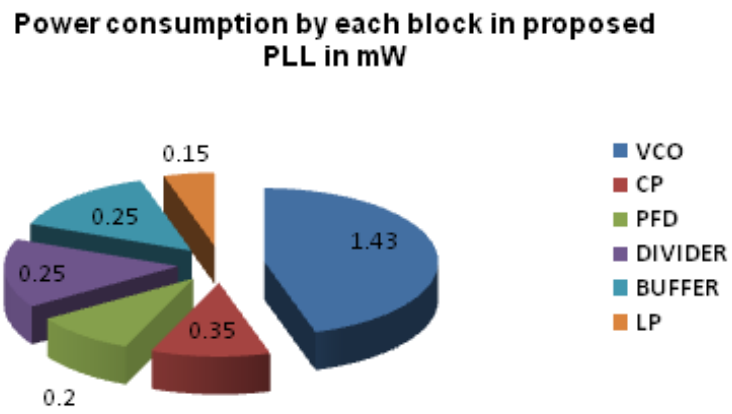


(d)

Fig. 4.18 (a) Periodic jitter variation with width W3, (b) PVT variations in output frequency, (c) $Jitter_{c\text{-}to\text{-}c}$ of DPLL-II, (d) Power consumption graph of DPLL-II

To show the proposed DPLL-II is robust against PVT variation, analysis is done at different PVT corners as shown in the Fig. 4.18 (b). The SS corner shows variation of 3.5% with respect to the TT corner. The input reference frequency is 25 MHz. The achieved value of root mean square (RMS) jitter is 5.1 ps at 1.6 GHz and 5.04 ps at 0.4 GHz respectively. The achieved cycle-to-cycle jitter is 2.13 ps at 1.6 GHz after the post layout simulation as shown in the Fig. 4.18 (c). The power consumed by the different blocks of DPLL-II is shown in the graph given in the Fig. 4.18 (d).

For DPLL-II, VCO-I works in linear range of gain up to 0.6 V with power consumption of 1.43 mW. The DPLL-II works at an output frequency of 1.6 GHz and maximum power consumption is 2.63 mW at supply voltage of 1.8 V. The variation in output frequency with the PVT corners is shown in Table 4.4. Table 4.5 shows the achieved values of different performance parameters of DPLL-II.

Table 4.4: Corner analysis of locking time of the proposed DPLL-II

Corners	Frequency Variation (%)	Locking Time(μs)
nom	-	2.5
ff	6%	2.6
ss	8%	4.8
sf	4%	2.3
fs	4%	2.3

Table 4.5: Achieved DPLL-II parameters

Parameters	Proposed DPLL-II
Supply Voltage (V)	1.8
PLL Frequency (GHz)	1.6
$Jitter_{c\text{-}to\text{-}c}$ (ps)	2.13@1.6GHz
$Jitter_{RMS}$ (ps)	5.1@1.6 GHz
Locking Time (μs)	2.5
Power Consumption (mW)	2.63

The proposed charges pump and phase frequency detector (PFD-II) with digital approach reduces the overall power budget of proposed DPLL-II design. The charge pump consumes only 0.35 mW. To evaluate the performance of proposed DPLL-II with other designs, comparative analysis of performance parameters is given in Table 4.6. The proposed DPLL-I has lower jitter as compared to work reported in [51].

Table 4.6: Relative comparison of parameters of proposed DPLL-I and DPLL-II designs with existing literature

Parameters	Proposed DPLL-II	Proposed DPLL-I	[51]	[57]	[60]	[80]	[87]	[88]
Supply Voltage(V)	1.8	1.8	1	1.2	1.8	1.8	1.2	1.8
PLL Frequency (GHz)	1.6	1.6	2.27-2.8	0.5-1.2	2.56	0.2–4	3.008	2.4-2.5
Ref. Frequency (MHz)	25	25	275	-	20	-	47	200
$Jitter_{(RMS)}$ (ps)	5.1	0.642	3.73	1.5	-	0.35	0.357	-
Locking Time (µs)	2.5	2.8	-	-	2.05	-	-	3.1
Power Consumption (mW)	2.63	2.3	1.82	2.6	6.9	10	4.6	-
Area (mm^2)	0.013	-	0.93	0.02	0.24	0.045	0.047	-
Technology Process	CMOS 180	CMOS 180	CMOS 65	CMOS 130	CMOS 180	CMOS 180	CMOS 65	CMOS 180

The proposed DPLL-I has lower power consumption as compared other designs given in the Table 4.6. The work shown in [57] has higher jitter compared to DPLL-I and power consumption in the similar range as DPLL-I. DPLL-II shows lower area consumption as compared to [60, 80]. Though the design reported in [87] has higher output frequency range and reduced jitter, but shows more power, and area consumption as compared to proposed DPLL designs. The proposed DPLL-II has lower locking time as compared to work in [88]. The proposed DPLL-II shows a wide output frequency range, reduced jitter, and it consumes lower layout area in the 0.18 μm technology. The locking time is superior in these works with adequate levels of power consumption as compared to other works shown in Table 4.6.

4.18 Disadvantages of DPLL design

Two DPLL designs are analyzed and discussed. The proposed DPLL designs achieve low power, low periodic jitter and meet the given specifications. The DPLL designs also show the fast-locking time. Though DPLL designs have met the given specifications but they have few disadvantages.

- The digital design methodology achieves low power but portability to newer technology requires the more design efforts as full custom approach is mandatory to design the DPLL designs.
- The cost and time to market is increased.
- The PVT variations are more in range of 6%-8% for output frequency of 1.6 GHz.
- Area required by MOSCAPs increases the overall area of DPLL designs.

4.19 Conclusion

The DPLL's design and top-level design of the proposed DPLL-I and DPLL-II have been discussed in this chapter. In this chapter, two charge pump PLL's are designed using digital design approach with focus on achieving low jitter, low power, and small area. Firstly, the proposed compact charge pump was designed to reduce overall an area and power budget of DPLL. PFD-I based on dynamic logic is designed.). Then secondly, inverters, and buffers based fast PFD-II improves a locking time *i.e.* 2.5 μs of DPLL-II. This PFD-II also improves locking time and it used in DPLL-II. Thirdly, the pseudo differential VCO-I using inverters as variable load and phase interpolators is designed. This VCO-I shows a superior phase noise of -137dBc/Hz. The proposed VCO-I is used in two digital PLL architectures. The RMS jitter of 0.2 ps is achieved for DPLL-I architecture. The reduced a $jitter_{c\text{-}to\text{-}c}$ of 2.13 ps is obtained for DPLL-II after post layout simulations. The main aim of designing a DPLL-I is to achieve low power, low area, low jitter by using digital technology. DPLL-II architecture is designed using

standard cells and achieves low power, low area and fast locking time. A novel inverter and buffer-based PDF-II is proposed. The novel inverter and switch-based charge pump is proposed to achieve low power. VCO-II is also designed using inverter only. Finally, proposed DPLL's with digital design methodology and switch logic shows the merits like low jitter and lesser area consumption. These DPLL architectures works at frequency of 1.6 GHz and designed in CMOS 0.18 μm technology can be used to produce clock in SoC, wireless transceiver and battery-operated applications. In order to overcome the problems of DPLL designs, all-digital phase locked loops are designed to meet the design specifications. The all-digital phase locked loops give a number of advantages as compared to the conventional DPLL designs. The following chapters describe ADPLL architecture for low power and low periodic jitter for given specifications of target applications.

CHAPTER 5

DESIGN AND ANLYSIS OF LOW POWER ALL DIGITAL PHASE LOCKED LOOP

5.1 Introduction to Low Power ADPLL

This chapter explains the design and analysis of the low power dual path ADPLL-I design for periodic jitter with value 6.6 ps and power consumption with value of 6.35 mW for high speed SoC applications. The target specification of power consumption is less than 8 mW for SoC applications [17]. The section 5.2 shows the requirement for low power circuit designing in the present-day technology. Section 5.3 shows the issues in ADPLL-I design and need of calibration. Also, section 5.3 gives information of the proposed ADPLL-I architecture. The section 5.4 explains a 4-bit flash TDC with calibration and its simulation results are depicted in section 5.5. The details and working of digital loop filter are given in the section 5.6. Sections 5.7 and 5.8 discuss the proposed VCO-I with its simulation results respectively. Section 5.9 describes the ADPLL-I architecture and it working. Section 5.10 shows the simulation results of ADPLL-I. Lastly section 5.11 concludes an ADPLL-I design.

5.2 The need of Low Power Design in Current ADPLL Design

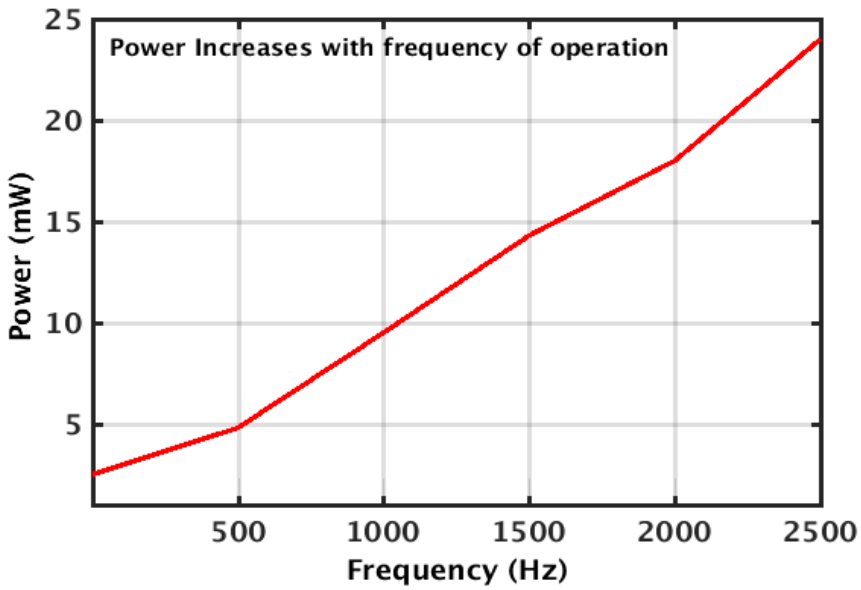
With the advent circuit expertise and technology, the large area consuming, and power-hungry analog blocks are replaced with a low power, low area, and robust digital bocks. Internet of things (IoT) shows improved performance in wireless sensor-based communication applications like agricultural and medical applications [1-5]. The battery operated and IoT based applications use more than 90% of the battery power in applications like heart rate monitoring [89-90]. The ADPLL used for IoT also consumes 40% power [7]. Therefore, high-performance ADPLLs with low power and low jitter are essential in applications like IoT, wireless transceiver, high speed SoC, and etc. The low power design is required because following reasons: growth of battery-powered systems, reliability, portability, and mobility [6-7].

5.2.1 Power Impact on System Design

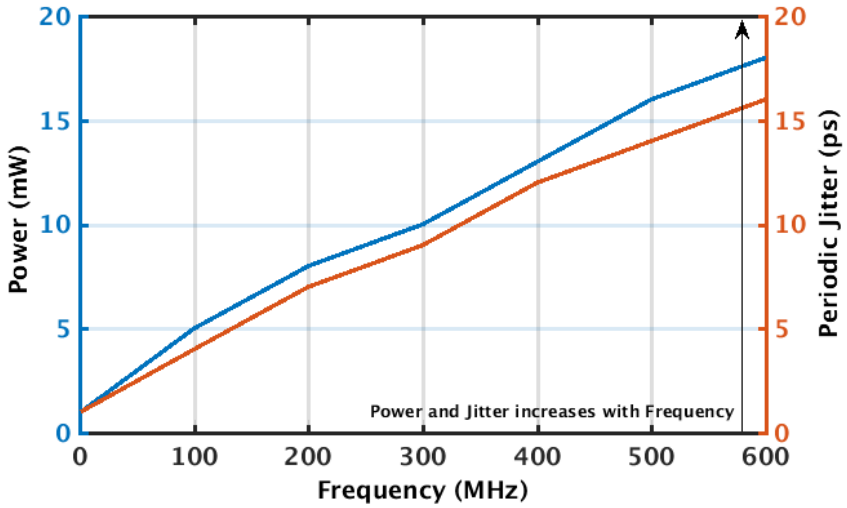
The power consumption of any circuit is directly proportional to its frequency of operation [89]. There are different sources of power consumption in CMOS technology like dynamic power, static power, and switching power [89]. The dynamic power dissipation happens whenever the logic level changes at output points due to change in the input signals. The switching power P_{sw} is given by:

$$P_{sw} = \alpha * C_L * V_{DD}^2 * f_{clk} \tag{5.1}$$

Where C_L is load capacitance, V_{DD} is supply voltage, α is switching activity, f_{clk} is the clock frequency. The load capacitance $C_L = \sum C_{IN} + C_{wire} + C_{par}$ where C_{IN} are the gate input capacitance, C_{wire} is the parasitic interconnect, and C_{par} is the diffusion capacitances of each gate [89-90]. Other than this, the short circuit power also contributes to the power consumption but majorly dynamic power affects overall power budget of system. The designing a low power ADPLL for high speed SoC applications is one of the most challenging research fields in current scenario. The significant benefits of ADPLL over conventional DPLL are like mitigation to PVT variations and low-cost digital processes. However, ADPLL have a critical disadvantage like more power and area consumption resulting from the digital-controlled oscillator (DCO) and TDC [91-92]. For a given power and area budget, at given supply voltage and frequency of operation, designing the low power ADPLL is challenge because as frequency increases, power also increases as shown in the Fig. 5.1 (a). In ADPLL, after DCO, the most power and area consuming block is TDC. Fig. 5.1 (b) shows the jitter and power relation with increasing frequency. As frequency increases, both power and jitter increases. Also, TDC significantly impacts the performance parameters such as the output jitter and locking time of ADPLL [73-75]. DCO is another major block which consumes power and also affects the jitter, phase noise, and output frequency range of ADPLL. Therefore, designing a low power TDC and DCO is essential. However, designing a low power and low area TDC with high resolution is a challenge in current design scenario.



(a)



(b)

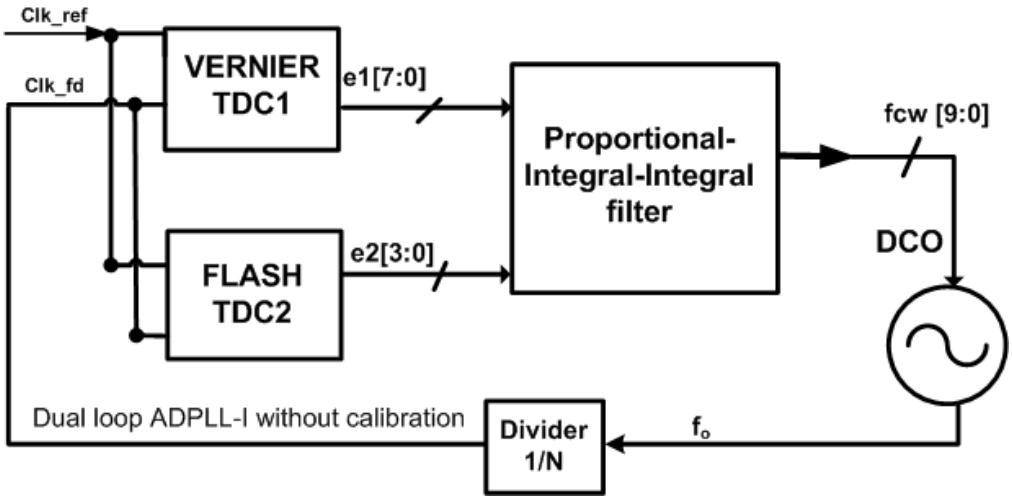
Fig. 5.1(a) Variation of power consumption with frequency of operation [90], (b) Power and jitter with frequency [91]

Also designing a DCO with low power and low jitter is difficult. ADPLL provides a more resilience to frequency drifts in the output frequency, faster acquisition, wider lock range, and reduced area consumption as compared to conventional DPLLs. The modern paradigm of ADPLL should have a lower power consumption, reduced jitter, and fast locking time with wide operating range of output frequency.

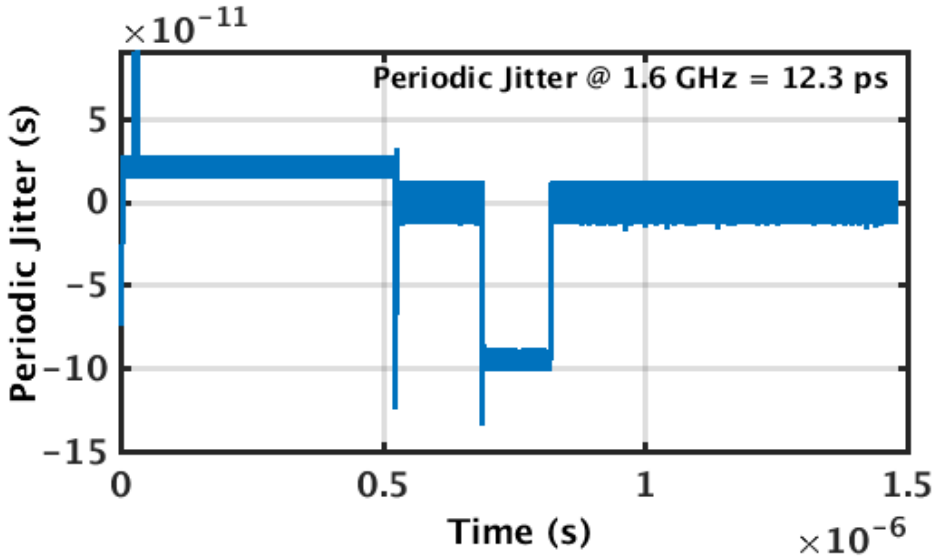
5.3 Design of ADPLL-I and current issues with the ADPLL-I

For battery operated portable applications, low power, and low periodic jitter are major design concerns. ADPLL-I is designed for SoC applications with the target power consumption < 8 mW [17]. The flash architecture gives advantages like fine resolution, lower area, higher speed, and lower power consumption. However, the dynamic range reduces as the bits are decreased that reduces the dynamic range of ADPLL. In order to meet the wide bandwidth requirement of ADPLL-I, the 4 bits are chosen to design a flash TDC which is described in the section 3.3. The 4-bit TDC2 achieves a periodic jitter of 0.75 ps. ADPLL-I design consists of 8-bit TDC1, TDC2 without calibration, DCO, dividers, and loop filter. The proposed ADPLL-I is implemented using 8-bit TDC1 and proposed 4-bit flash TDC2 to achieve low jitter. The dual path ADPLL is shown in the Fig.5.2 (a). The proposed ADPLL-I works in 2 loops concurrently. The clock Clk_ref is provided to TDC1 and TDC2 and error signals e1 [7:0] and e2 [3:0] are generated respectively. After few clock cycles, Clk_fd is generated by ADPLL-I. The error signals e1 [7:0] and e2 [3:0] are modulated by the proportional-integral-integral filter and produce control word fcw. The control word fcw [9:0] is given to DCO and output frequency of DCO is varied. The dual path ADPLL-I without calibration gives a periodic jitter of 12.3 ps

as shown in the graph in the Fig. 5.2 (b). Fig. 5.2 (c) shows a variation in the output frequency without calibration and maximum variation of 10% and 11% across FF and SS corners respectively is observed. The power consumption is 10 mW for ADPLL-I without calibration. This architecture does not meet the given specification of periodic jitter and power consumption for SoC applications. Therefore, in order to improve the periodic jitter of ADPLL-I, periodic jitter of TDC2 is improved using LMS based calibration algorithm. It is observed calibration has improved the periodic jitter of 4-bit flash TDC2 and thus also improves the periodic jitter of ADPLL-I design. In order to make the proposed ADPLL-I immune to PVT variations, least mean square (LMS) [93] based calibration technique is used in proposed 4-bit flash TDC2. The present work uses a simple, 4-bit flash based TDC architecture which takes 1 clock cycle to generate the error bits.



(a)



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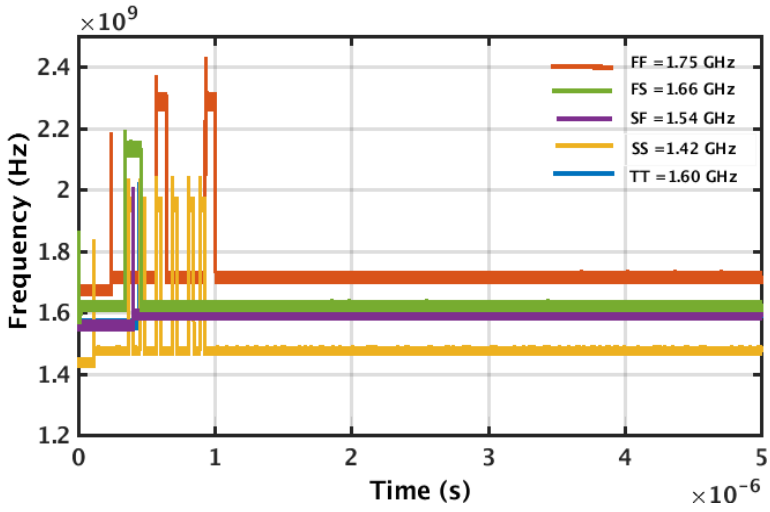

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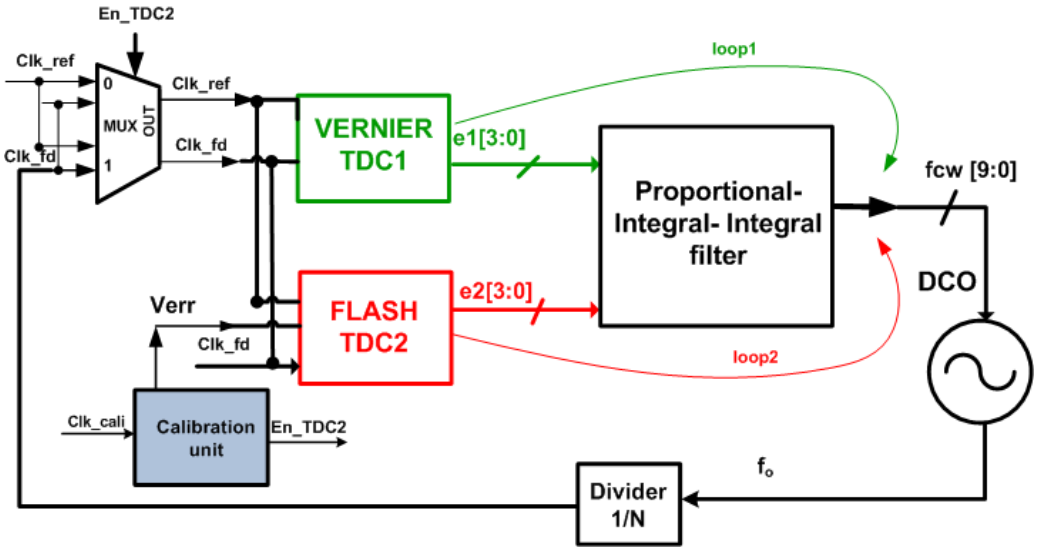


(d)

Fig. 5.2 (a) ADPLL-I- without calibration (b) Periodic jitter of ADPLL-I, PVT variation at output frequency of 1.6 GHz- without calibration, (c) Shows a PVT variations in the output frequency -without calibration, (d) Block level diagram of ADPLL-I-with calibration

Fig 5.2 (d) shows a dual path ADPLL-I architecture with calibrated 4-bit flash TDC2. It consists of two loops. The 4-bit flash TDC2 which is shown in the Fig. 3.3 and discussed in the section 3.3 used to design ADPLL-I. The clock Clk_ref is given to TDC1 and simultaneously, TDC2 is calibrated using LMS unit. The existing SAR TDC [73] is taken as reference TDC and local feedback Clk_fdl is generated using other TDC1 (2-bit) to calibrate TDC2. The En_TDC2 is generated by the FSM is used to switch between the two loops. When the phase difference between Clk_ref and Clk_fd lowers to range of TDC2, En_TDC2 used to switch to TDC2. The output errors of TDC1 and TDC2 are given to the proportional-integral-integral filter which scales it by gain factors. The output of filter is given to the DCO which varies its frequency according to control word. Since TDC1 is low resolution therefore,

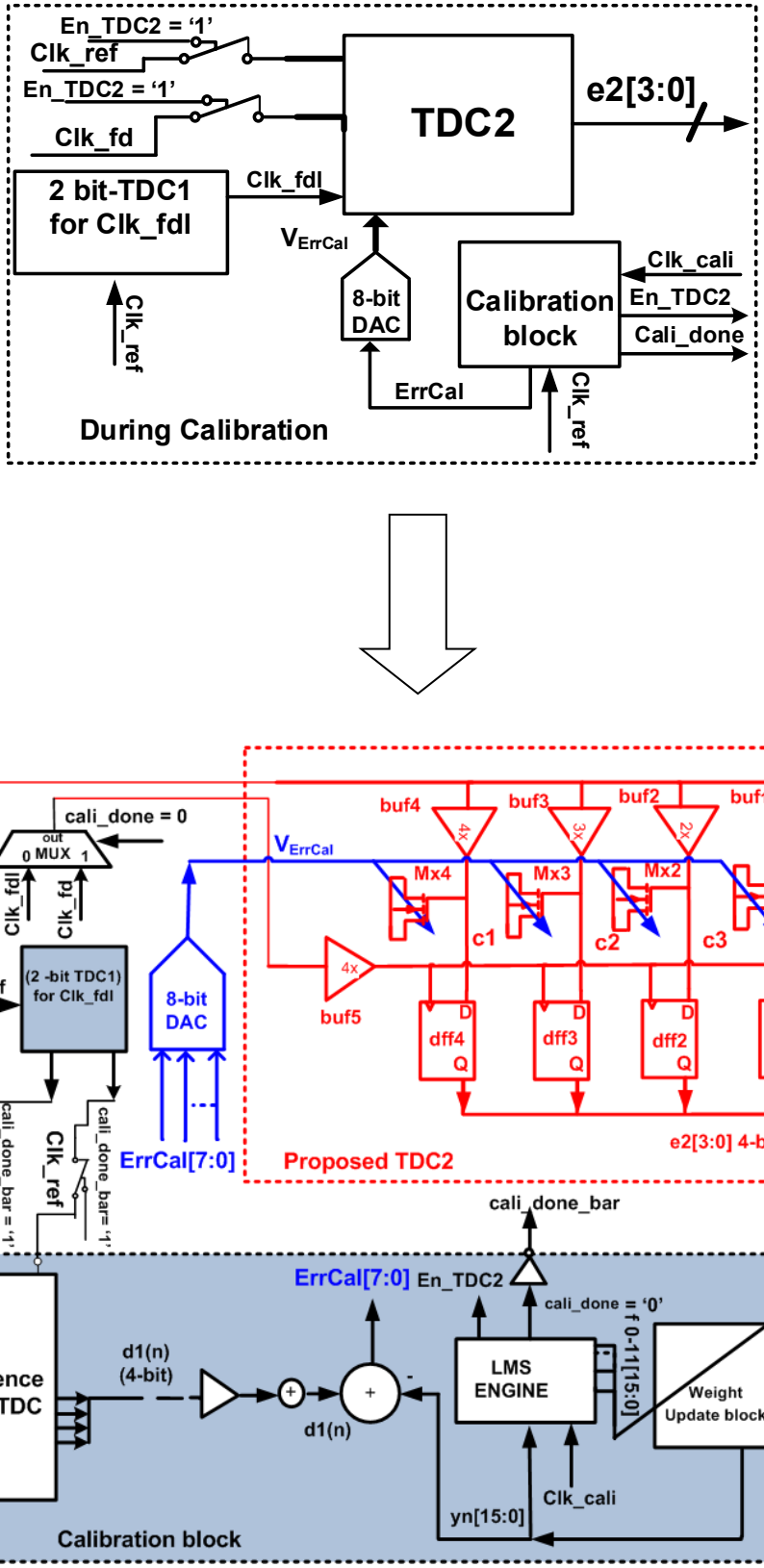
calibration is not required and it does not impact the performance parameters of ADPLL-I. The ADPLL-I gets locked at 1 μs with output frequency of 1.6 GHz. The next section gives detail of 4-bit flash TDC2**.**

5.4 Proposed 4-bit Flash TDC2 with Calibration

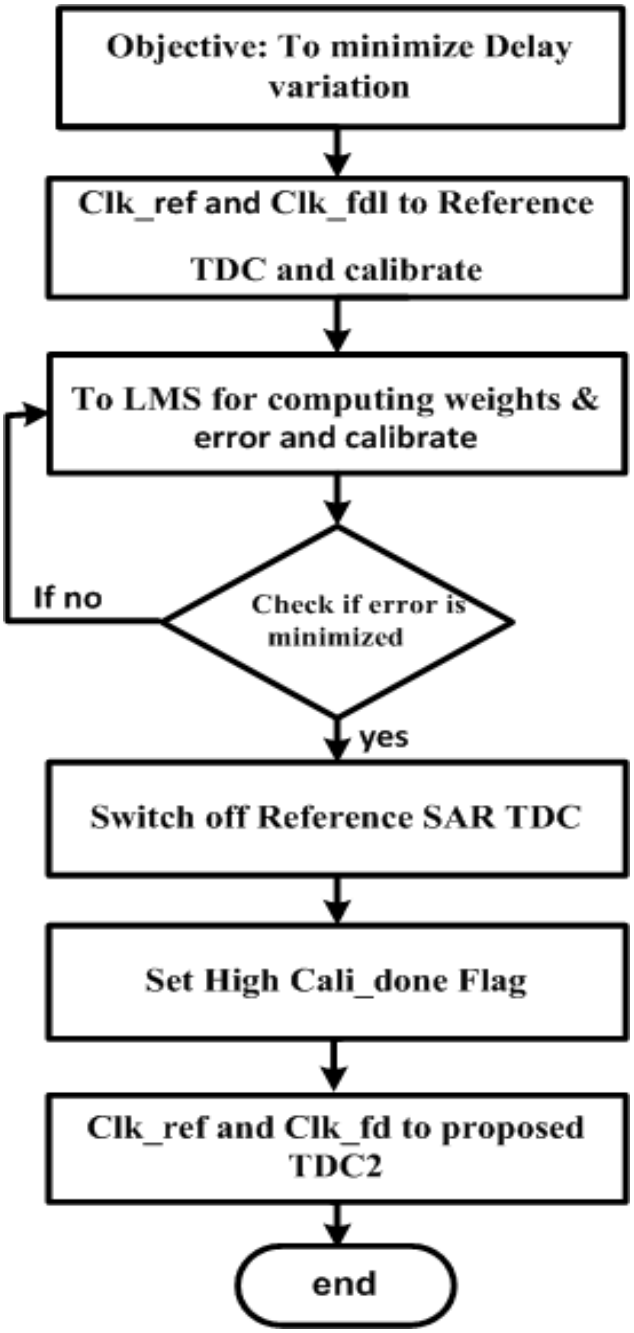
The proposed ADPLL-I architecture is designed to achieve the low power and low periodic jitter. A proposed 4-bit flash TDC2 has periodic jitter of 0.75 ps and PVT variation of 30% - 40% which is not suitable to design ADPLL-I. Though the proposed 4-bit TDC achieves low power and low periodic jitter but proposed flash TDC suffers from PVT variations and degrades the performance metrics of TDC. The resolution of TDC2 is given as $\Delta\tau = \tau_i - \tau_{i-1}$ where τ_i is delay of i^{th} buffer with i ε (1-4). To maintain the improved jitter and resolution due to PVT variations, a LMS based calibration algorithm [93] is adopted in this work for TDC2. LMS based algorithm works on principle of producing least mean square of error signal between actual and desired signal by using optimum values of filter coefficients. It is an adaptive filter. In this present work, desired signal is generated by using reference SAR TDC and actual signal is generated by the flash TDC. The error signal between them is used to fix at delay variation of buffers of flash TDC during PVT variations. Fig. 5.3 (a) shows a 4-bit flash TDC with calibration. Fig. 5.3 (b) shows the calibration steps of proposed 4-bit flash TDC2. Initially at the start up, a local feedback clock *i.e.* Clk_fdl is generated using a 2-bit Vernier based TDC1 to calibrate the TDC2. For calibration purpose, a slow but accurate reference TDC based on successive approximation register (SAR) logic is used [75]. The existing 4-bit SAR TDC consists of only multiplexers and D-flip-flops along with delay elements. It is advantageous to use SAR TDC as it increases a delay cell linearly with the increase in number of bits as compared to other TDC architectures like inverter delay line and Vernier TDC [73-74]. The delay cell chain grows exponentially with number of bits in Vernier and inverter delay line [73-74], thus affecting the power and area. To start the calibration, an external clock signal Clk_cali with period of 20 ns is given, Cali_done/Cali_done_bar signal is '0'/'1' and the output generated by TDC2 *i.e.* e2[3:0] is '0000'. Also, the weights f [15:0] assigned to the FIR filter of calibration block are set to state '1'. After the calibration is over, Clk_cali gets reset, Cali_done/Cali_done_bar signal is set to logic '1'/'0' by the finite state machine (FSM) in calibration block when error (ErrCal) becomes minimum and (V_{ErrCal}) is considered as logic zero by FSM after calibration. To reduce the design complexity, and power budget, delay tap length of FIR filter is taken as 11 for conversion. For calibration purpose, e2 [3:0] is made 16-bit by inserting zeros in remaining MSB's. The output of FIR filter is defined by:

$$y[\mathrm{n}:0] = \sum_{i=0}^{i=M-1} \mathrm{e2}[3:0][n-i] * \mathrm{f}[\mathrm{n}:0] \tag{5.2}$$

where i is the number of coefficients, M is length of FIR filter, n is number of bits of output of filter, and is equal to15. Initially, the value of the 4-bit output generated by SAR TDC is '0000'.



(a)



(b)

Fig. 5.3 (a) Proposed architecture of TDC2 with calibration, (b) Calibration steps of TDC2

Therefore, in order to make the error between reference input d1n [3:0] and actual input e2 [3:0] minimum, LMS algorithm is used in which the weights of tapped delay FIR filter are updated. To compute the minimum error (ErrCal) approximately near to zero, d1n [3:0] and yn[15:0] are given to LMS engine which update the weights f [15:0] according to

$$f_{final} = f + ErrCal * \mu * e2 \tag{5.3}$$

$$ErrCal = d1n - yn \tag{5.4}$$

where μ is the step size which reflects the convergence speed [93]. To reduce the complexity of design, the step size μ and the values of preliminary weights f are taken as '1'. The error voltage (V_{ErrCal}) from the DAC [29] settles at different values with different values of μ as shown in the Fig.5.4 (a). Error saturates at the minimum value once the weights become constant and remains constant until the next phase of calibration. In this design, current-output DAC is built from CMOS NAND gates given in the Fig. no.12 in reference [29]. The PMOS-current-source array is made by driving one of the two NAND gate inputs by a digital control word and the other input is kept fixed and the analog output is taken by connecting outputs of 8 NAND gates together. By connecting one input of NAND gate to its output and the other input connects to logic '1', NMOS current mirror is designed. The 8-bit DAC is adequate to characterize the error voltage in order to achieve the periodic jitter up to 1 ps for proposed TDC2. The calibration block produces a ErrCal [7: 0] and it is given to DAC. The output of 8-bit DAC is error voltage (V_{ErrCal}) can used be used to control the delay of buffers by changing the gate capacitance values of a MOSCAP (Mx1-Mx4). The value of error voltage (V_{ErrCal}) changes according to variation in 3-bit flash TDC. In order to tune delay of buffers (buf1 to buf4 in TDC2) with error voltage (V_{ErrCal}), a MOSCAP (Mx1-Mx4) is used at output of each buffer as shown in the Fig. 5.3 (a).

Table 5.1: Parameters of proposed TDC2

Parameters	TDC2 (with calibration)
Delay Elements	5
Number of Bits	4
Conversion Time (cycle(s))	1 clock
Dynamic Range (ps)	Lower (30)
Resolution (ps)	6
Architecture Type	Flash
Power Consumption (mW)	0.39
Periodic Jitter (ps)	0.61

It stabilizes the delay of buffers by fixing the MOSCAP values even with PVT variations. The propagation delay of ith buffer τ_i as shown in Fig. 5.3 (a) is given by equation (5.5) [94]:

$$\tau_i = 2.\frac{\sqrt{C_{L,i}}VDD}{\sqrt{C_{in,i}}}\left(\frac{1}{k_n\frac{W_i}{L_i}.(VDD-V_{tn})}+\frac{1}{k_p\frac{W_i}{L_i}.(VDD-V_{tp})}\right) \quad (5.5)$$

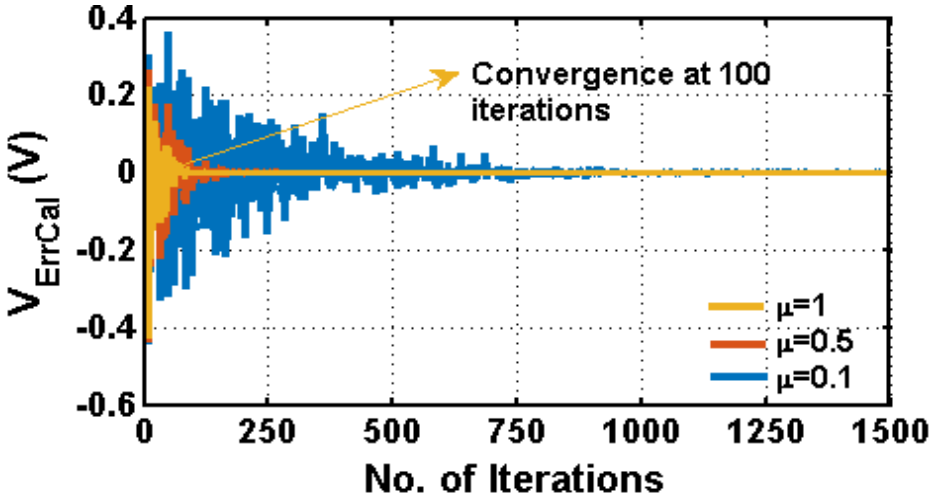
where $(C_{L,i} = C_{buf,i} + C_{Mx,i})$ and $C_{in,i}$ are the capacitances at output and input of buf,i respectively. Here $C_{Mx,i}$ is the gate capacitance of Mx,i and $C_{buf,i}$ is the intrinsic output capacitance of buf,i. W_i and L_i are width and length for buf,i respectively. Since the gain of TDC is an inverse of resolution [73-74], therefore gain of TDC2 is

$$K_{TDC2} = \frac{1}{\Delta\tau} = \frac{1}{6\ ps} \tag{5. 6}$$

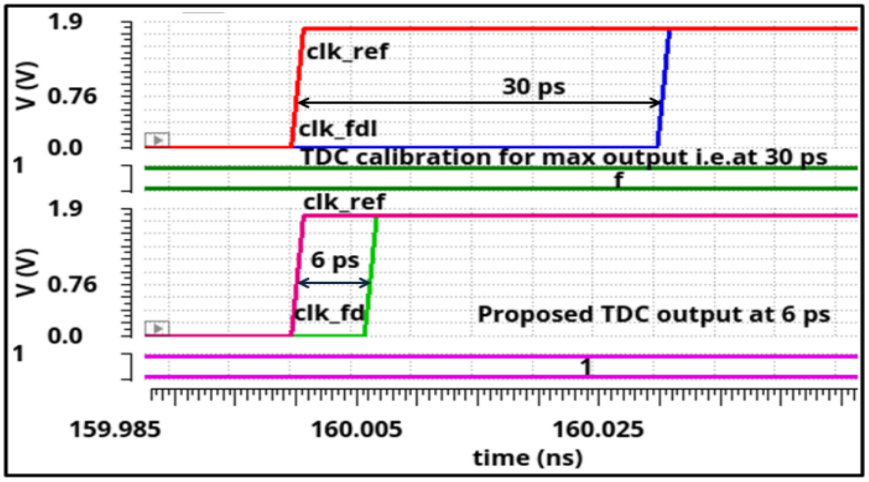
The achieved parameter of proposed TDC2 is given in Table 5.1. It observed that proposed TDC2 achieves fine resolution of 6 ps and power consumption of 0.39 mW. Also, the proposed TDC2 has high speed as gives output only in one clock cycle.

5.5 Simulation Results of 4-bit Flash TDC2 with Calibration

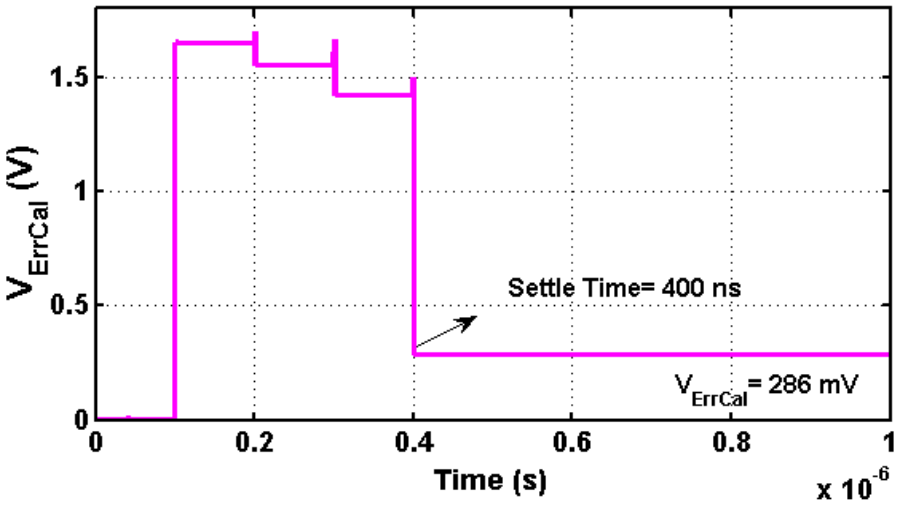
The simulations result of 4–bit flash TDC without calibration is shown in the section 3.3. The periodic jitter of 4-bit flash TDC2 without calibration is 0.75 ps. The calibration is done for proposed 4-bit flash TDC2 and simulation results are shown in this section. With decrease in the μ value, the error minimization time is increased due more computation involved in the process as clear from the Fig. 5.4 (a). As we increase the value of μ, the settling time for error (ErrCal) decreases from 1000 iterations to 100 iterations for value of μ from 0.1 to 1. In this case typical Δτ =6 ps and is governed by target periodic jitter specification of 8 ps in current ADPLL-I design. Further increasing the bits in TDC2 provides a higher resolution but the range is reduced. The calibrated output of TDC2 for maximum range is shown in Fig. 5.4 (b). The proposed TDC2 is calibrated for maximum range of 30 ps between the Clk_ref and Clk_fdl and to generate the difference of 30 ps between Clk_ref and Clk_fdl, a Vernier based TDC1 with 2-bit is sufficient. To overcome the problem of limited range of TDC2 in an ADPLL-I, a low resolution TDC of Vernier type (4-bit TDC1 shown in the Fig. 3.1 (b)) in parallel to TDC2 is used which has wider range. The resolution of TDC1 is chosen as 4-bit to limit the area and power consumption. The delay difference reduces to range of TDC2 *i.e.* 30 ps after few clock cycles. The digital error generated by the calibration block is sent to 8-bit DAC [29] to produces an error voltage (V_{ErrCal}) of 286 mV corresponding to DAC input of '00000001'as shown in the Fig. 5.4 (c). The 8-bit DAC [29] is adequate to characterize the error voltage Verr to achieve target periodic jitter of TDC2 ≅ 1 ps. The error voltage (V_{ErrCal}) settles at different values according to the step size. It is clear that without calibration, periodic jitter variation is more with standard deviation of 116 fs and mean value 715 fs as shown in the Fig. 5.4 (d).


Convergence at 100 iterations
μ=1
μ=0.5
μ=0.1
V_ErrCal (V)
No. of Iterations

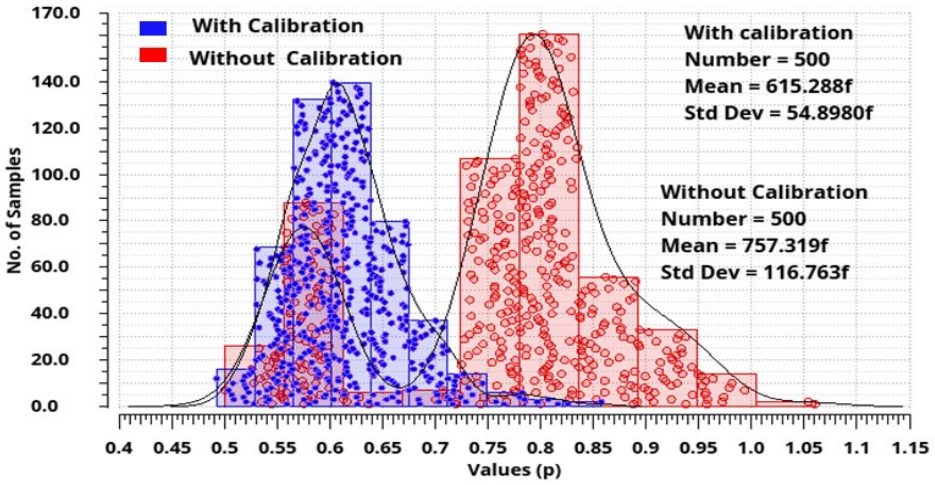
(a)


clk_ref
30 ps
clk_fdl
TDC calibration for max output i.e.at 30 ps
clk_ref
6 ps
clk_fd
Proposed TDC output at 6 ps
V (V)
time (ns)

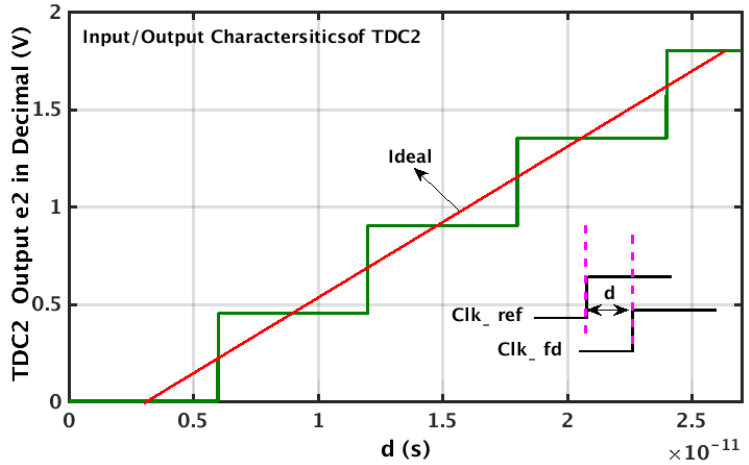
(b)


Settle Time= 400 ns
V_ErrCal = 286 mV
V_ErrCal (V)
Time (s)
x 10^-6

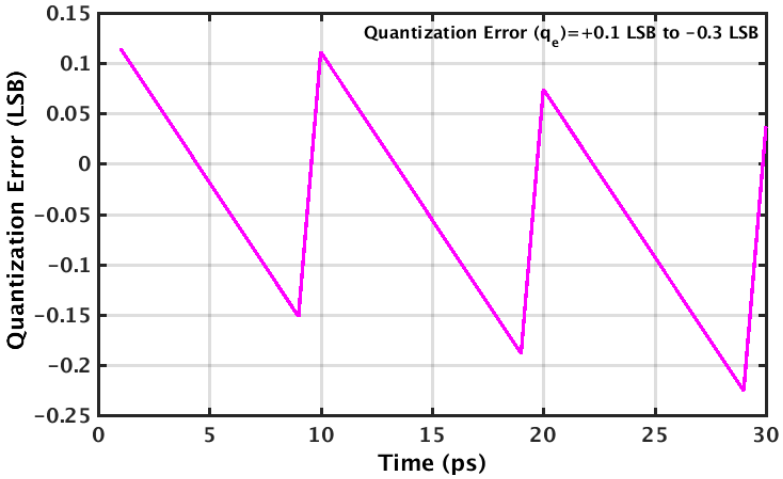
(c)



(d)



(e)



(f)

Fig. 5.4 (a) Variation of μ, (b) V_{ErrCal} saturation of TDC2, (c) Calibrated output of TDC2, (d) Comparison of period jitter of 4-bit flash TDC2 without calibration and with calibration, (e) Input and output characteristics of 4 -bit flash TDC2, (f) Quantization error of 4-bit flash TDC2

The TDC2 achieves a periodic jitter of 0.6 ps with calibration. After calibration, the proposed TDC2 achieves a periodic jitter of 0.6 ps. With calibration, the periodic jitter is reduced and variation due to mismatches is also reduced. The input and output characteristic of 4-bit flash TDC2 is shown in the Fig. 5.4 (e). The quantization error value of TDC2 lies in the range of -0.3 to 0.1 LSB as shown in the Fig. 5.4 (f). The proposed 4-bit flash TDC2 consumes power of 0.39 mW which very low as compared to other exiting designs.

5.6 Digital Loop Filter-I

As described earlier ADPLL-I works in two loops *i.e.* loop1 and loop 2. Therefore, 2 different filters are required to produce the control word as shown in Fig. 5.2 (d). In loop1, 4-bit Vernier TDC1 is working with digital loop filter in proportional and integral path with α as proportional and β as integral path coefficient respectively. Given the bandwidth, low jitter, and the proportional and integral coefficient of the PI controller, filter can be derived. The digital loop filter is shown in the Fig. 5.5 (a). For stable operation of ADPLL-I, the ratio of β and α should be much less than one [19].

$$\frac{\beta}{\alpha} << 1 \tag{5.7}$$

The ratio of α and β decides the stability of ADPLL for given reference frequency, phase margin, and unity gain bandwidth as shown in equation (5.8).

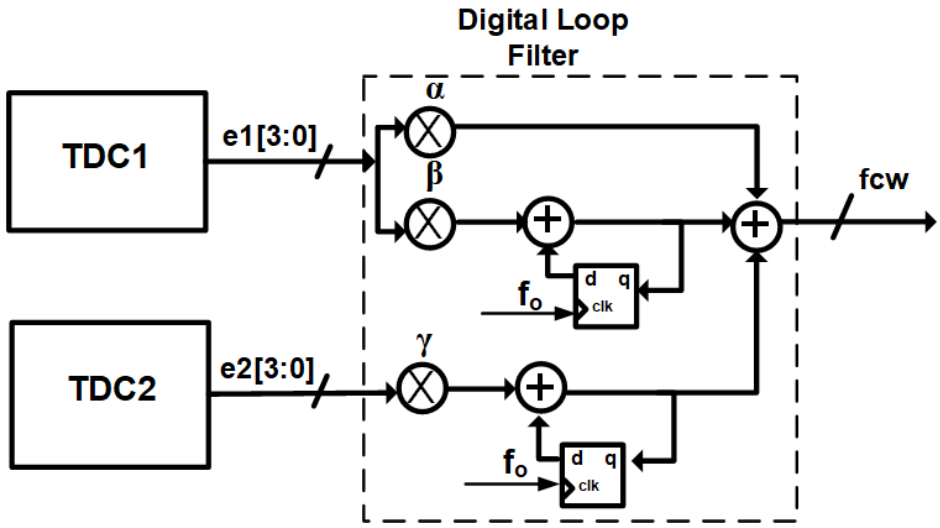
$$\frac{\alpha}{\beta} = \frac{f_{ref} \tan(PM)}{f_{UGB} 2\pi} - \frac{1}{2} \tag{5.8}$$

where PM is phase margin, f_{ref} is reference frequency, f_{UGB} is unity gain bandwidth, and N is the division ratio of ADPLL-I. It is concluded from equation (5.7) that for the given ADPLL-I reference frequency and the unity gain bandwidth, the ratio of β and α defines the phase margin and therefore the stability of an ADPLL-I system. The value α also depends upon the gain and jitter of DCO in the ADPLL.

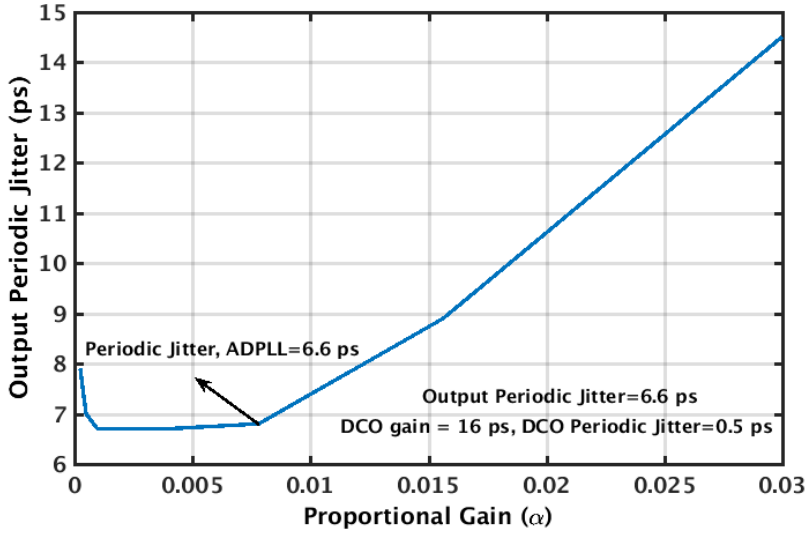
$$\alpha = \frac{\sqrt[4]{3\pi/8}}{\sqrt{N}} \frac{1}{K_{DCO}} \sigma_{DCO} \tag{5.9}$$

where N is the division ratio, K_{DCO} and σ_{DCO} are the gain and periodic jitter of DCO respectively. The proportional gain α significantly affects the periodic jitter of ADPLL-I [45]. Therefore, to obtain optimized jitter of ADPLL, a low gain and low jitter of DCO is required.

Fig. 5.5 (b) shows the variation of proportional gain α with the output periodic jitter of ADPLL-I.



(a)



(b)

Fig. 5.5 (a) Digital loop filter, (b) Proportional gain variation with output jitter

Initially for lower values of α, periodic jitter is more and then it becomes constant and finally it increases. The Z-domain transfer function of the digital loop filter for loop 1 is given by the following equation (5.10) [19, 20, 95]:

$$H(Z1) = \alpha + \frac{\beta}{1 - Z^{-1}} \tag{5.10}$$

Once TDC1 lowers phase difference to TDC2 range (*i.e.* 30 ps), ADPLL-I switches to loop 2 using signal En_TDC2 generated by calibration block. In loop2, the gain of ADPLL-I is affected by the TDC1 and as well as TDC2. In order to stabilize the ADPLL-I, an additional integral path with coefficient γ for proposed TDC2 is needed. 4-bit Vernier TDC1 and 4-bit

flash TDC2 together produces a floating point 32-bit output word. The following equation gives a loop filter transfer function during the loop2 working:

$$H(Z2) = \alpha + \frac{\beta}{1 - Z^{-1}} + \frac{\gamma}{1 - Z^{-1}} \tag{5.11}$$

The 10-bit MSB's from the output word of digital loop filter fcw [9:0] are used to tune the frequency of VCO-I and rest LSBs are truncated. The locking time and phase noise performance of ADPLL decides the bandwidth f_{bw} and coefficients of DLF. The coefficients of DLF enormously impact the bandwidth of ADPLL [96]. Generally, f_{bw} should be 10 times lesser than the reference frequency f_{ref} for loop stability [96] and in this case f_{ref} is 25 MHz and f_{bw} is chosen as 1 MHz. To achieve fast locking of 1μs and for the periodic jitter to be within ±1% of output frequency (*i.e.* 1.6 GHz), the optimum values for α, β, and γ are chosen as 2^{-6}, 2^{-8}, and 2^{-8} respectively.

5.7 Digitally Controlled Oscillator

In this work, the combination of VCO-I and 10-bit DAC [29] works as DCO as shown in the Fig. 5.6. The pseudo differential VCO-I is shown in the Fig. 4.5 (b). The 10-bit DAC is used to convert digital output of filter to analog. The 10-bit DAC gives accurate output which is enough to achieve a periodic jitter of 6.6 ps for ADPLL-I. With free running frequency of 1.6 GHz is proposed.

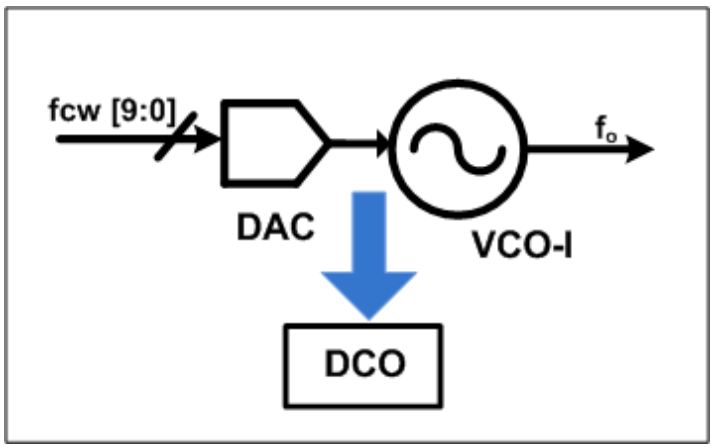
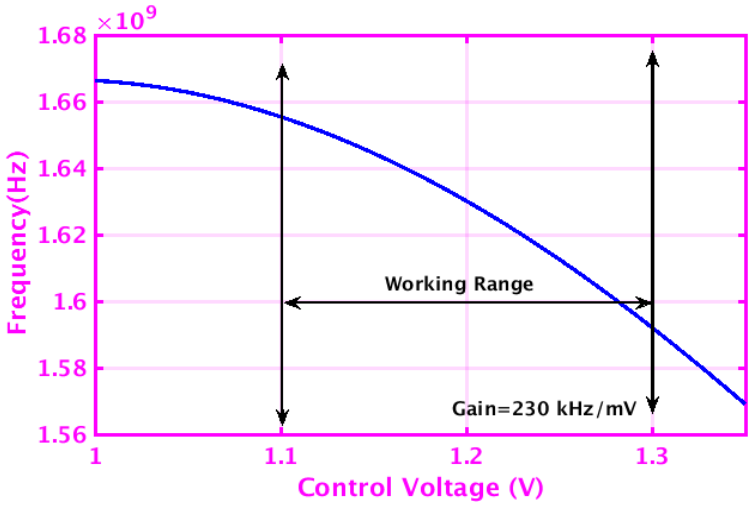


Fig. 5.6 Proposed DCO

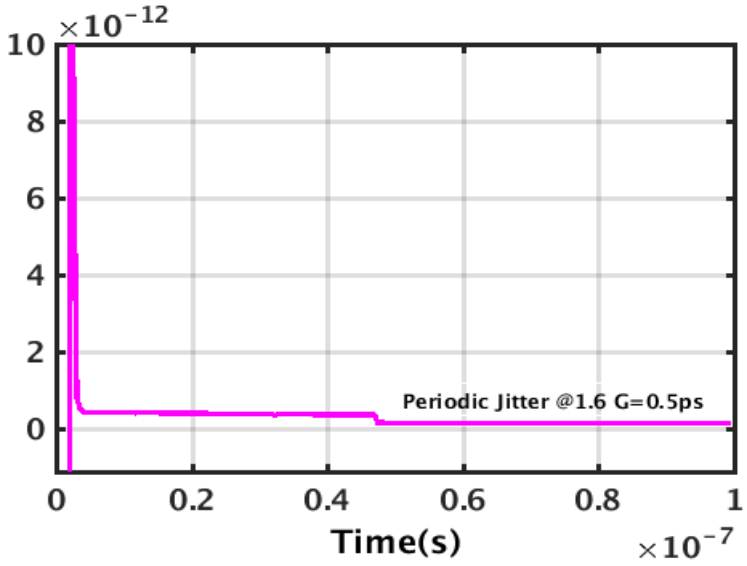
The design and working of proposed VCO-I is discussed in the section 4.7 and the simulation results of VCO-I are shown in the section 4.8

5.8 Simulation of DCO

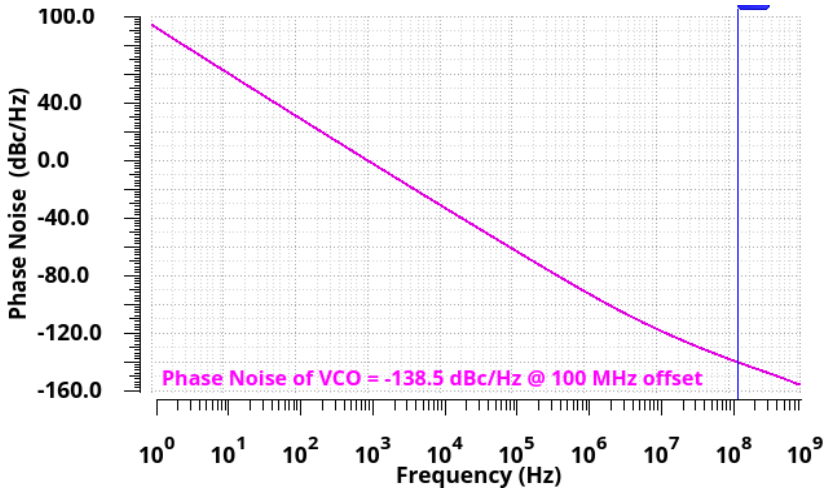
The DCO is designed with free running frequency of 1.6 GHz with periodic jitter of 0.5 ps which is required according to the specification necessary for the ADPLL design. The gain of DCO directly affects the jitter and phase noise of ADPLL-I. Lower gain of VCO is required to achieve low phase noise ADPLL-I. Fig. 5.7 (a) shows the gain of DCO and it is 230 kHz/mV which is optimized for a given output frequency specification of 1.6 GHz. The Width W=2.6 µm of MOS transistors is used in Inverter-cap (Invc1 to Invc4) working as load to achieve a desired output frequency of 1.6 GHz with minimum periodic jitter for ADPLL-I architecture. The periodic jitter of VCO-I is 0.5 ps as shown in the Fig. 5.7 (b). The phase noise of proposed VCO-I is -138.5 dBc/Hz which makes it suitable for designing low periodic jitter ADPLL architecture as depicted in the Fig. 5.7 (c).



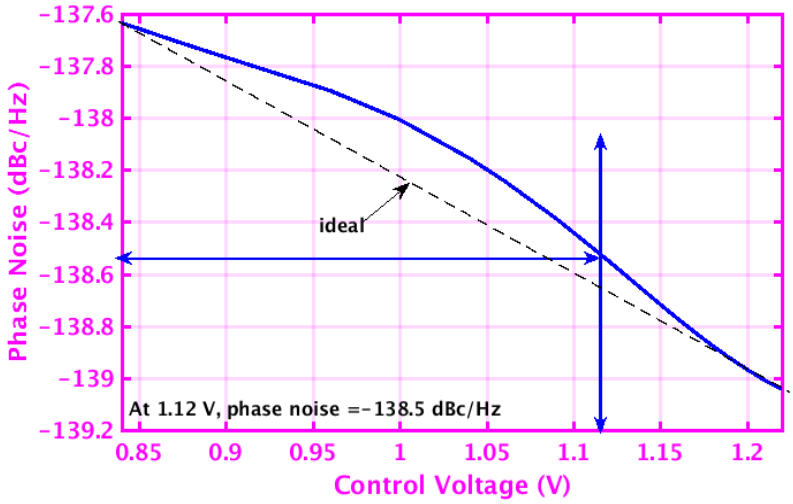
(a)



(b)



(c)



(d)

Fig. 5.7 (a) Gain of VCO-I for ADPLL-I, (b) Periodic jitter of VCO-I for ADPLL-I, (c) Phase noise of proposed VCO-I, (d) Phase noise variation of proposed VCO-I with control voltage variation

It is evident from the graph that as the control voltage is increased; the phase noise improves as shown in the Fig. 5.7 (d). This is due to increased power of carrier signal with increase biased control voltage. Further to achieve the low power ADPLL-I, low power VCO-I is used. The proposed VCO-I consumes power of 1.06 mW.

5.9 Architecture of ADPLL-I

This ADPLL-I consists of a DCO, two TDC's *i.e.* a conventional 4-bit Vernier TDC architecture (called as TDC1) in parallel with the proposed foreground calibration based 4-bit flash TDC (called as TDC2), DLF, and digital to analog converter (DAC). The important parameters of TDC are resolution and dynamic range which impact the performance parameters like periodic jitter, phase noise, and locking time of an ADPLL. Typically, an ADPLL has a phase difference of few hundred picoseconds between reference clock *i.e.* Clk_ref and feedback clock *i.e.* Clk_fd during its acquisition process. Therefore, a large

dynamic range and high resolution TDC is desirable in order to achieve the low periodic jitter ADPLL.

However, achieving a wide range TDC with high resolution remains a design challenge. To tackle this problem, a coarse 4-bit Vernier TDC (TDC1) is used which provides a wide range with low resolution. Along with it, a proposed 4-bit flash TDC (TDC2) is used which is high resolution but low range. In combination, both make a wide range and high resolution TDC. The dual path ADPLL-I (as shown in Fig. 5.8) is proposed in this work. ADPLL-I works in two loops *i.e.* loop1 and loop2. Initially, when the phase difference between Clk_ref and Clk_fd is more, TDC1 will generate the 4-bit error signal e1, which is used to drive the DCO. In this loop, ADPLL-I will bring the frequency near to reference frequency after few clock iterations and also lowers the phase difference to few picoseconds from initial nanoseconds range during loop1. Concurrently, during this time TDC2 is being calibrated. SAR TDC is turned on only during the calibration process. Once the weights become constant, it is reset to minimize the power until the next calibration phase starts.

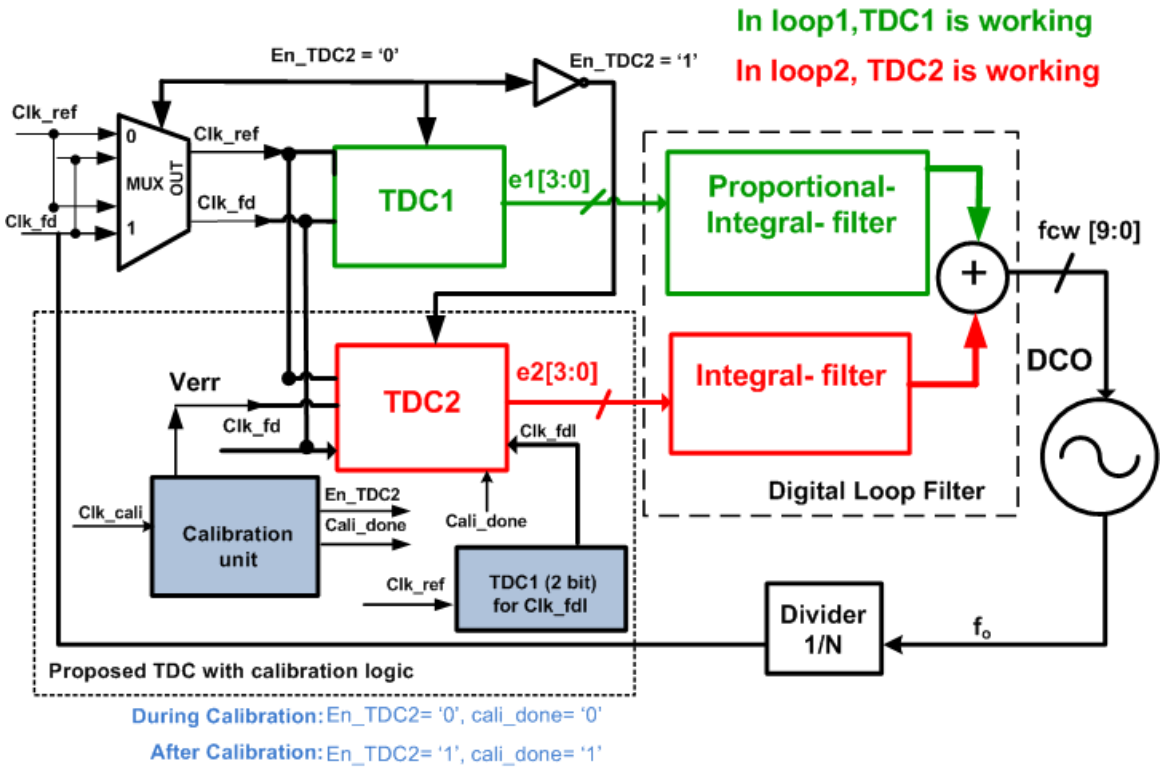
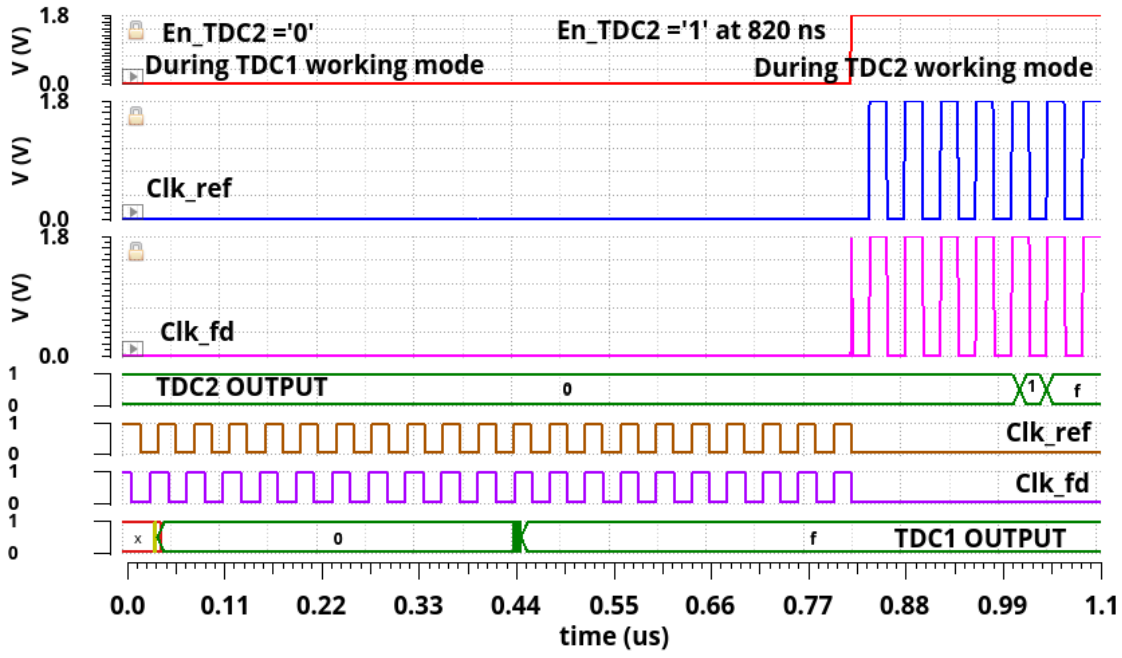


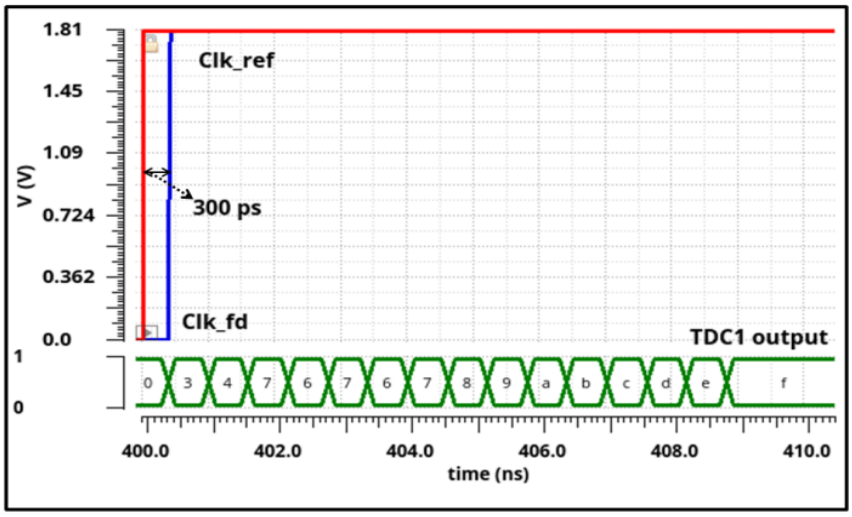
Fig. 5.8 Proposed ADPLL-I

ADPLL-I takes certain iterations to produce the feedback clock Clk_fd using TDC1 in loop1 path and so local Clk_fdl is generated using 2-bit Vernier TDC1. In Figure 5.8, two TDC's TDC1 are used. The vernier 4-bit TDC1 is used for a in loop1 for generating an error e1 which is given to digital filter. Other 2-bit TDC1 used to produce a local feedback signal Clk_fdl in calibration block. Once the calibration is done, the signal En_TDC2 is generated by calibration

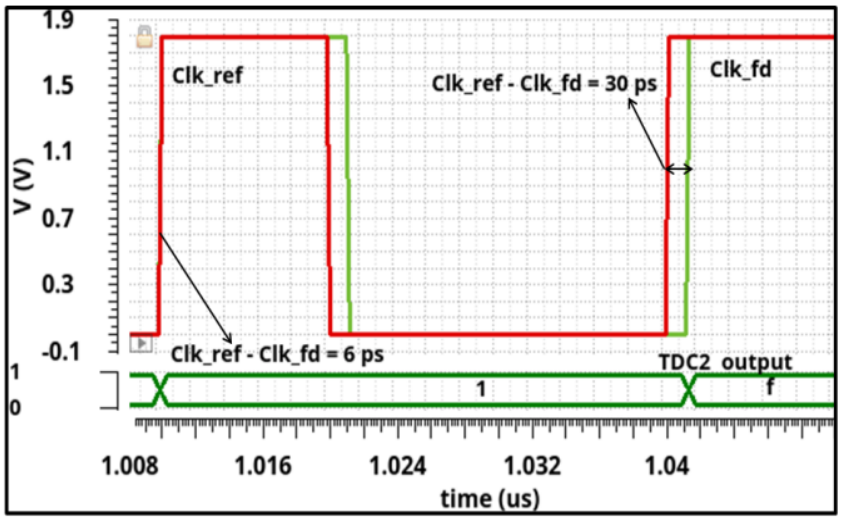
block which is used to switch between two TDC's. When the phase difference comes within the range of TDC2 and signal En_TDC2 becomes '1', an ADPLL-I switches to loop2 in which TDC2 comes in to picture. FSM detects the phase difference between Clk_ref and Clk_fd up to 30 ps and once the phase difference of 30 ps is achieved, FSM sends signal En_TDC2 to logic '1'. When the signal En_TDC2 becomes '1', ADPLL-I switches to loop2. The TDC2 will traverse the phase error till 1–bit resolution and ADPLL-I get locked with periodic jitter within 1% tolerance band of output frequency. Fig. 5.9 (a) shows output of TDC1 and TDC2 and their switching at 820 ns when signal En_TDC2 gets into logic '1'. It is observed from the simulations in the Fig. 5.9 (a) that as soon as the output of TDC1 becomes constant and the phase difference between Clk_ref and Clk_fd is 30 ps, the FSM is used to activate the signal En_TDC2 which switches ADPLL-I to TDC2. Fig. 5.9 (b) shows the outputs for TDC1 while the ADPLL-I design is in locking process. As evident, output of TDC1 becomes constant after 15 clock cycles. It is also noted from this figure that range of TDC1 is 300 ps for 4 bits and delay difference between Clk_ref and Clk_fd is more than range of TDC2 *i.e.* 30 ps. Fig. 5.9 (c) shows the output of TDC2 after calibration phase is over and ADPLL-I gets locked at 1 µs and dynamic range is 30 ps. The output for minimum input difference of 6 ps is '1h' and maximum input difference of 30 ps is 'Fh'. This dual loop architecture reduces the locking time while improving the periodic jitter with lower power consumption. The error signals (e1 and e2) are generated by TDC1 and TDC2 respectively. The outputs of TDC1 and TDC2 are given to digital loop filter. The digital loop filter consists of two paths with input errors from TDC1 and TDC2. Path with TDC1 has traditional PI filter.



(a)



(b)



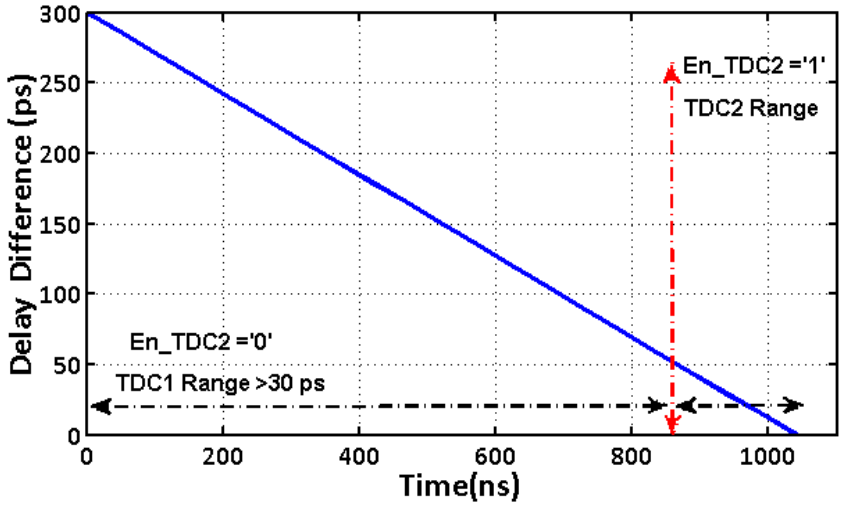
(c)

Fig. 5.9 (a) Output of TDC1 and TDC2 during ADPLL-I working in locking process, (b) Output of TDC1, (c) Output of TDC2

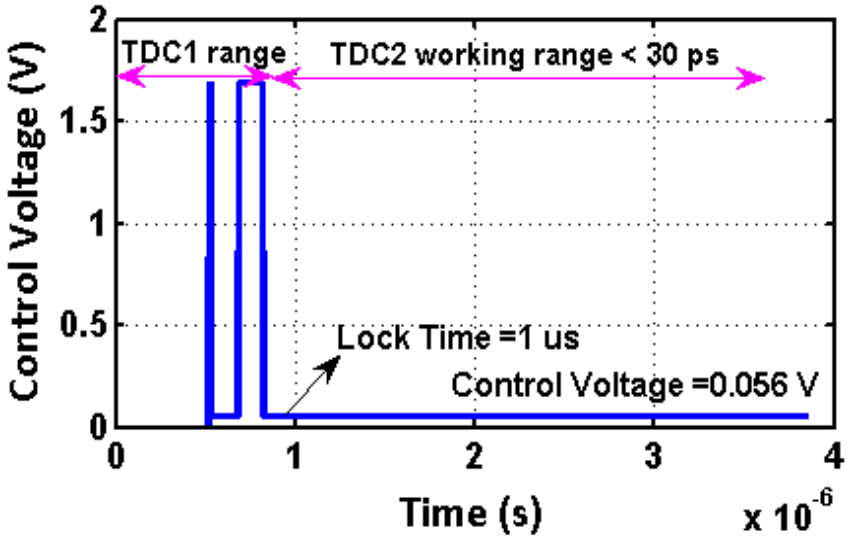
For TDC2, only integral path is required as TDC1 has already locked the ADPLL-I during the working of loop1. A control word (fcw) is generated after the addition of bits from these two paths. TDC1 provides a wide range of 300 ps with resolution of 30 ps and takes 15 clocks to produce the error resolution e1 [3:0] within the range of TDC2. Due to dual loop architecture and proposed flash TDC2, the fast settling time of 1 µs is obtained while maintaining periodic jitter of 6.6 ps as compared to existing designs. The frequency drift in output frequency of ADPLL-I is observed due to truncation error and quantization noise on account of the limited bit-width of digital loop filter and DAC. Further, the noise from the divider circuit also contributes to frequency drift in the output frequency of ADPLL-I. A frequency drift of 1% @1.6 GHz in the output frequency is observed when the reference input signal is fixed.

5.10 Simulation Results of ADPLL-I

ADPLL-I is designed with 1.8 V supply voltage in SCL 180nm CMOS technology. This ADPLL generates the frequencies of 1600 MHz, 400 MHz, 100 MHz, and 25 MHz. Fig. 5.10 (a) shows a working range of TDC1 and TDC2 with respect to delay difference between the Clk_ref and Clk_fd.



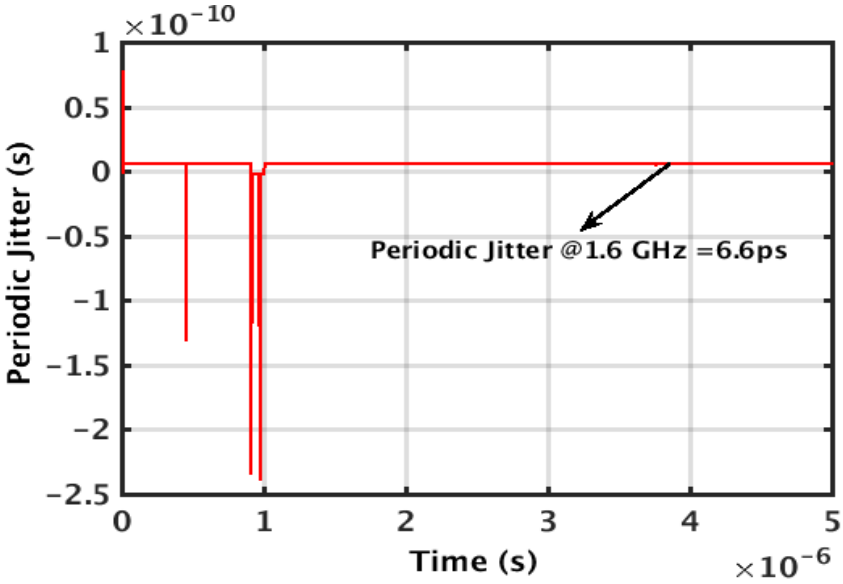
(a)



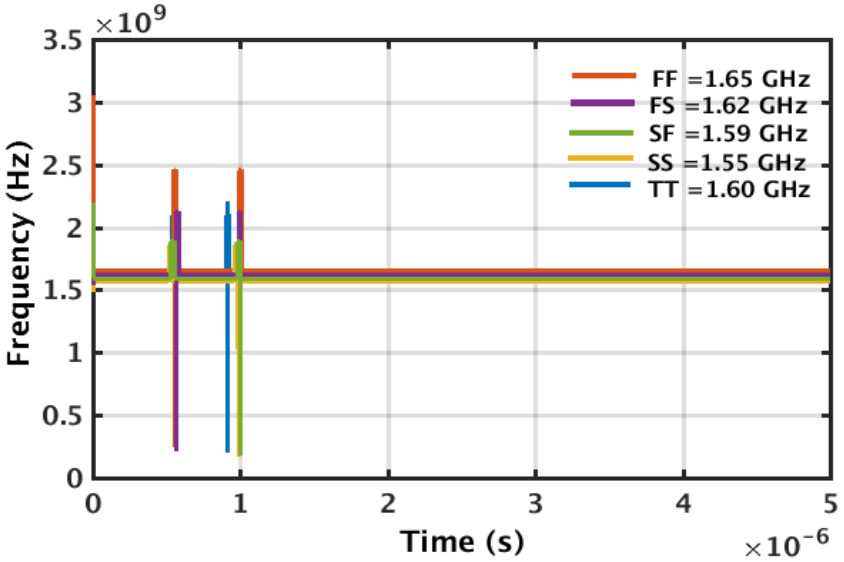
(b)

Fig. 5.10 (a) Graphical representation of delay difference with respect to time, (b) DAC output

Fig. 5.10 (b) shows the output of DAC which settles at 56 mV and locking time of ADPLL-I. The periodic jitter is 6.6 ps at 1.6 GHz as shown in the Fig. 5.11 (a). The variation in output frequency of ADPLL-I at 1.6 GHz after calibration for different PVT corners is shown in the Fig. 5.11 (b). It observed that maximum variation of 3.1% in output frequency at SS corner with respect to TT corner. Since the conventional Vernier TDC's consumes a lot of power owing to its requirement of a greater number of delay elements and D-flip-flops.



(a)



(b)

Fig. 5.11 (a) Periodic jitter of ADPLL-I, (b) PVT variation at output frequency of 1.6 GHz- with calibration

This increases overall budget of power for the ADPLL-I, the proposed 4-bit flash TDC2 consumes only 0.39 mV. Since only one TDC works at time, it consumes the low power. Remaining power is consumed by other parts of ADPLL-I. The power consumed by VCO-I and TDC1 is 1.4 and 1.2 mW respectively. The digital filter, dividers, and calibration unit consumes a power of 3.3 mW. The maximum power is consumed by TDC1 and VCO-I. The fine gain of 230 kHz/mV for proposed VCO. Such low gain of VCO is sufficient to suppresses an any non-linearity introduced due to DAC block of proposed architecture and therefore, any noise from the DAC will not impact the phase noise of VCO and keeps the variations within 0.1% of output frequency. Table 5.2 shows the periodic jitter variation across different PVT corners. It is observed that maximum variation in the periodic jitter is 3% around the SS corner

with respect to TT corner. The proposed ADPLL-I is locked at 25 clock cycles of reference frequency. The frequency spacing is 25 MHz for ADPLL-I.

Table 5.2: Periodic jitter of ADPLL-I at different PVT corners

PVT Corners	Periodic Jitter (ps) @ (1.6 GHz)
TT	6.6
FF	6.7
SS	6.3
FS	6.5
SF	6.4

Table 5.3: Shows performance parameters of ADPLL-I

Parameters	This work
Supply Voltage (V)	1.8
Output Frequency (GHz)	1.6
Resolution (ps)	6
Periodic Jitter (ps)	6.6
Locking Time (μs)	1
Power Consumption (mW)	6.35
Technology Process (nm)	180
Reference Frequency (MHz)	25
Frequency Spacing (MHz)	25
Division Ratio	64

Table 5.3 shows the achieved parameters of proposed ADPLL-I architecture. The proposed ADPLL-I with 4-bit flash TDC2 and low phase noise VCO-I shows the lower periodic jitter and improved locking time.

5.11 Conclusion

Chapter 5 shows the simulation results and discussion for the proposed ADPLL-I design. An ADPLL-I is designed with simple and high resolution 4-bit flash TDC2. Further to improve the phase noise performance, gate method-logy based low phase noise and low power VCO-I is used. Vernier based 4-bit TDC1 provides a dynamic range and helps to get fast locking of ADPLL-I. A LMS based calibration is used to obtain the enhanced periodic jitter of 4-bit flash

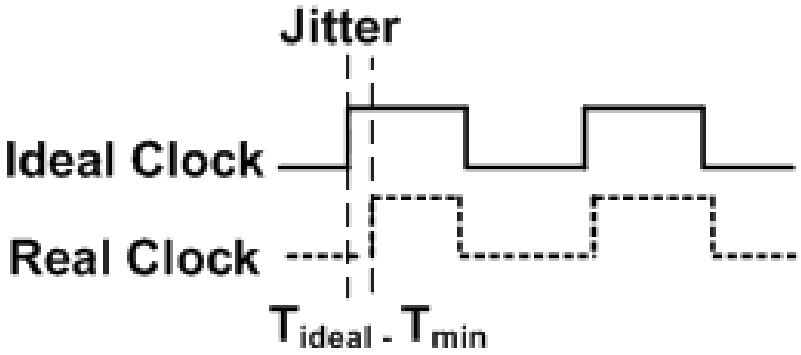
TDC2 which makes ADPLL-I PVT variations robust. The use charge pump and MOS based filter in digital phase locked loop DPLL-II, degrades the phase noise and PVT variations. TDC and VCO are main blocks which degrades the PVT variations in the ADPLL architectures. In ADPLL-I, PVT variations are improved due to use of 4-bit flash TDC1 with high resolution of 6 ps. Also, the calibration used in the proposed TDC2 suppresses any PVT variation in the TDC2 which overall improves the PVT variations in ADPLL-I design. The same oscillator is used in ADPLL designs. The periodic jitter of ADPLL-I is 6.6 ps with locking time of 1 μs and power consumption of 6.35 mW. Owing to the dual architecture, this ADPLL-I design is fast and can be used for low power SoC applications. The following chapter provides the details of simulation results and analysis for ADPLL-II design. The ADPLL-II is designed for wireless transceiver applications.

CHAPT ER 6

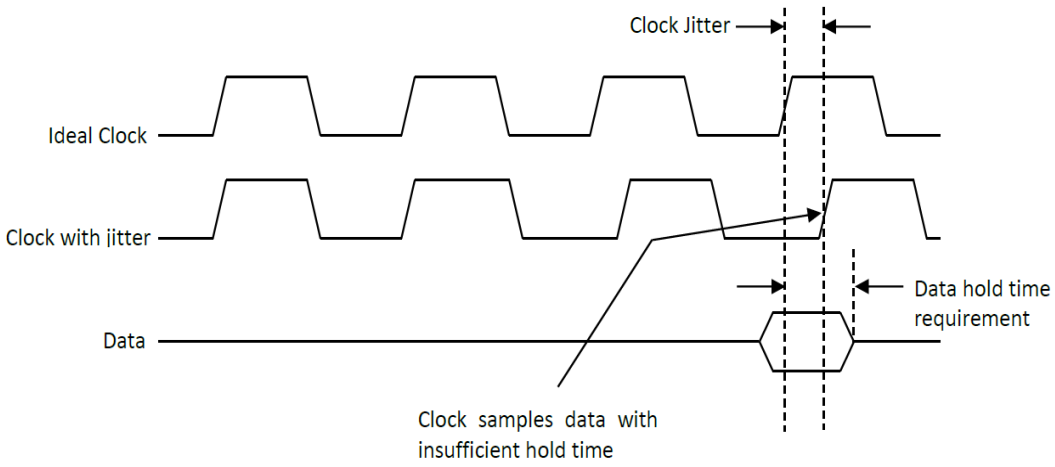
DESIGN AND ANALYSIS OF LOW JITTER ALL DIGITAL PHASE LOCKED LOOP

6.1 Introduction to Low Jitter ADPLL Design

The chapter 6 explains a low jitter ADPLL for wireless transceiver applications [4-5]. The jitter is defined measure of deviation of the ADPLL's actual clock output compared to ideal clock. There are extrinsic and intrinsic sources of jitter. Intrinsic sources of jitter occur from the current and voltage noise sources of the devices used in the different ADPLL components. Other than intrinsic sources of jitter, ADPLLs experience various kinds of external noise like –supply noise, quantization noise from DCO and TDC which contribute to the jitter of ADPLLs. Extrinsic noise sources of jitter like supply and substrate bounces and also noise from the reference crystal also affects the jitter of ADPLL [97]. Phase noise from VCOs and input reference sources also contribute to total noise which worsens the jitter budget of ADPLL. There are various kinds of jitter- periodic jitter, cycle-to-cycle jitter, and long term which affect the performance of an ADPLL. The periodic jitter is the deviation in output clock period compared to the average clock period of ideal clock source as shown in the Fig. 6.1 (a) [97]. The periodic jitter mainly affects the setup and hold time constraints in the digital system [98]. Fig. 6.1 (b) shows the effect of periodic jitter on the hold time [98]. The analysis of periodic jitter is important in digital circuits and SoCs. In these applications, time margins are very constrained. The clock jitter severely affects the SNR of ADCs thus needs to be reduced [99]. The RMS jitter defines maximum standard deviation of periodic jitter over 10000 clock cycles [98].



(a)



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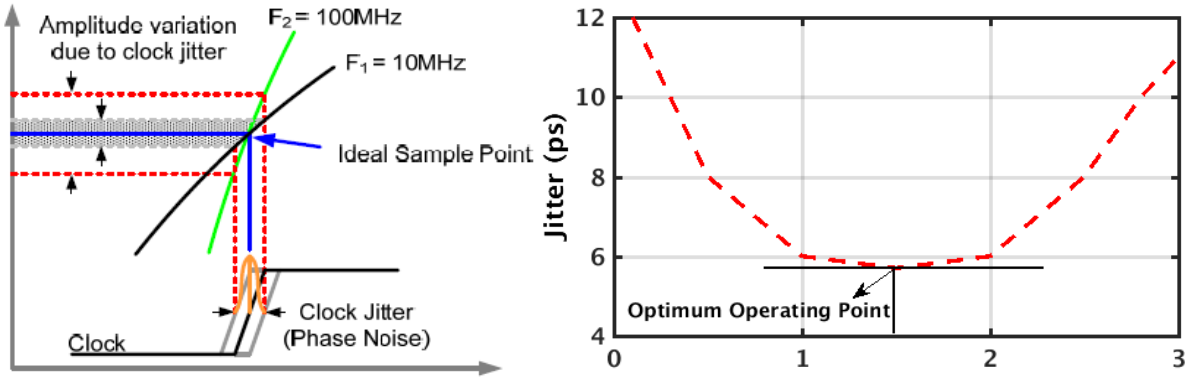


(c) (d)

Fig. 6.1 (a) Time jitter [97], (b) Periodic jitter, (c) Jitter variation with frequency [99], (d) Jitter optimization with loop bandwidth [45]

The peak-to-peak jitter determines the maximum and minimum deviation in the clock periods. The relation between peak-to-peak jitter and RMS jitter is given as [97-99]:

$$\text{Peak-to-peak jitter} = \pm 3.179 \text{ RMS jitter} \tag{6.1}$$

The cycle-to-cycle jitter is considered as a peak value which gives the maximum deviation between the rising edges of any two successive clocks edges over 10000 clock cycles [98-100]. Fig. 6.1 (c) shows the variation of jitter with frequency. As the frequency increases, the jitter also increases. Also, the loop bandwidth of the ADPLL system impacts the jitter of ADPLL. The loop bandwidth is determined mainly by the parameters of loop filter. Fig. 6.1 (d) shows a curve for jitter optimization with loop bandwidth of ADPLL. A narrow loop bandwidth minimizes the impact of the jitter at the input on of reference source but narrow loop bandwidth bypasses the jitter introduced by the DCO. On other hand, wide loop bandwidth reduces the jitter of DCO but does not filter the jitter introduced by the in-band noise sources such as crystal

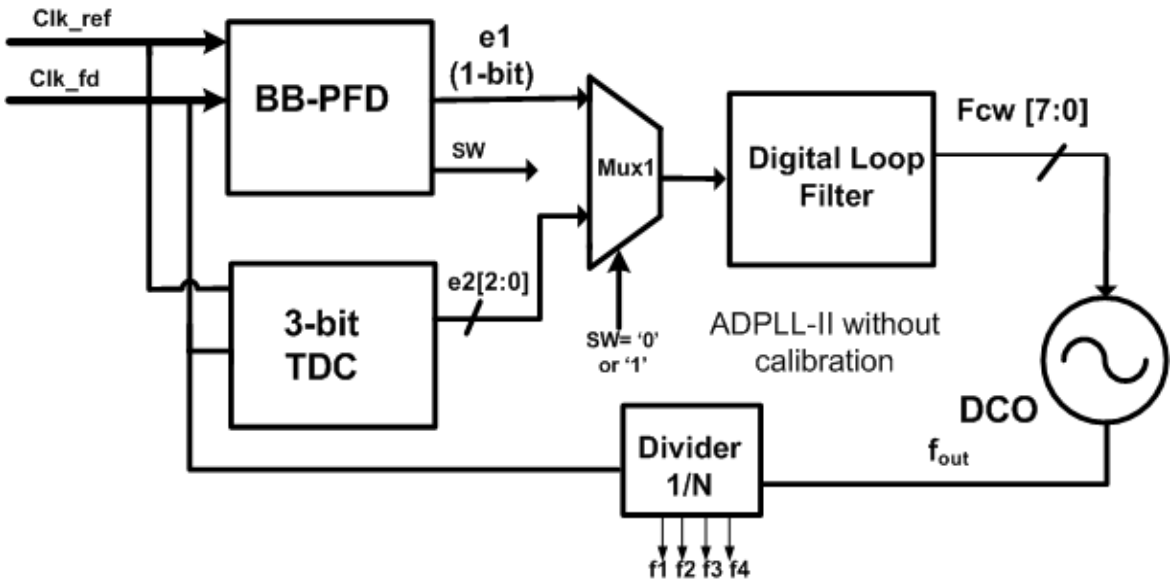
oscillator, PFD, and loop filter [61-62]. Therefore, an optimized loop bandwidth is required to have a reduced jitter of the ADPLL.

6.2 Problems with ADPLL-II Design and need of calibration for ADPLL-II

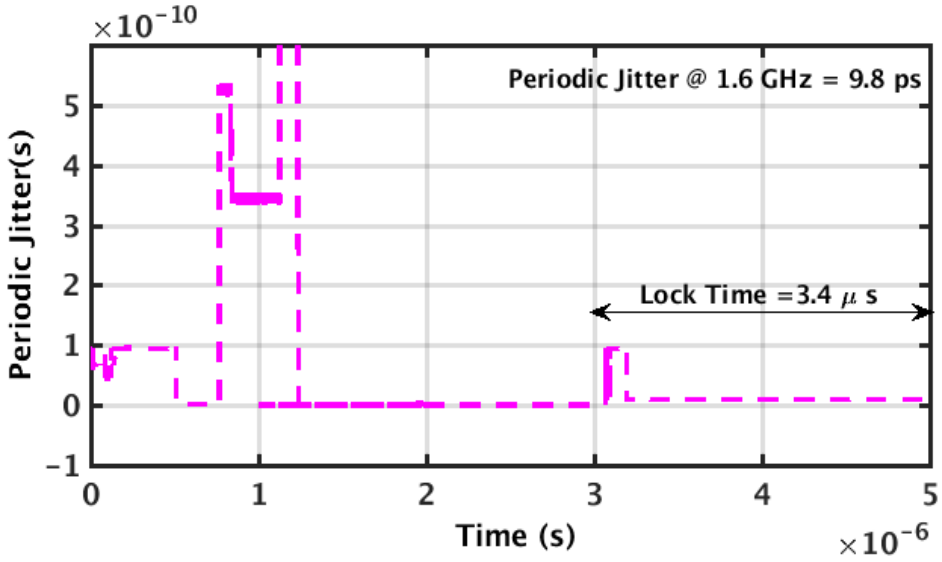
The proposed ADPLL-I architecture shows an improved performance parameters as compared to the many recent existing works [64-66]. The proposed ADPLL-I architecture provides the periodic jitter of 6.6 ps at an output frequency of 1.6 GHz and power consumption of 6.35 mW. This owes to the low power, low jitter simple 4-bit flash TDC2 design and the proposed inverter based VCO-I. Further to enhance the performance parameters of ADPLL-I design for wireless transceiver applications, another version of ADPLL architecture is proposed. For wireless transceiver applications, ADPLL-II requires a target jitter of 2 ps [5]. The proposed ADPLL-II is designed using the 3-bit flash TDC without calibration which is shown in the Fig. 3.5, bang-bang PFD, DAC [29], and VCO-I as shown in the Fig. 6.2 (a). ADPLL-II works in two loops. The Clk_ref is given to the BB-PFD loop. The Clk_fd is generated after few clock cycles and it is given to BB-PFD. The signal Sw is generated by the BB-PFD. Once the phase difference reduces to TDC range, the signal Sw switches to TDC loop and it starts tracking phase difference between Clk_ref and Clk_fd. The output of BB-PFD and TDC2 is given to filter. The output of filter is given to DCO. The DCO generates a frequency of 1.6 GHz, when ADPLL-II is locked. The proposed ADPLL-II without calibration achieves a periodic jitter of 9.8 ps as shown in the Fig. 6.2 (b). It is observed from the graph that jitter is more as compared to designs reported in the literature [5, 65-66].

The ADPLL-II architecture is described in the detail in this chapter. ADPLL-II consists of proposed bang-bang phase frequency detector (BB-PFD) and the proposed 3-bit flash architecture based TDC with calibration to enhance the performance parameters like locking time and periodic jitter. The block level architecture of ADPLL-II with calibration is shown in the Fig. 6.2 (c). TDC is major block and its parameters such as resolution, quantization error and dynamic range significantly affects performance parameters of the ADPLL. The PVT variation in the TDC drastically degrades the jitter parameter of ADPLL. To obtain low power and low periodic jitter ADPLL-II, a calibration technique is used in proposed 3-bit flash TDC. Also, a high resolution and wide range TDC is essential to design a low periodic jitter and a wide range an ADPLL. However, designing a wide dynamic range and high resolution TDC is challenge and generally consume more area and power [73-74]. In this work, a BB-PFD is utilized along with proposed high resolution TDC to achieve fast locking, low jitter, and wide range ADPLL. The ADPLL-II works in the two loops –BB-PFD and TDC loop. Initially, the Clk_ref is given to BB-PFD loop. Clk_fd is generated by the ADPLL-II and BB-PFD tracks a

phase difference between Clk_ref and Clk_fd. During the locking process, typically an ADPLL has a phase difference in range of few nano-seconds between reference clock and feedback clock [8, 12, 48, 96]. BB-PFD brings the frequency of feedback clock Clk_ref close to reference clock and reduces phase difference to few hundred pico-secs from range of nano-seconds. Even though, BB-PFD has benefit of low area and power but it suffers from the long settling time and degrades the output jitter in ADPLL [62]. Hybrid architecture of ADPLL employing both a BB-PFD and proposed 3-bit TDC which utilizes advantage of both BB-PFD and high resolution TDC and also tackle the above said issues of ADPLL thus obtains the target specifications of ADPLL-II.



(a)



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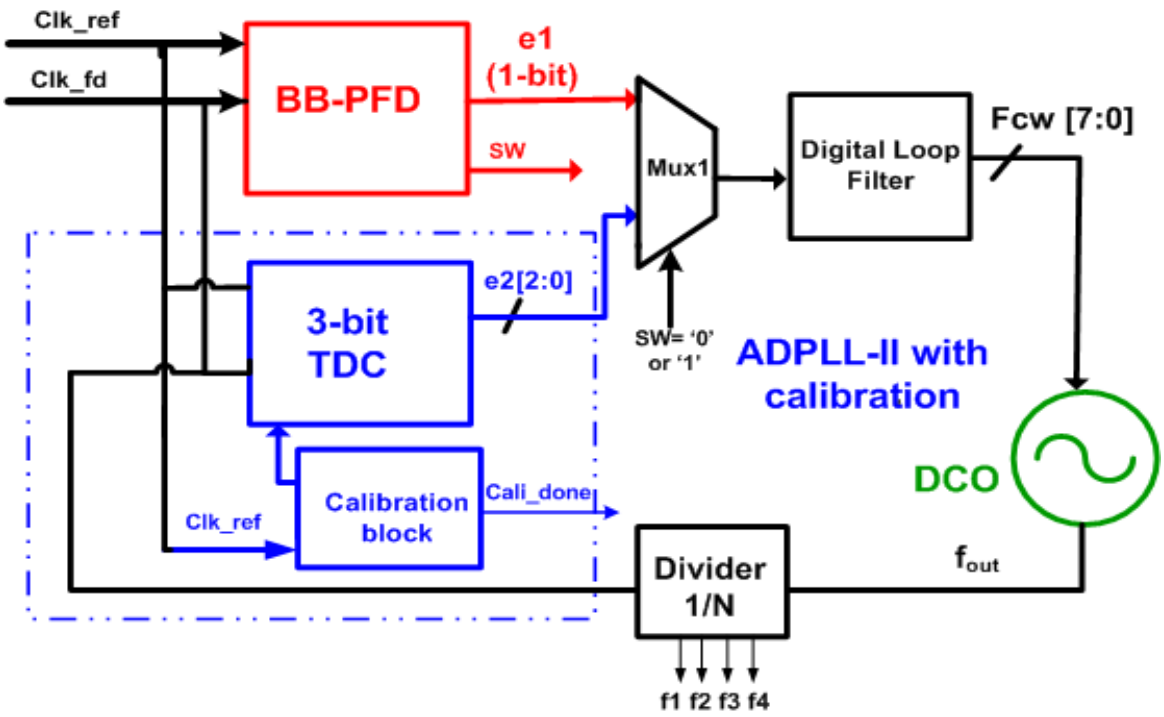


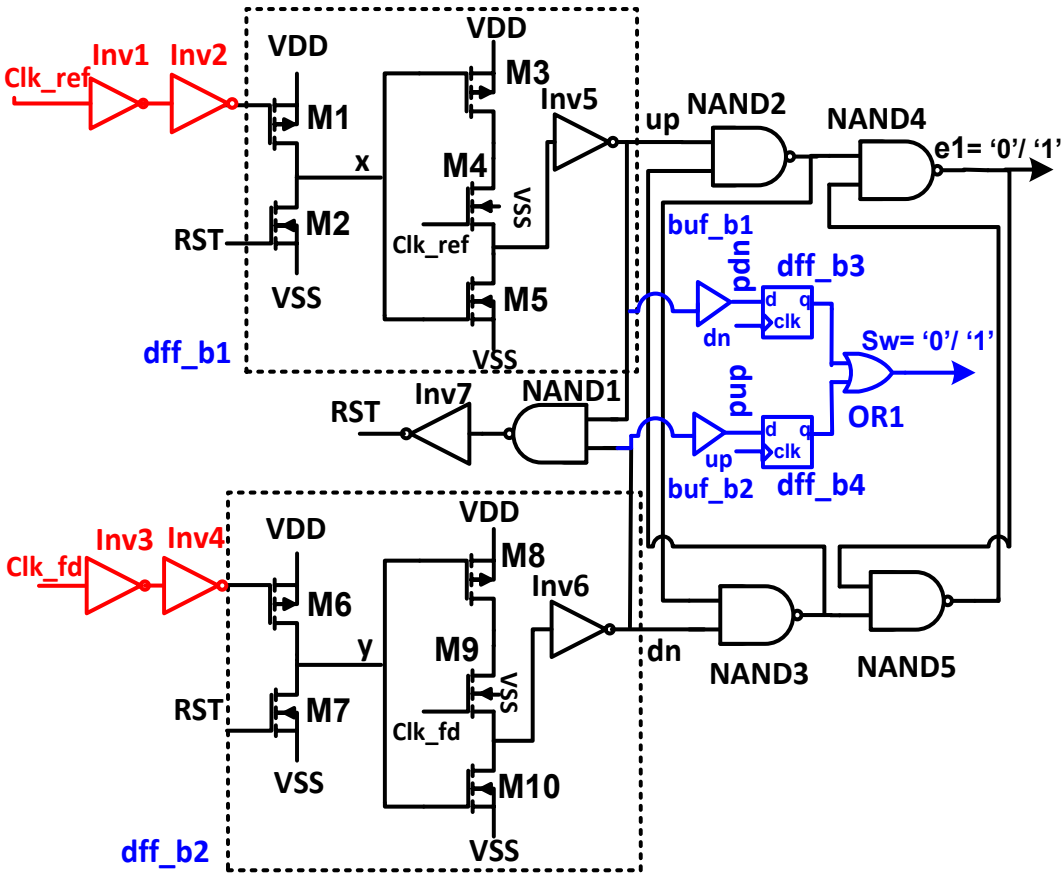
(c)

Fig. 6.2 (a) ADPLL-II -without calibration, (b) Periodic jitter of proposed ADPLL-II-without calibration, (c) Proposed block level design of ADPLL-II

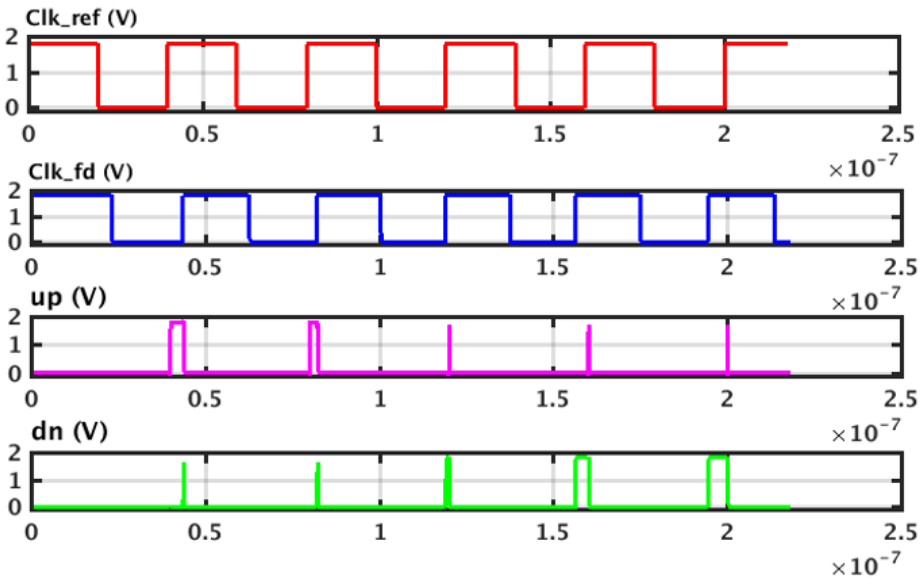
The switching between two loops is done using Sw signal. The signal Sw is generated by the BB-PFD and at the start, it is at logic '1'. When the phase difference between two clocks reduces and comes to the range of TDC, Sw becomes '0' and switches to TDC loop. The error signal e1 and e2 is given to the digital filter. The output of filter generates a code word Fcw [7:0] which is given to the DCO. The output of DLF is given to 8-bit DAC which changes the frequency of VCO-I. The following sections describe each block of ADPLL-II in detail.

6.3 Proposed Bang-Bang Phase Frequency Detector (BB-PFD)

BB-PFD suffers from issues such as blind and dead zone [76-77]. In BB-PFD designs, the blind zone is design problem which needs to be addressed. Conventionally, the D-flip-flop's (DFF's) used in the BB-PFD's, are complex and thus they suffer from the slow speed in BB-PFD and limits the performance of BB-PFD's at higher frequency range [62, 92]. The BB-PFD compares the rising edges of the reference clock and feedback clock and generates binary phase-error output. If the reference clock is ahead of the feedback clock, BB-PFD gives a logic '1' and on other hand, if the reference clock comes after the feedback clock, logic '0' is generated by the proposed BB-PFD. Fig. 6.3(a) shows the proposed BB-PFD. The BB-PFD has NAND, OR gates, and high-speed resettable DFF's with supplementary circuitry which generates the signal Sw and delay del_{Sw}. The output of up and dn pulses in the modified BB-PFD is shown in the Fig. 6.3 (b).



(a)



(b)

Fig. 6.3(a) Proposed BB-PFD design, (b) up and dn pulse output

The signal Sw is generated by D-flip-flops dff_b3, dff_b4, OR1 gate, and buffer buf_b1 and buf_b2. The del_{Sw} is delay provided by the additional buffers buf_b1 and buf_b2. When the delay difference between the clocks Clk_ref and Clk_fd is more than del_{Sw}, the flag Sw is at

logic ‘1’ and on other hand, if delay difference lower than del_{Sw}, the flag Sw is at logic ‘0’. When delay difference between the clocks Clk_ref and Clk_fd higher than the delay of buf_b1, then at rising edge of dn pulse, dff_b3 samples and gives the logic ‘1’ and on other hand when delay difference between the clocks Clk_ref and Clk_fd becomes lower than delay of buf_b1, then the output is at logic ‘0’at output of dff_b3. Similarly, dff_b4 samples rising edge of up pulse and if the delay del_{Sw} of buf_b2 is more than the delay difference of Clk_ref and Clk_fd gives logic ‘1’at output. On other hand, if delay del_{Sw} is lower, the logic ‘0’ is obtained at the output. Consequently, the flag Sw signal becomes logic ‘1’/ ‘0’ according to outputs of dff_b3 and dff_b4 after they are given to gate OR1. The issue of blind zone occurs in the proposed BB-PFD when the rising edge of clock Clk_ref comes earlier to the falling edge of the pulse ‘reset’ [76-77].

The width of up and down (dn) signal’s [9-10] affects the width of reset pulse. If the width of reset pulse is too narrow, it creates the dead zone issue in the BB-PFD. Therefore, to tackle dead zone issue, the wide up and dn pulses are necessary. But widening of widths of up and dn pulses degrades the locking time of ADPLL and makes it slow. The proposed dynamic logic-based BB-PFD design in this work solves these problems. It consists of a D-flip-flop dff_b1 made of (M1-M5 and inverter Inv5) in upper part, and similarly (M6-M10 and inverter Inv6) makes the D-flip-flop dff_b2 in the lower part. The node x and y as shown in Fig. 6.3 are pre-charged by providing additional delay at the inputs of transistor M1 and M6 which will contain the problem of blind zone. τ_{p_ch} is the charging time for the nodes x or y to reach up to VDD and less than the delay τ_{i1} (provided by Inv1 and Inv2) and similarly τ_{i2} (provided by Inv3 and Inv4). As a result, the total delay contributed by the NAND1 gate, inverter Inv7 and dff_b1 makes the RST pulse width wide enough to avoid the occurrence of blind zone. As simple and high-speed D-flip-flop dff_b1 is used, here RST pulse width is sufficiently narrower to avoid the chances of occurrence of rising edge of the Clk_ref with the RST pulse being at logic ‘1’.

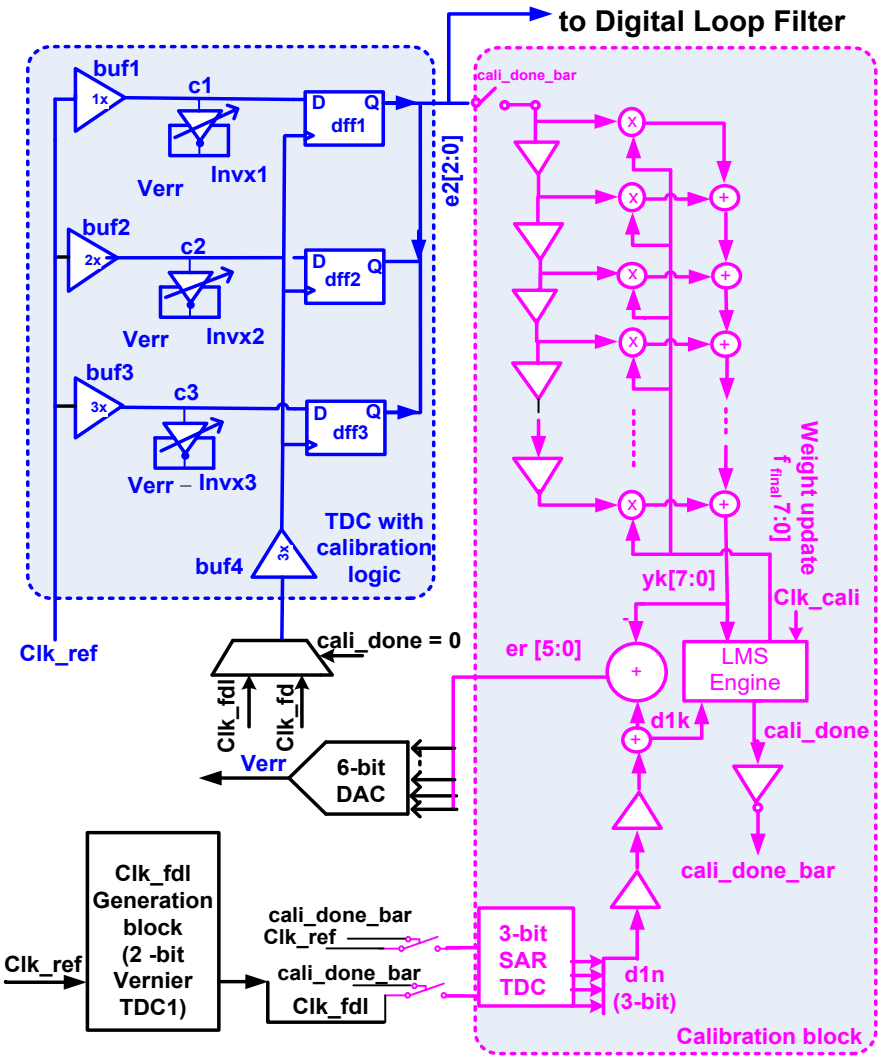
Table 6.1: Relative comparison of conventional and proposed BB-PFD

Parameter	Conventional [62]	Proposed
Speed (ns)	1.2	0.5
Design Style	Logic gate based	Dynamic Logic based
Error Range	(-2π to2 π)	(-π to π)
Detection Range	Unlimited	Limited
Reset Path	Yes	yes

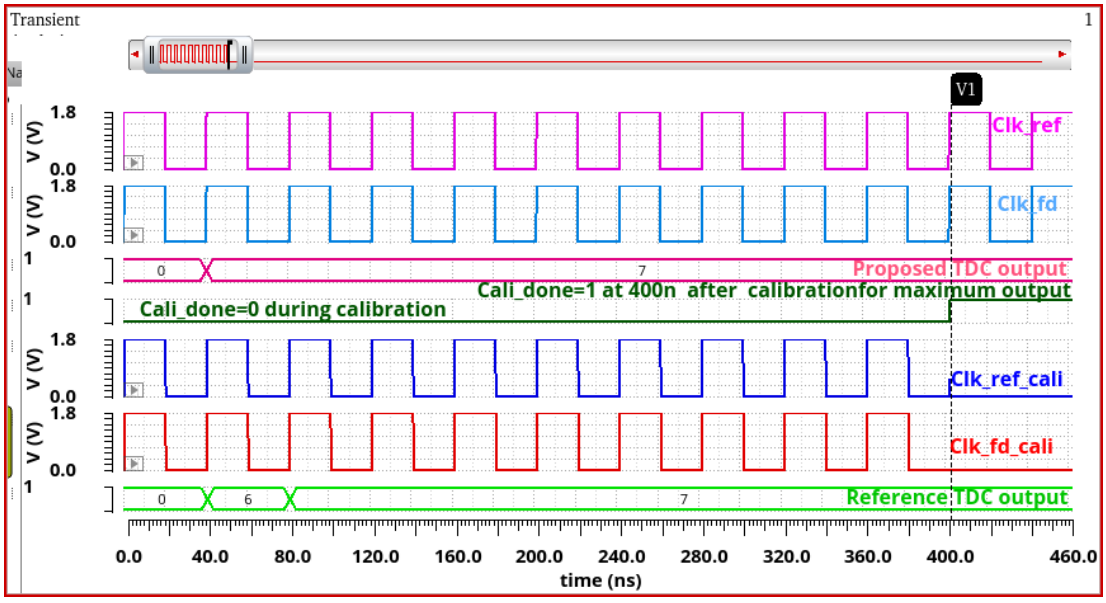
Similar argument is applicable to the lower portion of circuit also. When the clock Clk_ref and Clk_fd are in phase and accordingly up and dn pulses are at logic '1', the reset pulse activates MOSes M2 and M7 and thus discharges the up and dn to logic '0'. Table 6.1 shows a comparison between the conventional BB-PFD [62] and proposed BB-PFD. A conventional BB-PFD has lower speed of 1.2 ns as compared to the proposed BB-PFD which has a higher speed of 0.5 ns due to its shorter critical path delay. The conventional BB-PFD detects the phase error from -2π to 2π [9, 62] whereas the proposed design has range from -π to π due to its simple dynamic logic style. However, this limited range in the proposed BB-PFD does not affect the performance of ADPLL-II as the bandwidth of loop filter is optimized to reject the phase difference that lies outside range of -π to π. Though proposed BB-PFD provides a wide range but to achieve the low periodic jitter and fast locking ADPLL, the high resolution TDC in sub picoseconds range is required. The next section explains a 3 –bit flash TDC with calibration.

6.4 3-bit Flash TDC with Calibration

A 3-bit flash TDC described in section 3.4 achieves a periodic jitter of 0.46 ps and resolution of 3 ps which is not sufficient to meet the target specifications of ADPLL-II. As discussed earlier, the TDC suffers from PVT variations which degrades it noise thus requires a calibration. Consequently, calibration algorithms [93] are used in the proposed 3-bit flash TDC in this work (as shown in Fig. 6.4 (a)). The calibration unit will retain the enhanced jitter and high resolution during PVT variations. Here SAR TDC [75] is used for calibration because SAR TDC has lower delay elements as compared to other state of art designs like inverter delay line and Vernier TDC [73-74] and it also reduces the power and area of overall proposed 3-bit flash TDC. To start the calibration unit as shown in the Fig.6.4 (a), external clock signal Clk_cali of period of 20 ns is provided to the calibration block and during this time Cali_done and Cali_done_bar signals are '0'/ '1'. The output of 3-bit flash TDC *i.e.* e2 [2:0] is in reset mode. The finite impulse response (FIR) filter's [18-19] weights $f_{initial}$ [7:0] are initially assigned with value as '1'. When the calibration process ends, clock Clk_cali goes to reset state and signal Cali_done is at logic '1'. The length of FIR filter is taken as 11 to achieve low power and low design complexity. The error e2 [2:0] becomes 8-bit by padding zero's in residual MSB's for calibration process. The equation (5.2) defines the output of FIR filter. The adaptive LMS algorithm [93] is used to obtain error (Verr) roughly near to zero value (between reference input d1n [2:0] and actual input e2 [2:0]), by updating the weights of FIR filter.



(a)



(b)

Fig. 6.4 (a) Proposed 3-bit TDC with calibration, (b) Output of reference and proposed 3-bit flash TDC in calibration process

The intermediate outputs d1k [7:0] and yk [7:0] are given to calibration block which update the output f_{final}[7:0] according to equation (5.2), (5.3) and (5.4). The output of reference SAR TDC is shown in the Fig. 6.4 (b). The step size is taken as 1 to avoid design complexity. The resolution of proposed 3-bit flash TDC shown in the Fig.6.4 (a) *i.e.* $\Delta\tau$ is difference between delay of successive delay cells in upper and lower sections and it is represented as $\Delta\tau = \tau_i - \tau_{i-1}$ where τ_i is the delay of i^{th} buffer and i belongs to (1-3). The resolution $\Delta\tau$ is taken as 3 ps in 3-bit TDC design which is sufficient to achieve periodic jitter budget. The output of 6 -bit DAC is provided to Inverter-caps which fix the capacitance values of buffers (buf1-buf3). The capacitance offered by inverter cap ($C_{Invx,i}$ and i ∈3) is due its input gate terminal as shown in Fig. 4.5 (a).

The value of the capacitance s controlled with the error voltage (Verr) which fixes the delay of buffers (buf1-buf3). In the 4-bit flash TDC2, the MOSCAPs are used to fix delays of buffers as shown in the Fig. 6.4 (a). Since the Inverter-cap are more linear than the MOSCAP and provides the less variation in the capacitance, therefore, the 3-bit flash TDC with improved jitter and less variation in PVT is obtained. This method stabilizes the delay of buffers (buf1-buf3) by fixing the capacitance value in the Inverter-cap during PVT variations. The parallel combination of PMOS and NMOS in Inverter–cap reduces the capacitance variation for the same voltage variation (Vgc) from 0 V to 1.8 V for MOSCAP. The capacitance of MOSCAP varies enormously over different regions of operation as shown in the Fig. 4.6 (a) and thus it degrades periodic jitter of TDC designs. The Verr is voltage across inverter caps nodes $C_{Invx,i}$ (where i =1 to 3 and ∈ N) and capacitance value offered by $C_{Invx,i}$ is in range (3-5) pico-farads. The value of width W and length L of PMOS and NMOS in Inverter-cap are chosen as W = 1 μm and L =1 μm. The propagation delay of i^{th} buffer τ_i by [94]:

$$\tau_i = 2.\frac{\sqrt{C_{buf,i}+C_{Invx,i}}\,VDD}{\sqrt{C_{in,i}}}\left(\frac{1}{k_n\frac{W_i}{L_i}.(VDD-V_{tn})}+\frac{1}{k_p\frac{W_i}{L_i}.(VDD-V_{tp})}\right) \qquad (6.2)$$

where $C_{buf,i}$and $C_{invx,i}$ are the capacitances at the output and input of buf,i respectively. The $C_{Invx,i}$ is gate capacitance of Invx, i and the $C_{buf,i}$ is the inherent output capacitance of buf, i. W_i and L_i are width and length for buf, i. Fig. 6.4 (b) shows an output of reference SAR TDC and calibrated 3-bit flash TDC during and after calibration. It is observed that the output of reference and proposed TDC is at '7h', when the delay difference between Clk_ref and Clk_fd is 9 ps. The calibration unit takes 400 ns and signal Cali_done becomes logic '1' when

calibration is finished as shown in the Fig.6.4 (b). For proposed 3-bit flash TDC (as shown in Fig 6.4(a)), the calibration unit takes certain time to bring error to minimum value. The parameters achieved by 3-bit flash TDC are shown in the Table 6.2.

Table 6.2: Shows the achieved parameters of 3 -bit flash TDC

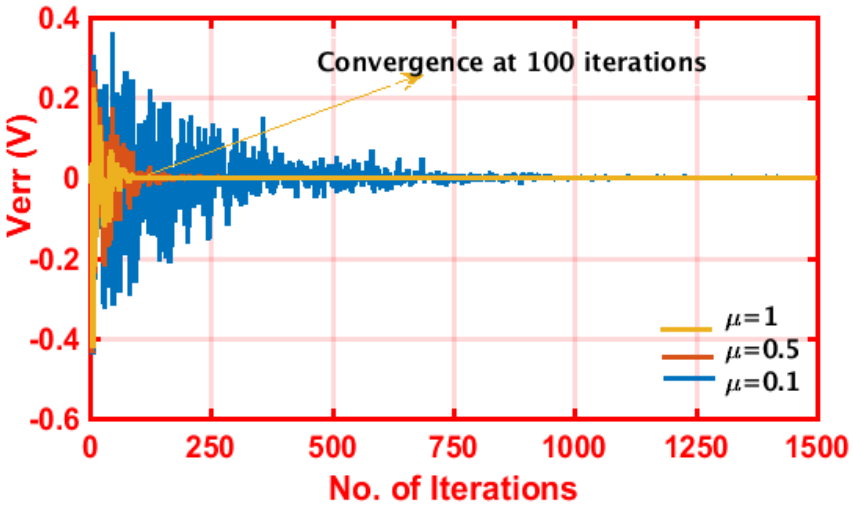
Parameters	3 –bit flash TDC
Delay elements	4
Conversion Time (cycle (s))	1 clock
DFF's	3
Periodic Jitter (ps)	0.152
Resolution (ps)	3

It is observed the proposed 3-bit flash TDC achieves a very low jitter of 0.152 ps and requires few delay elements. This is shown that the 3-bit flash TDC has better performance as compared other reported works [24, 26] and achieves the high resolution of 3 ps. The detail of LMS algorithm and SAR TDC is added on page no. 82 in section 5.4 The description for DAC is updated on page 85 in section 5.4 is added on the page.

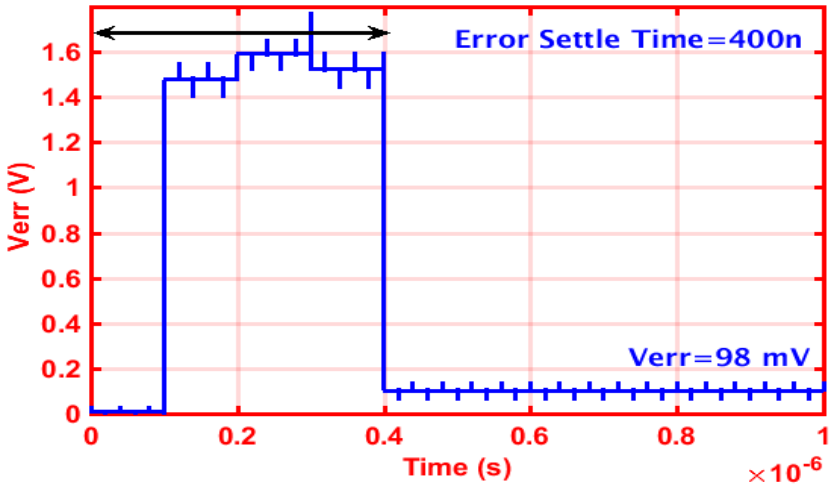
6.5 Simulation Results of 3-bit Flash TDC with Calibration

For the deviation of μ from 1 to 0.1, the number of iterations for minimal error rises from 100 to 1000 as shown in the Fig. 6.5 (a). As the value of μ is increased, the error estimation time is increased as a greater number of computations is involved in the process to bring error to minimum value. Fig. 6.5 (b) depicts the voltage (Verr) from the DAC output. It is fixed at 98 mV and corresponds to DAC input of '000001'after the calibration process is over. When the weights become stable and error signal has achieved the minimum value, lower 6 bits of signal er (er[5:0]) are provided to DAC input.

The analysis of periodic jitter of proposed 3-bit flash TDC with calibration across all the PVT corners is done to the show the variation in the periodic jitter. It is shown in Fig. 6.5 (c) that periodic jitter value after calibration is 0.152 ps. The PVT variation of 23% to 30 % is observed in 3-bit flash TDC without calibration shown in the Fig. 3.6 (b). With calibration, PVT variation is reduced to 8% to 17% for the extreme PVT corners. The variation is 3.2% only for proposed 3-bit flash TDC at SF and FS corner. The results of 3-bit flash TDC without calibration is shown in the chapter 3 section 3.5. The Fig. 3.6 (a) and Fig. 3.6 (b) shows a resolution of 3-bit flash TDC is 3 ps and periodic jitter is 0.46 ps. The total power consumption of 3-bit flash TDC is 0.35 mW.



(a)



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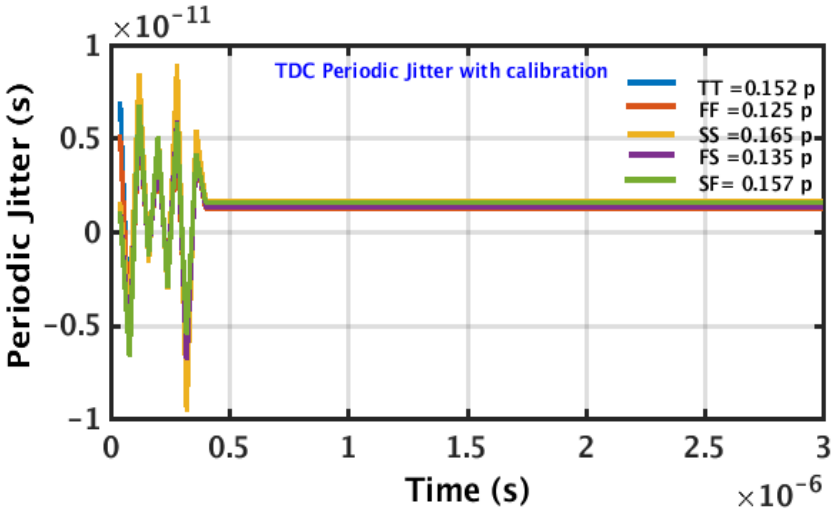


(c)

Fig. 6.5 (a). Variation of step size with number of iterations, (b) Error minimization after calibration process, (c) Periodic jitter of proposed TDC at PVT corners- with calibration

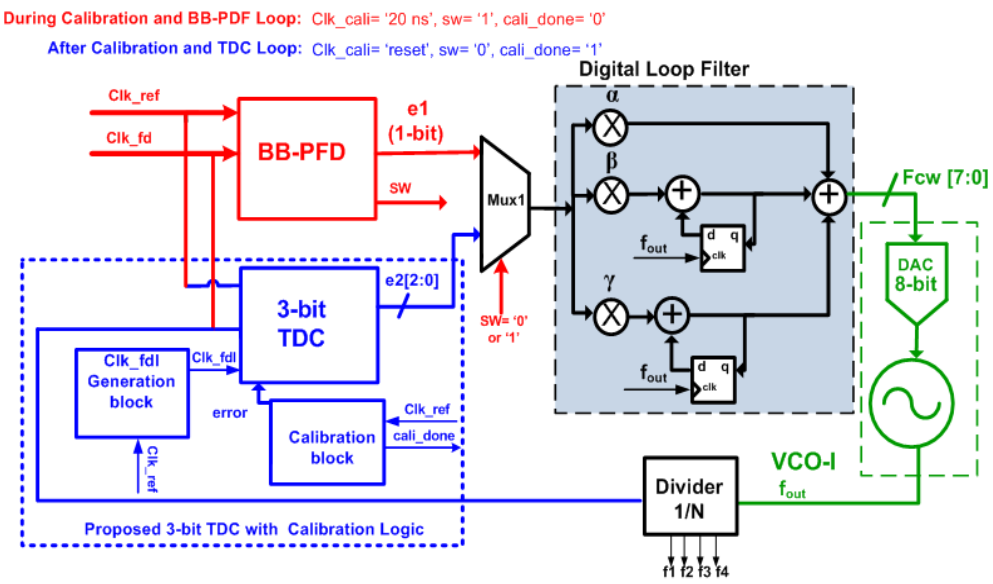
The proposed 3-bit flash TDC with calibration achieves a high resolution of 3 ps and periodic jitter of 0.152 ps which is suitable for designing the low periodic jitter ADPLL-II design.

6.6 Digital Loop Filter

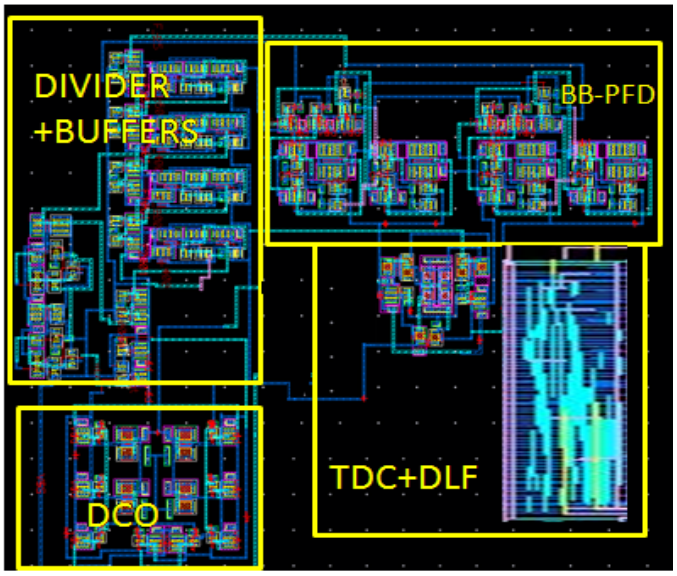
In ADPLL-II architecture as shown in the Fig. 6.2 (c), the outputs of BB-PFD and TDC are feed to the DLF. The digital loop filter is explained in the section 5.6 and is shown in the Fig. 5.5 (a). For stability during BB-PFD loop, the proportional integral filter works and produces control word Fcw to control the DCO frequency. Additionally, integral path is provided while ADPLL-II works in the proposed TDC loop. The switching between BB-PFD loop and TDC loop is done by the signal Sw as explained earlier in section 6.3 and section 6.4. The upper MSB's *i.e.* 8-bit of DLF are given to DAC. The frequency of DCO is varied by the output of DLF control word Fcw [7:0] which is output of DLF. Again, the values of coefficients of filter are chosen to have reduced jitter and fast locking time of ADPLL-II. For choosing an optimum value of α and β, the analysis proportional and integral gain with output periodic jitter is explained in the section 5.6. The values for filter coefficients α, β, and γ are chosen as 2^{-5}, 2^{-8}, and 2^{-8} respectively for working of ADPLL-II. The DCO for ADPLL-II architecture and its working of DCO is explained in the section 5.7.

6.7 Architecture of ADPLL-II

Fig. 6.6 (a) shows the proposed the hybrid and dual path ADPLL-II. The proposed 3-bit flash TDC, BB-PFD, a digital-to-analog converter (DAC), and VCO-I are the main blocks of proposed ADPLL-II. The foreground calibration is used to mitigate the problem of process, voltage, and temperature (PVT) spreads in the proposed 3- bit flash TDC as explained in the section 6.4. A proposed dynamic BB-PFD is also used which provides the fast settling process of ADPLL-II. Also, this ADPLL-II utilizes the gate based and reduced periodic jitter DCO which improves the phase noise and jitter of ADPLL-II. The layout of proposed ADPLL is shown in the Fig. 6.6 (b). Driven by the reference clock Clk_ref, initially ADPLL architecture takes certain cycles to produce feedback signal and also the reference and feedback signal has a phase difference in range of few nano-seconds while ADPLL is in the locking process [12, 48, 96]. Similarly, in proposed ADPLL-II design has phase difference between reference clock *i.e.* Clk_ref and feedback clock *i.e.* Clk_fd. The present research work proposes a 3-bit flash TDC which has higher resolution of 3 ps but suffers from limited dynamic range due to its flash based architecture. To overcome the issue of wide range issue of proposed flash TDC and to achieve wide range ADPLL-II, a proposed BB-PFD is employed with proposed high resolution 3-bit flash TDC.



(a)



(b)

Fig. 6.6 (a) Proposed ADPLL-II, (b) Layout of ADPLL-II

The hybrid architecture of ADPLL-II is implemented to have benefit of high resolution and fast settling TDC and wide dynamic range BB-PFD which achieves the target specifications of proposed ADPLL-II. The flowchart of calibration process is shown in the Fig. 6.7. At first, when the phase difference between clock Clk_ref and Clk_fd is huge in range of few nano-secs, an ADPLL-II starts working with BB-PFD which generates error signal of 1-bit. When the ADPLL-II is working in the BB-PFD loop, it takes few clock iterations which reduce the ADPLL-II's phase difference into few pico-secs range. The calibration block is also activated which calibrates the proposed 3-bit flash TDC while the BB-PFD is working and ADPLL-II is in acquisition process.

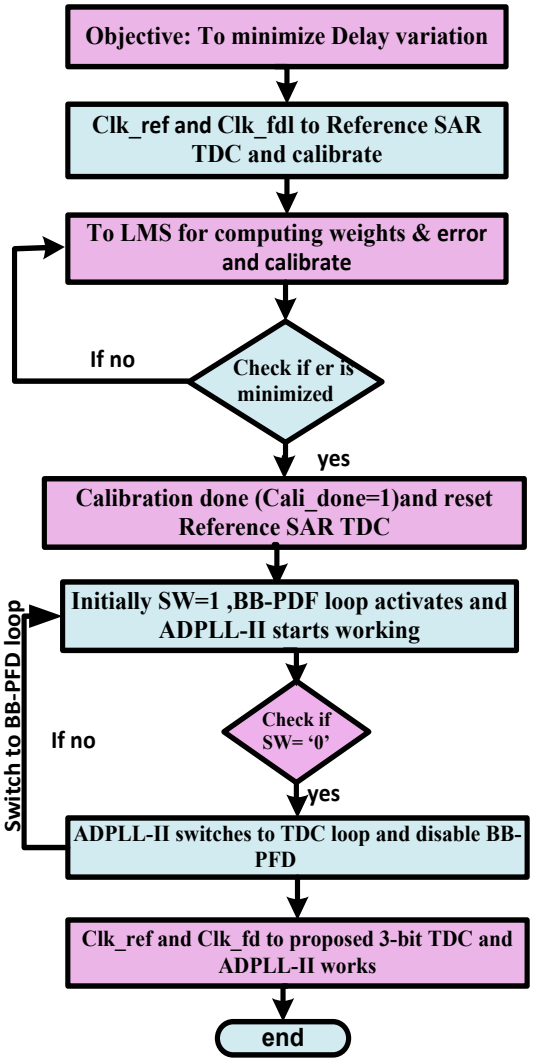
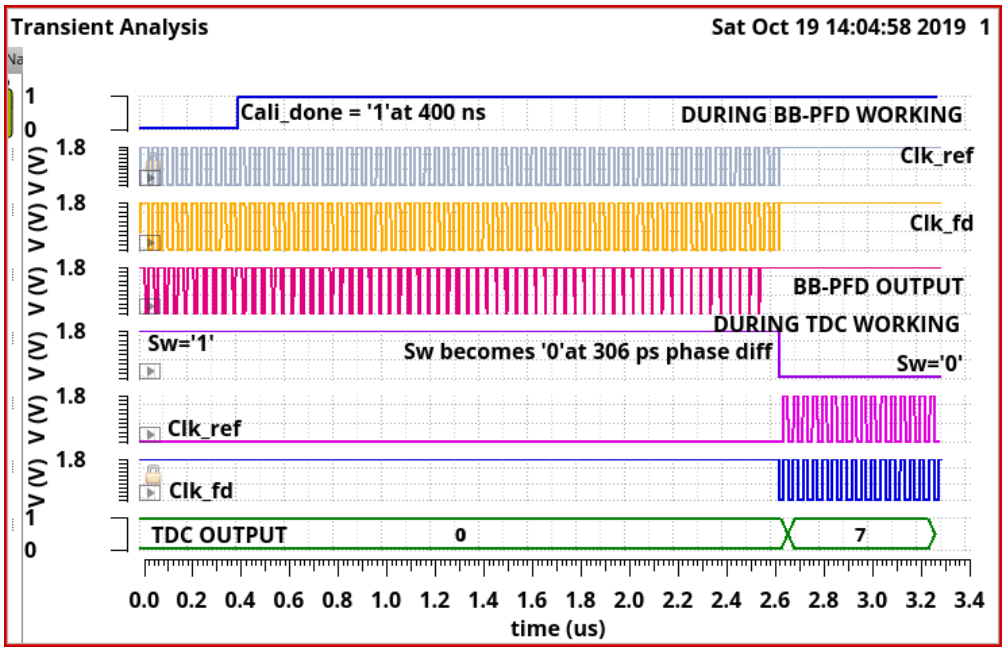


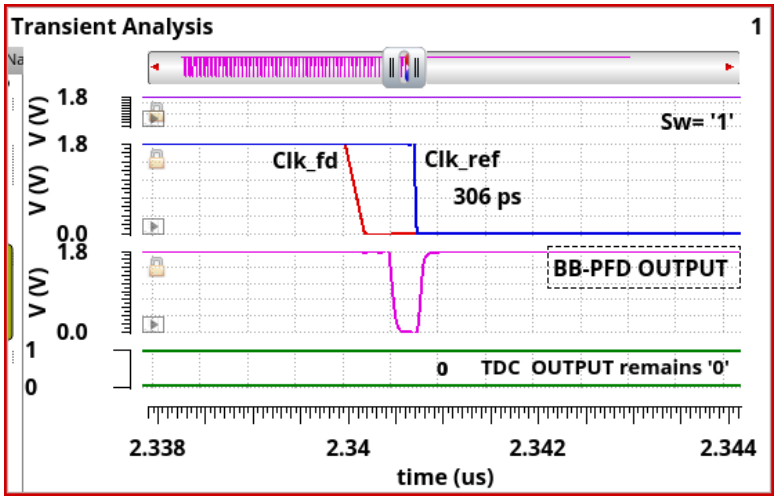
Fig. 6.7 Calibration process steps of TDC2 and ADPLL-II

The proposed BB-PFD also provides a signal (Sw) and acts as select signal of multiplexer (MUX1) which is used to switch between the BB-PFD loop and TDC loop. When the BB-PFD reduces phase difference between clock Clk_ref and Clk_fd to the range of proposed TDC *i.e.* 9 ps, the signal Sw becomes logic '0'. The error signals *i.e.* e1 and e2 which are generated by proposed BB-PFD and TDC respectively are given to the DLF. The frequency control word (Fcw) is provided to 8-bit DAC after the aggregation of bits from BB-PFD and TDC. The 8-bit DAC generates a control voltage and it is adequate to characterize the proposed ADPLL-II to achieve the periodic jitter of 2 ps. ADPLL being the feedback block takes certain clock iterations to generate the feedback clock Clk_fd. As a result, a local feedback clock *i.e.* Clk_fdl is required to start the calibration. The local feedback Clk_fdl is generated by providing reference clock Clk_ref to the upper section and with delay of 30 ps the lower section respectively of 2-bit Vernier TDC1 which is depicted in the Fig. 1.7 (a) (with n=2). The intrinsic delay of buffers utilized in the 2-bit Vernier TDC1 gives a delay difference of 30 ps.

The proposed 3-bit flash TDC has a dynamic range of 9 ps so minimum resolution of Vernier TDC should be 9 ps and dynamic range is 27 ps which is required to cover the dynamic range of proposed 3-bit flash TDC. Therefore, 30 ps is chosen as delay difference to produce Clk_fdl. The local feedback clock Clk_fdl is taken from output node of buffer buf_dn_2 in the Fig .1.7 (a) *i.e.* from Clk_2l node. Fig. 6.8 (a) shows the output of proposed BB-PFD and proposed TDC when the ADPLL-II is in the locking process. It is evident from the output of BB-PFD that when the phase difference lowers to picoseconds range, the signal Sw becomes '0'. As the Sw signal becomes logic '0', TDC loop starts to work. The proposed 3-bit flash TDC detects a phase difference of 3 ps between Clk_ref and Clk_fd. It corresponds to output '1H'.



(a)



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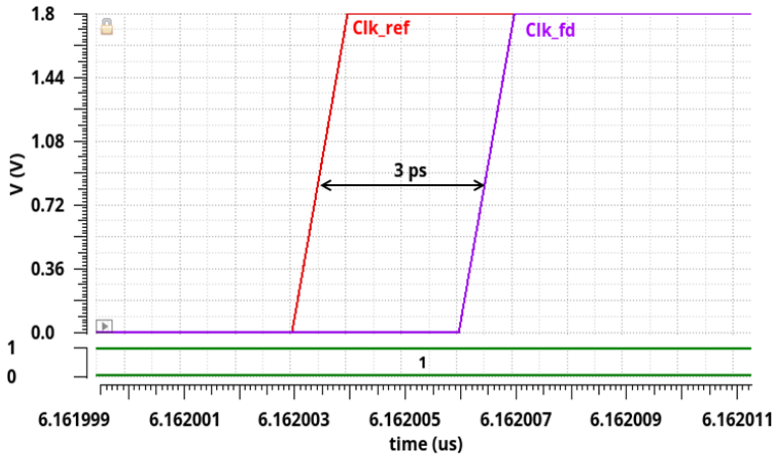


(c)

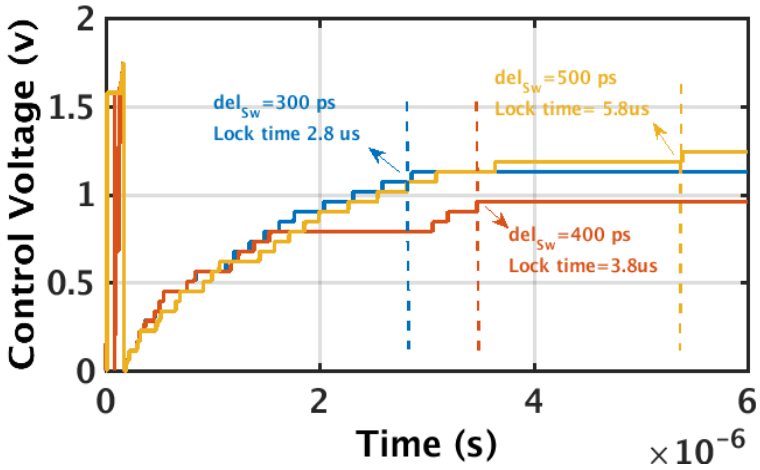
Fig. 6.8 (a) Output of BB-PFD and TDC during ADPLL-II locking process, (b) Output of proposed BB-PFD, (c) Shows an output of TDC while working in ADPLL-II

Fig. 6.8 (b) shows the output when proposed BB-PFD brings the delay difference to 306 ps and achieves a fast acquisition time of 2.6 µs. Thereafter, the proposed ADPLL-II switches to TDC loop. The output of TDC during locking time is depicted in the Fig. 6.8 (c).

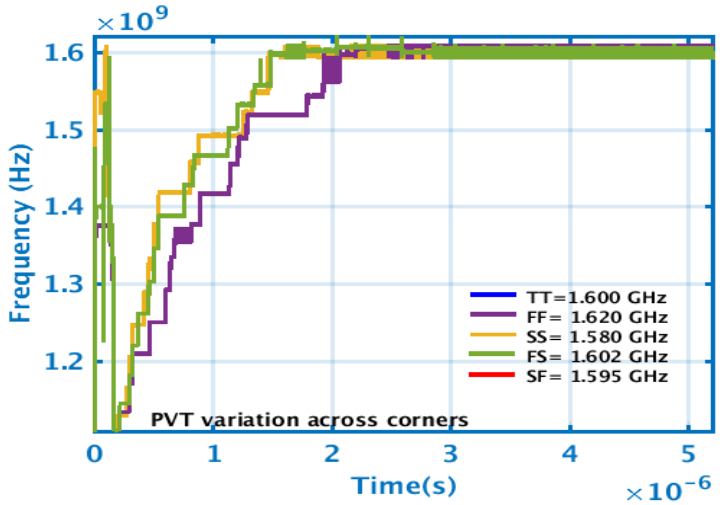
6.8 Simulation Results of ADPLL-II

This section shows the simulation results of proposed ADPLL-II. Fig. 6.9 (a) shows the variation of lock time with internal delay del_{Sw} of proposed BB-PFD. The locking time of ADPLL-II increases with increase in the delay del_{Sw}. The optimum value of delay del_{Sw} is 306 ps to achieve the fast lock time and to reduce periodic jitter of the proposed ADPLL-II. The proposed hybrid ADPLL-II switches between linear and non-linear characteristics. During the first or initial phase, in the frequency acquisition process, bang-bang PFD detects a frequency difference between reference and target frequency. During this phase, feedback signal frequency is increasing but phase error is still increasing as feedback frequency signal is slow. After few iterations, the feedback frequency is faster and phase error starts decreasing. ADPLL-II exhibits a non-linear characteristic and give rise to sharp rise and fall curves. Once the target frequency is achieved, BB-PFD reduces phase difference between reference and feedback clock and brings it to range of TDC. In TDC loop, the ADPLL-II shows linear characteristics and it keeps an ADPLL-II in the locked state. The variations in the output frequency of ADPLL-II across the different PVT corners are shown in the Fig. 6.9 (b). The reduced PVT variation of 2% is observed at the extreme corners with respect to typical corner in proposed ADPLL-II design. At the output frequency of 1.6 GHz, the observed pre-layout periodic jitter is 1.62 ps as given in the Fig. 6.10 (a). The periodic jitter after post layout simulations is 1.71 ps and it is 4.8% more than the pre-layout of 1.62 ps. Fig. 6.10 (b) shows the phase noise analysis of

proposed ADPLL-II architecture. The phase noise of proposed ADPLL-II architecture is -137.9dBc/Hz and -131.2 dBc/Hz respectively at an offset of 100 MHz after the pre-layout and post layout simulations. The RMS jitter of ADPLL-II is 0.28 ps. The power consumption by different blocks of ADPLL-II after post layout simulations is shown in the Fig. 6.10 (c).

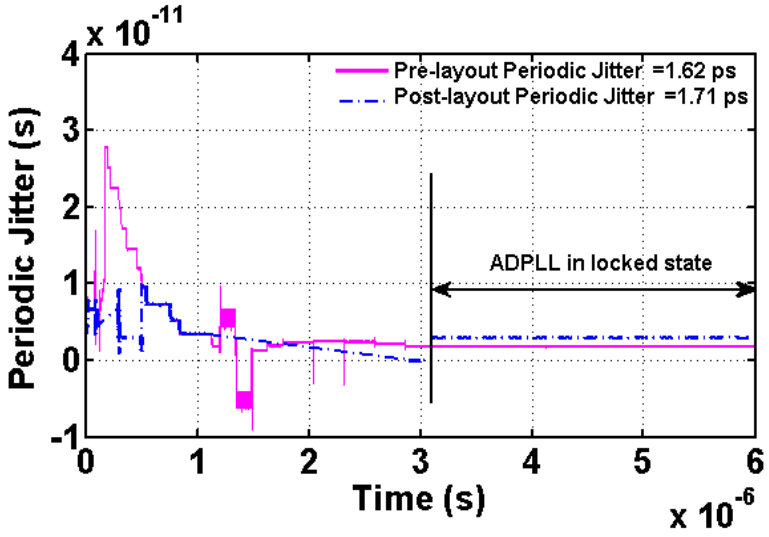


(a)

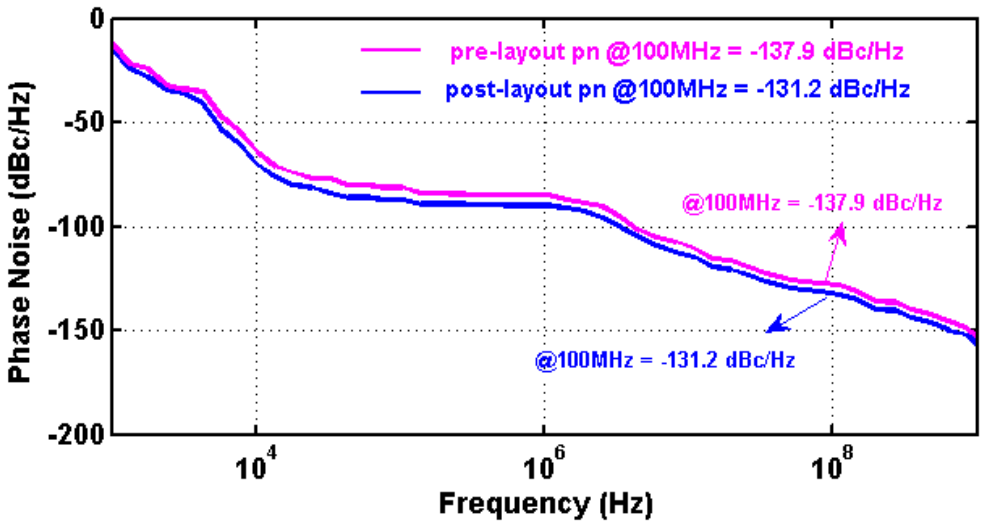


(b)

Fig. 6.9 (a) ADPLL-II locking time with different del_{Sw} values, (b) PVT variations of output frequency of ADPLL-II



(a)



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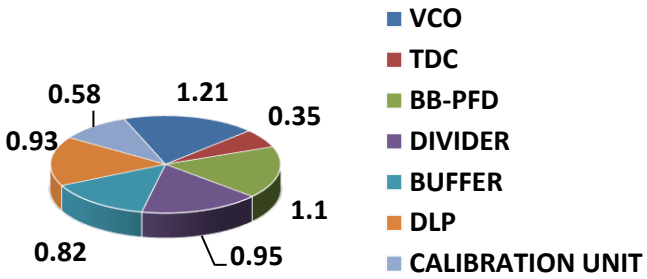


(c)

Fig. 6.10 (a) Periodic jitter of proposed ADPLL-II, (b) Phase noise of proposed ADPLL-II, (c) Power consumption by different blocks of ADPLL-II

The periodic jitter is in ±0.2% range of output frequency (*i.e.* 1.6 GHz) with the fast locking time of 2.8 µs. The post layout simulation shows the periodic jitter variation across different corners in ADPLL-II given in the Table 6.3. The FF and SS corner shows a variation of 2.9% and 2.6% respectively with respect to TT corner. There is variation of 1.6% at FS and SF corner. The values of performance parameters of proposed ADPLL-II are shown in Table 6.4.

Table 6.3: Periodic jitter of ADPLL-II at different PVT corners

PVT Corners	Periodic Jitter (ps)
TT	1.71
FF	1.67
SS	1.76
FS	1.69
SF	1.72

Table 6.4: Performance parameters of proposed ADPLL-II after post layout simulations

Parameters	Proposed ADPLL-II
Supply Voltage (V)	1.8
PLL output Freq. (GHz)	0.025-1.6
Resolution (ps)	3
Jitter (ps)	1.71
Reference Frequency (MHz)	25
Locking Time (μs)	3.1
Power Consumption (mW)	5.94
Division ratio	64
FoM (dB)	-227.6
Technology Process (nm)	180

The hybrid architecture of proposed ADPLL-II shows a fast-locking time and requires 5 clocks cycles to get an ADPLL-II locked.

6.9 Conclusion

In this chapter ADPLL-II design is proposed for low power, fast lock timing and low jitter. ADPLL-II design is proposed to improve the power consumption and periodic jitter as compared to the works in the literature. Another version of flash TDC with calibration is proposed. In ADPLL-II, architecture, high resolution TDC with 3 ps and calibration is used as compare to TDC2 with 6 ps resolution. High resolution of TDC reduces the PVT variations in the ADPLL-II architecture. Also, the bang-bang phase frequency used also gives lower PVT as architecture is digital in nature and comprised of few gates and D-flipflops. Whereas in ADPLL-I, Vernier TDC is used which is more prone to PVT variations and degrades PVT variations for ADPLL-I design more as compared to ADPLL-II. The resolution of 3-bit TDC is 3 ps and periodic jitter is 0.152 ps. The proposed ADPLL-II design has improved periodic jitter performance with value 1.71 ps and power consumption is 5.94 mW. To further enhance the parameters of ADPLL-II for low power SoC and wireless transceiver applications, ADPLL-III is proposed. The digital calibration based VCO-II, 3-bit flash TDC is used to propose the ADPLL-III.

CHAPT ER 7

DESIGN AND ANALYSIS OF GENERIC ALL DIGITAL PHASE LOCKED LOOP

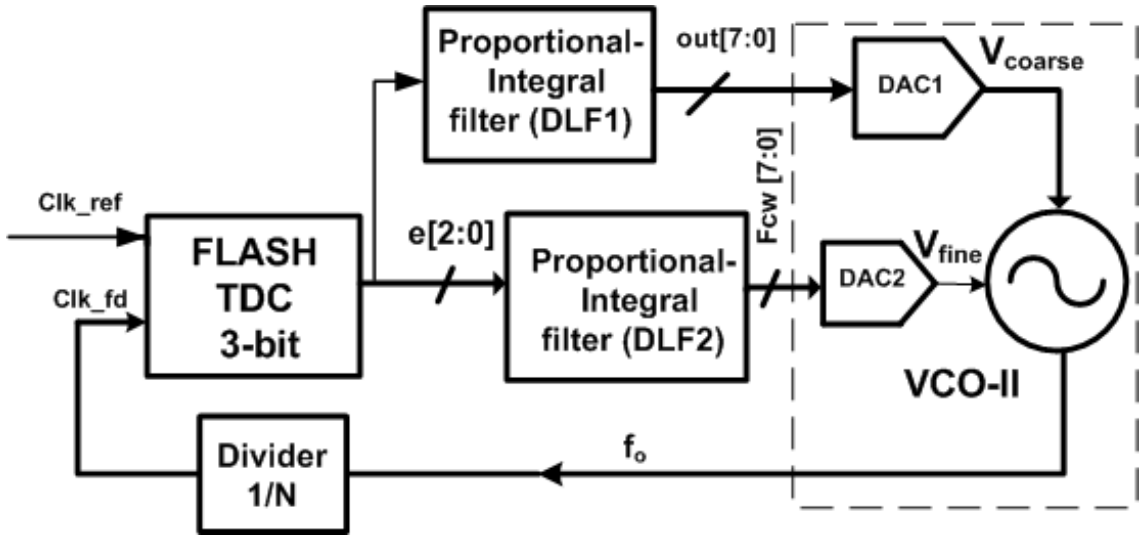
7.1 Introduction to ADPLL-III Design

In present work, ADPLL-III is designed to further enhance the parameters of earlier reported designs. ADPLL-III is designed for low power for SoC and wireless transceiver applications [4-5, 17]. ADPLL-I and ADPLL-II achieves a periodic jitter of 6.6 ps and 1.71 ps and power consumption of 6.3 mW and 5.9 mW respectively. The proposed ADPLL-III is designed with the target periodic jitter < 2 ps and power consumption < 6 mW for low power SoC and wireless transceiver applications [4-5, 17]. The periodic jitter, locking time, and power are main design constraints which determine the performance of ADPLL architecture. TDC and DCO are major source of jitter and power consumption in the ADPLL design. As described by the curve in the Fig. 6.1 (d), the loop bandwidth drastically impacts the jitter performance of ADPLL design and loop bandwidth depends upon the loop parameters. The optimized loop bandwidth ensures the reduced jitter ADPLL design [45, 62-63]. In this chapter another version of ADPLL is designed targeting low jitter and low power at output frequency specifications of 1.6 GHz. This architecture consists of 3-bit flash TDC, a background calibrated VCO-II, coarse and fine tune DACs, [29] and dividers. The proposed ADPLL-III design utilizes a 3-bit flash TDC which is described in section 3.4.

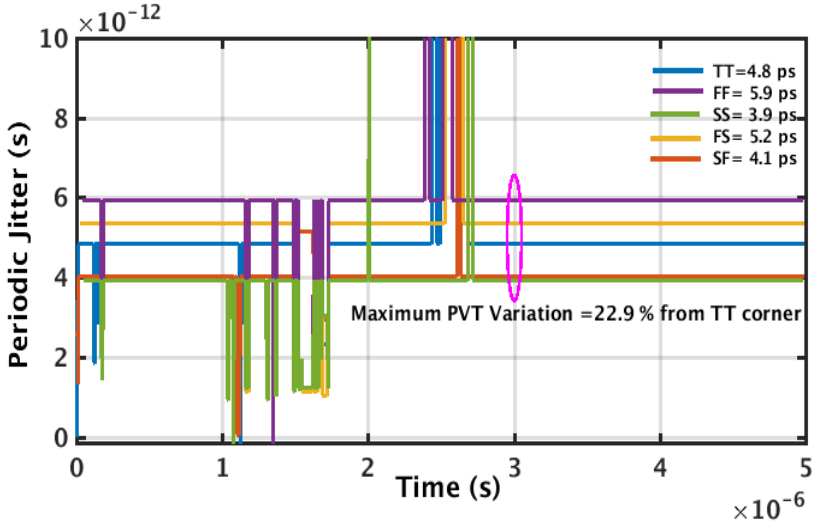
7.2 Issues with ADPLL-III design and need of calibration of VCO-II

The proposed ADPLL-III consists of 3-bit flash TDC, VCO-II, DAC [29], digital loop filter, and dividers as shown in the Fig. 7.1 (a). ADPLL-III works in two parallel loops and Clk_ref is given to the 3-bit flash TDC. The Clk_fd is produced by the ADPLL-III after certain iterations. The output of TDC is e [2:0] is given to two digital filters and outputs of filters are scaled by the gain coefficients of digital filters. The output of DLF-I is given to DAC1 and the output of DLF2 is given to DAC2. DAC1 and DAC2 produce a V_{coarse} and V_{fine} respectively. The V_{coarse} tunes a VCO-II to frequency range of 1.6 GHz. The V_{fine} fine tunes a VCO-II with finer gain which improves the phase noise performance of VCO-II. The ADPLL-III works at output frequency of 1.6 GHz. A low power and low periodic jitter 3-bit flash TDC along with low phase noise VCO-II is used to realize the ADPLL-III architecture. The achieved periodic jitter is 4.8 ps for ADPLL-III architecture. Fig. 7.1 (b) shows the PVT variations at different corners in periodic jitter for ADPLL-III design. It is observed that variation in ADPLL-III is 22.9%. Also, the power consumption of this architecture is 11 mW. In order to mitigate the PVT variations and to achieve low periodic jitter VCO-II, calibration is done on the proposed

VCO-II design and thus it reduces the periodic jitter and locking time of proposed ADPLL-III design. Fig. 7.1 (c) shows the block level diagram of ADPLL-III with calibration unit. The ADPLL-III has 3-bit flash TDC, VCO-II with calibration, lock detection circuit and DCO. The proposed 3-bit flash TDC has high resolution of 3 ps and periodic jitter of 0.46 ps as explained in the section 3.4. The clock Clk_ref is given to calibration unit, main loop, and lock detection simultaneously. The main loop generates a Clk_fd after single iteration. The calibration unit produces a control voltage V_{coarse} after comparing the phase difference between Clk_ref and Clk_fd. The Clk_ref and Clk_fd are given to lock detection which checks the minimum phase difference between the Clk_ref and Clk_fd. The signal pw is generated by lock detection circuit and initially, it is at logic '0'. Once the ADPLL-III gets locked into the state, pw becomes logic '1' and calibration unit is sent to reset state. In main loop, the output of TDC e [2:0] is given to digital filter.



(a)



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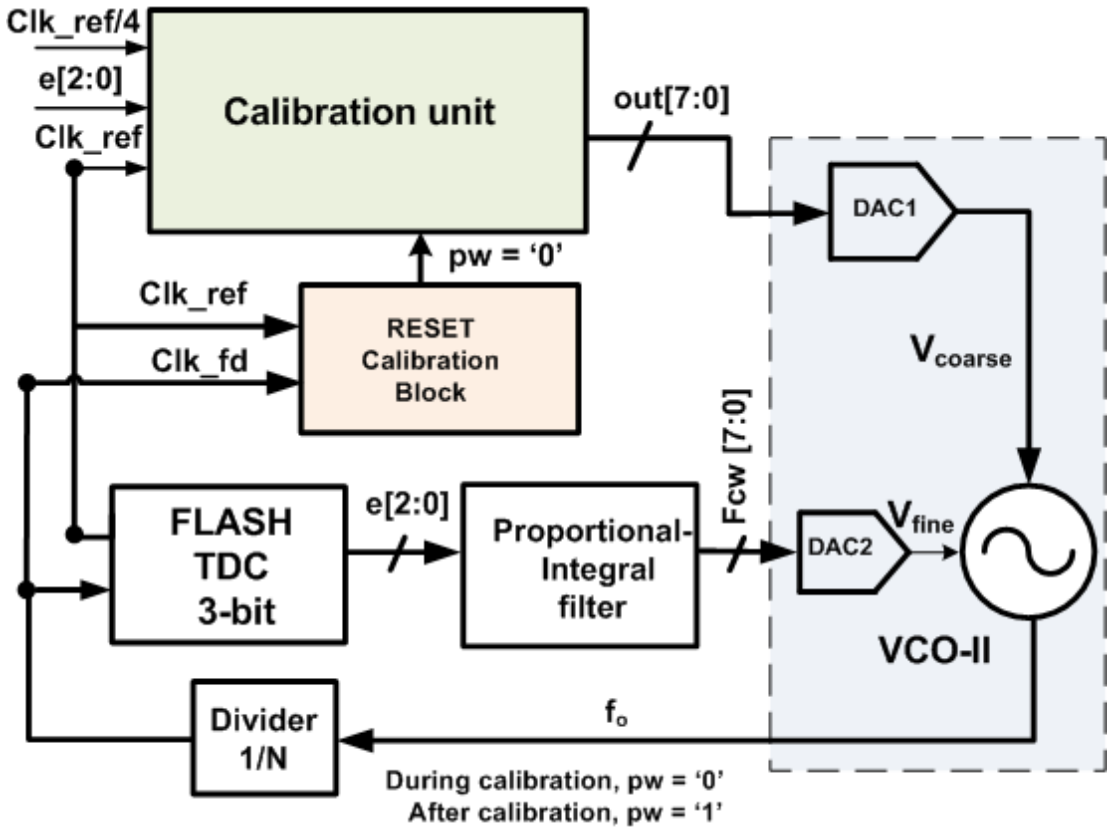


(c)

Fig. 7.1(a) ADPLL-III-without calibration, (b) PVT variation of periodic jitter in ADPLL-III -without calibration (c) Block level diagram of ADPLL-III

The filter coefficients α and β modulates the output of TDC. The output of filter is given to DAC2 which fine tunes the VCO-II. The ADPLL-III generates an output frequency of 1.6 GHz. The proposed VCO-II with calibration is described in the section 7.3 and its simulation results in section 7.4.

7.3 VCO-II Design

VCO is the heart of all PLL architectures. It generates desired frequencies which are controlled by the control voltage. The proposed VCO-II is shown in the Fig. 7.2 (a). Typical VCO design should have large gain K_{VCO} and large frequency range to cover wide applications range and to inhibit the PVT variations in VCO. But large gain of VCO degrades the noise related to control voltage and affects performance of VCO. This leads to frequency drifts and larger spurious frequencies in the output frequency. Such noise is undesirable as it creates interference in ADPLL especially, when it works at higher frequencies in range of gigahertz [101]. Therefore, in order to address this issue, wide tuning range of VCO is divided into smaller bands [91]. The large gain K_{Voarse} covers a wide range of frequency and within this frequency

range, the proposed VCO-II chooses a desired frequency with fine gain K_{fine}. The smaller gain of VCO-II allows selecting desired frequency with the fine resolution and thus it reduces the phase noise and jitter of the proposed VCO-II. The proposed VCO-II consists of Inverter (Inv1-Inv8) and NMOS (ML1 and ML2) which act as load elements. The Inverters (Inv1-Inv6) are primary inverters and load elements (ML1 and ML2) decide the frequency of operation. The control voltage V_{coarse} from DAC1 [29] is used to set the frequency of VCO-II to desired working range. The Inv7 & Inv8 are used as phase interpolators. They provide phase difference of 180 degrees between the two rings. The control voltage V_{coarse} and V_{fine} are used to vary the frequency of VCO-II. The V_{coarse} is provided at the gate input of NMOS (MLI and ML2) which brings the VCO-II to desired frequency of operation *i.e.* 1.6 GHz. The V_{fine} allows choosing the optimum frequency from operating frequency range of 1.6 GHz with low VCO gain in the range of few hundred kilohertz per millivolt. For selecting the optimum frequency with the fine resolution, calibration is needed. To achieve a fast locking time, low jitter, and low power, calibration unit (as shown in the Fig. 7.1(c)) is required which fixes the desired frequency of operation in the minimum time. Therefore, LMS algorithm [93] is used to find the optimum frequency of operation in background. The proposed calibration is fast and predominately digital in nature thus requires a low area and low power. The frequency of proposed VCO-II is fined tuned by the series combination of fine tune elements (Mp3 and Mp4). The series combination of fine tune elements (Mp3 and Mp4) provides a more linear change in resistance and capacitance of fine tune elements (Mp3 and Mp4) and therefore a fine variation in the output frequency of proposed VCO-II is obtained. The proposed VCO-II works in the linear range from 0.5 V to 1V with the V_{coarse} and it gives maximum frequency at 1V. The VCO-II shows a fine resolution of 160 kHz/mV which improves the phase noise performance of VCO-II. The gain K_{fine} gives frequency range from 1.55 to 1.63 GHz with control voltage of 0.1 to 1 V for the proposed VCO-II. The two 8-bit DACs –DAC1 & DAC2 and the proposed VCO-II are used as the DCO in this current ADPLL-III architecture. The proposed calibration based VCO-II, 3-bit flash TDC and digital filter is used in ADPLL-III design. The large gain and small gain curve for VCO are shown in the Fig. 7.2 (b) and Fig. 7.2 (c). For VCO-II at switching point and at the output nodes of the inverters of VCO-II as shown in the Fig. 7.2 (a), τ_{dn_coarse} is the delay from low to high transition in Inverters (Inv1- Inv6) and in coarse tune elements (ML1 and ML2) due to V_{coarse}. τ_{dn_fine} is delay offered by (Mp3 and Mp4) due to V_{fine}. Similarly, τ_{dp_coarse} and τ_{dp_fine} are the delays offered by the Inverter (Inv1-Inv6) & coarse tune elements (ML1 and ML2) and by the fine tune (Mp3 and Mp4) during high to low

transition at output node (n1-n6) of each inverter (Inv1 to Inv6). The frequency of oscillation of VCO-II is given by the inverse of delay offered by [91]:

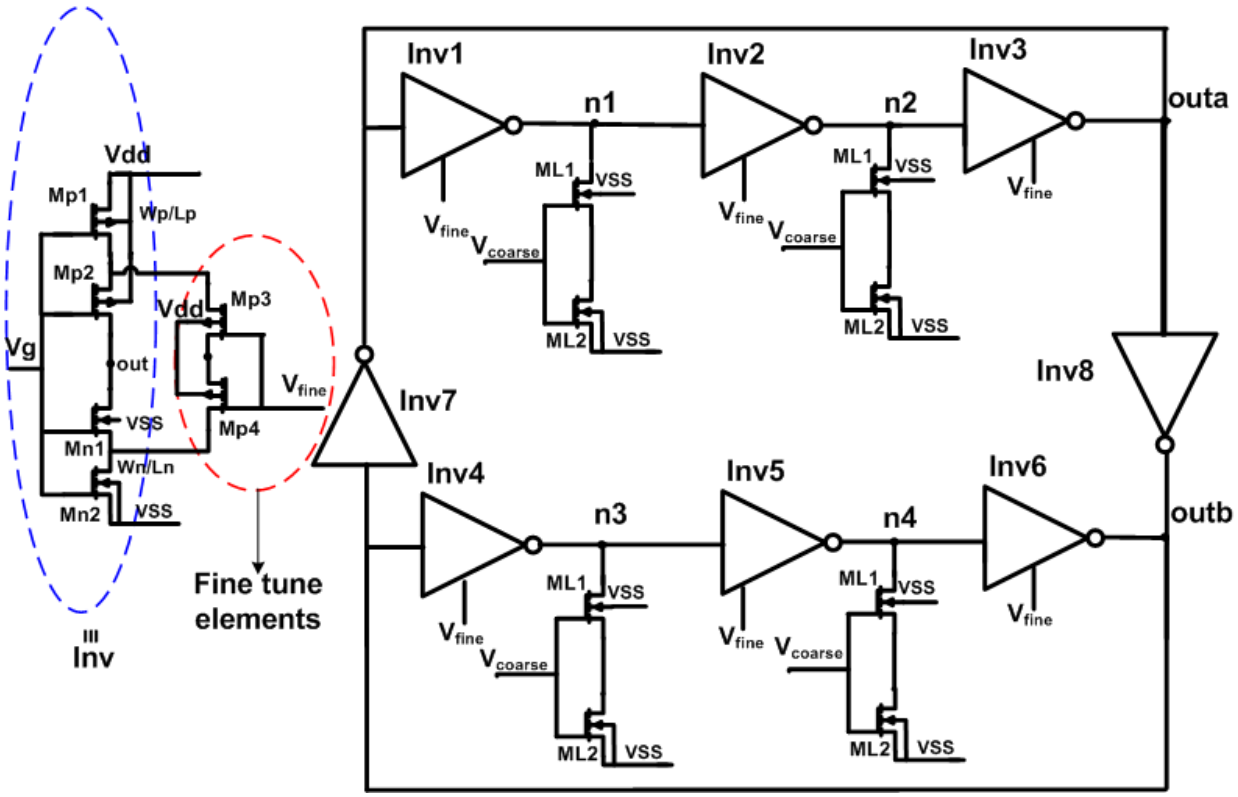
$$\tau_{dn\_coarse} = \frac{VDD}{2I_N}(n(C_{INV}) + (n-2)(C_{ML1} + C_{ML2})) \tag{7.1}$$

$$\tau_{dp\_coarse} = \frac{VDD}{2I_P}(n(C_{INV}) + (n-2)(C_{ML1} + C_{ML2})) \tag{7.2}$$

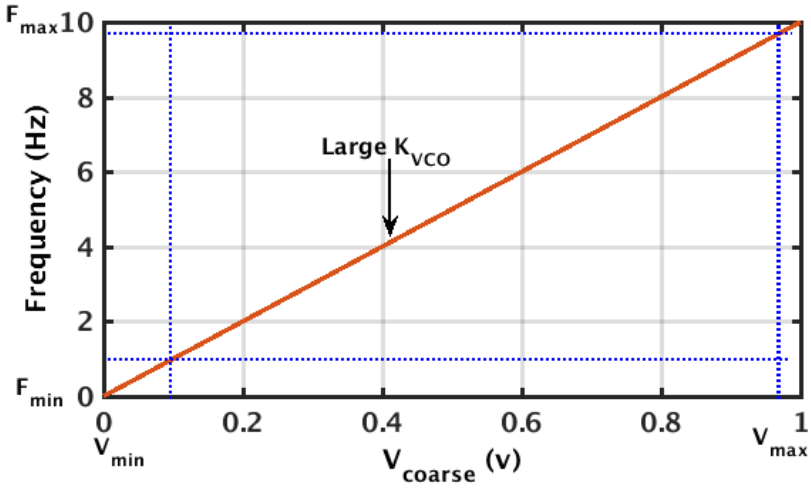
$$\tau_{dn\_fine} = \frac{VDD}{2I_N} n(C_{Mp3} + C_{Mp4} + \Delta C_{Mp3} + \Delta C_{Mp4}) \tag{7.3}$$

$$\tau_{dp\_fine} = \frac{VDD}{2I_P} n(C_{Mp3} + C_{Mp4} + \Delta C_{Mp3} + \Delta C_{Mp4}) \tag{7.4}$$

where C_{INV} is the gate capacitance offered by inverter (Inv1-Inv6), C_{ML2} and C_{ML1} are the gate capacitances given by coarse tune elements (ML1and ML2) with V_{coarse}, C_{Mp3} and C_{Mp4} are the gate capacitances of the fine tune elements (Mp3 and Mp4), ΔC_{Mp3} and ΔC_{Mp4} are the change in gate capacitances given by the fine tune elements (Mp3 and Mp4) with V_{fine}. n is the number of inverter stages in the VCO-II.



(a)



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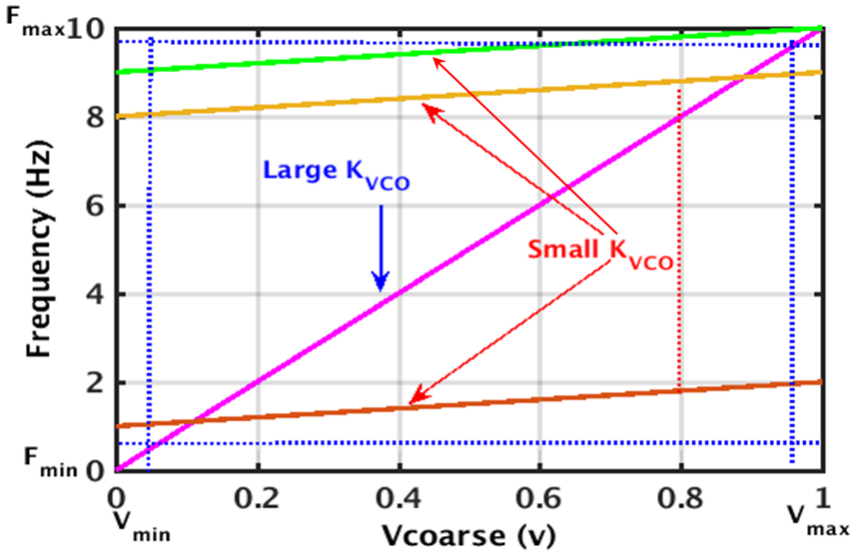


(c)

Fig. 7.2 (a) Proposed VCO-II, (b) Shows a VCO with large gain, (c) Shows VCO with smaller gain

VDD is the supply voltage. f_{VCO-II} is frequency of oscillation of VCO-II:

$$f_{VCO} = \frac{1}{n(\tau_{dn\_coarse} + \tau_{dp\_coarse} + \tau_{dn\_fine} + \tau_{dp\_fine})} \tag{7.5}$$

The jitter analysis of VCO-II is discussed next. For 0 to 1 transition, jitter depends upon the τdn_{coarse} and τdn_{fine}, C_{ML1} and C_{ML2}, C_{Mp3} and C_{Mp4}, ΔC_{Mp3} and ΔC_{Mp4}, I_N, v_{tN} switching voltage at toggle point $v_{tN} = 1/VDD$, and supply voltage VDD. The jitter due to coarse and fine tune elements is given below [91]:

$$\sigma N^2_{coarse} = n\left(\frac{4kT\gamma_N \tau_{d\_coarse}}{I_N(VDD - v_{tN})}\right) + \frac{kTn(C_{INV}) + (n-2)(C_{ML1} + C_{ML2})}{I_N^2} \tag{7.6}$$

$$\sigma N_{fine}^2 = n\left(\frac{4kT\gamma_N \tau_{d\_fine}}{I_N(VDD - v_{tN})} + \frac{kT(C_{Mp3}+C_{Mp4} + \Delta C_{Mp3} + \Delta C_{Mp4})}{I_N^2}\right) \quad (7.7)$$

where k is Boltzmann's constant, T is the temperature,ϒ is bias dependent factor. Similarly, σP_{coarse}^2 and σP_{fine}^2 are jitter calculated in the high to low transition. Considering $v_{tN} = v_{tP} = v_t$ and $I_N = I_P = I$ .The total jitter offered by the proposed VCO-II is given as below:

$$\sigma_T{}^2 = \frac{kT}{If_{VCO-II}}\left(\frac{2(\gamma_N + \gamma_P)}{(VDD - v_t)} + \frac{2}{VDD}\right) \quad (7.8)$$

The power consumed by VCO-II depends upon the frequency of oscillation f_{VCO-II}, n is number of stages of VCO-II and C_{INV} gate capacitance of inverter, and coarse and fine elements. The power P_{coarse} and P_{fine} are consumed by the coarse and fine tune elements respectively. The total power P_{Total} consumed by the VCO-II is given as by (7.11):

$$P_{coarse} = f_{VCO-II}V_{DD}^2(nC_{INV} + (n-2)(C_{ML1} + C_{ML2})) \quad (7.9)$$

$$P_{fine} = f_{VCO-II}V_{DD}^2(n(C_{Mp3}+C_{Mp4} + \Delta C_{Mp3} + \Delta C_{Mp4})) \quad (7.10)$$

$$P_{Total} = P_{coarse} + P_{fine} \quad (7.11)$$

It is concluded from above analysis that the change in the capacitance of coarse tune and fine elements drastically impacts the jitter but total jitter is independent of number stages of VCO-II and delay elements. The jitter and power are significantly affected by the frequency of oscillation and power supply of VCO-II and which also affects the overall power budget and periodic jitter specifications of ADPLL architecture.

7.3.1 VCO-II Calibration Process

Initially at startup, calibration block and main loop in the ADPLL-III is given reference clock signal Clk_ref with period of '40 ns' as shown in the Fig. 7.1 (c). Also initially, the signal pw is at logic '0'. After 1 clock cycle, the feedback clock signal Clk_fd is generated and the phase difference between Clk_ref and Clk_fd is large. The reference clock Clk_ref, Clk_ref/4 and feedback signal Clk_fd are provided to calibration loop as shown in the Fig. 7.1 (c). The reference Clk_ref and feedback Clk_fd is also given to main loop simultaneously. The calibration block works at the clock Clk_ref/4 with period of '10 ns. Also initially, the weights w [15:0] assigned to the FIR filter of calibration block are set to state '1'. After the calibration is done and pw signal is set to logic '1' by lock detection circuit, error signal outd [7:0] becomes minimum and given to DAC1 for coarse tuning of VCO-II. To reduce the power budget and design complexity, delay tap length of FIR filter is taken as 20 for conversion. The output of FIR filter is defined by:

$$dn[\mathrm{n}:0] = \sum_{i=0}^{i=M-1} \mathrm{SAR\_OUT}[2:0][n-i] * \mathrm{w}[\mathrm{n}:0] \quad (7.12)$$

where *i* is the number of coefficients, SAR_OUT [2:0] is desired signal generated by reference TDC, M is length of FIR filter, and n is number of bits of output of filter and is equal to 31. To start calibration, SAR TDC is taken as reference TDC [75]. 2-bit Vernier TDC is used to generate the signal Clk_fdl which is given to the SAR TDC as explained in the section 5.4. The output of SAR TDC is given to the FIR filter. The signal dn[31:0] is generated by the FIR filter. In order to make the error between reference input SAR_OUT [2:0] and actual input e2[2:0] minimum, LMS algorithm is used in which the weights of tapped delay FIR filter are updated. The minimum error (outd) is set to value of '00001000', SAR_OUT [2:0] and e2[2:0] are given to LMS engine which updates the weights w [31:0] according to:

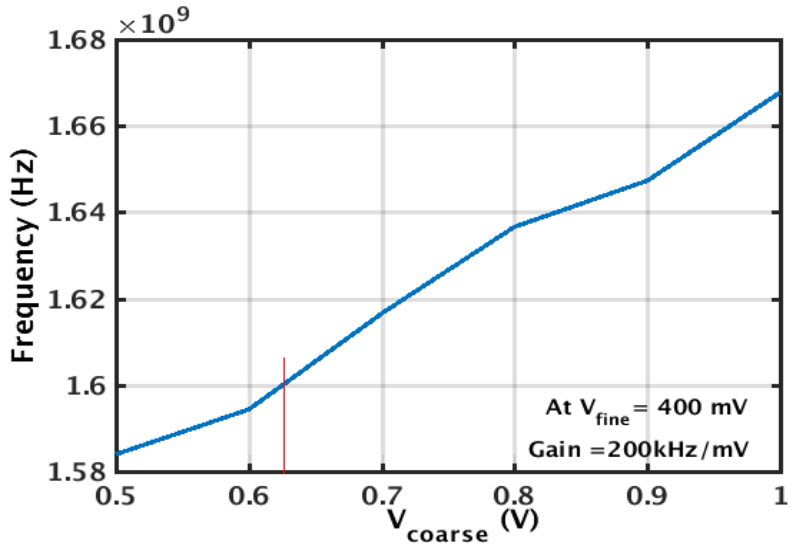
$$w_{final}[n:0] = w[n:0] + outd[n:0] * \mu * e2[2:0] \quad (7.13)$$

$$outd[n:0] = dn[n:0] - yn[n:0] \quad (7.14)$$

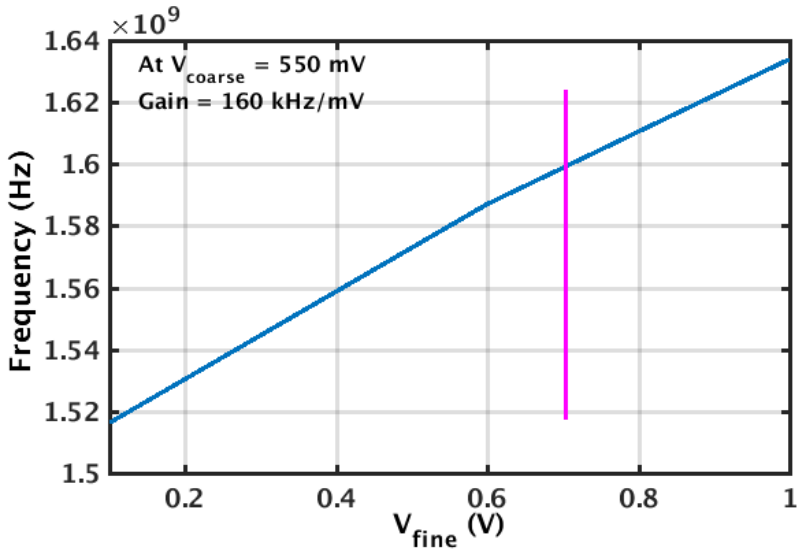
where μ is the step size used for convergence speed [93]. To lower the complexity of ADPLL design, the step size μ and the values of preliminary weights are taken as '1'. The error voltage (outd) from the DAC1 settles at constant value. The error signal (outd[7:0]) saturates at particular value after the weights become constant and remains constant until the next phase of calibration starts. The MSBs of output out [7:0] of LMS engine is given to the DAC1. The DAC1 settles at the value of 520 mV. By taking the SAR TDC as reference TDC, the power is reduced as SAR TDC takes few D-flip-flops and multiplexers to generate the accurate output. The LMS will track the phase difference between the Clk_ref and Clk_fd and reduces the phase difference to minimum after few clock cycles. The DAC1 produces a control voltage V_{coarse} which changes the frequency of VCO-II and bring the frequency of VCO-II to desired range of 1.6 GHz. The calibration block takes 240 ns to calibrate the proposed VCO-II. Simultaneously, ADPLL-III is also working in the main loop and parameters of loop filter ensure the stability of ADPLL-III. The phase difference between the reference Clk_ref and feedback Clk_fd reduces and ADPLL-III gets into locked state after 1.5 μs. Section 5.4 on page no. 82 shows detail of LMS algorithm and SAR TDC. The description for DAC is added on page 85 in section 5.4.

7.4 Simulation Results of VCO-II

This section shows the simulation results of VCO-II design. The background calibration is done to achieve the low periodic jitter of ADPLL-III design. The Fig. 7.3 (a) and (b) shows the achieved gain VCO-II with control voltage V_{coarse} and V_{fine} respectively.



(a)



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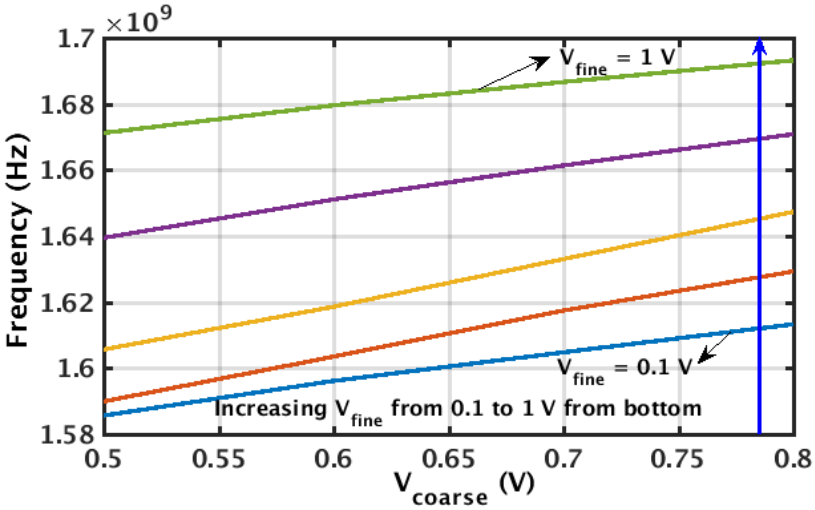
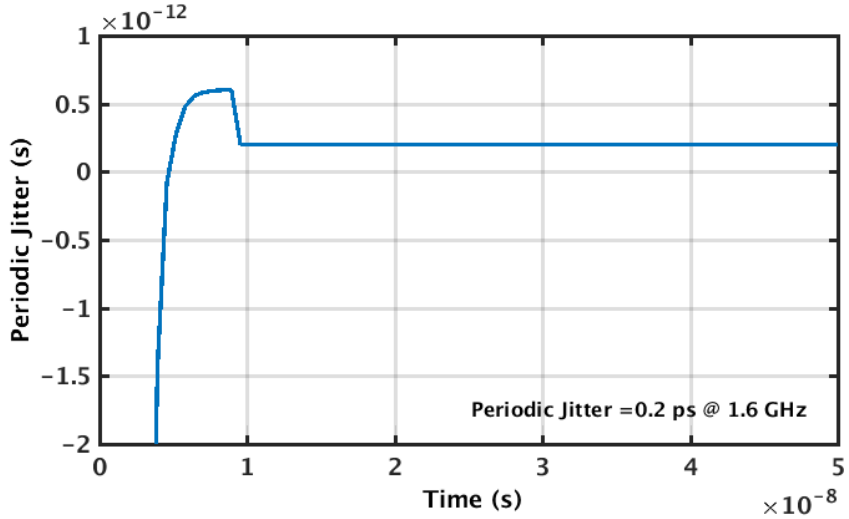


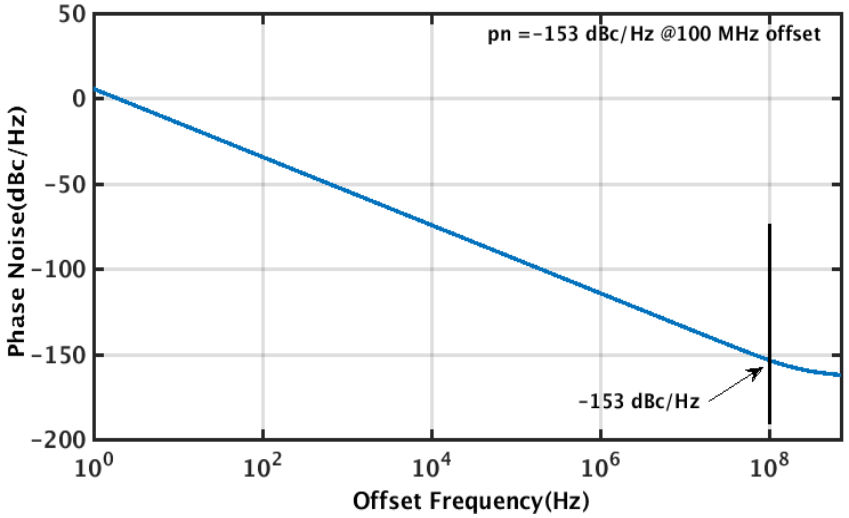
(c)

Fig. 7.3 (a) Gain of VCO-II with $V_{coarse,}$ (b) Gain of VCO-II with V_{fine}, (c) Gain variation with V_{coarse} and V_{fine}

It is observed that achieved gain sensitivity with V_{coarse} is 200 kHz/mV and with V_{fine} is 160 kHz/mV respectively. Fig. 7.3 (c) shows the variation of V_{coarse} and V_{fine} with the output frequency of proposed VCO-II. The curve shows linearity range from 0.5 V to 1 V with V_{coarse} and from 0.1 to 1 V with V_{fine} respectively. The minor variation in linearity does not affect the performance of VCO-II. Fig. 7.4 (a) shows the periodic jitter of VCO-II and value of periodic jitter is 0.2 ps. The achieved periodic jitter of VCO-II is very low and thus enhances the performance of ADPLL-III design. The phase noise of VCO-II is -153 dBc/Hz at 100 MHz offset as shown in the graph in Fig. 7.4 (b). The PVT variation is shown in the Fig. 7.4 (c). It is observed the variation of 0.5% and 2.3 % is observed with SS and FF with respect to TT corner. Table 7.1 shows the performance parameters of VCO-II. The proposed cascode structure of VCO-II helps to alleviate problem of PVT variations.



(a)



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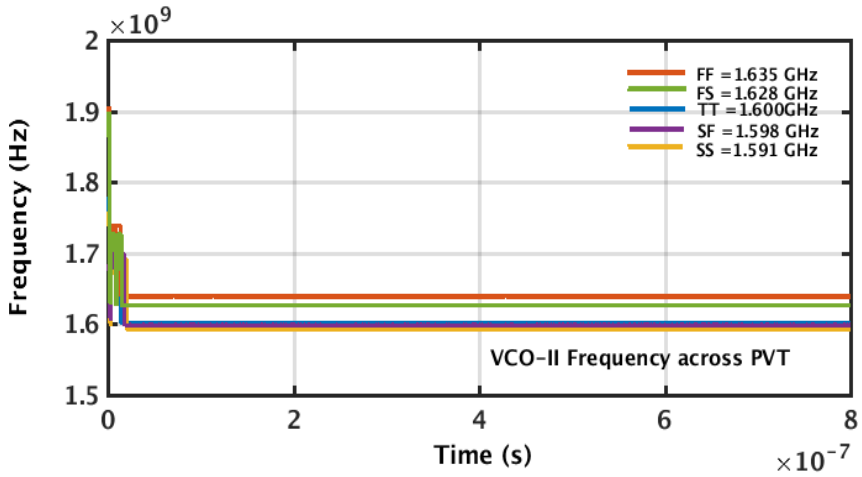


(c)

Fig. 7.4 (a) Periodic jitter of VCO-II, (b) Phase noise of VCO-II, (c) PVT variation of VCO-II

Table 7.1: Performance parameters of VCO-II

Parameters	Proposed VCO-II
Periodic Jitter (ps)	0.2
Power (mW)	0.9
Phase Noise (dBc/Hz) @ 100 MHz	-153
Gain (kHz/mV)	160

Further, the LMS algorithm is used for gain calibration for VCO-II. The proposed architecture of VCO-II benefits to realize low phase noise and low PVT variations in the ADPLL-III design.

7.5 ADPLL-III Architecture

Fig. 7.5 (a) and (b) shows the proposed architecture of ADPLL-III design and flowchart for calibration steps respectively. Fig .7.5 (c) shows a layout of proposed ADPLL-III architecture. It consists of 3-bit flash TDC, proposed VCO-II with background calibration, 8-bit coarse and fine tune DACs. For given design specifications of periodic jitter 1.8 ps and power consumption of 6 mW for ADPLL-III, 8-bit DACs are sufficient to characterize the ADPLL-III. The fine gain of 160 kHz/mV for proposed VCO-II is achieved by calibration process. Such low gain of VCO-II is sufficient to mitigates an any non-linearity given by DAC block of proposed architecture and therefore, any noise from the DAC will not affect the phase noise of VCO-II and retains the variations within 0.1% of the output frequency. The background calibration loop with LMS algorithm [93] is used. The calibration process is used in this architecture to reduce the periodic jitter of VCO-II which also reduces the periodic jitter of ADPLL-III design. The calibration process also reduces the locking time of ADPLL-III as the V_{coarse} tracks the frequency of VCO-II early due to fast calibration path and brings the frequency

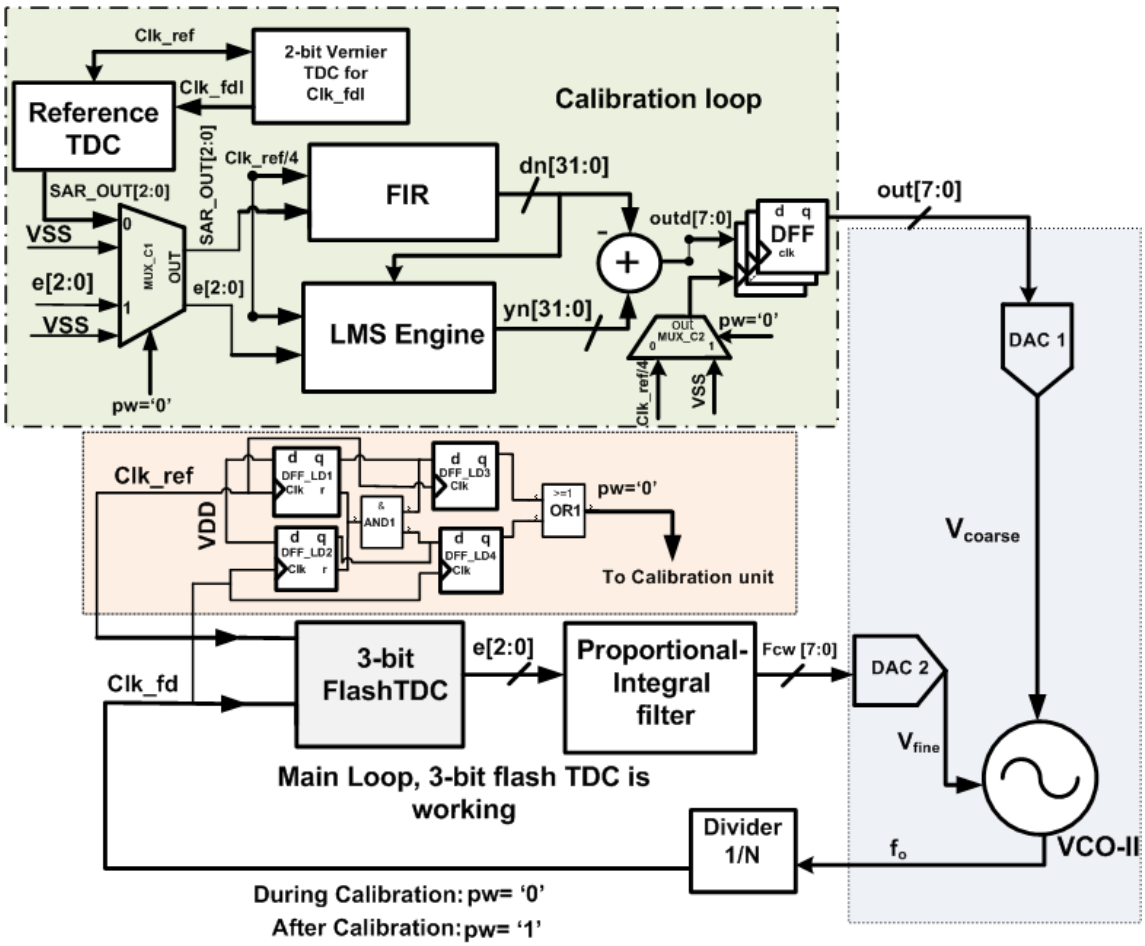
of proposed ADPLL-III to desired range. The 3-bit flash TDC have periodic jitter of 0.46 ps and the proposed VCO-II has periodic jitter of 0.2 ps. The proposed VCO-II with calibration has very less periodic jitter and thus 3-bit flash TDC without calibration is used in order to have less complexity, low area, and low power consumption for ADPLL-III design. The gain and loop bandwidth of ADPLL design significantly impacts the jitter performance [61-62]. The relation between gain and loop bandwidth is given by equation [61]:

$$G_{loop}(Z) = \frac{NK_{TDC}K_{DCO}}{1-Z^{-1}} * (\alpha + \frac{\beta}{1-Z^{-1}}) \tag{7.15}$$

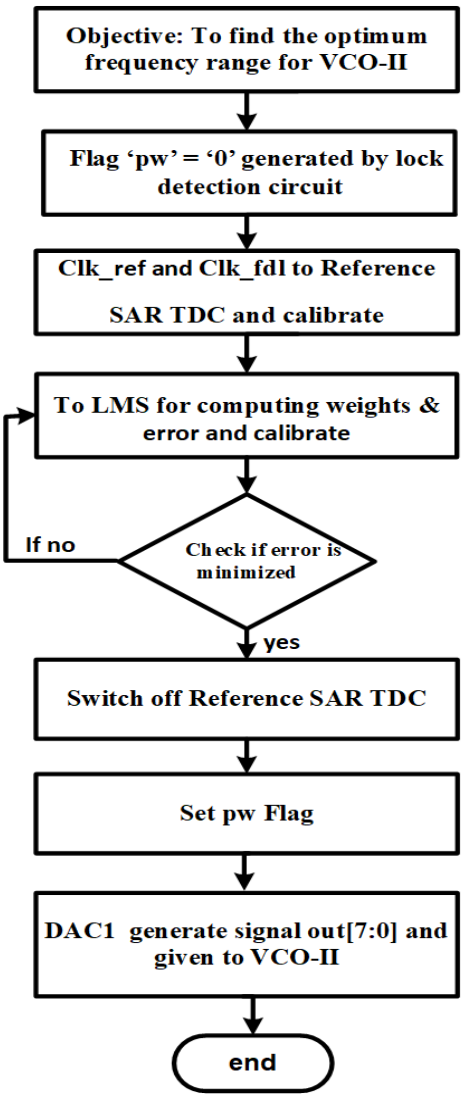
$$G = NK_{TDC}K_{DCO} \tag{7.16}$$

$$f_{bw} = \frac{\beta}{2\pi} f_{ref} G \tag{7.17}$$

where $G_{loop}(Z)$ is the loop gain, K_{DCO} and K_{TDC} are the gains of DCO and TDC respectively, N is gain of divider, α and β are the parameters of loop filter. f_{bw} and f_{ref} are the bandwidth and reference frequency of ADPLL-III respectively.



(a)



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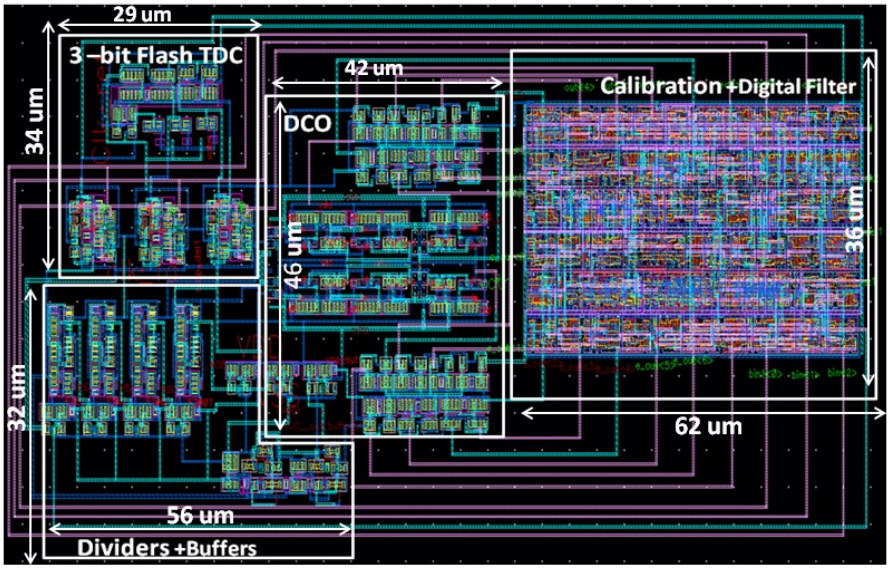
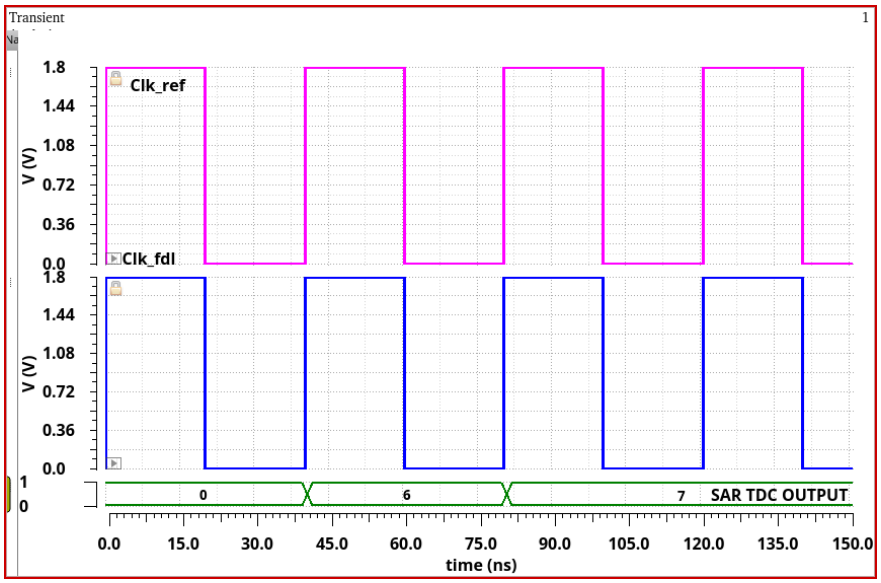


(c)

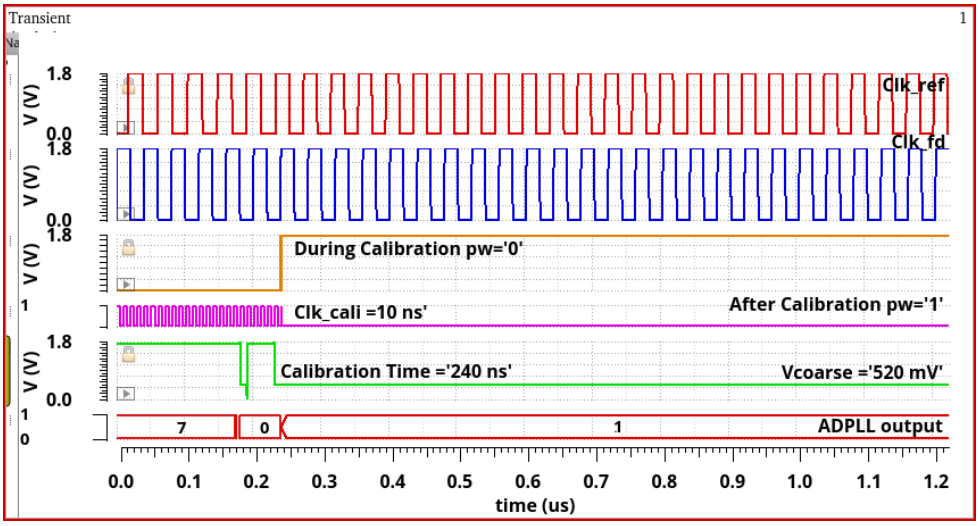
Fig. 7.5 (a) Proposed ADPLL-III, (b) Calibration steps for VCO-II, (c) Layout of ADPLL-III

The gain sensitivity of VCO significantly changes the jitter of the ADPLL [101]. The ADPLL works in 2 loops- main loop and calibration loop. At starting, the reference signal Clk_ref with period of '40 ns' and Clk_fd (generated by the ADPLL) is given calibration loop, lock detection circuit and main loop. The signal pw is used to send calibration loop to reset mode and initially it is at logic '0'. The calibration loop brings the VCO frequency to range of 1.6 GHz and concurrently, the main loop is in the locking process. After VCO frequency comes to range of 1.6 GHz and ADPLL gets into the locked condition, the signal pw is generated by lock detection circuit and it becomes high. The calibration loop goes to 'reset' mode and the earlier value of out[7:0] is hold by D-flip-flop DFF after the signal pw becomes logic '1'. The proposed ADPLL is working in main loop in parallel to calibration loop. The output e[2:0] of 3-bit flash TDC is given to the proportional integral (PI) filter [19] and it scales the output of TDC and provides the control word Fcw [7:0]. The 8-bit DAC1 is used for coarse tuning and DAC2 for fine tuning of the proposed VCO. In two different loops, DAC1 and DAC2 work continuously and independently and control the VCO-II. Though, DAC1 holds the value of control word using signal pw, once the ADPLL-III is locked. After being locked, ADPLL in the locked state is maintained by the DAC2 in the main loop. The control voltage V_{fine} is generated by control word Fcw [7:0]. The control voltage V_{fine} is used to modify the frequency of proposed VCO-II with fine resolution of 160 kHz/mV. For output frequency of 1.6 GHz and for periodic of 2 ps, the coefficients of loop filter are α and β are taken with values 2^{-7} and 2^{-8} respectively. The typical PI filter is used in ADPLL-III design [59]. The calibration loop is sent to reset mode by signal pw for reducing the power consumption. The V_{coarse} is generated by control word out[7:0] from calibration unit and it settles at 520 mV. The lock detection circuit consists of D-flip-flops (DFF_LD1, DFF_LD2, DFF_LD3, and DFF_LD4), and gates (OR1 and AND1). The reference signal Clk_ref and feedback signal Clk_fd is given to DFF_LD1, DFF_LD2, DFF_LD3, and DFF_LD4 which check the rising edges of reference and feedback clocks. The D-flip-flop DFF_LD1 and DFF_LD2 generate an up and dn signals which are given to DFF_LD3 and DFF_LD4 respectively. The D-flip-flops DFF_LD3 and DFF_LD4 are sampled by Clk_ref & Clk_fd and outputs of DFF_LD3 and DFF_LD4 are given to the OR1 gate which generates signal pw. The logic gate AND1 is used to reset the DFF_LD1 and DFF_LD2 when the Clk_ref and Clk_fd are at logic '1'. When the reference Clk_ref and feedback Clk_fd are in phase, pw becomes 1; otherwise, it is at logic '0'. The error e[2:0] becomes constant and remains unchanged after the ADPLL-III is locked. When the ADPLL-III is locked, the signal pw becomes the logic '1' and Clk_ref and Clk_fd is cut off and calibration unit goes to reset mode while ADPLL-III is working in the main loop. The 8 D-flip-flops (DFF) are used to hold the value of control word outd [7:0] until the ADPLL-III comes

out of lock state. The output of SAR TDC is shown in the Fig. 7.6 (a). The SAR TDC shows that for the delay difference of 9 ps, the output is represented as '7H'. Fig. 7.6 (b) shows the output of ADPLL-III. It is observed that for maximum input delay difference, the output is '7H'. For minimum delay difference between Clk_ref and Clk_fd, the output is '1H'. The signal pw in logic state '0' during the calibration process. Once the calibration is over, the signal pw goes to logic state '1'. If ADPLL-III comes out of lock, pw becomes '0', once more calibration loop starts and multiplexer MUX_C2 allows the Clk_ref/4 to update the control word out[7:0] and updated control word vary the frequency of VCO-II until ADPLL-III gets into lock state.



(a)



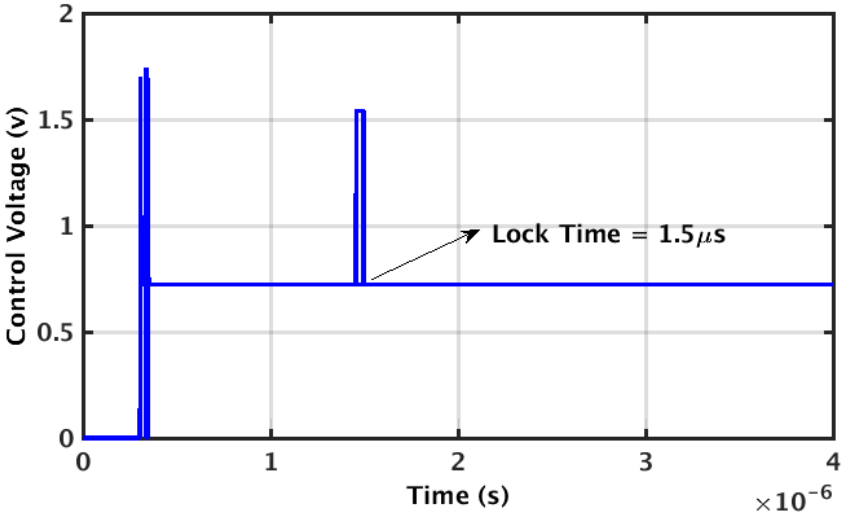
(b)

Fig. 7.6 (a) Output of SAR TDC, (b) Output of ADPLL-III

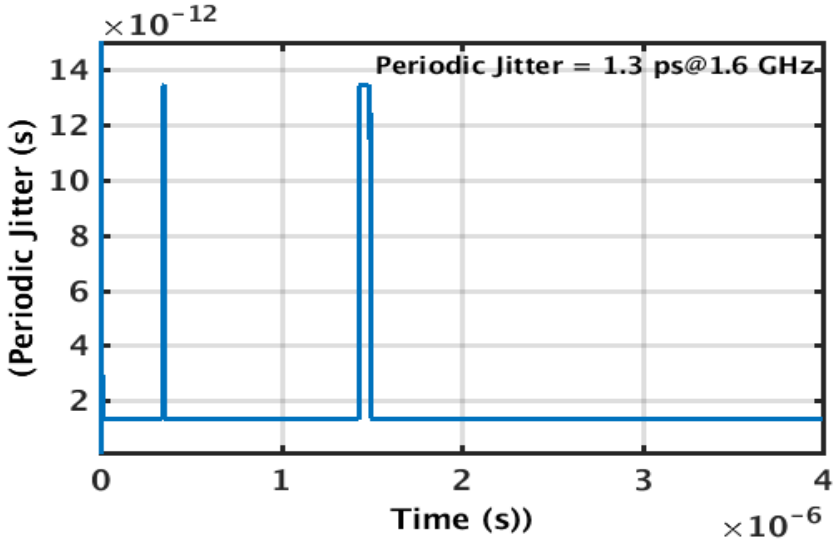
This technique reduces the overall power budget of ADPLL-III design. The proposed ADPLL-III design achieves a fast locking, low power, and low periodic jitter. The proposed ADPLL-III architecture achieves low power of 5.3 mW and low periodic jitter of 1.83 ps. The following section shows the simulation results of proposed ADPLL-III.

7.6 Simulation Results of ADPLL-III

This section shows the simulation results of the proposed ADPLL-III. Fig. 7.7 (a) shows a locking time of ADPLL-III and lock time is 1.5 µs. The background calibration based VCO-II affects the locking time of ADPLL-III. Fig. 7.7 (b) shows the achieved periodic jitter of 1.3 ps of proposed ADPLL-III. The Fig. 7.7 (c) shows the power consumption by different blocks of ADPLL-III.



(a)



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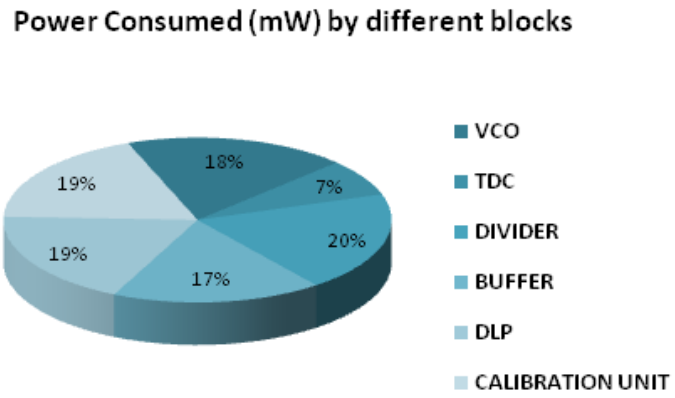

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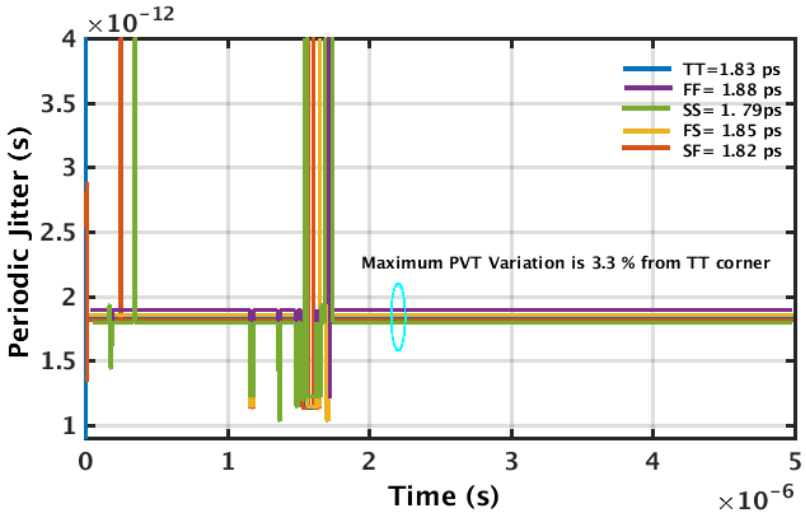

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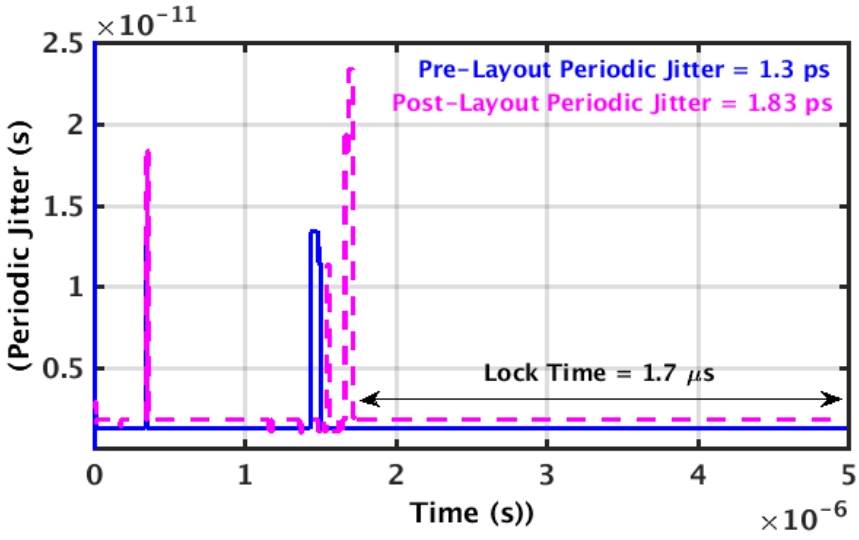

(e)

Fig. 7.7 (a) Lock time of ADPLL-III, (b) Periodic jitter of ADPLL-III, (c) Power consumption by ADPLL-III, (d) PVT variation of periodic jitter in ADPLL-III, (e) With calibration - pre and post layout periodic jitter of ADPLL-III

The RMS jitter of proposed ADPLL-III is 0.3 ps. The Fig. 7.7 (c) shows the power consumption by different blocks of ADPLL-III. Fig. 7.7 (d) show the PVT corner variations in periodic jitter with calibration for ADPLL-III design. The maximum variation in periodic jitter is 3% at FF corner with respect to TT corner. It is observed that PVT variation in ADPLL-III without calibration is 22.9% as shown in Fig. 7.1 (b) and in latter case with calibration, it is only 3.3%. The increase in pre-layout and post layout values of periodic jitter is 6.5% as shown in the graph in Fig. 7.7 (e). The periodic jitter is increased due to the parasitic addition after post layout simulations. Table 7.2 shows the periodic jitter variation in the proposed ADPLL-III. The maximum observed PVT variation is 3% and 2.3% at FF and SS corner respectively with respect to TT corner. The figure- of-merit FoM is given by [47]:

$$FoM = 10\log(RMSJitter^2 * \frac{Power}{1m}) \tag{7.18}$$

Table 7.2: PVT variations in periodic jitter across different corners

PVT Corners	Periodic Jitter (ps)
TT	1.83
FF	1.85
SS	1.79
FS	1.83
SF	1.82

Table 7.3: Achieved performance parameters of ADPLL-III

Parameters	Proposed ADPLL-III
Supply Voltage (V)	1.8
PLL Output Freq. (GHz)	1.6
Resolution (ps)	3
Periodic Jitter (ps)	1.83
Reference Frequency (MHz)	25
Locking Time (μs)	1.7
Power Consumption (mW)	5.3
Division ratio	64
FoM (dB)	-242.7
Technology Process (nm)	180

The (FoM) factor of proposed ADPLL is -242.7 dB. Table 7.3 shows the achieved parameters of ADPLL-III. The next section concludes the ADPLL-III design.

7.7 Conclusion

ADPLL-III architecture with VCO-II background calibration is presented in this chapter. The major aim of this work is to obtain the low periodic jitter, low power, and PVT insensitive ADPLL. This design incorporates a 3-bit flash TDC, low phase noise, and low power background calibration based VCO-II. The novel low phase noise and low power VCO-II with calibration is used to achieve a fast locking and low jitter ADPLL-III. The achieved resolution of 3-bit flash TDC is 3 ps. The power consumption of the ADPLL-III is 5.3 mW at 1.6 GHz. The ADPLL-III is designed in the CMOS 180 nm SCL technology at 1.8V. The achieved periodic jitter of ADPLL-III is 1.83 ps. The phase noise of VCO-II is -153dBc/Hz. The comparative analyses of proposed ADPLL designs are shown in the Table 7.4. The proposed ADPLL architectures show the lower power consumption and improved periodic jitter for the 1.6 GHz output frequency range.

Table 7.4: Shows relative performance parameters of ADPLL-I, ADPLL-II, and ADPLL-III with existing works

Parameters	ADPLL -III	ADPLL -II	ADPLL -I	[35]	[65]	[66]	[102]
Supply Voltage (V)	1.8	1.8	1.8	1.8	1.2	1.2	1.2
Frequency Output (GHz)	1.6	1.6	1.6	0.14~1.45	1.5–2.05	1-2	0.148 -1.45
Resolution (ps)	3	3	6	1	5.1	-	-
Periodic Jitter (ps)	1.83	1.71	6.6	21.9	1.07	7.5	-
Locking Time (μs)	1.7	3.1	1	7.57	20	5	-
Power Consumption (mW)	5.3	5.94	6.35	18.2	4	10.8	48.5
Technology Process (nm)	180	180	180	180	55	65	65
Reference Frequency (MHz)	25	25	25	-	24	50	-
Division Ratio	64	64	64	-	85	40	-

The frequency spacing is 25 MHz of proposed ADPLL-I, ADPLL-II, and ADPLL-II. The proposed ADPLL-I, ADPLL-II, and ADPLL-III have lower power consumption as compared to design reported in the [35]. It is observed from Table 7.4 that proposed ADPLL-I have fast locking time and improved jitter as compared to other designs reported in [65-66]. Though proposed ADPLL-II has more jitter as compared to other design in [65], but it has lower power consumption, locking time, and higher resolution. The locking time is 3.1 μs of proposed

ADPLL-II which is improved as compared to works reported in [102]. ADPLL-I has shown better performance parameters like lock time and power consumption as compared to other existing designs. As compared to [102], the power consumption is reduced in the proposed ADPLL-I, ADPLL-III, and ADPLL-III architectures. The proposed ADPLL-II has lower power consumption and improved periodic jitter as compared to ADPLL-I. ADPLL-I has fast locking time for output frequency of 1.6 GHz. The fast locking time is obtained due dual loop architecture of ADPLL-I. ADPLL-I design has periodic jitter of 6.6 ps and power consumption of 6.35 mW and lock time of 1 μs whereas ADPLL-II has lower periodic jitter of 1.71 ps and power consumption of 5.94 mW. There are number of tradeoffs exist for designing a realistic ADPLL designs. The designing a low power and low jitter ADPLL is big challenge as reducing jitter leads to design ADPLL with more power consuming blocks like TDC because for low jitter, a high resolution TDC is required which need more power. In order to have low jitter ADPLL, low jitter VCO is required which consumes more power. Also, for fast locking, wider loop bandwidth is required but wide loop bandwidth degrade the jitter performance. ADPLL-III shows better performance for power consumption as compared to earlier designs. The proposed ADPLL-III has locking time of 1.7 μs which is improved as compared to [65-66]. The low power consumption of 5.3 mW and periodic jitter of 1.83 ps is achieved for ADPLL-III design. These proposed ADPLL designs are suitable for battery operated, SoC, and wireless transceiver applications.

CHAPT ER 8

CONCLUSION AND FUTURE SCOPE

8.1 Conclusion

In this thesis, the analysis and design of digital and all-digital phase locked loop architectures for frequency synthesis for high-speed, battery-operated devices, SoCs, and wireless transceivers are presented. It has been shown in the work that TDC significantly impacts the overall power budget of an ADPLL design. To tackle issues of low resolution, high power, more area, and low speed, two 3-bit and 4–bit flash based TDC's are proposed. The 4-bit and 3-bit flash TDCs achieves a fine resolution of 6 ps and 3 ps respectively. To tackle the issues of PVT variations, digital calibration is used. Also, the periodic jitter achieved by 4-bit and 3-bit flash TDCs are 0.75 ps and 0.46 ps respectively. Highly standard cell methodology is used to design DPLL-II which makes this design portable and portable to other technologies. overall, the DPLL-II outperforms a DPLL-I in terms of locking time. However, DPLL-I and DPLL-II achieve a better result but still have portability and scalability is problem. Also, due to usage of analog blocks like charge pump, filter, and VCO, DPLLs suffer from leakage currents, PVT variations and requires a more design efforts. Further a low jitter and low power ADPLL are designed to tackle above said problems.

The two architectures for charge pump based Digital PLLs (DPLL-I and DPLL-II) have been proposed. Generally, a gate based VCO draws more power in overall DPLL design. Therefore, a low power, and low phase noise gate based VCO-I is designed for the DPLLs. The proposed VCO-I achieves a periodic jitter of 0.2 ps, a phase noise of -137dBc/Hz and power consumption is 1.43 mW. The proposed DPLL-I achieves low power of 2.3 mW, locking time of 2.8 μs and periodic jitter of 0.642 ps at the output frequency of 1.6 GHz. DPLL-II achieves the power consumption of 2.63 mW and periodic jitter is 5.1 ps with the locking time of 2.5 μs which is better as compared to DPLL-I.

The novel low power ADPLL-I design is proposed which achieves a low power, low jitter and fast locking time. ADPLL-I is dual path ADPLL with low power and high resolution TDC1 and TDC2. However, flash TDC suffers from PVT variations, therefore, digital calibration is used in ADPLL designs to tackle a problem of PVT variations. The proposed 4-bit flash TDC2 with calibration achieves a low periodic jitter of 0.61 ps and the power consumed by the TDC2 with calibration is 0.39 ps. The proposed ADPLL-I achieves low periodic jitter of 6.6 ps and power consumption is 6.35 mW with locking time of 1 μs. To enhance the results of ADPLL-I, novel ADPLL-II with 3-bit flash TDC and Bang Band PFD. ADPLL-II design requires the wide range TDC but it is challenge in the flash architecture.

Therefore, dual loop architecture is proposed which solves the limited dynamic range issue of ADPLLs. Another version of ADPLL is designed (ADPLL-II) which uses proposed bang-bang PFD and 3–bit flash TDC to achieve low jitter, fast locking, and low power ADPLL design. The 3-bit flash TDC with calibration has achieved a periodic jitter of 0.15 ps with fine resolution of 3 ps which is suitable for ADPLL-II architecture. ADPLL-II achieves periodic jitter of 1.71 ps with power consumption of 5.94 mW and locking time of 3.1 µs. The generic ADPLL-III is designed with background calibration of VCO-II to achieve low jitter, low power, PVT variations, and fast locking time. With proposed VCO-II having low phase noise and low power enhances the performance parameters of novel ADPLL-III. The simulation results of VCO-II shows that it has low power consumption of 0.9 mW and periodic jitter as 0.2 ps. Using this, the proposed ADPLL-III achieves a periodic jitter of 1.83 ps and the locking time of 1.7 µs with the power consumption of 5.3 mW. ADPLL-III achieves an improved power and locking time parameters as compared to the ADPLL-I and ADPLL-II. The periodic jitter is also improved as compared to ADPLL-I though it has slightly higher as compared to ADPLL-II.

In summary, this thesis presents design and analysis of different flash TDC architectures for low power, high resolution and fast locking ADPLL designs. Further, different novel ADPLL architectures are proposed to achieve low power, low periodic jitter, and fast locking and tackle PVT related issues. These proposed architectures are suitable for applications involving SoCs, wireless transceivers, and battery-operated devices.

8.2 Future Scope

The work and results of DPLLs and ADPLLs architectures are presented in this thesis but still few research problems for future work can be taken. The digital design methodology gives many advantages over the analog process like low cost and less design to market time. It also tackles the technological issues in newer technology nodes like leakage currents, PVT variations, and mismatches. The following points show the scope of future work which can be done:

1. Firstly, in the present work, ADPLL designs are implemented in the digital flow using digital tools but designing the all-digital synthesizable ADPLL is still challenge. The FPGA implementation of all-digital PLL requires a lot of attention. FPGA implementation of ADPLL provides easy, configurable ADPLL design which saves lot of time and design effort to design ADPLL.
2. Secondly, DCO designs in the present work are designed using DAC and VCO. The non-linearity of DAC degrades the performance of ADPLLs. Other challenge is to

achieve DCO with high resolution and low power and low area. New techniques can be proposed to achieve a high resolution and low power DCO. Also, to achieve the DCO functionality using the synthesizable flow is design challenge. The digital tools limit the implementation of DCO. Therefore, this design challenge leaves lot of work that can be taken as research problem.

3. The present ADPLL architectures have achieved an improved results but still further enhancement of present results can be done. Designing wide range in nanoseconds and high resolution TDC requires a lot of research. The reported works of TDC shows a complex architecture which requires more power and silicon area. The present work has achieved the high resolution 4-bit TDC2 and 3-bit TDC but with limited dynamic range. Therefore, more research can be done to achieve wide range, low power, and high resolution TDC.
4. ADPLL-III shows better results for power, locking time, and jitter but the architecture is little complex. Further work can be done to simplify the architecture and achieve further enhanced results for wireless transceiver applications.

LIST OF PUBLICATIONS

SCI Publications:

1. Jagdeep Kaur Sahani, Anil Singh, Alpana Agarwal, "A 2.3 mW Multi-frequency Clock Generator with -137 dBc/Hz Phase Noise VCO in 180nm Digital CMOS Technology," Journal *of Circuits, Systems, and Computers*, vol. 29, no. 8, pp. 2050130-1-15, **2020**. **(Impact factor -1.33)**
2. Jagdeep Kaur Sahani, Anil Singh, Alpana Agarwal, "A Wide Frequency Range Low Jitter Integer PLL with Switch and Inverter based CP in 0.18 µm CMOS Technology," *Journal of Circuits, Systems, and Computers*, vol. 29, no. 9, pp. 2050142-1-22, 2020. **(Impact factor -1.33)**
3. Jagdeep Kaur Sahani, Anil Singh, Alpana Agarwal, "A Fast Locking and Low Jitter hybrid ADPLL Architecture with Bang Bang PFD and PVT calibrated Flash TDC," *AEU-International Journal of Electronics and Communications*, vol. 124, pp.153344-1-10, 2020. **(Impact factor -3.183)**
4. Sahani, J.K., Singh, A. & Agarwal, A.," A 1 µs Locking Time Dual Loop ADPLL with Foreground Calibration-Based 6 ps Resolution Flash TDC in 180 nm CMOS," *Circuits Syst Signal Process vol.* **41, pp.**1299–1323, 2022. **(Impact factor -2.225)**
5. Sahani, JK, Singh, A, Agarwal, A., "A low jitter and fast locking all digital phase locked loop with flash based time to digital converter and gain calibrated voltage controlled oscillator," *Int J Circ Theory Appl.* pp. 1- 13, 2022. **(Impact factor -2.038)**

International Conference Publications:

1. Jagdeep Kaur Sahani, Anil Singh and Alpana Agarwal, "A High Resolution and Low Jitter 5-bit Flash TDC Architecture for High Speed Intelligent Systems," in Proceedings of *International Conference Intelligent Systems*, London, UK, 2019, pp. 266-278.

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