“Performance analysis of center to center separation between adjacent tubes of Single-Walled Carbon Nanotubes bundle as VLSI Interconnects”

Dissertation submitted towards the partial fulfillment of requirement for the award of degree of

Master of Technology

In

VLSI Design

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July 2016

CERTIFICATE & DECLARATION

I hereby declare that the work which is being presented in the dissertation titled **"Performance analysis of center to center separation between adjacent tubes of Single Walled Carbon Nanotubes bundle as VLSI Interconnect"** in the partial fulfillment of the requirement for the award of the degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out as under guidance of **Dr.Karamjit Singh Sandha** (Assistant Professor, ECED) during 2014-2016.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENT

It is my proud privilege to acknowledge and extend my gratitude to several persons who helped me directly or indirectly in completion of this report. I express my heart full indebtedness and owe a deep sense of gratitude to my teacher and my faculty guide **Dr. Karamjit Singh Sandha** for their sincere guidance and support with encouragement to go ahead.

I am also thankful to **Dr. Sanjay Sharma**, Professor and Head, Electronics and Communication Engineering Department, for providing the adequate infrastructure for carrying out the work along with the motivation that inspired me for this work.

I would also like to thank my friends who have more or less contributed to the preparation of this report. I will be always indebted to them. Last but not the least, I would like to thank my parents for their years of unyielding love and encourage. They have always wanted the best for me and I admire their determinations and sacrifices.

The study has indeed helped me to explore knowledge and avenues related to my topic and I am sure this will help me in my future.

Gaurav

ABSTRACT

The work in this report presents the application of Carbon nanotubes (CNTs) as a VLSI interconnect and its superiority over copper interconnect at 32, 22 and 16 nm technology nodes. CNTs are the promising candidates for the future interconnects and it is always used in the bundle form because the resistance offered by an isolated CNT is very high. The advantage of using carbon nanotubes as a bundle form is that the effective resistance get divided by number of CNTs in a bundle and as a result of this, the resistance decreases. The impedance parameters of a CNT bundle depend on the number of CNTs in a bundle. CNTs can outperform copper at the intermediate and global interconnect level. The SWCNT bundle is most desirable form of CNT based interconnect provided all constituent CNTs of the bundle are metallic.

All the impedance parameters have been calculated by writing the script in MATLAB. It has been observed that all the impedance parameters are directly proportional to the length of interconnect. It is also observed that the resistance and inductance of interconnect increases with the decrease in technology node whereas it is reverse for capacitance.

Further, the effect of center to center separation of adjacent tubes have been analyzed. A mathematical model is presented which include the effect of center to center shell distance for different technology nodes. The effect of separation of adjacent tubes in a SWCNT bundle plays an important role in the interconnect delay and power dissipation. The delay increases with an increase in the separation between adjacent tubes for the entire range of length values and tube diameters but the opposite is true for power dissipation i.e power dissipation decreases with increase in separation. Furthermore, by using equivalent single conductor model, the propagation delay and power dissipation are simulated using spice simulation tool. The Optimum CMOS driver size and effect of repeaters on a SWCNT interconnect has been analyzed. It is shown in the results that the influence of center to center separation of adjacent tubes on a SWCNT bundle has a considerable impact on the propagation delay and power dissipation. It is also observed that as the bundle density is decreased the corresponding delay increases but at the same time power dissipation decreases.

TABLE OF CONTENTS

LIST OF ACRONYMS

IC	Integrated Circuit
VLSI	Very large scale integration
CNT	Carbon Nanotube
SWCNT	Single-Walled Carbon Nanotube
MWCNT	Multi-Walled Carbon Nanotube
ESC	Equivalent Single Conductor
MFP	Mean free path
MCB	Mixed Carbon nanotubes
SPICE	Simulation program with integrated circuit emphasis.
ITRS	International technology roadmap for semiconductors

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 INTRODUCTION

Interconnects act as a path for the signals propagating in an integrated circuit connecting one node to the other node and also provide connection to the nodes of one block to the nodes of other block. Basically, it is a conducting material of thin film [2] which is used to provide an electrical connection between one node of a circuit to the other node of a circuit. There are three types of interconnects: local, intermediate, and global.

• Local interconnects are used for connecting gates, and transistors within a functional block They consist of very thin film. The length of local interconnect is about few micrometers .

• Intermediate interconnects are used to provide connections within the functional block but are larger in length than local interconnects with a range of few hundreds of micrometers to 1 mm. They've the ability to provide low resistance path.

• Global interconnects are used to provide electrical connection from one functional block to the other block. The length of global interconnect is from 1 mm to few mm.

In early days aluminum was used as an interconnect material because of its following advantages [3]

- Low resistivity
- Good Conductivity
- Ease of deposition
- Dry etching
- Does not contaminate Si
- Excellent adhesion to dielectrics.

It also forms good ohmic contact with silicon. Despite of its goodness it also has certain disadvantages:-

- Electro-migration
- Higher resistivity
- Short mean free path of the order of few nanometers.

As we move down toward technology scaling [1], current density of the interconnect is increased. At higher current densities electro-migration [4,5] (it is the transportation of material due to the movement of the ions in a conductor) takes place.

1.1 Copper interconnect

As the electro-migration [7] problem in aluminum was troubling the performance of interconnect at μm technologies, there was a dire need of better interconnect. So copper came as a strong contender for interconnect which has higher conductivity and has less issues of electro migration than aluminum [28]. Because of the advantages of copper over aluminum it appeared as a widely used metal for interconnect, particularly for the IC's which demands high performance. The basic structure for copper interconnect is shown in Fig.1.1.

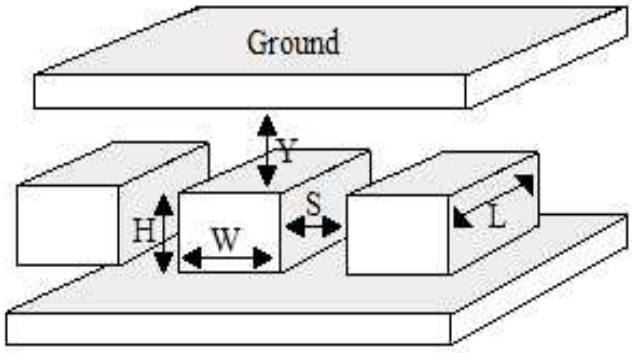

Fig.1.1 A basic copper interconnect structure [39]

1.1.1 Resistance of copper interconnect

The resistance associated with the copper interconnect depends on the resistivity of copper, it varies directly proportional with resistivity as well as its length. However, it is inversely proportional to the area of copper interconnect. So the analytical expression for the resistance can be written as

$$R = \frac{\rho . L}{W . H} \tag{1.1}$$

where ‘ρ’ represents the resistivity of copper and ‘L’ is the length of interconnect. ‘*W*’ and ‘*H*’ denotes the width and height of copper interconnect respectively.

1.1.2. Inductance of copper interconnect

The inductance coupled with copper interconnect is due to the changing current in it. A magnetic field is produced by the action of this changing current which in turn produces a voltage in the circuit, therefore an inductance is produced which is known as self inductance (L_S) [8] and is given by the equation.

$$L_S = \frac{\mu.L}{2\circledR}\left[\ln\left(\frac{2L}{W+H}\right)+\frac{1}{2}\left(\frac{0.22(W+H)}{L}\right)\right] \tag{1.2}$$

where ‘μ’ is the permeability of copper.‘*W*’,‘*H*’ and ‘*L*’ are the width, height and length of copper interconnect respectively.

1.1.3. Capacitance of copper interconnect

On scrutinizing the interconnect structure of copper in Fig.1.1, it is lucid that it is fixed at distance ‘*Y*’ above the ground plane. This separation ‘*Y*’ is filled with a dielectric material of permittivity ‘ε’. As a result, interconnect and the ground plane behaves as the conducting plates of a capacitor. When the signal is passed through the interconnect it acquires some charge and act as parallel plate capacitance. Nevertheless, the thickness of the interconnect is quite evident therefore creating fringing electric fields which contributes to another type of capacitance known as fringing capacitance. Consequently, the total capacitance (C_g) of copper interconnect is the addition of parallel plate capacitance and fringing capacitance, which is given by the equation (1.3).

$$C_g = \varepsilon\left[\frac{w}{Y}+2.22\left(\frac{S}{S+0.7Y}\right)^{3.19}+1.17\left(\frac{S}{S+1.15Y}\right)^{0.76}\left(\frac{H}{H+4.53Y}\right)^{0.12}\right] \tag{1.3}$$

In equation (1.3) '*W*' and '*H*' is the width and height of copper interconnect respectively whereas 'S' is the spacing , '*Y*' is the height above ground and 'ε' is the permittivity [15]. These equations will be used for the calculating the impedance parameters of copper interconnect. Previous studies have proved that copper is still a good choice for interconnect at local length and for technology nodes above 45 nm. However, when the technology node is further degraded, the choice of copper as an interconnect could be a wrong choice as it offers high resistivity at lower technology nodes.

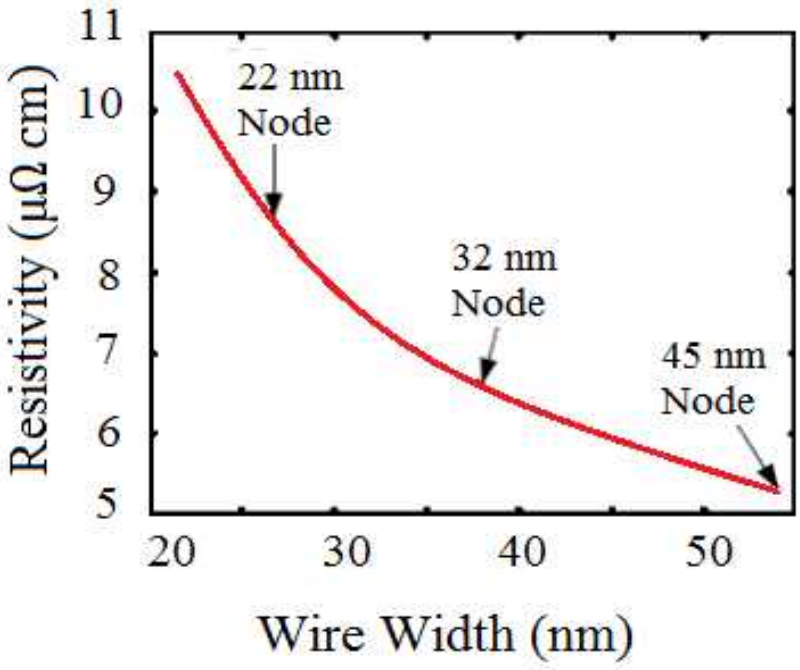

Fig.1.2. Resistivity of copper as a function of wire width at various technology nodes [10]

It is vivid from Fig.1.2 that resistivity of copper escalates exponentially when the technology node is reduced below 45 nm. It means the resistance of interconnect increases exponentially with the reduction of technology. When the feature size is reduced below 45 nm the enhanced grain boundary scattering and surface scattering [10,11] results in increase in scattering resistance of the interconnect. The interconnect delay is increased exponentially with the reduction of technology while the power dissipation of the circuit is not reducing at the same rate causing power per unit area to increase. Due to this problem, there is a dire need to replace copper as VLSI interconnects at global level. Researchers have proposed carbon nanotubes as a perfect material for the interconnects [12] and for the upcoming technology.

1.2 Carbon nanotubes

Carbon nanotubes (CNTs) are made up of an allotrope of carbon called graphene. It is fabricated by rolling graphene layers in the shape of cylinders. They have diameter in the range of nanometers that is why they have got the name nanotubes [18,19] . The CNTs will be either metallic or semiconducting and this depends on the direction in which the grahene layers are rolled up. Only the metallic CNTs participate in the current conduction [16,17] whereas the semiconducting CNTs are of no use and hence do not participate in current conduction. The growth of CNT is done in the shape of flawless cylinders and it's wall is formed by layer of graphene. As far as the research till now is concerned, carbon nanotubes have been proved to be the best interconnect material [21] for the integrated circuits manufacturing. They have shown extremely favorable results in terms of propagation delay at lower technology nodes.

1.2.1 Advantages of CNT over COPPER [20]

- High mechanical stability
- High thermal stability
- High thermal conductivity
- Large current carrying capacity
- Lower resistivity
- Mean free path of the order of 1000 nm.

Table.1.1 Comparison of properties of CNT and copper [3]

Properties	**CNT**	C**opper**
Mean free path (nm)	Greater than 1000	40
Maximum current density (A/cm^2)	Greater than 10^10	~10^6
Thermal conductivity (W/mK)	5800	385

Table.1.1 represents the properties of CNT and copper as an interconnect. It can be seen that CNT is superior to copper in terms of mean free path, maximum current density and thermal conductivity.

1.2.2 Classification of CNTs

CNTs are broadly classified under two categories,

- Single-walled carbon nanotubes (SWCNTs)
- Multi-walled carbon nanotubes (MWCNTs).

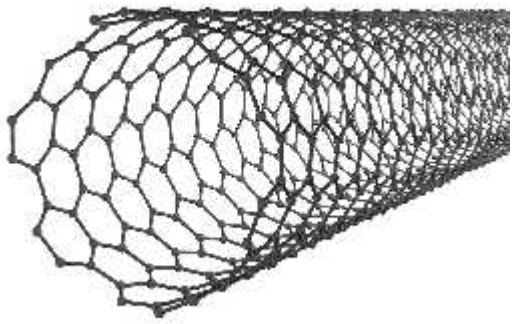

Fig.1.3 Single walled carbon nanotubes [7]

SWCNT is made up by rolling a thin layer of graphene and it consists of only one layer [6] while the MWCNT consists of multi layers (more than two layers) of graphene of different diameters rolled up in a concentric form. The SWCNT can be used as VLSI interconnects [7-9] because the electron mean free path [27] of SWCNT is more than 1000 nm which results in lower resistivity. Due to the high resistance linked with a single CNT which is more than 6.45 KΩ poses a restriction that we should use a bundle of CNTs which consists of large number of isolated CNTs in parallel. The number of shells in a MWCNT and number of metallic SWCNTs decides the impedance parameters MWCNT and SWCNT bundle respectively. In a SWCNT bundle, some of the nanotubes are semiconducting while others are metallic. Only metallic CNTs contributes to current conduction and formation of interconnect. The semiconducting CNTs never take part in the current conduction. Large numbers of CNTs in a multi-walled CNT are metallic. On the other hand a large number of CNTs in a SWCNT bundle are semiconducting. A MWCNT with two shells is double walled CNT. This form of

CNT has been found to be a very useful for application as interconnects. It is very difficult to achieve ballistic transport [29] for MWCNTs for a long length [10-11] whereas SWCNTs have mean free path of the order of a micron due to its diameter in nano range. SWCNTs has only one shell with diameter ranging from 0.33 nm to 5.0 nm and lengths from 2 nm to 10 nm, whereas MWCNTs has several concentric shells [39] with diameter ranging from several nanometers to tens of nanometers and length of several microns.

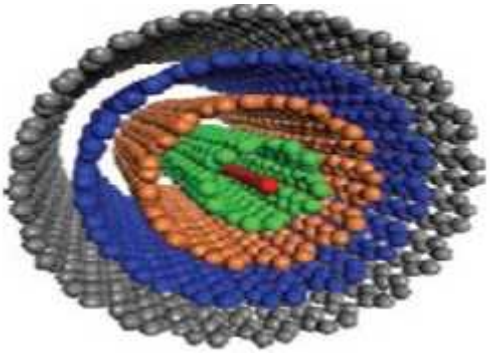

Fig.1.4. Multi-walled Carbon nanotubes [15]

On the basis of circuit simulation researchers reported that an SWCNT-bundle interconnect provides the low-resistivity advantage over copper when the bundle length is semi-global or global.

1.3. Equivalent Circuit Model for an Isolated Single Walled Carbon Nanotube

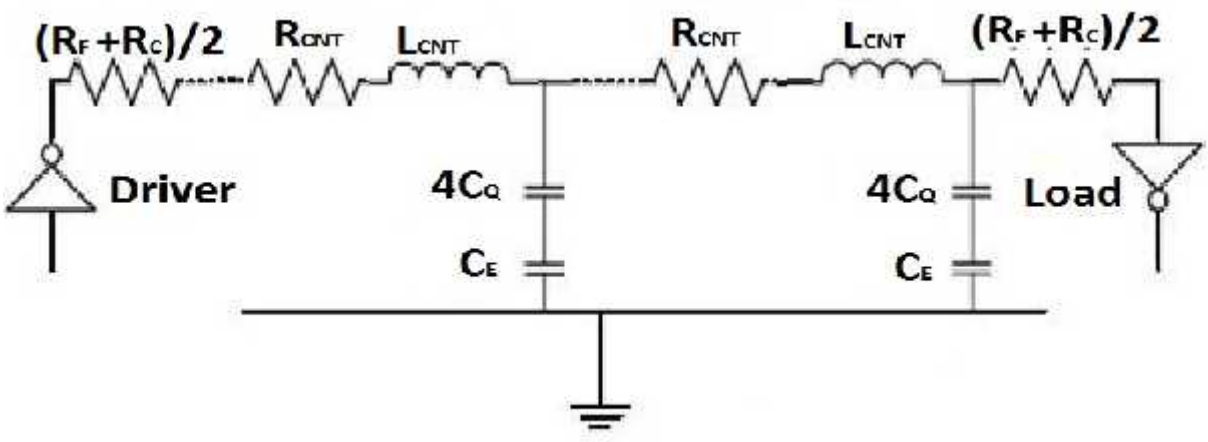

Fig.1.5. Equivalent Circuit Model for an Isolated Single Walled Carbon nanotube [10].

The equivalent circuit model for isolated single-walled carbon nanotubes is shown in Fig.1.5. The model and its components are explained in detail in the following subsections.

1.3.1 Isolated SWCNT Resistance

The conductance of a SWCNT is analyzed using the two terminal Landauer Buttiker formula. According to this formula, for a single dimension system with 'n' number of channels. The conductance is directly proportional to the number of channels [24,25]. Each carbon nanotubes has four number of conducting channels which results in a resistance of 6.45 KΩ. This is the quantum resistance also known as fundamental resistance is involved with the single walled carbon nanotubes. This resistance can't be avoided as is divided equally between two opposite sides of SWCNT.

$$R_F = \frac{h}{4e^2} \tag{1.4}$$

The mean free path (L_O) of carbon nanotubes is approximately equal to 1μm. The mean free path is defined as the distance travelled by an electron until scattering occurs. For SWCNT with interconnect length less than 1 μm, the fundamental resistance R_F is considered. For all the interconnects lengths larger than its mean free path i.e 1 μm, the scattering resistance R_{CNT} will also be included. The resistance of SWCNT increases when length of carbon nanotubes becomes larger than its mean free path. In addition to the fundamental resistance a scattering resistance [30] appears which depends upon length and MFP of SWCNT and can be written as given below in equation (1.5)

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{L_o} \tag{1.5}$$

In actual, the calculated resistance of CNT is much larger than the sum of fundamental and scattering resistance. This is because of imperfect contact of metal and carbon nanotubes, which is called contact resistance. The imperfect metal-carbon nanotubes contact resistance (R_C) of carbon nanotubes ranges from few ohms to 100 KΩ. Therefore it can be concluded that the total resistance is the sum of quantum resistance, scattering resistance and metal-carbon nanotubes imperfect contact resistance The total resistance offered by the isolated

single walled carbon nanotubes is very high. Therefore, it is required to use a bundle of carbon nanotubes as an interconnect. The advantage of using a SWCNT bundle as interconnect is that the total resistance gets divide by total numbers of CNTs in the bundle.

The total resistance of an isolated SWCNT can be written as

$$R_{Isolated} = R_F + R_C + R_{CNT} \tag{1.6}$$

1.3.2 Isolated SWCNT capacitance

The capacitance of Carbon nanotubes is from two sources. The first one is the electrostatic capacitance (C_E) which is calculated by considering the Carbon nanotubes as a thin wire, of diameter 'd', positioned at a distance 'y' above the ground plane. The electrostatic capacitance is calculated per unit length. It is reported to be 30 aF/um for y=1 μm and d=1 nm. Another capacitance which is involved with the isolated single walled carbon nanotubes is the quantum capacitance which is due to the quantum electrostatic energy stored in the nanotubes when it carries current.

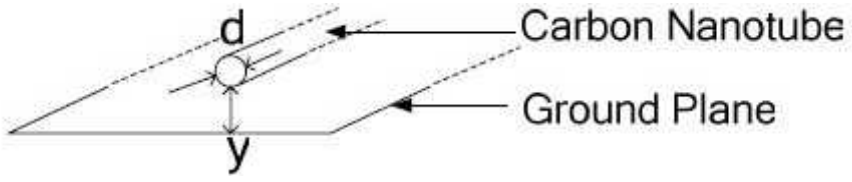

Fig.1.6. Isolated carbon nanotube with diameter 'd' placed at a distance 'y' above ground plane.[8]

$$C_E = \frac{2\circledR£}{\ln\left(\frac{y}{d}\right)} \tag{1.7}$$

$$C_Q = \frac{2e^2}{h v_F} \tag{1.8}$$

When this quantum electrostatic energy is equated to capacitance, the formula for quantum capacitance is realized and is shown in equation (1.7). This capacitance is also realized as per unit length. Here in equation (1.8) 'v_F' is the Fermi velocity and '*h*' is the Planck's constant. For a CNT the Fermi velocity is reported to be $8x10^5$ m/s. Thus, the quantum capacitance becomes equal to 100 aF/um. There are four conducting channel in a carbon nanotubes so the total quantum capacitance results from four parallel capacitances and is noted to be $4C_Q$. In the effective circuit model, both of the electrostatic quantum capacitance appears in series.

1.3.3 Isolated SWCNT Inductance.

The inductance of the isolated Single walled carbon nanotubes arises from two factors. First one is the magnetic inductance(L_M) and the second is the Kinetic inductance(L_K).the magnetic inductance is due to the magnetic field which comes into play when an isolated current carrying wire is placed at some distance above ground plane. The Kinetic inductance is due to the kinetic energy stored in each conducting channel. L_M is reported to be 1.4 pH/um when d=1nm and y=1µm. on the other hand L_K is known to be 16 nH/µm. L_K does have considerable impact on delay calculation of interconnects. The formula for L_M and L_K is shown below in equation (1.9) and equation (1.10) represents the isolated SWCNT inductance

$$L_M = \frac{\text{«}}{2\text{®}} \ln\left(\frac{y}{d}\right), L_K = \frac{h}{2e^2 v_F} \tag{1.9}$$

$$L_{CNT} = L_K + L_M \tag{1.10}$$

1.4 SWCNT as a bundle

A bundled SWCNT consists of a large number of SWCNTs. The SWCNTs inside a bundle are arranged in parallel. The inter-CNT distance between one CNT and the other CNT is 0.34 nm. This is the minimum distance that must be maintained between CNTs. This distance is known as vander-wall gaps [33,34]. The diameter of SWCNT is typically about 1 nm. In Fig.1.7 a view of SWCNT bundle is shown. Some SWCNT bundle parameters are shown like '*x*' which is center to center distance of CNTs. H_B is the height of SWCNT bundle and W_B is

the width of the bundle and '*d*' is the diameter of a single CNT inside the bundle. The bundle is placed at a height h_t above the ground plane.

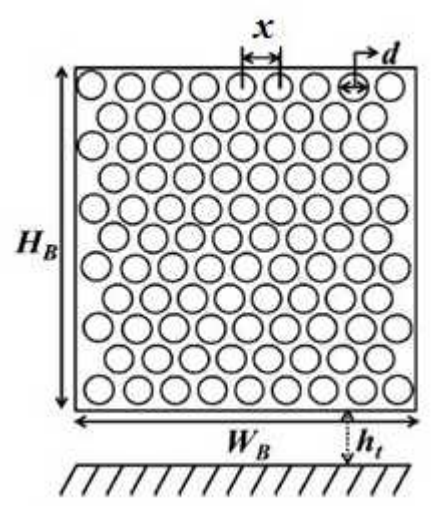

Fig.1.7. SWCNT Bundle placed at a height h_t above the ground plane [18]

The total number of SWCNTs in a bundle can be calculated by following equations (1.11) and (1.12)

$$n_{CNT} = n_W n_H - \frac{n_H}{2},\ If\ \ n_H\ is\ even \tag{1.11}$$

$$= n_W n_H - \frac{n_H - 1}{2}\ ,\ If\ \ n_H\ is\ odd \tag{1.12}$$

Where

$$n_W = \frac{W_B - d}{x} \quad \text{and} \quad n_H = \frac{H_B - d}{\frac{\sqrt{3}}{2}x} + 1$$

where '*d*' is the diameter of Single walled carbon nanotubes and '*x*' is the distance between center to center of the neighboring tubes of the SWCNT bundle. n_H indicates the number columns and n_W indicates the number of rows in a single walled carbon nanotubes bundle. n_{CNT} denotes the total number of carbon nanotubes in the bundle

1.5 Equivalent model for SWCNT bundle

The equivalent circuit model for SWCNT bundle is presented in Fig.1.8. In this Figure, the $R_{CNT} / n_{CNT,} L_{bundle}, C_Q^{bundle}$ and C_E^{bundle} are the distributed parameters.

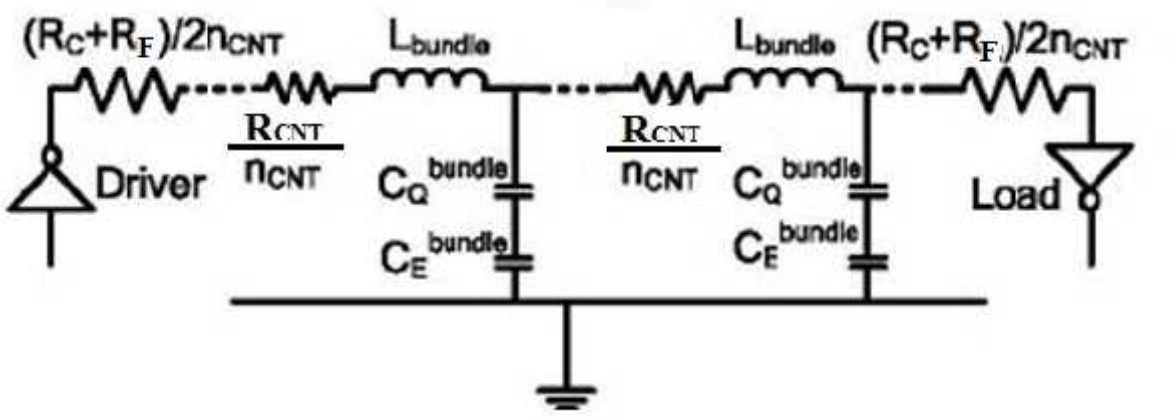

Fig.1.8 Equivalent model for SWCNT bundle [9]

1.5.1 SWCNT bundle resistance

For calculating the effective resistance of a single walled carbon nanotubes bundle, it has been assumed that all the CNTs in the bundle are metallic in nature and are supposed to be conducting. The SWCNT bundle resistance is shown below in equation (1.13). Here in equation (1.13) n_{CNT} is the number of carbon nanotubes in a bundle and $R_{isolated}$ is the isolated carbon nanotubes resistance.

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} \tag{1.13}$$

1.5.2 SWCNT bundle capacitance

Single walled carbon nanotubes bundle effective capacitance is the addition of quantum capacitance and electrostatic capacitance. The effective electrostatic capacitance of the SWCNT bundle is shown in equation (1.14). The total effective capacitance [20,21] of bundle of SWCNT is given by equation (1.16), where C_E^{Bundle} and C_Q^{Bundle} are the total electrostatic capacitance and total quantum capacitance of SWCNT bundle. C_{En} and C_{Ef} are

the intrinsic plate capacitances and n_W and n_H are the number of columns and number of rows in an interconnect bundle. The total electrostatic capacitance of the bundle is given by equation (1.14)

$$C_E^{bundle} = 2C_{En} + \frac{n_W - 2}{2} C_{Ef} + 3\frac{(n_H - 2)}{5} C_{En} \tag{1.14}$$

Here C_{En} and C_{Ef} are the intrinsic plate capacitances and n_H and n_W are the number of rows and number of columns in a single walled carbon nanotubes bundle respectively. Another capacitance which is associated with SWCNT bundle is the quantum capacitance [38]. Since the individual quantum capacitances of the carbon nanotubes are in parallel. So, the total quantum capacitance is the sum of all the isolated quantum capacitances of all the carbon Nanotubes forming a CNT bundle. The formula for the quantum capacitance of a CNT bundle is shown below in equation (1.15). Here C_Q^{CNT} is the quantum capacitance of an isolated single walled carbon nanotubes and n_{CNT} is the total number of CNTs in the bundle.

$$C_Q^{bundle} = C_Q^{CNT} . n_{CNT} \tag{1.15}$$

The net capacitance of SWCNT bundle is calculated by the series combination of quantum and electrostatic capacitance and is given by C_{bundle} in the equation (1.16) below.

$$\frac{1}{C_{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}} \tag{1.16}$$

1.5.3 SWCNT bundle Inductance

The SWCNT bundle inductance is given by the parallel combination of the magnetic and kinetic inductance. Since L_K (Kinetic inductance) is large enough as discussed earlier so it is excluded from delay calculations [36]. Isolated SWCNT is given by $L^{CNT} = L_K + L_M$. Thus the total SWCNT bundle inductance can be calculated by dividing isolated SWCNT inductance by number of carbon nanotubes in a bundle, which is given by equation (1.17)

$$L_{bundle} = \frac{L_{CNT}}{n_{CNT}} \tag{1.17}$$

1.6 Thesis Organization

CHAPTER 1- A brief introduction and classification has been given about carbon nanotubes. Equivalent circuit models of isolated SWCNT and SWCNT bundle have been discussed.

CHAPTER 2- This chapter puts emphasis on the previous research papers related to performance of carbon nanotubes and its superiority over copper interconnect and also its use in future technologies

CHAPTER 3- Based on the literature survey, research gaps have been proposed which will form the basis of this report work.

CHAPTER 4- Based on the research gaps some objectives are defined and a methodology is proposed to attain the required objectives.

CHAPTER 5- This chapter deals with the results obtained for effect of center to center separation between adjacent tubes on performance of SWCNT bundle and its comparison with copper at various technology nodes.

CHAPTER 6- This chapter forms the conclusion of the report and the future scope of CNTs has also been discussed.

CHAPTER 2 LITERATURE REVIEW

Effect of scaling of interconnections on the time delay of VLSI circuits [1]

-Krishna C. Saraswat and Farrokh Mohammadi

They explained that the interconnect delay dominates the device delay. It is due to the reason that integrated circuit area is increased and the device dimensions are decreased simultaneously. In their paper they talk about scaling of integrated circuit and minimum feature size. Scaling means increase in IC size and reduction in minimum feature. The delay is associated with scaling. Analytical expressions are developed which can associate delay with a variety of physical parameters like the material used for the interconnect, interconnect length, minimum feature size and IC area. After that Empirical expressions are discussed. On the basis of Empirical expressions they have said that when the IC area is increased the interconnect delay becomes more important than device delay.

Optimal Interconnection Circuit for VLSI [2]

-H. B. Bakoglu et al.

This paper proposed that for observing the performance of a VLSI circuit, the propagation delay of interconnect is an important factor. When the IC size is enhanced and dimensions of interconnects are scaled the delay increases sharply. For calculating the delay they proposed a model which can give detail about the effects of scaling MOSFETs, interconnects and IC dimensions. They have presented a comparison of poly silicon interconnect and aluminum and also discussed about the interconnect delays of forthcoming VLSI circuits. By using repeaters the delay can be reduced. Others options for reducing delay are the use of cascaded drivers and appropriately scaled multilevel conductors. They have presented a model which can successfully reduce the propagation delay to a good extent because it uses most favorable interconnect parameters and repeaters.

Performance analysis of carbon nanotubes interconnects for VLSI applications [10]

-Navin Srivastava and Kaustav Banerjee

This paper talks about using single walled carbon nanotube (CNT) bundles as an interconnect for VLSI circuits, by keeping in mind the aspects where this technology can lack. They have proposed equivalent circuit model for both isolated single walled CNT and bundle of single walled CNTs. A comparison of copper interconnects and SWCNT bundle interconnects has been presented in terms of propagation delay at all different levels of interconnects. By this paper it can be concluded that single walled CNTS can perform better than copper at global and intermediate level while copper performance is outstanding as compared to single walled CNT bundle in terms of delay. The necessities that are required to carbon nanotubes feasible to use them as next generation interconnects were presented.

Control of SWCNT interconnect performance by tube diameter[17]

-Mayank Kumar Rai et al

They presented a study on the isolated CNT diameter inside a SWCNT bundle. The study talks about how the isolated CNT diameter can manipulate the bundle delay. Their study shows that because of the lower resistance of single walled CNT bundle interconnects, the delay is lower than copper interconnects. Delay increases directly proportional to the isolated CNT diameter. As the diameter increases the number of CNTs inside a bundle reduces which results in increase in resistance and hence increase in delay. So a minimum diameter of CNT must be chosen.

On the applicability of single-walled carbon nanotubes as VLSI interconnects [18]

-Navin Srivastava et al

This paper presented a detailed study on using of single-walled CNTs as interconnects for deep submicron integrated circuits. A complete study on the impedance parameters of SWCNT bundle interconnect is done. Various types of resistances involved with the interconnects have been discussed like quantum resistance, contact resistance and scattering

resistance. Two types of inductances are discussed namely magnetic inductance and kinetic inductance out of which kinetic inductance is not included in delay calculations because kinetic inductance is very greater than magnetic inductance and it has an important effect on delay calculations. Different kind of inductive effects are presented. Vias are discussed which are also known as vertical interconnects. It has been reported that the delay is reduced by 40% in global interconnects. After that it is shown that dense CNT bundles can perform better than spatially packed CNT bundles because number of CNTs increases in a densely packed CNT bundle. This in turns decreases the resistance of the bundle interconnect and hence the delay decreases. On the other hand number of CNTs in a bundle decreases in a spatially packed CNT bundle. So the resistance increases and hence the delay increases. When the delay increases the power dissipation decreases. So a trade off is required between them.

Analyzing Carbon Nanotube Interconnects in VLSI Application [20]

-Mahmudur Rahman, Ahrar Ahmed Chowdhury

In this paper the electrical properties of carbon nanotubes as an interconnect in VLSI circuits have been analyzed. Accordingly, the effectiveness of metallic SWNT interconnect has been studied using Raman spectroscopy for its outstanding ballistic conductivity, low resistance and low capacitance. The performance analysis of SWCNT bundle based on RLC parameters is discussed. Impact of Resistivity on MWCNT, SWCNT bundles with full and one-third metallic portion is studied and by using this result, the paper concludes that metallic interconnects is the future of VLSI technologies.

Performance Comparison between Single Wall Carbon Nanotubes Bundle and Multiwall Carbon Nanotubes for Global Interconnects [22]

-Manoj Kumar Majumder et al.

This paper proposed a full detail about the delay for single walled carbon nanotubes and multi-walled carbon nanotubes at different interconnect lengths. They have also specified number of carbon nanotubes required for a particular delay in a SWCNT and number of shells required for a particular delay in a MWCNT. By using one-dimensional fluid theory they have

revised the models of single walled CNTs and multi walled CNTs. Propagation delay is discussed for both the models at deep submicron technology. They have come to conclusion that it doesn't matter what type of CNT it is. The delay is directly proportional to the length of the interconnect. If same delay is required for single walled and multi-walled carbon nanotubes, then the number of single walled CNTs should be greater than the number of shells in a multi walled CNT.

Estimation of Time Delay and Repeater Insertion in Multiwall Carbon Nanotube Interconnects [24]

- Feng Liang, Gaofeng Wang, Wen Ding

This paper uses a finite difference time domain (FDTD) method on a derived equivalent single conductor model for interconnect line. Based on this a 50% time delay analysis is performed for a driver-interconnect-load structure using SPICE simulation. In this paper a CMOS gate is used as a driver for interconnect line. Based on the simulation results the impact on propagation time delay with the variation of length at intermediate length has been plotted for 14nm and 22nm technology nodes. Simulations are also carried to study the optimum number of repeaters needed by MWCNT and copper at 1000μm intermediate length and at 2000μm and 5000μm global length. The paper concludes that the propagation time delay in MWCNT is much less than that observed in copper at global, intermediate level. The number of repeaters used by MWCNT at a particular length is one third of that used by copper in order to reduce the time delay.

Comparison of Propagation Delay Characteristics for Single-Walled CNT Bundle and Multi-walled CNT in Global VLSI Interconnects [25]

-Manoj Kumar Majumder et al.

This paper presented a broad discussion of single-walled carbon nanotubes bundles and multi walled carbon nanotubes. The propagation delay is discussed at global interconnect lengths. They have also stated the area required for an equal number of single walled CNTs and

number of shells in a multi walled carbon nanotubes. They stated that it does not matter what is the type of CNT. The delay increases with increase in interconnect length. For the same delay, equal number of CNTs in SWCNT bundle and number of shells in MWCNT the area required for SWCNT bundle is more than MWCNT

Influence of distance between adjacent tubes on SWCNT Bundle interconnect delay and power dissipation [31]

-Mayank Kumar Rai and Sankar Sarkar

This paper analyzed the influence of separation between adjacent tubes in a single walled CNT bundle of various lengths and tube diameters, on power dissipation and delay of the bundle. Calculations have been done on the impedance parameters and the outcomes are compared with copper interconnects at 22nm technology node. SPICE simulations have been done and it is observed that if the distance between adjacent tubes inside a SWCNT bundle is increased then the delay is also increased in the same proportion. Its true for the entire range of length values and tube diameters whereas the opposite is correct for power dissipation.

Analysis of delay and dynamic crosstalk in bundled carbon nanotube interconnects [35]

-B.K Kaushik,Manoj Kumar Majumder and Sanjeev Kumar Manhas.

They explained that by mixing SWCNTs and multi-walled CNTs in an arranged fashion can form an interconnect which can provide solutions to many problems in deep submicron technology. Such types of structures are called mixed carbon nanotube bundles (MCBs). They have discussed different kind of random fashion structures and well arranged structures of MCBs. MCBs are formed by placing SWCNTs and MWCNTs inside a single bundle. After that an equivalent circuit model of the MCB has been discussed. Through this model, the dynamic crosstalk performance and propagation delay of the structures of MCBs are calculated. From the calculations it is seen that propagation delay as well as dynamic crosstalk are reduced to much extent. The reduction is more in a MCB if the constitutes are packed spatially and the MWCNTs are placed around the SWCNT bundles which are placed at the center of the MCB. When the well arranged MCBs are compared to the MCBs which contains SWCNTs in a random fashion the average delay is reduced in well arranged MCBs.

CHAPTER 3 RESEARCH GAPS

Carbon nanotubes as VLSI interconnect is an excellent candidate for the forthcoming IC design. The work presented in the literature shows that CNT can outperform copper and has the ability to replace copper in the field of interconnects.

As the technology is scaled down CNT becomes more efficient as compared to copper because mean free path of copper is 45 nm. Below 45 nm technology node copper is not a suitable candidate. Therefore, CNT will be suitable candidate at technology nodes below 45 nm. The work in the literature review has been done on SWCNT bundle and MWCNT and also on the mixed CNTs. The SWCNT bundle is most advantageous form of CNT based interconnect given that all component CNTs of the bundle are metallic.

The effect of separation of adjacent tubes in a SWCNT bundle plays an important role in the interconnect delay and power dissipation. The delay increases with an increase in the separation between adjacent tubes for the entire range of length values and tube diameters but the opposite is true for power dissipation i.e power dissipation decreases with increase in separation. This happens because with increase in separation, the number of CNTs in a bundle decreases the result of which is that resistance and inductance of the bundle increases but the capacitance decreases because resistance and inductance are inversely proportional to the number of CNTs but capacitance is directly proportional to the number of CNTs.

The center to center distance between adjacent shells is equal to the distance from the center of one CNT to the center of other CNT. In this case, the CNTs are densely packed and separation is equal to the diameter of single CNT.

Work has been done on sparsely packed CNT bundle whose center to center separation is greater than the diameter of CNT. Apparently, the densely packed bundles gives higher performance in comparison to those which are sparsely packed.

Therefore, a higher performance trade-off between propagation delay and power dissipation can be analyzed for densely packed SWCNT bundle. By varying the separation interconnect delay and power dissipation can be altered.

CHAPTER 4 OBJECTIVE

Based on the literature survey and research gaps from the previous chapters, the following objectives are proposed.

1. To study the effect of center to center separation between adjacent tubes in a SWCNT bundle on the impedance parameters at 32nm, 22nm and 16nm technology nodes and propose its equivalent circuit model.
2. To simulate the proposed equivalent single conductor model of SWCNT bundle using SPICE simulation tool.
3. To compare the results of delay and power dissipation for SWCNT bundle with copper at 32, 22 and 16 nm technology nodes.

PROPOSED METHODOLOGY

To analyze SWCNT bundle as an interconnect and to compare it with copper, impedance parameters from equations (1.1),(1.2),(1.3) and (1.13),(1.16),(1.17) for copper interconnect and SWCNT bundle respectively have been calculated in MATLAB. The equivalent single conductor circuit diagram for SWCNT bundle interconnect as shown in Fig.4.1will be spice simulated in tanner tools.

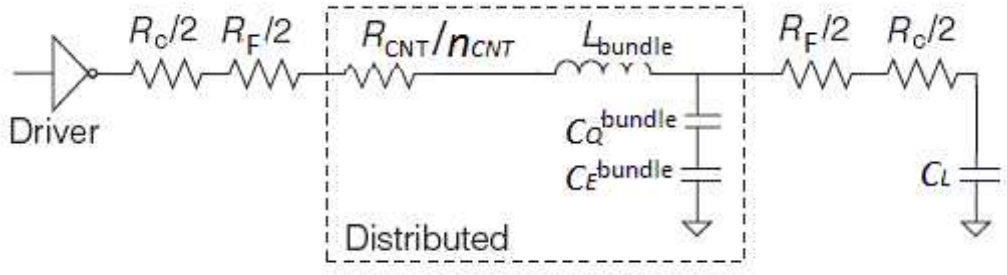

Fig.4.1. Equivalent single conductor model for SWCNT bundle interconnect

The work will be mostly concentrated on distributed model of SWCNT bundle interconnects. The input to the circuit will be provided by a 2 MHz pulse with rise time and fall time of 1ps. The circuit will be driven by a CMOS inverter and capacitor of 1fF will be taken as a load. A

1000 μm global interconnect will be selected and next step will be to increase the W/L ratio of CMOS driver in 10,20,30,40 and so on until an optimum value is achieved, the value at which power-delay product is minimum. That ratio will be selected as a universal ratio for all other calculations of delay and power in particular technology node. Apparently, Optimum value may be achieved at different W/L ratio for different technology nodes. Subsequently, repeaters will be inserted which will decrease the delay.

The number of repeaters [23] which have minimum power delay product will be used for the rest of delay and power calculations. The same W/L ratio and number of repeaters will be used for other interconnect lengths at particular technology nodes. For the ease of comparison both SWCNT bundle and copper interconnect will be provided same conditions like input pulse, load capacitance, W/L ratio and number of repeaters used.

CHAPTER 5 RESULTS AND DISCUSSIONS

To study the performance of SWCNT bundle interconnect with respect to variation in distance between adjacent tubes and to compare with its rivalry which is copper interconnect, we first need to evaluate the impedance parameters of both SWCNT bundle and copper interconnect. This has to be done by performing coding of impedance equations in MATLAB. Structure parameters used for calculations have been taken from ITRS 2013. The performance of SWCNT interconnect is to be analyzed at 32,22 and 16 nm technology node at different interconnect lengths and also by varying the distance between neighboring shells inside a SWCNT bundle at all the three technology nodes.

Table.5.1 Structure parameters of interconnect from ITRS 2013 [33]

Parameters	Technology node		
	32 nm	22nm	16 nm
Wire width(nm)	40	28	18
Wire height(nm)	120	84	54
Oxide thickness(nm)	93.6	65.5	40
Relative permittivity of dielectric	2.77	2.59	2.31
V_{DD}(volts)	0.9	0.8	0.7
Resistivity of copper (μΩ.cm)	3.66	4.2	5.66

5.1 Copper interconnect delay

First of all, the impedance parameters of copper interconnect are calculated by performing coding of impedance equations of copper in MATLAB as described in CHAPTER 1 at various interconnect lengths. All the ITRS 2013 structure parameters are taken into consideration while calculating these impedance parameters.

The following tables has been obtained for copper interconnect impedance parameters at 32, 22 and 16 nm technology node with the help of MATLAB.

Table.5.2.Impedance parameters of copper at 32 nm technology node

Length of interconnect(µm)	Impedance parameters(32 nm)		
	Resistor(KΩ)	Inductance(nH)	Capacitance(fF)
200	1.525	0.33	16.939
400	3.05	0.723	33.87
600	4.575	1.133	50.82
800	6.1	1.558	67.75
1000	7.625	1.992	84.70

Table.5.3.Impedance parameters of copper at 22 nm technology

Length of interconnect(µm)	Impedance parameters(22 nm)		
	Resistor(KΩ)	Inductance(nH)	Capacitance(fF)
200	3.572	0.348	15.84
400	7.143	0.752	31.67
600	10.72	1.176	47.52
800	14.29	1.615	63.35
1000	17.85	2.063	79.20

Table.5.4.Impedance parameters of copper at 16 nm technology node

Length of interconnect(µm)	Impedance parameters(16 nm)		
	Resistor(KΩ)	Inductance(nH)	Capacitance(fF)
200	11.70	0.365	14.34
400	23.41	0.787	28.69
600	35.12	1.23	43.03
800	46.83	1.685	57.38
1000	58.53	2.152	71.73

On having a keen glance at Tables.5.2,3 and 4, it is noticed that all the impedance parameters are increasing as the interconnect length is expanding. This is due to the fact that all these

parameters R, L and C are directly proportional to the length. Another observation which is worth noticing is that as the technology node is scaled down, the resistance and inductance of copper interconnect augment while the capacitance decreases. The reason behind this is, when the technology is scaled down the width and height of the interconnect reduce. The relation of resistance and inductance with the width and height is inversely proportionate. On the contrary, width and height of interconnect is directly proportionate to the capacitance. The following Table 5.5 depicts the delay calculated for copper interconnect delay at 32, 22 and 16 nm technology nodes for lumped model.

Table.5.5 Copper interconnect delay for lumped model

Length of interconnect(µm)	Copper interconnect delay(ns)		
	32 nm	22 nm	16 nm
200	0.635	0.647	0.870
400	1.35	1.46	2.46
600	2.21	2.55	4.85
800	3.19	3.91	8.02
1000	4.30	5.54	11.91

5.2 Impact of separation on number of CNTs in a bundle

As the distance between neighboring shells in a bundle is increased the number of CNTs in it will decrease and it is shown in Fig.5.1. This in turn provides a rise in resistance and inductance because both of them are inversely proportional to the number of CNTs. On the other hand, there is a decrease in capacitance as it is directly proportional to the number of CNTs. Therefore number of CNTs in a bundle is an important factor in determining the delay and power dissipation of SWCNT bundle interconnect. Furthermore, when the technology is scaled down, there is a decrease in the number of CNTs in the bundle. This happens because as the technology node is reduced, width and height of the bundle are also reduced. Thus, the dimensions of the bundle are reduced so does the number of CNTs.

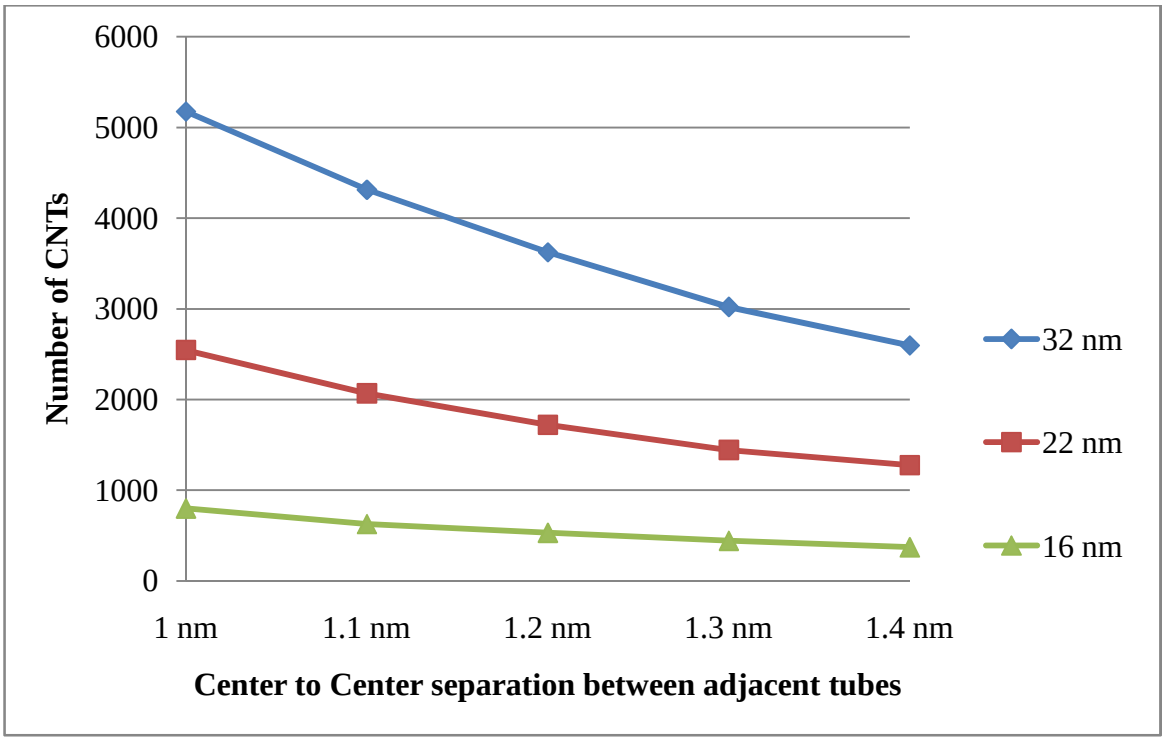

Fig.5.1. Variation in number of CNTs with respect to separation at 32, 22 and 16 nm technology nodes.

5.3 Performance analysis at 32 nm technology node

The impedance parameters of SWCNT bundle interconnect are calculated in MATLAB by varying the separation between adjacent shells at different interconnect lengths. The following Figs are obtained after plotting the values against separation. On scrutinizing Figs.5.2,3 and 4, it is observed that the resistance as well as inductance increases with increase in separation whereas the opposite is true for capacitance. The cause for this variation lies in the fact that number of CNTS in a bundle reduces with increase in separation. Moreover, the number of CNTs are inversely proportional to the resistance and inductance while it is directly proportional to capacitance.

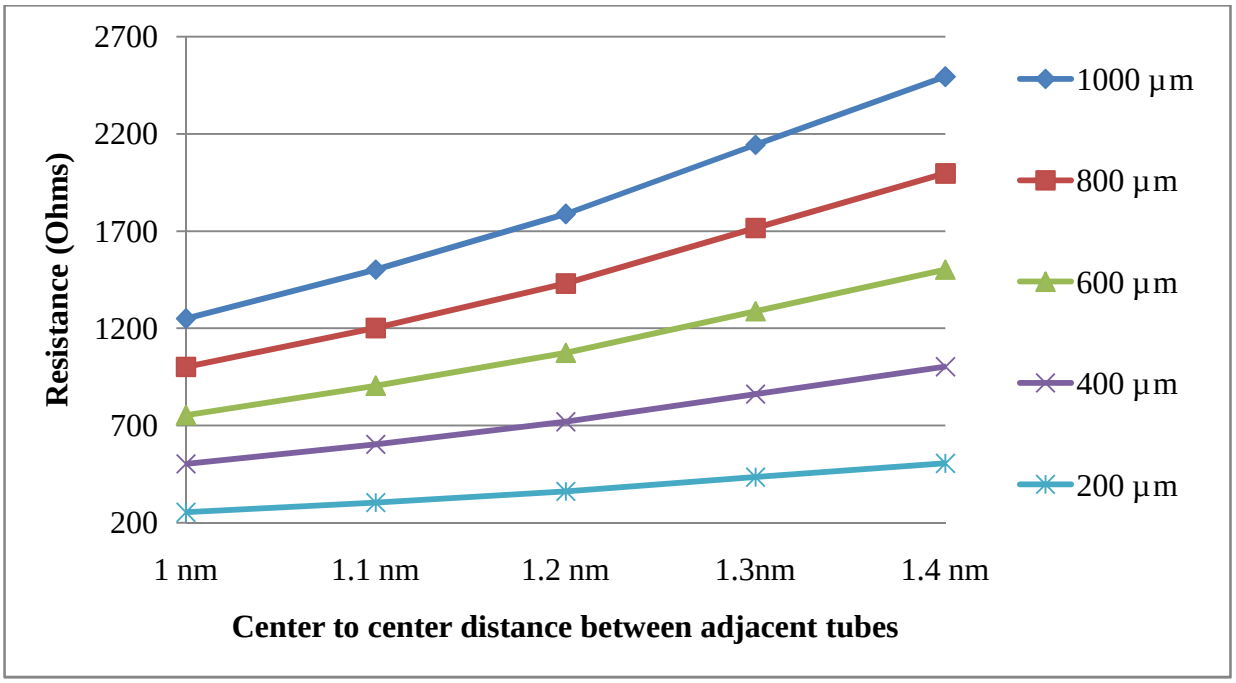

Fig.5.2. Effect of increase in separation on resistance at various interconnect lengths at 32 nm technology node.

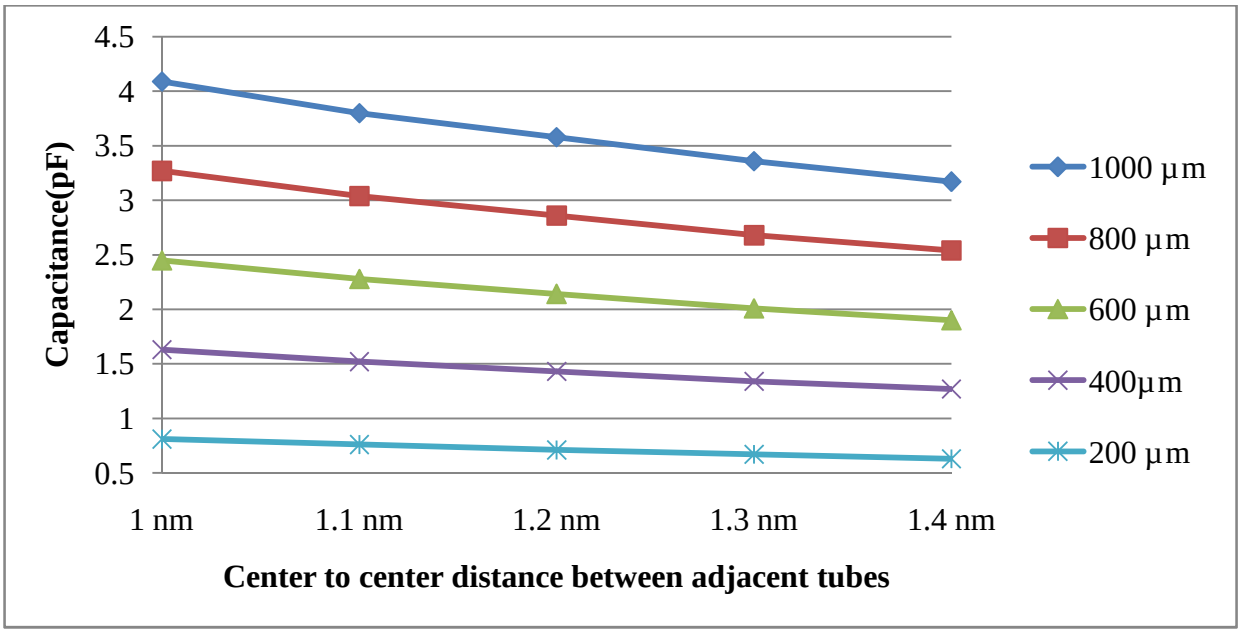

Fig.5.3. Effect of increase in separation on Capacitance at various interconnect lengths at 32 nm technology node.

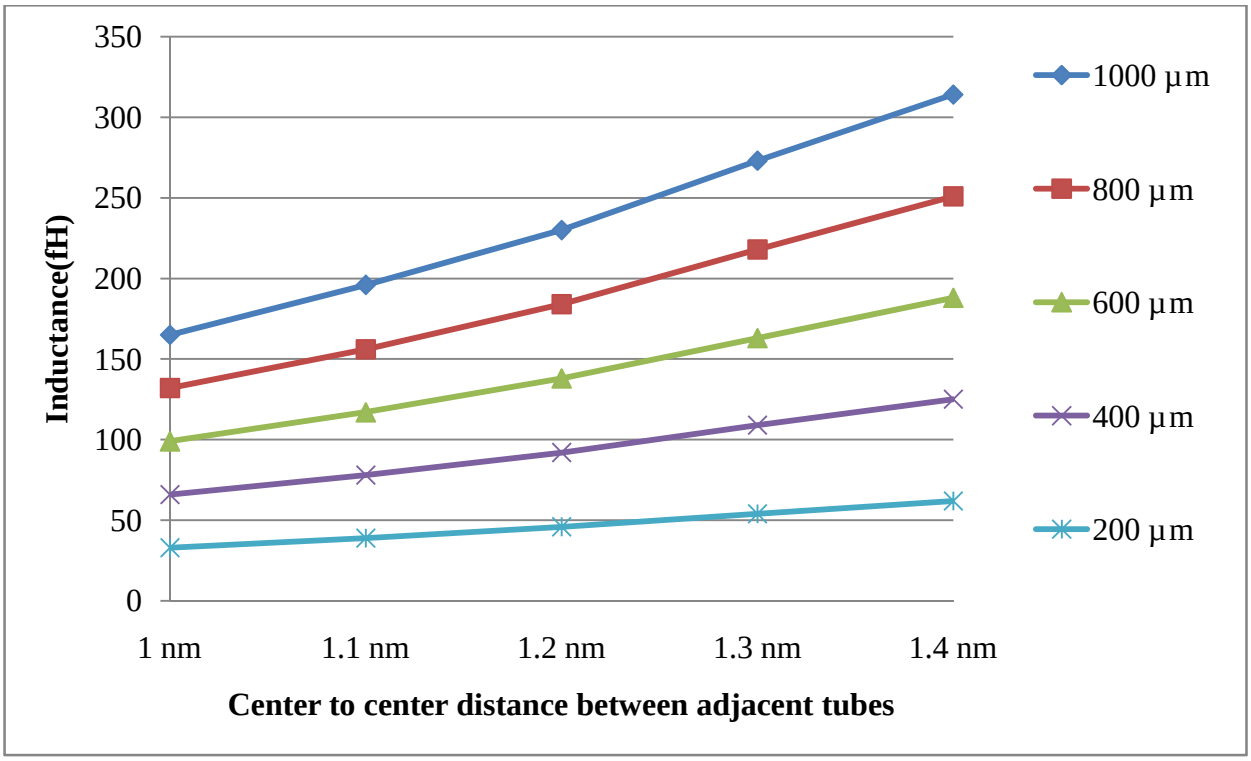

Fig.5.4 Effect of increase in separation on inductance at various interconnect lengths at 32 nm technology node.

5.3.1 Optimum driver size

Now that the impedance parameters at 32 nm technology node have been obtained, the power and delay of SWCNT bundle interconnect are first calculated for lumped model of the interconnect at various W/L ratio of the CMOS driver. The ratio varies in terms of 10,20,30 till 70. At each point power and delay is calculated and also their product. The Fig 5.5 depicts that power delay product decreases with increase in W/L ratio of CMOS driver. There is a point reached when the power delay product refuses to decrease further or there is a very small decrease. At that point we can say that an optimum value of W/L ratio is achieved. In this case the optimum value is achieved at ratio of 50. At this point the impedance of interconnect best matches with the impedance of CMOS driver. Consequently, this value will be used for further investigation on delay and power at 32 nm technology node while working on distributed model of SWCNT bundle interconnect which includes repeaters.

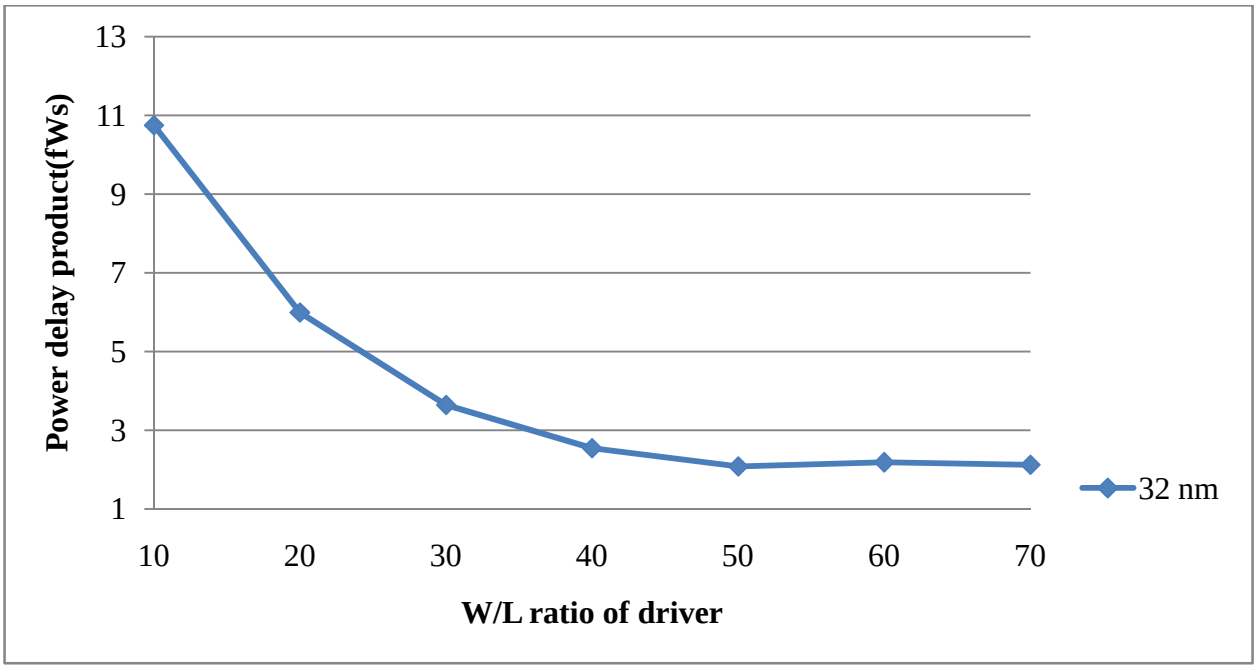

Fig.5.5 Variation in power delay product with respect to increase in W/L ratio of driver.at 32 nm technology node

5.3.2 Repeater insertion

Repeaters (as shown in Fig. 5.6)are actually the buffers or inverters used in order to reduce the propagation delay. The role of repeaters is to reduce the length of interconnect into 'N' segments, where N represent number of repeaters and it is known that propagation delay is dependent on length of interconnect and therefore insertion of repeaters results in reduction of propagation delay.

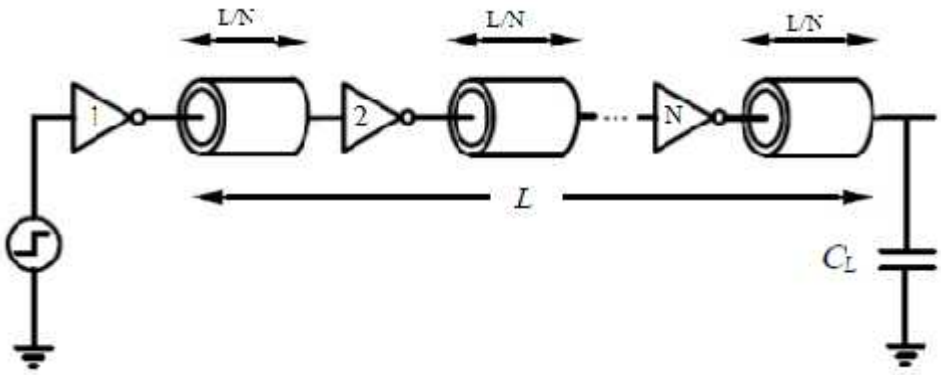

Fig.5.6 Repeaters used in ESC model.

The repeater insertion causes reduction in the distributed parameters of interconnects by the factor of N. When the repeaters are inserted the impedance parameters also reduce by a factor of N. Consequently, the delay is reduced but the power is enhanced. However the overall power delay product is reduced. In Fig.5.7 it can be apprehend that the power delay product reduces rapidly as the number of repeaters are increased. After achieving a lowest value, the product becomes nearly constant or there is a little variation. The number at which this scenario happens is taken as number of repeaters to be taken in all other calculations for a particular technology node. At 32 nm technology node, the number of repeaters which

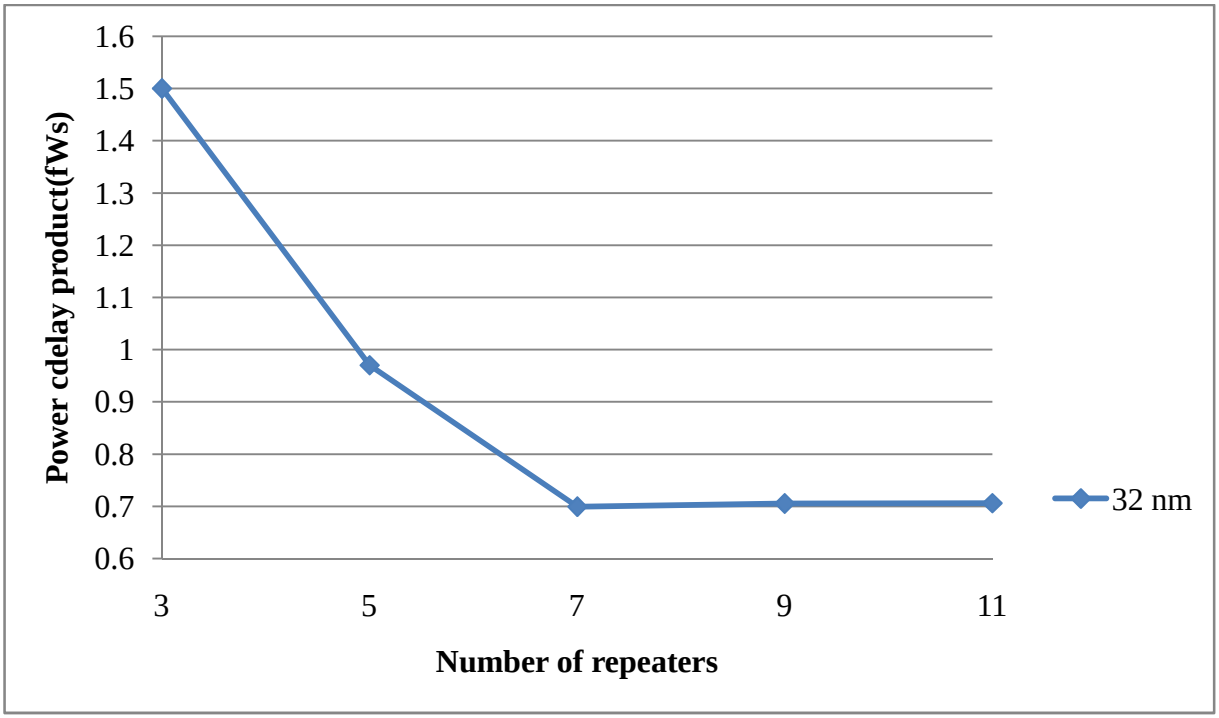

Fig.5.7 Power delay product vs. number of repeaters at 32 nm technology node.

provides minimum power delay product is 7. The schematic of tanner tools for ESC distributed model of SWCNT bundle interconnect with 7 repeaters at 32 nm technology node is shown Fig.5.8

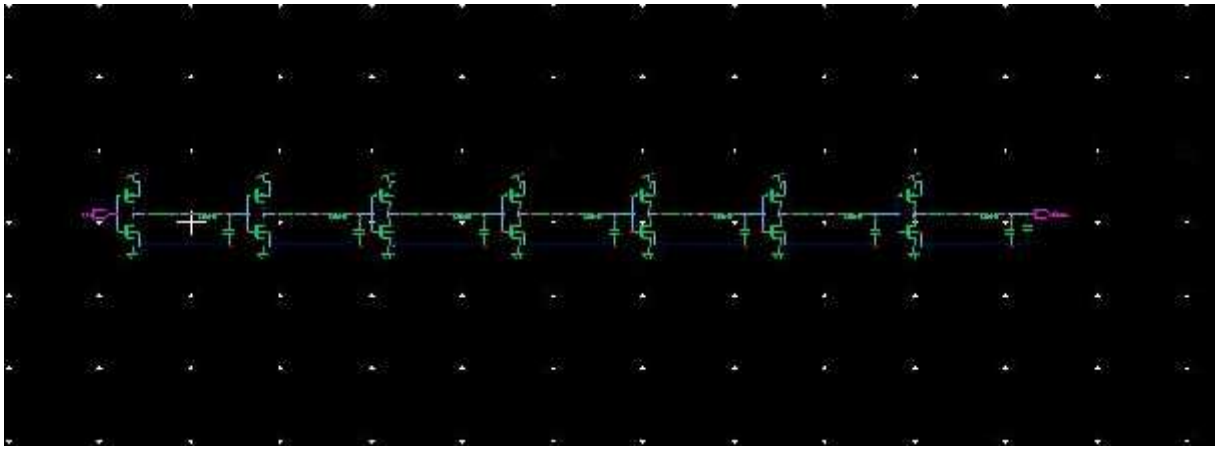

Fig.5.8. Schematic for ESC distributed model of SWCNT bundle interconnect with 7 repeaters at 32 nm technology node.

5.3.3 Effect of separation on propagation delay of SWCNT bundle

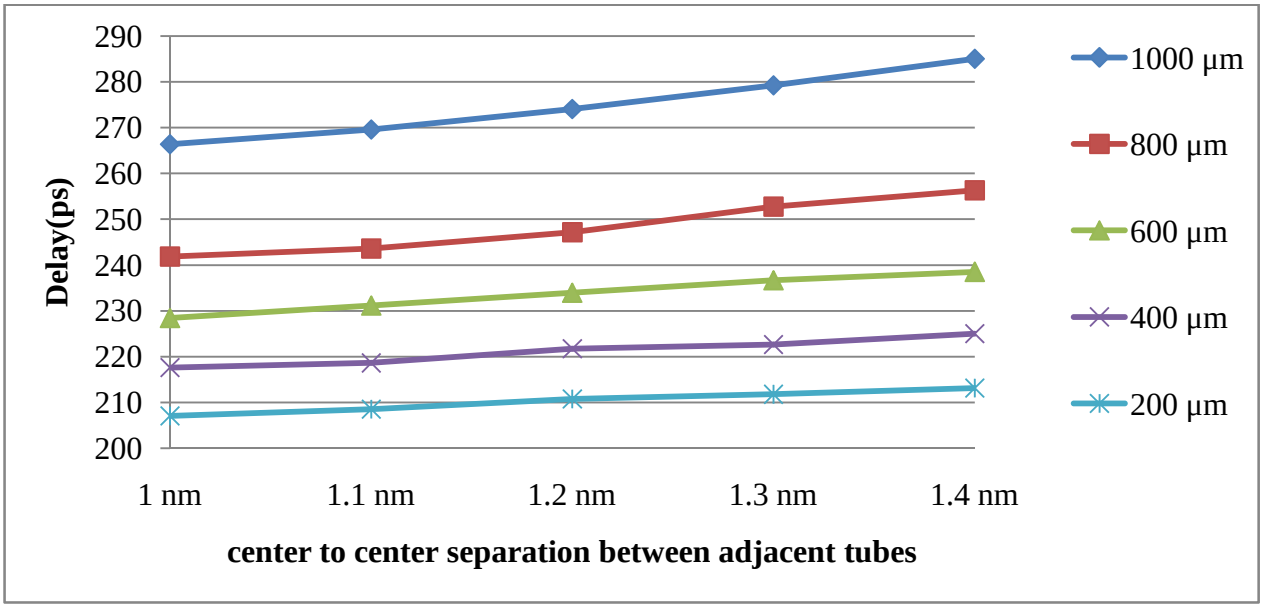

Fig.5.9 Increase in delay with respect to increase in separation between adjacent shells at 32 technology node.

From Fig.5.9 it is vivid that the delay increases with the increase in separation between neighboring shells. As a matter a fact, it happens because increase in separation results in the rise of resistance and inductance. However, during this course of action the capacitance

decreases. Now the delay mainly depends upon the resistance and capacitance and has negligible inductive effects. The increase in delay proves that increase in resistance is more pronounced over the decrease in capacitance. On further probing into the Fig.5.9, it is examined that there is high rise in delay at 1000 µm interconnect length as compared to 200 µm interconnect. Why it is so? The answer to this question is that resistance also increases with length. Therefore at higher lengths the increase in resistance due to length contributes to the existing increase with respect to separation. Thus the delay is further enhanced.

5.3.4 Effect of separation on normalized propagation delay

Now that the delay of SWCNT bundle has been calculated, it can be compared with copper interconnect. The following Fig.5.10 has been obtained which represents the ratio of delay of SWCNT bundle interconnect and copper interconnect which is known as normalized delay.

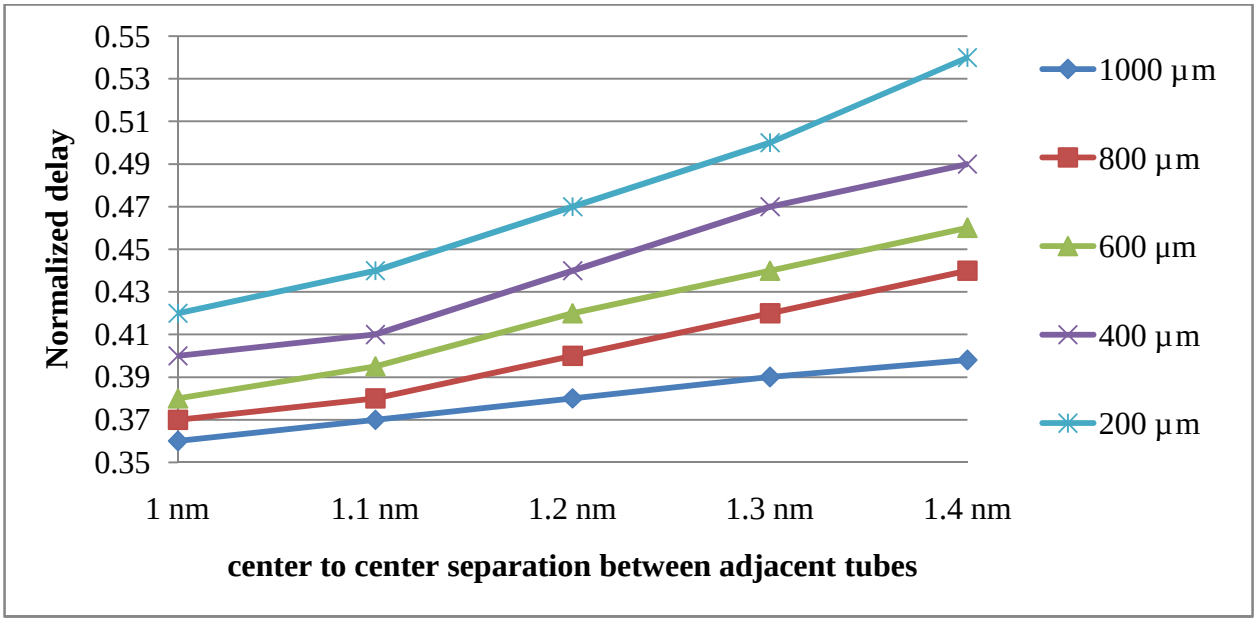

Fig.5.10. Normalized delay vs. centre to centre distance between adjacent tubes for different interconnect lengths at 32 nm technology node.

For the ease of estimate, copper interconnect delay has been calculated at same input pulse,W/L ratio, number of repeaters i.e with ‘50’ W/L ratio of CMOS driver and ‘7’ number of repeaters. 90% delay has been withdrew from the results of both of the interconnects. It is manifest from Fig.5.10 that the normalized delay also increases with increase in center to

center distance between adjacent tubes. It is quite obvious because the actual delay of SWCNT bundle rises as the separation increases. Furthermore, it is examined that normalized delay increases with decrease in interconnect length. The reason behind this is that, amelioration in performance of SWCNT bundle interconnect is better for longer interconnects.

5.3.5 Effect of separation on power dissipation of SWCNT bundle

Fig.5.11. demonstrates the reduction in power dissipation with respect to increase in center to

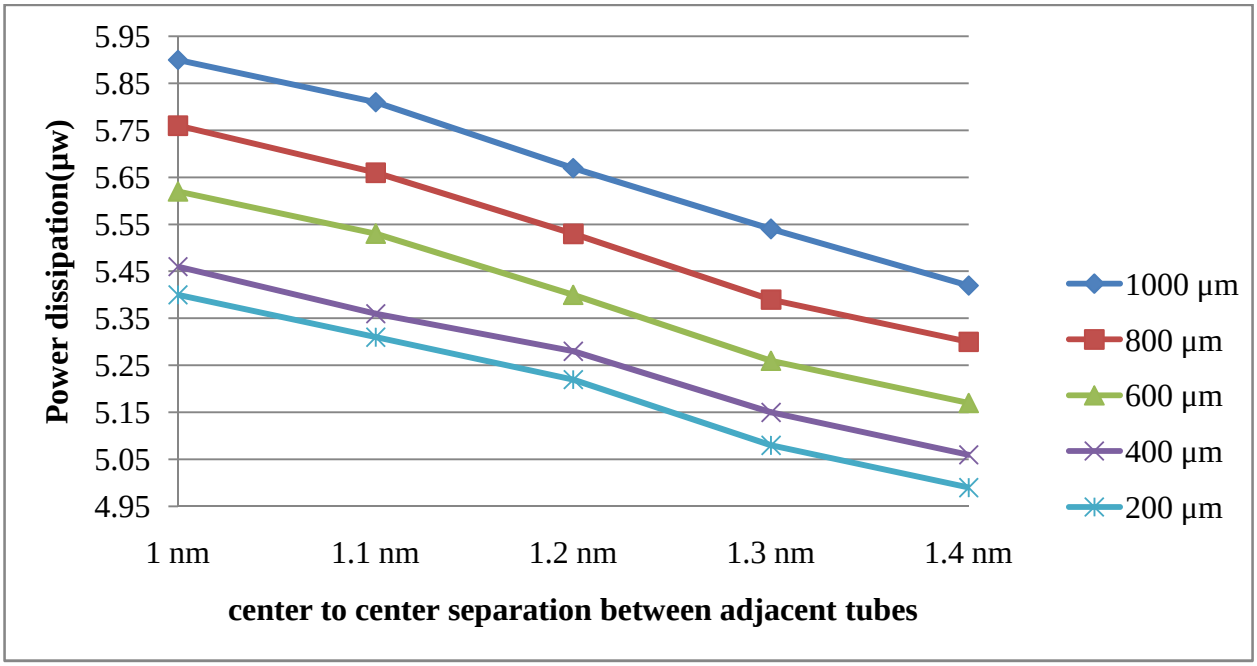

Fig.5.11. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 32 nm technology node.

center separation between adjacent tubes in a SWCNT bundle interconnect at different interconnect lengths. This reduction supports the dominance of reduction in capacitance over increase in resistance. Nevertheless, the capacitance increases with increase in length of the interconnect.

5.3.6 Effect of separation on normalized power dissipation

The Fig.5.12**.** depicts the decrease of normalized power which is ratio of power of SWCNT bundle interconnect and copper interconnect. It can be clearly seen from the Fig that the ratio is more than 1, which means copper interconnect exhibits better performance than SWCNT in terms of power dissipation. Seemingly, the SWCNT bundle interconnect exhibits more power than its competitor. However, with the increase in center to center distance between adjacent tubes in a SWCNT bundle interconnect the normalize power decreases. This is due to the fact that actual power dissipation of SWCNT bundle decreases with the increase in separation and so does the normalized power. Likewise, actual power dissipation, the normalized power dissipation also increases with increases in interconnect length.

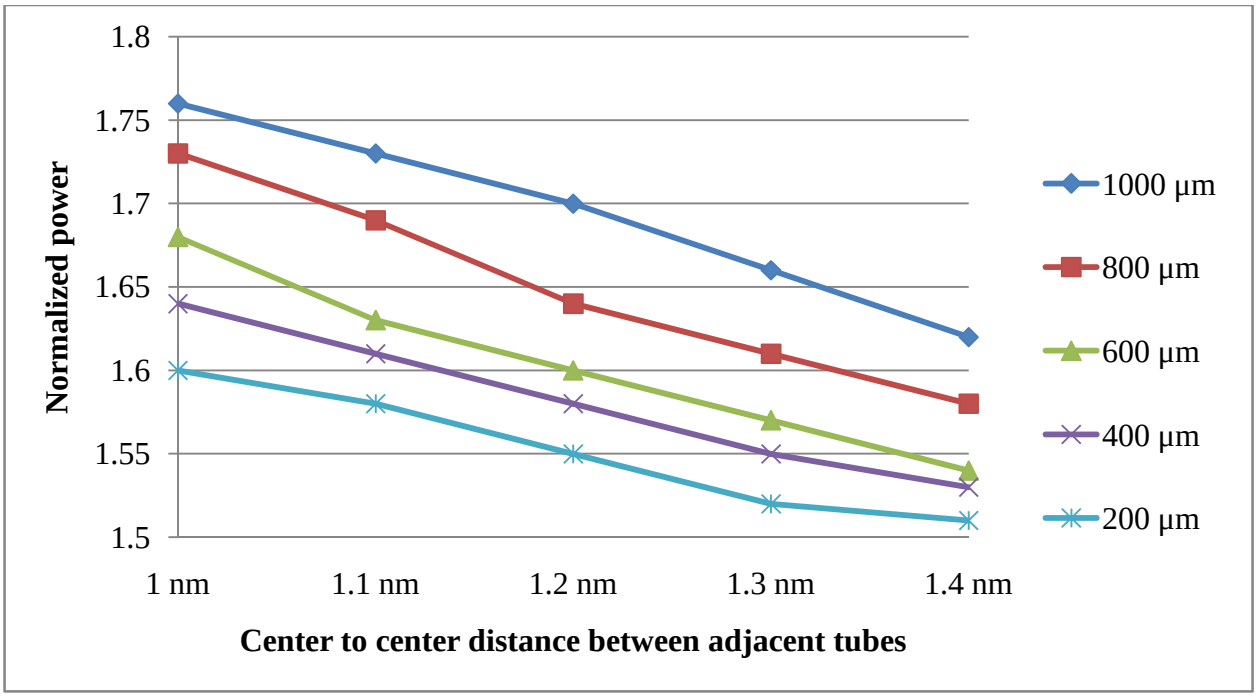

Fig.5.12. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 32 nm technology node.

5.3.7 Effect of separation on power-delay product of SWCNT bundle

The power delay product of SWCNT bundle interconnect mostly decreases with increase in separation between adjacent tubes. This indicates dominance of power dissipation over propagation delay. However, at some points the propagation delay dominates over the power

dissipation. As a result, there is a trivial increase in power delay product. This happens because ultimately the propagation delay and power dissipation depends on the impedance parameters. In Fig.5.13 it is depicted that the power delay product increases with increase in interconnect length. As the propagation delay and power dissipation also increases with increase in length so does the power delay product. The propagation delay increases with separation because the resistance rises with increase in separation whereas the power. dissipation decreases with separation because the capacitance decreases with increase in separaion

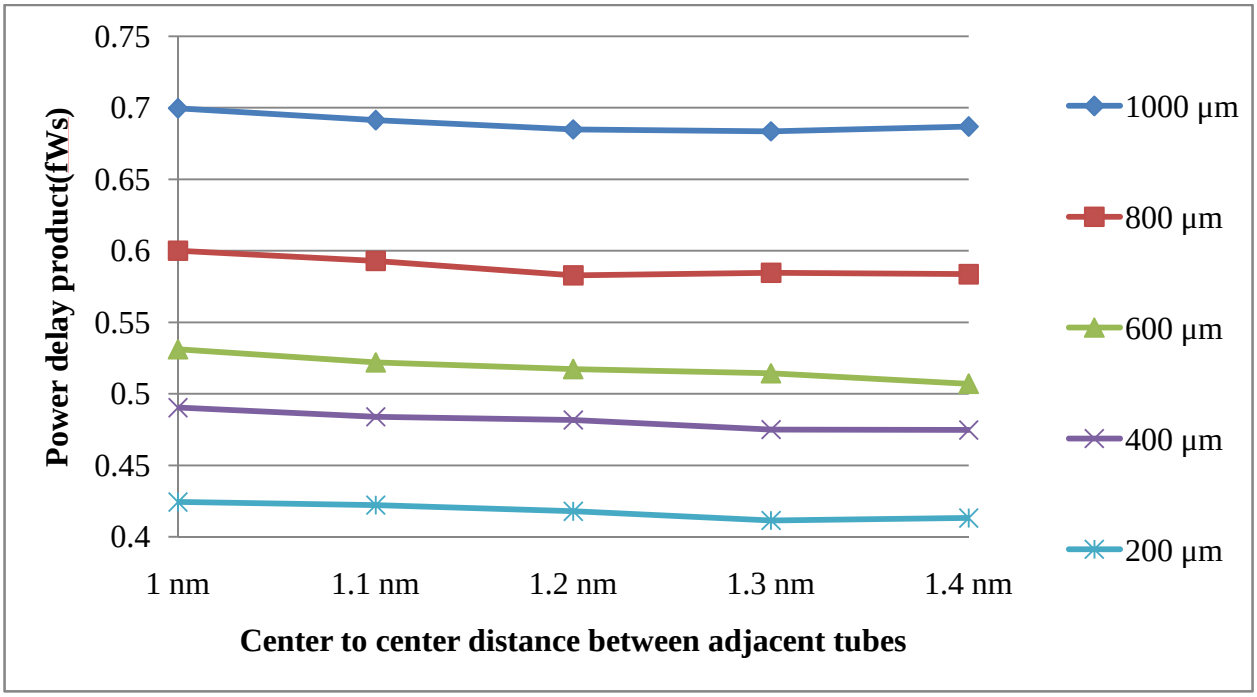

Fig.5.13. Power delay product vs. increase in separation between adjacent tubes for different interconnect lengths at 32 nm technology node.

5.4 Performance analysis at 22 nm technology node

The performance analyses of SWCNT bundle interconnect versus copper interconnect and the effect of center to center distance between adjacent tubes on propagation delay has been examined at 32 technology node. Now, we shall approach towards 22 technology node and

observe what would happen if same kind of variations are applied to SWCNT bundle at this technology. In order to do this, first of all we need to calculate the impedance parameters of SWCNT bundle interconnect. These parameters have been calculated by performing coding of impedance equations in MATLAB. Structure parameters for interconnect at 22 nm technology node has been used for calculations. After calculating the impedance parameters with respect to increase in center to center distance between neighboring tubes in a SWCNT bundle. The values obtained are plotted versus separation. the following Figs.5.14,5.15 and 5.16 represents the effect of separation between center to center distance between adjoining tubes on impedance parameters.

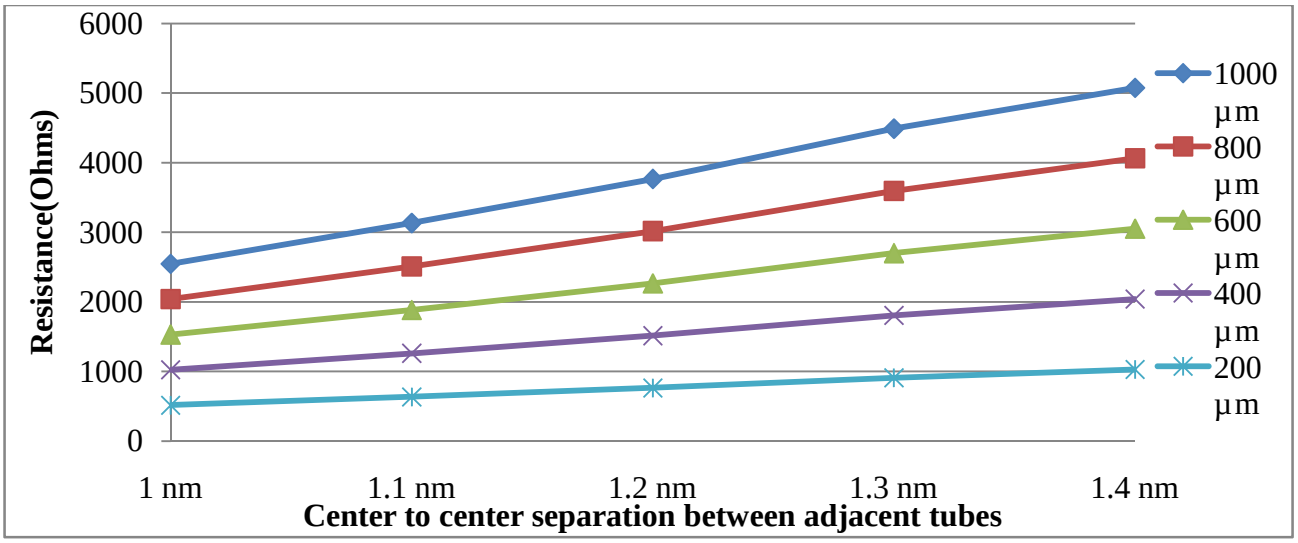

Fig.5.14. Resistance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node.

The trends which were observed for impedance parameters with respect to increase in center to center separation between adjoining tubes at 32 nm technology node are also observed at 22 nm technology node. But this time the value of resistance and inductance increased further. On the other hand, the value of capacitance decreased further. Now the question is why it is so? The answer is at 22 nm technology node, the width and height of interconnect reduces further in comparison with 32 nm technology node. Consequently, the number of CNTs inside a SWCNT bundle interconnect reduces. This in turn increases the resistance and inductance and decreases the capacitance further.

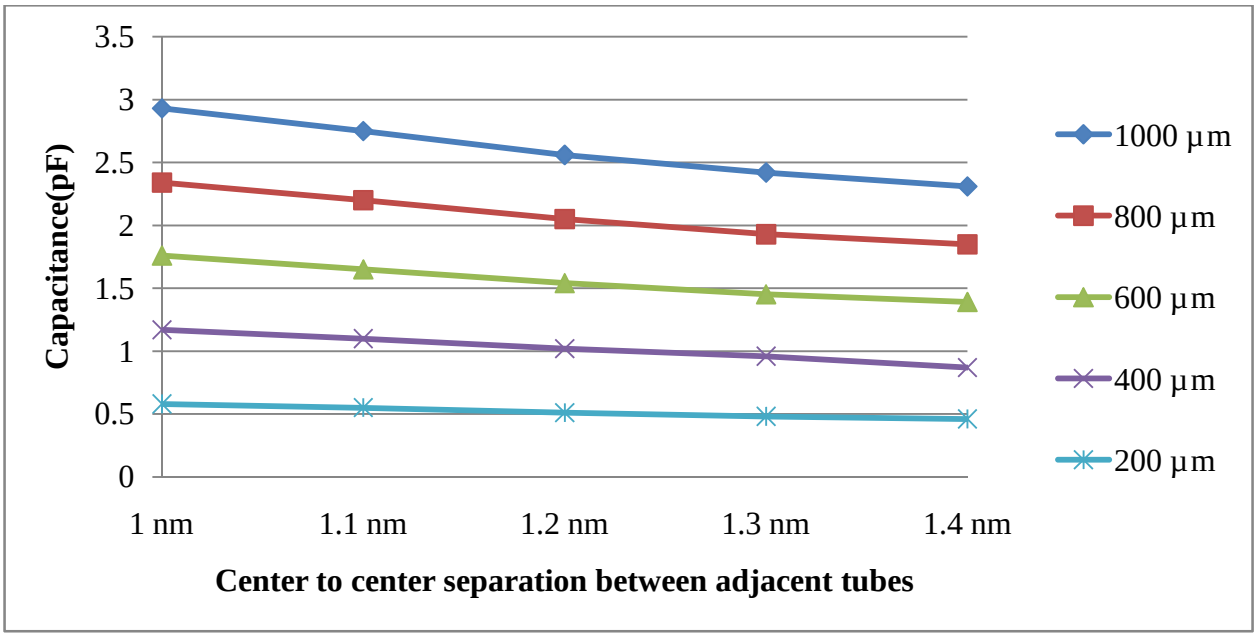

Fig.5.15. Capacitance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node.

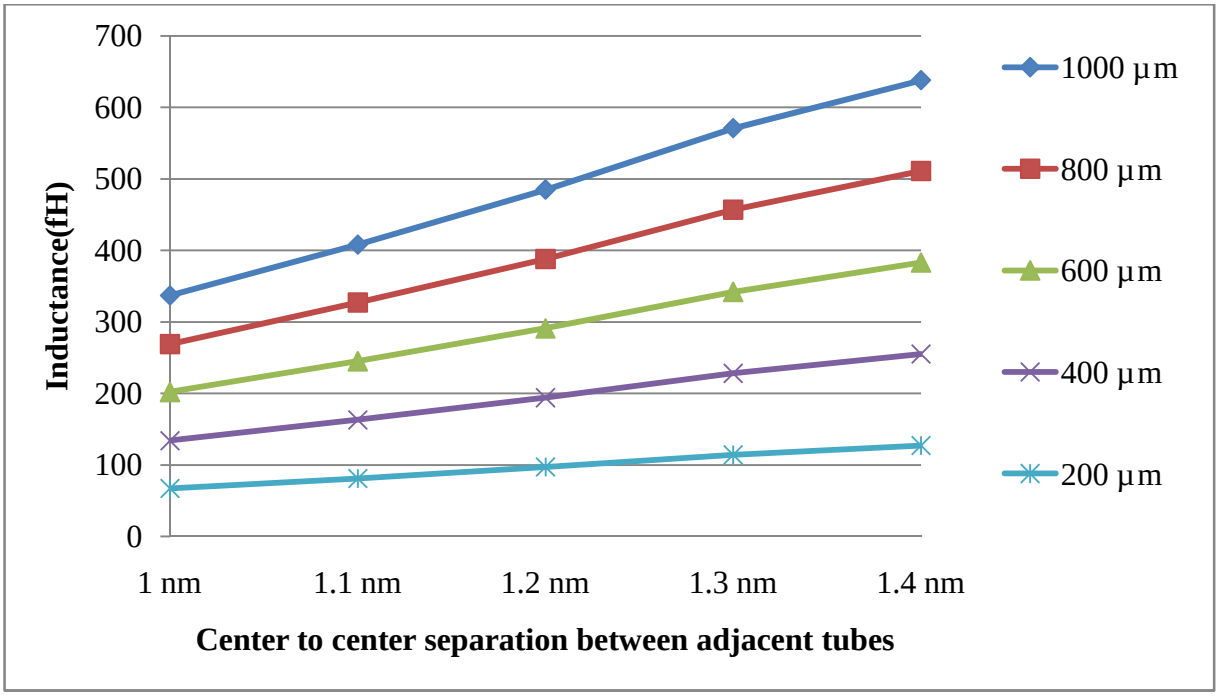

Fig.5.16. Inductance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node.

Now that the, value of impedance parameters at 22 nm technology node are known. We shall repeat the whole procedure now for this technology. The delay and power dissipation are calculated for lumped model at 22 nm technology for 1000 μm long interconnect by varying the W/L ratio of CMOS driver from 10 to 70. The minimum power delay product is obtained at W/L ratio of 50 which is represented by Fig.5.17**.** One thing, which is worth noticing is that power delay product has increased as compared to 32 nm technology node

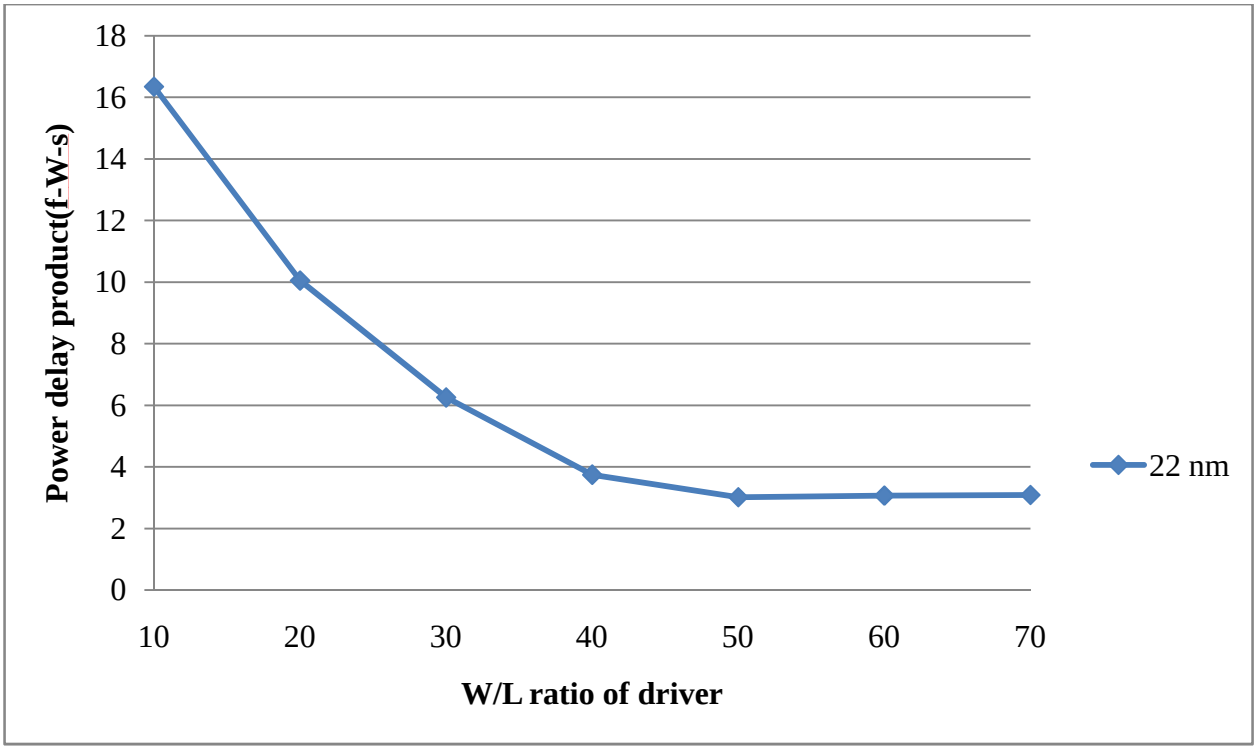

Fig.5.17. Variation in power delay product with respect to increase in W/L ratio of driver at 22 nm technology node.

This increase indicates the supremacy of increase in delay over decrease in power dissipation. The next step is to work on distributed model and to insert repeaters until the minimum power delay product is attained.

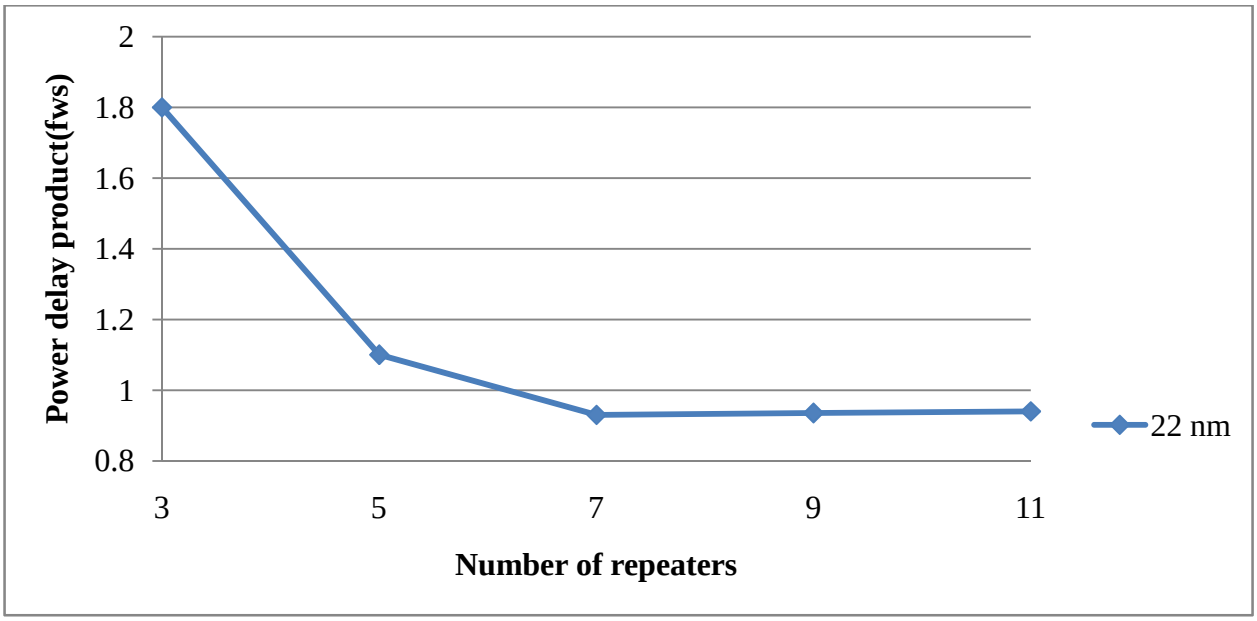

Fig.5.18. Power delay product vs. number of repeaters at 22 nm technology node

At 22 nm technology node, the minimum product is attained with seven repeaters, which is depicted by Fig.5.18. The CMOS W/L ratio of 50 and 7 repeaters will be used for all the interconnect lengths at 22 nm technology node. There is decrease in power delay product because impedance parameters get divided by a factor of N and there is fall in propagation delay. The minimum power delay product obtained at this technology node is greater than what has been obtained for 32 nm technology. Again the increase in propagation delay, with respect to scaling of technology node dominates over decrease in power dissipation

5.4.1 Effect of separation on propagation delay of SWCNT bundle

On examining Fig.5.19 , it can be stated that the propagation delay increases with increase in center to center separation between adjoining tubes. This kind of trend has also been seen at 32 nm technology node. However, at this time the propagation delay has been uplifted as compared to 32 nm node. What would be the reason for the increase in delay with decrease in technology node? The answer is, with the reduction in technology node, the width and height of the interconnect decreases. Therefore, the number of CNTs inside a bundle decreases. This in turn leads to an increase in resistance and so does the propagation delay.

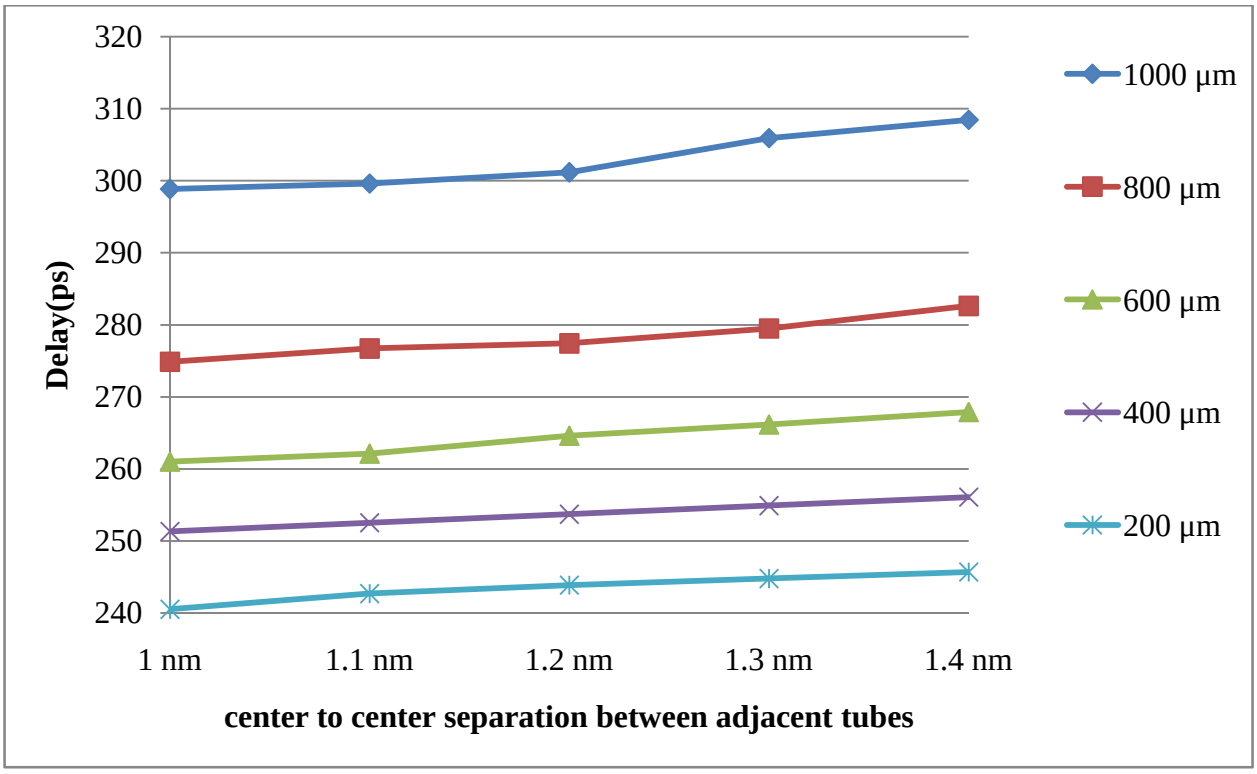

Fig.5.19 Increase in delay with respect to increase in separation between adjacent shells at 22 nm technology node.

5.4.2 Effect of separation on normalized propagation delay

Like the actual propagation delay, the normalized propagation delay also increases with increase in center to center separation between adjoining tubes. The explanation of this increase is same as mentioned for 32 nm technology node. Although the Fig.5.20 looks very similar to the Fig.5.10 obtained in the case of 32 nm technology node. However, there is one thing to observe, the normalized delay at 22 nm technology node is smaller than the normalized delay at 32 nm technology node for all length of interconnects.

The reason for this occurrence is, when the technology is scale down, the propagation delay of both SWCNT bundle and copper interconnect increases but the propagation delay of copper interconnect increases rapidly because the resistance of copper interconnect increases rapidly.

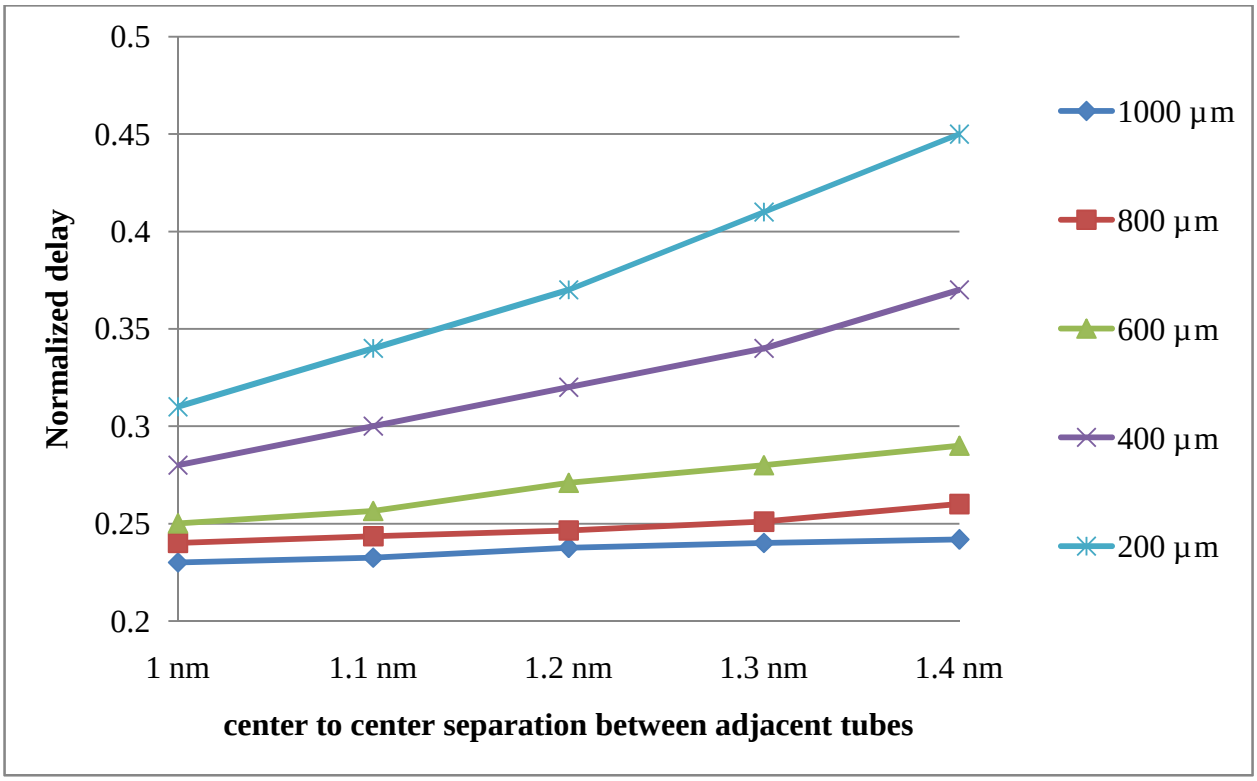

Fig.5.20. Normalized delay vs. centre to centre distance between adjacent tubes at different interconnect lengths at 22 nm technology node.

5.4.3.Effect of separation on power dissipation of SWCNT bundle

The increase in center to center separation shows same kind of effect as seen at 32 nm technology node. However, this time there is a fall in power dissipation for each and every interconnect length as compared to 32 nm technology node. This fall in power dissipation (as shown in Fig.5.21) occurs due to scaling of technology node. Because of the scaling the number of CNTs in a SWCNT bundle reduces. As a result, the resulting capacitance decreases as capacitance is directly proportional to the number of CNTs. Apparently, the power dissipation increase with increase in length of interconnect because the impedance parameters increase with length.

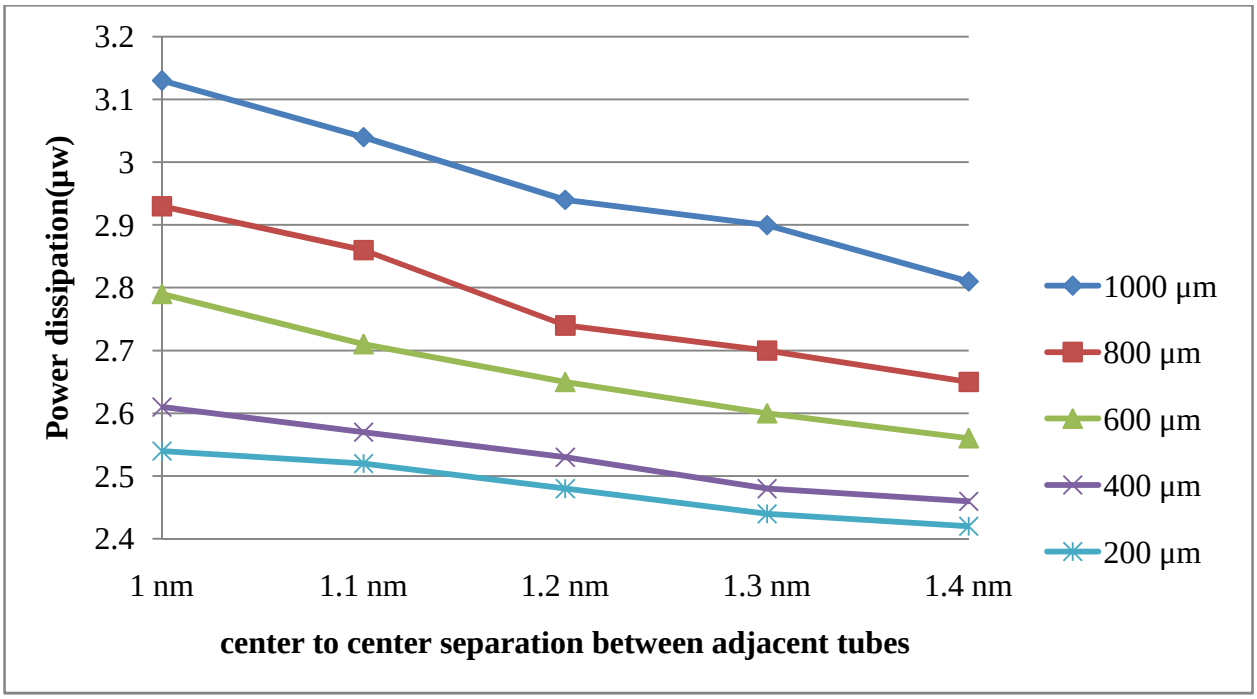

Fig.5.21. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 22 nm technology node.

5.4.4 Effect of separation on normalized power dissipation

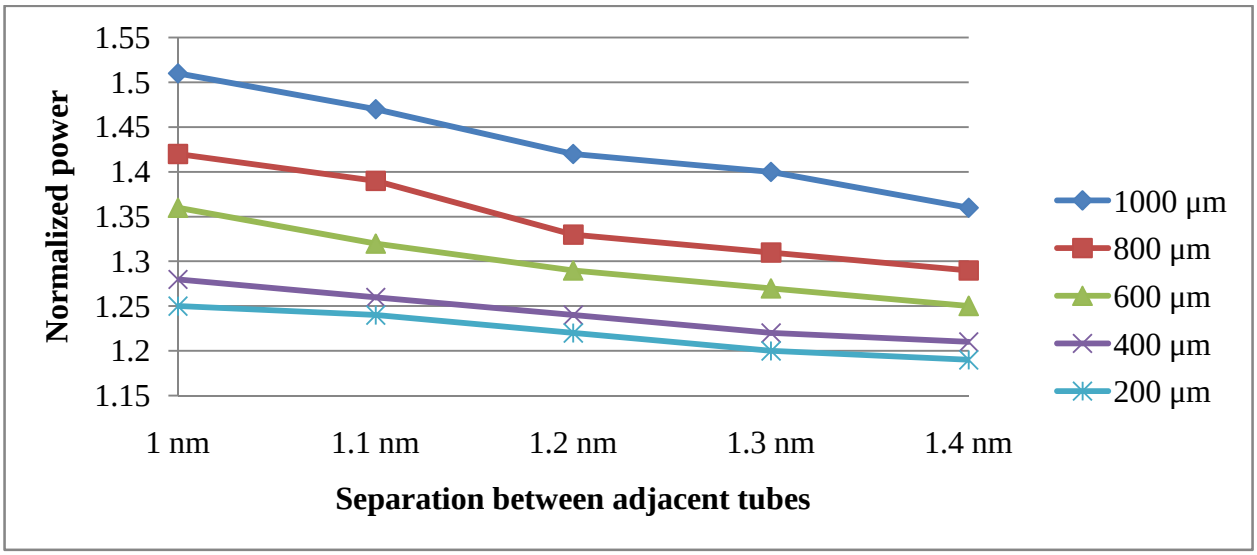

Fig.5.22. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 22 nm technology node.

Like the actual power dissipation, the normalized power dissipation also decreases with increase in center to center separation between adjoining tubes. The explanation of this decrease is same as mentioned in the case of normalized power dissipation at 32 nm technology node. Although the Fig.5.22 looks very similar to the Fig.5.12 obtained in the case of 32 nm technology node. However, there is one thing to observe, the normalized power dissipation at 22 nm technology node is smaller than the normalized delay at 32 nm technology node for all length of interconnects. The reason for this occurrence is, when the technology is scaled down, actual power dissipation decreases and the power dissipation of SWCNT bundle interconnect decreases more rapidly as compared to copper interconnect.

5.4.5 Effect of separation on power-delay product of SWCNT bundle

The impact of separation on power delay product of SWCNT bundle is shown in Fig.5.23 at 22 nm technology node. It is similar as that for 32 nm technology node, expect for a change that the power delay product has increased for all the interconnect lengths with the scaling of technology. This means, it is the increase in propagation delay which dominates over the decrease in power dissipation with respect to scaling in technology node.

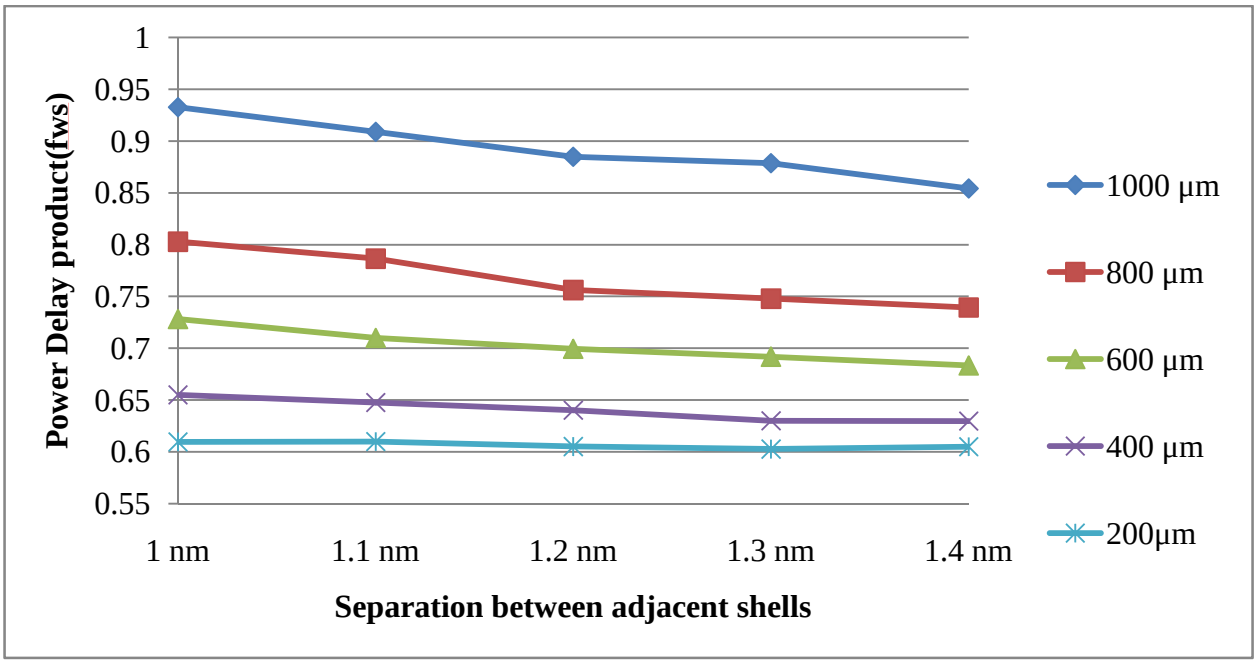

Fig.5.23. Power delay product vs. increase in separation between adjacent tubes for different interconnect lengths.at 22 nm technology node

5.5 Performance analysis at 16 nm technology node

Like the impact of center to center separation on propagation delay and power dissipation of SWCNT bundle interconnect and its performance with respect to copper interconnect has been observed at 32 and 22 nm technology node. Similarly, now the effect has to be seen at 16 nm technology node. For this purpose, first we need to evaluate the impedance parameters at this technology. These parameters are calculated in MATLAB for the center to center separation between adjoining tubes in a bundle varying from 1nm to 1.1 nm. The outcomes for the resistance, capacitance and inductance are shown in Figs.5.24,5.25 and 5.26 rescpectively.

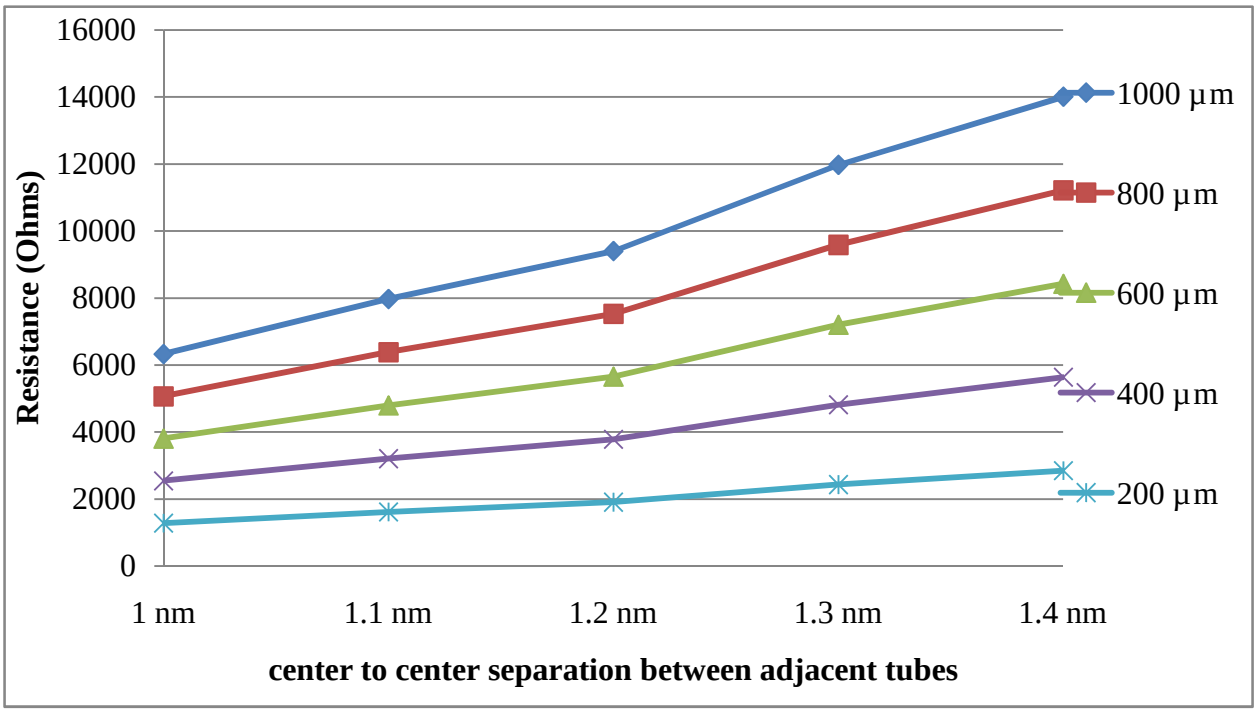

Fig.5.24 Effect of increase in separation on resistance at various interconnect lengths at 16 nm technology node.

Similar type of trends which were observed for 32 and 22 nm technology nodes has been observed for impedance parameters when plotted against center to center separation between

nearby tubes at 16 nm technology node. The reason for these trends is the same as explained for other two technologies. However, the resistance and inductance obtained for this technology are highest amongst the all three technologies. On the contrary, the capacitance obtained is the lowest amongst the all three technologies. The reason for this, 16 nm technology node has the lowest width and height of the interconnect as compared to the 32 and 22 nm technology nodes. So, it is obvious for the SWCNT bundle to hold the lowest number of CNTs as compared with other two technologies. Therefore, the resistance and inductance is the highest amongst all the three technology nodes whereas the opposite is true for capacitance.

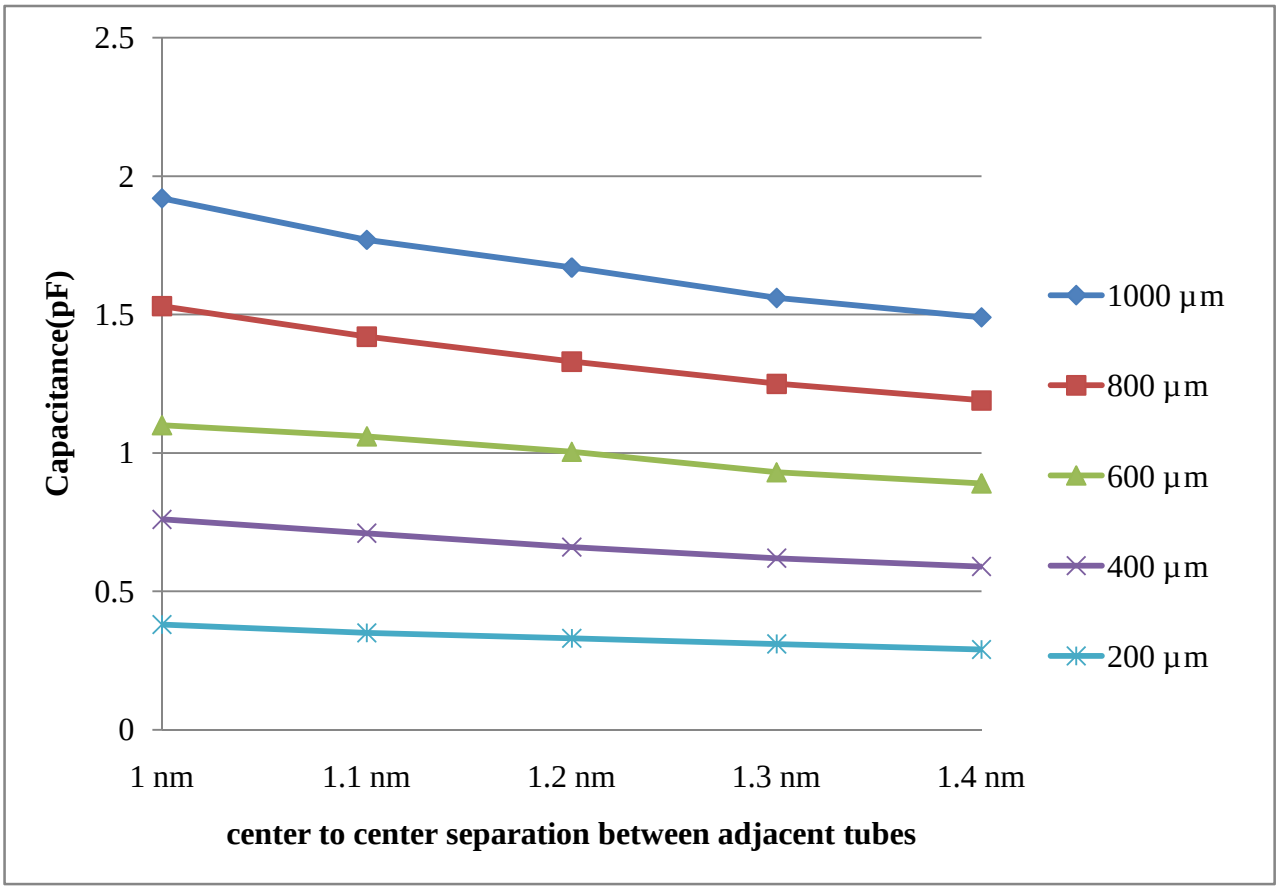

Fig.5.25 Effect of increase in separation on capacitance at various interconnect lengths at 16 nm technology node.

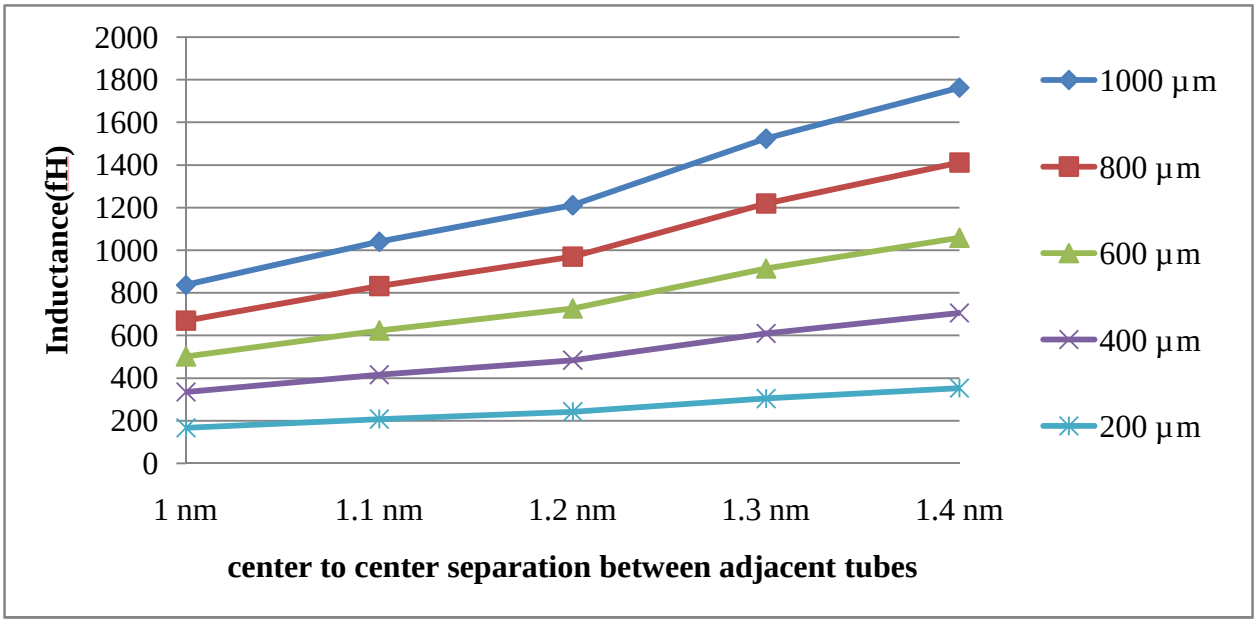

Fig.5.26 Effect of increase in separation on inductance at various interconnect lengths at 16 nm technology node.

Now using these values, the whole procedure is again repeated for 16 nm technology. The power delay product is calculated by varying the W/L ratio from 10 to 70 for lumped model of SWCNT bundle 1000 µm long interconnect. The minimum power delay product is obtained at CMOS W/L ratio of 40 as shown in Fig.5.26. Now this W/L ratio will be used for propagation delay and power dissipation calculations for distributed model of SWCNT bundle interconnect at 16 nm technology node.

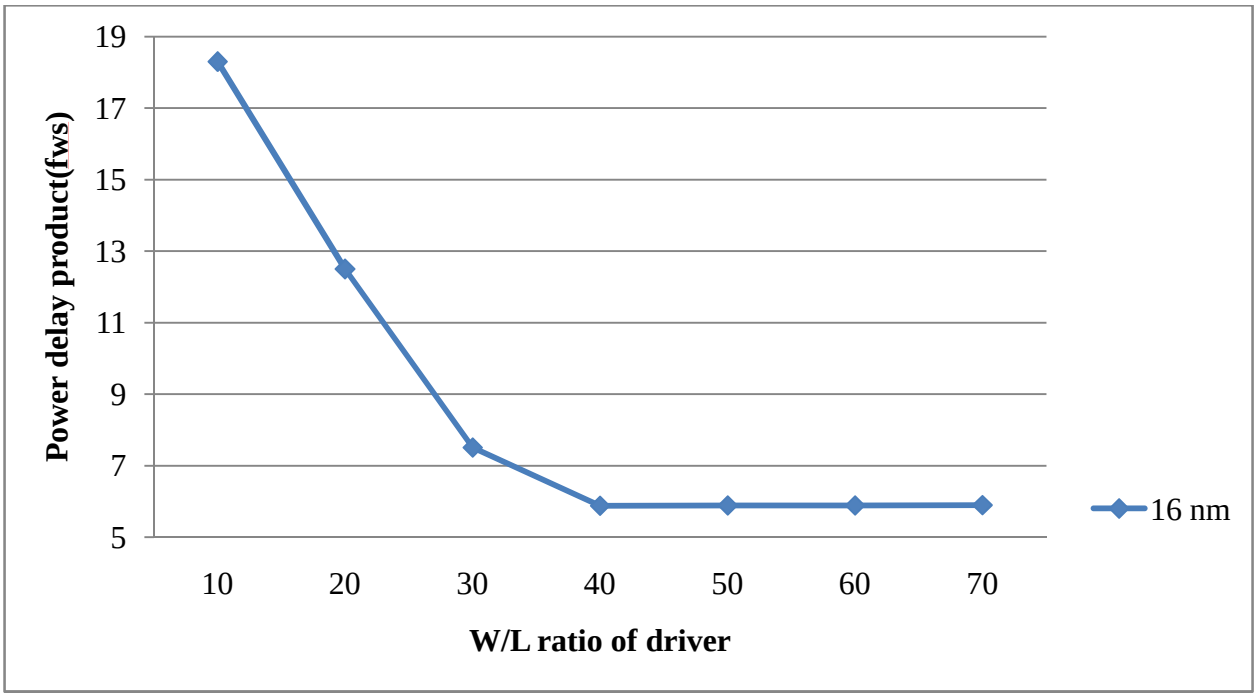

Fig.5.27. Variation in power delay product with respect to increase in W/L ratio of driver.at 16 nm technology node.

The Fig.5.27 is showing the same trend as followed by 32 and 22 nm technology nodes. However, the power delay product is increased, if it is compared with both 32 and 22 nm technology nodes. This increase indicates the supremacy of increase in delay over decrease in power dissipation. Due to the insertion of repeaters, there is a fall in power delay product which is shown in Fig.5.26 The next step is to work on distributed model and to insert repeaters until the minimum power delay product is attained. At 16 nm technology node, the minimum product is attained with nine repeaters, which is depicted by Fig.5.28

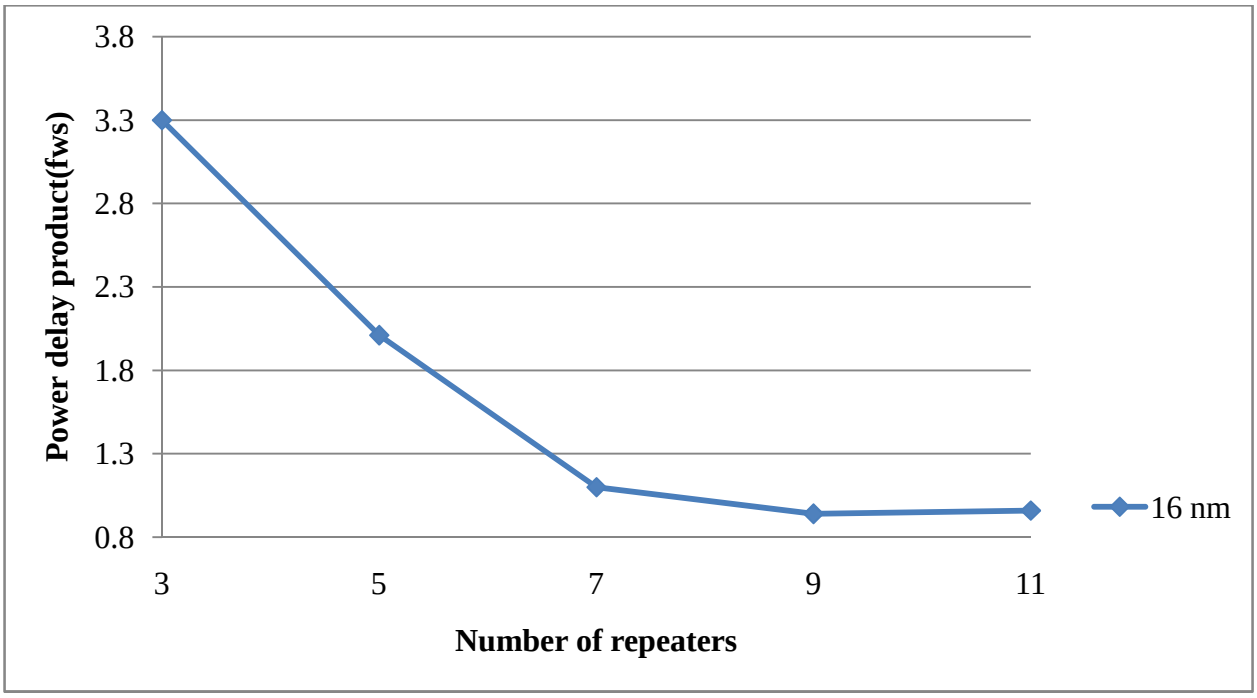

Fig.5.28. Power delay product vs. number of repeaters at 16 nm technology node.

The CMOS W/L ratio of 40 and 9 repeaters is used for all the interconnect lengths at 16 nm technology node.

5.5.1 Effect of separation on propagation delay of SWCNT bundle

With the increase in center to center separation between adjoining tubes, propagation delay increases. It is a similar observation which was observed at 32 and 22 nm technology nodes. The reason for this increase in propagation delay is same as that explained for the increase at 32 and 22 nm nodes. Evidently, the propagation delay at this node is highest among the all three technologies. This is due to the fact that, width and height of interconnect at 16 nm technology is the smallest as compared to other two technologies. One interesting thing to note in Fig.5.29 is that at 1000 μm interconnect length the propagation delay increases rapidly. This happens because of two reasons, first is the resistance is very high at long length and due to reduction in technology it adds to the propagation delay.

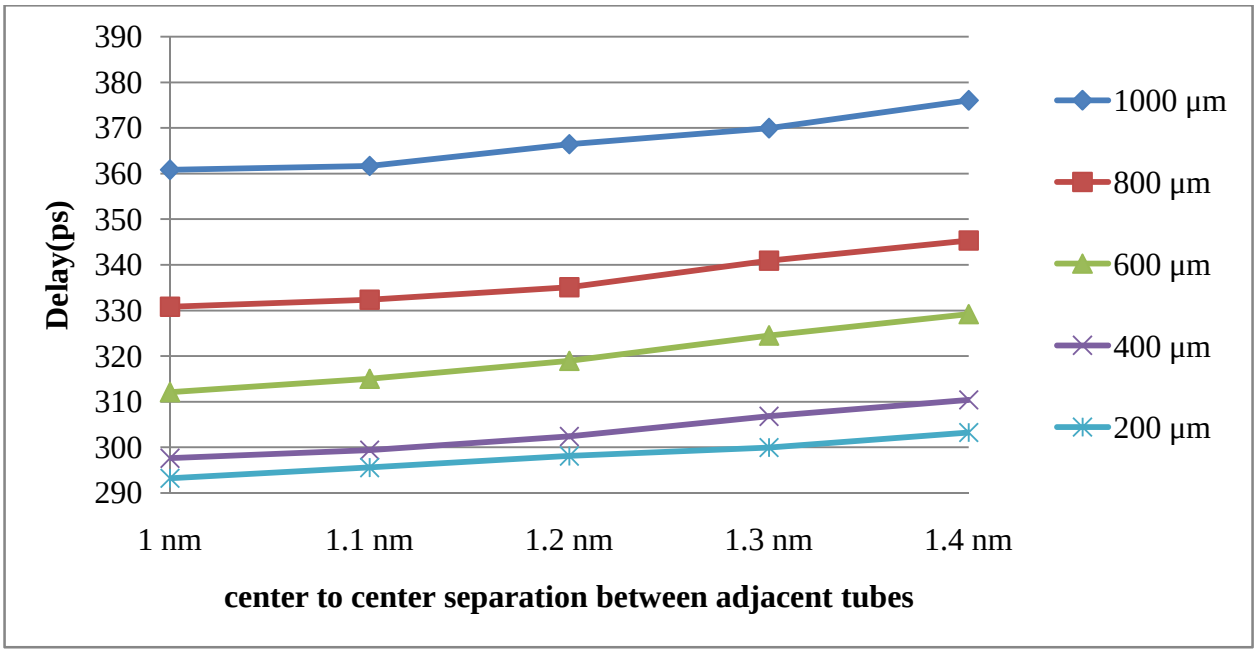

Fig.5.29 Increase in delay with respect to increase in separation between adjacent tubes at 16 nm technology node.

5.5.2 Effect of separation on normalized propagation delay

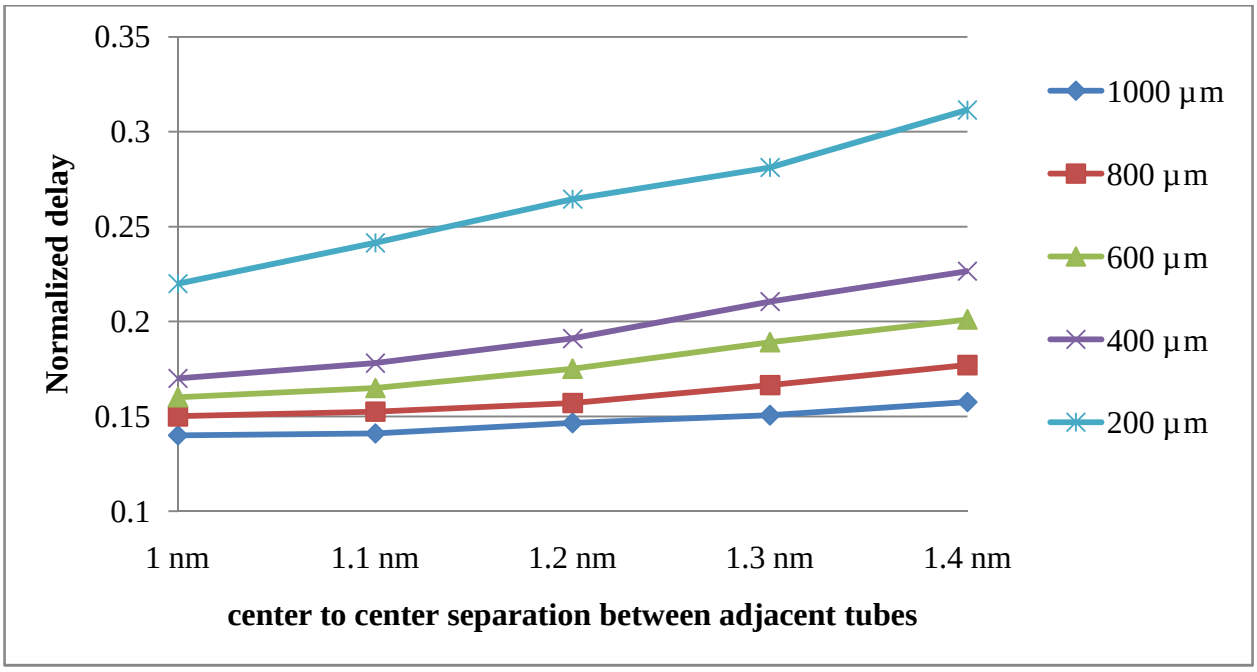

Fig.5.30. Normalized delay vs. centre to centre distance between adjacent tubes at different interconnect lengths at 16 nm technology node.

The normalized delay like the propagation delay increases with separation. Fig.5.30. elucidates this scenario and it is vivid from the Fig that normalized delay increases with increase in interconnect length. The explanations to these occurrences are same as the explanations of 32 and 22 nm technology nodes. Here at 16 nm node, the normalized delay is further reduced as compared to other two technology nodes. Again the reason is same as explained in case of normalized delay at 22 nm technology node.

5.5.3 Effect of separation on power dissipation of SWCNT bundle

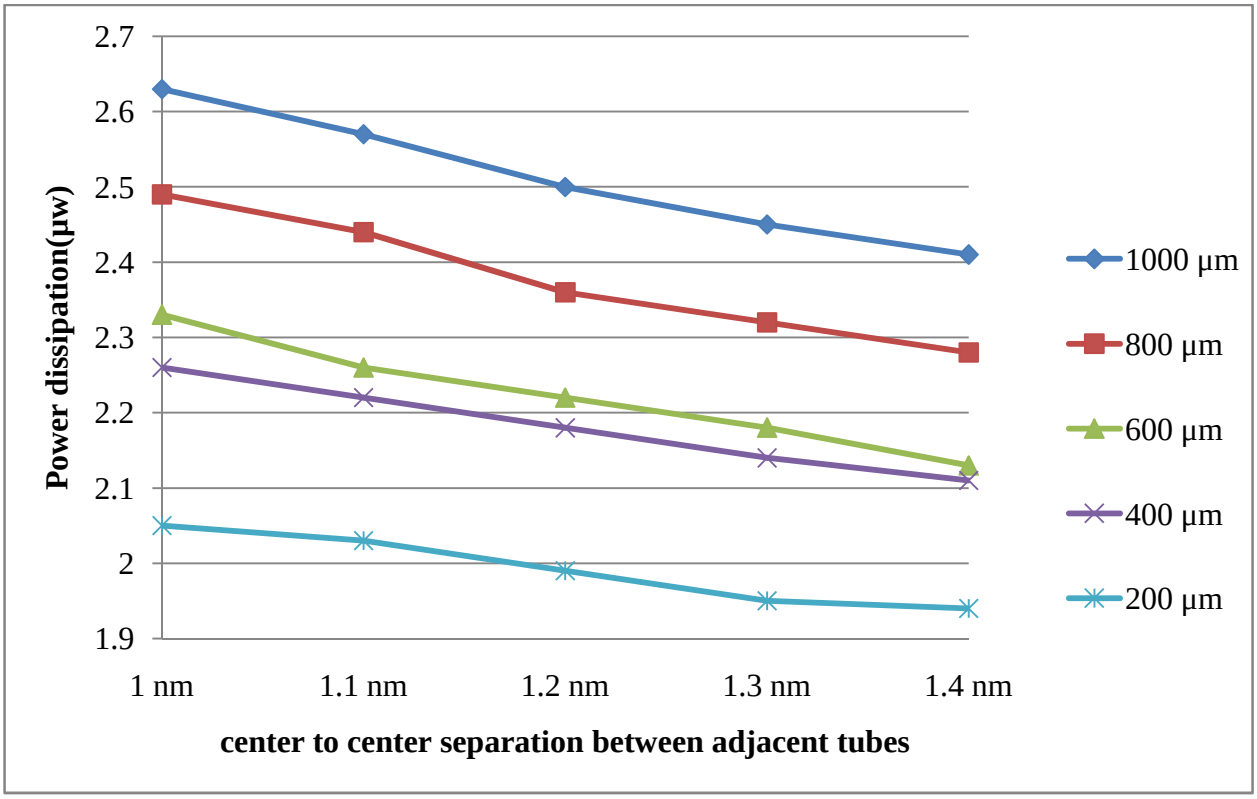

Fig.5.31. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 16 nm technology node.

The increase in center to center separation in Fig.5.31 shows same kind of effect as seen at 32 and 22nm technology node. However, this time the power dissipation is lowest amongst all the three technology nodes and this is true for each and every interconnect length

5.5.4 Effect of separation on normalized power dissipation

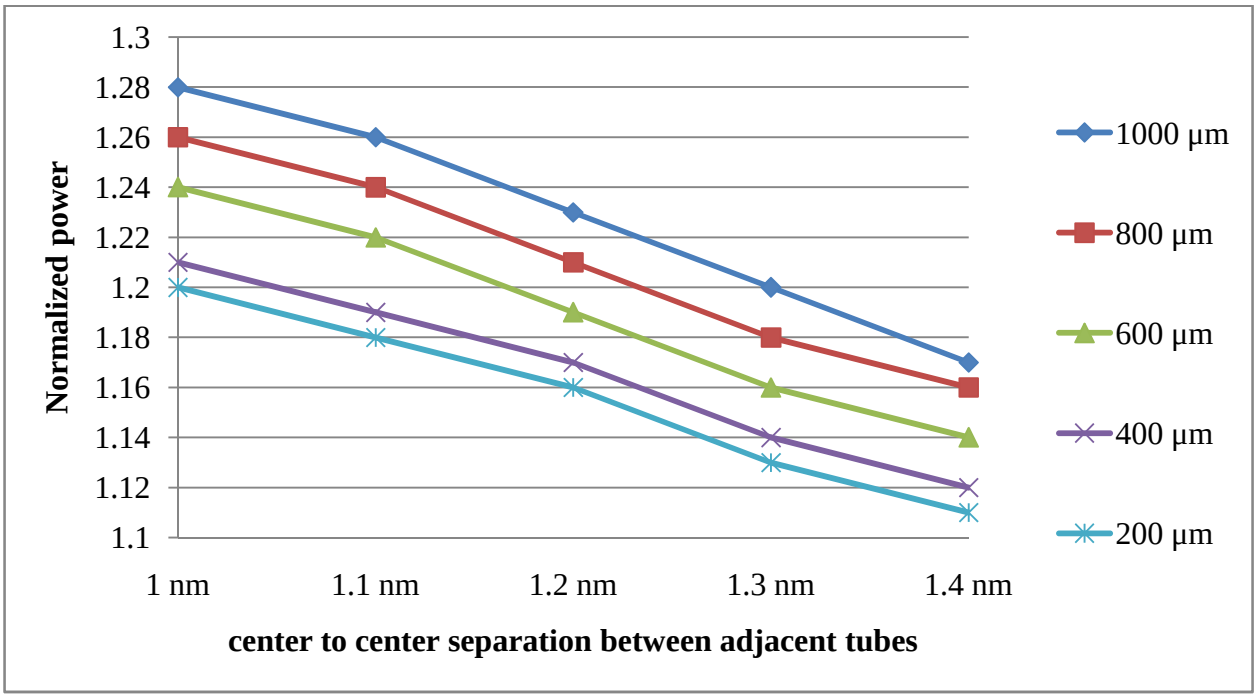

Fig.5.32. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 16 nm technology node.

The normalized delay is plotted against increase in separation between adjacent tubes at 16 nm technology node in Fig.5.32. Just like the actual power dissipation, the normalized power dissipation also does decrease. The normalized power obtained for every interconnect length is minimal in contrast to other two technologies. This clarifies that the performance of SWCNT bundle at 16 nm technology node in terms of power dissipation is better as compared to other two nodes.

5.5.5. Effect of separation on power-delay product of SWCNT bundle

The power delay product of SWCNT bundle interconnect mostly decreases with increase in separation between adjacent tubes as shown in Fig.5.33 .This indicates dominance of power dissipation over propagation.delay.

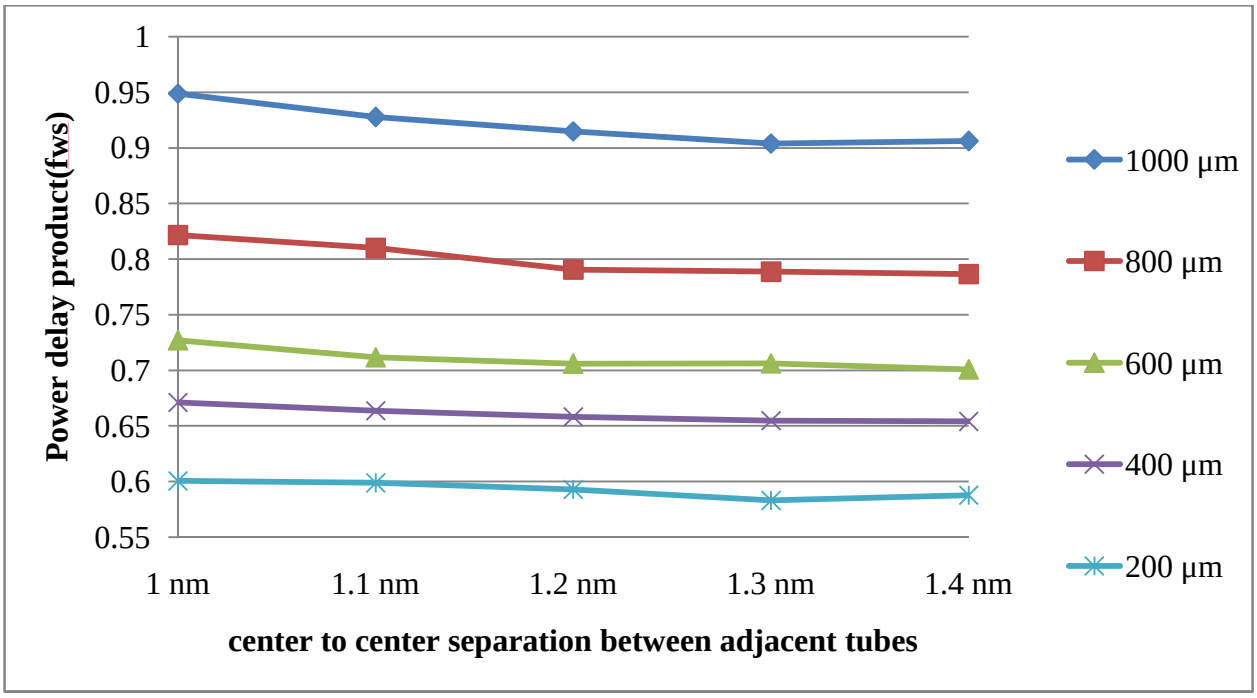

Fig.5.33. Power delay product vs. increase in separation between adjacent tubes at different interconnect lengths at 16 nm technology node.

However, at some points the propagation delay dominates over the power dissipation. As a result, there is a trivial increase in power delay product with respect to increase in separation. The power delay product increases further as the technology is scaled down from 22 nm to 16 nm. It happens because with scaling, the propagation delay increases whereas the power dissipation decreases and it is the increase in delay which overshadows the decrease in power dissipation.

CHAPTER 6 Conclusion and Future scope

CNTs are the promising candidates of future VLSI interconnect. They are mechanically and thermally stable and are prone to electro migration. The resistance of CNT is much lower than copper while the capacitance is larger but the propagation delay of CNT is lower than copper making it suitable for interconnect application and better than copper.

The SWCNT bundle is most desirable form of CNT based interconnect provided all constituent CNTs of the bundle are metallic. In SWCNT bundle interconnects, it is found that isolated tube diameter and separation play an important role in determining delay and power dissipation. Another parameter of importance is the interconnect length. When the interconnect length increases all the impedance parameters increases. This is true for all technologies. It is felt that both SWCNT and MWCNT perform better than copper in the semi-global and global levels of interconnect length.

|It is also seen that the delay decreases by increasing the aspect ratio of repeaters of SWCNT bundle interconnect. This is true for both lumped and distributed model. The delay further decreases when the number of repeaters in a SWCNT bundle interconnect increases. At all technologies, with the increase in separation, the propagation delay increases whereas the power dissipation decreases and the same effect comes into action when the technology is scaled down. To achieve better performance, it is required that the SWCNT bundle should be densely packed, and the separation should be restricted around 1 nm.

The work in this report does not include the effect of temperature change on carbon nanotubes and is needed to be studied. Most of the research is concentrated on the analysis of CNT, however a very little work has been done in the field of fabrication of CNTs and it is needed to be focused in future. The imperfect contact resistance arises due to lack of proper growth techniques of CNTs and therefore study can be done in order to find effective fabrication methods which can reduce contact resistance

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ABSTRACT The work in this report presents the application of Carbon nanotubes (CNTs) as a VLSI interconnect and its superiority over copper interconnect at 32, 22 and 16 nm technology nodes. CNTs are the promising candidates for the future interconnects and it is always used in the bundle form because the resistance linked with an isolated CNT is very high. So, it is mandatory to use them as a bundle. The advantage of using carbon nanotubes in bundle form is that the effective resistance gets divided by number of CNTs in a bundle and as a result of this, the resistance decreases. The impedance parameters of a CNT bundle depend ultimately on the number of CNTs in a bundle. CNTs can outperform copper at the intermediate and global interconnect level. The

SWCNT bundle is most desirable form of CNT based interconnect provided all constituent CNTs of the bundle are metallic. All the impedance parameters have been calculated by performing simulations of impedance equations in MATLAB. It has been observed that all the impedance parameters are directly proportional to the length of interconnect. Moreover, it is observed that the resistance and inductance of interconnect increases with the decrease in technology node whereas it is reverse for capacitance. An equivalent single conductor model has been proposed for calculating the propagation delay and power dissipation. SPICE Simulation tool has been used to calculate the propagation delay and power dissipation. Optimum CMOS driver size ratio and effect of insertion of repeaters in a SWCNT bundle has been analyzed. Moreover, it is shown that the influence of center to center separation of adjacent tubes in a SWCNT bundle plays an important role in determining the propagation delay and power dissipation. As the bundle density is decreased the corresponding delay increases but at the same time power dissipation decreases. Furthermore, it has been discussed that keeping the adjacent shells in a SWCNT at a minimal distance can enhance the performance of SWCNT interconnect. CHAPTER 1 INTRODUCTION Interconnects act as a path for the signals propagating in an integrated circuit connecting one node to the other node and also provide connection to the nodes of one block to the nodes of other block. Basically it is a conducting material of thin film which is used to provide an electrical connection between one node of a circuit to the other node of a circuit. There are three types of interconnects: local, intermediate, and global . • Local interconnects are used for connecting gates, and transistors within a functional block They consist of very thin film. The length of local interconnect is about few micrometers . • Intermediate interconnects are used to provide connections within the functional block but are larger in length than local interconnects up to few hundreds of micrometers. They've the ability to provide low resistance path [2]. • Global interconnects are used to provide electrical connection from one functional block to the other block. The length of global interconnect is about few millimeters. In past aluminum was used as an interconnect material because of its following properties:- ? Low resistivity [3] ? Good Conductivity ? Ease of deposition ? Dry etching ? Does not contaminate Si ? Excellent adhesion to dielectrics. It also forms good ohmic contact with silicon. Despite of its goodness it also has certain disadvantages:- ? Electro-migration ? Higher resistivity ? Short mean free path of the order of few nanometers. As we move down with the technology scaling [1], current density of the interconnect is increased. At higher current densities electro-migration [4,5] (it is the transportation of material due to the movement of the ions in a conductor) takes place. 1.1 Copper interconnect As the electro-migration problem in aluminum [7] was troubling the performance of interconnect at lower technologies, there was a dire need of better interconnect. So copper came as a strong contender for interconnect which has higher conductivity and has less issues of electro migration than aluminum [28]. Because of the advantages of copper over aluminum it appeared as a widely used metal for interconnect, particularly for the IC's which demands high performance. Fig.1.1 A basic copper interconnect structure 1.1.1 Resistance of copper interconnect The resistance associated with the copper interconnect depends mainly on the resistivity of copper, it varies directly proportional with resistivity as well as its length. However, it is inversely proportional to the area of copper interconnect. So the analytical expression for the resistance can be written as R ? W.H ?.L (1.1) In equation (1.1) 'ρ' represents the resistivity of copper interconnect and 'L' is the length of interconnect.'W' and'H' denotes the width and height of copper interconnect respectively. 1.1.2. Inductance of copper interconnect The inductance coupled with copper interconnect is due to the changing current in it. A magnetic field is produced by the

action of this changing current which in turn produces a voltage in the circuit, therefore an inductance is produced which is known as self inductance [8] and is given by the formula. LS ? ?.L ? ? 2L ? 1 ? 0.22 ?W ? H ? ?? 2? ??ln ?? W ? H ?? ? 2 ? ? L ??? ? (1.2) In equation (1.2) 'LS' and 'μ' is the self inductance and permeability of copper respectively. On the other hand 'W','H' and'L' is the width, height and length of copper interconnect respectively. 1.1.3. Capacitance of copper interconnect On scrutinizing the interconnect structure of copper in Fig.1.1, it is lucid that it is fixed at distance 'Y' above the ground plane. This separation 'Y' is filled with a dielectric material of permittivity 'ε'. As a result, interconnect and the ground plane behaves as the conducting plates of a capacitor. When the signal is passed through the interconnect it acquires some charge and act as parallel plate capacitance. Nevertheless, the thickness of the interconnect is quite evident therefore creating fringing electric fields which contributes to another type of capacitance known as fringing capacitance. Consequently, the total capacitance (Cg) of copper interconnect is the addition of parallel plate capacitance and fringing capacitance, which is given by the formula in equation (1.3). ?w ? 2.22 ?? S ? 3.19 S 0.76 Cg ?????Y ? ? H ?0.12 ? ? S ? 0.7Y ? ? ?1.17??? S ? 1.15Y ? ? ? ? H ? 4.53Y ? ? ?? ? (1.3) In equation (1.3) 'W' and 'H' is the width and height of copper interconnect respectively whereas 'S' is the spacing , 'Y' is the height above ground and 'ε' is the permittivity [15]. These formulas will be required for the calculating the propagation delay and power dissipation of copper interconnect. Previous studies have proved that copper is still a good choice for interconnect at local length and for technology nodes above 45 nm. However, when the technology node is further degraded, the choice of copper as an interconnect could be a wrong choice as it offers high resistivity at lower technology nodes. Fig.1.2. Resistivity of copper as a function of wire width at various technology nodes It is vivid from Fig.1.2 that resistivity of copper escalates exponentially when the technology node is reduced below 45nm. It means the resistance of interconnect increases exponentially with the reduction of technology. When the feature size is reduced below 45 nm the enhanced grain boundary scattering and surface scattering [10,11] results in increase in scattering resistance of the interconnect. The interconnect delay is increased exponentially with the reduction of technology while the power dissipation of the circuit is not reducing at the same 5 rate causing power per unit area to increase. Due to this problem, there is a dire need to replace copper as VLSI interconnects at global level. Researchers have proposed carbon nanotubes as a perfect material for the interconnects [12] and for the upcoming technology. 1.2 Carbon nanotubes Carbon nanotubes(CNTs) are made up of an allotrope of carbon called graphene. It is fabricated by rolling graphene layers in the shape of cylinders. They have diameter in the range of nanometers that is why they have got the name nanotubes [18,19] . The CNTs will be either metallic or semiconducting and this depends on the direction in which the grahene layers are rolled up. Only the metallic CNTs participate in the current conduction [16,17] whereas the semiconducting CNTs are of no use and hence do not participate in current conduction. The growth of CNT is done in the shape of flawless cylinders and it's wall is formed by layer of graphene. As far as the research till now is concerned, carbon nanotubes have been proved to be the best interconnect material [21] for the integrated circuits manufacturing. They have shown extremely favorable results in terms of propagation delay at lower technology nodes. 1.2.1 Advantages of CNT over COPPER ? High mechanical stability ? High thermal stability ? High thermal conductivity ? Large current carrying capacity [20] ? Lower resistivity ? Mean free path of the order of 1000 nm. Table.1.1 Comparison of CNT and copper Properties CNT Copper Maximum current density (A/cm2) Mean free path (nm) Greater than 1000 40 Greater than 10^10 ~10^6 Thermal conductivity (W/mK) 5800 385 Table.1.1 represents an

evaluation of properties of CNT and copper as an interconnect. It can be clearly seen that CNT is superior to copper in terms of mean free path, maximum current density and thermal conductivity. 1.2.2 Classification of CNTs CNTs are broadly classified under two categories, ? Single-walled carbon nanotubes (SWCNTs) ? Multi-walled carbon nanotubes (MWCNTs). Fig.1.3 Single walled carbon nanotubes [1] SWCNT is made up by rolling a thin layer of graphene and it consists of only one layer [6] while the MWCNT consists of multi layers (more than two layers) of graphene of different diameters rolled up in a concentric form. The SWCNT can be used as VLSI interconnects [7- 9] because the electron mean free path of SWCNT is more than 1000 nm [27]which results in lower resistivity. Due to the high resistance linked with a single CNT which is more than 6.45 KΩ poses a restriction that we should use a bundle of CNTs which consists of large number of isolated CNTs in parallel. The number of shells in a MWCNT and number of metallic SWCNTs decides the impedance parameters MWCNT and SWCNT bundle respectively. In a SWCNT bundle, some of the nanotubes are semiconducting while others are metallic. Only metallic CNTs contributes to current conduction and formation of interconnect. The semiconducting CNTs never take part in the current conduction.Large numbers of CNTs in a multi-walled CNT are metallic. On the other hand a large number of CNTs in a SWCNT bundle are semiconducting. A MWCNT with two shells is double walled CNT. This form of CNT has been found to be a very useful for application as interconnects. It is very difficult to achieve ballistic transport [29] for MWCNTs for a long length [10-11] whereas SWCNTs have mean free path of the order of a micron due to its diameter in nano range. SWCNTs has only one shell with diameter ranging from 0. 33nm to 5.0nm and lengths from 2nm to 10nm, whereas MWCNTs has several concentric shells [39] with diameter ranging from several nanometers to tens of nanometers and length of several microns. Fig.1.4. Multi-walled Carbon nanotubes [1] On the basis of circuit simulation researchers reported that an SWCNT-bundle interconnect provides the low-resistivity advantage over copper when the bundle length is semi-global or global. 1.3 Equivalent Circuit Model for an Isolated Single Walled Carbon Nanotube Fig.1.5. Equivalent Circuit Model for an Isolated Single Walled Carbon nanotube [9]. The equivalent circuit model for isolated single-walled carbon nanotubes is shown in Fig. 1.5. The model and its components are explained in detail in the following subsections. 1.3.1 Isolated SWCNT Resistance The conductance of a CNT is analyzed using the two terminal Landauer Buttiker formula. According to this formula, for a single dimension system with 'n' number of channels. The conductance is directly proportional to the number of channels [24,25]. Each carbon nanotubes has four number of conducting channels which results in a resistance of 6.45 KΩ. This is the quantum resistance also known as fundamental resistance is involved with the single walled carbon nanotubes. This resistance can't be avoided as is divided equally between two opposite sides of CNT. RF ? 4e2 h (1.4) The mean free path of carbon nanotubes is about 1μm. The mean free path is defined as the distance travelled by an electron until scattering occurs. For carbon nanotubes which have length shorter than 1μm, the resistance is independent of length. The resistance of carbon nanotubes increases when length of carbon nanotubes becomes larger than mean free path. For an isolated single walled carbon nanotube, in addition to the fundamental resistance a scattering resistance appears which varies with length of SWCNT. The formula [30] for the scattering resistance is given below in equation (2) RCNT ? ??? 4he2 ??? LLo (1.5) In actual, the calculated resistance of CNT is much larger than the sum of fundamental and scattering resistance. This is because of imperfect contact of metal and carbon nanotubes, which is called contact resistance. The imperfect metal-carbon nanotubes contact resistance (RC) of carbon nanotubes ranges from few ohms to 100 KΩ. Therefore it can be concluded that the

total resistance is the sum of quantum resistance, scattering resistance and metal- carbon nanotubes imperfect contact resistance The total resistance involved with the isolated single walled carbon nanotubes is very high. Therefore it is required that a bundle of carbon 9 nanotubes is to be used as an interconnect. Equation (1.6) represents the total isolated resistance of aSWCNT. RIsolated ? RF ? RC ? RCNT (1.6) The advantage of using a SWCNT bundle as interconnect is that the total resistance gets divide by total numbers of CNTs in the bundle. 1.3.2 Isolated SWCNT capacitance The capacitance of Carbon nanotubes is from two sources. The first one is the electrostatic capacitance (CE) which is calculated by considering the Carbon nanotubes as a thin wire, of diameter 'd', positioned at a distance 'y' above the ground plane. The electrostatic capacitance is calculated per unit length. It is reported to be 30 aF/um for y=1 μm and d=1 nm. Another capacitance which is involved with the isolated single walled carbon nanotubes is the quantum capacitance which is due to the quantum electrostatic energy stored in the nanotubes when it carries current. Fig. 1.6.Isolated carbon nanotube with diameter 'd' placed at a distance 'y' above ground plane.[8] CE ? ln ??? dy ??? 2?? CQ ? 2e2 hvF (1.7) (1.8) When this quantum electrostatic energy is equated to capacitance, the formula for quantum capacitance is realized and is shown in equation (1.7). This capacitance is also realized as per unit length. Here in equation (1.8) 'vF' is the Fermi velocity and 'h' is the Planck's constant. For a CNT the Fermi velocity is reported to be 8x105 m/s. Thus, the quantum capacitance becomes equal to 100aF/um. There are four conducting channel in a carbon nanotubes so the total quantum capacitance results from four parallel capacitances and is noted to be 4CQ. In the effective circuit model, both of the electrostatic quantum capacitance appears in series. 1.3.3 Isolated SWCNT Inductance. The inductance of the isolated Single walled carbon nanotubes arises from two factors. First one is the magnetic inductance(LM) and the second is the Kinetic inductance(LK).the magnetic inductance is due to the magnetic field which comes into play when an isolated current carrying wire is placed at some distance above ground plane. The Kinetic inductance is due to the kinetic energy stored in each conducting channel. LM is reported to be 1.4 pH/um when d=1nm and y=1μm. on the other hand LK is known to be 16 nH/μm. LK does have considerable impact on delay calculation of interconnects. The formula for LM and LK is shown below in equation (1.9) and equation (1.10) represents the isolated SWCNT inductance LM ? 2? ln ??? dy ??? , LK ? ? h 2e2vF LCNT ? LK ? LM (1.9) (1.10) 1.4 Bundled SWCNT A bundled SWCNT consists of a large number of SWCNTs. The SWCNTs inside a bundle are arranged in parallel. The inter-CNT distance between one CNT and the other CNT is 0.34 nm. This is the minimum distance that must be maintained between CNTs. This distance is determined by vander-wall gaps [33,34]. The diameter of SWCNT is typically about 1 nm. So the center to center distance between CNTs is about 1.34 nm. Here in Fig1.7 a view of SWCNT bundle is shown. Some SWCNT bundle parameters are shown like 'x' which is center to center distance of CNTs. HB is the height of SWCNT bundle and WB is the width of the bundle and'd' is the diameter of a single CNT inside the bundle. The bundle is placed at a height ht above the ground plane. Fig.1.7. SWCNT Bundle placed at a height ht above the ground plane [17]The total number of SWCNTs in a bundle can be calculated by following formula given in equation (11) and (12). Here 'd' is the diameter of Single walled carbon nanotubes and'x' is the distance between center to center of the neighboring tubes of the SWCNT bundle nCNT ? nW nH ? H , If nH is even n 2 (1.11) = nW nH ? nH ?1 2 , If nH is odd (1.12) Where nW ? WB ? d and nH ? H B ? d ? 1 x 3 2 x nH indicates the number columns and nW indicates the number of rows in a single walled carbon nanotubes bundle. nCNT denotes the total number of carbon nanotubes in the bundle 1.5 Equivalent model for SWCNT bundle The equivalent circuit

model for SWCNT bundle is represented by Fig. 1.8. In this Figuret, the RCNT / nCNT,Lbundle,CbQundle and CEbundle are the distributed parameters. Fig.1.8 Equivalent model for SWCNT bundle [8] 1.5.1 SWCNT bundle resistance For calculating the effective resistance of a single walled carbon nanotubes bundle, it has been assumed that all the CNTs in the bundle are metallic in nature and are supposed to be conducting. The SWCNT bundle resistance is shown below in equation (1.13). Here in equation (1.13) nCNT is the number of carbon nanotubes in a bundle and Risolted is the isolated carbon nanotubes resistance. Rbundle ? nCNT Risolated (1.13) 1.5.2 SWCNT bundle capacitance Single walled carbon nanotubes bundle effective capacitance is the addition of quantum capacitance and electrostatic capacitance. The effective electrostatic capacitance of the SWCNT bundle is shown in equation (1.14). The total effective capacitance [20,21] of bundle of SWCNT is given by equation (1.16), where $CEBundle$ and $CQBundle$ are the total electrostatic capacitance and total quantum capacitance of SWCNT bundle. CEn and CEf are the intrinsic plate capacitances and nW and nH are the number of columns and number of rows in an interconnect bundle. The total electrostatic capacitance of the bundle is given by equation (1.14) CEbundle ? 2CEn ? nW ? 2 CEf ? 3 ? nH ? 2? 2 5 CEn (1.14) Here CEn and CEf are the intrinsic plate capacitances and nH and nW are the number of rows and number of columns in a single walled carbon nanotubes bundle respectively. Another capacitance which is associated with SWCNT bundle is the quantum capacitance [38]. Since the individual quantum capacitances of the carbon nanotubes are in parallel. So, the total quantum capacitance is the sum of all the isolated quantum capacitances of all the carbon Nanotubes forming a CNT bundle. The formula for the quantum capacitance of a CNT bundle is shown below in equation (1.15). Here $CQCNT$ is the quantum capacitance of an isolated single walled carbon nanotubes and nCNT is the total number of CNTs in the bundle. CQbundle ? CQCNT .nCNT (1.15) The net capacitance of SWCNT bundle is calculated by the series combination of quantum and electrostatic capacitance and is given by Cbundle in the equation (1.16) below. 1 ? bundle ? bundle 1 1 (1.16) Cbundle CQ CE 1.5.3 SWCNT bundle Inductance The SWCNT bundle inductance is given by the parallel combination of the magnetic and kinetic inductance. Since LK (Kinetic inductance) is large enough as discussed earlier so it is excluded from delay calculations [36]. Isolated SWCNT is given by LCNT ? LK ? LM . Thus the total SWCNT bundle inductance can be calculated by dividing isolated SWCNT inductance by number of carbon nanotubes in a bundle, which is given by equation (1.17) Lbundle ? CNT L (1.17) nCNT 1.6 Thesis Organization CHAPTER 1- A brief introduction has been given about carbon nanotubes and also about their classification. Equivalent models of isolated CNT and SWCNT bundle has been discussed, based on the models, impedance parameters has been determined CHAPTER 2- This chapter puts emphasis on the literature survey and the work which has been done till now in the field of CNTs. CHAPTER 3- Based on the literature survey, research gaps have been found which will form the basis of this report work. CHAPTER 4- Based on the research gaps some objectives are defined and a methodology is proposed to attain the required objectives. CHAPTER 5- This chapter deals with the results obtained for effect of center to center separation between adjacent tubes on performance of SWCNT bundle and its comparison with copper at various technology nodes. CHAPTER 6- This chapter forms the conclusion of the report and the future scope of CNTs has also been discussed. CHAPTER 2 LITERATURE REVIEW Effect of scaling of interconnections on the time delay of VLSI circuits [1] -Krishna C. Saraswat and Farrokh Mohammadi They explained that the interconnect delay dominates the device delay. It is due to the reason that integrated circuit area is increased and the device dimensions are decreased simultaneously. In their paper they talk about scaling of integrated circuit and minimum

feature size. Scaling means increase in IC size and reduction in minimum feature. The delay is associated with scaling. Analytical expressions are developed which can associate delay with a variety of physical parameters like the material used for the interconnect, interconnect length, minimum feature size and IC area. After that Empirical expressions are discussed. On the basis of Empirical expressions they have said that when the IC area is increased the interconnect delay becomes more important than device delay. Optimal Interconnection Circuit for VLSI [2] -H. B. Bakoglu et al. This paper proposed that for observing the performance of a VLSI circuit, the propagation delay of interconnect is an important factor. When the IC size is enhanced and dimensions of interconnects are scaled the delay increases sharply. For calculating the delay they proposed a model which can give detail about the effects of scaling MOSFETs, interconnects and IC dimensions. They have presented a comparison of poly silicon interconnect and aluminum and also discussed about the interconnect delays of forthcoming VLSI circuits. By using repeaters the delay can be reduced. Others options for reducing delay are the use of cascaded drivers and appropriately scaled multilevel conductors. They have presented a model which can successfully reduce the propagation delay to a good extent because it uses most favorable interconnect parameters and repeaters. Performance analysis of carbon nanotubes interconnects for VLSI applications [9] -Navin Srivastava and Kaustav Banerjee This paper talks about using single walled carbon nanotube (CNT) bundles as an interconnect for VLSI circuits, by keeping in mind the aspects where this technology can lack. They have proposed equivalent circuit model for both isolated single walled CNT and bundle of single walled CNTs. A comparison of copper interconnects and SWCNT bundle interconnects has been presented in terms of propagation delay at all different levels of interconnects. By this paper it can be concluded that single walled CNTS can perform better than copper at global and intermediate level while copper performance is outstanding as compared to single walled CNT bundle in terms of delay. The necessities that are required to carbon nanotubes feasible to use them as next generation interconnects were presented. Control of SWCNT interconnect performance by tube diameter[16] -Mayank Kumar Rai et al They presented a study on the isolated CNT diameter inside a SWCNT bundle. The study talks about how the isolated CNT diameter can manipulate the bundle delay. Their study shows that because of the lower resistance of single walled CNT bundle interconnects, the delay is lower than copper interconnects. Delay increases directly proportional to the isolated CNT diameter. As the diameter increases the number of CNTs inside a bundle reduces which results in increase in resistance and hence increase in delay. So a minimum diameter of CNT must be chosen. On the applicability of single-walled carbon nanotubes as VLSI interconnects [17] -Navin Srivastava et al This paper presented a detailed study on using of single-walled CNTs as interconnects for deep submicron integrated circuits. A complete study on the impedance parameters of SWCNT bundle interconnect is done. Various types of resistances involved with the interconnects have been discussed like quantum resistance, contact resistance and scattering resistance. Two types of inductances are discussed namely magnetic inductance and kinetic inductance out of which kinetic inductance is not included in delay calculations because kinetic inductance is very greater than magnetic inductance and it has an important effect on 17 delay calculations. Different kind of inductive effects are presented. Vias are discussed which are also known as vertical interconnects. It has been reported that the delay is reduced by 40% in global interconnects. After that it is shown that dense CNT bundles can perform better than spatially packed CNT bundles because number of CNTs increases in a densely packed CNT bundle. This in turns decreases the resistance of the bundle interconnect and hence the delay

decreases. On the other hand number of CNTs in a bundle decreases in a spatially packed CNT bundle. So the resistance increases and hence the delay increases. When the delay increases the power dissipation decreases. So a trade off is required between them. Analyzing Carbon Nanotube Interconnects in VLSI Application [19] -Mahmudur Rahman, Ahrar Ahmed Chowdhury In this paper the electrical properties of carbon nanotubes as an interconnect in VLSI circuits have been analyzed. Accordingly, the effectiveness of metallic SWNT interconnect has been studied using Raman spectroscopy for its outstanding ballistic conductivity, low resistance and low capacitance. The performance analysis of SWCNT bundle based on RLC parameters is discussed. Impact of Resistivity on MWCNT, SWCNT bundles with full and one-third metallic portion is studied and by using this result, the paper concludes that metallic interconnects is the future of VLSI technologies. Performance Comparison between Single Wall Carbon Nanotubes Bundle and Multiwall Carbon Nanotubes for Global Interconnects [21] -Manoj Kumar Majumder et al. This paper proposed a full detail about the delay for single walled carbon nanotubes and multi-walled carbon nanotubes at different interconnect lengths. They have also specified number of carbon nanotubes required for a particular delay in a SWCNT and number of shells required for a particular delay in a MWCNT. By using one-dimensional fluid theory they have revised the models of single walled CNTs and multi walled CNTs. Propagation delay is discussed for both the models at deep submicron technology. They have come to conclusion that it doesn't matter what type of CNT it is. The delay is directly proportional to the length of the interconnect. If same delay is required for single walled and multi-walled carbon nanotubes, then the number of single walled CNTs should be greater than the number of shells in a multi walled CNT. Estimation of Time Delay and Repeater Insertion in Multiwall Carbon Nanotube Interconnects [23] - Feng Liang, Gaofeng Wang, Wen Ding This paper uses a finite difference time domain (FDTD) method on a derived equivalent single conductor model for interconnect line. Based on this a 50% time delay analysis is performed for a driver-interconnect-load structure using SPICE simulation. In this paper a CMOS gate is used as a driver for interconnect line. Based on the simulation results the impact on propagation time delay with the variation of length at intermediate length has been plotted for 14nm and 22nm technology nodes. Simulations are also carried to study the optimum number of repeaters needed by MWCNT and copper at 1000μm intermediate length and at 2000μm and 5000μm global length. The paper concludes that the propagation time delay in MWCNT is much less than that observed in copper at global, intermediate level. The number of repeaters used by MWCNT at a particular length is one third of that used by copper in order to reduce the time delay. Comparison of Propagation Delay Characteristics for Single-Walled CNT Bundle and Multi-walled CNT in Global VLSI Interconnects [24] -Manoj Kumar Majumder et al. This paper presented a broad discussion of single-walled carbon nanotubes bundles and multi walled carbon nanotubes. The propagation delay is discussed at global interconnect lengths. They have also stated the area required for an equal number of single walled CNTs and number of shells in a multi walled carbon nanotubes. They stated that it does not matter what is the type of CNT. The delay increases with increase in interconnect length. For the same delay, equal number of CNTs in SWCNT bundle and number of shells in MWCNT the area required for SWCNT bundle is more than MWCNT Influence of distance between adjacent tubes on SWCNT Bundle interconnect delay and power dissipation [30] -Mayank Kumar Rai and Sankar Sarkar This paper analyzed the influence of separation between adjacent tubes in a single walled CNT bundle of various lengths and tube diameters, on power dissipation and delay of the bundle. Calculations have been done on the impedance parameters

and the outcomes are compared with copper interconnects at 22nm technology node. SPICE simulations have been done and it is observed that if the distance between adjacent tubes inside a SWCNT bundle is increased then the delay is also increased in the same proportion. Its true for the entire range of length values and tube diameters whereas the opposite is correct for power dissipation. Analysis of delay and dynamic crosstalk in bundled carbon nanotube interconnects [34] -B.K Kaushik, Manoj Kumar Majumder and Sanjeev Kumar Manhas. They explained that by mixing SWCNTs and multi-walled CNTs in an arranged fashion can form an interconnect which can provide solutions to many problems in deep submicron technology. Such types of structures are called mixed carbon nanotube bundles (MCBs). They have discussed different kind of random fashion structures and well arranged structures of MCBs. MCBs are formed by placing SWCNTs and MWCNTs inside a single bundle. After that an equivalent circuit model of the MCB has been discussed. Through this model, the dynamic crosstalk performance and propagation delay of the structures of MCBs are calculated. From the calculations it is seen that propagation delay as well as dynamic crosstalk are reduced to much extent. The reduction is more in a MCB if the constitutes are packed spatially and the MWCNTs are placed around the SWCNT bundles which are placed at the center of the MCB. When the well arranged MCBs are compared to the MCBs which contains SWCNTs in a random fashion the average delay is reduced in well arranged MCBs. . CHAPTER 3 RESEARCH GAPS Carbon nanotubes as VLSI interconnect is an excellent candidate for the forthcoming IC design. The work presented in the literature shows that CNT can outperform copper and has the ability to replace copper in the field of interconnects. As the technology is scaled down CNT becomes more efficient as compared to copper because mean free path of copper is 45 nm. Below 45 nm technology node copper is not a suitable candidate. Therefore, CNT will be suitable candidate at technology nodes below 45 nm. The work in the literature review has been done on SWCNT bundle and MWCNT and also on the mixed CNTs. The SWCNT bundle is most advantageous form of CNT based interconnect given that all component CNTs of the bundle are metallic. The effect of separation of adjacent tubes in a SWCNT bundle plays an important role in the interconnect delay and power dissipation. The delay increases with an increase in the separation between adjacent tubes for the entire range of length values and tube diameters but the opposite is true for power dissipation i.e power dissipation decreases with increase in separation. This happens because with increase in separation, the number of CNTs in a bundle decreases the result of which is that resistance and inductance of the bundle increases but the capacitance decreases because resistance and inductance are inversely proportional to the number of CNTs but capacitance is directly proportional to the number of CNTs. The center to center distance between adjacent shells is equal to the distance from the center of one CNT to the center of other CNT. In this case, the CNTs are densely packed and separation is equal to the diameter of single CNT. Work has been done on sparsely packed CNT bundle whose center to center separation is greater than the diameter of CNT. Apparently, the densely packed bundles gives higher performance in comparison to those which are sparsely packed. Therefore, a higher performance trade-off between propagation delay and power dissipation can be analyzed for densely packed SWCNT bundle. By varying the separation interconnect delay and power dissipation can be altered. CHAPTER 4 OBJECTIVE Based on the research gaps discussed in CHAPTER 3 the following objectives are proposed. 1. To study the effect of center to center separation between adjacent tubes in a SWCNT bundle on impedance parameters at 32 nm, 22 nm and 16 nm technology nodes. 2. To realize an equivalent single conductor model for SWCNT bundle and simulate it using SPICE simulation tool. 3. To compare the results of delay and power dissipation

for SWCNT bundle with copper at 32, 22 and 16 nm technology nodes. PROPOSED METHODOLOGY To analyze SWCNT bundle as an interconnect and to compare it with copper, impedance parameters from equations (1.1),(1.2),(1.3) and (1.13),(1.16),(1.17) for copper interconnect and SWCNT bundle respectively have been calculated in MATLAB. The equivalent single conductor circuit diagram for SWCNT bundle interconnect as shown in Fig.4.1will be spice simulated in tanner tools. Fig.4.1. Equivalent single conductor model for SWCNT bundle interconnect The work will be mostly concentrated on distributed model of SWCNT bundle interconnects. The input to the circuit will be provided by a 2 MHz pulse with rise time and fall time of 1ps. The circuit will be driven by a CMOS inverter and capacitor of 1fF will be taken as a load. A 1000 μm global interconnect will be selected and next step will be to increase the W/L ratio of CMOS driver in 10,20,30,40 and so on until an optimum value is achieved, the value at which 23 power-delay product is minimum. That ratio will be selected as a universal ratio for all other calculations of delay and power in particular technology node. Apparently, Optimum value may be achieved at different W/L ratio for different technology nodes. Subsequently, repeaters will be inserted (as shown in Fig.4.2) which will decrease the delay. Fig.4.2. Repeaters used in ESC model. The number of repeaters [23] which have minimum power delay product will be used for the rest of delay and power calculations. The same W/L ratio and number of repeaters will be used for other interconnect lengths at particular technology nodes. For the ease of comparison both SWCNT bundle and copper interconnect will be provided same conditions like input pulse, load capacitance, W/L ratio and number of repeaters used. CHAPTER 5 RESULTS AND DISCUSSIONS To study the performance of SWCNT bundle interconnect with respect to variation in distance between adjacent tubes and to compare with its rivalry which is copper interconnect, we first need to evaluate the impedance parameters of both SWCNT bundle and copper interconnect. This has to be done by performing coding of impedance equations in MATLAB. Structure parameters used for calculations have been taken from ITRS 2013. The performance of SWCNT interconnect is to be analyzed at 32,22 and 16 nm technology node at different interconnect lengths and also by varying the distance between neighboring shells inside a SWCNT bundle at all the three technology nodes. Table.5.1 Structure parameters of interconnect from ITRS 2013[33] Parameters Technology node 32 nm 22nm 16 nm Wire width(nm) 40 28 18 Wire height (nm) 120 84 54 Oxide thickness(nm) 93.6 65.5 40 Relative permittivity of dielectric 2.77 2.59 2.31 VDD(volts) 0.9 0.8 0.7 Resistivity of copper (μΩ.cm) 3.66 4.2 5.66 5.1 Copper interconnect delay First of all, the impedance parameters of copper interconnect are calculated by performing coding of impedance equations of copper in MATLAB as described in CHAPTER 1 at various interconnect lengths. All the ITRS 2013 structure parameters are taken into consideration while calculating these impedance parameters. The following tables has been obtained for copper interconnect impedance parameters at 32, 22 and 16 nm technology node with the help of MATLAB. Table.5.2.Impedance parameters of copper at 32 nm technology node Length of Impedance parameters(32 nm) interconnect(μm) Resistor(KΩ) Inductance(nH) Capacitance(fF) 200 1.525 0.33 16.939 400 3.05 0.723 33.87 600 4.575 1.133 50.82 800 6.1 1.558 67.75 1000 7.625 1.992 84.70 Table.5.3.Impedance parameters of copper at 22 nm technology Length of Impedance parameters(22 nm) interconnect(μm) Resistor(KΩ) Inductance(nH) Capacitance(fF) 200 3.572 0.348 15.84 400 7.143 0.752 31.67 600 10.72 1.176 47.52 800 14.29 1.615 63.35 1000 17.85 2.063 79.20 Table.5.4.Impedance parameters of copper at 16 nm technology node Length of Impedance parameters(16 nm) interconnect(μm) Resistor(KΩ) Inductance(nH) Capacitance(fF) 200 11.70 0.365 14.34 400 23.41 0.787 28.69 600 35.12 1.23 43.03 800 46.83 1.685 57.38 1000 58.53 2.152 71.73 On having a keen glance at

tables.5.2,3 and 4, it is noticed that all the impedance parameters are increasing as the interconnect length is expanding. This is due to the fact that all these parameters R, L and C are directly proportional to the length. Another observation which is worth noticing is that as the technology node is scaled down, the resistance and inductance of copper interconnect augment while the capacitance decreases. The reason behind this is, when the technology is scaled down the width and height of the interconnect reduce. The relation of resistance and inductance with the width and height is inversely proportionate. On the contrary, width and height of interconnect is directly proportionate to the capacitance. The following table 5.5 depicts the delay calculated for copper interconnect delay at 32, 22 and 16 nm technology nodes for lumped model. Table.5.5 Copper interconnect delay for lumped model Length of interconnect(μm) Copper interconnect delay(ns) 32 nm 22 nm 16 nm 200 0. 635 0. 647 0.870 400 1.35 1.46 2.46 600 2.21 2.55 4.85 800 3.19 3.91 8.02 1000 4.30 5.54 11.91 5.2 Impact of separation on number of CNTs in a bundle As the distance between neighboring shells in a bundle is increased the number of CNTs in it will decrease and it is shown in Fig.5.1. This in turn provides a rise in resistance and inductance because both of them are inversely proportional to the number of CNTs. On the other hand, there is a decrease in capacitance as it is directly proportional to the number of CNTs. Therefore number of CNTs in a bundle is an important factor in determining the delay and power dissipation of SWCNT bundle interconnect. Furthermore, when the technology is scaled down, there is a decrease in the number of CNTs in the bundle. This happens because as the technology node is reduced, width and height of the bundle are also reduced. Thus, the dimensions of the bundle are reduced so does the number of CNTs. 27 6000 5000 Number of CNT s 4000 3000 32 nm 2000 22 nm 1000 16 nm 0 1 nm 1.1 nm 1.2 nm 1.3 nm 1.4 nm Center to Center separation between adjacent tubes Fig.5.1. Variation in number of CNTs with respect to separation at 32, 22 and 16 nm technology nodes. 5.3 Performance analysis at 32 nm technology node The impedance parameters of SWCNT bundle interconnect are calculated in MATLAB by varying the separation between adjacent shells at different interconnect lengths. The following Figs are obtained after plotting the values against separation. On scrutinizing Figs.5.2,3 and 4, it is observed that the resistance as well as inductance increases with increase in separation whereas the opposite is true for capacitance. The cause for this variation lies in the fact that number of CNTS in a bundle reduces with increase in separation. Moreover, the number of CNTs are inversely proportional to the resistance and inductance while it is directly proportional to capacitance. 2700 1000 μm 2200 Resistance (Ohms) 800 μm 1700 600 μm 1200 400 μm 700 200 μm 200 1 nm 1.1 nm 1.2 nm 1. 3nm 1.4 nm Center to center distance between adjacent tubes Fig.5.2. Effect of increase in separation on resistance at various interconnect lengths at 32 nm technology node. 4.5 4 Capacitance(pF) 3 1000 μm 3.5 2.5 800 μm 2 600 μm 1.5 400μm 1 200 μm 0.5 1 nm Center to center distance between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.3. Effect of increase in separation on Capacitance at various interconnect lengths at 32 nm technology node. 350 300 1000 μm 250 800 μm Inductance(fH) 200 600 μm 150 400 μm 100 50 200 μm 0 1 nm Center to center distance between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.4 Effect of increase in separation on inductance at various interconnect lengths at 32 nm technology node. 5.3.1 Optimum driver size Now that the impedance parameters at 32 nm technology node have been obtained, the power and delay of SWCNT bundle interconnect are first calculated for lumped model of the interconnect at various W/L ratio of the CMOS driver. The ratio varies in terms of 10,20,30 till 70. At each point power and delay is calculated and also their product. The Fig 5.5 depicts that power delay product decreases with increase in W/L ratio of CMOS

driver. There is a point reached when the power delay product refuses to decrease further or there is a very small decrease. At that point we can say that an optimum value of W/L ratio is achieved. In this case the optimum value is achieved at ratio of 50. At this point the impedance of interconnect best matches with the impedance of CMOS driver. Consequently, this value will be used for further investigation on delay and power at 32 nm technology node while working on distributed model of SWCNT bundle interconnect which includes repeaters. 13 11 Power delay product(fWs) 9 7 5 3 32 nm 1 10 20 30 40 50 60 70 W/L ratio of driver Fig.5.5 Variation in power delay product with respect to increase in W/L ratio of driver.at 32 nm technology node 5.3.2 Repeater insertion Repeaters are actually the buffers or inverters (as shown in Fig. 4.2) used in order to reduce the propagation delay. The role of repeaters is to reduce the length of interconnect into 'N' segments, where N represent number of repeaters and it is known that propagation delay is dependent on length of interconnect and therefore insertion of repeaters results in reduction of propagation delay. The repeater insertion causes reduction in the distributed parameters of interconnects by the factor of N. When the repeaters are inserted the impedance parameters also reduce by a factor of N. Consequently, the delay is reduced but the power is enhanced. However the overall power delay product is reduced. In Fig .5. 6 it can be apprehend that the power delay product reduces rapidly as the number of repeaters are increased. After achieving a lowest value, the product becomes nearly constant or there is a little variation. The number at which this scenario happens is taken as number of repeaters to be taken in all other calculations for a particular technology node. At 32 nm technology node, the number of repeaters which 1.6 1.5 Power cdelay product(fWs) 1.4 1.3 1.2 1.1 1 0.9 0.8 0.7 32 nm 0.6 3 5 7 9 Number of repeaters 11 Fig.5.6 Power delay product vs. number of repeaters at 32 nm technology node. provides minimum power delay product is 7. The schematic of tanner tools for ESC distributed model of SWCNT bundle interconnect with 7 repeaters at 32 nm technology node is shown Fig5.7 Fig5.7. Schematic for ESC distributed model of SWCNT bundle interconnect with 7 repeaters at 32 nm technology node. 5.3.3 Effect of separation on propagation delay of SWCNT bundle 290 280 270 Delay(ps) 260 250 240 230 220 210 200 1 nm 1000 µm 800 µm 600 µm 400 µm 200 µm 1.1 nm 1.2 nm 1.3 nm 1.4 nm center to center separation between adjacent tubes Fig5.8 Increase in delay with respect to increase in separation between adjacent shells at 32 technology node. From Fig.5.8 it is vivid that the delay increases with the increase in separation between neighboring shells. As a matter a fact, it happens because increase in separation results in the rise of resistance and inductance. However, during this course of action the capacitance decreases. Now the delay mainly depends upon the resistance and capacitance and has negligible inductive effects. The increase in delay proves that increase in resistance is more pronounced over the decrease in capacitance. On further probing into the Fig.5.8, it is examined that there is high rise in delay at 1000 µm interconnect length as compared to 200 µm interconnect. Why it is so? The answer to this question is that resistance also increases with length. Therefore at higher lengths the increase in resistance due to length contributes to the existing increase with respect to separation. Thus the delay is further enhanced. 5.3.4 Effect of separation on normalized propagation delay Now that the delay of SWCNT bundle has been calculated, it can be compared with copper interconnect. The following Fig.5.9 has been obtained which represents the ratio of delay of SWCNT bundle interconnect and copper interconnect which is known as normalized delay. 0.55 0.53 Normalized delay 0.51 0.49 0.47 0.45 0.43 0.41 0.39 0.37 0.35 1 nm 1000 µm 800 µm 600 µm 400 µm 200 µm 1.1 nm 1.2 nm 1.3 nm 1.4 nm center to center separation between adjacent tubes Fig.5.9. Normalized delay vs. centre to centre distance between adjacent

tubes for different interconnect lengths at 32 nm technology node. For the ease of estimate, copper interconnect delay has been calculated at same input pulse,W/L ratio, number of repeaters i.e with '50' W/L ratio of CMOS driver and '7' number of repeaters. 90% delay has been withdrew from the results of both of the interconnects. It is manifest from Fig.5.9 that the normalized delay also increases with increase in center to center distance between adjacent tubes. It is quite obvious because the actual delay of SWCNT bundle rises as the separation increases. Furthermore, it is examined that normalized delay increases with decrease in interconnect length. The reason behind this is that, amelioration in performance of SWCNT bundle interconnect is better for longer interconnects. 5.3.5 Effect of separation on power dissipation of SWCNT bundle Fig.5.10. demonstrates the reduction in power dissipation with respect to increase in center to 5.95 5.85 Power dissipation(μw) 5.75 5.65 5.55 5.45 5.35 5.25 5.15 5.05 4.95 1 nm 1000 μm 800 μm 600 μm 400 μm 200 μm 1.1 nm 1.2 nm 1.3 nm 1.4 nm center to center separation between adjacent tubes Fig.5.10. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 32 nm technology node. center separation between adjacent tubes in a SWCNT bundle interconnect at different interconnect lengths. This reduction supports the dominance of reduction in capacitance over increase in resistance. Nevertheless, the capacitance increases with increase in length of the interconnect. 5.3.6 Effect of separation on normalized power dissipation The Fig.5.11. depicts the decrease of normalized power which is ratio of power of SWCNT bundle interconnect and copper interconnect. It can be clearly seen from the Fig that the ratio is more than 1, which means copper interconnect exhibits better performance than SWCNT in terms of power dissipation. Seemingly, the SWCNT bundle interconnect exhibits more power than its competitor. However, with the increase in center to center distance between adjacent tubes in a SWCNT bundle interconnect the normalize power decreases. This is due to the fact that actual power dissipation of SWCNT bundle decreases with the increase in separation and so does the normalized power. Likewise, actual power dissipation, the normalized power dissipation also increases with increases in interconnect length. 1.8 1.75 Normalized power 1.7 1000 μm 1.65 1.6 800 μm 600 μm 1.55 400 μm 1.5 200 μm 1 nm Center to center distance between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.11. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 32 nm technology node. 5.3.7 Effect of separation on power-delay product of SWCNT bundle The power delay product of SWCNT bundle interconnect mostly decreases with increase in separation between adjacent tubes. This indicates dominance of power dissipation over propagation delay. However, at some points the propagation delay dominates over the power dissipation. As a result, there is a trivial increase in power delay product. This happens because ultimately the propagation delay and power dissipation depends on the impedance parameters. In Fig.5.12 it is depicted that the power delay product increases with increase in interconnect length. As the propagation delay and power dissipation also increases with increase in length so does the power delay product. The propagation delay increases with separation because the resistance rises with increase in separation whereas the power. dissipation decreases with separation because the capacitance decreases with increase in separaion 0.75 Power delay product(fWs) 0.7 0.65 0.6 0.55 0.5 0.45 0.4 1 nm 1.1 nm 1.2 nm 1.3 nm 1.4 nm Center to center distance between adjacent tubes 1000 μm 800 μm 600 μm 400 μm 200 μm Fig.5.12. Power delay product vs. increase in separation between adjacent tubes for different interconnect lengths at 32 nm technology node. 5.4 Performance analysis at 22 nm technology node The performance analyses of SWCNT bundle interconnect versus copper interconnect and the effect of center to center distance between

adjacent tubes on propagation delay has been examined at 32 technology node. Now, we shall approach towards 22 technology node and observe what would happen if same kind of variations are applied to SWCNT bundle at this technology. In order to do this, first of all we need to calculate the impedance parameters of SWCNT bundle interconnect. These parameters have been calculated by performing coding of impedance equations in MATLAB. Structure parameters for interconnect at 22 nm technology node has been used for calculations. After calculating the impedance parameters with respect to increase in center to center distance between neighboring tubes in a SWCNT bundle. The values obtained are plotted versus separation. the following Figs.5.13,14 and 15 represents the effect of separation between center to center distance between adjoining tubes on impedance parameters. 6000 Resistance(Ohms) 4000 µm 800 5000 1000 3000 µm 600 2000 µm 400 1000 0 µm 200 µm 1 nm Center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.13. Resistance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node. 3.5 3 Capacitance(pF) 2.5 1000 µm 2 800 µm 1.5 600 µm 1 400 µm 0.5 0 200 µm 1 nm Center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.14. Capacitance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node. The trends which were observed for impedance parameters with respect to increase in center to center separation between adjoining tubes at 32 nm technology node are also observed at 22 technology node. But this time the value of resistance and inductance increased further. On the other hand, the value of capacitance decreased further. Now the question is why it is so? The answer is at 22 nm technology node, the width and height of interconnect reduces further in comparison with 32 nm technology node. Consequently, the number of CNTs inside a SWCNT bundle interconnect reduces. This in turn increases the resistance and inductance and decreases the capacitance further. Now that the, value of impedance parameters at 22 nm technology node are known. We shall repeat the whole procedure now for this technology. The delay and power dissipation are calculated for lumped model at 22 nm technology for 1000 µm long interconnect by varying the W/L ratio of CMOS driver from 10 to 70. The minimum power delay product is obtained at W/L ratio of 50 which is represented by Fig.5.16. One thing, which is worth noticing is that power delay product has increased as compared to 32 nm technology node 700 600 1000 µm Inductance(fH) 400 600 µm 500 800 µm 300 200 100 400 µm 200 µm 0 1 nm Center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.15. Inductance vs. center to center separation between adjacent tubes for various interconnect lengths at 22 nm technology node. 18 Power delay product(f-W-s) 16 14 12 10 8 6 4 22 nm 2 0 10 20 30 40 50 60 W/L ratio of driver 70 Fig.5.16. Variation in power delay product with respect to increase in W/L ratio of driver at 22 nm technology node. This increase indicates the supremacy of increase in delay over decrease in power dissipation. The next step is to work on distributed model and to insert repeaters until the minimum power delay product is attained. 2 Power delay product(fws) 1.8 1.6 1.4 1.2 0.8 22 nm 1 3 5 7 9 Number of repeaters 11 Fig.5.17. Power delay product vs. number of repeaters at 22 nm technology node At 22 technology node, the minimum product is attained with seven repeaters, which is depicted by Fig.5.17. The CMOS W/L ratio of 50 and 7 repeaters will be used for all the interconnect lengths at 22 nm technology node. There is decrease in power delay product because impedance parameters get divided by a factor of N and there is fall in propagation delay. The minimum power delay product obtained at this technology node is greater than what has been obtained for 32 nm technology. Again the increase in propagation delay, with respect to scaling of technology node dominates over decrease in power

dissipation 5.4.1 Effect of separation on propagation delay of SWCNT bundle 320 310 1000 µm 300 800 µm Delay(ps) 290 280 600 µm 270 400 µm 260 250 200 µm 240 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.18 Increase in delay with respect to increase in separation between adjacent shells at 22 nm technology node. On examining Fig.5.18 , it can be stated that the propagation delay increases with increase in center to center separation between adjoining tubes. This kind of trend has also been seen at 32nm technology node. However, at this time the propagation delay has been uplifted as compared to 32 nm node. What would be the reason for the increase in delay with decrease in technology node? The answer is, with the reduction in technology node, the width and height of the interconnect decreases. Therefore, the number of CNTs inside a bundle decreases. This in turn leads to an increase in resistance and so does the propagation delay. 5.4.2 Effect of separation on normalized propagation delay Like the actual propagation delay, the normalized propagation delay also increases with increase in center to center separation between adjoining tubes. The explanation of this increase is same as mentioned for 32 nm technology node. Although the Fig.5.19 looks very similar to the Fig.5.9 obtained in the case of 32 nm technology node. However, there is one thing to observe, the normalized delay at 22 nm technology node is smaller than the normalized delay at 32 nm technology node for all length of interconnects. 0.5 0.45 1000 µm Normalized delay 0.4 800 µm 0.35 600 µm 0.3 400 µm 0.25 0.2 200 µm 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.19. Normalized delay vs. centre to centre distance between adjacent tubes at different interconnect lengths at 22 nm technology node. The reason for this occurrence is, when the technology is scale down, the propagation delay of both SWCNT bundle and copper interconnect increases but the propagation delay of copper interconnect increases rapidly because the resistance of copper interconnect increases rapidly. 5.4.3.Effect of separation on power dissipation of SWCNT bundle The increase in center to center separation shows same kind of effect as seen at 32 nm technology node. However, this time there is a fall in power dissipation for each and every interconnect length as compared to 32 nm technology node. This fall in power dissipation(as shown in Fig.5.20) occurs due to scaling of technology node. Because of the scaling the number of CNTs in a SWCNT bundle reduces. As a result, the resulting capacitance decreases as capacitance is directly proportional to the number of CNTs. Apparently, the power dissipation increase with increase in length of interconnect because the impedance parameters increase with length. 3.2 3.1 Power dissipation(µw) 3 2.9 2.8 1000 µm 2.7 800 µm 2.6 600 µm 2.5 400 µm 2.4 200 µm 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.20. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 22 nm technology. 5.4.4 Effect of separation on normalized power dissipation 1.55 1.5 Normalized power 1.45 1.35 1000 µm 1.4 1.3 1.25 800 µm 600 µm 400 µm 1.2 200 µm 1.15 1 nm 1.1 nm 1.2 nm 1.3 nm Separation between adjacent tubes 1.4 nm Fig.5.21. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 22 nm technology. Like the actual power dissipation, the normalized power dissipation also decreases with increase in center to center separation between adjoining tubes. The explanation of this decrease is same as mentioned in the case of normalized power dissipation at 32 nm technology node. Although the Fig.5.21 looks very similar to the Fig.5.11 obtained in the case of 32 nm technology node. However, there is one thing to observe, the normalized power dissipation at 22 nm technology node is smaller than the normalized delay at 32 nm technology node for all length of interconnects. The reason for this occurrence is, when the technology is scaled down, actual power

dissipation decreases and the power dissipation of SWCNT bundle interconnect decreases more rapidly as compared to copper interconnect. 5.4.5 Effect of separation on power-delay product of SWCNT bundle The impact of separation on power delay product of SWCNT bundle is shown in Fig.5.22 at 22 nm technology node. It is similar as thatfor 32 nm technology node, expect for a change that the power delay product has increased for all the interconnect lengths with the scaling of technology. This means, it is the increase in propagation delay which dominates over the decrease in power dissipation with respect to scaling in technology node. 1 Power Delay product(fws) 0.9 0.85 1000 µm 0.95 0.75 800 µm 0.8 0.7 600 µm 0.65 0.6 400 µm 0.55 200µm 1 nm 1.1 nm 1.2 nm 1.3 nm Separation between adjacent shells 1.4 nm Fig.5.22. Power delay product vs. increase in separation between adjacent tubes for different interconnect lengths.at 22 nm technology node 5 .5 Performance analysis at 16 nm technology node Like the impact of center to center separation on propagation delay and power dissipation of SWCNT bundle interconnect and its performance with respect to copper interconnect has been observed at 32 and 22 nm technology node. Similarly, now the effect has to be seen at 16 nm technology node. For this purpose, first we need to evaluate the impedance parameters at this technology. These parameters are calculated in MATLAB for the center to center separation between adjoining tubes in a bundle varying from 1nm to 1.1 nm. The outcomes for the resistance, capacitance and inductance are shown in Figs.5.23,24 and 25 rescpectively. 16000 14000 1000 µm Resistance (Ohms) 10000 800 µm 12000 8000 600 µm 6000 4000 400 µm 2000 200 µm 0 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.23 Effect of increase in separation on resistance at various interconnect lengths at 16 nm technology node. Similar type of trends which were observed for 32 and 22 nm technology nodes has been observed for impedance parameters when plotted against center to center separation between nearby tubes at 16 nm technology node. The reason for these trends is the same as explained for other two technologies. However, the resistance and inductance obtained for this technology are highest amongst the all three technologies. On the contrary, the capacitance obtained is the lowest amongst the all three technologies. The reason for this, 16 nm technology node has the lowest width and height of the interconnect as compared to the 32 and 22 nm technology nodes. So, it is obvious for the SWCNT bundle to hold the lowest number of CNTs as compared with other two technologies. Therefore, the resistance and inductance is the highest amongst all the three technology nodes whereas the opposite is true for capacitance. 2.5 2 Capacitance(pF) 1.5 1000 µm 0.5 600 µm 400 µm 1 800 µm 0 200 µm 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.24 Effect of increase in separation on capacitance at various interconnect lengths at 16 nm technology node. 2000 1800 1000 µm 1600 Inductance(fH) 1400 800 µm 1200 1000 600 µm 800 600 400 µm 400 200 200 µm 0 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.25 Effect of increase in separation on inductance at various interconnect lengths at 16 nm technology node. Now using these values, the whole procedure is again repeated for 16 nm technology. The power delay product is calculated by varying the W/L ratio from 10 to 70 for lumped model of SWCNT bundle 1000 µm long interconnect. The minimum power delay product is obtained at CMOS W/L ratio of 40 as shown in Fig.5.26. Now this W/L ratio will be used for propagation delay and power dissipation calculations for distributed model of SWCNT bundle interconnect at 16 nm technology node. 19 Power delay product(fws) 15 17 13 11 9 7 5 16 nm 10 20 30 40 50 60 70 W/L ratio of driver Fig.5.26. Variation in power delay product with respect to increase in W/L ratio of driver.at 16 nm technology node. The Fig.5.26 is showing the same trend as followed by

32 and 22 nm technology nodes. However, the power delay product is increased, if it is compared with both 32 and 22 nm technology nodes. This increase indicates the supremacy of increase in delay over decrease in power dissipation. Due to the insertion of repeaters, there is a fall in power delay product which is shown in Fig. 5.26 The next step is to work on distributed model and to insert repeaters until the minimum power delay product is attained. At 16 nm technology node, the minimum product is attained with nine repeaters, which is depicted by Fig.5.27 3.8 Power delay product(fws) 3.3 2.8 2.3 1.8 1.3 0.8 16 nm 3 5 7 9 Number of repeaters 11 Fig.5.27. Power delay product vs. number of repeaters at 16 nm technology node. The CMOS W/L ratio of 40 and 9 repeaters is used for all the interconnect lengths at 16 nm technology node. 5.5.1 Effect of separation on propagation delay of SWCNT bundle With the increase in center to center separation between adjoining tubes, propagation delay increases. It is a similar observation which was observed at 32 and 22 nm technology nodes. The reason for this increase in propagation delay is same as that explained for the increase at 32 and 22 nm nodes. Evidently, the propagation delay at this node is highest among the all three technologies. This is due to the fact that, width and height of interconnect at 16 nm technology is the smallest as compared to other two technologies. One interesting thing to note in Fig.5.28 is that at 1000 µm interconnect length the propagation delay increases rapidly. This happens because of two reasons, first is the resistance is very high at long length and due to reduction in technology it adds to the propagation delay. 390 380 370 1000 µm 360 Delay(ps) 350 800 µm 340 600 µm 330 320 400 µm 310 200 µm 300 290 1 nm 1.1 nm 1.2 nm 1.3 nm center to center separation between adjacent tubes 1.4 nm Fig.5.28 Increase in delay with respect to increase in separation between adjacent tubes at 16 nm technology node. 5.5.2 Effect of separation on normalized propagation delay 0.35 0.3 Normalized delay 0.25 0.2 0.15 1000 µm 800 µm 600 µm 400 µm 200 µm 0. 1 1 nm 1.1 nm 1.2 nm 1.3 nm 1.4 nm center to center separation between adjacent tubes Fig.5.29. Normalized delay vs. centre to centre distance between adjacent tubes at different interconnect lengths at 16 nm technology node. 50 The normalized delay like the propagation delay increases with separation. Fig.5.29. elucidates this scenario and it is vivid from the Fig that normalized delay increases with increase in interconnect length. The explanations to these occurrences are same as the explanations of 32 and 22 nm technology nodes. Here at 16 nm node, the normalized delay is further reduced as compared to other two technology nodes. Again the reason is same as explained in case of normalized delay at 22 nm technology node. 5.5.3 Effect of separation on power dissipation of SWCNT bundle 2.7 Power dissipation(µw) 2.4 1000 µm 2.6 2.5 2.3 800 µm 2.2 600 µm 2.1 400 µm 1.9 200 µm 2 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.30. Power dissipation vs. center to center distance between adjacent tubes for different interconnect lengths at 16 nm technology node. The increase in center to center separation in Fig.5.30 shows same kind of effect as seen at 32 and 22nm technology node. However, this time the power dissipation is lowest amongst all the three technology nodes and this is true for each and every interconnect length 5.5.4 Effect of separation on normalized power dissipation 1.3 1.28 1.26 1000 µm Normalized power 1.24 1.22 800 µm 1.2 1.18 600 µm 1.16 1.14 400 µm 1.12 1.1 200 µm 1 nm 1.1 nm 1.2 nm 1.3 nm 1.4 nm center to center separation between adjacent tubes Fig.5.31. Normalized power dissipation vs. separation between adjacent tubes for different interconnect lengths at 16 nm technology node. The normalized delay is plotted against increase in separation between adjacent tubes at 16 nm technology node in Fig.5.31. Just like the actual power dissipation, the normalized power dissipation also does decrease. The normalized power obtained for every interconnect length is minimal in contrast to other

two technologies. This clarifies that the performance of SWCNT bundle at 16 nm technology node in terms of power dissipation is better as compared to other two nodes. 5.5.5.Effect of separation on power-delay product of SWCNT bundle The power delay product of SWCNT bundle interconnect mostly decreases with increase in separation between adjacent tubes as shown in Fig.5.32 .This indicates dominance of power dissipation over propagation.delay. 1 0.95 Power delay product(fws) 0.9 1000 µm 0.85 0.8 0.75 800 µm 0.7 0.65 600 µm 0.6 400 µm 0.55 200 µm 1 nm center to center separation between adjacent tubes 1.1 nm 1.2 nm 1.3 nm 1.4 nm Fig.5.32. Power delay product vs. increase in separation between adjacent tubes at different interconnect lengths at 16 nm technology node. However, at some points the propagation delay dominates over the power dissipation. As a result, there is a trivial increase in power delay product with respect to increase in separation. The power delay product increases further as the technology is scaled down from 22 nm to 16 nm. It happens because with scaling, the propagation delay increases whereas the power dissipation decreases and it is the increase in delay which overshadows the decrease in power dissipation. CHAPTER 6 Conclusion and Future scope CNTs are the promising candidates of future VLSI interconnect. They are mechanically and thermally stable and are prone to electro migration. The resistance of CNT is much lower than copper while the capacitance is larger but the propagation delay of CNT is lower than copper making it suitable for interconnect application and better than copper. The SWCNT bundle is most desirable form of CNT based interconnect provided all constituent CNTs of the bundle are metallic. In SWCNT bundle interconnects, it is found that isolated tube diameter and separation play an important role in determining delay and power dissipation. Another parameter of importance is the interconnect length. When the interconnect length increases all the impedance parameters increases. This is true for all technologies. It is felt that both SWCNT and MWCNT perform better than copper in the semi-global and global levels of interconnect length. The center to center distance between adjacent shells is equal to the distance from the center of one CNT to the center of other CNT. In this case, the CNTs are densely packed and separation is equal to the diameter of single CNT. By varying this separation interconnect delay and power dissipation can be altered. It is also seen that the delay decreases by increasing the aspect ratio of repeaters of SWCNT bundle interconnect. This is true for both lumped and distributed model. The delay further decreases when the number of repeaters in a SWCNT bundle interconnect increases. At all technologies, with the increase in separation, the propagation delay increases whereas the power dissipation decreases and the same effect comes into action when the technology is scaled down. To achieve better performance, it is required that the SWCNT bundle should be densely packed, and the separation should be restricted around 1 nm. The work in this report does not include the effect of temperature change on carbon nanotubes and is needed to be studied. Most of the research is concentrated on the analysis of CNT, however a very little work has been done in the field of fabrication of CNTs and is needed to be studied. The imperfect contact resistance arises due to lack of proper growth techniques of CNTs and therefore study can be done in order to find effective growth which can reduce contact resistance 1 2 3 4 6 7 8 10 11 12 13 14 15 16 18 19 20 21 22 24 25 26 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 51 52 53 54