A NOVEL ARCHITECTURE FOR SAMPLE RATE CONVERTER USING FIR FILTER

A Dissertation Submitted in partial fulfilment of the requirement for the award of the degree of

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In

Electronics and Communication Engineering

Submitted by

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DECLARATION & CERTIFICATE

I hereby declare that the work which is being presented in the dissertation, entitled, **"A Novel Architecture for Sample Rate Converter using FIR filter"** in partial fulfillment of the requirement for the award of degree of Master of Engineering in Electronics and Communication Engineering, submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Dr. Sanjay Sharma(Professor and Head),** Electronics and Communication Engineering Department and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by student is correct to the best of my knowledge and belief.

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ABSTRACT

In digital signal processing, the use of different sampling rates within a system becomes an important topic. Different sampling rates are used for different systems. Sampling rate Conversion has many applications in communication and signal processing, where two systems with different sampling rates need to be interconnected. The aim of digital sampling rate converter is to generate a discrete time signal from one sample rate to another. When sampling of signal is done, some information is lost and in the process of re-sampling of signal, some sort of distortion is introduced. The generation of output samples from input samples may be performed by the applications of various techniques. There are two basic methods to convert the sampling rate. In the first method the signal is re-sampled after converting it in analog domain. In the second method digital signal processing techniques are applied to get the new samples from the existing samples. The second technique introduces low distortion and noise.

When sampling rate of a discrete time signal is to be increased, it is passed through interpolator followed by anti imaging filter. When sampling rate is to be decreased, the anti aliasing filter is used prior to decimator. In rational sample rate converter common filter, which works as anti imaging as well as anti aliasing filter is used between interpolator and decimator. In most of the cases of sample rate conversion, FIR filters are preferred over IIR filters because they do not possess feedback loops and are easier to implement than IIR filters. Moreover the phase response of FIR filter is linear, so the phase distortion of output signal is minimized.

In this thesis, various techniques of FIR filter implementations for rational sampling rate conversion are discussed keeping in mind that during filter operation after interpolation some of the samples are zero and in the process of decimation some of the signal values are to be discarded. Efficient implementation of Lth band filter using coefficient symmetry is proposed for which implementation complexity is lower than other implementations. Also for the larger values of Interpolation and decimation, multistage implementation is proposed which reduces the filter order requirement and computational complexity.

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LIST OF ACRONYMS

BPF	Band Pass Filter
CD	Compact Disk
CIC	Cascade Integrator Comb
CT	Contineous Time
DCT	Discrete Cosine Transformation
DT	Discrete Time
DVD	Digital Video/Versatile Disk
ECT	Electronic Current Transformer
FFT	Fast Fourier Transformation
FIR	Finite Impulse Response
FRFT	Fraction Rate Fourier Transform
IF	Intermediate Frequency
HPF	High Pass Filter
IIR	Infinite Impulse Response
LPF	Low Pass Filter
LTI	Linear Time Invariant
MATLAB	Matrix Laboratory
MFB	Multi-rate filter bank
RSRC	Rational Sample Rate Converter
SDR	Software Defined Radio
SRC	Sampling Rate Conversion/Converter

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CHAPTER 1

INTRODUCTION

1.1 Discrete Time Sequence

In digital signal processing, we describe signals as sequences of numbers called samples. A sample value of a characteristic discrete-time signal is denoted as *x(n)* with argument '*n*' being an integer between -∞ and+∞. It is clear that '*n*' is only for integer and not for the non-integer. The method to get discrete time sequence is to sample the continuous signal. That means taking a value of the continuous signal every T seconds. This T can be any number greater than zero. The sampling frequency $F_s=1/T$ [1]. This is illustrated in fig. 1.1.

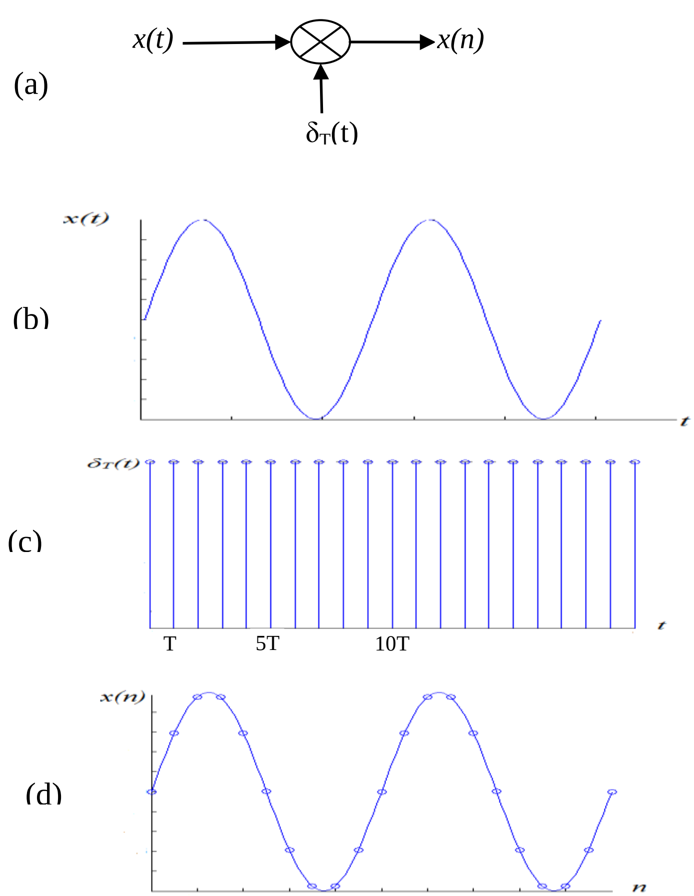


Figure 1.1 Sampling of Continuous time signal (a) Sampling block diagram (b) Continuous time sequence (c) Impulse train (d) Discrete time sequence [1].

1.2 Multirate Digital Signal Processing

Theoretically, the very basic and simple idea of altering the sampling frequency of the signal is to convert the sampled sequence in analog domain and resample this continuous time sequence at the new required sampling rate by assuming that there is no need of additional anti-imaging or anti-aliasing filter. This approach of sample rate alteration has some related harms in practice. A main realistic problem of this approach is that the perfect operations necessary to recreate the continuous-time signal from the unique samples of discrete sequence and to resample this signal at the new sampling rate cannot be implemented accurately. By a careful designing of the individual components, these realistic distortions can be minimized up-to some extent but cannot be eliminated entirely [2].

A multi-rate filter can be defined as a digital filter for which the sampling frequency of the input signal is altered at one or more transitional points. Multi-rate techniques can be used in filters for sampling rate conversion where the input and output rates are different, and also in designing the filters with identical input and output sampling rates. Different digital systems, used for engineering applications works at different sampling rates so, sampling rate converter is required for the efficient operation of these systems. The nyquist theory of sampling simply sets a limitation on least sampling rate of signal (an analog signal is to be sampled at rate which is twice or above the maximum frequency contained in the signal, and some additional factors determines the actual sampling rates to be used. Example of multi-rate signal processing is different audio systems which use different sampling rates e.g. 44.1, 48, and 96 kHz. Another example is, American television, European television, and movies all use diverse numbers of frames/samples per second. Users would akin to transport source digital data among these systems. Merely replaying the given data at the new sampling rate will not generally work. It will introduce large changes in terms of pitch for audio signal and progress as well for video signal. Thus sample rate conversion is essential in practice [3].

In Sampling Rate Conversion process we are digitally altering the sampling frequency of a digital signal from a given sampling frequency $F_s = 1/T_s$ to a new required sampling frequency $F'_s = 1/ T'_s$ [2]. New sampling rate can be higher or may be lower than the original sampling rate of sequence. When the new sampling frequency F'_s is higher than the original sampling frequency F_s then new sampling time T'_s is lower than original sampling time T_s defined by (1.1) and (1.2) respectively.

$$F_s < F'_s \tag{1.1}$$

$$T_s > T'_s \tag{1.2}$$

The process of increasing sampling rate is usually called interpolation as new samples are being generated from its existing set of discrete samples. The mathematical procedure of interpolation, or creating the new set of samples received widespread attention from mathematicians and researchers, who were concerned in the problem of tabulating helpful mathematical functions. The main problem was to know how often a given signal had to be sampled so that one could make use of some simple interpolation law to obtain precise values of the signal at the higher sampling rate. This work did not only lead to an early admiration of the sampling process, but it also lead to some attractive lessons of interpolation functions, which could offer almost arbitrarily high precision in the interpolated signal values, given that adequate tabulated values of the signal were obtainable [3]. The procedure of digitally altering the sampling rate of a digital signal from the given rate F_s to a lower rate F'_s, represented by (1.3) and (1.4).

$$F_s > F'_s \tag{1.3}$$

$$T_s < T'_s \tag{1.4}$$

This process of reducing sampling rate is called decimation. Decimation and Interpolation of digital signal can be described as a twofold process i.e. a digital signal that applies to a decimator can be transformed into its dual digital signal that implements an interpolator using simple alteration techniques.

1.2.1 Interpolation

It is increasing the sampling rate and signal reconstruction by interpolating additional samples. Structure of interpolator is given in fig. 1.2 and time domain sequence of input and interpolated signal (L=2) is shown in fig 1.3. The interpolation process consists of following steps [4].

- The signal sample rate F_s is increased by L by adding L-1 zeros in between each two original samples. The original samples and their timings do not change
- The new sample rate is LF_s.
- The resulting signal is low pass filtered to eliminate imaging components.
- The original interesting band $F_s/2$ is still the same.
- The cut off frequency of filter used is π/L.

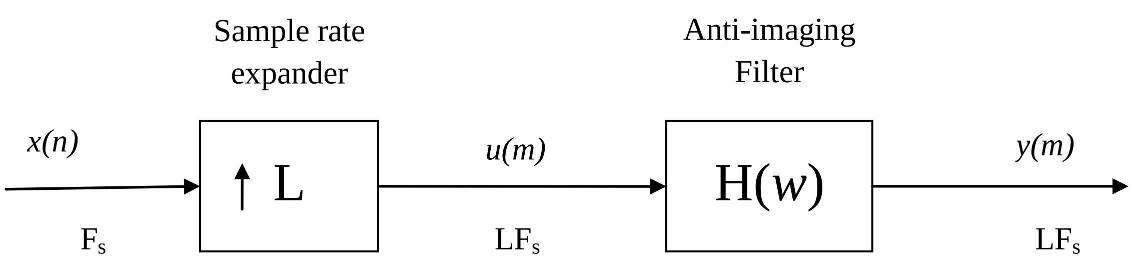


Figure 1.2 Stages of Interpolation [4].

$$u(m) = \begin{cases} x\left[\frac{m}{L}\right], & for \ \mathrm{m} = 0, L, 2L\ldots\ldots \\ 0, & otherwise \end{cases} \tag{1.5}$$

$$y(m) = \sum_{k=0}^{N} h_k u(m-k) \tag{1.6}$$

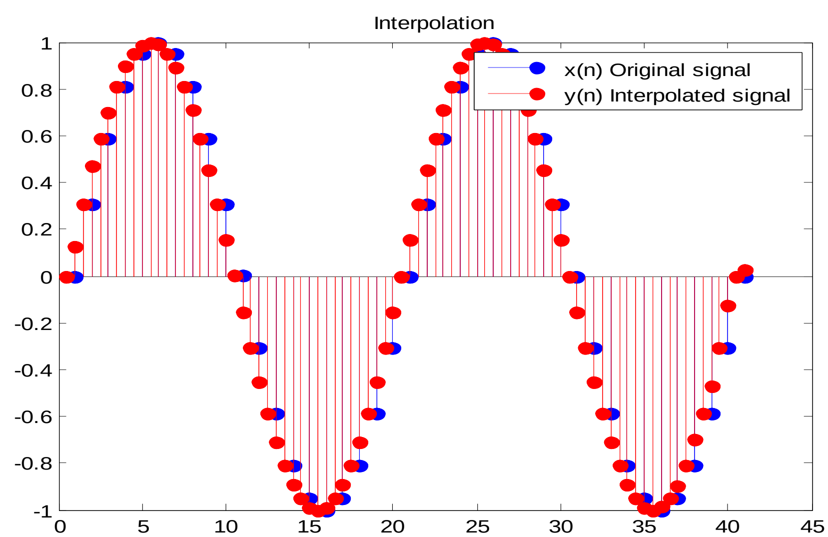


Figure 1.3 Original and Interpolated signal (L=2)

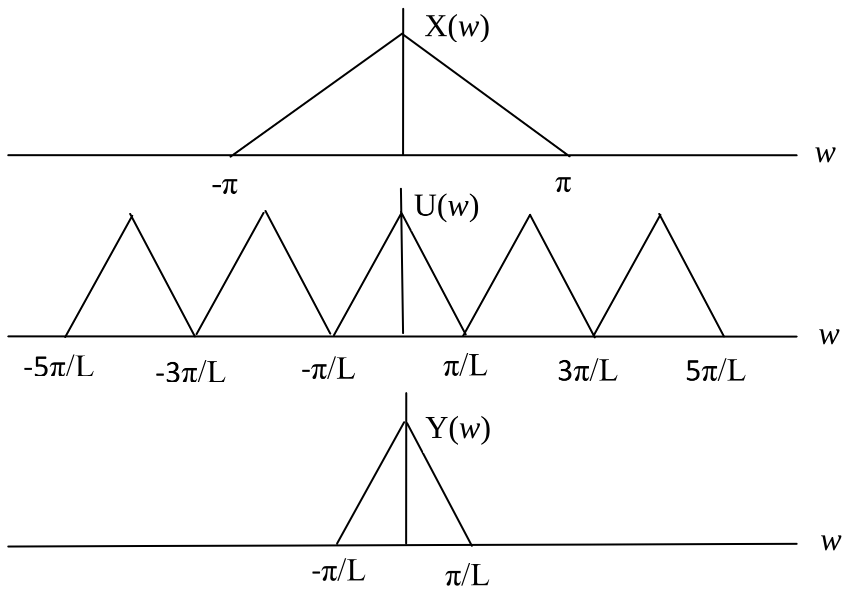


Figure 1.4 Spectrum of original and interpolated signal

1.2.2 Decimation

It is reduction of sampling frequency. It is process of decimation by factor M, omitting M-1 samples between the original samples. Decimation process block diagram is shown in fig. 1.5 and time domain representation of decimation (M=2) is given in fig. 1.6. Decimation process includes the following steps,

- The signal with sampling rate F_s is firstly filtered by low pass anti aliasing digital filter.
- After the filtering the sampling rate is still F_s.
- Then it is decimation by M i.e. every Mth sample is selected from the signal.
- The final sampling rate is F_s/M.
- The original interesting band was $F_s/(2M)$.
- The cut off freq used is π/M.

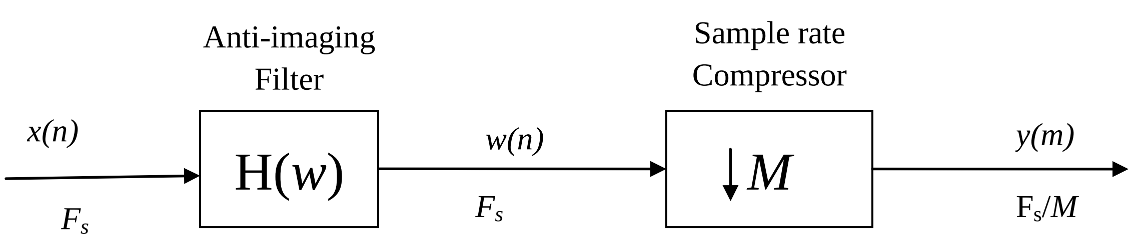


Figure 1.5 Stages of Decimation [4].

$$y(m) = w(Mm) = \sum_{k=0}^{N} h_k x(mM - k) \qquad (1.7)$$

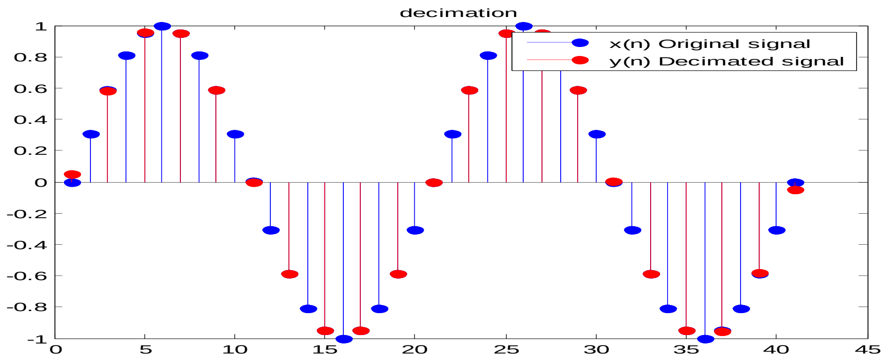


Figure 1.6 Original and Decimated signal.

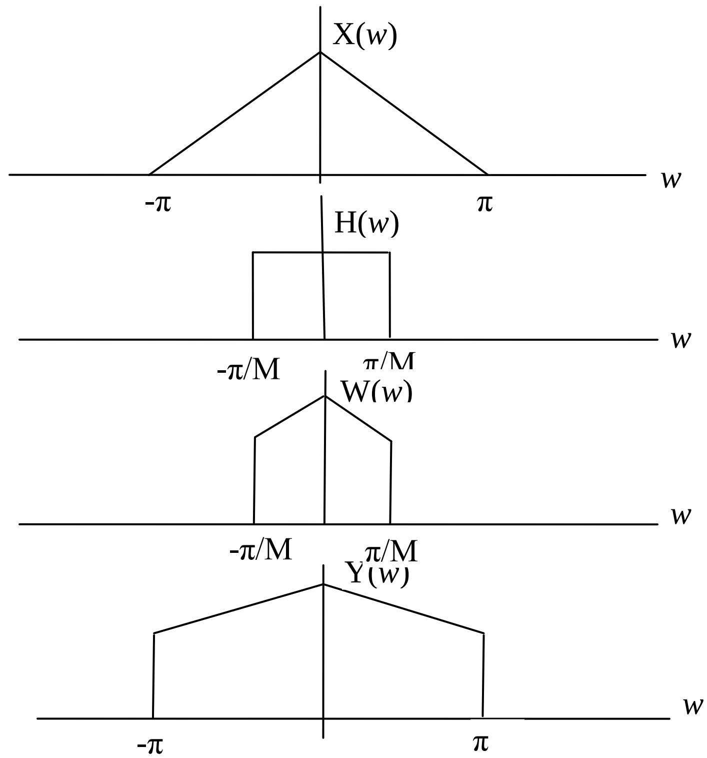


Figure 1.7 Spectrum of input and decimated signal

1.2.3 Conversion by Rational factor (*L/M*)

In many cases sampling rate alteration by a factor which is non-integer is needed. In practice, the conversion by factor *L/M* between audio formats is done by

1. Interpolation of the input signal by *L* followed by anti-imaging filtering by $h_1(z)$.
2. Decimation by factor *M* preceded by anti-aliasing-filtering by $h_2(z)$.

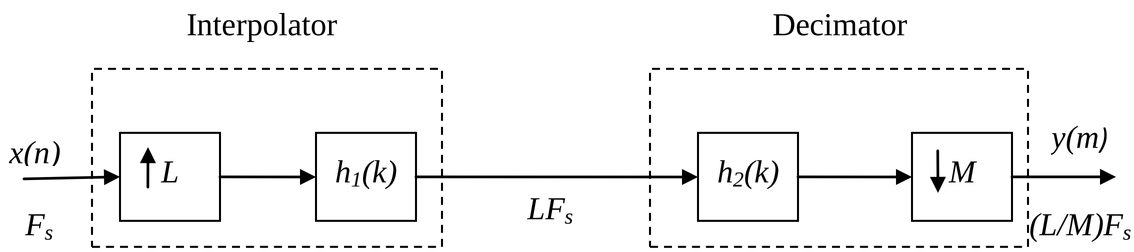


Figure 1.8 Cascade structure of Interpolator and Decimator [5].

The cascaded low pass filters $h_1(k)$ and $h_2(k)$ have the same sample rate, and can be combined as shown in fig. 1.9.

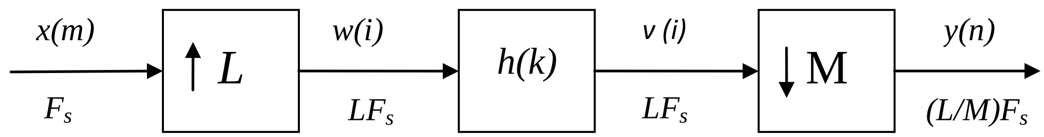


Figure 1.9 Stages of rational sampling rate conversion [5].

$$y(m) = \sum_{k=0}^{N} h_k x\left[\frac{Mm - k}{L}\right] \tag{1.8}$$

- Input discrete sequence is up-sampled by factor L.
- Up-sampled sequence is passed through filter $h(z)$ which works as equally anti-imaging and anti-aliasing filter.
- Cut off frequency of filter $h(z)$ is min(π/L, π/M).
- Resulted signal from filter is decimated by factor M.

1.3 Filters used in Sampling Rate Conversion

For sample rate conversion system both types of filters(FIR and IIR) can be used. In most applications of sampling rate conversion FIR filters are preferred over IIR filters due to the reasons listed ahead;

- The phase response of FIR filter is firmly linear, while in case of IIR filter it is not. The nonlinearity of IIR filter is inversely proportional to its selectivity.
- In case of FIR filter, fast fourier transform can be used but in case IIR filter we cannot use the FFT.
- The structure of FIR filter is non recursive, so the finite precision arithmetic errors in

this filter are small. In case of IIR filter, due to its recursive structure, and parasitic oscillation may occur.

The design steps of FIR filter for sample rate converter are;

- The specification of filter requirement and calculation of the filter coefficients.
- Representation of digital filter by its suitable structure.
- Analysis of filter performance alteration by the effect of finite word length.
- Implementation of digital filter on hardware and/or software.

The steps given are not necessarily independent nor are they always performed in same order. Advance techniques can combine second and aspects of third and fourth step. Sometimes it is necessary to iterate few times between the steps to design an efficient filter.

1.4 Motivation of the Thesis

In modern digital signal processing systems, it is required to work on the different sampling rate for efficiency improvement of overall digital system. The motivation for concentrating on sample rate conversion lies in the fact that it has several applications in communications, digital image processing, digital audio system and multimedia. The main benefit of a multi-rate system is the significant reduction of computational complexity and consequently reduces the cost. The computational effectiveness of multirate algorithm is dependent its capability to use unlike sampling rates in simultaneously the different part of the digital system. The sampling rate alterations generate the unwanted effects through the system i.e. spectral aliasing in the sampling rate decrease and spectral images in the sampling rate increase.

The multi-rate filtering makes the universal concept of multi-rate signal processing relevant in practice. The basic multi-rate signal processing building blocks is key to many applications of signal compression and communication [6]. Another application of multi-rate signal processing includes,

- Conversion of variable rate to fixed rate output data in a modulator and inverse task in demodulator.
- Sample rate conversion is used before converting data from digital to analog domain.

- Multi-rate systems are used in CD players when music signal is converted from Digital to Analog.
- Communication system.
- Speech and audio processing system.
- Antenna systems
- Radar systems.

1.5 Problem Formulation

In multi rate signal processing different sampling rates are used at different stages of digital system. The basic approach of converting sequence in analog domain and re sampling creates distortion problem. In digital domain the phase distortion can be overcome by use of FIR filters over IIR filter. The poly phase implementation of FIR filter takes the advantage of moving the filter operations at the lower sampling frequency. When poly-phase implementation is combined with coefficient symmetry implementation [46], the implementation complexity reduces nearly half but not exactly half. Efficient filter structure is required which reduces the filter computational complexities compared to the one described in [46]. Also for the high values of interpolation and decimation, a very high order filter is required. So, a novel algorithm is required to design a sample rate converter to save the memory requirement and reduce the computational complexity.

1.6 Objectives

The objective of this thesis is to get a deeper understanding of sample rate conversion, the theoretical background and their implementation in digital signal processing. The other objective of the work is

- To reduce the computational time of Fractional sample rate convertor by efficiently design of low pass FIR filter between up-sampler and down-sampler considering the facts that some of signal values are zero after interpolation and some values are discarded at the output.
- To reduce the number of computations by utilizing the coefficient symmetry and Lth band filter property.
- To reduce the storage for filter coefficients by multistage implementation.

1.7 Organization of Thesis

This Thesis is divided into six chapters and organized as follows

Chapter-1 Describes the theory and development and utility of discrete time system and multi rate signal processing. It defines the basic building blocks of sample rate converter i.e. interpolator, decimator and rational sample rate converter.

Chapter-2 Contains the literature review of research papers related to the dissertation work. It contains literature review of different design implementations of sampling rate converter and their implementation complexities.

Chapter-3 In this chapter the various implementation of FIR filters in sampling rate converter i.e. direct form implementation, poly-phase implementation, implementation using coefficient symmetry and their multiplication and addition complexities are discussed.

Chapter-4 Defines Proposed structure for sample rate conversion using Lth band filter implementation and a multistage implementation is proposed for the large values of interpolation and decimation factor..

Chapter-5 In this chapter work done in dissertation to design the computational and memory efficient structure for sampling rate converter is compared with different implementation structures. Also example of proposed multistage structure is discussed by obtaining an optimum structure for DVD to CD sample rate conversion

Chapter-6 It concludes the research work done in this thesis and future scope of work is discussed.

CHAPTER 2

LITERATURE REVIEW

2.1 Research Papers Literature Review

In-order to start the thesis, the initial step is to study and analyze the research papers that have been performed previously by other researchers. Research papers associated to this work are selected and studied. Researched papers are described below:

R.E. Chrochiere et al. [9] gave general idea of multi-rate signal processing applied in interpolation and decimation. Basic concepts of sampling rate conversion were discussed. Comparison of direct form and poly-phase structure of FIR filter was done. Equivalent multiband filter of low pass filter was designed and calculation of minimum mean squared error was done. It was observed that cascade structure of decimator and interpolator results in an well-organized approach to the realization of narrow-band low pass filter.

C. C. Hsiao [12] proposed the use of poly-phase filter array for efficient realization of sampling rate by non integer factor. The filter in the high sampling rate side can be decomposed in poly-phase filter structures which can be stimulated to lower sampling rate side without altering the filter functions. The structure of poly-phase filter has been extended from integer to rational (L/M) sampling rate conversion system, by maintaining the input-output relation of the system. For FIR filter there is a reduction in computational complexity by L or M and poly-phase filter coefficients are calculated in symmetric way from the integral filter.

B. Guoan [14] proposed that during sample rate conversion by factor (L/M), delay necessities linked with each sub-filter path in such a arrangement have not been adequately considered. It was proposed that a reduction on the number of information data stores by a factor of L(interpolation factor) can be achieved. Parameter formalized three dimensional structure with minimum delay requirement was achieved using transformation rules. The proposed structure is suited for a time-multiplexed implementation which allows fewer arithmetic operators and data stores to be built in hardware as compared with direct implementation of poly-phase structure.

J. kovacevic et al. [15] presented a universal, direct designing method of the perfect reconstruction of the filter banks with rational sampling rate conversion. These filter banks containing N number of branches and each of its branches has a different sampling factor of p_i/q_i and sum of all branches is equals to one. Advantage of this proposed method with comparison to direct implementation of sample rate conversion was given by giving a design example.

G. Bi et al. [16] presented delay requirement analysis in detail and show that the re-sampling by factor L(Interpolation factor) for sample rate conversion on the data stores can be achieved. Efficient structure was proposed based on the minimization of the delay units. The paper also presented the hardware implementation which demonstrated the usefulness of the proposed approach. Using the multiplexing technique, a hardware efficient implementation can be achieved, which can provide a significant chip area reduction as compared with a direct implementation of poly-phase structure.

B. Levitan et al. [17] derived a general conversion between equivalent parallel and hierarchic analysis multi-rate filter banks(MFBs). Multi-rate filter banks are used for rational number change in sampling rate between successive outputs and arbitrary LTI filtering for each output. MRB conversion allows taking advantage of the property tradeoffs between hierarchic and parallel MRB architectures. If the speed is primary consideration, a hardwired parallel architecture can be used. MRBs with low-pass filter satisfy the stability condition, since the filter cutoffs typically decrease with decreasing sampling rate.

W. H. Yim [18] proposed a method for sampling rate conversion in linear multi-rate digital signal processing system by efficiently realization by a matrix of poly-phase filter. The method represents a new analytical approach that simplifies the design of poly-phase matrix and associated structures. The proposed approach makes it simple to derive Z-transform of sub filters and to minimize delay elements. The new approach results in single decomposition formula which is simpler than previous graphical design procedures.

F. Ling [19] discussed the relevance of digital rate alteration in echo cancellation modems.

Because of the nature of the appliance, the alteration percentage is not a predestined or set rational value. In this concept the alteration of sample rate alteration was done by a ratio which is non-rational and estimated implementations of such a rate converter were considered [19].

H. Murakami [20] proposed that when length of filter is highly composite a new recursive polynomial factorization can be done. This recursive factorization of filter can be used to describe a comprehensive form of the discrete fourier transform(DFT) and to obtain an algorithm which is efficient in terms of computations. It was shown that the comprehensive form of the DFT closely linked to the poly-phase implementation, and can be functional for the design of sampling rate alteration systems. It is also proposed that for the larger filter lengths cyclic sampling rate alteration system by a rational factor which is more efficient than rational poly-phase implementation can be applied.

Z. Jian [21] extended the symmetric FIR filter algorithm**.** By exploiting the symmetric relationship in coefficients of poly-phase sub filters, reduction in the number of multiplications by half compared with the direct computation was achieved. Paper shows that the number of adders could also be reduced asymptotically by 50%.The reduction of arithmetic operations have been made on the very basic structure of symmetric FIR interpolators and decimators, sot these algorithms will be interesting for many implementations, particularly in VLSI and on microprocessors.

H. murakami [22] related the real valued change to poly phase implementation of sequence and applied this inspection to sampling rate alteration system that are implemented by the real valued fast cyclic convolution algorithm. It was given that the proposed algorithms are useful when signal and digital filter's impulse response is restricted to be real in nature.

S. Emami [23] presented new methods for performing decimation and interpolation which are easy to compute and can be realized in Digital Signal Processing. Three stages proposed for efficient sampling rate alteration by factor L/M are;

- Forming the streams: In decimation both input sequence and impulse response of the filter are segmented to M streams. In the process of interpolation only the impulse response is segmented into streams

- Convolutions: A total of L (or M) convolution operations are performed for interpolation (or decimation).
- Combining intermediate results: The intermediate results are added up column by column in decimation, whereas in interpolation the intermediate results are multiplexed. A comparison between the number of operations (multiplications and additions) required by given method.

A. I. Russell [24] Show that in Rational Sampling Rate Conversion by factor L/M, poly phase decomposition can be used for efficient implementation of infinite impulse response (IIR) filters. The computational complexity of the recursive and non-recursive parts of the filter are considered in independently, and the gain in efficiency of a factor of LM/(L + M -1) is obtained for the recursive part. The value of gain is applicable only when value of interpolation factor(L) and decimation factor(M) is greater than one.

K. Rajamani et al. [25] proposed a technique for sampling rate alteration to alter44.1 kHz compact disc (CD) to 48 kHz digital audio tape (DAT) in efficient manner. In this methodology input signal is up sampled by two, and then this interpolated signal is passed through the fractional delay filter that performs a simple decimation. This proposed method can also be applied for sample rate conversion from DAT to CD without varying the filter coefficients. The algorithm is simulated in MATLAB and can be applied to the real time digital signal processors (DSP).

W. H. Yim [26] analyzed the distortion for multiplier less sampling rate alteration using linear transfer function. The proposed approach show that any approximate conversion is equivalent to the use of multi rate finite impulse response (FIR) filter, where all non zero coefficients are identical and leads to simplified analysis in terms of the transfer function of the digital filter.

A. I. Russel et al. [28] presented a new algorithm for sample rate conversion by rational factor. It was proposed that if the transfer function of selected continuous time(CT) filter is rational, then this system can be simulated using a discrete time(DT) algorithm for which there is low requirements of memory and computations. The discrete time(DT) implementation is composed of a parallel architecture, where each branch of filter consists of a time-varying filter with one or two taps, followed by a permanent recursive filter operating at the output sampling rate. The calculation of coefficients of these type of time varying filters can be done in recursive manner. So, the need to store large number of filter coefficients is completely eliminated.

N. Aikawa et al. [30] presented a structure for rational sampling rate conversion, which is based on a kernel based block filter. The impulse response of the proposed filter can be approximated by polynomials so there is no need to redesign a filter when sampling rate is changed. The proposed kernel based block filter in this paper has the block structure that the impulse response of sampling section since the third is represented by the polynomial used for the second sampling section. The memory requirements of filter proposed in this proposed implementation is low. Moreover, the proposed filter has the other advantage that it can handle arbitrary fractional sampling rate conversion.

D. Babic et al. [31] proposed the use of polynomial based interpolation filters to reduce the implementation complexity when sample rate conversion factor is fraction of two very large integer values or an irrational numbers. This idea is extended to uninformed polynomial-based interpolation and the relation between various polynomial-based interpolation filters (Farrow filter structures and its modifications) and poly-phase finite impulse response(FIR) model filters was derived. Relation between various types of polynomial-based digital filters and the model FIR filter was being developed and to find corresponding modification of the Farrow filter structure for the given poly-phase finite impulse response filter the derived relation could be used.

S. Samadi et al. [32] presented a complete formulation and an accurate resolution to the difficulty of designing systems for simultaneous sampling rate enhance and fractional-sample delay in the Lagrangian sense. The Lagrangian interpolation property has been incorporated into the solution by assuming that the continuous-time version of the signal is a polynomial possessing a Newton series representation. The solution, a three-parameter FIR system, has been derived in the both the time and domains. Frequency-domain properties of the solution have been analyzed and it has been proved that systems are optimal low-pass filters in the maximally flat sense.

M. M. Kashtiban [34] presented the structure for sampling rate alteration from CD to DAT which is optimum and minimum in order. Multistage Implementation of up sampling and down sampling was applied to obtain filter structure which is of minimum order. Using the Implementation proposed the filter order and computations are much more reduced compared to previously defined implementations.

R. Brogovic [35] proposed the efficient implementation of linear FIR filter for sampling rate alteration of signal by arbitrary rational factor. Coefficient symmetry property of linear phase finite impulse response filter is used and the facts are used that in interpolation by factor L, every Lth signal sample is non-zero and in decimation by factor L, every Lth sample is considered at the output. Using these facts efficient filter structure was designed.

O. Gustafsson et al. [37] discussed different alternatives and use of constant matrix multiplication for sample rate conversion. It was shown that rational sampling rate alteration based on finite impulse response(FIR) filter can be described as a constant matrix multiplication. The computational complexity of this realization can be reduced compared with separate multiple constant matrix(MCM) blocks.

Y. ping lu et al. [38] proposed a time-varying filter structure for the improvement of the mathematical calculation efficiency for the sample rate conversion algorithm based on the interpolation and decimation. It was also proposed that changing high sampling rate to reduced rate is of much practical importance in comparison to changing low rate to high one in terms of reducing computational complexity of implementation. The proposed method in this paper was useful to Electronic current transformer (ECT), in which there is need to alter different sampling rates of sequence to the same rate, when the differential protection device is connected with the diverse ECTs of dissimilar sampling rates.

F. Sheikh [39] developed improved structure for rational sample rate conversion in the digital Intermediate frequency(IF) stage of multi-standard wireless transceivers. Novel technique for proficient allocation of decimation (interpolation) factors in a multi-stage sample rate conversion(SRC) architecture is being proposed. New method is based on a factorization algorithm that breaks the sample rate conversion ratios so as to make best use of hardware resource sharing. The projected structure is suitable for digital signal processing implementation in digital intermediate frequency(IF) stage of a software defined radio(SDR) system. The comparison of mathematically complexity and performance of sample rate conversion filters for popular viable standards has been also provided.

G. J. Dolecek [40] presented the modified conventional Cascaded-integrator-comb(CIC) filter for rational sample rate conversion(RSRC). Stepped triangular form of the CIC impulse response filter, the corresponding expanded cosine digital filter, and sine based compensation digital filter is used for overall realization of filter. The proposed filter has an improved pass band leads to improved SNR. This filter performs sampling rate alteration efficiently by use of only additions/subtractions leading to novel filter structure for SDR.

M. Laddomada [41] addressed the design of comprehensive comb decimation digital filter, proposing some narrative decimation schemes tailored to $\sum\Delta$ modulators. In terms of quantization noise rejection and selectivity, the GCFs provides improved performances compared to comb decimation filters but in this case pass-band drop penalty is very limited and computational complexity of the decimation filter realization is increased. Comparisons and tradeoff have been discussed with respect to classic comb filters. The proposed algorithm for approximating the multipliers embedded in sample non recursive filter architecture, with power of 2 coefficients was proposed.

R. tao et al. [42] discussed the sampling of continuous-time frequency limited signal to obtain its error free discrete time version of signal and achieve the ideal sampling rate alteration for discrete time signal. The study proposes the sampling theorem for the fractional fourier transform(FRFT) of frequency limited signals from the point of view of signals and systems. Moreover, this study proposes the sampling rate alteration theory with a factor of fractional ratio, and validates its viability by performing required simulations. The results proposed in this paper extended further for the theories of the fractional fourier transform (FRFT), which can proceed equivalent applications such as filter banks theorem for the fractional fourier transform.

D. W. Barker [43] presented techniques for proficient re-sampling a discrete time signal. Implementations such as use of single tapped delay line digital filter to reduce the input sampling data storage requirement and to compute the filter coefficients for interpolation and decimation filter, and provided the information with regard to minimizing the re-samplers timing jitter error.

G. J. Dolecek [44] addressed the structure of cost-effective recursive generalized comb filters (GCFs) by proposing an efficient technique employing power-of-2 (PO2) terms to quantize the multipliers in the *z*-transfer function. Design of multiplier less and recursive GCFs by proposing an effective technique to jointly quantize the coefficients in the *z*-transfer function in such a way as to meet perfect pole–zero cancelation was focused.

N. R. Nagrale [45] presented a novel algorithm for decimation system. The overall memory elements and computational load was reduced by the proposed algorithm. The proposed implementation improves the rational decimation system by implementing the two stage decimator filters at the regions where sampling rate is minimum. There is a potential reduction in computational complexity by implementing the two stage of decimator. The proposed structure reduces the overall memory and power requirement therefore, the proposed configuration shows efficient distinctiveness to be applied for Software Defined Radio(SDR) receiver.

R. Bregovic et al. [46] proposed an proficient filter structure for implementing a finite impulse response (FIR) filter with linear phase for an a given order N for sampling-rate alteration by rational factor L/M , where L(M) is the integer up-sampling (down sampling) factor to be performed before or after the filter. In the proposed realization, the coefficient symmetry property of FIR linear phase filter is taken in account and the requirement of delay elements can be kept low. The proposed implementation is based on the following three facts;

1. The impulse response of filter is symmetrical.
2. Only every Lth input sample applied to filter has a nonzero value.
3. Only every Mth output sample has to be considered after filtering operation.

By applying these properties, the realization which is efficient in computational complexity than previously defined implementations has been achieved. The method proposed in this paper does not exactly reduce the computational complexity by factor of two as compared with the poly-phase decomposition method. It was mentioned that the proposed implementation becomes impractical for larger values of L and M.

G. Bi et al. [47] presented the methods of rational sampling rate conversion by manipulating the discrete cosine transforms. Conversion error performance and the computational efficiency are compared with existing methods. Since the proposed methods performs filtering with ideal pass band response and zero transitional band, so high conversion accuracy can be achieved by using this method. The overlap operation is used to minimize the conversion errors. The concept of given methods is simple and better conversion accuracy can be achieved with much less computational costs.

N. Takahashi et al. [48] described a technique (in rational sampling rate conversion by L/M) to overcome the difficulty of requirement of extremely narrow normalized bandwidth and a sharp transition characteristic when both L and M have large values and both L and M are composite numbers, giving an multistage converter structure where each stage is consisting of an up-sampler and a down-sampler, both of a small conversion ratios, with a filter having not so sharp normalized transition characteristic in the middle, remarkably reduced total computation complexity.

CHAPTER 3

FIR FILTER STRUCTURES FOR SAMPLE RATE CONVERTER

In Chapter 1. we described the task of digital filters for sampling rate conversion. In this chapter the aspects of implementation of interpolation and decimation are discussed. Initially all the computations are to be done on higher sampling frequency. The aim is to design alteration structures for which the mathematics operations of the filter are to be performed at the lower sampling rate. The overall computational complexity can be reduced by using this type of structure.

3.1. Basic Implementations

In sample rate conversion digital filters play very important role and anti-aliasing filters are used before decimation process and anti-imaging filters are used after interpolation process. The performance of these anti-imaging and anti-aliasing filters defines the overall performance of a decimator and/or interpolator. As described in Chapter 1, the operations of filtering are to be performed at the higher sampling rate.

3.1.1 FIR Decimator

In the basic realization of an FIR decimator, a direct-form finite impulse response filter is used in series with the down sampling operation as described in fig. 3.1. The FIR filter acts as anti-aliasing filter**.** In this basic implementation of the FIR decimator, the number of the multiplications per output sample in the decimator is equal to the FIR filter length N + 1.

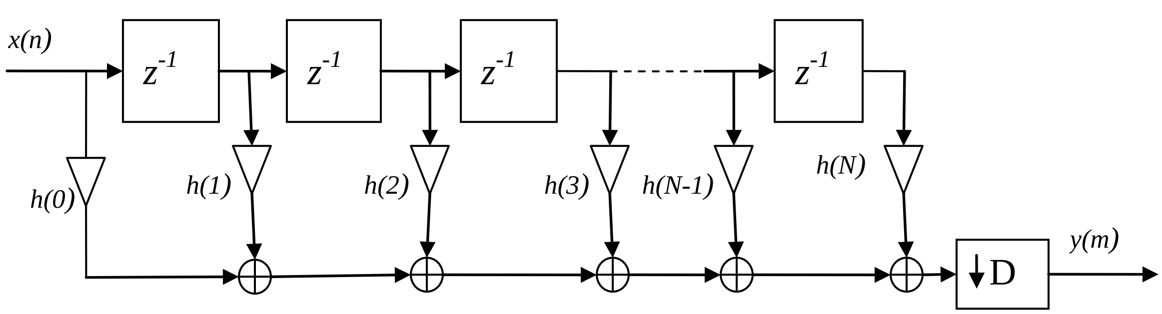


Figure 3.1. Basic realization of FIR filter for Decimator [5].

3.1.2 FIR Interpolator

The interpolator is a series structure of an up-sampler followed by an FIR filter which acts as an anti-imaging digital filter, represented in fig. 3.2. As in the case of FIR decimator multiplications per output sample is N+1, where N is the filter order.

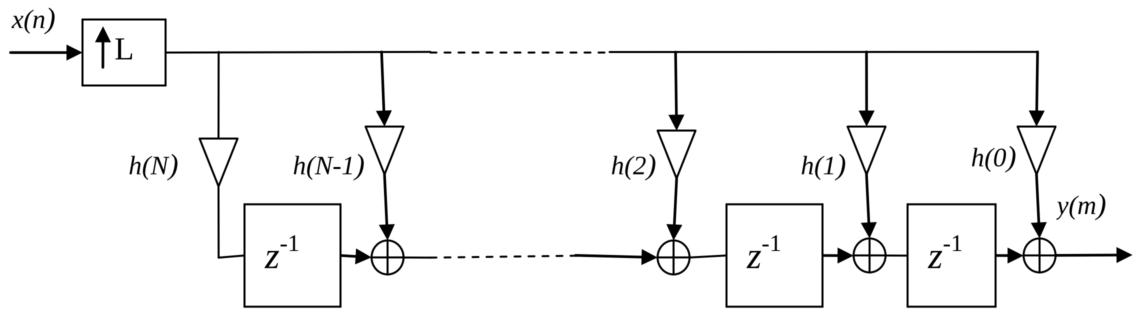
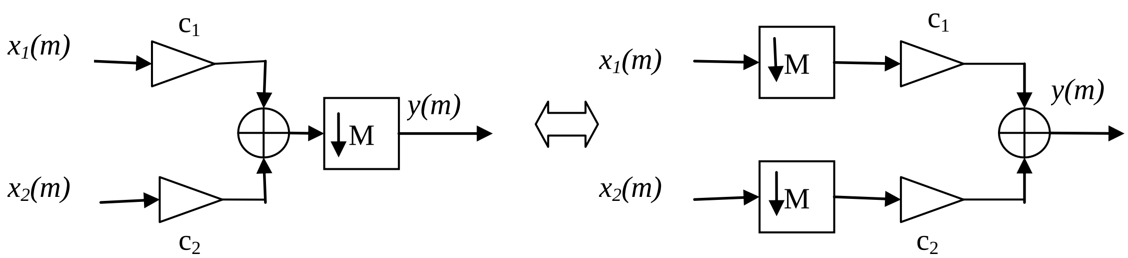


Figure 3.2. Basic Implementation of FIR interpolator [5].

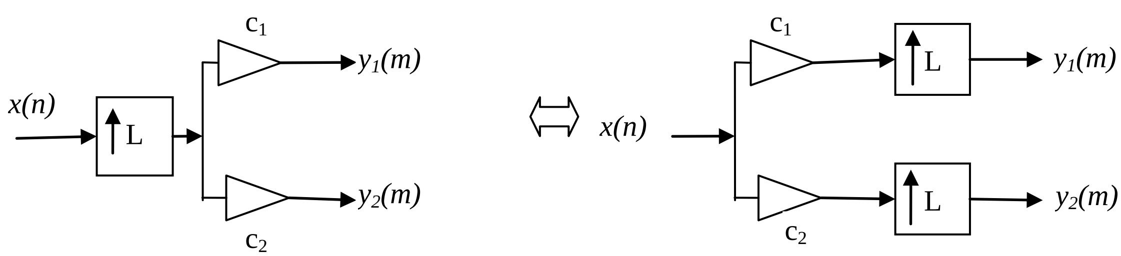
Implementation of rational Sample rate converter is same as the implementations of FIR interpolator and decimator, where filter is in between interpolator and decimator which act as anti-imaging and anti-aliasing filter simultaneously. Also the number of multiplications is given by order of filter plus one.

3.2. Noble Identities

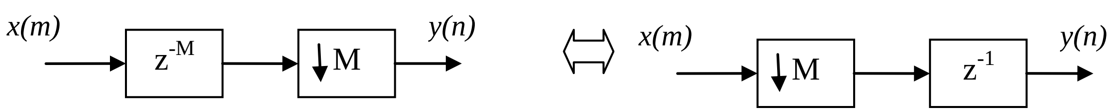
The six noble identities, used to efficiently move the down sampler and up sampler to a advantageous position to make an efficient sample rate conversion structure. It results in the performance of multiplications and additions at lower sampling rates. In sampling rate converter, due to the operations of filtering in higher sampling rate, the computational complexity can be improved by introducing down sampling (up sampling) operations into the filter structures. In the identities shown in fig. 3.3.(a) and 3.3.(b) respectively, additions and multiplications can be moved to lower sampling rate. In third and fourth identities, shown by fig. 3.3(c) and 3.3(d) respectively show that a delay of M or L sampling periods at higher sampling rate is equivalent to a delay of one sampling period at the lower rate. In the identities shown by fig. 3.3(e) and 3.3(f) respectively, the generalized form of the third and fourth identities is given. These noble identities are used in Poly-phase implementations of FIR filter in SRC.



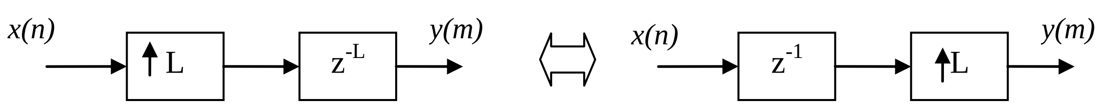
(a)



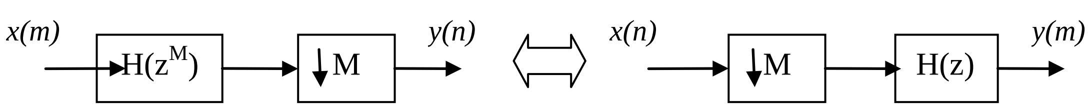
(b)



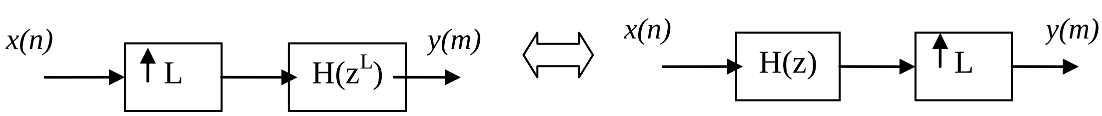
(c)



(d)



(e)



(f)

Figure 3.3. Noble identities [5].

3.3. Polyphase Implementation

The basic procedure of re-sampling a discrete time sequence by an integer factor consists of either inserting a sequence of zero samples between each input sample followed by low-pass anti-imaging digital filter (interpolation) or low-pass anti-aliasing filtering of an input signal and discarding some samples at the output (decimation). To improve the computational complexity of digital filter, poly-phase filters were introduced. Using this implementations at interpolator the multiply by zero samples can be eliminated and at decimator low pass filter output computations are avoided which are to be discarded at the output [12]. The realization of a higher order FIR filter in parallel structure can be done based on polyphase decomposition. The transfer function of digital FIR filter is to be decomposed into M or L lower-order transfer functions, called the poly-phase components, which are added together later-on to form the original overall transfer function. For the sake of simplicity poly-phase decomposition of filter *H(Z)* of order *N* as represented by equation (3.1) and (3.2) can be done into two equivalent filters $E_0(Z)$ and $E_1(Z)$ given by equation (3.3) and (3.4) respectively.

$$H(Z) = h(0)+ h(1)Z^{-1}+ h(2)Z^{-2}+ h(3)Z^{-3}+ \ldots\ldots h(N-2)Z^{-(N-2)}+h(N-1)Z^{-(N-1)} \quad (3.1)$$

$$H(Z) = h(0)+ h(2)Z^{-2}+ \ldots\ldots h(N-2)Z^{-(N-2)}$$
$$+ Z^{-1}(h(1)+ h(3)Z^{-2}+\ldots+ h(N-1)Z^{-(N-1)}) \quad (3.2)$$

$$E_0(Z^2)= h(0)+ h(2)Z^{-2}+ \ldots\ldots h(N-2)Z^{-(N-2)} \quad (3.3)$$

$$E_1(Z^2) =h(1)+ h(3)Z^{-2}+\ldots+ h(N-1)Z^{-(N-2)} \quad (3.4)$$

The transfer function *H(Z)* represented by equation (3.1) can also be represented as sum of two poly-phase components $E_0(Z^2)$ and $E_1(Z^2)$ as

$$H\left(Z\right)= E_0\left(Z^2\right)+Z^{-1}E_1\left(Z^2\right) \quad (3.5)$$

An FIR digital filter can be implemented as a parallel structure of M or L poly-phase components, which are added together at the output. The poly-phase components are sometimes called poly-phase sub filters or poly-phase branches. A poly-phase component is usually implemented in the direct transversal form. fig. 3.4(a) shows a decimator composed of the series connection of an FIR filter implemented as a parallel connection of M poly-phase branches, and factor-of-M down-sampler. In fig. 3.4(b) noble identities described in section 3.2 are used to reduce the computational complexity of SRC. Similar structure for Interpolation can be implemented as shown in fig. 3.5.

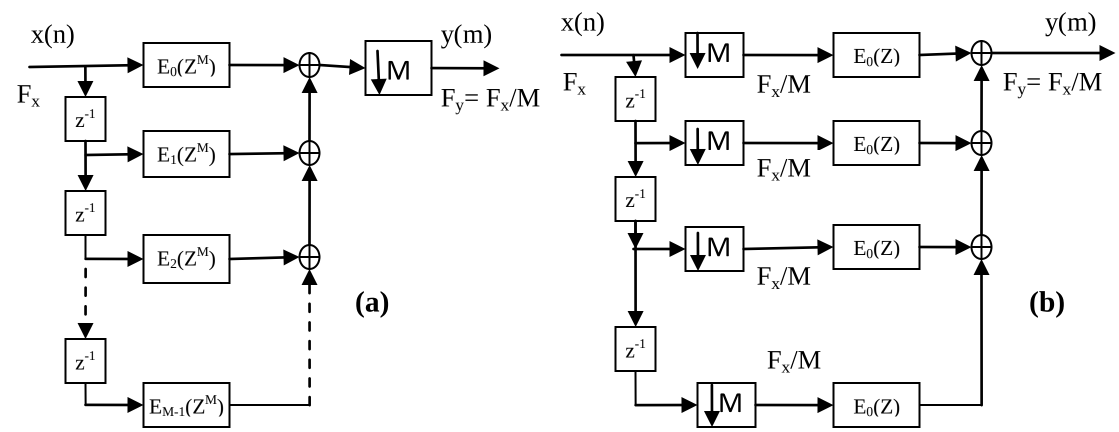


Figure 3.4. Poly-phase Implementation of Decimator (a) Poly-phase filter structure followed by decimator.(b) Computational efficient structure of decimation [12].

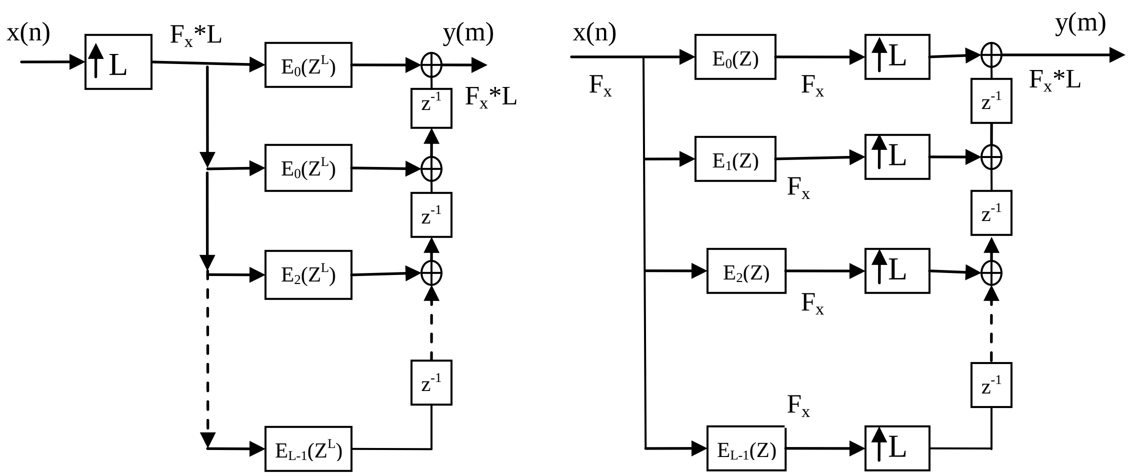


Figure 3.5. Polyphase Implementation of Interpolator (a)Polyphase filter structure preceded by Interpolator.(b) Computational efficient structure of Interpolation [12].

3.3.1. Polyphase Implementation of Rational Sample Rate Converter

The poly-phase configurations have been developed which enable the mathematical operations to be evaluated at the lower sampling frequency. The computationally efficient fractional sampling rate converters based on the polyphase decomposition of FIR filters are described in [16]. A rational (L/M) sampling rate conversion structure can be realized with a 1-to-L interpolator followed by an M-to-1 decimator, (fig. 3.6) where L and M are mutually prime numbers. The narrow band digital filter *H(z)* between the up and down samplers is used for anti-imaging as well as anti-aliasing purposes.

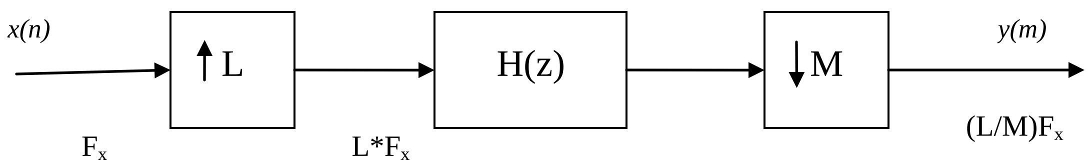


Figure 3.6. Rational sampling rate converter [16].

The filter H(z) can be decomposed into L or M polyphase branches and can be moved to the lower sampling rate as shown in figure 3.7(a) and 3.7(b) depending on the value of L and M.

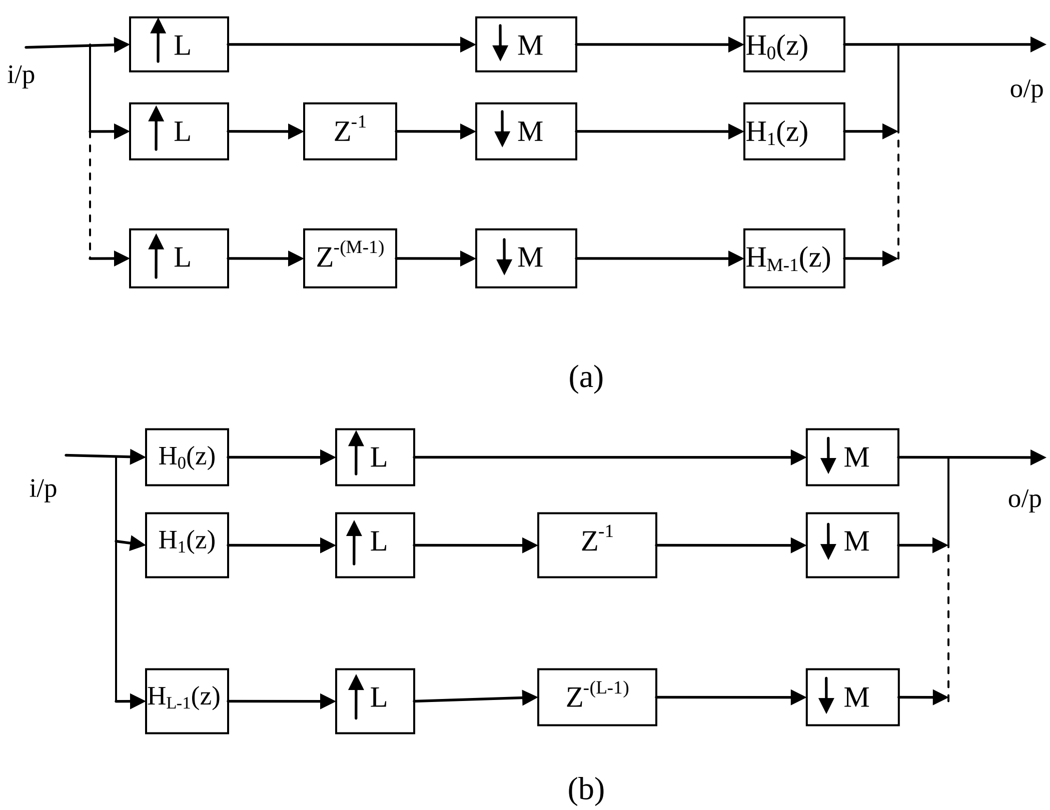


Figure 3.7. Poly-phase implementation of L/M SRC (a) M>L, (b) L>M [16].

Multiplication and Addition complexities for polyphase structure is lower that direct implementation structure. Fig. 3.8(a) and 3.8(b) below shows the computational complexity v/s filter order graph for rational factor 3/5 for which filter is moved to lower sampling side at input side of structure.

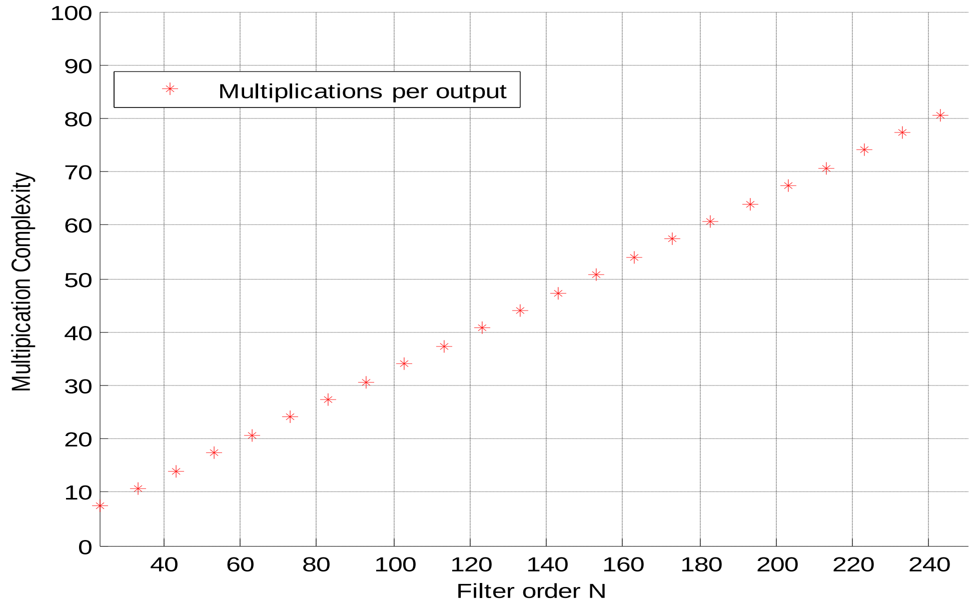


Figure 3.8(a) Multiplication complexity for polyphase structure

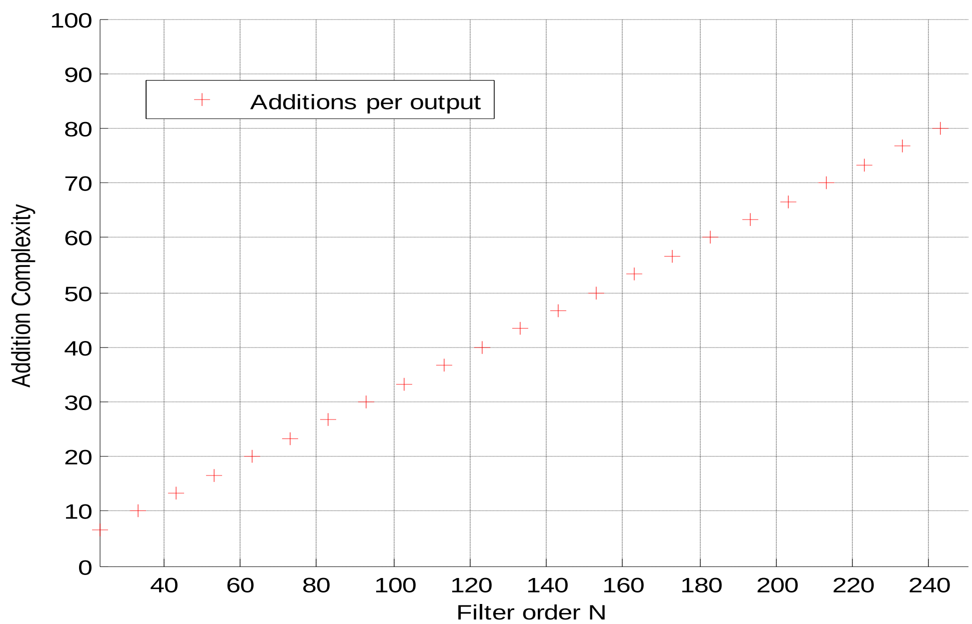


Figure 3.8(b) Addition complexity for polyphase structure

3.4. Sampling Rate Conversion Exploiting Coefficient Symmetry

The Coefficient Symmetry property of FIR filter *H(z)*, used in sampling rate compression, which suppresses the Image signals as well as prevent from aliasing effect can be used efficiently in sampling rate converter [46]. The filter *H(z)* of order *N* and its coefficient filter property are defined by equation (3.6) and (3.7) respectively.

$$H(z) = \sum_{k=0}^{N} h_k z^{-k} \tag{3.6}$$

$$h_{N-k} = h_k, \qquad k = 0,1,\ldots\ldots N \tag{3.7}$$

Time domain relation of figure(1.9) defined in chapter(1) can be defined by following set of equations.

$$w(i) = \begin{cases} x\left(\frac{i}{L}\right); & \text{for } n = 0, L, 2L, \ldots. \\ 0; & \text{otherwise} \end{cases} \tag{3.8}$$

$$v(i) = \sum_{k=0}^{N} h_k w(i-k) \tag{3.9}$$

$$y(n) = v(Mn) \tag{3.10}$$

Till now coefficient symmetry is not used and will be used in further steps. Signal x(n) is assumed to be casual i.e. x(n)=0 for n<0. Equations (3.8),(3.9) and (3.10) can be combined to give the direct relation between input and output given by (3.11).

$$y[n] = \sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L}\right] \tag{3.11}$$

Since the sequence x(n) exist only for integer values of n, so (3.11) takes only those values for which *(Mn-k)/L* is an integer. Above equation shows the relation between input and output in linear form, to get this relation in matrix form (3.11) can be further manipulated described by following steps. Based on (3.11) , *y(n+KL)* for K be an integer can be calculated by use same filter coefficient h_k by shifting x(n) by factor KM as shown by (3.12)

$$y[n+KL]=\sum_{k=0}^{N} h_k x\left[\frac{M(n+KL)-k}{L}\right]$$

$$=\sum_{k=0}^{N} h_k x\left[\frac{Mn-k}{L}+MK\right] \quad (3.12)$$

To get the generalized array y[n+l] for l=0,1,…..L-1 from the input array we can write y[n+l] as

$$y[n+l]=\sum_{k=0}^{N} h_{(lM+(K_l-\lfloor lM/L\rfloor))L}\, x\left[\frac{Mn}{L}-K_l+\left\lfloor\frac{lM}{L}\right\rfloor\right]$$

$$=\sum_{k=0}^{N} h_k x\left[\frac{Mn}{L}-\frac{k-lM}{L}\right] \quad (3.13)$$

For n to take the values *0,L,2L…*, the term *(Mn/L)* will take values 0,M,2M,…., and to take integer values of x in (3.13), the term *(k-lM)/L* should be integer for which *k* should be given by

$$k=\text{mod}(lM,L)+K_lL \quad (3.14)$$

The value of *k* is bounded by N, $0<k<N$ and k_l is bounded by $K_l^{\max}$, $0 < K_l < K_l^{\max}$ where $k_l^{\max}$ is defined by

$$K_l^{\max}=\left\lfloor\frac{(N-\text{mod}(lM,L))}{L}\right\rfloor=\left\lfloor\frac{N-lM}{L}\right\rfloor+\left\lfloor\frac{lM}{L}\right\rfloor \quad (3.15)$$

$$y[n+l]=\sum_{k=0}^{N} h_{(lM+(K_l-\lfloor lM/L\rfloor))L}\, x\left[\frac{Mn}{L}-K_l+\left\lfloor\frac{lM}{L}\right\rfloor\right]$$

$$=\begin{bmatrix} h_{lM-\lfloor lM/L\rfloor L} \\ h_{lM-\lfloor lM/L\rfloor L+L} \\ : \\ h_{lM+\lfloor (N-lM)/L\rfloor L} \end{bmatrix}^T \begin{bmatrix} x\left[m+\lfloor lM/L\rfloor\right] \\ x\left[m+\lfloor lM/L\rfloor-1\right] \\ : \\ x\left[m-\lfloor lM/L\rfloor\right] \end{bmatrix} \quad (3.16)$$

y(n+l) given by equation can be written in compact matrix form(3.17), where output vector $\mathbf{y}_{n,I}$ is product of filter coefficient matrix $\mathbf{H}_{L\times(p+q+1)}$ and input signal vector $\mathbf{x}_{m+p,m-q}$.

$$\mathbf{y}_{n,L} = \mathbf{H}_{L\times(p+q+1)}\mathbf{x}_{m+p,m-q} \tag{3.17}$$

Where $\mathbf{y}_{n,L}$, q, p, $\mathbf{x}_{m+p,m-q}$, and $\mathbf{H}_{L\times(p+q+1)}$ are given by equation (3.18) through (3.22)

$$y_{n,L}=[y[n]\ \ y[n+1]\ \ y[n+2]\ \ldots\ldots\ y[n+L-1]]^T \tag{3.18}$$

$$q = \left\lfloor \frac{N}{L} \right\rfloor \tag{3.19}$$

$$p = \left\lfloor \frac{(L-1)M}{L} \right\rfloor \tag{3.20}$$

$$\mathbf{x}_{(m+p),(m-q)}=[x[m+p]\ x[m+p-1]\ \ldots\ldots\ x[m-q]] \tag{3.21}$$

$$\mathbf{H}_{L\times(p+q+1)} = \begin{bmatrix} h_{-pL} & .. & h_{-L} & h_0 & h_L & .. & h_{(q-1)L} & h_{qL} \\ h_{M-pL} & .. & h_{M-L} & h_M & h_{M+I} & .. & h_{M+(q-1)L} & h_{M+qL} \\ h_{2M-pL} & .. & h_{2M-I} & h_{2M} & h_{2M+L} & .. & h_{2M+(q-1)L} & h_{2M+qL} \\ .. & .. & .. & .. & .. & .. & .. & .. \\ h_{(L-1)M-pL} & .. & h_{(L-1)M-L} & h_{(L-1)M} & h_{(L-1)M+L} & .. & h_{(L-1)M+(q-1)L} & h_{(L-1)M+qL} \end{bmatrix} \tag{3.22}$$

To estimate the complexity of this rational sampling rate converter, the input-output transfer matrix $\mathbf{H}_{L\times(p+q+1)}$ given by (3.22) can be broken into two parts $\mathbf{H}_{C1}$ and $\mathbf{H}_{C2}$ as follows,

$$\mathbf{H}_{L\times(p+q+1)} = \begin{bmatrix} \mathbf{0}_{L_1,p-p_1} & \mathbf{H}_{C1} \\ \mathbf{H}_{C2} & \mathbf{0}_{L_2,q-q_2} \end{bmatrix} \tag{3.23}$$

$$L_1 = r+1 \tag{3.24}$$

$$L_2 = L - L_1 \tag{3.25}$$

where r is last row of matrix $\mathbf{H}_{C1}$, finding the value of r corresponds to find an integer $r \in \{0,1,....,L-1\}$ such that

$$mod\left(rM, L\right) \; = \; N - \; qL \tag{3.26}$$

$$p_1 = \frac{(L_1 - 1)M - (N - qL)}{L} \tag{3.27}$$

$$q_2 = \left\lfloor \frac{N - \text{mod}(L_1 M, L)}{L} \right\rfloor - \left\lfloor \frac{L_1 M}{L} \right\rfloor \tag{3.28}$$

When implementing matrices HC1 and HC2 the size of matrices is L_H by 2λ where L_H and λ are given by;

$$L_H = \begin{cases} L_1, & forH_{C1} \\ L_2, & forH_{C2} \end{cases} \tag{3.29}$$

$$\lambda = \begin{cases} \left\lfloor \dfrac{q + p_1 + 1}{2} \right\rfloor & forH_{C1} \\ \left\lfloor \dfrac{q_2 + p + 1}{2} \right\rfloor & forH_{C2} \end{cases} \tag{3.30}$$

Multiplication Complexity is denoted by C_{pm}. Multiplication complexity of matrix H_{C1} is given by;

$$C_{mHc1} = \lambda \tag{3.31}$$

The multiplication complexity of matrix H_{C2} of size L_H by 2λ is given by

$$C_{mHc2} = \lambda + \frac{1}{L_H} \left\lfloor \frac{L_H}{2} \right\rfloor \tag{3.32}$$

The total multiplication complexity of sample rate converter is given by

$$C_{pm} = \frac{L_1 C_{mH_{C1}} + L_2 C_{mH_{C2}}}{L} \tag{3.33}$$

Addition complexity of matrix H_{C1} is given by;

$$C_{aHc1} = \begin{cases} \lambda + \dfrac{2\lambda}{L_H} - \dfrac{\text{mod}(L_H, 2)}{L_H} & , for.L_H > 1 \\ 2\lambda - 1 & , for.L_H = 1 \end{cases} \tag{3.34}$$

The multiplication complexity of matrix H_{C2} of size L_H by 2λ is given by

$$C_{aHc2} = \begin{cases} \lambda + \dfrac{2\lambda}{L_H} + 1 - \dfrac{\text{mod}(L_H, 2)}{L_H} & , for.L_H > 1 \\ 2\lambda & , for.L_H = 1 \end{cases} \tag{3.35}$$

The total addition complexity of sample rate converter denoted by C_{pa} is given by

$$C_{pa} = \frac{L_1 C_{aH_{C1}} + L_2 C_{aH_{C2}}}{L} \tag{3.36}$$

The Computational complexities for implementation using coefficient symmetry are reduced nearly half of that of polyphase structure and are given by fig. 3.9(a) and 3.9(b).

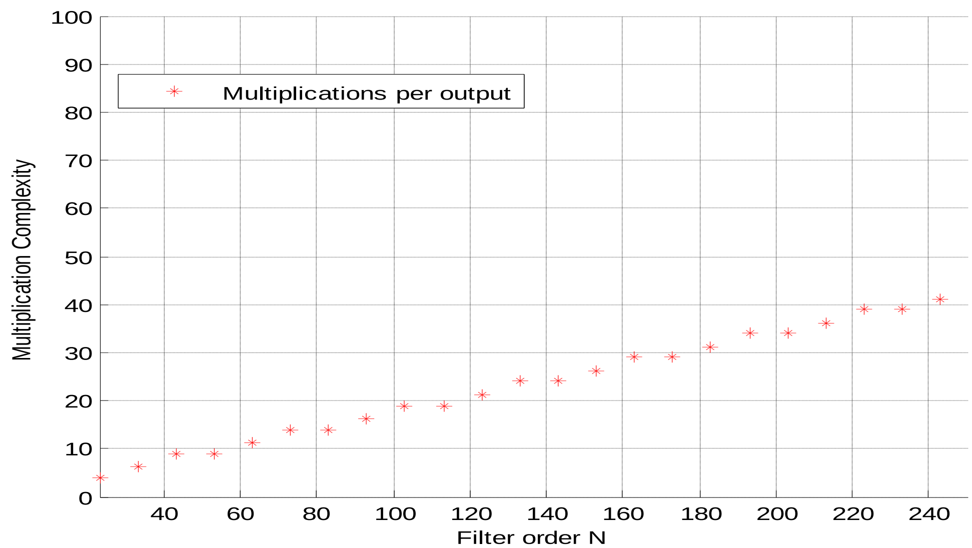


Figure 3.9(a) Multiplication complexity for coefficient symmetric structure (L/M=3/5)

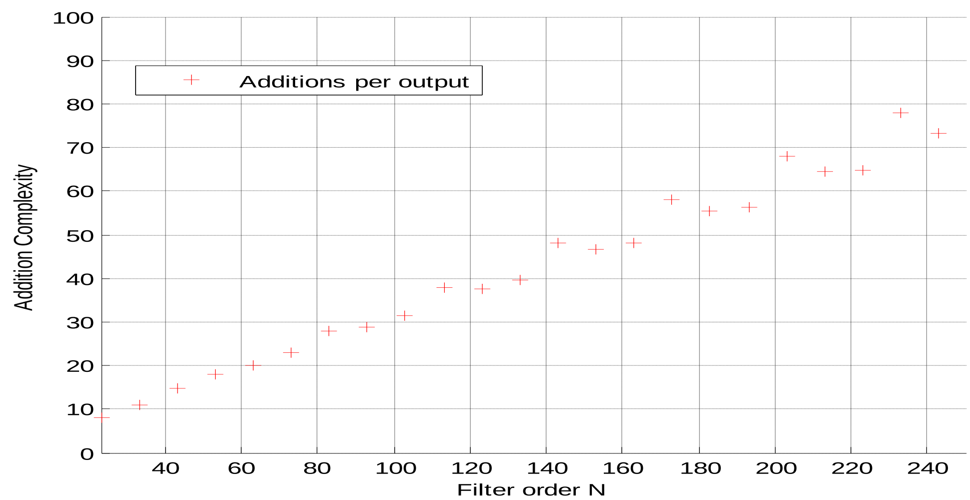


Figure 3.9(b) Addition complexity for coefficient symmetric structure (L/M=3/5)

CHAPTER 4

PROPOSED STRUCTURE FOR SAMPLE RATE CONVERTER

In this chapter new proposed structure of filter in sample rate conversion is discussed based on the structure defined in literature. The new proposed structure is efficient in terms of computational complexity and storage complexity.

4.1. Proposed Lth band filter for Rational Sample Rate Converter

Lth band digital filters are used in single rate and multi rate digital signal processing. The characteristics of these types of filters is that its cut off frequency is located at π/L, and symmetric transition band. Every Lth sample from centre sample has zero value in time domain, and value of central sample is 1/L. This type of filter exhibits zero inter-symbol interference property because of the zero crossings of impulse response at regular intervals. Implementation multiplication complexities can be reduced up to significant level using Lth band filter. The Lth band filters can be used in multi rate signal processing due to their interesting properties.

Impulse response and frequency response of Lth band filter for L=4 of order N=19 is described in figure 4.1(a) and 4.1(b) respectively.

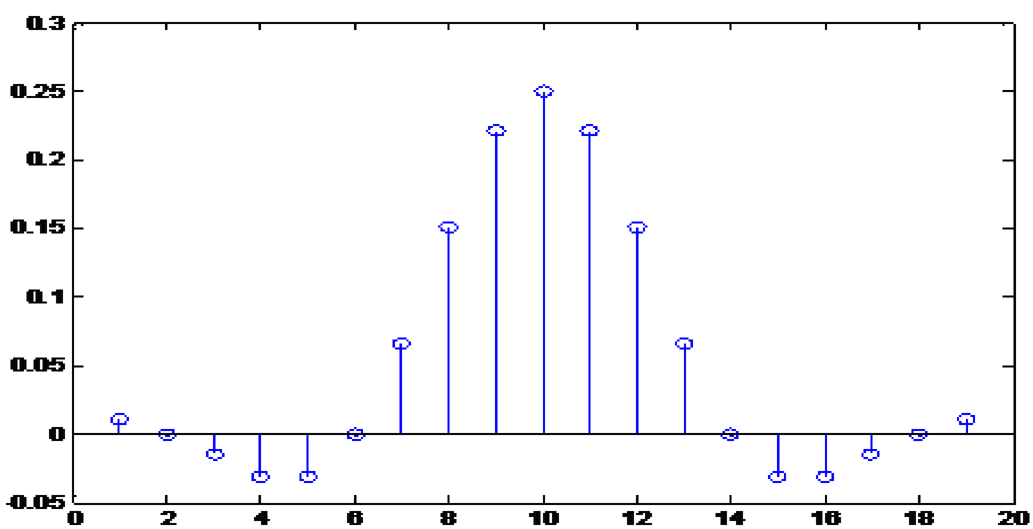


Figure 4.1 (a) Impulse response of Lth band filter(L=4,N=19)

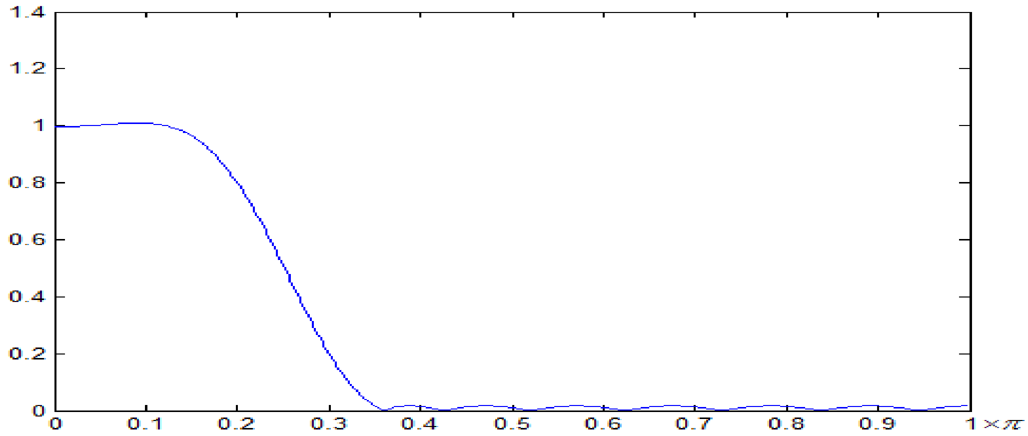


Figure 4.1. (b) Frequency response of Lth band filter (L=4,N=19)

The transfer function H(z) of Lth band filter of order $N=2K+1$ can be described by following relation

$$H(z)=\sum_{n=0}^{2K}h(n)z^{-n} \tag{4.1}$$

Impulse response h(n) of Lth band filter is symmetric in nature and can be described by

$$h(2K-n)=h(n) \qquad \text{for } n=0,1,2,.....2K \tag{4.2}$$

The frequency response $H(e^{jw})$ and zero phase frequency response $H(w)$ of Lth band filter is given by (4.3) and (4.4) respectively.

$$H(e^{jw})=e^{-jkw}H(w) \tag{4.3}$$

$$H(w)=1/L+2\sum_{n=1}^{K}h(K-n)\cos(wn) \tag{4.4}$$

The impulse response $h(n)$ and frequency response $H(w)$ of Lth band filter satisfies the following two properties

$$h(K)=1/L, h(K+rL)=0 \qquad \text{for } r=1,2,\dots\dots\left\lfloor\frac{K}{L}\right\rfloor \tag{4.5}$$

$$\sum_{r=0}^{L-1}H(w+2\pi rl/L)=1 \tag{4.6}$$

The pass band and stop band edge frequencies w_p and w_s of Lth band filter are symmetric about the frequency π/L . These cut off frequencies can be defined as a function of roll off factor ρ of response in transition band of filter as

$$w_p=(1-\rho)\,\pi/L \quad \text{and} \quad w_s=(1+\rho)\,\pi/L \tag{4.7}$$

Roll off factor ρ is defined in range 0<ρ<1 and total transition bandwidth (w_p-w_s) is given by

$$w_s-w_p=2\rho\,\pi/L \tag{4.8}$$

The relation between pass band and stop band ripples, δ_p and δ_s respectively is given by

$$\delta_p=(1-L)\delta_s \tag{4.9}$$

The multiplication and addition complexity can be drawn as shown in fig. 4.2(a) and 4.2(b) respectively as below,

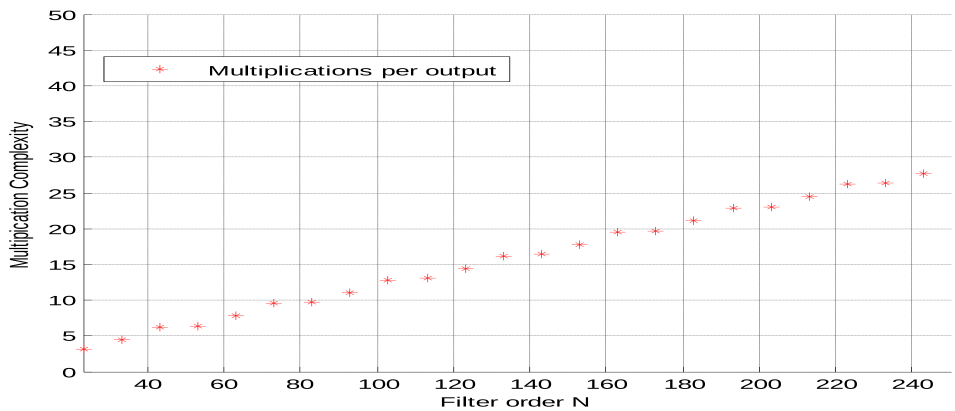


Figure 4.2(a) Multiplication complexity for proposed structure (L/M=3/5)

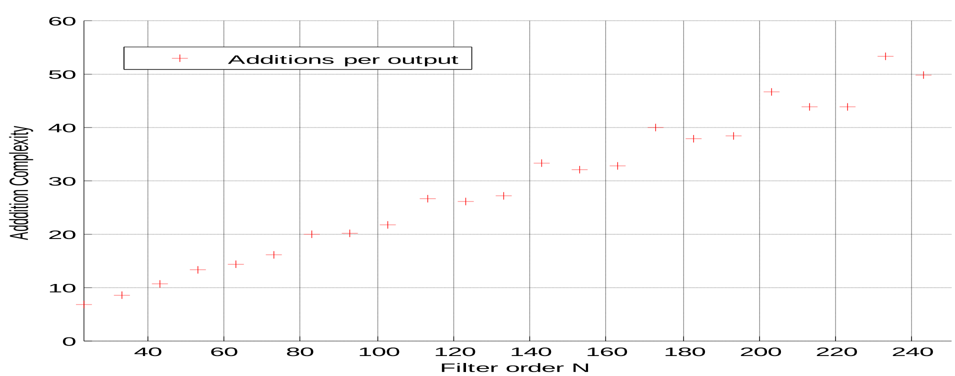


Figure 4.2(b) Addition complexity for proposed structure (L/M=3/5)

4.2. Design example of Sample Rate Converter using proposed method

In this section design of efficient sample rate conversion filter of order N=26 for rational factor (3/5) by combining the method specified by equation(3.17) and Lth band property specified by equation(4.5) is given. A specified in section 3.4 the output signal samples of sampling rate converter as a function of input signal samples is given in matrix multiplication form as

$$\mathbf{y}_{n,3} = \mathbf{H}_{3\times 12}\mathbf{x}_{m+3,m\text{-}8} \tag{4.10}$$

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & h_0 & h_3 & h_6 & h_9 & h_{12} & h_{11} & h_6 & h_5 & h_2 \\ 0 & 0 & h_2 & h_5 & h_8 & h_{11} & h_{12} & h_9 & h_6 & h_3 & h_0 & 0 \\ h_1 & h_4 & h_7 & h_{10} & h_{13} & h_{10} & h_7 & h_4 & h_1 & 0 & 0 & 0 \end{bmatrix} \mathbf{x}_{m+3,m-8} \tag{4.11}$$

for n= 0,L,2L,... = 0,3,6,.. , the values of m are described as m=(5/3)n and the vector $\mathbf{x}_{\text{m+2,m-4}}$ is described by equation(3.21). Since we are utilizing Lth band filter property so the value of central coefficient is 1/3 and can be normalized to 1 and every 3rd coefficient from centre coefficient is zero i.e. h_1, h_4, h_7 and h_{10} are zero. So the equation (4.11) can be re-written as

$$\begin{bmatrix} y(n) \\ y(n+1) \\ y(n+2) \end{bmatrix} = \begin{bmatrix} 0 & h_0 & h_3 & h_6 & h_9 & h_{12} & h_{11} & h_6 & h_5 & h_2 \\ h_2 & h_5 & h_8 & h_{11} & h_{12} & h_9 & h_6 & h_3 & h_0 & 0 \\ 0 & 0 & h_{13} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \mathbf{x}_{m+1,m-8} \tag{4.12}$$

To implement the sampling rate conversion efficiently, the above structure can be split into following two parts:

$$\begin{bmatrix} y(n) \\ y(n+1) \end{bmatrix} = \begin{bmatrix} 0 & h_0 & h_3 & h_6 & h_9 & h_{12} & h_{11} & h_8 & h_5 & h_2 \\ h_2 & h_5 & h_8 & h_{11} & h_{12} & h_9 & h_6 & h_3 & h_0 & 0 \end{bmatrix} \mathbf{x}_{m+1,m-8}$$

$$\begin{bmatrix} y(n) \\ y(n+1) \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \begin{bmatrix} c_0 & c_1 & c_2 & c_3 & c_4 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & d_4 & d_3 & d_2 & d_1 & d_0 \end{bmatrix} \mathbf{x}^{(4)}_{m+1,m-8} \tag{4.13a}$$

where

$$c_0 = \frac{h_2}{2}, d_0 = -\frac{h_2}{2}, c_1 = \frac{h_0 + h_5}{2}, d_1 = \frac{h_0 - h_5}{2}, c_2 = \frac{h_3 + h_8}{2}, d_2 = \frac{h_3 - h_8}{2}$$

$$c_3 = \frac{h_6 + h_{11}}{2}, d_3 = \frac{h_6 - h_{11}}{2}, c_4 = \frac{h_9 + h_{12}}{2}, d_4 = \frac{h_9 - h_{12}}{2}.$$

$$\mathbf{x}^4_{m+1,m-8} = \begin{bmatrix} \mathbf{I_5} & \mathbf{J_5} \\ \mathbf{J}_5 & \mathbf{-I_5} \end{bmatrix} \mathbf{x}_{m+1.m-8}$$

The coefficients c_0, c_1, c_2, c_3, c_4, d_0, d_1, d_2, d_3 and d_4 are dependent on fiter coefficients and can be calculated in advance. $\mathbf{I_5}$ and $\mathbf{J_5}$ are identity and counter identity matrix respectively.

$$\left[y(n+2)\right] = h_{13}x_{m-1} \tag{4.13b}$$

The structure for implementing the filter structure shown by equation (4.13a) and (4.13b) is shown in fig. 4.3.

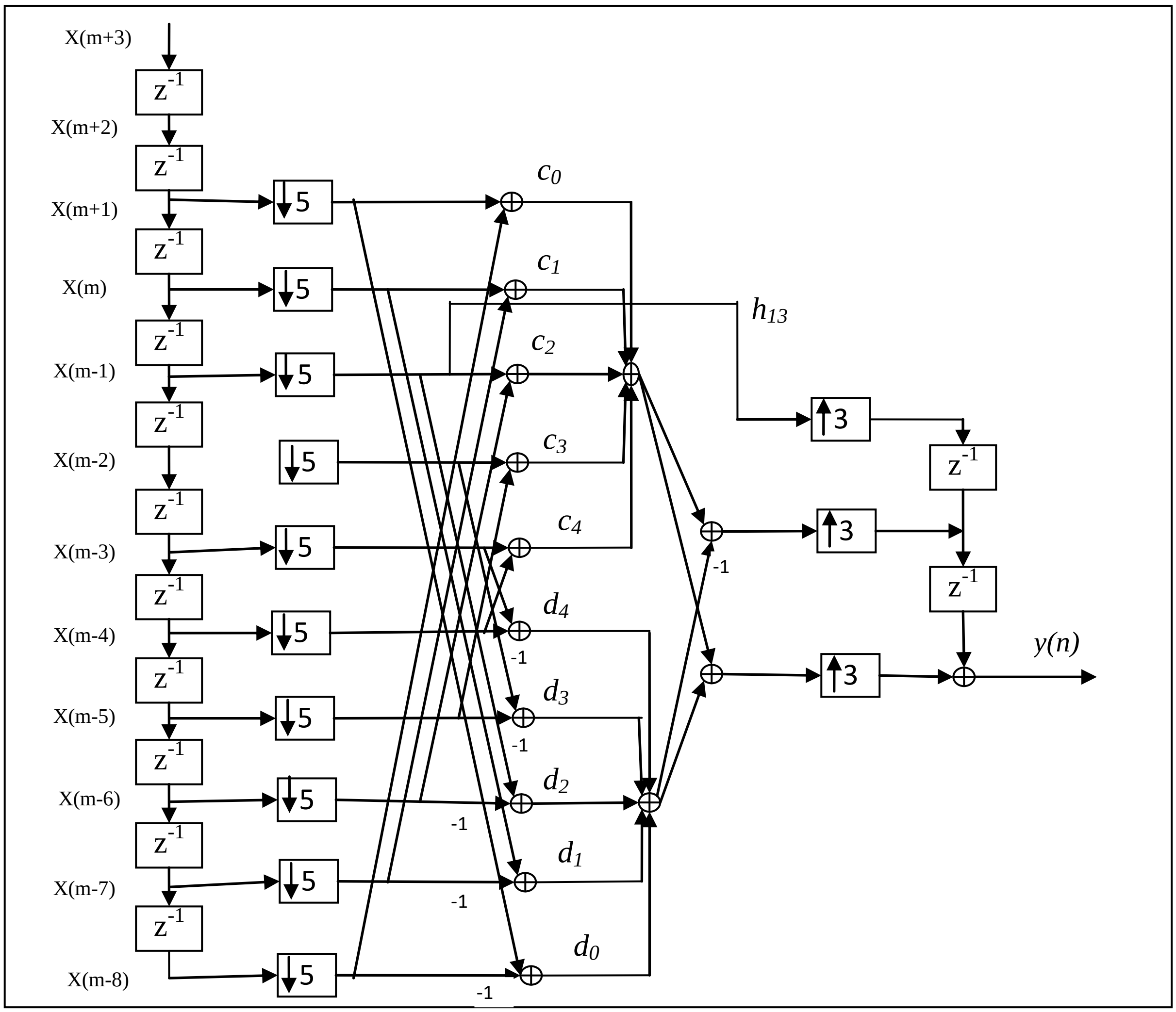


Figure 4.3. Proposed Implementation using coefficient symmetry and Lth band filter property for rational factor 3/5.

4.2.1 Simulation of Proposed Design Structure

In this section simulation of proposed sample rate converter structure using filter order 26 is done in MATLAB by taking a sinusoidal signal of frequency 12 KHz initially sampled at sampling frequency of 96 KHz. This signal is resampled by factor 3/5. The sampling frequency will become 57.6 KHz. Spectrum of original sampled signal and resampled signal is analyzed.

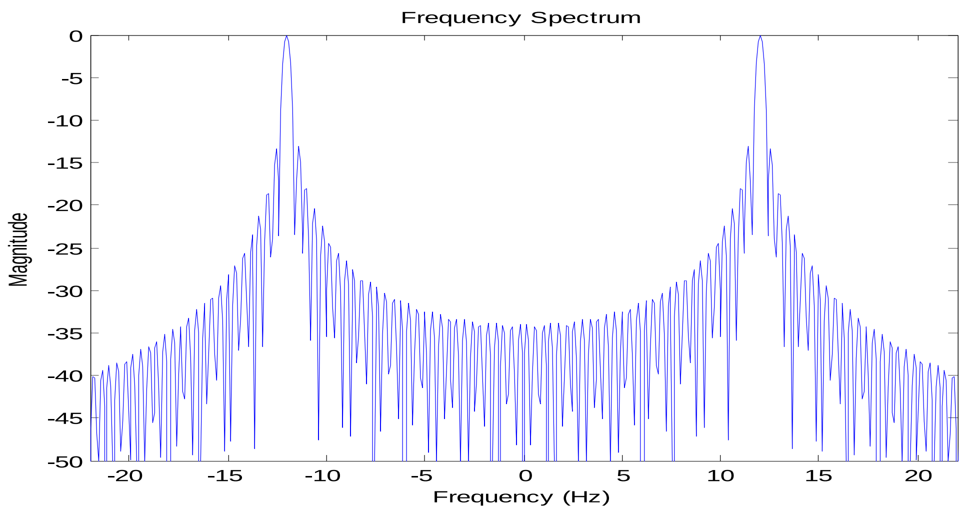


Figure 4.4 Frequency Spectrum of sinusoidal signal(12KHz) sampled at 96 KHz

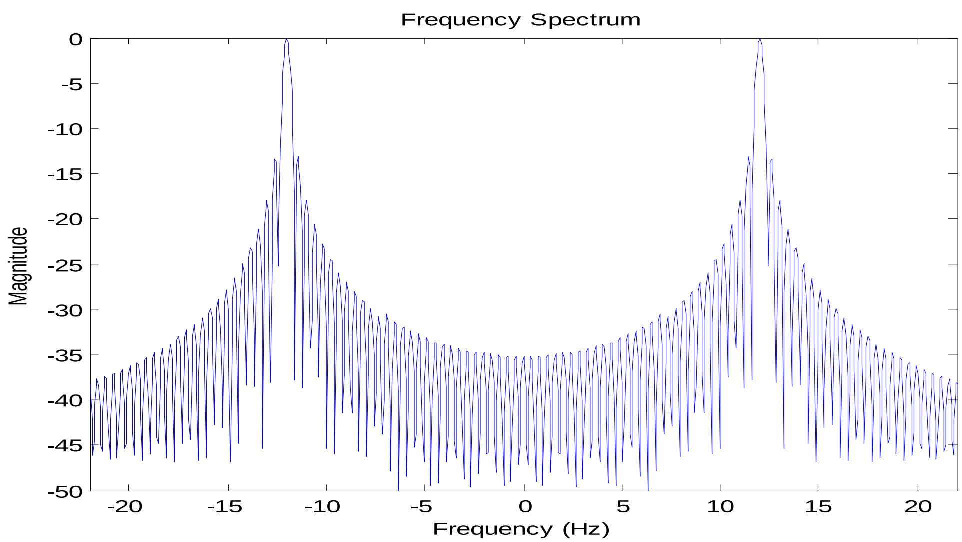


Figure 4.5 Frequency Spectrum of resampled signal by factor 3/5

The filter is designed in way that it achieves 30 dB attenuation in stopband so as expected the output distortion in resampled signal is 30 dB below the signal level.

4.3. Proposed Multistage Implementation of Sampling Rate Converter

Filter order for sampling rate conversion depends upon transition width, which depends upon the values of interpolation, decimation factor and sampling frequency. For higher values of Interpolation/Decimation factor the filter required is of very higher order, which is impractical to design. For Higher values of Interpolation/Decimation we use multistage structure in which large rational factor can be divided into several stages to reduce the overall filter order and computations. In multistage cascade structure, we perform Interpolation and decimation in multiple stages, i.e. $(L,M) = \prod_{i=1}^{S}(Li, Mi)$ where S is the number of stages. The multistage structure of rational sample rate converter can be drawn as;

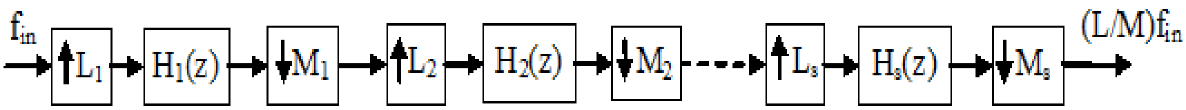


Figure 4.6. Multistage implementation of Rationam Sample Rate converter.

In each stage filter is interpolated by *Li* passed through filter and down-sampled by *Mi*. Filter order required in each stage is of low order.

The generalized method can be defined to find optimum multistage cascaded structure for sampling rate conversion. The different cascaded structures of sample rate conversion can be taken and optimum structure can be found in terms of multiplications per second(MPS) and order of filter required. Total order of filter (*N*) can be calculated as summation of order at each stage(N_i) defined by equation(4.14).

$$N = \sum_{i=1}^{S} N_i \tag{4.14}$$

For rational sampling rate converter given by fig. 4.4, the stop band frequency f_{st}, transition width Δf and filter order N of the filter required at each stage can be calculated by equations (4.15), (4.16) and (4.17) respectively.

$$f_{st} = \frac{LF_s}{2M} \tag{4.15}$$

$$\Delta f = \frac{f_{st} - f}{F_s} \tag{4.16}$$

Filter order, *N-1* of equiripple filter type with pass band ripple δ_p and stop band attenuation δ_s is given by Kaiser's formula;

$$N - 1 = \left\lceil \frac{K(\delta_p, \delta_s)}{\Delta f} \right\rceil \tag{4.17}$$

$$K(\delta_p, \delta_s) = \frac{-20\log_{10}\sqrt{\delta_p \delta_s} - 13}{14.6} \tag{4.18}$$

Multiplications Per Second(MPS) at each stage can be calculated by multiplying sampling rate by filter order at each stage. If M_i is MPS at each stage defined as $M_i = N_i \times F_{si}$, then total MPS denoted as M is summation of M_i at each stage given by relation

$$M = \sum_{i=1}^{4} M_i \tag{4.19}$$

Based on the Multiplications per second and filter order an optimum structure can be chosen from different structures defined by design example shown in next chapter.

CHAPTER 5

RESULTS AND DISCUSSIONS

In this chapter comparison of different implementations i.e. direct implementation, poly-phase implementation, coefficient symmetry implementation and Lth band filter implementation, has been done based on the computational complexity. The implementation, for which computational complexity is low for a given order, is considered to be the most efficient structure for sampling rate conversion. Design of multistage implementation of the sample rate conversion is also discussed to reduce the filter order which further reduces the computations.

5.1. Computational Complexity

The computational complexity of a filter in multi rate system can be found by two properties: the total number of multipliers and the sampling frequency at which each of the multiplier operates. The complexity is equivalent to number of multiplications per second or multiplication per unit output. Multiplications per second depend upon the filter order and filter sampling frequency while multiplications per unit output depend only on the filter order and not on the sampling frequency. We will first calculate complexity in terms of multiplications per unit time for different implementations and for multistage implementation complexity will be calculated in terms of multiplications per second.

5.2. Computational Complexity for Different Implementations

Computational complexity for different implementations can be compared by calculating number of multiplications per unit output and then by plotting curve between number filter order and number of multiplications. The implementation for which the slope of curve of filter order vs. complexity is lower is considered to be efficient structure.

5.2.1 Direct Implementation

Direct implementation refers to implementation shown by figures 3.1 and 3.2 in previous chapter. For the filter of order N the number of multiplications(Additions) per unit output is denoted by Mdir(Adir) and given by (5.1) .

$$\text{Mdir} = N+1 \text{ , Adir} = N \tag{5.1}$$

5.2.2 Poly-phase Implementation

The poly-phase implementation described in section 3.2 of previous chapter 3 shows that how filter operations can be moved to lower sampling rate. Multiplications per output samples can be decreased by moving a filter to lower sample rate by poly-phase implementation of filter. When a filter is interpolated by factor L and passed through filter then after applying poly-phase implementation the number of multiplications and Additions per output sample denoted by Mpoly and Apoly respectively, is given by (5.2) .

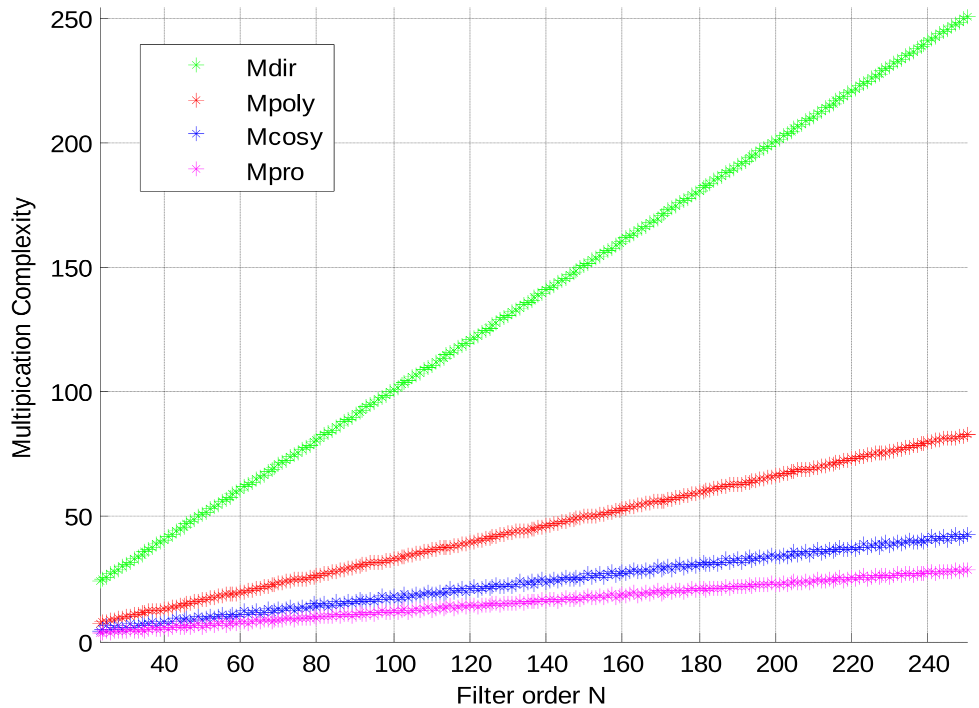
$$\text{Mpoly} = \frac{N+1}{L} \text{ , Apoly} = \text{Mpoly-1} \tag{5.2}$$

5.2.3 Implementation using Coefficient Symmetry

In this implementation described by section 3.4 of previous chapter the multiplication complexity can be reduced nearly half of the poly-phase implementation. In this implementation input-output relation is given by matrix multiplication and Centro symmetry property on matrix is applied on transfer matrix **H** defined by (3.22). The multiplication complexity is denoted by Mcosy and is defined by equ. 3.32. Multiplication complexity Mcosy versus filter order N curve is given in fig. 5.1. The Addition complexity defined by equ. 3.35 for this structure is more than polyphase structure for lower filter orders but for high orders complexity decreases as shown in fig. 5.2.

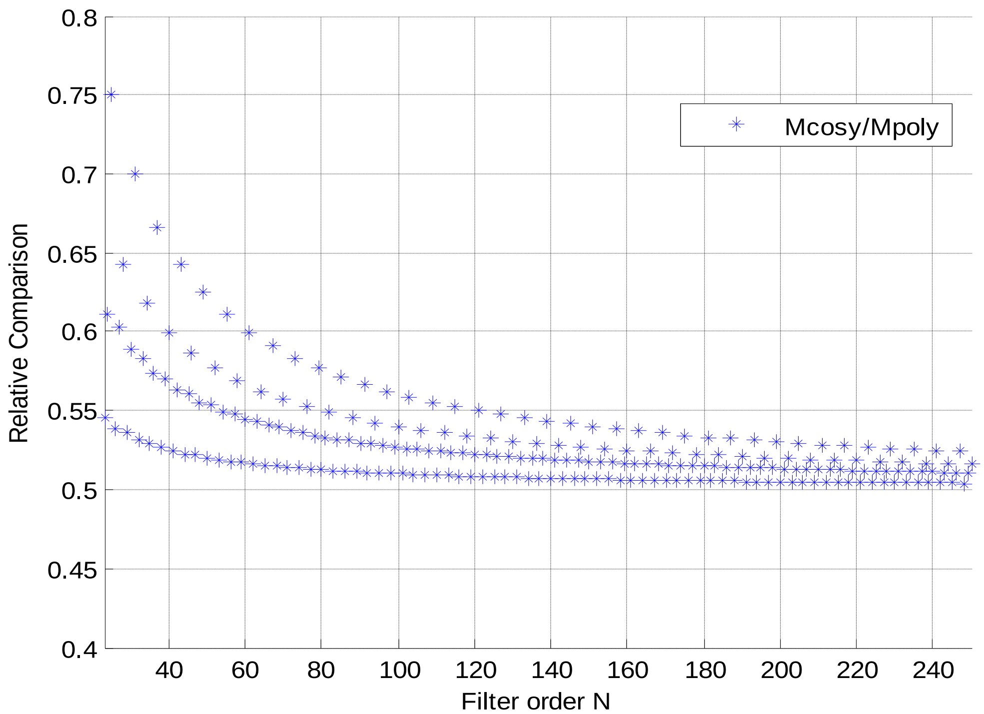
5.2.4. Proposed Implementation using Lth Band Filter

In Lth band filter since in the filter impulse response every Lth value is zero as well as filter coefficients are symmetric. Poly-phase and filter coefficient symmetry is applied on Lth band filter to reduce the slope of complexity vs. filter order curve. Since every Lth coefficient is zero so in this implementation only $2\left\lfloor\frac{N-1}{L}\right\rfloor$ coefficients are non zero. Multiplication complexity (Mpro) and Adddition Nomplexity (Apro)is shown in figs. 5.1 and 5.2. It is clearly seen in figure that complexity of Lth band filter is least of all the implementations.



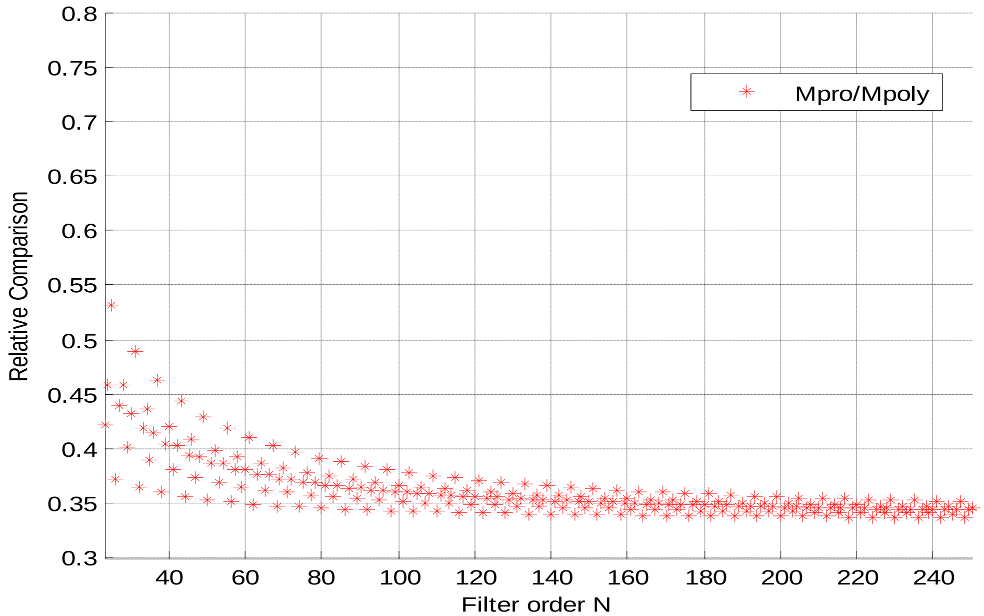
Mdir
Mpoly
Mcosy
Mpro
Multipication Complexity
Filter order N
250
200
150
100
50
0
40
60
80
100
120
140
160
180
200
220
240

(a)

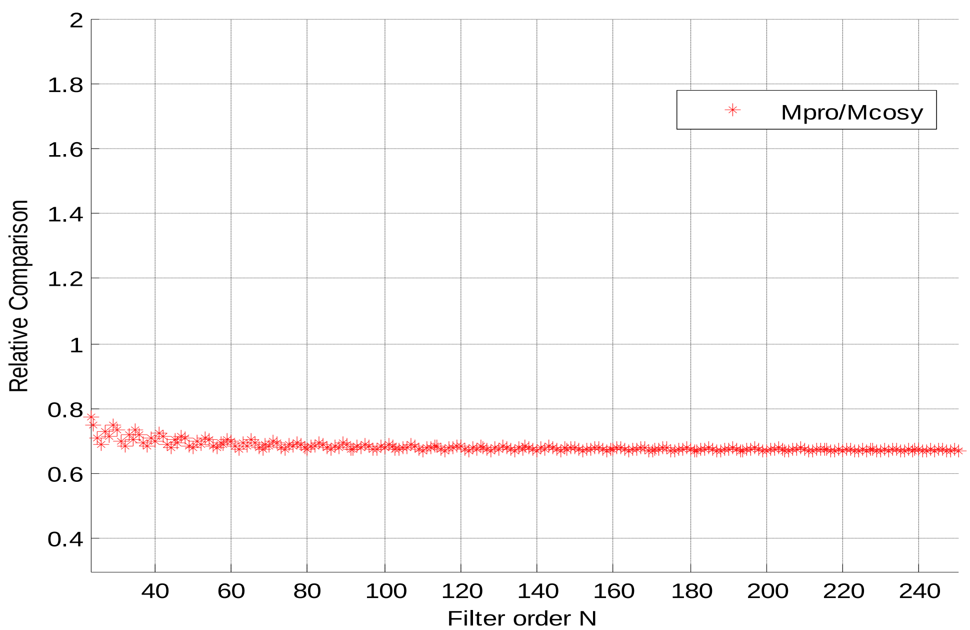


Mcosy/Mpoly
Relative Comparison
Filter order N
0.8
0.75
0.7
0.65
0.6
0.55
0.5
0.45
0.4
40
60
80
100
120
140
160
180
200
220
240

(b)



(c)

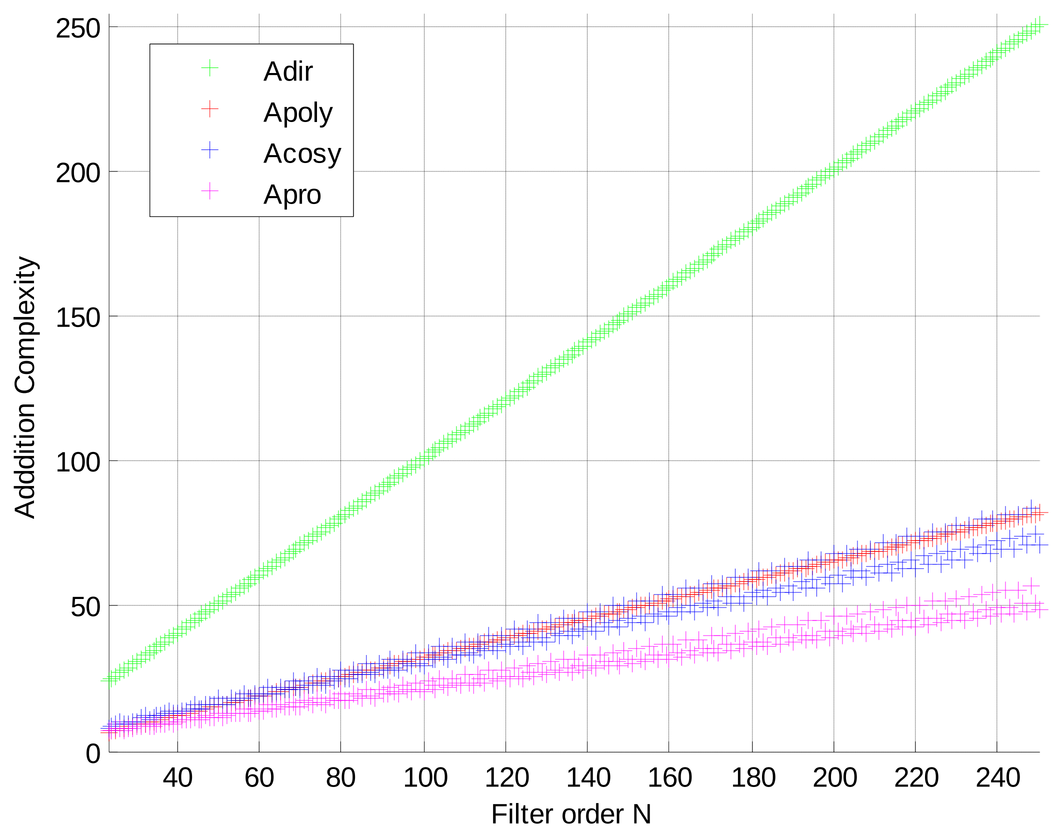


(d)

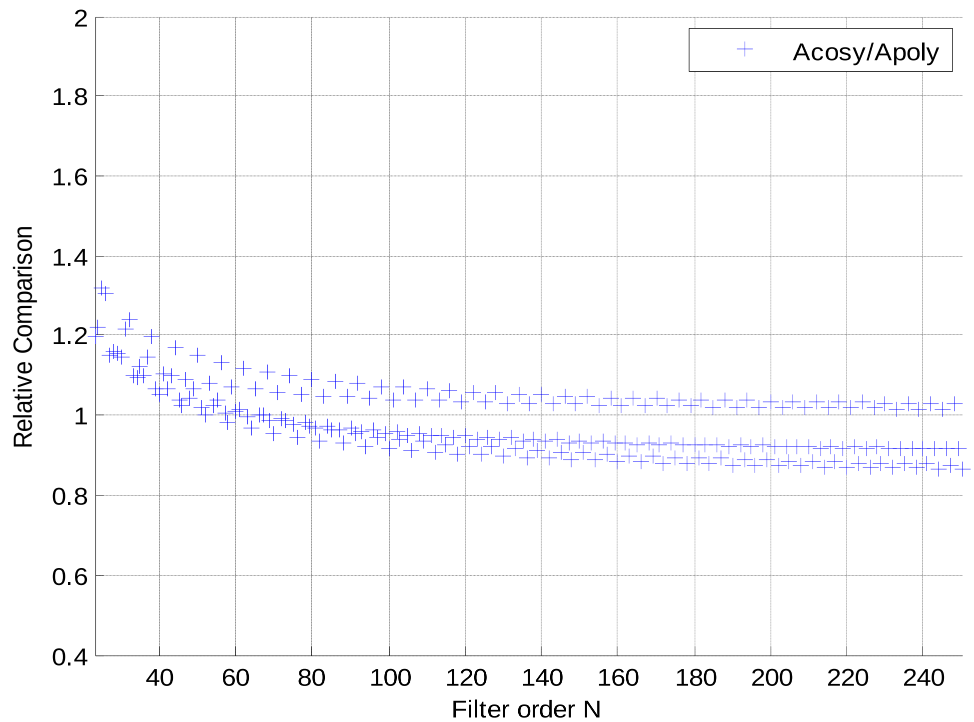
Figure 5.1. Multiplications complexity comparison of different structures for rational sampling rate conversion by factor 3/5. Mdir, Mpoly, Mcosy and Mpro stands for direct, poly-phase, coefficient symmetric and proposed Multiplication implementation respectively. (a) Multiplication complexity (b) relative comparison of poly-phase and coefficient symmetry structure (c) Relative comparison for poly-phase and proposed implementation (d) Relative comparison of proposed and coefficient symmetric structure

Table 5.1 Multiplication Complexity comparison of different structures for rational sample rate converter by factor 3/5

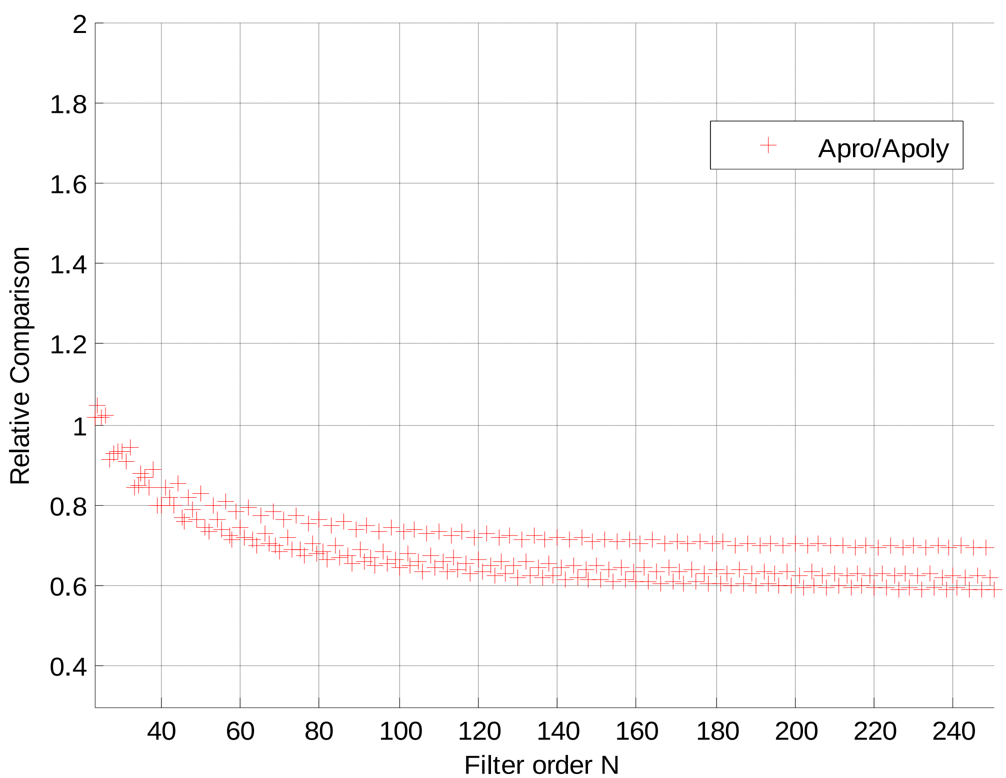
Filter Order N	Mpoly	Mcosy	Mpro	Relative Comparison		
				Mcosy/Mpoly	Mpro/Mpoly	Mpro/Mcosy
25	8.66	6	4.25	0.692	0.49	0.71
35	12	6	4.42	0.50	0.368	0.74
97	32.6	18	12.20	0.552	0.374	0.68
125	42	21	14.40	0.5	0.343	0.69
191	64	32	21.22	0.5	0.331	0.66
237	79.3	40.22	26.93	0.5071	0.339	0.67



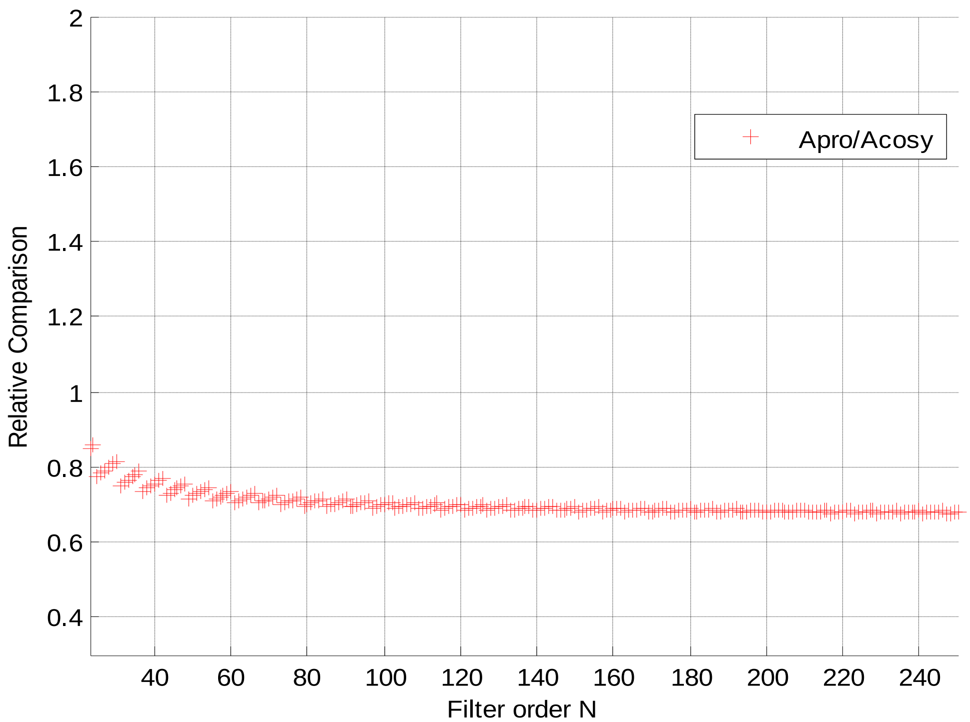
(a)


Acosy/Apoly
Relative Comparison
Filter order N
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
40
60
80
100
120
140
160
180
200
220
240

(b)


Apro/Apoly
Relative Comparison
Filter order N
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
40
60
80
100
120
140
160
180
200
220
240

(c)



(d)

Figure 5.2. Additions complexity comparison of different structures for rational sampling rate conversion by factor 3/5. Adir, Apoly, Acosy and Apro stands for direct, poly-phase, coefficient symmetric and proposed Addition complexity respectively. (a) Addition complexity (b) relative comparison of poly-phase and coefficient symmetry structure (c) Relative comparison for poly-phase and proposed implementation (d) Relative comparison of proposed and coefficient symmetry property structure.

Table 5.2. Addition Complexity comparison of different structures for rational sample rate converter by factor 3/5

Filter Order N	Apoly	Acosy	Apro	Relative Comparison		
				Acosy/Apoly	Apro/Apoly	Apro/Acosy
25	7.33	9.66	7.47	1.31	1.01	0.77
35	10.66	12	9.37	1.13	0.88	0.78
97	31.33	29.66	20.51	0.95	0.65	0.69
125	40.66	42	29.26	1.03	0.72	0.70
191	62.66	64	43.91	1.02	0.70	0.69
237	78	71.44	48.55	0.92	0.62	0.68

5.3. Design example of Multistage Structure for DVD to CD conversion

Understanding of multistage structure is easy by taking an example of DVD to CD conversion in which we use Interpolation factor L=147 and Decimation factor M=320 to convert sampling frequency from 96 kHz to 44.1 kHz. For these values of L and M the filter transition width required is very small which require filter of very high order.

We can make different stages by dividing interpolation and decimation stages as $L=3\times7\times7$ and $M=2^6\times5$. In each stage filter is interpolated by L_i passed through filter and down-sampled by M_i. Filter order required in each stage is of low order.

The proposed multistage structure for sample rate conversion is **3:1, 7:20, 7:16** . Sampling frequencies at different stages is shown in fig. 5.3 below.

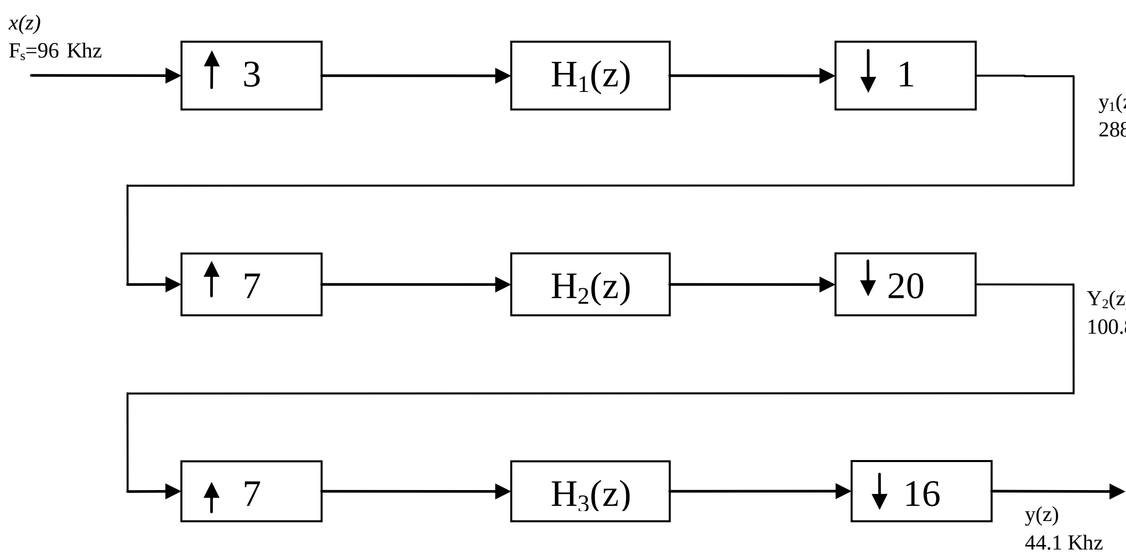


Figure 5.3. Optimum multistage structure for DVD to CD rate Converter.

We can calculate the order of filter at each stage by using the relations (4.14), (4.15) and (4.16). The details of the behavior of first stage of RSC are shown in fig. 5.4 below, in which signal shown in 5.4(a) with sampling frequency 96 KHz is interpolated by factor 3 , which produces the image frequencies at 96 KHz and 192 KHz shown in 5.4(b). Magnitude response of the filter with pass band edge at 20 KHz and stop band edge at 73.95 KHz figure 5.4(c) removes the image components.

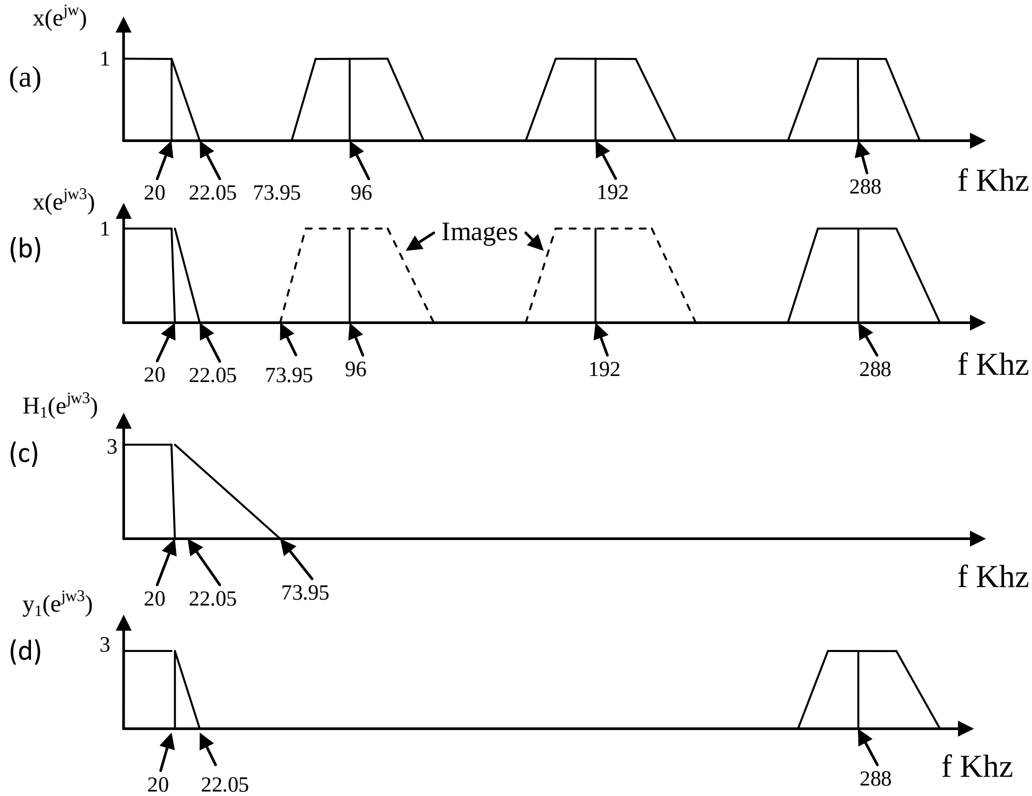


Figure 5.4. Magnitude response of first stage of optimum DVD to CD rate converter.

For first stage i.e. L=3 and M=1 the filter order required is given by

$$N_1 = 18 \tag{5.3}$$

For second stage i.e *L*=7 and *M*=20 the sampling frequency is 705.6kHz and filter order is calculated as

$$N_2 = 27 \tag{5.4}$$

Similarly at stage third N_3 is calculated as

$$N_3 = 39 \tag{5.5}$$

The total order *N* of the configuration is given by

$$N = \sum_{i=1}^{4} N_i = 84 \tag{5.6}$$

We can take advantage of polyphase filter structure at each stage given by 5.5 below.

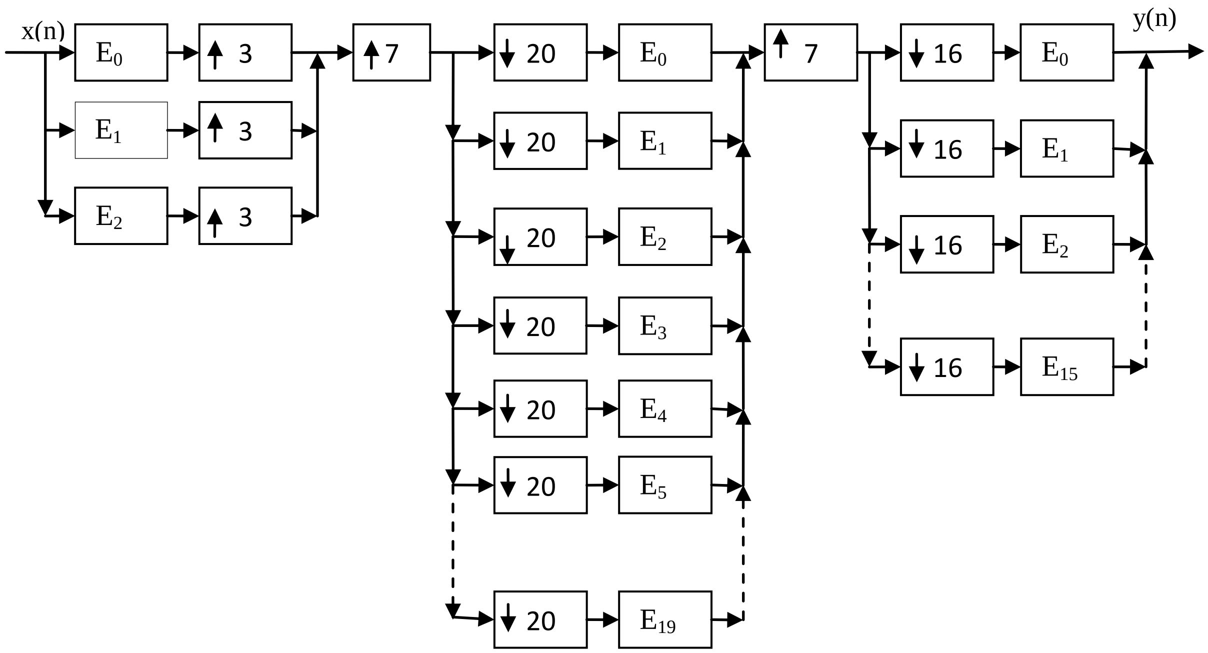


Figure 5.5. proposed optimum multistage structure for DVD to CD rate conversion.

Multiplications Per Second(MPS) at each stage can be calculated as

$$M = \sum_{i=1}^{4} M_i = (18\times 96) + (27\times 100.8) + (39\times 44.1) \approx 6170 \qquad (5.7)$$

A Table 5.3 shows the comparison of multiplications per second (MPS) between different Cascaded implementations by using poly-phase implementation.

Table 5.3. Comparison of common configurations for different cascaded structures for sampling rate conversion from DVD to CD(96 KHz to 44.1 KHz)

Configuration	**Total filter order(N)**	**MPS**
147:320	838	36913
7:8 7:5 3:8	100	7801
7:8 3:4 7:10	127	7574
3:1 7:1 7:320	68	10518
3:2 7:1 7:160	73	7298
3:1 7:10 7:32	74	8450
3:1 7:20 7:16	84	6170
3:1 7:32 7:10	113	6427

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1. Conclusion

Sample rate conversion system can change the sampling frequency of input signal and make it suitable for the digital system. It makes possible those digital systems to communicate, which has different sampling rate. Interpolation means use mathematical way to predict the unknown samples between the existing samples. Anti-imaging filters are used to remove the image signals created due to the effect of interpolation in frequency domain. Anti-aliasing filters are used to avoid the aliasing effect due to decrease in sampling frequency in case of decimation process. In rational sample rate conversion process in which filter is used in between interpolator and decimator acts as anti-imaging as well as anti-aliasing filter.

In most of the cases FIR filters are used in implementation of rational sampling rate conversion system because phase response of FIR filters is linear in nature and results in no phase distortion of output signal. Minimum phase distortion is desired for signals for which time envelope of signal is to be preserved. Moreover, FIR filters contain no feedbacks which are easy to design.

There are several implementations of FIR filters for efficiently design of sample rate converter. The computational complexity of implementation can be found number of multiplications per second or multiplications per output. For direct implementation of FIR filter of order N, the number of multiplications per output is N+1. FIR filters in sample rate converter can be decomposed into its poly-phase filter components and can be moved to lower sampling rate using some noble identities. When filter is applied after interpolation by factor L, then decomposition of filter into L poly-phase filters and moving to lower sampling side results in reduction of multiplication complexity by factor L. FIR filters exhibit coefficient symmetry property, using this property in rational sample rate converter input-output relation can be written in matrix multiplication form and by using this property multiplication complexity can be decreased by factor of 2L compared to direct implementation.

Rational sample rate converter can also be implemented using Lth band filter for which from center coefficient of impulse response, every Lth coefficient is zero. By efficiently implementation of Lth band filter using coefficient symmetry property, the multiplication complexity can be reduced below the factor of 2L.

For larger values of interpolation and decimation, the filter requirements(number of delays, number of multipliers and number of required bits) becomes very high. Designing of filter for these type of sample rate converter becomes impractical in nature. For this type of SRC the conversion process is decomposed into several stages. Due to this multistage structure filter order requirement reduces which in turn reduces the multiplications per second. Using the implementations defined sample rate conversion system with smallest computational complexity can be attained.

6.2. Future Scope

A simple Sampling Rate Conversion technique is over/under sampling and band-limiting the signal, but this requires a high order anti-imaging/anti-aliasing filters to attenuate the image components caused by over/under sampling. Future work in SRC includes:

- In sampling rate conversion system computational complexity can further be reduced by many other efficient implementations e.g. Farrow filtering Structures.
- Efficient implementation using Lth band can be applied at each stage of multistage structure defined in thesis to further reduce the computational complexity.
- The implementations proposed in this work can be combined with work defined in [37] for design of multiplier-less sample rate converter.

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List of Publications

1. J. Singh and S. Sharma, "A Novel Architecture for Fractional Sample Rate conversion using FIR Filters," Communicated for publication to *Elsevier Digital Signal Processing, 2015.*