LEVERAGING AI-DRIVEN APPROACH FOR INNOVATING IO CHARACTERIZATION

A Thesis submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in

VLSI DESIGN

Submitted By

Prashant Kumar Chauhan

602362025

Under Supervision of

Dr. Harpreet Vohra

Associate Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR INSTITIUTE OF ENGINEERING & TECHNOLOGY

(A DEEMED TO BE UNIVERSITY), PATIALA, PUNJAB

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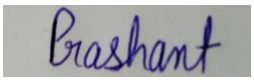
DECLARATION

I, **Prashant Kumar Chauhan** hereby declare that the Seminar Research report entitled is "**LEVERAGING AI-DRIVEN APPROACH FOR INNOVATING IO CHARACTERIZATION**" in partial fulfilment of the requirement of the award of the degree of **Master of Technology(VLSI Design)** submitted at **Electronics and Communication Engineering Department**, Thapar Institute of Engineering & Technology(Deemed to be university),Patiala is a record of work carried out under supervision of **Dr. Harpreet Vohra (Associate Professor, Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology(Deemed to be University)** from **JULY 2024** TO **JUNE 2025**. The Matter in this has not been submitted in part to any other university or institute for the award of any other degree.



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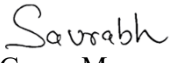
Prashant Kumar Chauhan
602362025

Saurabh Srivastava  Group Manager (ST Microelectronics) Date:25/06/2025	Dr. Harpreet Vohra Associate Professor  Department of Electronics and Communication Engineering, Thapar Institute of Engineering & Technology, Patiala Date: 25/06/2025

CERTIFICATE

life.augmented
STMicroelectronics Private Ltd.
Plot No.1, Knowledge Park-III,
Greater Noida – 201 308.
Uttar Pradesh, India
Tel : +91-120-4003000
Fax :+91-120-4003007
Email : infostm.india@st.com
CIN : U32109DL1990FTC039906
www.st.com

June 27, 2025

TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Prashant CHAUHAN** has undergone internship in our **TRD** Group from **July 03, 2024 to June 27, 2025** and has successfully completed the project on: **Leveraging AI-Driven Approach for Innovating Io Characterization**

During the internship period, Prashant was found to be sincere and professional in conduct.

We wish him all the best for the future endeavors.

for **STMicroelectronics Pvt. Ltd.**

Sanjay Kumar PIPLANI
India Talent Acquisition Head

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I will be ignorant if I do not express my gratitude to the author of the references and other literature cited in this Thesis. Finally, I want to thank all my colleagues for their encouragement through potential discussions and suggestions.

ABSTRACT

Standard cell modelling requires library characterization as an essential design procedure which generates precise and dependable models that detail their timing performance in addition to their power consumption and other functional parameters. System-on-Chip (SoC) implementation requires this process to make sure digital chip designs achieve specified performance power area (PPA) targets successfully. The characterization technique operated by Siemens' Kronos depends on Eldo analog simulations, but this method leads to long development cycles and high computational resource utilization. The established techniques experience reduced accuracy effectiveness when used for multiple electrical specifications while the industry moves towards manufacturing denser designs.

Siemens introduced Solido Characterization Suite through advanced machine learning-based algorithms to optimize characterization processes. The innovative suite decreases the requirement for large-scale simulations to cut down on computational expenses and reduce characterization periods. The Solido Generator stands among the principal elements of the suite by quickly analysing design characteristics across selected Process, Voltage and Temperature (PVT) regions to establish new PVT data points with high precision.

The report analyses problems with conventional library characterization approaches then describes how Solido Characterization Suite offers advanced solutions to these issues. The report uses detailed examinations and specific case examples to show how machine learning transforms characterization processing into a quick and correct method of library development. The Solido Characterization Suite emerges as a fundamental tool in present-day semiconductor design because it shows great potential for enhancing design efficiency together with reliability improvements.

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CHAPTER 1

Introduction

This chapter introduces the fundamental concepts of modern semiconductor design, focusing on "CAD (Computer-Aided Design) View Generation" and "Library Characterization". CAD views, such as schematic, layout, netlist, and electrical views, are essential for designing, verifying, and manufacturing Integrated Circuits (ICs), ensuring accuracy, reducing errors, and streamlining workflows. The chapter highlights the importance of "Intellectual Property (IP)", pre-designed components that accelerate chip development, with types including soft, firm, and hard IPs. It also emphasizes the critical role of "I/O (Input/Output) circuits", which serve as interfaces between a chip's internal circuitry and external devices, ensuring signal conditioning, protection, and overall performance. The chapter delves into "Library Characterization", a process that simulates standard cells under various Process, Voltage, and Temperature (PVT) conditions to determine timing, power, and noise parameters, which are vital for optimizing performance, power, and area (PPA) in chip design. Additionally, it outlines the benefits of library characterization, such as improved efficiency and reliability, while acknowledging the challenges of traditional methods. This sets the stage for exploring advanced machine learning-based solutions in subsequent chapters, providing a strong foundation for the innovative approaches discussed in the thesis.

1.1 Role of CAD views in VLSI

CAD views are used across the VLSI domain at every step. The various levels of abstraction provided help the users to relate to the circuit level information and grasp the contents required in an efficient manner as shown in Figure 1.1. CAD also helps organizing the data systematically to enable interoperability among global development and research teams[1].

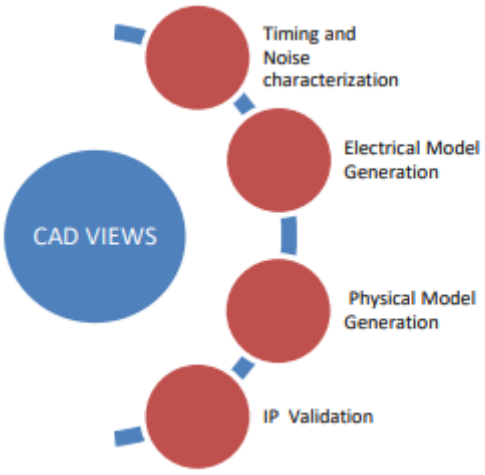


Fig.1.1: Role of CAD views in VLSI[1]

1.2 CAD View Generation & Classification

It is the Process of generating all required EDA views for a given Design/Tools & Flow to enable targeted SOC's e.g, liberty file, LEF, FRAM etc.

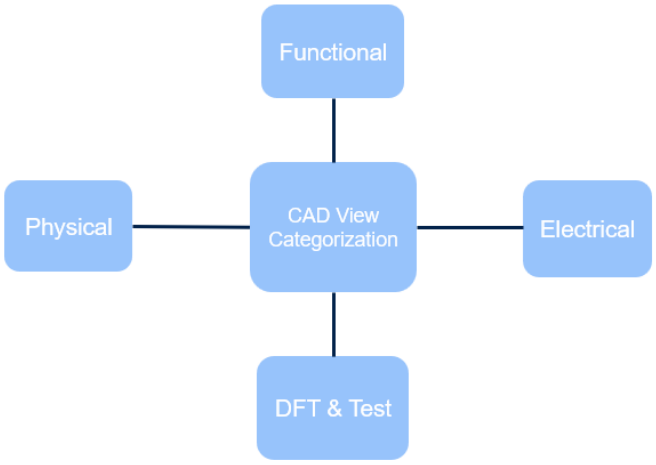


Fig:1.2: CAD View Categorization

1.2.1 Definition and Purpose

A design problem requires different views or representations through the CAD View Generation process. Different views hold vital importance throughout the electronic design process at its design phase along with verification and simulation as well as manufacturing steps. Design accuracy stands as the main purpose to guarantee understanding of the design as well as its analytical and production capabilities. The usage of CAD views in SoC Design Flow is Shown in Fig 1.3.

1.2.2 Types of Views

Different types of views are created throughout CAD operations with distinct functional roles:

- **Schematic View**: This representation shows the circuit based on high-level components through symbols connected with lines. The design team utilizes this view for the first design steps as well as confirmation processes.
- **Layout View**: This display shows the actual placement of components together with wire routing on integrated circuits and printed circuit boards. The manufacturing process together with physical form development requires this information.
- **Netlist View**: Lists all the components and their interconnections in a textual format. The netlist format supports simulation together with verification tasks.
- **Abstract View**: Entry-level designers prefer abstract design representations based on symbols to simplify complex circuits through the symbolic view.
- **Electrical View**: It Contains information about design timing features, and how power Distributed and consumed in the Design.

1.2.3 Process of CAD View Generation

Several sequential steps lead to the production of CAD views.

- **Design Entry**

  The first design occurs through CAD tool entry. The design entry process can happen through schematic capture and HDL (Hardware Description Language) coding and alternative methods.

- **Synthesis**

  The high-level design undergoes synthesis for transformation into a lower-level representation which may present itself as a gate-level netlist. The abstract design gets translated into a physical form which can be realized through this step.

- **Layout Generation**

  Engineers place components into the layout view which then follows with the connection routing process. The design process at this stage requires floor planning as well as placement followed by routing to meet all necessary physical requirements.

- **Verification**

  A verification process confirms that all views demonstrate exact design representation while matching all required specifications. Verification methods, timing examination, and electrical power evaluation are part of this process.

- **Extraction**

  Parasitic extraction produces supplementary views for analyzing physical phenomena in the design operation. The views undergo verification tests after which they serve for future analysis and optimization steps.

- **Back-Annotation**

  The physical design data about timing and power gets added to higher-level views for maintaining consistency through back-annotation processes.

1.3 Why CAD view Generation Needed?

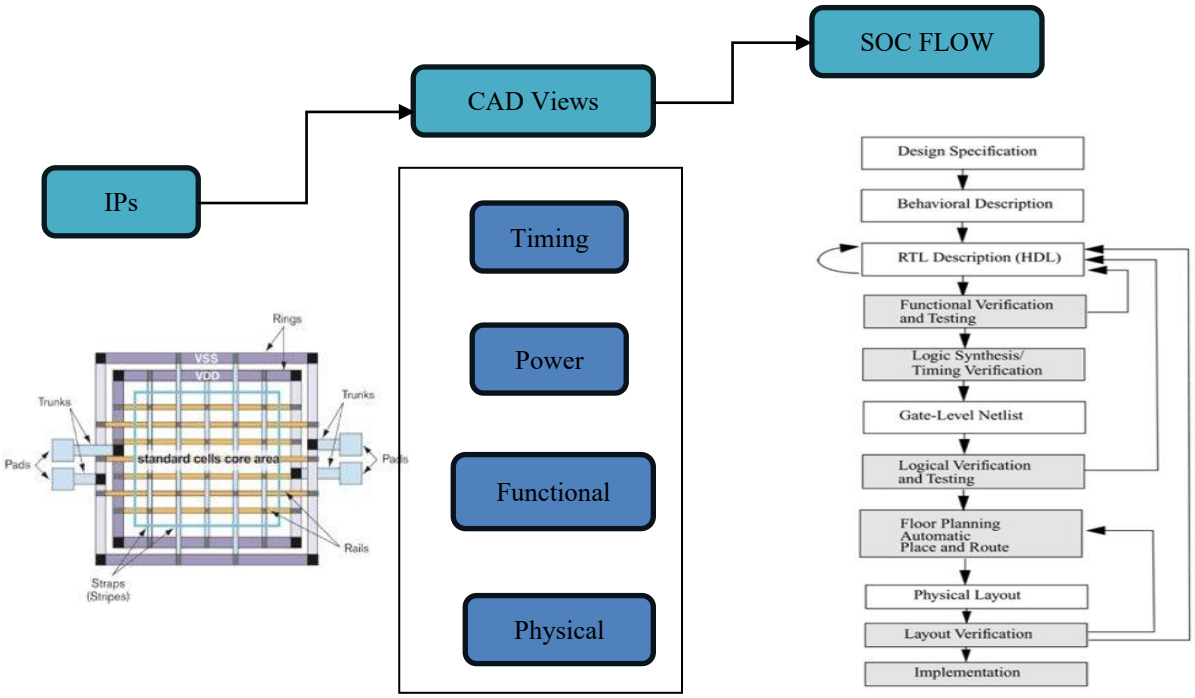


Fig.1.3: Usage of CAD view in SoC Flow

The essential nature of CAD (Computer-Aided Design) View Generation emerges in Electronic Design Automation (EDA) because of multiple reasons. Due to its importance several crucial reasons demand CAD view generation in Electronic Design Automation (EDA):

1.3.1 Design Visualization

- **Comprehensive Representation**: The collaboration generates complete design presentations which help engineers obtain a multi-tiered visualization of their designs.
- **Simplification**: The process simplifies complex designs through multiple view perspectives resulting in simpler components that support better analysis for individual areas of design understanding.

1.3.2 Verification and Validation

- **Functional Verification**: Verification of logical design functions occurs through schematic along with netlist views which confirm that design specifications are fulfilled.
- **Physical Verification**: The layout views serve to verify actual elements including component locations together with wires and design constraint compliance.
- **Timing Analysis**: The timing views assist verification teams to check that the design operates correctly at its designated clock speeds.
- **Power Analysis**: Implications of power usage and distribution analysis can be accessed through power views because power-sensitive designs need this capability.

1.3.3 Simulation and Testing

- **Behavioral Simulation**: Behavioral Simulation uses netlist and symbolic views to perform design behavior tests while engineers undertake pre-fabrication design debugging by means of these perspectives.
- **Post-Layout Simulation**: The physical attributes together with parasitic effects can be examined with Layout views for post-layout simulation which ensures correct system operation in real-world conditions.

1.3.4 Optimization

- **Performance Optimization**: The optimization of performance metrics including speed and power consumption and area receives support from different views.
- **Design Space Exploration**: Through different views engineers gain the ability to perform design space exploration for trade-off assessment that results in higher optimized designs.

1.3.5 Manufacturing Preparation

- **Fabrication Readiness**: Layout views provide both fabrication readiness and ensure the design will become manufacturable with precision.
- **DRC and LVS Checks**: The combination of Design Rule Checking (DRC) with Layout Versus Schematic (LVS) evaluates the layout view along with the schematic view to validate manufacturing rules and functional accuracy.

1.3.6 Documentation and Communication

- **Design Documentation**: Several design views function as a complete documentation system that provides essential details for design maintenance service and system revisions.
- **Team Collaboration**: Multiple views allow engineers to work together effectively because different members can concentrate on separate aspects of the design (logic design and physical design and verification).

1.3.7 Error Detection and Correction

- **Early Detection**: Design view generation and analysis enables quick identification of errors and problems which helps prevent costly later-stage mistakes throughout the design development.
- **Iterative Refinement**: Design refinement occurs through repeated improvement rounds that use different view generations for the purpose of detecting and resolving problems quickly.

1.3.8 Cost and Time Efficiency

- **Reduced Rework**: The verification process with various views decreases design rework and thus minimizes both time expenditures and financial expenses.

- **Streamlined Workflow**: The CAD view generation mechanism simplifies workflow procedures to deliver faster time-to-market while also boosting whole process efficiency.

1.4 What is IP?

"IP" stands for Intellectual Property. Pre-designed and pre-verified components and blocks belong to IP in VLSI and permit use during the development of integrated circuits (ICs). IP blocks play an indispensable role by speeding up design processes while decreasing expenses and providing dependable outcomes for intricate chip designs.

1.5 Types of IP in VLSI

There are several types of IP blocks used in VLSI design, each serving different purposes and offering varying levels of flexibility and integration. Here are the main types:

1.5.1 Soft IP

Soft IP cores are provided as synthesizable HDL (Hardware Description Language) code that uses either VHDL or Verilog. These cores provide extensive flexibility because they let designers optimize and adapt the IP cores specifically to match their different target technologies and applications. Soft IP serves as a common element during digital logic design along with usage in processor development and custom logic block creation. Integrating with HDL code allows designers to customize and optimize this CPU core for diverse performance and area specifications.

1.5.2 Firm IP

A firm IP core provides netlists to customers which represent the design after synthesis and before physical implementation. The cores deliver some level of design customization through flexibility while staying close to actual hardware build. The netlist delivery defines firm IP cores as an interface between soft IP flexibility and hard IP predictability for custom designs. A netlist representing the memory controller exists for integration in multiple projects with certain design modifications.

1.5.3 Hard IP

Such cores arrive as prepared physical layouts specifically designed to function with manufacturing process and technology nodes. The delivery approach provides minimum flexibility yet delivers the most predictable results for performance along with area and power consumption. High-speed interfaces analog blocks standard cells and critical elements receive this design because performance along with reliability require its application. The production of specific fabrication process requires a pre-designed and optimized PLL (Phase-Locked Loop) block.

1.6 What are IO's?

VLSI contains specially designed IO elements which interface integrated circuit core signals to external devices. External communication is managed through these elements between the internal circuitry of the chip and other external devices or systems. The functions that I/O blocks execute include voltage level translation together with signal buffering and electrostatic discharge (ESD) protection. The correct transmission and reception of signals by these blocks allows integrated circuit interfaces to work smoothly with system components including sensors and actuators as well as communication interfaces.

1.7 Why do IO's need special attention? Why are they important?

IO (Input/Output) elements in a chip play a crucial role in ensuring the proper functioning and protection of the core circuitry. Here's a simplified explanation of their importance:

1.7.1 Responsibilities of IO Elements:

- **Signal Checking**: The core's requirements determine the checks that I/O elements perform during signal inspection against external devices. When a signal seems dangerous to core safety the I/O channels either transform it or simply discard it.
- **Signal Conditioning**: External signals undergo signal conditions during their transition from core outputs to external environment to confirm compliance with safe operational specifications.
- **Protection**: The core remains protected from signal-induced destruction that originates from improper inputs with wrong voltages or noisy signals through I/O elements. Since IO's are placed at Periphery of Chip as Shown in fig 1.2.
- **Performance Impact**: The complete chip efficiency depends directly on the operational performance of its I/O elements. Core operation will suffer even when the design is well-executed because of inadequate I/O performance.
- **Practical Testing**: The designer needs to perform extensive real-world testing of I/O elements to verify their operational strength and delay parameters and power consumption levels. Testing such circuits helps maintain correct operation and reliability of the chip.

The survival and dependability of the chip rely on I/O elements. These components protect the core structure and maintain signal stability while ensuring signals entering or leaving remain inside secure and predefined degrees. The successful operation of I/O elements requires proper design combined with thorough testing because this prevents harm to internal components and external components connected to them.

1.8 Types of IO's

1.8.1 Input IO Cells

The device functions to acquire external signals then moves them for internal processing.

Input Buffer Amplifies incoming signals and Shields against electrostatic discharge.

1.8.2 Output I/O Cells

The function of an output I/O cell exists to deliver internal logic signals which control external equipment. Output Buffer sends signals to appropriate voltage levels.

1.8.3 Bidirectional I/O Cells

The cells execute as both input and output components which function through control signals. Tri-State Buffer Disables output in input mode. A control logic module facilitates the change between input and output states.

Such implementation example exists within the data bus line which operates as both sender and receiver through control signals. The I/O cells establish proper links for the internal units to communicate with external devices. The VLSI functionality depends on components through their fundamental functional operation.

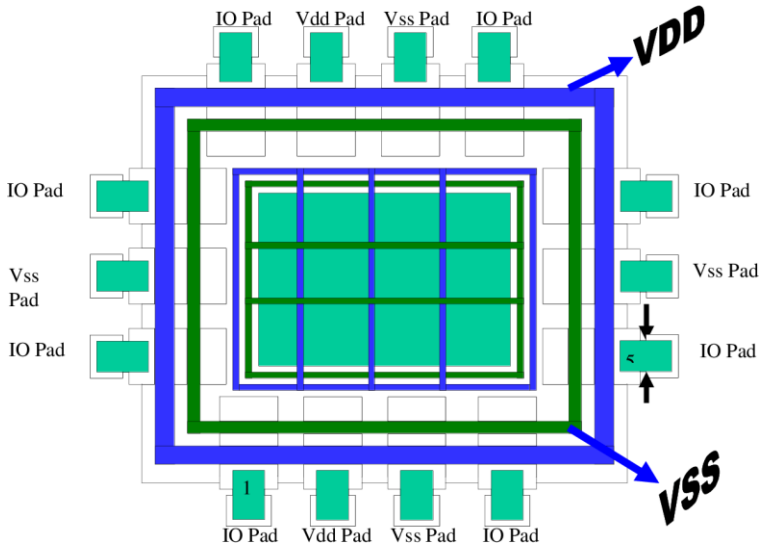


Fig.1.4: IO Pads

Source: [Power Grid Analysis In VLSI Designs | Semantic Scholar]

1.9 What is Library Characterization?

To make working electrical circuits, you need to know more than just the basic function of a cell. There are more things to think about. For example, the speed of a single cell can change the speed of the whole circuit, and the power used by a single cell can change the total power. Aside from that, the total load could change both the speed and the power. The goal of standard-cell classification is to gather this kind of data[2].

When you use analog simulators to simulate a standard cell, you can get input load, speed, and power data in a format that can be used by tools that come after. This is called library characterization. Either a unique analog simulator, whose output is used to make the characterization data, or a library characterization tool can be used to do this. Figure 1.3 shows the flow to make described data.

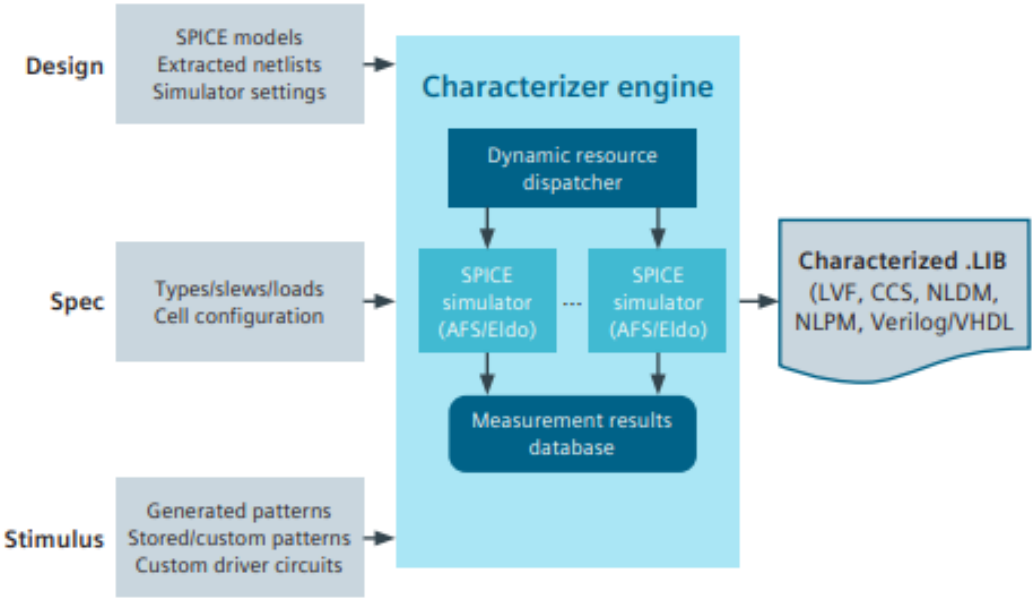


Fig.1.5: Kronos Characterization Engine

Source: [Kronos Characterizer | Siemens Software]

1.10 Library Characterization Process

Some of the views needed to describe a digital library are generally given by the design, while others need to be found. For example, "! (A & B)" could be used to describe the logic function of a NAND gate. Depending on the technology and design goals, all other views can be drawn from this equation with a few extra assumptions and limits. An method can be used to make the netlist of combinatorial cells. From the netlist, a plan will be made that can be used to find the cell's parasitic capacitances and resistances. The netlist of transistors and parasitics that you get can then be used to get a general idea of how the cell handles time, power, and noise.

To measure the time and power of a transistor, simulations are run under various conditions since factors like process variations, voltage, temperature (PVT), input signals, and output loads significantly affect its behavior. Testing under both best-case and worst-case PVT conditions helps predict the fastest and slowest performance, ensuring the design is reliable. Transistors also need to handle a wide range of input signal speeds (edge rates) and output loads, which can be represented on a two-dimensional grid. By testing at specific points on this grid and using linear approximation, the behavior between those points can be estimated efficiently and accurately.

1.11 Why is Cell Library Characterization Important?

Digital chip design relies heavily on cell library models, which are created through a process called cell library characterization. These models are essential for every step of the chip design process, from converting the design from RTL to GDSII. They are used for tasks like analysis (logic simulation, verification, timing, power, noise, etc.), implementation (synthesis, test insertion, placement, clock tree synthesis, routing), and fixing issues (engineering changes, rule fixes, etc.), as shown in Fig. 1.4.

Standard cells need to be characterized so that design tools can work with them effectively. For example, synthesis tools need information about the cell's logic function, the load it presents to connected signals, its speed under different input and output conditions, its power consumption, and its physical size. This information helps the tools convert high-level designs into optimized collections of standard cells.

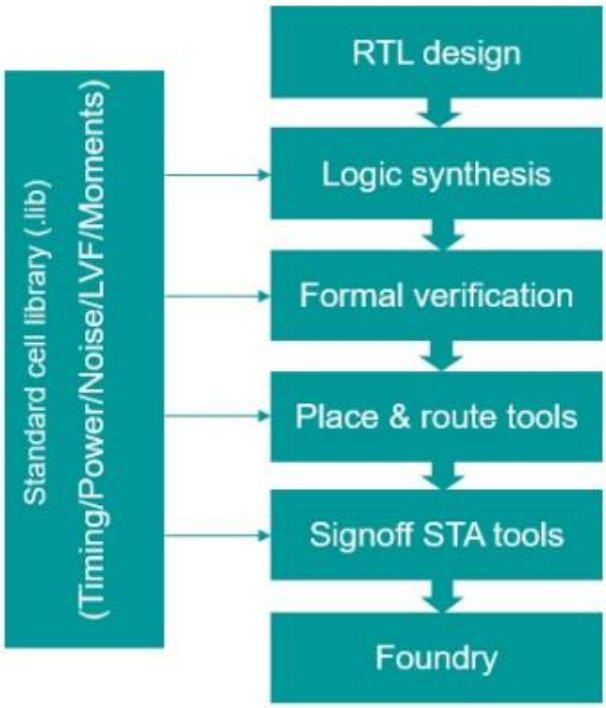


Fig.1.6: Standard cell library usage in digital design flow.

1.12 The Benefits of Library Characterization.

The characterization of electronic libraries provides essential support to reach powerful system designs within shorter periods of time. Digital logic together with memories I/O and custom IP represent major components of chip area because designs are developed through static timing analysis-based methodologies which rely on Liberty models built after library characterization.

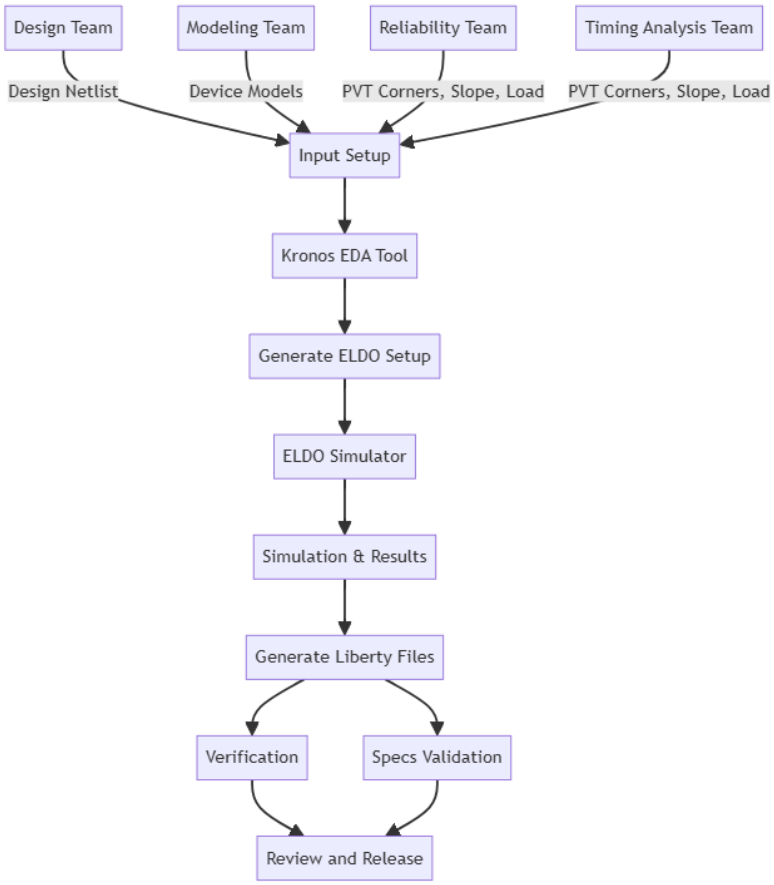


Fig.1.7: IP Characterization Flow

Library characterization development serves as a fundamental requirement for SoC design success in the dynamic semiconductor industry. The creation of liberty files that store standard cell characteristics including timing and power attributes grows more complex because of rising cell numbers and extensive Process, Voltage, and Temperature variations.

The Kronos characterization tool by Siemens needs Eldo as its simulator to conduct simulations which requires considerable simulation time and processing power. The library development process requires extensive use of time and resources until designers achieve adequate product specifications within SoC project deadlines as shown in fig.1.5.

The semiconductor industry's ongoing progress toward smaller process nodes and complex designs makes it increasingly hard to achieve precise electrical parameter measurements with conventional characterization methods. Complete characterizations of devices create additional problems that diminish traditional characterization tools' effectiveness.

The Solido Characterization Suite from Siemens uses advanced machine learning-based algorithms to tackle these limitations. This revolutionary software suite produces liberty files automatically which means users can skip complete characterization procedures and minimize their computational load. The Solido Generator functions as the core component of this suite to enable users to perform PVT characterization for design subsets which generates supplemental PVT points inside a quick timeframe while sustaining high accuracy levels.

This report examines the assessment difficulties of semiconductor design libraries together with traditional tool inadequacies before introducing advanced capabilities from Solido Characterization Suite. Detailed analytical research and case studies will investigate the benefits of machine learning technology to revolutionize characterization processes whereas this advance leads to improved efficiency and accuracy in library development.

CHAPTER 2

Literature Review

This chapter focuses on importance of IP Characterization in semiconductor designs. It highlights the advancement of characterization techniques and addresses challenges such as deep sub-micron designs, complexity, and need for accurate timing and power modelling.

Also,it explores the application of "Machine Learning (ML)" in library characterization, focusing on its ability to address the growing complexity of modern semiconductor designs. It highlights how ML techniques enhance characterization accuracy, reduce-runtime, and optimize resource utilization compared to traditional methods.

A critical aspect of library characterization in semiconductor designs and it highlights the importance of liberty files in providing accurate timing, power and noise models for EDA tools.

2.1 IP Characterization

An overview of library characterization in semi-custom design, highlighting the advancements made over the past decade and the challenges posed by deep sub-micron design and rapid process technology progression[3]. Library characterization in semi-custom design involves creating accurate abstractions of library elements (gates or cells) to predict the behavior of the design. Traditionally, characterization focused on performance (timing), but with the increasing focus on portable products, power characterization has also become important. The paper emphasizes the need for accurate characterization to enable synthesis, floorplanning, delay calculation, simulation, and place & route. Existing Characterization Flow is shown in fig 2.1

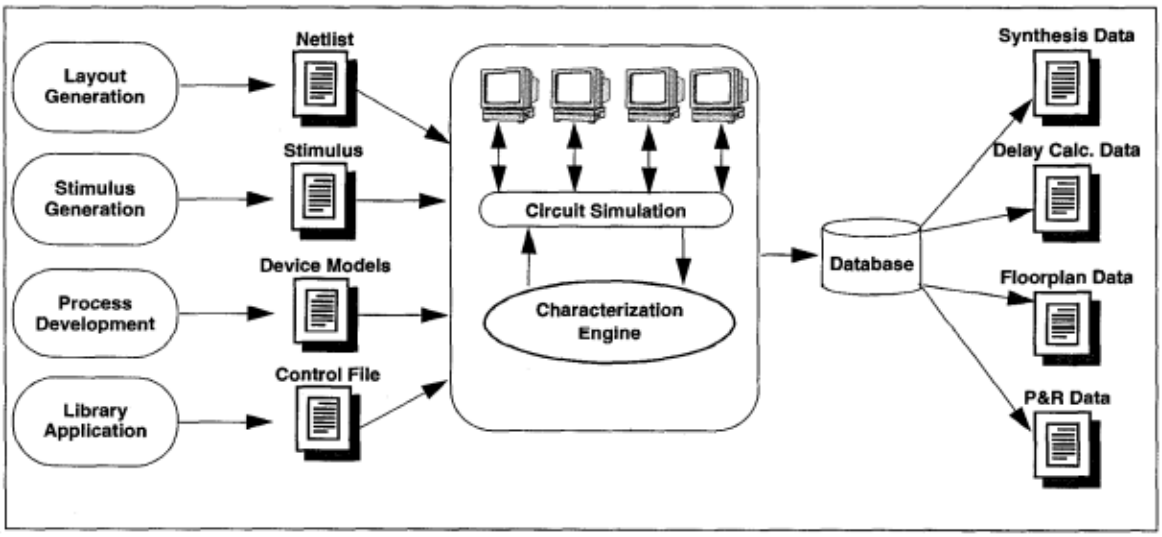


Fig.2.1: Existing Characterization Flow[3]

It focuses on designing and characterizing standard cell libraries optimized for subthreshold circuits. The increasing demand for low power consumption in digital IC design has led to the exploration of subthreshold operation[4], which offers significant power savings at the cost of performance.

Traditional standard cell libraries designed for nominal VDDs are not suitable for subthreshold circuits due to varying threshold voltages and parasitic effects.

A fast method for timing characterization of standard cell libraries using curve fitting. The proposed approach significantly reduces the CPU resources and storage required for generating large-scale liberty files. The methodology reduces the characterization time from 650 hours to less than 1 hour, with an error of less than 3% compared to traditionally characterized data[5]. Standard cell libraries are essential for digital IC design, providing predefined logic blocks with timing and power characteristics. Characterization of these libraries involves simulating each cell under various process, voltage, and temperature (PVT) conditions to ensure performance targets are met. The results are stored in liberty files, which are used by EDA tools for synthesis, simulation, and place & route. Traditional characterization methods are time-consuming and resource-intensive, prompting the need for faster and more efficient approaches.

A high-level IP-oriented power estimation methodology for System on Chip (SoC) designs. The methodology separates the activity of the IP from its implementation, enabling the creation of models that can be used with different frequencies, layouts, and implementation technologies. The proposed method achieves accurate results within 15% of RTL estimations and offers speedups of three to four orders of magnitude[6]. Power consumption is a critical factor in SoC design, and estimating it early in the design process is essential to meet time-to-market requirements. Traditional methods using Hardware Design Languages (HDLs) at the Register Transfer Level (RTL) are time-consuming due to the need for synthesis and iterative simulations. High-level models, such as those based on SystemC, offer promising alternatives but lack comprehensive frameworks for power-aware design environments.

Literature Review on IP Characterization is shown in Table Below 2.1

Table 2.1: Literature Review on IP Characterization

Aspect	**An Overview of Library Characterization in Semi-Custom Design**	**Fast Timing Characterization of Cells in Standard Cell Library Design Based on Curve Fitting**	**Design and Characterization of Standard Cell Libraries for Optimal Subthreshold Circuits**	**IP Characterization Methodology for Fast and Accurate Power Consumption Estimation at Transactional Level Model**
Focus	The paper provides an overview of advancements in library characterization for semi-custom design, addressing challenges posed by deep sub-micron design and rapid process technology progression.	The paper presents a fast method for timing characterization of standard cell libraries using curve fitting. The method aims to solve CPU resources and storage issues associated with generating large-scale liberty files.	Designing and characterizing standard cell libraries optimized for subthreshold circuits.	High-level IP-oriented power estimation methodology for SoC designs.
Results	Significant advancements in library characterization, including automation, distributed processing, and diverse modeling possibilities. Effective methods for timing and power characterization, stimulus generation, and data management.	The proposed method reduces the characterization time from 650 hours to less than one hour for a full library.The accuracy of the interpolated timing and power data is validated on a real circuit design, showing less than 3% error.	Achieves 8.53% lesser power and 17.53% lesser area (INWE) and 15.2% lesser delay (RSCE) compared to conventional libraries.	Achieves accurate results within 15% of RTL estimations, significant speedups in simulation time.
Conclusion	Library characterization has evolved from script-based systems to	The fast-timing characterization approach using	Optimized standard cell libraries show significant	Provides a fast and accurate way to estimate power

	sophisticated automated systems. Despite these advancements, new challenges such as rapid library retargeting, data management, and accounting for interconnect and high-frequency effects need to be addressed to support deep sub-micron design and rapid process technology progression.	curve fitting significantly reduces the runtime required to generate liberty files, making it a cost-effective solution.	improvements in power efficiency and performance.	consumption, allowing for reuse across different technologies.
Research Gaps	Further exploration of accurate modeling techniques for resistive interconnects. Development of tools that consider faster runtime and simultaneous input switching	The method is currently validated only on 14nm technology; further validation on other technology nodes is needed.	Primarily tested with 8-bit booth multiplier; broader range of circuits needed for validation. - Impact of process variations on RSCE and INWE not fully explored.	Refinement needed for continuous and discontinuous memory access impact on power consumption.

2.2 ML Based Characterization

The increasing complexity and demand for Liberty (.lib) files at advanced process nodes. It highlights the challenges of validating and verifying these files, which are critical for ensuring successful timing closure and preventing silicon failures. The paper presents the use of machine learning (ML) techniques in Siemens EDA's Solido Characterization Suite to enhance .lib characterization and verification processes[7]. The traditional corner-based signoff approach has become insufficient for modern technology nodes due to increased variability and design complexities. As technology nodes shrink, variability increases, necessitating more rigorous .lib requirements. The paper emphasizes the need for advanced ML techniques to address these challenges.ML based flow chart for library characterization is given in fig 2.2.

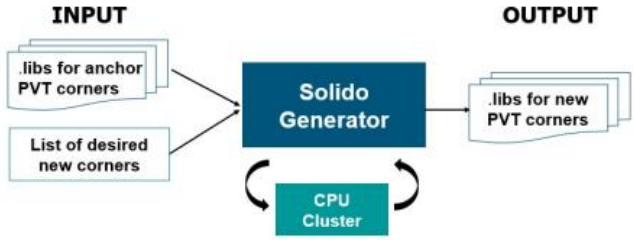


Fig.2.2: Flow chart of PVT generation with Solido Generator[6].

Machine Learning (ML) approach to rapidly generate full cell libraries on demand, facilitating extensive design space exploration and fully automated Design Technology Co-Optimization (DTCO). The proposed method demonstrates a high prediction accuracy and significant improvements in circuit performance, particularly for emerging technologies like Negative Capacitance (NC)-FinFET[8]. Standard cell libraries are essential for sharing process technology between foundries and circuit designers, providing descriptions of cells for use in Electronic Design Automation (EDA) tools. However, traditional libraries may not cover all operational conditions, limiting the designer's ability to optimize circuits fully. DTCO aims to bridge the gap between device physics and circuit performance by optimizing technology and circuit design together.

It explores efficient learning strategies for machine learning (ML)-based characterization of aging-aware cell libraries. It addresses the challenge of high demand for training data and costly SPICE simulations required for generating training samples. Machine learning has become integral to electronic design automation (EDA), accelerating simulations and improving program accuracy[9]. ML-based standard cell library characterization enables rapid generation of cell libraries, facilitating extensive design-space exploration and more accurate results. However, the benefits are limited by the high demand for training data and the computational cost of SPICE simulations. Efficient learning strategies are needed to reduce training data requirements while sustaining high prediction accuracy.

A next-generation multi-objective co-optimization approach that integrates machine learning (ML) with human intelligence to address the challenges in technology enablement for sub-10nm technology nodes. Advanced technology development demands extensive co-optimization across multiple domains, from process integration to system/product levels. Traditional methodologies relying solely on human expertise are limited by time-to-market (TTM) constraints and may miss potential PPA improvements due to human bias[10]. The paper proposes enhancing conventional practices with ML techniques to explore a broader design space, achieve faster convergence to optimal solutions, and improve QoR.

Literature Review on ML Based Characterization is shown in Table Below 2.2

Table. 2.2: Literature Review on ML Based Characterization

Aspect	**Cell Library Characterization using Machine Learning for Design Technology Co-Optimization**	**Addressing Library Characterization and Verification Challenges Using ML**	**Efficient Learning Strategies for Machine Learning-Based Characterization of Aging-Aware Cell Libraries**	**Machine Learning-enhanced Multi-dimensional Co-Optimization of Sub-10nm Technology Node Options**
Focus	Rapid generation of cell libraries for DTCO using ML.	ML techniques for accelerating library characterization and verification.	Efficient learning strategies to reduce training data for aging-aware cell libraries.	Multi-dimensional co-optimization of sub-10nm technology node options using ML.
Results	High prediction accuracy (R^2 ~98%), improved circuit performance.	Improved library characterization and validation runtime, better quality libraries.	Up to 77% reduction in training data, high prediction accuracy.	10X improvement in TAT, better PPA compared to human-optimized designs.
Conclusion	The approach shows promise in DTCO with high accuracy, but the dependency on training data quality and potential over-optimism need addressing.	ML methods help generate accurate Liberty files quickly and effectively, improving PPA and yield.	The paper presents efficient learning strategies for aging-aware libraries, but the high computational overhead and limited ML algorithm exploration are areas for improvement.	The ML-enhanced co-optimization framework significantly improves TAT and PPA, but extensive setup and generalization challenges remain.
Research Gaps	Dependency on initial training data quality, potential over-optimism in predictions.	Limited focus on specific ML techniques used, potential scalability issues for larger nodes.	High computational overhead for active learning, limited exploration of other ML algorithms	Requires extensive setup and interfacing, potential challenges in generalizing to other nodes.

2.3 Liberty File

A new methodology for fast timing and power characterization of standard cell libraries using mathematical equations. This approach aims to reduce the CPU resources and time required for generating liberty files while maintaining high accuracy. The methodology is validated by comparing generated liberty files with characterized ones, showing an error of less than 3%[11]. Standard cell libraries are essential for static timing analysis (STA) tools used during synthesis and place & route (P&R) to simplify logic optimization and power estimations. Characterization involves performing simulations under various process, voltage, and temperature (PVT) conditions to generate liberty files. Traditional methods are resource-intensive and time-consuming, especially for advanced technology nodes.

A novel 3-dimensional (3D) monotonic characterization method for standard cell libraries to enhance power, performance, and area (PPA) in ASIC/CPU design. Standard cell libraries are crucial for optimizing PPA in ASIC/CPU design. Various library types and sub-types are developed to address trade-offs in area, performance, power, design for manufacturability (DFM), and design rule checking (DRC). The paper discusses the complexity introduced by these variations and proposes a method to improve PPA through 3D monotonic characterization[12].

The development of ASCLIC, a Software-as-a-Service tool for standard cell library characterization. ASCLIC aims to provide accessible and affordable characterization services, particularly for educational institutions. The tool supports Non-Linear Delay Model (NDLM) and Non-Linear Power Model (NLPM) and can efficiently utilize single and multi-core systems[13]. Standard cell library characterization is crucial for ASIC design, enabling accurate timing and power modelling. Existing commercial tools are often inaccessible due to high costs, prompting the need for an affordable and accessible alternative.

Literature Review on Liberty Files is shown in Table Below 2.3

Table. 2.3 Literature Review on Liberty File

Aspect	**New Efficient and Accurate Method of Generation of Standard Cells Liberty Files for Timing and Internal Power**	**Novel 3D Monotonic Characterization of Standard Cell Liberty File Attributes w.r.t ASIC Tool Flow**	**Development of Automated Standard Cell Library Characterization (ASCLIC) for Nanometer System-on-Chip Design**
Focus	Fast timing and power characterization of standard cell libraries using mathematical equations.	3D monotonic characterization method to enhance PPA in ASIC/CPU design.	Development of ASCLIC, a Software-as-a-Service tool for standard cell library characterization.
Result	Significant reduction in characterization time (from 650 hours to less than an hour) High accuracy	Significant PPA improvements in ASIC/CPU design	- Efficient multi-core implementation - Comparable accuracy to commercial tools - Reduced execution time and resource usage
Conclusion	The methodology significantly reduces characterization time while maintaining high accuracy.	The 3D monotonic characterization method enhances PPA in ASIC/CPU design, showing various advantages and no disadvantages.	Future work includes enhancing the frontend and expanding support for various models and simulators.
Research Gap	- Validation needed on other technology nodes - Limited focus on other factors affecting characterization	- Further exploration of algorithm applicability across different ASIC flows and tool vendors	- Limited support for newer delay models - Need for more interactive frontend - Expansion to multi-server support

CHAPTER 3

Optimizing IP Library Re-Characterization for Efficiency and Accuracy

This chapter explores the application of artificial intelligence to enhance IO characterization processes the research focuses on the challenges and inefficiencies associated with traditional library characterization methods, particularly in the context of standard cell modeling for System-on-Chip (SoC) implementations. The conventional techniques, reliant on analog simulations, often result in prolonged development cycles and high computational resource utilization. To address these issues, Siemens has introduced the Solido Characterization Suite, leveraging advanced machine learning algorithms to optimize the characterization process. This innovative suite reduces the need for extensive simulations, thereby cutting down computational expenses and shortening characterization periods. The thesis provides a comprehensive analysis of these traditional approaches, highlighting their limitations, and demonstrates through detailed examinations and case studies how machine learning can transform the characterization process into a more efficient and accurate method. The findings suggest that the Solido Characterization Suite holds significant potential for improving design efficiency and reliability in semiconductor design, marking a substantial advancement in the field of electronic design automation.

3.1 Objectives

The main goal behind this initiative involves creating methods for speeding up IP library re-characterization processes while maintaining results integrity. Advanced machine learning (ML) techniques will serve to quicken both the characterization and verification processes of .lib files after their implementation and development phase. The project makes use of ML algorithms to create accurate characterization data predictions which eliminate the need for extensive simulations as a result of ren time reduction as depicted in Table 4.1. The project takes measures to guarantee that characterized libraries comply with modern technology nodes requirements by delivering precise electrical parameter performance at all ranges to enable advanced semiconductor design development. A combination of procedural optimization and workflow enhancement will shorten the characterization duration while protecting the analytical result standards(Accuracy)as depicted in Table 4.3. The project adds a focus on ML techniques to enhance both the measurement precision and quality of libraries before validation for adherence to industrial requirements and specification criteria. This project seeks to enhance IP library re-characterization speed through its established objectives which enable more efficient operations for present-day semiconductor design requirements.

3.2 Methodology

Siemens introduced the Solido Characterization Suite as an answer to handle the shortcomings of traditional characterization tools by implementing ML-based algorithmic capabilities. Solido Characterization Suite delivers multiple advantages that enhance operational effectiveness by improving characterization workflow operations. The Solido Characterization Suite generates liberty files through machine learning algorithms without requiring complete characterization procedures. Data predictions along with automatic generation occur within the suite's algorithm system to eliminate the need for prolonged simulation runs as shown in fig.3.1. Due to reduced computational needs this approach results in better operational efficiency for the characterization system.

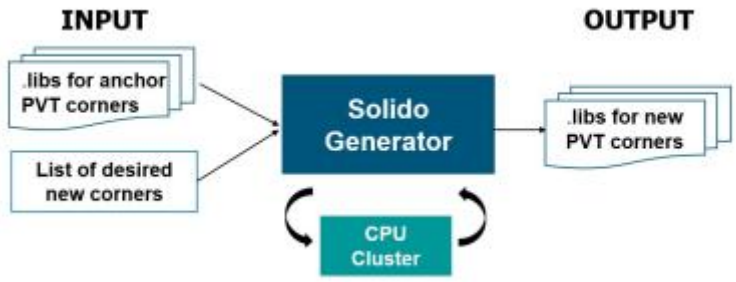


Fig.3.1: Solido ML Generator Model

Source: [Solido Characterization Suite | Siemens Software]

The Solido Characterization Suite enables users to analyse design deployments for selected PVT (Process, Voltage, Temperature) ranges where it generates new PVT measurements quickly. This assessment capability delivers both fast productions as shown on fig.4.1 as well as precise accuracy among the data points produced. The suite uses PVT space subsets to deliver accurate predictions for new points through efficient extrapolation which surpasses conventional approach.

The Solido Characterization Suite contains its main element as the Solido Generator. Through this tool users can efficiently determine PVT characteristics of design subsets in the PVT space and create new PVT points without compromise Employment of the Solido Generator leads to vast time savings that lower the complete characterization duration. The solution decreases both computational resource usage and overall operational costs needed to perform the process as shown in flowchart fig.3.2. The Solido Generator produces precise liberty files for modern technology nodes through its accurate output generation.

The Solido Characterization Suite uses ML algorithms and efficient characterizing features to overcome traditional tool’s while reducing runtime and conserving resources while maintaining high accuracy levels.

3.2.1 Solido Algorithm for Full library re-characterization

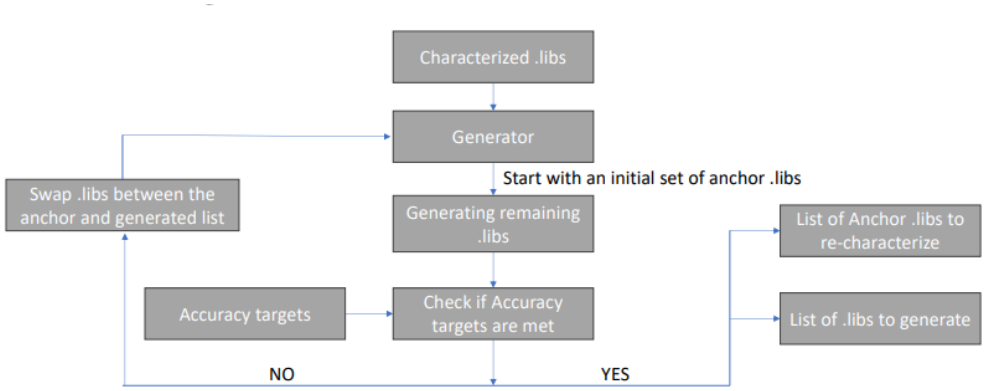


Fig.3.2: Flow Chart for Full Library Re-characterization

The Solido algorithm provides a step-by-step method to generate semiconductor design libraries which includes characterizing existing libraries.

The procedure starts by utilizing pre-characterized anchor libraries. The anchor libraries act as critical components for producing more libraries.

- **Initial Setup**: The process starts by using a first series of characterized library files (.libs) during setup. The pre-characterized libraries serve as basic benchmarks to develop additional libraries.
- **Generator**: The generator starts library creation procedures through utilization of anchor libraries as an initial foundation. The anchor libraries become the basis for new library production through this procedure.
- **Generating Remaining Libraries**: The generator develops new libraries which need characterizations. The list derives from the anchor libraries to include all necessary libraries for the final design.
- **Accuracy Check**: The algorithm verifies that the generated new libraries meet the stated accuracy requirements after their creation. The check of accuracy targets during this step plays a vital role in verifying that the produced libraries achieve the established specifications.
- **Re-characterization**: The algorithm performs re-characterization by finding libraries for correction when accuracy targets remain unmet. The accuracy process depends on switching anchor list and generated list components until the desired precision levels are achieved.
- **Iteration**: The system repeats its rounds between library generation and accuracy verification until it fulfils all specified accuracy measurements. The final set of libraries achieves accurate and reliable results through this repeated process.

- **Completion**: The procedure finishes when all accuracy targets are completed to produce the final list of libraries. The semiconductors use these generated libraries for design purposes.

The Solido algorithm features a systematic approach to validate additional libraries with initial characterized libraries for securing exact and dependable semiconductor designs.

3.2.2 Solido Algorithm for New PVT corner addition

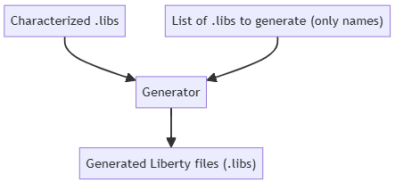


Fig.3.3: Flow Chart for New PVT corner addition

During a full design cycle of a product, characterization is usually first done for a small set of PVTs, and incremental PVT requests are added as work continues. The turn-around-time on individual PVT requests after the initial set can often be a significant bottleneck in a design team's productivity. One way to use the tools in the Generator package is to generate new PVT requests using the original set of PVTs as input data.

- **Characterized. libs:** This represents the existing characterized library files that contain the necessary data for generating new Liberty files.
- **List of libs to generate (only names):** This is a list that contains only the names of the Liberty files that need to be generated. It does not contain the actual data, just the identifiers for the files to be created.
- **Generator:** This is the core component of the process. It takes the characterized. libs and the list of names to generate the required Liberty files. The generator uses the data from the characterized. libs and matches it with the names in the list to produce the new files.
- **Generated Liberty files (.libs):** This is the output of the process. These are the newly generated Liberty files that have been created based on the input characterized. libs and the list of names.

3.2.3 Solido Algorithm for Target Percentage

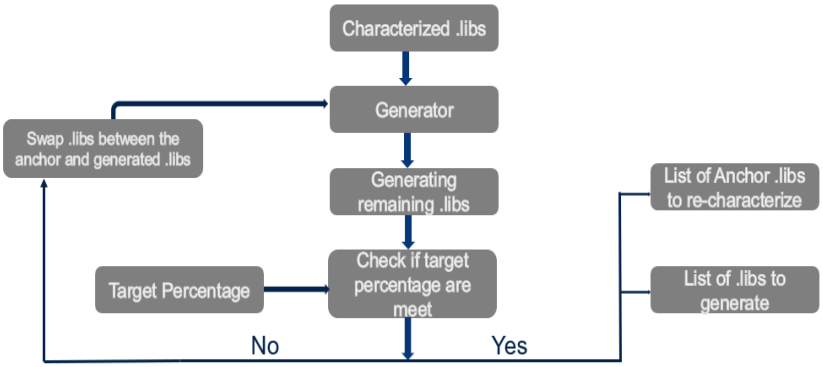


Fig:3.4: Flow Chart for Target Percentage Feature of Solido.

The target_percentage is an important setting used in Design of Experiments (DoE), especially when working with tools like Anchor-opt to optimize or analyze design corners. It tells the tool what percentage of the design corners (specific combinations of input conditions) should be generated or estimated, instead of being fully simulated or measured. This percentage can range from 5% to 95%, allowing you to strike a balance between saving time and maintaining accuracy.

For example, if you set the percentage to 20%, the tool will generate 20% of the design corners while still ensuring that the overall results remain accurate. You can also try multiple percentages, like 10%, 50%, or 90%, to see how the tool performs with different levels of generated data. This flexibility lets you adjust the DoE process based on your specific needs, whether you want to prioritize accuracy or reduce computational effort.

In general, using a lower percentage of generated corners means more simulations are run, which improves accuracy but takes more time and resources. On the other hand, a higher percentage reduces the workload by generating more data points, but it might slightly affect accuracy. The tool is designed to find the best balance for your chosen percentage, ensuring reliable results while optimizing efficiency.

CHAPTER 4

Results & Analysis

This chapter focuses on the results and analysis of the methodologies and tools discussed in the previous chapters, particularly the application of advanced machine learning techniques for library characterization. This chapter evaluates the performance of the "Solido Characterization Suite" in optimizing the characterization process, reducing runtime, and maintaining accuracy. Detailed comparisons are presented between traditional characterization methods, such as SPICE simulations, and the machine learning-based approach, highlighting the significant improvements in efficiency and computational resource utilization. The chapter also analyzes the accuracy of the generated results, ensuring they meet industry standards for timing, power, and noise parameters. Additionally, the chapter explores the impact of features like target percentage generation and incremental PVT corner additions on runtime reduction and accuracy. Through comprehensive data analysis and visualization, Chapter 4 demonstrates the effectiveness of machine learning in addressing the challenges of traditional library characterization methods and establishes its potential as a transformative tool in modern semiconductor design.

The primary objective of this thesis is to implement strategies to significantly reduce the runtime of IP library re-characterization while maintaining the accuracy and reliability of the results.

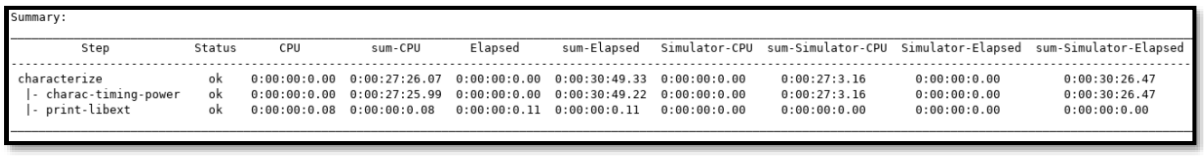
4.1 Actual Run Time Comparison Table for Full Library Re-characterization:

Table 4.1.: Run Time Comparison Table for 163 PVT's Corners

Total PVT's	Generated PVT's	Run Time		Speed Up
		Spice Char	Solido Char	
207	163	4890 Min	96 Min	50.93 X (98 % saved)

Above table 4.1 shows the Run-Time comparison between Spice Characterization Simulation and Solido Characterization Simulation for 163 PVT's corners.

Table 4.2.: Spice Simulator Run Time for 1 PVT Corner



Summary:

Step	Status	CPU	sum-CPU	Elapsed	sum-Elapsed	Simulator-CPU	sum-Simulator-CPU	Simulator-Elapsed	sum-Simulator-Elapsed
characterize	ok	0:00:00:0.00	0:00:27:26.07	0:00:00:0.00	0:00:30:49.33	0:00:00:0.00	0:00:27:3.16	0:00:00:0.00	0:00:30:26.47
|- charac-timing-power	ok	0:00:00:0.00	0:00:27:25.99	0:00:00:0.00	0:00:30:49.22	0:00:00:0.00	0:00:27:3.16	0:00:00:0.00	0:00:30:26.47
|- print-libext	ok	0:00:00:0.08	0:00:00:0.08	0:00:00:0.11	0:00:00:0.11	0:00:00:0.00	0:00:00:0.00	0:00:00:0.00	0:00:00:0.00

Characterization Time for 1 PVT's in SPICE Simulator ~ 30 Min

Total PVT's to Generated =163

Total Simulation Time for 163 PVT's to Generated =163 * 30

=4890 Min

```
Generator Summary
-----------------------------------------
Version: 2024.2

Start time: 2024-11-28 10:44:21
End time: 2024-11-28 12:21:00
Total run time: 1:36:40

Ran on local cluster using 30 nodes
```

Fig.4.1: Solido Characterization Tool Run Time for 163 PVT's Corner

4.2 Actual Run Time Comparison Table for new PVT's Addition

Table 4.3.: Run Time Comparison Table for 12 new PVT's Corners

Characterized PVT's	Additional PVT's	Run Time		Speed Up
		Spice Char	Solido Char	
65	12	360 Min	6 Min	60 X (98.3 % saved)

- Analyze behavior across existing PVT data using ML and build accurate models for all measurements - timing, power, noise etc.
- Uses existing. libs as input → PDKs, netlist or spice-simulation not needed.

4.3 Accuracy Result of Solido Characterization Tool:

Table 4.4.: Accuracy Report Table from Solido tool

Summary for overall:

Output	Absolute Tol.	Relative Tol.	In Tolerance	Out of Tolerance	Total Compared	Percent in Tolerance	All Points
NLDM fall delay time	2.50e-11	5.0%	4785	105	4890	97.9%	4890
NLDM fall transition time	2.50e-11	5.0%	4890	0	4890	100.0%	4890
NLDM internal power	5e-13	10.0%	17604	0	17604	100.0%	17604
NLDM leakage power	1e-06	10.0%	187382	720	188102	99.6%	188102
NLDM rise delay time	2.50e-11	5.0%	4863	27	4890	99.4%	4890
NLDM rise transition time	2.50e-11	5.0%	4890	0	4890	100.0%	4890

- **Absolute Tolerance:** The absolute tolerance value for the metric, representing the maximum allowable deviation from the expected value in absolute terms.
- **Relative Tolerance:** The relative tolerance value for the metric, representing the maximum allowable deviation from the expected value as a percentage.
- **In Tolerance:** The number of data points that fall within the specified tolerance limits (both absolute and relative).
- **Out of Tolerance:** The number of data points that fall outside the specified tolerance limits.

For Example:

For NLDM fall delay time:

Absolute Tol.: 2.50×10^{-11}

Relative Tol.: 5.0%

In Tolerance: 4785 points

Out of Tolerance: 105 points

Total Compared: 4890 points

Percent in Tolerance: 97.9%

All Points: 4890 points

This means that out of 4890 data points for NLDM fall delay time, 4785 points were within the specified absolute tolerance of 2.50×10^{-11} and relative tolerance of 5.0%, resulting in 97.9% of the points being in tolerance.

The implementation of Solid ML characterization significantly reduces the run time of machine learning models through optimized data processing and efficient algorithmic strategies. Despite this reduction in run time, the accuracy of the models is maintained.

4.4 Run time reduction using target percentage features of Solido Tool:

```
================= DoE =================
Completed 24 iterations
Target generate percent: 50%
Final set: anchor    22/44 (50%)
Final set: generated 22/44 (50%)
Final set: excluded  0/44 (0%)
```

Fig.4.2: Optimization Result for Target Percentage

- **Target Percentage (50%):**
  means we have instructed the tool to generate 50% of the design corners rather than fully simulating and measuring them.
- **Anchor: 22/44 (50%):**
  Out of the total 44 design corners, 22 were designated as anchor points. These are the corners that were fully simulated to provide a solid foundation for the analysis**.**
- **Generated: 22/44 (50%):**
  The remaining 22 design corners were generated or estimated using statistical or interpolation techniques, based on the information derived from the anchor points.
- **Excluded: 0/44 (0%):**
  No corners were excluded from the analysis, meaning all 44 corners were either simulated or generated.

Table 4.5.: Accuracy Report Table for target-percentage (50%) from Solido tool

Summary for overall:

Output	Absolute Tol.	Relative Tol.	In Tolerance	Out of Tolerance	Total Compared	Percent in Tolerance	All Points
NLDM fall delay time	2.50e-11	5.0%	4994	5038	10032	49.8%	10032
NLDM fall transition time	2.50e-11	5.0%	10028	4	10032	99.9%	10032
NLDM internal power	5e-13	10.0%	32734	4578	37312	87.7%	37312
NLDM leakage power	1e-06	10.0%	23468	1920	25388	92.4%	25388
NLDM rise delay time	2.50e-11	5.0%	5765	4267	10032	57.5%	10032
NLDM rise transition time	2.50e-11	5.0%	10032	0	10032	100.0%	10032

The above results indicate that the target generate percentage of 50% may not provide sufficient accuracy for all metrics. While some metrics perform well, others show poor accuracy, such as NLDM fall delay time (49.8%) and NLDM rise delay time (57.5%).

The results highlight significant reductions in runtime and computational resource usage compared to traditional methods like SPICE simulations, while maintaining high accuracy in timing, power, and noise parameters. Features such as target percentage generation and incremental PVT corner additions further enhance efficiency without compromising precision. The analysis confirms that machine learning approaches address the limitations of conventional techniques, making them highly suitable for modern semiconductor design.

CHAPTER 5

Conclusion

Library characterization is very important for designing modern electronic devices because it lets us accurately model performance, power, and other important parameters. But traditional ways of characterizing are becoming less and less useful because designs are getting more complicated, accuracy is needed more, and the process takes a long time. Siemens "Solido Characterization Suite" uses cutting-edge machine learning algorithms to solve these problems in a way that changes the game.

The results of this thesis show that the Solido Characterization Suite cuts down on the time and computing power needed to characterize a library by a large amount. For example, it speeds up full library re-characterization by '50.93x' and incremental PVT additions by '60x', all while keeping high accuracy, with '97.9% of data points' falling within tolerance limits. It can predict more PVT points using only a few conditions, which means that long SPICE simulations are no longer necessary. This speeds up the process, makes it more efficient, and uses fewer resources.

The tool also has new features like "target percentage generation," which lets you make trade-offs between runtime and accuracy, making the characterization process even better. These features make the Solido Characterization Suite an important tool for dealing with the difficulties of modern semiconductor designs.

The future of library characterization looks bright, with chances for more progress in smarter algorithms, scalability, cross-platform compatibility, and environmentally friendly practices. These new ideas will make it possible to make electronic devices that are more powerful, efficient, and dependable, which is what the semiconductor industry needs more of.

In conclusion, the "Solido Characterization Suite" is a big step forward in library characterization. It offers a faster, more accurate, and more efficient way to do things that works well with the problems that come up in modern design workflows. It is a very important step toward moving electronic design automation forward and changing the future of semiconductor technology.

Future Scope

The future of library characterization looks better and better as tools like the Solido Characterization Suite continue to improve it. Solido ML has to get quicker while optimizing anchor corners to keep up with the expanding needs of modern semiconductor design. This will make the characterization process both faster and more accurate. To reach this goal, there are a few important areas that could use further work.

It will be very important to keep improving machine learning algorithms so that they can converge on anchor corner improvements faster while keeping or even improving accuracy. These algorithms need to learn and change over time so that the characterization process is easier and less computer power is needed. Also, using advanced characterization methods on new technologies like quantum computing and neuromorphic computing will need custom ML approaches that can address the unique problems that come up in these fields.

Scalability will also be very important since characterization techniques need to change to work with designs that are getting bigger and more complicated. By focusing on ML-driven improvements for anchor corners, the process can be speed up, which will save time and money on full characterization. More automation of the characterization process will mean less manual work, which will speed up and improve processes.

In addition to speed, creating methods that take into account not only timing and power but also dependability, aging effects, and security will provide anchor corner optimizations a more complete approach. By adding these advanced methods to traditional design processes, you can make sure that they are easy to use and deploy. Solido ML will also be able to give faster results while optimizing anchor corners in a variety of settings if it is compatible with a wide range of design tools and platforms. This will make it easier to integrate into existing design and verification processes.

Solido ML will help make electronic devices that are more powerful, efficient, and reliable by focusing on speed and anchor corner optimization. This will match the needs of modern semiconductor design while pushing the limits of creativity.

References

1. R. Abhirami and R. Ratra, "Challenges and solutions for IP CAD view generation for efficient system on chip integration," *Journal of Emerging Technologies and Innovative Research*, vol. 6, no. 4, pp. 148-150, Apr. 2019.
2. Synopsys. (n.d.). What is library characterization? Synopsys. https://www.synopsys.com/glossary/what-is-library-characterization.html
3. B. Ackalloor and D. Gaitonde, "An overview of library characterization in semi-custom design," *Proceedings of the IEEE 1998 Custom Integrated Circuits Conference (Cat. No.98CH36143)*, Santa Clara, CA, USA, 1998, pp. 305-312, doi: 10.1109/CICC.1998.694988.
4. M. K. M, A. A. A and S. P, "Design and Characterization of Standard Cell Libraries for Optimal Subthreshold Circuits," *2023 Innovations in Power and Advanced Computing Technologies (i-PACT)*, Kuala Lumpur, Malaysia, 2023, pp. 1-5, doi: 10.1109/i-PACT58649.2023.10434863.
5. K. Charafeddine and F. Ouardi, "Fast timing characterization of cells in standard cell library design based on curve fitting," *2017 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS)*, Fez, Morocco, 2017, pp. 1-6, doi: 10.1109/WITS.2017.7934646..
6. M. Rogers-Vallée, M. -A. Cantin, L. Moss and G. Bois, "IP characterization methodology for fast and accurate power consumption estimation at transactional level model," *2010 IEEE International Conference on Computer Design*, Amsterdam, Netherlands, 2010, pp. 534-541, doi: 10.1109/ICCD.2010.5647622.
7. T. Durga, "Addressing library characterization and verification challenges using ML," Siemens Digital Industries Software, White Paper, Jan. 2022. [Online].
8. F. Klemme, Y. Chauhan, J. Henkel and H. Amrouch, "Cell Library Characterization using Machine Learning for Design Technology Co-Optimization," *2020 IEEE/ACM International Conference On Computer Aided Design (ICCAD)*, San Diego, CA, USA, 2020, pp. 1-9.
9. F. Klemme and H. Amrouch, "Efficient Learning Strategies for Machine Learning-Based Characterization of Aging-Aware Cell Libraries," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 12, pp. 5233-5246, Dec. 2022, doi: 10.1109/TCSI.2022.3201431.
10. A. Ceyhan, J. Quijas, S. Jain, H. . -Y. Liu, W. E. Gifford and S. Chakravarty, "Machine Learning-enhanced Multi-dimensional Co-Optimization of Sub-10nm Technology Node Options," *2019 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, 2019, pp. 36.6.1-36.6.4, doi: 10.1109/IEDM19573.2019.8993557.

11. K. Charafeddine and F. Ouardi, "New efficient and accurate method of generation of standard cells liberty files for timing and internal power," *2017 International Conference on Electrical and Information Technologies (ICEIT)*, Rabat, Morocco, 2017, pp. 1-6, doi: 10.1109/EITech.2017.8255291.
12. L. M. K. Garimella and S. R. S. Garimella, "Novel 3D monotonic characterization of standard cell Liberty file attributes wrt ASIC tool flow," in *Proc. 2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2019, pp. 227–230.
13. M. S. I. Bin Hussin, Y. W. Lim, N. A. Kamsani, S. J. Hashim, and F. Z. Rokhani, "Development of automated standard cell library characterization (ASCLIC) for nanometer system-on-chip design," in *Proc. 2017 IEEE 15th Student Conference on Research and Development (SCOReD)*, Dec. 2017, pp. 93–97.

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