Design and Analysis of Low Dropout Voltage Regulator for Ultra-Low-Power Applications

Thesis

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CERTIFICATE

I, **Lalit Sood,** hereby declare that the research work contained in the dissertation entitled **"DESIGN AND ANALYSIS OF LOW DROPOUT VOLTAGE REGULATOR FOR ULTRA-LOW-POWER APPLICATIONS"** is carried out by me at **Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala** in fulfillment of the requirements for the award of degree of **"Doctor of Philosophy"** is a record of actual research conducted under the guidance of **Dr. Alpana Agarwal**. The material presented in this work does not include material previously published or written by another person, unless appropriately mentioned in the text.

The results obtained in this work have not been presented, in whole or in part, to other institutes or universities for obtaining an academic degree or diploma.

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I, **Dr. Alpana Agarwal**, hereby certify that the above information provided by the candidate is correct and true to the best of my knowledge. He has worked under my supervision and complied with the requirements for the submission of this thesis, which reached the requisite standard.

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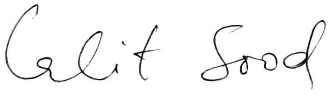

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ABSTRACT

A system-on-chip (SoC) with near-threshold supply voltage operation has received a significant amount of attention. Due to its high energy-efficiency, it supports a number of low power emerging applications such as wireless sensor networks and Internet-of-Thing devices. By integrating diverse digital, analog, mixed-signal, and power delivery subsystems, these SoC designs must harness dozens of voltage domains to push the boundaries of power efficiency, performance, and robustness.

A low dropout (LDO) regulator is a key building block for creating voltage domains on a chip due to its high-power density. In particular, its digital implementation, i.e., digital LDO, recently has emerged as a popular topology since it can support a wide range of input voltage from sub-threshold to near-threshold voltage domains, while conventional analog LDOs become less effective. However, the existing digital LDO designs use full-custom comparators to compare reference and output voltages, which make the designs partially synthesizable. Aside from that, most digital LDOs require a huge off-chip output capacitor to stabilize the output voltage. Also, digital LDOs require high clock frequency (f_{CLK}) to provide fast-transient response; however, such solutions inevitably increase power dissipation.

This thesis presents my research on digital LDOs for ultra-low-power applications. My research focuses on CMOS standard-cell-based implementation of LDO. To implement the entire digital LDO using CMOS standard cells, a fully synthesizable comparator (FS-COM) is first designed and proposed to determine the error voltage. The FS-COM can support rail-to-rail common-mode input voltages (V_{CM}). The fast-transient response of FS-COM, even at sub-threshold or near threshold voltage levels, makes it suitable for high-speed ultra-low-power designs. A fully-synthesizable LDO is then proposed using FS-COM for applications consuming up-to tens of microamps. With a supply voltage (V_{SUP}) of 0.5Vand a load current (I_{OUT}) of up-to 2mA, a regulated V_{OUT} is attained with a dropout voltage of 50mV. At f_{CLK} = 10MHz, the proposed LDO achieves a quiescent current (I_Q) and fast-TR of 2.2µA and 910ns, respectively. A maximum current efficiency (η) of 99.89% is attained with output ripples < 1mV. The last design introduces overshoot/undershoot detector and freeze-mode to achieve ripple-free output and a fast-transient response. The layouts of proposed designs are implemented using conventional synthesis and place-and-route (PnR).

LIST OF PUBLICATIONS

PUBLISHED

P1. Lalit Sood and Alpana Agarwal, “A CMOS standard-cell based fully-synthesizable low-dropout regulator for ultra-low power applications," AEU - International Journal of Electronics and Communications, Volume 141, 2021, 153958.
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P2. Lalit Sood and Alpana Agarwal, “A Transient-Enhanced Low-Power Standard-Cell-Based Digital LDO," The Arabian Journal for Science and Engineering, 2022.
(SCI Indexed; Impact Factor 2.334)

COMMUNICATED

P1. Lalit Sood and Alpana Agarwal, “A Low-Power Fully-Synthesizable Clocked Comparator for Ultra-Low-Power Applications,” VDAT 2023 to be held at BITS-Pilani.

LIST OF ACRONYMS, ABBREVIATIONS & SYMBOLS

η	Current Efficiency
σ_{IOS}	Standard Deviation of Input Offset Voltage
ADC	Analog-to-Digital Converter
A-LDO	Analog Low Dropout Regulator
Bi-SR	Bidirectional Shift Register
CL-DLDO	Capacitor-Less DLDO
CLK	Clock
CMOS	Complementary Metal–Oxide–Semiconductor
CT	Coarse-Tuning
D-FF	D-Flip Flop
D-LDO	Digital Low Dropout Regulator
D-CTRL	Digital Logic Controller
DVFS	Dynamic Voltage and Frequency Scaling
f_{CLK}	Clock Frequency
FOM	Figure of Merit
FS-COM	Fully-Synthesizable Comparator
FS-LDO	Fully-Synthesizable Low Dropout Regulator
FT	Fine-Tuning
I_{IN}	Input Current (Drawn from Supply)
I_{OUT}	Load Current
I_Q	Quiescent Current
LCO	Limit-Cycle Oscillations
MT	Medium-Tuning
NAND-COM	NAND-Based Comparator
NOR-COM	NOR-Based Comparator
Op-Amp	Operational Amplifier
OPR	Operating Range
OUD	Overshoot/Undershoot Detector
PDN	Pull-Down Network

PMA	P-MOSFET Array
PnR	Place-and-Route
QT	Quivering Tuning
QTU	Quivering Control Unit
RTL	Resister-Transistor Logic
TFS-LDO	Transient Enhanced Fully-Synthesizable Low Dropout Regulator
TBA	Tri-State Buffer Array
V_{CM}	Common-Mode Voltage
VCO	Voltage-Controlled Oscillator
V_{REF}	Reference Voltage
V_{RES}	Voltage Step Resolution
V_{SUP}	Supply Voltage
V_{TH}	Threshold Voltage
Vt_{INV}	Switching Threshold of INV cell

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CHAPTER 1

INTRODUCTION

"***Science*** *is a powerful way to the systematic study of the structure and behaviour of the physical and natural world through observation, experimentation and analysis, and* ***Technology*** *is the applications of scientific knowledge for practical purposes.*"

-Anonymous

A low dropout (LDO) regulator is an electronic circuit that produces and maintains a constant output voltage regardless of input voltage or load conditions. It can operate with a small difference between its output and supply voltages. It produces a regulated output voltage from power supply in a range that other electrical components can handle.

Recently, digital LDOs (DLDO) have attracted attention due to their fewer stability problems at sub-threshold voltage levels. Also, their small area and power requirements make them more attractive compared to their analog counterparts. The available DLDOs are partially synthesized and require tedious manual design. These DLDOs monitor their outputs using various analog circuits, such as time-to-digital converters, analog-to-digital converters, analog comparators, etc. The key objective of this thesis is to design and propose a fully-synthesizable DLDO adapted to the rapid design market. The main challenge in designing a fully-synthesizable DLDO is to design a synthesizable error amplifier that can track output changes. In the next chapters, a fully-synthesizable clocked comparator used as an error amplifier in the proposed fully-synthesizable DLDO architectures is presented.

1.1 BACKGROUND

In recent years, the Internet of Things (IoT) and portable mobile devices have received significant attention due to their wireless connection and accessibility through cloud Internet services. The majority of these devices are battery-powered and have multi-core or application processors that can operate on low supply voltage (V_{SUP}). These devices require different V_{SUP}

levels to power their digital, analog, and mixed-signal circuits in order to improve power efficiency. The ever-increasing demand for multi-functional, power-efficient portable devices necessitates the use of ultra-low-power design approaches [1, 2]. Most IoT devices rely on energy harvested from external sources like thermal energy, solar power, kinetic energy, wind energy [3]. External noise has a significant impact on the harvested energy. As a result, the harvested energy must be cleaned before it is fed into the noise-sensitive circuits. It is first stored in tiny batteries before being transmitted to power-sensitive devices via low-power regulating circuits. Moreover, some IoT devices remain active for a short period of time and are kept in sleep or stand-by mode for a long time. In sleep or stand-by mode, the digital circuitry of these devices can be operated at very low V_{SUP} to reduce the overall power consumption [4]. In addition, portable battery-operated mobile devices consume some of the battery power for their internal clock oscillators and control circuits during idle or standby mode [5]. These devices must have an efficient power management system to provide different V_{SUP} levels in different operating modes to prolong the battery life [6]. [7-10] show that the circuit, operating at sub-threshold voltage level, results in a high power efficiency.

In a system-on-chip (SoC), multiple voltage regulators are used to provide different levels of power supply to its different sub-circuits. As the number of power domains increases, area and power efficiency of voltage regulators become more important. Voltage regulators use separate power domains to supply power from a source to a load circuit while maintaining a stable output voltage. The input voltage from a power source, such as a battery, changes over time, and the current drawn by a load circuit may fluctuate depending on the task, especially if the load is a digital circuit. Voltage regulators must therefore respond to and compensate for changes in voltage and current in a timely and accurate manner.

There are two types of voltage regulators: switching regulators and linear regulators. Switching regulators, like buck converters, use switches and passive components such as an inductor. Linear regulators, on the other hand, function as voltage dividers: linear regulators control output voltage by adjusting their equivalent impedance relative to their load impedance. Linear regulators are preferred for fully integrated systems. Since linear regulators, unlike switching regulators, do not require large inductors, they can significantly reduce area and cost when a large number of power domains are required. Linear regulators also have a relatively short response time to external changes, making them suitable for power-saving techniques.

1.2 LOW DROPOUT REGULATOR

The LDO regulators are widely used in power management systems to regulate voltage levels within a chip. An LDO regulator designed to drive small loads with a small output capacitor can be integrated on-chip for a better power supply rejection ratio (PSRR) and response time. The LDO regulators can regulate an output voltage (V_{OUT}) even when the difference between the V_{SUP} and V_{OUT} is minimal.

1.3 PERFORMANCE METRICS

The performance of an LDO regulator can be characterized by the following parameters [1, 2, 5-13]:

- **Input voltage (V_{SUP}) range:** It is the input supply range for which the LDO can perform and meet the system requirements. The lowest V_{SUP} level must be greater than the LDO's dropout voltage plus V_{OUT}.
- **Dropout voltage:** It is the minimum voltage difference between the V_{SUP} and V_{OUT} levels required to regulate LDO's output. It is measured as the voltage drop across the pass transistor. A low dropout voltage is desirable as it leads to the increased power efficiency of the regulator. However, to keep the pass transistor in saturation, a minimum fixed amount of dropout is required.

$$\text{Dropout voltage} = V_{SUP} - V_{OUT} \tag{1.1}$$

- **Quiescent current (I_Q):** The I_Q of an LDO regulator is defined as the current drawn by the regulator to ensure the proper voltage biasing. Alternatively, it is measured as the difference between the load current (I_{OUT}) and the current drawn from V_{SUP}.

  A low value of I_Q is desirable to achieve high power efficiency. The I_Q does not directly contribute to the output power delivered, as it consists of biasing currents required to keep the design working.

$$I_Q = I_{IN} - I_{OUT} \tag{1.2}$$

- **Power supply rejection ratio (PSRR):** The PSRR is a measure of the capability of an LDO regulator to protect the V_{OUT} from the noise or ripples on V_{SUP} and is expressed as a ratio of output ripple voltage to input ripple voltage.

$$\text{PSRR} = \frac{V_{OUT}\ \text{Variations}}{V_{SUP}\ \text{Variations}} \tag{1.3}$$

- **Current efficiency (η):** The current efficiency of an LDO regulator is expressed as the ratio of current delivered to the load (I_{OUT}) to the total current drawn from the input supply.

$$\eta = \frac{I_{OUT}}{(I_{OUT} + I_Q)} \times 100 \tag{1.4}$$

- **Load transient response:** It is defined as the LDO regulator's capability to maintain the V_{OUT} at desired level when I_{OUT} changes suddenly. It takes several factors into account, like peak overshoot and undershoot voltages, and settling time.
- **Peak-to-peak ripple voltage (ΔV_{ripple}):** This term is used to indicate the noise on LDO's output at steady-state. This parameter plays an important role in characterizing the performance of a digital LDO regulator whose output continues to oscillate around reference level in steady-state.
- **Load regulation:** It is defined as the LDO regulator's ability to regulate the V_{OUT} during a change in IL. It is measured in terms of mV/mA.

$$\text{Load regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \tag{1.5}$$

- **Figure of merit (FOM):** The FOM [27] is used to measure an LDO regulator's effectiveness and is calculated by the following equation. The lower the value of FOM, the better the LDO.

$$\text{FOM} = \frac{C_{OUT} \times \Delta V_{OUT} \times I_Q}{I_{MAX} \times \Delta I_L} \tag{1.6}$$

Where I_{MAX} is the maximum load current supported by the LDO, and ΔI_L is the load change.

1.4 LDO TOPOLOGIES

An LDO regulator can be broadly classified into two categories, based on the topologies used for its implementation - analog LDO (ALDO) regulators and digital LDO (DLDO) regulators.

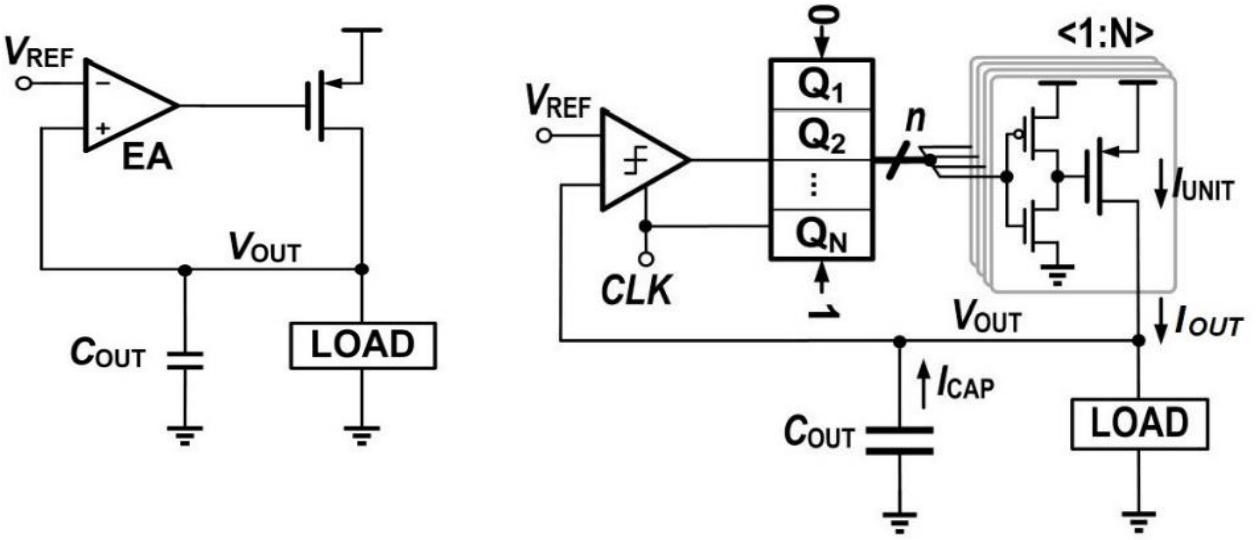


Fig. 1.1. Basic topologies of (a) ALDO, and (b) DLDO.

1.4.1 ALDO REGULATOR

The conventional ALDO regulator establishes negative feedback by using an operational amplifier (Op-Amp) and a power transistor, as shown in Fig. 1.1(a). The negative feedback maintains the V_{OUT} level equal to the reference voltage (V_{REF}) level for a specific load range.

The ALDO regulators have been explored to achieve a fast-transient response, high PSRR, and high current efficiency, especially for sensitive load circuits [11-15]. As the voltage level of V_{SUP} is reduced, the performance of the ALDO regulator begins to degrade [9]. At lower values of V_{SUP}, designing an Op-Amp is highly challenging since each transistor demands a voltage headroom to operate under the saturation region [6-9, 16-19]. The bandwidth and gain of an Op-Amp are sensitive to the PVT variations, which impact the response time and stability margin [20]. Designing an LDO regulator using a digital approach is an alternative way to make it operational at low V_{SUP} levels [18, 21].

1.4.2 DLDO REGULATOR

The need of a low-level, regulated power supply for digital circuits in ultra-low-power systems drives the push to investigate digital implementations of LDO regulators. The first-ever LDO regulator with digital control, shown in Fig. 1.1(b), is presented in [22]. This conventional DLDO regulator reduces the voltage headroom requirement by operating parallelly connected PMOS power transistors in their linear regions, in contrast to the ALDO regulator where a single PMOS power transistor is kept in the saturation region to regulate V_{OUT}.

The critical components of the conventional DLDO regulator are - comparator, digital controller, and PMOS power switch array. This DLDO regulator replaced the op-Amp used in the ALDO regulator with a comparator that can operate at a supply voltage as low as 0.5V. A digital serial-in-parallel-out bi-directional shift register has been used as a digital controller. The digital controller turns on/off the PMOS power switches to maintain the V_{OUT} at the desired level. Since the CMOS based switches need a minimum 0.5V gate voltage to perform switching [4], this conventional DLDO regulator can operate at a supply voltage down to 0.5V. At V_{SUP} = 0.5V, this regulator can provide a regulated V_{OUT} of 0.45V. It achieved a current efficiency of 98.7% with quiescent and load currents of 2.7µA and 200µA, respectively, in 65nm CMOS technology.

1.5 ORGANIZATION OF THE THESIS

Chapter-1: INTRODUCTION

This chapter discusses demonstrates the historical development of the low dropout regulator (LDO). The performance parameters of LDO are also discussed.

Chapter-2: LITERATURE REVIEW

In this chapter, a comprehensive review of related literature with their background is presented. It includes the preamble of LDO regulators for ultra-low-power applications along with the motivation and objectives of the thesis. Finally, based on the literature gaps, objectives and methodology for the current work have been decided.

Chapter-3: FULLY-SYNTHESIZABLE CLOCKED COMPARATOR

This chapter proposes a fully-synthesizable comparator (FS-COM) to monitor LDO’s output voltage. Thereafter a comparative analysis between proposed and existing designs is also presented.

Chapter-4: FULLY-SYNTHESIZABLE LDO

The proposed fully-synthesizable low dropout regulator is presented in this chapter. Following that, a comparison of proposed and existing designs is presented.

Chapter-5: TRANSIENT-ENHANCED FULLY-SYNTHESIZABLE LDO

This chapter discusses the additional digital circuitries introduced to fully-synthesizable low dropout regulator in order to enhance its transient response. Thereafter a comparative analysis between proposed and existing designs is also presented.

Chapter-6: CONCLUSIONS & FUTURE SCOPE

In this final chapter of the thesis, a summary of the proposed work and its potential future scope is documented.

CHAPTER 2

LITERATURE SURVEY

"A significant literature will provide a vital feature of any thesis. An actual survey, summarizing and fusing what is known while recognizing gaps in the knowledge base, facilitating theory development, closing areas where enough research already exists, and uncovering areas where more research is needed."

J. Webster and R. Watson, 2002

2.1 LITERATURE REVIEW OF LOW-VOLTAGE LDO REGULATORS

LDO regulators have been extensively researched for their low voltage operation. For ultra-low-power designs, DLDO regulators have received more attention than ALDO regulators due to their design simplicity. The DLDO regulators also exhibit trade-offs between power consumption, transient response speed, and ripples at steady-state [9, 23]. Their trade-offs on voltage regulation metrics are different from their analog counterparts [24]. Mixed-signal design approaches have been used to break these trade-offs [1]. Several types of research have been conducted to investigate low voltage LDO regulators using analogue, digital, and mixed-signal design approaches, as detailed below.

Different hybrid DLDO architectures that employ both analog and digital controllers are presented in [1, 3, 5, 6, 16, 17, 20, 21, 23].

Saad Bin Nasir [1] et al. highlights several characteristics of existing DLDO regulators, including their fast-transient response, design synthesizability, and performance adaption. However, they failed to provide a high dc accuracy at steady-state. In this paper, a hybrid LDO regulator using a parallel combination of analog and digital LDO regulators is presented and fabricated in 130nm CMOS to overcome the lack of output dc accuracy at a steady state. Although a high dc accuracy was achieved with the help of an ALDO regulator with a higher gain-bandwidth product, this design fails to support a wide load range due to the different power consumption and strengths of the two controllers.

Saad Bin Nasir [3] et al. proposed a hybrid low dropout voltage regulator using a switched-mode control (SMC) method to enable fast switching between the analog and digital controllers to broaden the dynamic range of voltage and current operations. This design achieved an optimal output dc accuracy and a fast-transient response of 0.71ns/mA while maintaining a current efficiency of 98.64%.

Stefan Leitner [5] et al. analyzed that low-power fine-grain power management systems use analog and digital mixed control for DLDO regulators. The presence of both continue- and discrete-time domains complicates the derivation of close-loop functions for these DLDO regulators. As a result, it is difficult to predict the performance of this type of regulator for a wide range of load variations, limiting the designer's capability. This paper presented close-loop mathematical equations for estimating the settling time and worst-case V_{OUT} deviation. These mathematical equations can assist designers in predicting the performance of such analog and digital mixed control based DLDO regulators during the early stages of design.

Saad Bin Nasir [6] et al. presented a scan-reconfigurable hybrid LDO regulator to provide control over the power efficiency/PSRR trade-off. The presented prototype is fabricated in a 130nm CMOS process. It achieved a PSR of -9dB to -34dB with a corresponding power efficiency of 87% to 56%, making it suitable for load circuits with a wide operational range.

Ning Zhang [16] et al. presented an analog-digital mixed-mode control-based LDO regulator with a single transistor-assisted buffer that can support a wide load range. The unity gain buffer can provide comprehensive control over the power MOSFET's gate voltage, allowing the proposed LDO regulator to regulate the V_{OUT} even under low load conditions. In contrast, digital control allows this LDO regulator to perform well under high load conditions. This design occupied an active area of $0.01mm^2$ in 180nm CMOS technology. This regulator achieved a load regulation of 0.21mV/mA with a 1µF external output capacitor and can support up to 150mA load current. The droop voltage is reduced by more than half by incorporating digital assistance to the LDO regulator.

Da Li [17] et al. presented a tunable DLDO regulator with a high transient response speed using the bisection method (BM). Instead of shift registers, binary adders were used in the proposed DLDO regulators to turn on/off the binary distributed PMOS switches. The bisection method tunes the PMOS switches in constant-step increments to keep the V_{OUT} steady-state during a load change. This regulator employs additional analog-assist technology to improve transient recovery

time after a voltage undershoot caused by a load change. The proposed DLDO regulator is built in a 180nm CMOS 1-poly and 6-metal process with a 0.1nF load capacitor. A load change of 18mA with a 1ns edge time causes a voltage undershoot/overshoot of 187/43mV. This DLDO regulator has a fast-settling time of 3.3µs and a small FOM of 0.42ps with a quiescent current of 9µA.

Jonghyun Oh [20] et al. proposed a synthesizable low-voltage DLDO regulator, excluding the power transistor and the externally connected load capacitor. It can regulate a V_{OUT} of 0.45V with a V_{SUP} of 0.5V, with a maximum current efficiency of 99.95% and a quiescent current of 4.7µA. For a 1mA increase in load current, a 70mV droop and settling time of 100ns have been achieved. This DLDO regulator occupied a 0.044mm^2 active area in the 28nm CMOS process.

Mo Huang [21] et al. implemented a tri-loop-based analog-assisted DLDO regulator without requiring any output capacitor. The output current steps are divided into three blocks in this design, which are controlled by coarse and fine loops with carry-in and carry-out operations. With the help of high-pass analog-assisted method that controls the unit current passing through the power MOS array, overshoots and undershoots on V_{OUT} have been significantly reduced. The coarse-tuning loop reduces recovery time, whereas the fine-tuning loop improves dc accuracy. After the fine-tuning operation, a freeze mode is introduced at a steady state to further reduce the quiescent current consumption. In 65nm CMOS technology, this DLDO regulator achieved a FOM of 0.23ps. The results showed a peak overshoot/undershoot of 105mV on V_{OUT} for a 10mA/1ns load step without using any output capacitor.

Han Li [23] et al. presented a transient enhanced fully integrated analog and digital mixed control-based LDO regulator with improved voltage regulation. The digital control is used to support a wide load range. The analog control, which includes a miller compensation capacitor and a buffer stage, is used to achieve stability and an improved slew rate. This LDO regulator, manufactured in a 180nm CMOS process, has an active chip area of 0.022mm^2 and can deliver a maximum load current of 150mA while regulating V_{OUT} = 1V with a 0.2V dropout voltage. A load regulation of 0.17mV/mA has been achieved with an improvement of more than 480% compared to the conventional design without digital control.

[24-26] present various DLDOs that track the output voltage using Flash ADC.

Yong-Jin Lee [24] et al. proposed a coarse- and fine-loop-based DLDO to handle large load requirements for mobile application processors. In the coarse loop, transient response speed has been increased by supplying a high current to the load with a flash analog-to-digital converter (ADC) based control. In contrast, the fine loop provides a high dc accuracy with shift register-based control and small-sized power transistors. A fully-digital control has been used to activate/deactivate the coarse and fine loops. This design was manufactured in 28nm CMOS technology, and occupied a 0.021mm^2 chip area. It can deliver a load current of up to 200mA while maintaining a V_{OUT} = 0.9V and a V_{SUP} = 1.1V. A voltage droop of approximately 120mV has been observed on V_{OUT} during load transition of 180mA.

Bai Nguyen [25] et al. proposed an analog assisted DLDO regulator with a trip-point controller and a dynamic step quantizer to achieve a fast transient response speed with 160mV V_{OUT} droop at 250A/ps. This DLDO regulator is comprised of three major components: 1) a high-speed, low-power inverter-based flash ADC to provide fast transient response while consuming little power, 2) a digital controller to minimise DC variations in V_{OUT}, and 3) a low-power ALDO regulator to reduce ripple V_{OUT} at steady state. This design achieved a DC load regulation of 16mV and a current efficiency of 99.4%. This DLDO is capable of overcoming the traditional design trade-offs between power integrity, power consumption, and dynamic transient speed.

Zhendong Ding [26] et al. proposed a flash ADC-based DLDO regulator with transient enhancement techniques. This design, manufactured in a 65nm CMOS process, can support I_{OUT} ranging from 0.04mA to 82.7mA while regulating V_{OUT} = 0.9V with V_{SUP} at 1.0V. For a 48mA load change, the settling time is reduced from 30μs to 6μs by using an exponential-ratio array in conjunction with the array of power transistors. Several performance parameters have been measured and compared to those of shift register-based DLDO regulators in order to highlight the advantages of the proposed flash ADC-based DLDO regulator. The presented prototype has several advantages, including high process scalability, low voltage operation, small area requirements, and good stability over a wide load range.

The DLDO architectures proposed in [27-36] employ multi-loop architecture or adaptive current step size control to maintain V_{OUT} level when load changes.

Haixin Song [27] et al. proposed a coarse-fine dual-loop-based DLDO regulator using a 1-bit delta-sigma modulator for low voltage phase-locked loops. The hardware of this DLDO regulator is less complicated than that of a conventional DLDO regulator. A binary-weighted transistor

array is used for the coarse loop, and a 1-bit delta-sigma modulator is used for the fine loop. This design is fabricated in a 65nm CMOS process and can deliver a load current from 100µA to 6mA while maintaining V_{OUT} at 0.95V with a V_{SUP} of 1V. The ripples on V_{OUT} have been reduced to less than 1mV at steady state with the help of an externally connected 100nF load capacitor.

Mo Huang [28] et al. implemented a DLDO regulator using coarse- and fine-tuning with burst mode to improve its transient response speed. During an overshoot or undershoot on the V_{OUT}, coarse tuning is enabled by using large-sized power transistors with a fast clock for a fixed duration to recover the V_{OUT} quickly. At steady-state, fine-tuning has been used with a low f_{CLK} and smaller power transistors to keep $V_{OUT} = V_{REF}$. This DLDO regulator with burst mode and coarse-fine-tuning is implemented in 65nm CMOS and consumed a low quiescent current of 82µA, achieving a current efficiency of 99.92%. With the help of coarse-fine tuning and burst mode, the undershoot on V_{OUT} has been reduced from 340mV to 55mV while supplying a load current of up to 100mA. This design achieved a FOM of 0.43ps and a fast-settling time of 700ns.

Saad Bin Nasir [29] et al. presented a scan programmable discrete-time DLDO regulator. This voltage regulator is fabricated in a low-power 130nm technology to deliver I_L (max) = 4.6mA while operating down to 0.5V. With the assistance of an SMC operation, this DLDO regulator achieved an 8x increase in transient response speed while maintaining more than 90% current efficiency.

Fan Yang [30] et al. improved the DLDO regulator's transient response speed and output dc accuracy by incorporating a multi-step switching (MSS) scheme. The asynchronous clocking and adaptive pipeline control are used during MSS operation. The transient response speed is increased by varying the power transistor size in two different lengths of coarse steps during large load variations. V_{OUT} is maintained at steady-state by more refined measures to reduce ripple voltage. The presented DLDO regulator is made in 65nm CMOS technology and can regulate V_{OUT} from 0.55V to 0.95V for V_{SUP} from 0.6V to 1V with a nominal 50mV dropout voltage and a load current of up to 500mA. This design achieved 100mV/10ns reference voltage switching and a resolution of 9.5b (768 levels) with a 5mV output ripple. At steady-state, this regulator consumed 300µA of quiescent current.

Ki-Chan Woo [31] et al. proposed a coarse-fine dual-loop DLDO regulator to achieve a fast-transient response. In comparison to the conventional DLDO, the proposed DLDO regulator achieved a 2x transient response speed. To increase transient speed, this design used a double

edge-triggered comparator and performed the shift-register operation on both the rising and falling edges of the clock. This DLDO regulator is built in 65nm CMOS technology and has a current efficiency of 99.94% with a ripple voltage of 1.5mV. The settling time has been reduced from 880ns to 340ns in comparison to the conventional DLDO regulator. The undershoot and overshoot voltages have been reduced to 37mV and 23mV, respectively, for a load change from 2mA to 100mA in 80ns. The undershoot and overshoot voltages have been reduced to 37mV and 23mV, respectively, for a load change from 2mA to 100mA in 80ns. The undershoot and overshoot voltages have been reduced to 37mV and 23mV, respectively, for a load change from 2mA to 100mA in 80ns. The undershoot and overshoot voltages have been reduced to 37mV and 23mV, respectively, for a load change from 2mA to 100mA in 80ns. The undershoot and overshoot voltages have been reduced to 37mV and 23mV, respectively, for a load change from 2mA to 100mA in 80ns.

Seong Jin Yun [32] et al. proposed a cap-less DLDO regulator with self-clocking burst logic for ultra-low-power applications. The proposed DLDO regulator has been fabricated in the 14nm FinFET CMOS process and occupied a $0.0035mm^2$ area, excluding an integrated output capacitor of 0.1nF. This regulator achieved a small FOM of 0.097ps and a quiescent current of 0.69μA.

Arvind Singh [33] et al. proposed a transient enhanced DLDO regulator with an all-digital auto-tuning engine and dynamic gain control circuit for feedback compensator that performs well under load changes, aging, passive and process variations. The proposed design improved transient performance for aging-induced degradations by 30% and showed a 110% improvement under process variations. The test chip has been fabricated in 130nm CMOS with a chip area of $0.85mm^2$. This design achieved a maximum current efficiency of 97.8% with a settling time of 55ns for a load change from 5mA to 45mA in 0.1ns.

Ki-Chan Woo [34] et al. proposed a transient enhanced coarse-fine dual loop-based DLDO regulator to reduce the output ripple voltage without V_{OUT} ringing in the transient state. To avoid ringing in the transient state and ensure a fast transient response, an auxiliary power stage consisting of an auxiliary power PMOS array and an auxiliary shift-register has been used. This DLDO is designed in 65nm CMOS technology and achieved a low ripple voltage of 3mV. For a load change from 10mA to 100mA with an edge time of 20ns, this design achieved overshoot and undershoot voltages of 47mV and 23mV, respectively. The settling time has been reduced to 130ns, with a quiescent current consumption of 75μA.

Yongfu Li [35] et al. proposed a low quiescent current DLDO regulator for near- and sub-threshold V_{SUP} operations in low-power wireless sensor applications. This DLDO regulator's control logic used hill-climbing and binary search algorithms to improve transient response and reduce ripples and spikes on the V_{OUT}. The hysteresis and freeze mode controls, along with a proposed dynamic comparator, have been used to improve the regulator's performance even further and reduce the quiescent current at steady state. This DLDO regulator achieved 99.9% current efficiency while consuming 8.9µA quiescent current with V_{SUP} at 0.5V. With load and line regulations of 0.6mV/mA and 1.6, respectively, a power efficiency of 89.9% has been achieved.

Guigang Cai [36] et al. presented a fully integrated DLDO regulator that uses adaptive current step size control to achieve a high transient response speed with improved output dc accuracy. Power transistors are divided into ten blocks in this design, with each block containing a different transistor size. A low ripple V_{OUT} is regulated by turning on and off the small-sized power transistors at a steady state. Larger power transistors, on the other hand, provide quick V_{OUT} recovery during instant load changes. An auxiliary block made up of power NMOS and PMOS transistors is used to reduce limit cycle oscillation during light load conditions and improve transient response. The proposed design, manufactured in a 65nm CMOS process, achieved a current efficiency of 99.96% with a quiescent current of 34.6µA. This prototype achieved undershoot and overshoot voltages of 53mV and 37mV, respectively, for a load step of 100mA with V_{SUP} = 0.6V and V_{OUT} = 0.5V. This unique design took up 0.17mm^2 of chip space, including a 1nF on-chip capacitor, and achieved a FOM of 0.183ps.

The DLDOs presented in [37-40] use time-based approaches to provide a regulated output voltage.

Somnath Kundu [37] et al. proposed a fully integrated, highly digital LDO regulator using a time-based approach. The conventional voltage quantizer is replaced in this prototype by a pair of voltage-controlled oscillators and a time quantizer. The presented DLDO regulator is implemented using a D-FF based beat frequency quantizer to generate the sampling clock. A variable clock frequency (f_{CLK}) is used to reduce power consumption at steady-state and achieve a fast-transient response when the load changes. An inherent active voltage positioning function has been employed to reduce the peak-to-peak voltage deviation. For functionality testing, this design is fabricated in a low power 65nm CMOS process with an active area of 0.0374$mm^{2,}$

including an on-chip capacitor of 40pF. With a minimum V_{SUP} of 0.6V, this DLDO regulator can deliver up to 100mA load current while maintaining the V_{OUT} at 0.4V. This DLDO recovers 108mV voltage droop caused by 50mA of load step within 1.24µs. This design has achieved a 1.38ps FOM and maximum current efficiency of 99.5%.

Tak-Jun Oh [38] et al. developed a time-to-digital (TDC) based DLDO regulator with a fast-transient response. Whenever an overshoot or undershoot is detected on V_{OUT}, this DLDO regulator increases its loop gain to improve its transient response speed. When the V_{OUT} stabilises, the loop gain returns to its nominal value. This DLDO regulator was built in a 110nm CMOS process and took up 0.04mm^2 of space. This prototype consumed 15µA quiescent current and had a maximum current efficiency of 99.98% with V_{SUP} = 0.7V. With a minimum dropout voltage of 100mV, this DLDO regulator can generate V_{OUT} ranging from 0.5V to 0.9V. When compared to a conventional DLDO regulator, the settling time is reduced by 60% without affecting the V_{OUT} at steady state.

Naoki Ojima [39] et al. used place & route (PnR) tools to implement a synthesizable DLDO regulator using a standard cell-based design flow. The difference between V_{OUT} and V_{REF} is converted into time delay difference, which is compared by a phase detector made up of a buffer and a D-flip-flop (D-FF). The PMOS transistor is designed and added to the standard cell library using the PnR tools. Except for the PMOS transistor and the output capacitor, this DLDO regulator is designed using Verilog code to make it synthesizable. The proposed DLDO regulator, fabricated in 65nm standard CMOS process, occupied an active area of 0.015mm^2. The transient response of 6.6µs has been observed for a load step of 5mA with V_{SUP} and V_{OUT} at 1V and 0.8V, respectively. This DLDO regulator has achieved a current efficiency of 99.6%, with 35.2µA quiescent current consumption.

Jeonghyun Lee [40] et al. used a single voltage-controlled oscillator (VCO) based edge-racing (SVER) time quantizer to implement a DLDO regulator with high transient speed and output dc accuracy. SVER changes the f_{CLK} dynamically in proportion to the output error voltage to achieve a fast transient response while consuming less power in the steady state. Furthermore, SVER employs a single VCO to reduce V_{OUT} error due to local mismatches. The proposed LDO regulator is fabricated in a 65nm CMOS process and has a current efficiency of 99% for load currents ranging from 3mA to 25mA with a maximum V_{OUT} deviation of 2mV.

[41-43] include various techniques in DLDO design to achieve dynamic voltage scaling.

Saad Bin Nasir [41] et al. demonstrated a wide dynamic range DLDO regulator that enables per-core dynamic voltage and frequency scaling (DVFS). This DLDO regulator employs an asynchronous non-linear control to achieve a fast-transient response during large load variations. The proposed DLDO regulator is fabricated in a 65nm CMOS process and can regulate V_{OUT} ranging from 0.15V to 1.15V. This regulator achieves a current efficiency of more than 99.5% while supplying a load current of 4mA and an output capacitor of 1nF.

Yen-Chia Chu [42] et al. proposed a transient enhanced DLDO regulator using auto-tuning algorithms. This DLDO regulator provides greater design flexibility in terms of dynamic voltage scaling (DVS), auto-tuning, and loop compensation techniques. This DLDO regulator is built in 0.18µm CMOS technology for performance testing. The V_{OUT} of this DLDO regulator can precisely perform DVS at various V_{OUT} levels (1/2, 5/9, 2/3, and 5/6 of the input voltage) for a wide input voltage range (0.9-1.8V). With an externally connected 1µF output capacitor, the V_{OUT} variations up to 50mV have been observed with a worst-case transient time of 2µs. This DLDO regulator can operate at peak efficiency in a variety of conditions.

Miguel E. Perez [43] et al. introduced a distributed and asynchronous LDO regulator to meet the power requirements of highly dynamic and high-power processors. With the help of a distributed network of LDO micro regulators, this paper presented novel methods for sensing and controlling the voltage error caused by a voltage drop on the power grid, allowing a processor to achieve better performance without using uneconomical guard banding. This regulator achieved 17 fast voltage transitions by adding a switched-capacitor accelerator to the charge pump of each micro regulator, resulting in power-efficient dynamic voltage and frequency scaling (DVFS). This design is fabricated in a 14nm CMOS process and occupied an area of $0.14mm^2$. The line and load regulations of 6.7mV/V and 1.5mV/A have been observed, respectively. The proposed design achieved a power and current efficiency of 89.9% and 98.5%, respectively, with a maximum power density of $91.1W/mm^2$.

The DLDOs proposed in [44-52] achieve a fast-transient response by using event-driven controllers.

Fan Yang [44] et al. presented a capacitor-less asynchronous DLDO to achieve a high transient speed over a wide load range of 0-500mA with V_{SUP} = 0.6V. This design used adaptive sizing with a row and column-based three-dimensional power-MOSFET stage. The design is shown to achieve a satisfactory resolution of ~9.5 bits (768 levels) with 5mV output ripple voltage. A

nanoseconds' transient response with 200mV/10ns reference voltage switching has been achieved with a 0.3mA quiescent current consumption at steady state. This DLDO is fabricated in a 65nm CMOS process and occupied an active area of 0.158mm^2.

Doyun Kim [45] et al. proposed an event-driven controlled fully integrated DLDO regulator with a time-coding scheme to reduce the size of the external load capacitor. A colossal load capacitor is generally connected externally to compensate for the variations in the V_{OUT} due to instant load changes. A high f_{CLK}, in addition to a large load capacitor, is required for the conventional DLDO regulator to respond quickly to large load variations, resulting in increased power consumption. This design added event-driven control to the DLDO regulator to reduce transient settling time when the V_{OUT} deviates from the V_{REF} beyond a certain threshold. With a low f_{CLK}, this DLDO regulator achieved a high transient response speed while consuming less dynamic power. With V_{SUP} = 0.5V, this regulator can provide the load current of up to 400µA while keeping V_{OUT} at 0.45V. The presented design achieved current efficiency of 96.3% with a worst-case voltage droop of 40mV using an on-chip integrated output capacitor of 40nF.

Fan Yang [46] et al. added a soft MSS and adaptive timing control to the DLDO regulator to improve load regulation. During MSS operation, the soft MSS control is used to ensure a smooth transition. Adaptive timing, on the other hand, aids in delivering a wide range of load current (up to 500mA) while keeping the V_{OUT} stable. In a 65nm CMOS process, this DLDO regulator achieved a load regulation of 0.15mV/mA with a minimum V_{SUP} of 0.6V.

Yuanqing Huang [47] et al. proposed a transient enhanced DLDO regulator with asynchronous-flash (AF) coarse tuning. To maintain dc accuracy, the unary-weighted power MOSFETs have been fine-tuned at a low f_{CLK} via a bidirectional shift register. After fine-tuning, a freeze mode is implemented at steady-state to further reduce power consumption. During a load change, the AF coarse loop controlled the binary-weighted power MOSFETs to provide a fast-transient response. The proposed prototype is fabricated in a 28nm CMOS process and can supply a load current up to 33mA while consuming a quiescent current of only 10.5µA. This DLDO regulator can regulate V_{OUT} = 0.45V with V_{SUP} = 0.5V and achieve a 0.11ps FOM with 102mV voltage undershoot for 30mA/20ns load step.

Doyun Kim [48] et al. proposed an event-driven LDO regulator with self-triggering control to address two major shortcomings of conventional event-driven LDO regulators: long settling time and low current density. With a V_{SUP} (min) = 0.5V, the dropout voltage is measured as 50mV.

This LDO regulator is fabricated in 65nm CMOS technology with an output capacitor of 0.1nF. This regulator outperformed the previous event-driven and time-driven LDO regulators in terms of settling time, droop voltage, output capacitor size, and current density.

Jun-Eun Park [49] et al. added an event-driven digital control based on a residue-tracking loop to the DLDO regulator to support high load current requirements while maintaining the dc accuracy. A latch-based shift register is used to further improve the dc accuracy during large variations in load current. This DLDO regulator is built in 65nm low power CMOS technology and includes a 0.1nF output capacitor on the chip. The results showed less than 1.1% voltage variations on V_{OUT} for V_{SUP} ranging from 0.5V to 1V. This design achieves a load regulation and FOM of 0.1mV/mA and 6.74fs, respectively.

Lei Zhao [50] et al. proposed a power-efficient dual loop-based DLDO regulator with combined synchronous and asynchronous (CoSA) logics for fast transient response. The coarse loop is based on a two-step logic, react-then-write, and is enabled during large load variations to improve the transient response speed. To reduce the settling time even further, the coarse loop used true single-phase clock (TSPC) dynamic latches along with a continuous-time self-biased comparator to detect the V_{OUT} droop. The proposed DLDO regulator is implemented in a 28nm bulk CMOS technology and occupied an active area of 0.019mm^2, including an integrated 150pF output capacitor. The overshoot and undershoot voltages are 45mV and 56mV, respectively, for load switching between 5mA and 25mA within 10ns.

Nghia Tang [51] et al. analyzed that the capacitor-less ALDOs provide a better PSRR whereas capacitor-less DLDO (CL-DLDO) are more power-efficient and scalable. This paper presented a capacitor less DLDO with an analog PSRR enhancer to achieve the benefits of the CL-DLDO regulator while maintaining PSRR. To achieve a fast transient response, an asynchronous digital feedback controller is used, while PSRR has been improved by using a wide-bandwidth analog controller that is independent of load changes. This regulator is fabricated in 130nm and occupied a 0.0645mm^2 active area. This prototype can deliver a load current of up to 50mA while maintaining V_{OUT} = 0.8V with V_{SUP} = 1V. With a better PSR for frequencies up to 10MHz, the design achieved a peak current efficiency of 99.3%.

Khondker Zakir Ahmed [52] et al. modified the DLDO regulator with an event-driven computational controller to support a wide load range of 400A to 2A. The control mechanism determines the exact number of power gates required to achieve a fast-transient response

independent of V_{REF} and load transients, as well as the value of the output capacitor. The digital implementation of the control mechanism makes it fast and synthesizable. The results showed that this design achieved a less than 20ns settling time during load transients and provided fixed overshoot and undershoot voltages independent of the step size of load current.

[53-55] demonstrate DLDOs capable of regulating multiple different output voltages.

Salvador Carreon-Bautista [53] et al. presented a fully autonomous power management unit (PMU) to extract maximum power for DC-type energy harvesting sources (e.g., biomass, thermal, solar). The PMU includes a start-up circuit powered by harvested energy from renewable sources. A maximum power point tracking scheme is used to extract maximum power from renewable sources with low overhead power consumption. A capacitive dc-dc converter is used to perform the step-up operation on harvested energy to power the DLDO regulator and deliver a regulated V_{OUT}. This system is fabricated in 180nm CMOS technology and achieved a maximum end-to-end efficiency of 57% with an input power of 1.75mW.

Peter Hazucha [54] et al. reviewed that CMOS-based low-power microprocessors require multiple different V_{SUP} levels for their internal blocks – high voltage for I/O buffers, medium voltage for analog blocks, and low voltage for digital blocks. In this paper, an LDO regulator for generating multi-supply voltage levels was demonstrated in the 90nm CMOS process. This LDO regulator achieved a fast-transient response of 540ps at V_{SUP} = 1.2V and V_{OUT} = 0.9V.

Yasu Lu [55] et al. proposed a single-controller-four-output DLDO regulator to regulate four different voltage domains using adaptive-time-multiplexing control. The presented master digital controller has a 62% smaller area than the sum of the four independent controllers. A push-pull auxiliary loop and an analog-assisted loop take over control at steady-state to reduce quiescent current and improve dc accuracy and transient response. This design in 65nm CMOS technology achieved an undershoot voltage of 100mV for a load change of 47mA with a 20ns edge time, yielding a FOM of 0.12ps.

[56-58] apply novel design strategies to improve the transient response of DLDO.

Chao-Chang Chiu [56] et al. added a resistance locked loop to the DLDO regulator to provide a load current of up to 200mA when V_{OUT} = 0.4V and V_{SUP} = 0.6V. This design consumes a quiescent current of 25.1μA to provide I_{OUT} = 200mA. It was demonstrated that the proposed DLDO regulator reduces switching noise by 77% when compared to a conventional DLDO

regulator. The proposed DLDO regulator in 40nm CMOS technology took up 0.0375mm^2 of chip area.

Sung-Won Choi [57] et al. presented a quasi-digital LDO (Q-DLDO) regulator for phase-change random access memory systems. A negative supply has been used to achieve an extremely fast transient response speed. The proposed Q-DLDO regulator employed a single power MOSFET similar to a conventional analog LDO regulator to regulate V_{OUT} = -3V with V_{SUP} at -3.2V. The gate node of a power MOSFET was controlled by digital adaptive currents, pull and push currents. In 180nm CMOS technology, this Q-DLDO regulator occupied a 0.041mm^2 active area and included a 3nF on-chip load capacitor. The voltage spike caused by an 80mA load change has been effectively reduced to 150mV. This prototype has achieved a FOM of 0.042V/µm^2.

Junyao Tang [58] et al. proposed a fully integrated pseudo-DLDO regulator for low power applications based on an NMOS power transistor. The feedback control loop is made up of three key components: latched comparator, charge pump, and resistor-capacitor (RC) network. The error voltage generated by the latched comparator is used to control the NMOS transistor's gate voltage via an RC network. This design's source follower configuration aided in achieving a high transient response speed by using only a 20pF on-chip output capacitor. This design occupied a 0.08mm^2 area in 0.18µm CMOS technology and can provide up to 100mA load current while consuming only 6.3µA quiescent current. This design is suitable for low power applications with limited area due to its low quiescent current and high-power efficiency.

2.1.1 COMPARISON

The performance parameters of LDO regulators that support low-voltage operation are summarised and compared in Table 2.1. The LDO design in [2] demonstrated a fast transient response while consuming a low quiescent current of 3µA, ensuring a reasonable high current efficiency. The TDC design used for the signal conversion makes this design complicated and less reliable for moderate f_{CLK}. The average load regulation provided by this design degrades further at the lower f_{CLK}. The power-efficient DLDO regulator proposed in [24] is appropriate for low-voltage battery-operated devices. The DLDO presented in [36] used an adaptive current step size to achieve a high load regulation of 36.8mV/mA. Despite its low voltage operation, it is not suitable for devices with a limited power budget.

Table 2.1. Performance comparison of various low voltage LDOs

Paper	**[21]**	**[24]**	**[28]**	**[29]**	**[50]**	**[52]**	**[59]**	**[60]**	**[61]**	**[62]**	
Architecture	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	ED	Analog	
Synthesizable	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	No	
Technology [nm]	65	28	65	130	28	22	65	130	65	65	
Active Area [mm^2]	0.034	0.021	0.01	0.114	0.019	0.165	0.012	0.114	0.029	0.16	
V_{SUP} [V]	0.5-1	1.1	0.6-1.1	0.5-1.2	0.6-0.65	0.55-1.2	0.5-1	0.5-1.2	0.5-1	0.2	0.6
V_{OUT} [V]	0.45-0.95	0.9	0.4-1	0.45-1.14	0.55-0.6	0.5-1.15	0.35-0.95	0.45-1.14	0.45-0.95	0.05-0.15	0.3-0.55
Max. I_{OUT} [mA]	12	200	100	4.6	5-25	0.4-2000	2.8	3	7.2-3511	0.1	50
I_Q [µA]	3.2	110	82	24-221	28	2400	45.2	24	12.5-216	0.41	32
f_{CLK} [MHz]	10	1000	500	100	10	200	12	10	200	1	1
Transient Time [µs]	1	10	0.7	1	10	80	0.037	3	80	-	
Load Reg. [mV/mA]	2.3	120	0.06	10	20	0.2	46	10	100	34.8	133.9
Current Efficiency [%]	95.5	99.94	99.92	98.3	99.6	99.76	98.4	98.3	96.3	99.59	99.93
FOM [ps]	0.23	7.75	0.43	36	0.59	0.198	67.1	0.0765	1.11	227.8	1.68

[44] shows a low-voltage ALDO regulator capable of regulating 0.2V, but it has reliability issues due to device mismatch. The research work in [52] proposed and introduced a computational controller to the DLDO in order to achieve a fast-transient response. As an added circuit to the DLDO, the computational controller design increased the overall quiescent current consumption. A novel event-driven architecture has been used in [53] to achieve a fast response time. The current efficiency of this event-driven LDO is observed to be low.

The low-voltage operation of LDO regulators can reduce power consumption and increase battery backup of IoT devices [4]. For harvested energy management systems, ultra-low-power CMOS circuits are indispensable. As device sizes shrink below 14nm, power management needs to become more adaptive and intelligent in order to control dynamic and leakage power dissipation. Low voltage operation is one method of increasing the power efficiency of a circuit. Analog circuit performance degrades at lower V_{SUP} levels due to insufficient voltage headroom required for transistors to operate in the saturation region. However, digital circuits, such as application processors or multi-core processors, can perform well under low voltage conditions by operating transistors in a linear region. An LDO regulator was first proposed in [22] using a digital approach to regulate a sub-threshold voltage of 0.45V. The use of digital and analog design techniques can improve an LDO regulator's performance at sub-threshold voltage levels.

2.2 GAPS IN THE STUDY

ALDOs fail to operate at lower supply voltages because each transistor requires a voltage headroom based on the operation. The operation of VLSI circuits at very low voltages is effective in reducing both dynamic and leakage power. At low power supply voltage, the maximum energy efficiency is achieved. Designing an LDO using digital approach is one way to make it operational at lower supply voltages. Several studies have been conducted in this domain, with the goal of identifying new ways to compete with the performance of ALDOs. The following gaps are identified after studying various architectures used in the design of low-voltage LDO regulators:

- A system that uses the dynamic voltage and frequency scaling (DVFS) scheme, such as a portable device that can run for days on a small battery, needs to run most of its modules on low voltage levels. During standby mode, several of these modules are run at a supply voltage of less than 50 mV. These modules are powered by LDOs through a global supply

rail V_{SUP}. Designing an LDO becomes more challenging when V_{SUP} is altered by external noise, which can cause it to vary over a large range.

The work in [59] presented an analog-based LDO that generates a low voltage output. The output produced by this design is unstable and varies between 0.05V and 0.15V, which is not suitable for a supply-sensitive circuit. Also, powering a circuit with a highly variable supply not only affects its performance, but also contributes to increased power consumption. When designing a low voltage LDO, providing an accurate and stable output becomes a major challenge.

- Existing DLDOs are slow to respond to large current steps, especially at low voltages. Slow response can be mitigated by increasing f_{CLK}; however, this comes at the expense of increased power consumption and, more importantly, decreased loop stability. The work in [60] solves this problem by employing an asynchronous shift register rather than the more common synchronous shift register. However, the circuit operation is too sensitive to PVT variation to achieve consistent performance across chips.
- Load current dynamics are common, especially when dealing with digital circuits, which can consume tens of nanoamperes during standby and hundreds of milliamperes during normal operation. The system compensation should ensure that the LDO is stable and has good settling characteristics regardless of load current dynamics. The dynamic range of a DLDO is limited by the number of bits in its UP/DN counter. DLDO output may take longer to settle down during large load transitions. Existing DLDOs have a limited dynamic range over which the load can be regulated and stable [9, 21, 23, 58-59].
- Existing LDOs are being developed using mixed-signal or fully analog design approaches. In the literature review, it has been observed that the implementation of a digital LDO can reduce design time and provide much better performance at near threshold voltage levels. Digital LDOs can be further explored to make them fully synthesizable and further reduce design time.
- Digital LDOs in the literature use clocked comparator, time-to-digital converter (TDC), or 1-bit ADC [104–106] to monitor V_{OUT}. Using analog circuitry increases manual work and potentially design time. The digital implementation of the output monitoring circuit can be investigated.
- Existing digital LDOs use power MOSFETs to drive the load, contributing to the proliferation of analog components.

- Most digital LDOs introduce ripples in the V_{OUT} at steady-state due to its digital control. Energy-efficient and supply-sensitive circuits require a precise ripple-free power supply.
- To control the current supplied to the load, most digital LDOs use large bidirectional shift registers, which generate high leakage current and make them unsuitable for low-power applications.

2.3 OBJECTIVES

Following a review of the literature and the inspiration provided by research gaps, the following research objectives are created:

1. To propose a digitally controlled LDO design to generate very low voltage level (0.5V).
2. To design and characterize the proposed LDO to enhance its transient settling time.
3. To develop a design technique to compensate changes in V_{OUT} due to large variations in load current while moving from no-load to full-load.

CHAPTER 3

FULLY-SYNTHESIZABLE CLOCKED COMPARATOR

3.1 INTRODUCTION

This chapter proposes a high-speed low-power clocked comparator for digital low dropout regulator. The fast-transient response of the proposed comparator at a low V_{SUP} of 0.5V makes it suitable for high-speed ultra-low power designs.

Clocked comparators are well known for their low power requirements and are widely used in a variety of applications such as voltage regulators, analog-to-digital converters (ADCs), and sensor circuits. The growing interest in battery-powered IoT and portable mobile devices has promoted the research on low voltage operation of clocked comparators [6, 51, 64]. Recently, the clocked comparators have been explored extensively to make them suitable for ultra-low-power designs [64-68]. The comparators, designed using the traditional analog approach, need a supply voltage higher than the transistor threshold voltage (V_{TH}) for their operation [69-70]. When the supply voltage drops below V_{TH}, the analog comparators fail to maintain the minimum voltage margin across the transistors to keep them in saturation mode, resulting in overall performance degradation.

Designing a high-speed analog comparator becomes more challenging at sub-threshold supply levels. In a specific technology, the operating speed can be increased by using large transistors to compensate for the low supply level, but this comes at the expense of a larger area and increased power budget. Additionally, the traditional analog-based comparators support a limited input common-mode voltage (V_{CM}) range at low supply levels. To overcome these design challenges at low supply levels, many design approaches, such as supply voltage boosting techniques [71-72], body-driven devices [73-74], current mode designs [75] have been adopted. The bootstrapping and boosting techniques rely on boosting the reference, clock, or V_{SUP} to deal with switching issues and V_{CM} range limitation. Though these techniques are useful, but not reliable at lower CMOS technology nodes. In [73], body-driven MOSFET transistors are used as depletion-type devices to operate at low V_{SUP} levels by reducing the V_{TH} level. Following this approach,

[74] proposed a 1-bit quantizer for low voltage modulators. Despite many advantages of body-driven MOSFETs, these devices have a smaller transconductance and need to be fabricated through a unique deep n-well process. [76-78] improves the speed of the traditional dynamic comparator by using additional circuitry. The comparator presented in [76] can operate at V_{SUP} levels down to 0.5V and consumes only 18μW power, but the device mismatch in the additional circuitry used makes it less reliable. These circuits are designed in a full-custom manner and placed separately from their associated standard-cell modules at the full-chip level, necessitating additional effort to establish their interconnections [79].

3.2 EXISTING FULLY-SYNTHESIZABLE CLOCKED COMPARATORS

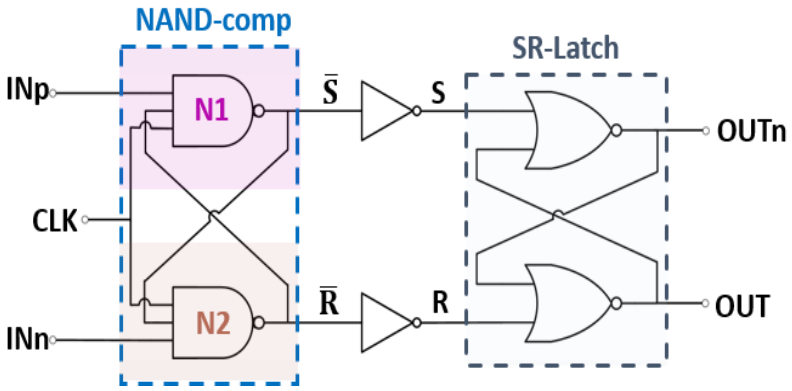
To address the above discussed limitations of analog comparators at low supply levels, the first-ever fully-synthesizable low-voltage clocked comparator was presented in [79]. This design is comprised entirely of CMOS standard cells, which makes it fully-synthesizable. Despite the advantages, this circuit cannot support a lower level of V_{CM}, limiting its applications.

To accommodate lower V_{CM} levels, the work in [80] employs a pull-down network (PDN). When the input V_{CM} level is low, the large current flowing through the PDN balances the current supplied by PMOS devices. The PDN strength needs to be chosen carefully. The strength that is either too low or too high fails to bring the output voltage to the supply rails. In [81], various sets of comparators with different V_{CM} levels are used to broaden the input V_{CM} range and make it suitable for a wider range of applications. The [79-81] architectures support a limited V_{CM} range since they require a sufficiently high V_{CM} level to ensure that the PMOS transistors, connected to the inputs, are in cut-off state.

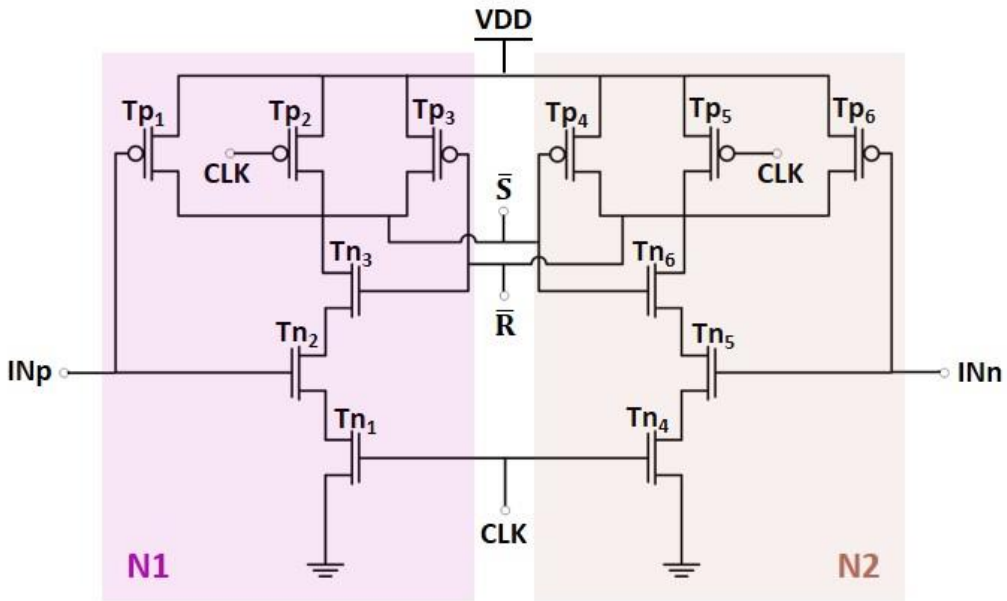
The work in [82-84] combines the NAND and NOR gate-based comparators to support extended V_{CM} range at the expense of increased surface area and power consumption. When input V_{CM} is ~$V_{SUP}/2$, these designs do not produce expected results. Two unique comparator architectures derived from OR-AND-INVERTER logic gates are demonstrated in [85]. These architectures are incapable of handling rail-to-rail V_{CM} levels and have a high input offset voltage. Therefore, it is necessary to investigate a novel all-digital comparator architecture with enhanced characteristic parameters which can support a wider V_{CM} range. This chapter presents a unique prototype that can operate at sub-threshold voltage levels down to 0.3V and support rail-to-rail V_{CM} inputs. The proposed comparator consumes a maximum power of 0.033μW, which makes it suitable for ultra-low-power designs.

As shown in Fig. 3.1(a), the clocked comparator in [79] employs two cross-coupled NAND3-gates (NAND-COM) and an SR latch. When the clock (CLK) is set to logic high, the comparator enters the sampling phase and compares the input signals INp and INn. The NAND-COM outputs, $\bar{\mathbf{S}}$ and $\bar{\mathbf{R}}$, control the levels of OUT and OUTn via an SR-latch.

When CLK is set to zero, the comparator enters the hold phase and stores the sampled NAND-COM outputs in the SR-latch. This prototype performs excellently for input V_{CM} levels close to V_{SUP}. This circuit is only suitable for a few applications, such as stochastic flash ADC [79].



(a)



(b)

Fig. 3.1. (a) The gate-level and (b) transistor-level circuit diagram of clocked comparator presented in [79].

Fig. 3.1(b) shows the transistor-level diagram of the comparator circuit presented in [79]. This design can produce the expected outputs when input signals INp and INn are high enough to keep the PMOS transistors, Tp1 and Tp2 in their cut-off states. When CLK = 0, the outputs $\overline{S}$ and $\overline{R}$ are pre-charged to V_{SUP}, regardless of INp and INn levels. As CLK rises to V_{SUP}, the comparator enters the sampling phase and the signals $\overline{S}$ and $\overline{R}$ begin to discharge through PDNs of N1 and N2 gates, respectively. Assuming there is no device mismatch, the capacitive loads at the nodes $\overline{S}$ and $\overline{R}$ are almost equal since the design is symmetrically connected. With equal capacitive loads at output nodes of N1 and N2 gates, the discharge rate of $\overline{S}$ and $\overline{R}$ is predominately determined by the signals INp and INn, which control the flow of current through Tn2 and Tn5 transistors of PDNs of NAND-COM. For INp>INn, the signal $\overline{S}$ is discharged at a faster rate than the signal $\overline{R}$. The cross-coupled connection between the N1 and N2 gates establishes positive feedback when the signal $\overline{S}$ drops below the threshold voltage of the Tp4 transistor and charges the signal $\overline{R}$ to V_{SUP}. The signals $\overline{S}$ and $\overline{R}$ are stored in SR-latch to generate the outputs OUT and OUTn, which remain unaltered when CLK = 0. For INp < INn, the comparator works vice versa.

This comparator works well when V_{CM} is close to V_{SUP} ensuring that Tp1 and Tp2 transistors remain in their cut-off states. At lower V_{CM} levels, the increased gate-source voltage, across the transistors Tp1 and Tp2, causes large drain currents to flow into the output nodes of N1 and N2 gates. The increased gate-source voltage makes the discharge rate of $\overline{S}$ and $\overline{R}$ too slow that INp and INn fail to pull either of them to the ground during the sampling phase. As a result, the signals $\overline{S}$ and $\overline{R}$ get stuck in their pre-charge state (V_{SUP}) at low V_{CM} levels. The simulation results show that this comparator does not produce the desired results when the input V_{CM} level drops below ~V_{SUP}/2.

To support a wider V_{CM} range, [82] employs two cross-coupled NOR3 gates (NOR-COM) along with the NAND-COM, as depicted in Fig. 3.2. A dual-input SR-latch is used to store the outputs of NAND-COM and NOR-COM. The performance of NOR-COM can be analyzed using its transistor-level circuit diagram. The simulation results show that NOR-COM works well for the lower V_{CM} levels.

At high V_{CM} levels, the NOR-COM fails to raise the potential of signals S1 and R1 from the ground to V_{SUP}. Thus, S1 and R1 get stuck at the ground level even during the sampling phase. In other words, the NOR-COM can produce a valid output for the V_{CM} levels close to the ground.

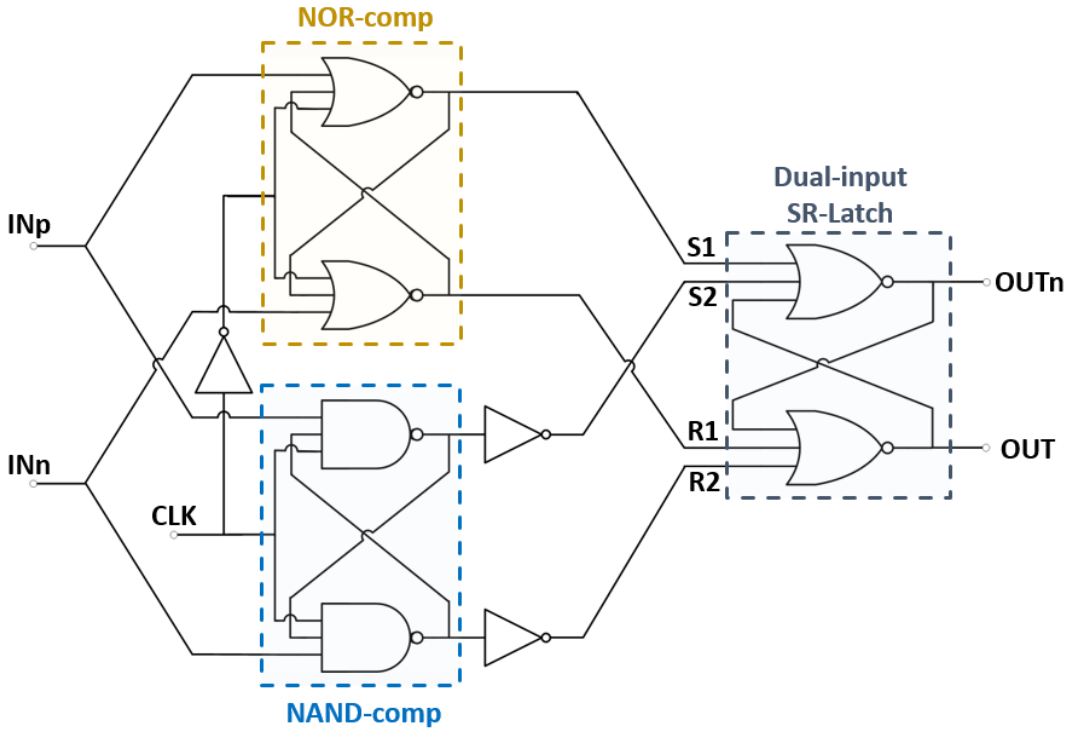


Fig. 3.2. The gate-level circuit diagram of all-digital comparator circuit [82].

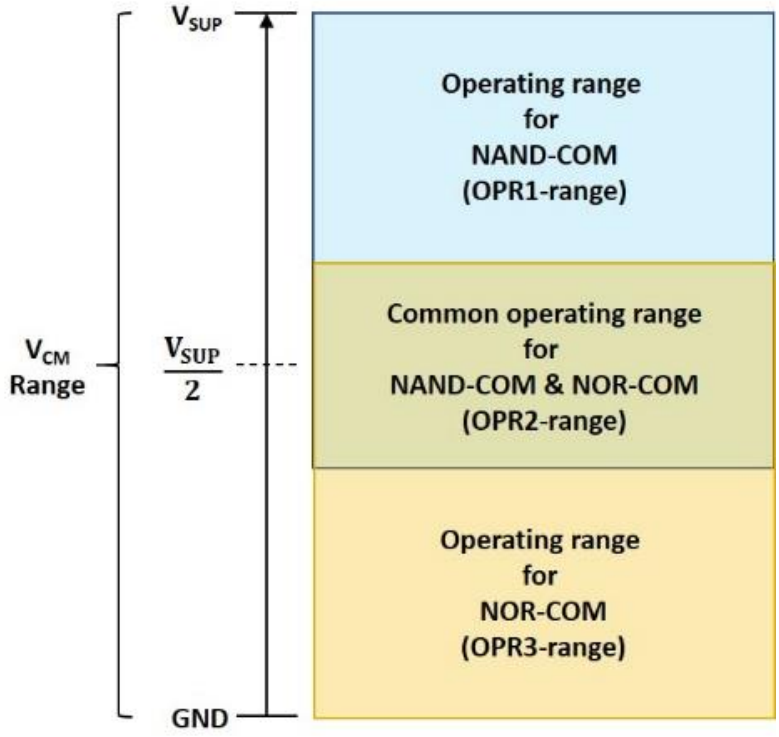


Fig. 3.3. The operating ranges for NAND-COM and NOR-COM.

In contrast, it fails to generate desired results at higher values of V_{CM}. The simulation results show that the NOR-COM can produce valid outputs when V_{CM} is lower than the ~V_{SUP}/2 level.

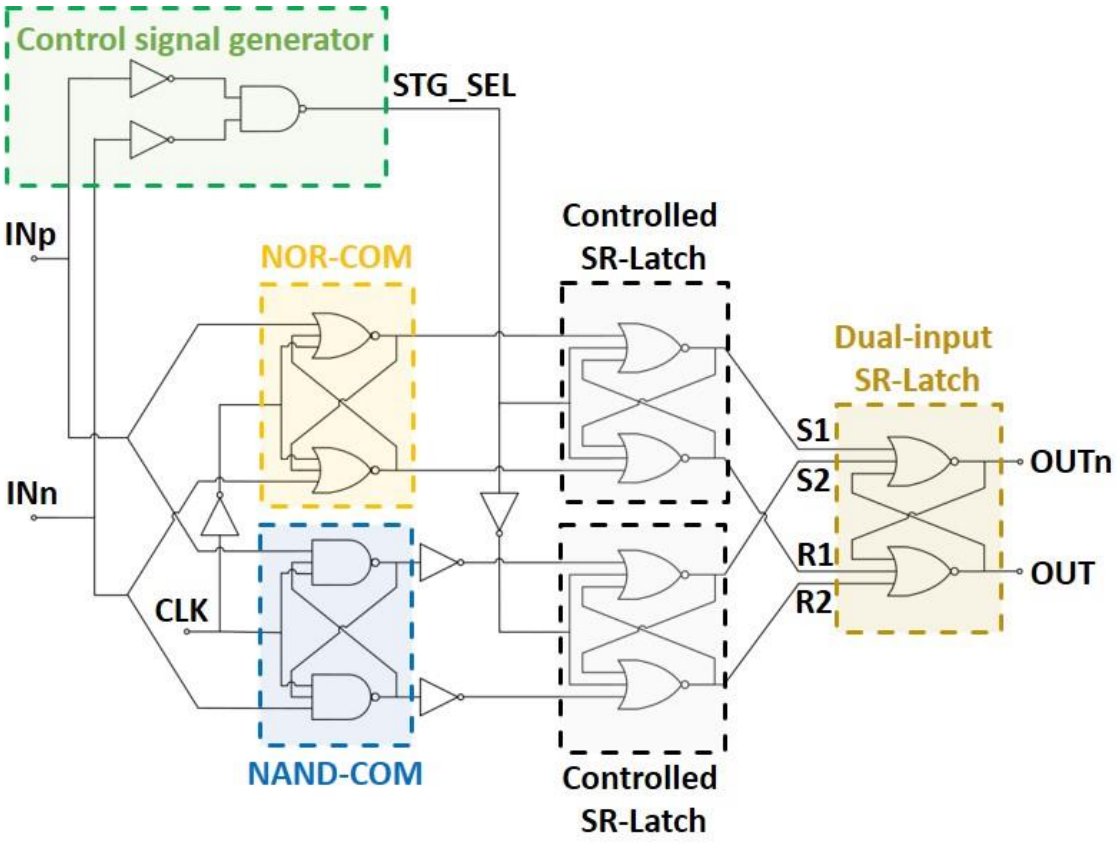
The entire V_{CM} range can be divided into three different operating ranges for NAND-COM and NOR-COM to produce valid outputs, as shown in Fig. 3.3. For the V_{CM} range close to V_{SUP} (OPR1-range), only NAND-COM can produce correct results, while the NOR-COM outputs remain at ground level. Since the OPR3-range is close to the ground level, the NOR-COM can generate valid outputs, and the NAND-COM outputs remain at the V_{SUP} level. The OPR2-range near V_{SUP}/2 presents the overlap between OPR1-range and OPR3-range, where both NAND-COM and NOR-COM can produce valid results.

The comparator in [82] works well for the V_{CM} levels lying in the OPR1-range and OPR3-range but does not provide adequate results in the OPR2-range. Under the OPR1-range, the outputs OUT and OUTn are determined by NAND-COM through dual-input SR-latch, while the signals S1 and R1 rest at their pre-charge state (ground). Similarly, for V_{CM} levels that lie in the OPR3-range, the outputs of NOR-COM decide OUT and OUTn, while the outputs of NAND-COM remain in their pre-charge state, i.e., V_{SUP}, causing S2 = 0 and R2 = 0. In OPR1-range and OPR3-range, only one stage, either NAND-COM or NOR-COM, determines the final output while the other remains in its pre-charge state.

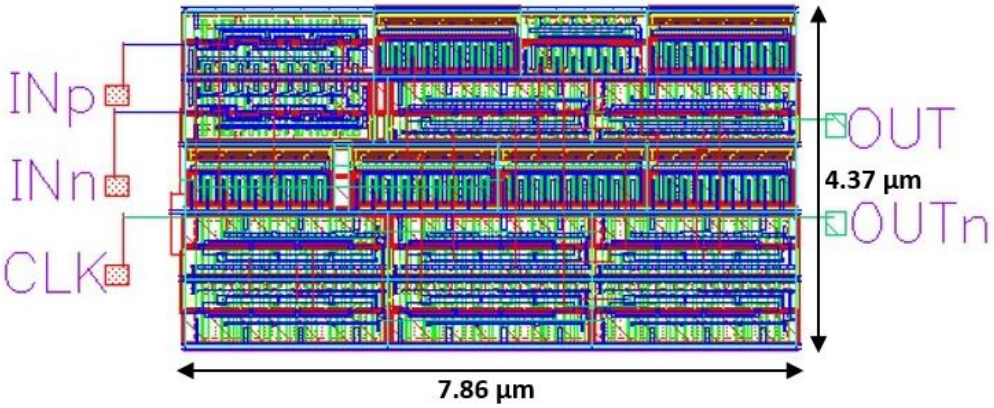
For the V_{CM} value lying in the OPR2-range, both NAND-COM and NOR-COM produce valid outputs and set the OUT and OUTn signals to an undesired output state. When INp>INn, NOR-COM causes S1 = 0 and R1 = 1, and NAND-COM causes S2 = 1 and R2 = 0, forcing both OUT and OUTn to ground. Similarly, for INp<INn, OUT and OUTn are forced to V_{SUP}, which is also an undesirable output condition.

3.3 FULL-SWING FULLY-SYNTHESIZABLE VOLTAGE COMPARATOR

A novel architecture for the clocked comparator is presented to overcome the limitations of all-digital comparator circuits while preserving its synthesizability. The proposed circuit can process rail-to-rail V_{CM} levels and operate at a V_{SUP} down to 0.3V. The proposed prototype employs NAND-COM and NOR-COM stages, control signal generator, controlled SR-latches and a dual-input SR-latch as shown in Fig. 3.4(a).



(a)



(b)

Fig. 3.4. The proposed architecture of the fully-synthesizable comparator. (a) Its gate-level circuit diagram and (b) Its layout.

3.3.1 The control signal generator (CSG)

This CSG enables NAND-COM and NOR-COM by determining the levels of input signals. The CSG employs NOT and NAND2 standard cells to derive a control signal, STG_SEL, to control the latch operation of NAND-COM and NOR-COM output signals with the help of controlled SR-latches. The STG_SEL signal maintains the comparator's functionality by enabling only one controlled SR-latch to set a valid output state for OUT and OUTn, even when VCM falls under the R2 region. The typical value of the switching threshold (Vt_{INV}) of INV gate is around $V_{SUP}/2$. The variations in Vm across the process corners have no impact on the comparator's performance as long as its value lies within the R2 region.

3.3.2 Working

For INp and INn larger than Vm, i.e., INp>Vm and INn>Vm, the STG_SEL is set to V_{SUP} that allows NAND-COM to decide the levels of outputs OUT and OUTn. Simultaneously, the STG_SEL = 1 forces S1 and R1 to ground through controlled SR-latch to nullify the impact of NOR-COM on OUT and OUTn. Similarly, when both INp and INn are lower than Vm, the STG_SEL gets set to ground. The STG_SEL = 0 forces S2 and R2 to ground, and permits NOR-COM to fix the levels of OUT and OUTn through S1 and R1 signals.

For the V_{CM} levels falling under the OPR2-region, both NAND-COM and NOR-COM can generate valid outputs; hence CSG can be designed to allow either NAND-COM or NOR-COM to regulate the OUT and OUTn signals. The operating speed of NAND-COM is observed to be much faster than that of NOR-COM. Thus, for the V_{CM} lying within the OPR2-region, the CSG is designed to choose the NAND-COM for governing the outputs OUT and OUTn.

3.3.3 Results and analysis

The proposed comparator is designed and synthesized using a 45nm CMOS process starting from its Verilog description. The proposed prototype can be conveniently integrated with other digital blocks through Verilog coding. The layout generated by using automatic PnR tools occupies 138μm^2, as shown in Fig. 3.4(b). The effect of input offset voltage can be minimized by using high strength logic gates [77, 83] with increased area and power budget. As the proposed design comprises a limited number of logic gates, it is worth compromising with area and power to achieve a low input offset voltage and an excellent overall performance. The logic gates with the

highest strength available in standard cell library are used by explicitly mentioning them in Verilog code.

Although the proposed comparator can be synthesized from a Verilog code, the digital synthesizer treats this circuit as a digital one. It may replace its logic gates during design optimization while maintaining the digital functionality as per the code, but the optimized circuit may fail to produce the analog perspective results. To avoid undesirable changes in the proposed design caused by the optimization process, the synthesis command "set_dont_touch comparator" or equivalent can be used [76].

The proposed design has been verified for its robustness across the supply voltage ranging from 0.3V to 1.8V through post-layout simulations. However, the comparator has been built with the purpose of being used in proposed digital low-dropout regulator with a V_{SUP} as low as 0.5V. The Fig. 3.5 shows the comparator output waveforms with the V_{CM} levels in the different operating regions of NAND-COM and NOR-COM at V_{SUP} = 0.5V. During STG_SEL = 1, the comparator outputs, OUT and OUTn, are determined by NAND-COM, else NOR-COM sets the comparator outputs.

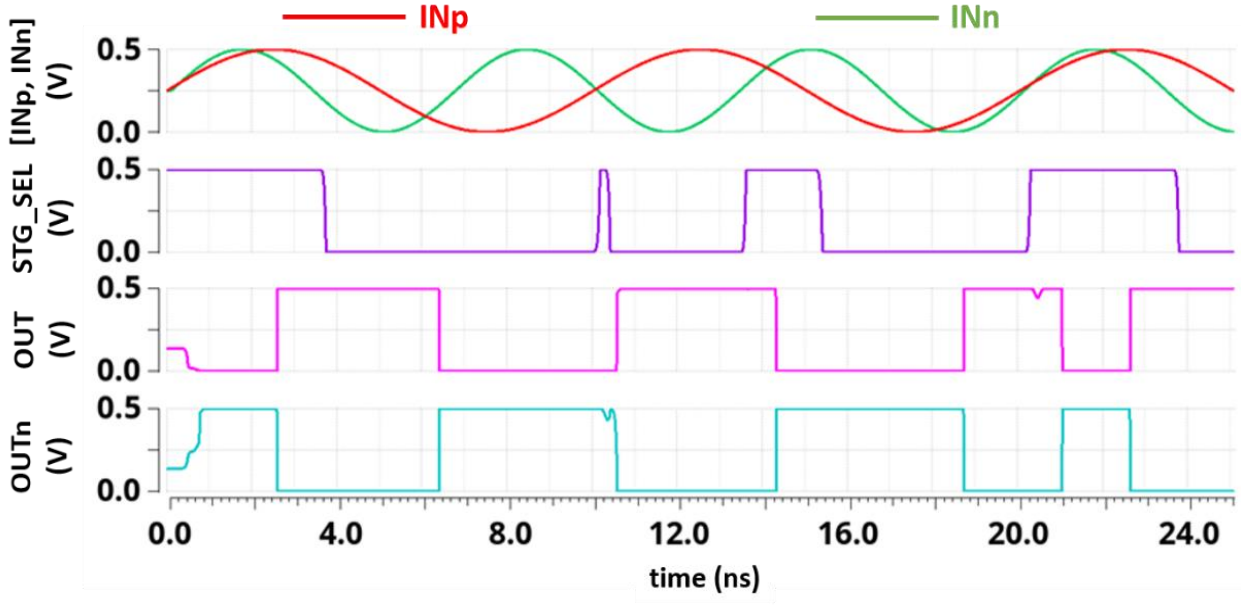
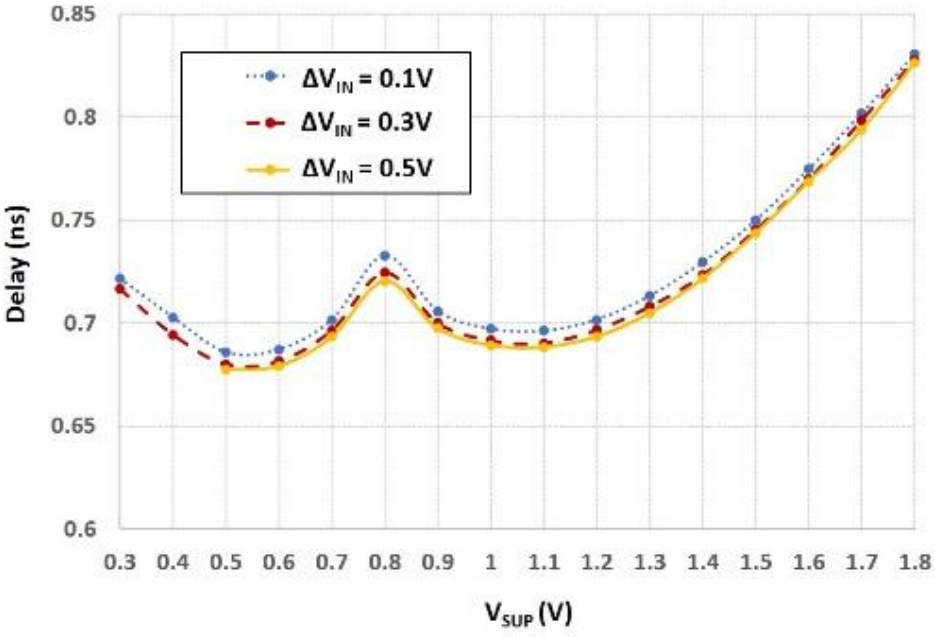
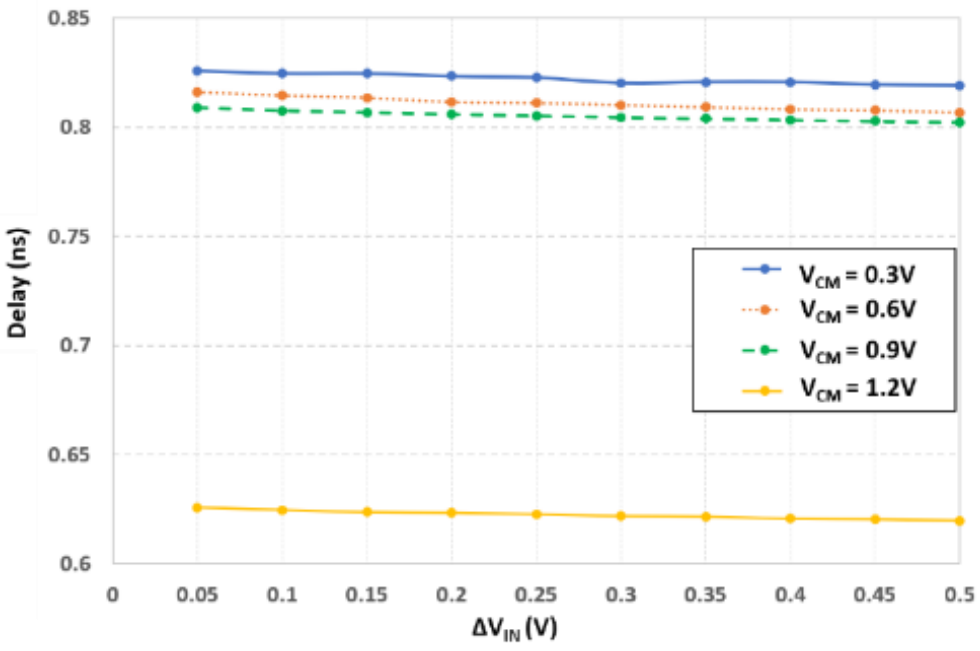


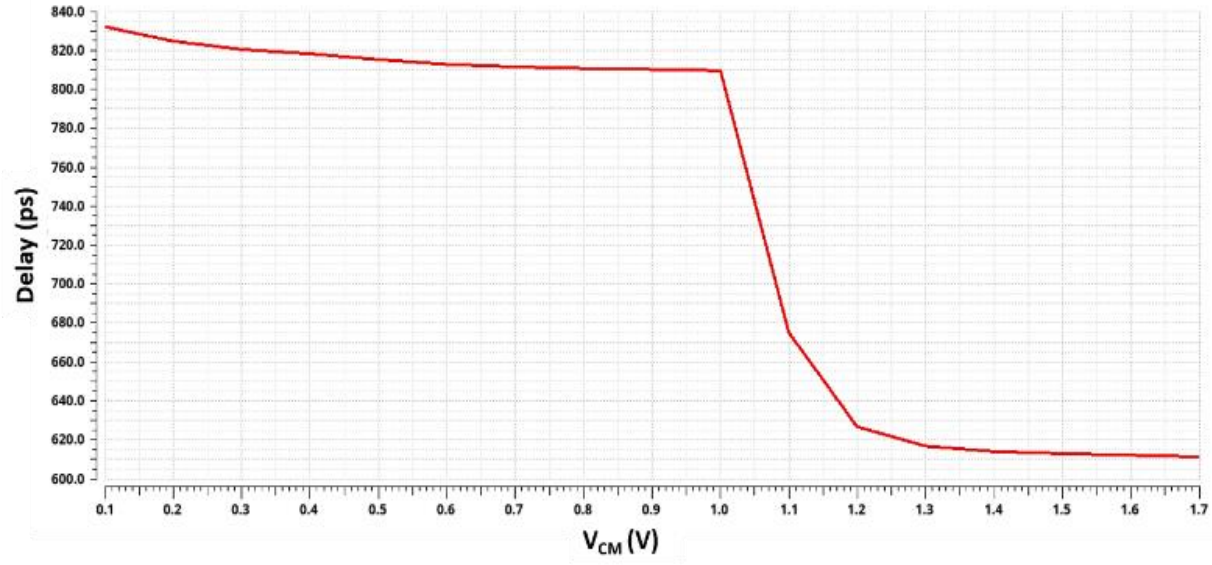
Fig. 3.5. Post-layout simulation waveforms at V_{SUP} = 0.5V.


0.85
0.8
0.75
0.7
0.65
0.6
Delay (ns)
ΔV_IN = 0.1V
ΔV_IN = 0.3V
ΔV_IN = 0.5V
0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8
V_SUP (V)

(a)


0.85
0.8
0.75
0.7
0.65
0.6
Delay (ns)
V_CM = 0.3V
V_CM = 0.6V
V_CM = 0.9V
V_CM = 1.2V
0 0.05 0.1 0.15 0.2 0.25 0.3 0.35 0.4 0.45 0.5
ΔV_IN (V)

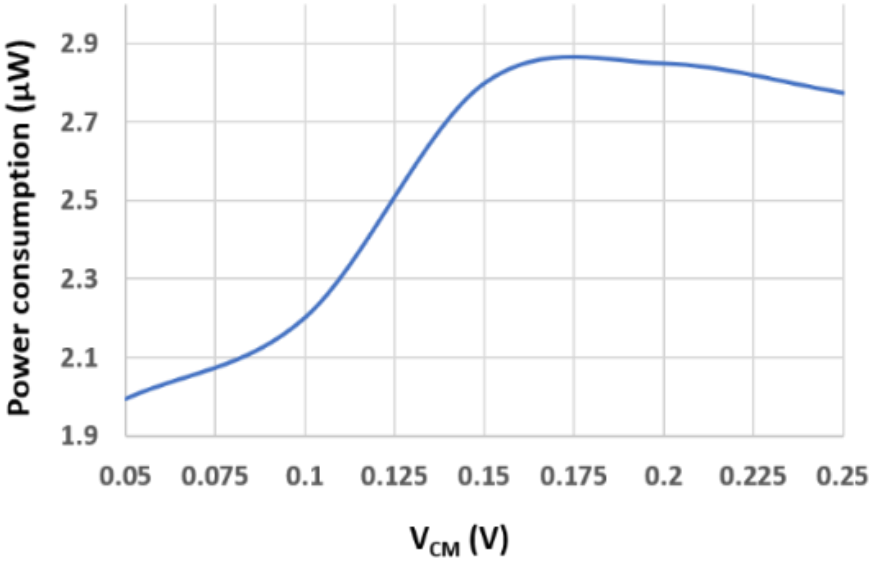
(b)



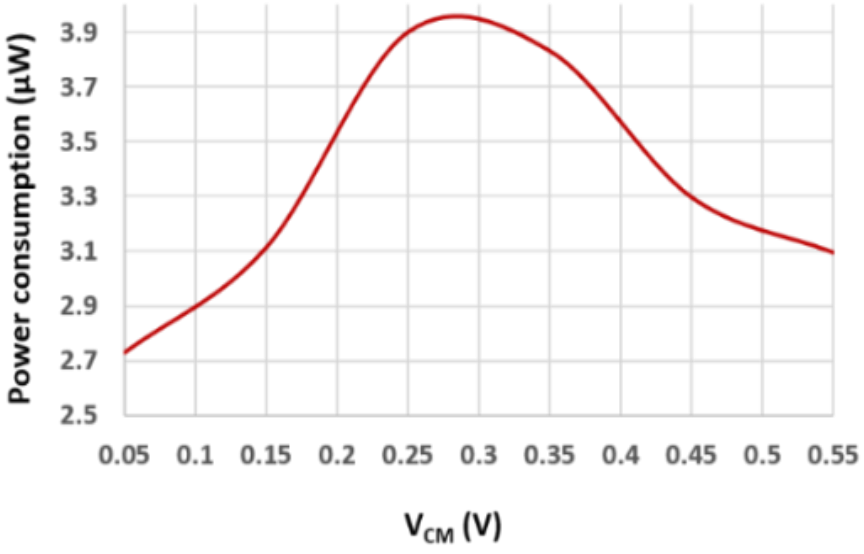
(c)

Fig. 3.6. Propagation delay characteristics of the proposed comparator (a) delay vs V_{SUP}, (b) delay vs ΔV_{IN} at V_{SUP} = 1.8V and (c) delay vs V_{CM} at V_{SUP} = 1.8V.

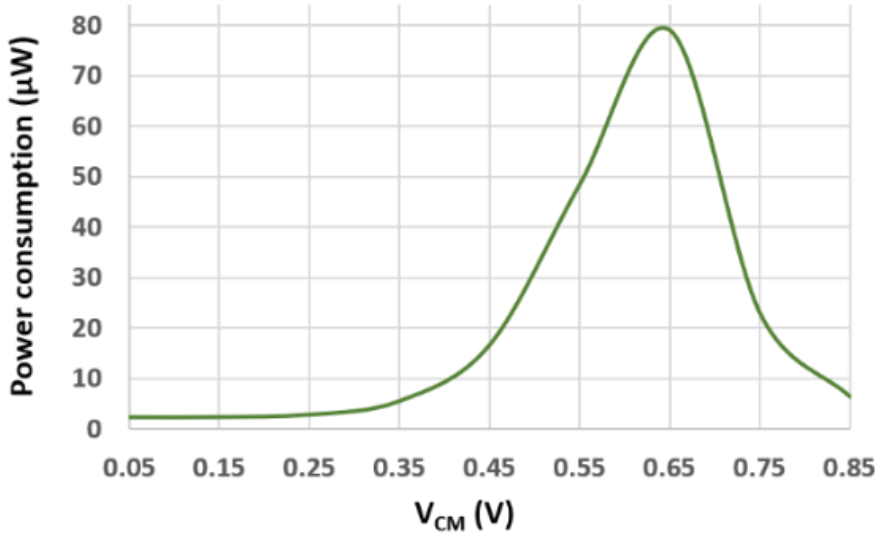
The clock-to-output propagation delay of the proposed comparator has been plotted and shown in Fig. 3.6(a) across the V_{CM} levels with differential input voltage (ΔV_{IN}) of 50mV at V_{SUP} = 1.8V. It is worth noticing that for the lower range of V_{CM}, NOR-COM evaluates the output state and results in significantly larger delays than the high values of V_{CM} where NAND-COM determines the output state. For a fixed value of ΔV_{IN}, the clock-to-output propagation delay for V_{CM} levels towards V_{SUP} is lower by at least 20% from the maximum delay across the entire V_{CM} range. The maximum delay of the proposed comparator for ΔV_{IN} = 50mV is observed to be 662ps, 705ps, and 830ps for V_{SUP} = 0.5V, 1.2V, and 1.8V, respectively. The propagation delay is high near lower levels of ΔV_{IN} and decreases as ΔV_{IN} increases, as depicted in Fig. 3.6(b). At a supply voltage level of 0.8V, the propagation delay is 732ps for ΔV_{IN} = 0.6V and drops to 722ps as ΔV_{IN} changes to 0.9V, which further drops to 719ps for ΔV_{IN} = 1.2V. The delay reduces by more than 4% as the supply voltage is increased to 1V. The maximum delay is achieved at V_{SUP} = 1.8V, as shown in Fig. 3.6(c).


Power consumption (µW)
2.9
2.7
2.5
2.3
2.1
1.9
0.05
0.075
0.1
0.125
0.15
0.175
0.2
0.225
0.25
V_{CM} (V)

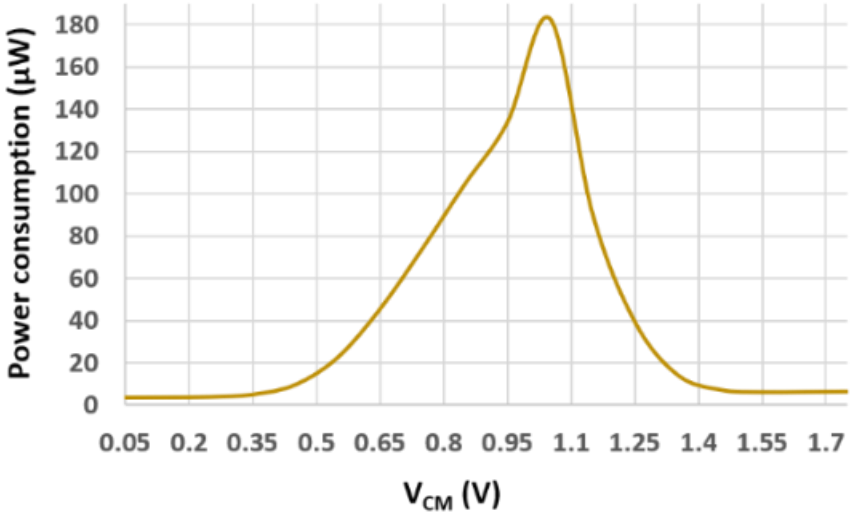
(a)


Power consumption (µW)
3.9
3.7
3.5
3.3
3.1
2.9
2.7
2.5
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.55
V_{CM} (V)

(b)



(c)

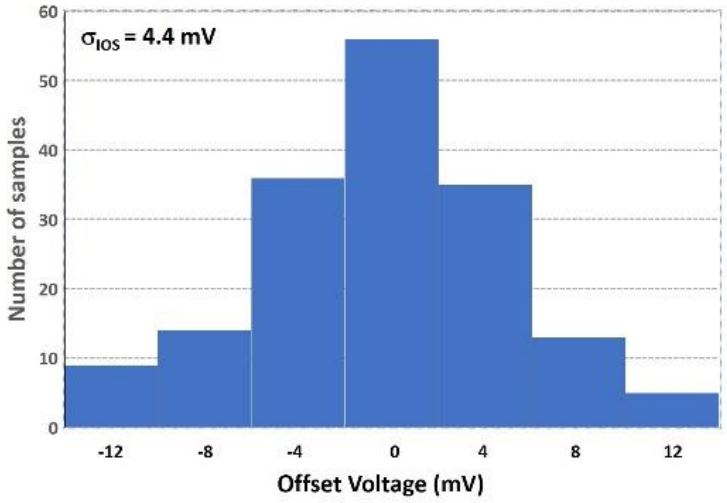


(d)

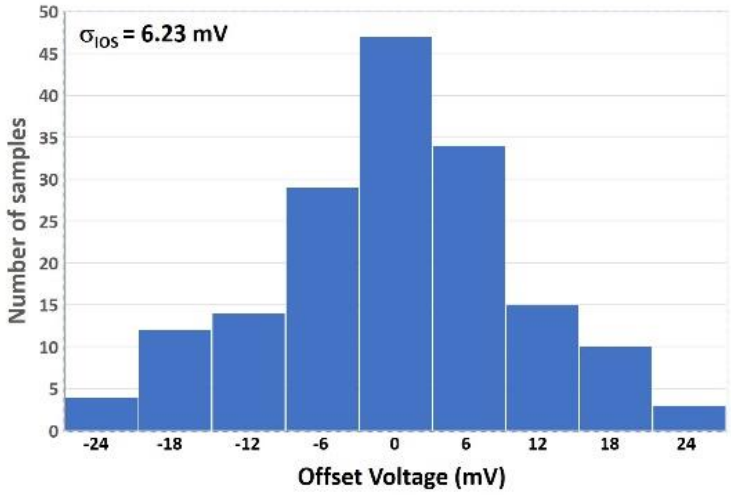
Fig. 3.7. Power consumption vs V_{CM} for ΔV_{IN} = 5mV at (a) V_{SUP} = 0.3V, (b) V_{SUP} = 0.6V, (c) V_{SUP} = 0.9V and (d) V_{SUP} = 1.8V.

The results reported in Fig. 3.7 shows that the power consumption is maximum for the V_{CM} levels falling under R2 region. Under R2 region, both NAND-COM and NOR-COM stay active to evaluate the final output that results in increased current consumption, whereas in other operating regions, only one comparator stage, either NAND-COM or NOR-COM, evaluate the outputs OUT and OUTn, while the other comparator stage remains in its pre-charge state. The maximum power consumption does not exceed 0.033µW, 3.9µW, 79µW, and 165µW at supply voltage levels of 0.3V, 0.6V, 0.9V, and 1.8V, respectively for ΔV_{IN} = 50mV.

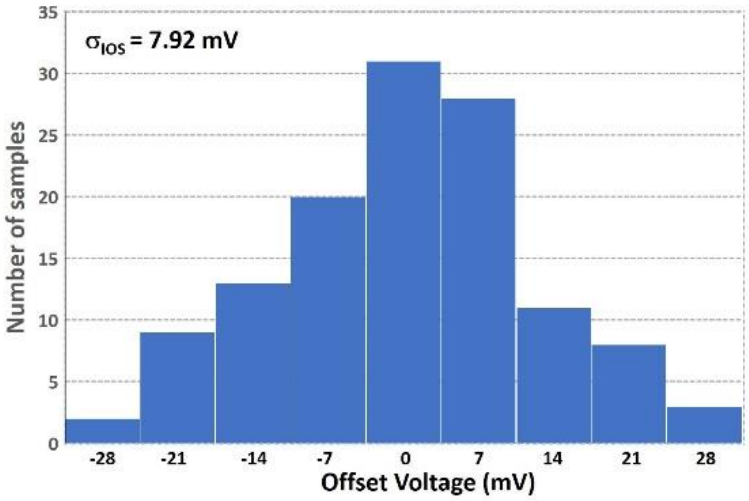
The proposed design is subjected to a Monte-Carlo analysis with 100 samples to determine its input offset standard deviation (σIOS) at various VSUP levels. The σIOS is found to be 4.4mV, 6.23mV, 7.92mV, and 8.01mV at VSUP = 0.3V, 0.6V, 0.9V, and 1.8V, respectively as illustrated in Fig. 3.8.



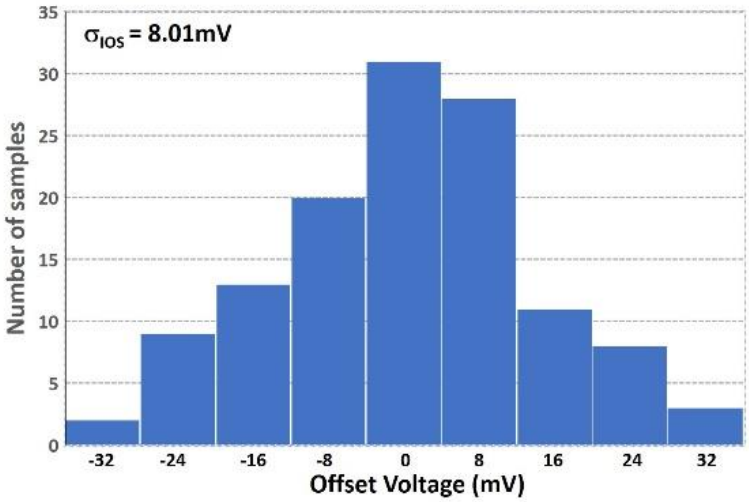
(a)



(b)



(c)



(d)

Fig. 3.8. Monte-Carlo plots at (a) V_{SUP} = 0.3V, (b) V_{SUP} = 0.6V, (c) V_{SUP} = 0.9V and (d) V_{SUP} = 1.8V.

The proposed comparator's performance matrices are summarized in Table 3.1, along with a comparison with state of the art. The comparator architectures in [79] and [80] are replicated in the 45nm CMOS process and simulated to determine their performance parameters, as the required data is not available in these papers. The proposed comparator can handle full swing V_{CM} levels and covers more comprehensive V_{CM} range compared to the prior digitally implemented comparator designs. Moreover, the proposed design can operate at a supply voltage down to 0.3V with an input offset voltage of 4.4mV while consuming a maximum power of 2.9µW that makes it suitable for ultra-low power designs.

Table 3.1. Performance comparison of FS-COM with existing synthesizable comparators

Paper	**[79]**		**[80]**			**[82]**			**[85] Arch. I**			**[85] Arch. II**			**Proposed**		
Synthesizable	Yes		Yes			Yes			Yes			Yes			Yes		
Process [nm]	45		45			40			65			65			45		
V_{SUP} [V]	0.6	0.3	0.6	0.9	0.3	0.6	0.9	0.3	0.6	0.9	0.3	0.6	0.9	0.3	0.6	0.9	1.8
V_{CM} Range	0.4-0.6	0.15-0.3	0.3-0.6	0.45-0.9	0-0.3	0.1-0.6	0.2-0.9	0-0.3	0.18-0.48	0.27-0.63	0-0.3	0-0.6	0-0.9	0-0.3	0-0.6	0-0.9	0-1.8
Delay [ns]	0.65	15.1	1.1	0.41	100	3	0.25	13.3	0.53	0.16	15.49	0.69	0.23	0.71	0.67	0.7	0.83
Input offset voltage [mV]	6.23	7.3	6.23	9.7	28	40	60	>100	>200	177	28	34	49	4.4	6.23	7.92	6.08
Power [µW]	2.7	0.031	2.7	71	0.015	1.5	40	6.6	338	3242	10	591	5540	0.033	3.9	79	165
Power-Delay Product [fJ]	1.755	46.81	2.97	29.11	1.5	4.5	10	87.78	179.14	518.72	154.9	407.79	1274.2	0.0234	2.613	55.3	136.95

3.4 SUMMARY

A fully-synthesizable clocked comparator has been presented in this chapter. The proposed design's operation has been demonstrated through post-layout simulations for the full swing analog input signals for a supply voltage ranging from 0.3V to 1.8V in 45nm CMOS process. Since the proposed design can be scripted through Verilog coding, it can be adopted as a substitute for its analog counterpart in analog-mixed signal vendors. The fast response time and low voltage operation of the proposed clocked comparator with acceptable input offset make it a suitable option for high-speed ultra-low power devices including low dropout voltage regulators, ADCs, and IoT devices.

CHAPTER 4

FULLY-SYNTHESIZABLE LDO

4.1 INTRODUCTION

This chapter presents a fully-synthesizable digital voltage regulator (FS-LDO) for applications consuming up-to tens of microamps. The proposed design uses a synthesizable controller (DLDOC) to detect load fluctuations and control a tri-loop structural design. This tri-loop structure minimizes the ripples on output voltage (V_{OUT}) and provides a fast-transient response (TR). This structure decreases the length of bi-directional shift register (Bi-SR) which reduces the overall power consumption. A quivering control is introduced to minimize the V_{OUT} oscillations in steady-state. The fully-synthesizable comparator (FS-COM) proposed in chapter 3 is used to monitor the load changes and demonstrate the entire design using CMOS standard cells. A tri-state buffer array (TBA) is employed instead of conventional PMOS switch array (PMA) to make this design fully-synthesizable. A pattern detection mechanism is used to switch between different loops. The proposed prototype occupies 6,394µm^2 area in 45nm CMOS technology. This design is implemented using conventional synthesis and place-and-route (PnR). With a supply voltage (V_{SUP}) of 0.5 – 1V and a load current (I_{OUT}) of up-to 2mA, a regulated V_{OUT} is attained with a dropout voltage of 50mV. At 10MHz clock frequency (f_{CLK}), the proposed LDO achieves a quiescent current (I_Q) and fast-TR of 2.2µA and 1.2µs, respectively. A maximum current efficiency (η) of 99.89% is attained with output ripples < 1mV.

4.2 PROPOSED FULLY-SYNTHESIZABLE LDO

In the baseline DLDO [22], the comparator senses the difference between V_{OUT} and V_{REF} and provides a digital output to the Bi-SR. The comparator output controls the register values of Bi-SR to turn-on/off the power MOSFETs in the PMA to maintain the V_{OUT} level equal to V_{REF} [86]. The V_{OUT} and V_{REF} are compared either by the clocked comparator, time-to-digital converter (TDC), or 1-bit ADC [87–93]. These circuits need to be designed using analog-design approaches. In order to design a fully-synthesizable LDO, an FS-COM is designed and used in the proposed FS-LDO which can be described in Verilog code. The power MOSFETs are

replaced with high-V_{TH} tri-state buffers to demonstrate the implementation of the proposed FS-LDO using automated digital design flow. The proposed design is implemented using conventional synthesis and placement and routing (PnR) tools by explicitly mentioning the desired strengths of CMOS standard-cells in the Verilog code. The proposed design can be easily integrated with other digital circuits through coding. The Fig. 4.1 shows the top-level block diagram of the proposed FS-LDO. The FS-LDO includes a digital controller (DLDOC), a tri-state buffer array (TBA), and an FS-COM. To demonstrate this design using standard cell logic gates, the V_{OUT} is fed directly to the comparator without using a voltage divider (R1 and R2 resistors). The proposed DLDO maintains $V_{OUT} = V_{REF}$. However, a voltage divider can be used to provide a tunable V_{OUT}.

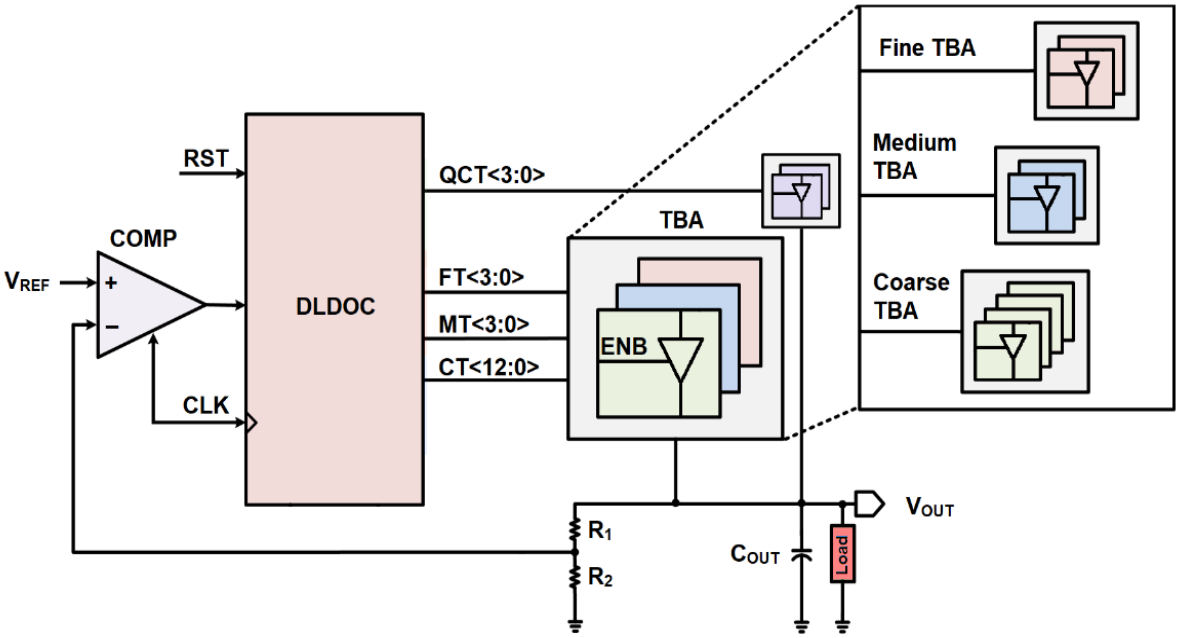


Fig. 4.1. Complete architecture of proposed FS-LDO.

A tri-loop architecture with coarse tuning (CT), medium tuning (MT), and fine tuning (FT) is adopted to reduce the leakage current (I_{LC}) and achieve a fast-transient response. The baseline DLDO uses long Bi-SR, leading to a slow transient response and large I_Q consumption. All the PMA transistors are switched on in full-load condition, increasing the leakage current (I_{LC}) through the DLDO. For the same load condition, the proposed tri-loop-based architecture requires a relatively small Bi-SR and reduced number of switches, which reduces the overall I_{LC} consumption. In steady-state, quivering control (QCT) is used to improve output dc accuracy.

The quivering is implemented using four tri-state buffers with the smallest strength (x1). The TBA coarse-section contains thirteen tri-state buffers with highest strength (x64) available in CMOS standard cell library while four moderate strength (x16) and four small strength (x4) tri-state buffers are used for medium and fine tunings respectively. In a TBA section, the input pins of the tri-state buffers are connected to the V_{SUP}, while their enable pins (ENB) are connected to the outputs of the corresponding Bi-SR.

4.2.1 WORKING PRINCIPLE

The working principle of the proposed FS-LDO can be well understood using the conceptual drawing of output waveform shown in Fig. 4.2. During a large load change, the coarse tuning is activated first, followed by medium tuning and fine tuning. Once V_{OUT} reaches the desired voltage level, the quivering control is activated to improve V_{OUT} accuracy. In the event of slight fluctuations in load, the quivering control remains in action to maintain the V_{OUT} at desired level.

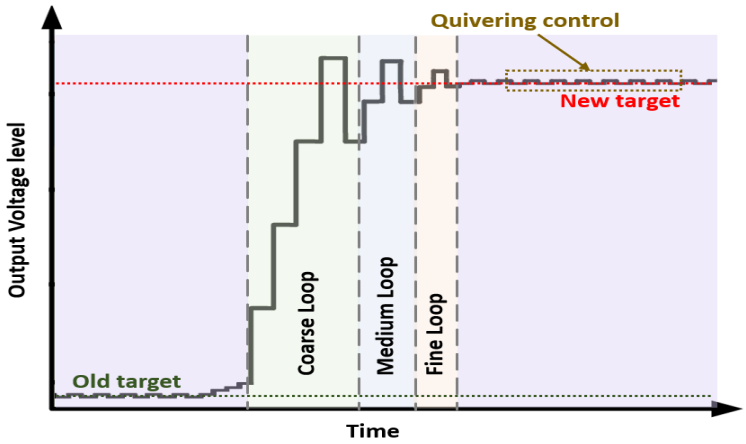


Fig. 4.2. Conceptual output waveform of the proposed FS-LDO.

The baseline DLDO [22] uses a long Bi-SR that results in a slow TR. Moreover, when all switches are on at full load, a large I_{LC} flows through the body of the DLDO. To solve this problem, FS-LDO used three different loop architectures in the TBA to control CT, MT and FT as shown in Fig. 4.1. The voltage step resolution of coarse TBA is higher than the medium TBA. Also, the voltage step resolution of medium TBA is higher than the fine TBA. Only one section either coarse, medium or fine is enabled at a time and single tri-state buffer is enabled/disabled per clock cycle. The V_{OUT} variations and TR time is decided by the number of enabled/disabled tri-state buffers per clock cycle. The tri-loop architecture provides a fast-TR and reduces the length of the Bi-SR and therefore reduces the associated power loss.

4.3 IMPLEMENTATION OF SUB-BUILDING BLOCKS OF FS-LDO

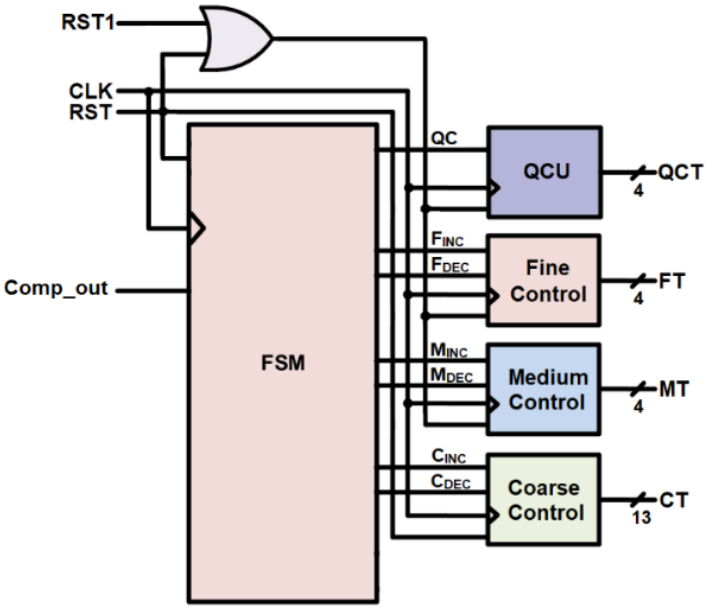
4.3.1 FS-LDO controller

The DLDOC is the key controlling unit of FS-LDO design. It controls the TBA loops and directs quivering control to achieve a low ripple output voltage with fast-

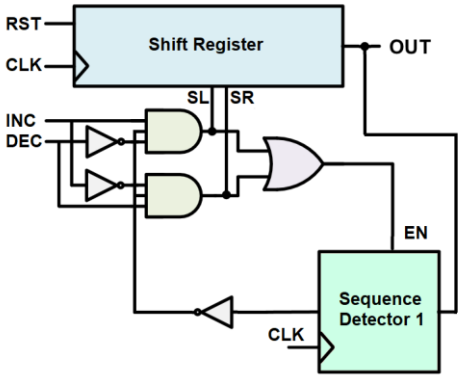
TR. The Fig. 4.3 shows the architecture of DLDOC. It contains a digital FSM, loop control logic and quivering control unit. The digital FSM in Fig. 4.3(a) includes an FSM controller, TBA control loops and a quivering control unit (QCU) to control CT, MT and FT.

The Fig. 4.3(b) shows the block level representation of loop control units used for controlling coarse, medium and fine loops. The loop control units receive the INC/DEC signals from FSM controller to control TBA in corresponding loop. It contains a Bi-SR, a sequence detector and logic controlling CMOS gates. The Bi-SR is a parallel in-out bi-directional shift register. The Bi-SR is loaded with all zeros at power up to initialize all the tri-state buffers in disable state. To ramp-up V_{OUT}, 1-bit shift left operation is performed on Bi-SR, followed by filling LSB position with one on each clock cycle. This operations enables the tri-state buffers one-by-one until the V_{OUT} reaches to its desired level. Similarly, when the load decreases, 1-bit shift right operation is performed on Bi-SR, followed by filling MSB position with zero, disabling the tri-state state buffer on each clock cycle. The sequence detector follows the pattern of CMP_OUT and freezes the Bi-SR data as V_{OUT} starts toggling around its target value. To achieve a high dc accuracy, the QCU is designed to control smallest sized tri-state buffers with the help of a pattern detector as shown in Fig. 4.3(c). At steady-state, the QCU keeps enabling/disabling one tri-state buffer in quivering mode. The Fig. 4.4 shows the flowchart of DLDOC.

When the FS-LDO turns on, the V_{OUT} is compared with V_{REF}, and FSM enables the coarse loop. When V_{OUT} reaches the V_{REF} level and starts ringing around it, the sequence detector (sequence detector 1) turns off the coarse loop and freezes its value. At the same time, FSM enables the medium loop with smaller voltage step resolution. Again, when V_{OUT} starts toggling around V_{REF} level, the medium loop is turned-off, enabling fine loop. On completion of fine tuning, the FSM turns on the quivering control to improve the output dc accuracy while monitoring the output variations in steady-state. When load changes, if the quivering fails to recover V_{OUT} within next four clock cycles, the FSM activates the coarse loop. At the same time, the FSM resets the shift registers controlling the medium TBA, fine TBA, and quivering by loading them with zeros. Following coarse loop, the subsequent loops including quivering are enabled one after the other to bring V_{OUT} to the target level.



(a)



(b)

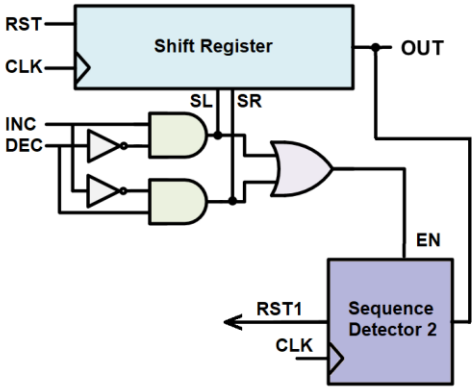


Fig. 4.3. Architecture of DLDOC (a) FSM (b) loop control logic (c) QCU

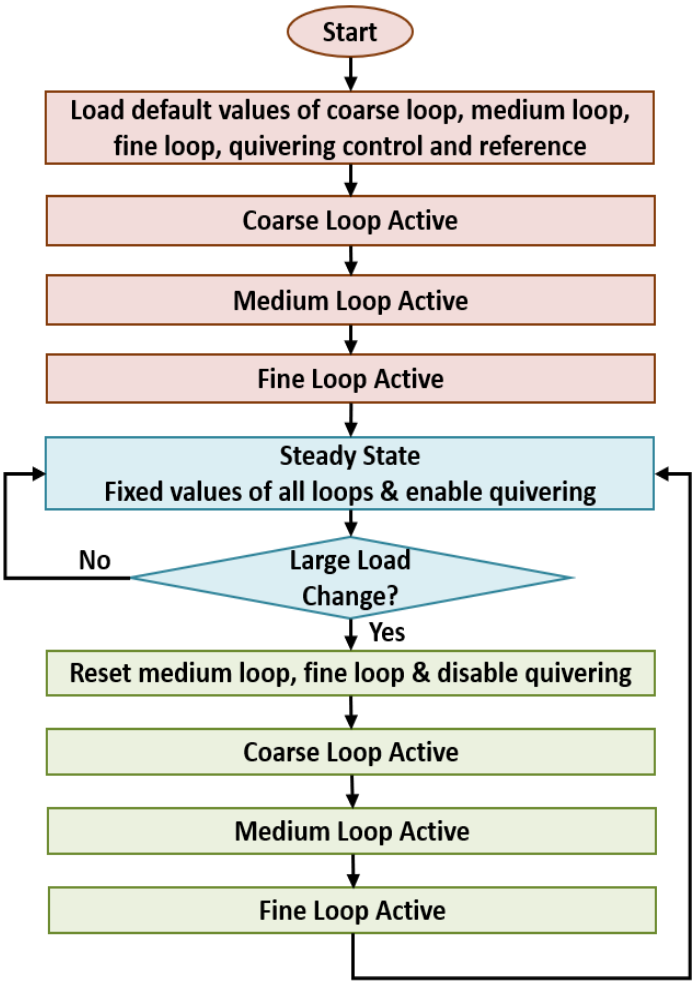


Fig. 4.4. Flow chart diagram of DLDOC

4.3.2 Sequence detector

Compared to the prior art which require min and max V_{REF} levels to detect V_{OUT} undershoots and overshoots, the proposed FS-LDO needs a single V_{REF} level. When a design requires multiple reference voltages, the same number of bandgap references and comparator circuits are needed. Using more circuits can make the design complex and directly contribute to increased chip area and power consumption. The switching between coarse, medium and fine loops is controlled by a sequence detector. The sequence detector circuit is implemented using standard cell library gates. The sequence detector monitors the CMP_OUT signal. During coarse tuning, if the sequence detector observes CMP_OUT signal as “01”, indicating that V_{OUT} is toggling around V_{REF} level, the FSM freezes the coarse loop and enables the medium loop. Also, by observing “01” on CMP_OUT signal during medium tuning, the FSM enables the fine tuning and freezes

medium tuning. In a similar way, quivering is activated after fine tuning. During quivering, when a high load transition occurs and the CMP_OUT signal does not toggle within next four clock cycles, the FSM switches to the coarse loop.

4.3.3 Quivering control

In the previous literature, various techniques such as dead zone [94] and freeze mode [57] are employed to improve output dc accuracy. At steady-state, when fine tuning overs, the freeze mode is activated through external control signal [57]. The main disadvantage of using this method is that it freezes the system by stopping the regulator clock, which sets V_{OUT} to a voltage level relatively lower or higher than

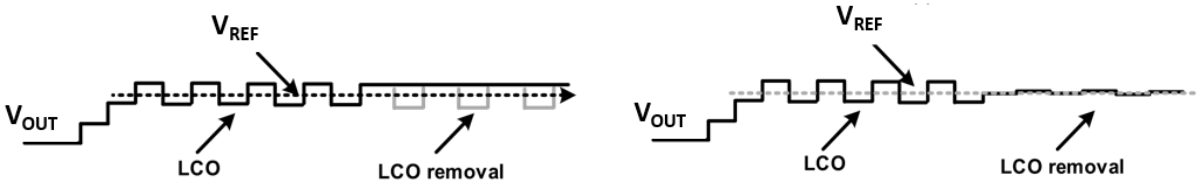


Fig. 4.5. Conceptual output waveforms with (a) freeze mode and (b) quivering.

the target level as picturised in Fig. 4.5(a). At steady-state, when the controller is deactivated, load fluctuations cannot be detected or corrected. To solve these problems of above discussed architectures, a digital quivering technique is incorporated in the proposed FS-LDO to suppress the limit-cycle oscillations (LCO) at the output during steady state. The Fig. 4.3(c) shows a conceptual block diagram of the QCU used to control quivering. The DLDOC activates the QCU automatically after the fine tuning in the steady state. The QCU controls four tiny tri-state buffers. After fine-tuning, QCU turns on/off one tri-state buffer on each clock cycle to produce more accurate V_{OUT} level. At steady-state, it keeps toggling one tri-state buffer to monitor the load variations. The quivering control improves the V_{OUT} accuracy by almost 75% over that of a fine loop, as illustrated in Fig. 4.5(b). In quivering state, the variations in load are sensed automatically and FS-LDO attains steady state again within few clock cycles.

4.4 SIMULATION RESULTS

The layout of the presented FS-LDO is shown in Fig. 4.6. The entire layout is generated using an automated P & R tool, eliminating the need for any manual work in the layout design. This proposed FS-LDO regulator occupies an area of 6,394μm^2 in a 45nm CMOS technology. The

measured load transient response is shown in Fig. 4.7. The I_{OUT} transient edge time is kept less than 1ns. When I_{OUT} switches from 2mA to 0.5mA with V_{SUP} = 0.5V and V_{OUT} = 0.45V, the maximum overshoot voltage of 30mV is observed. Also, an undershoot voltage of 140mV is seen at V_{SUP} = 0.5V for a low-to-high I_{OUT} transition, as shown in Fig. 4.7(a). At V_{SUP} = 1V and V_{OUT} = 0.95V, overshoot and undershoot voltages of 11.7mV and 18.1mV, respectively, are observed as shown in Fig. 4.7(b).

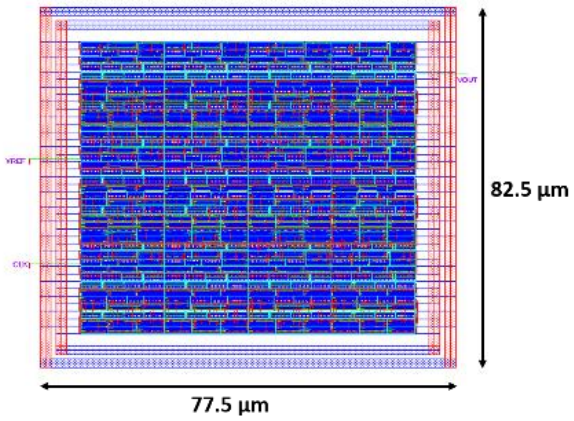


Fig. 4.6. FS-LDO's layout.

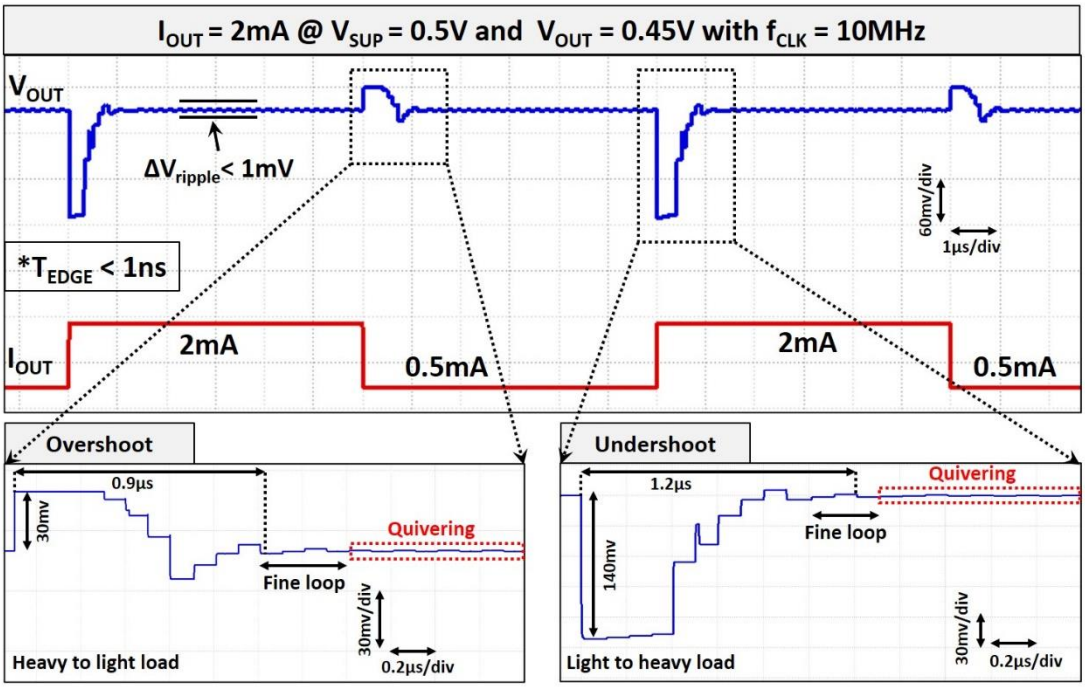


Fig. 4.7(a). Measured load transient response

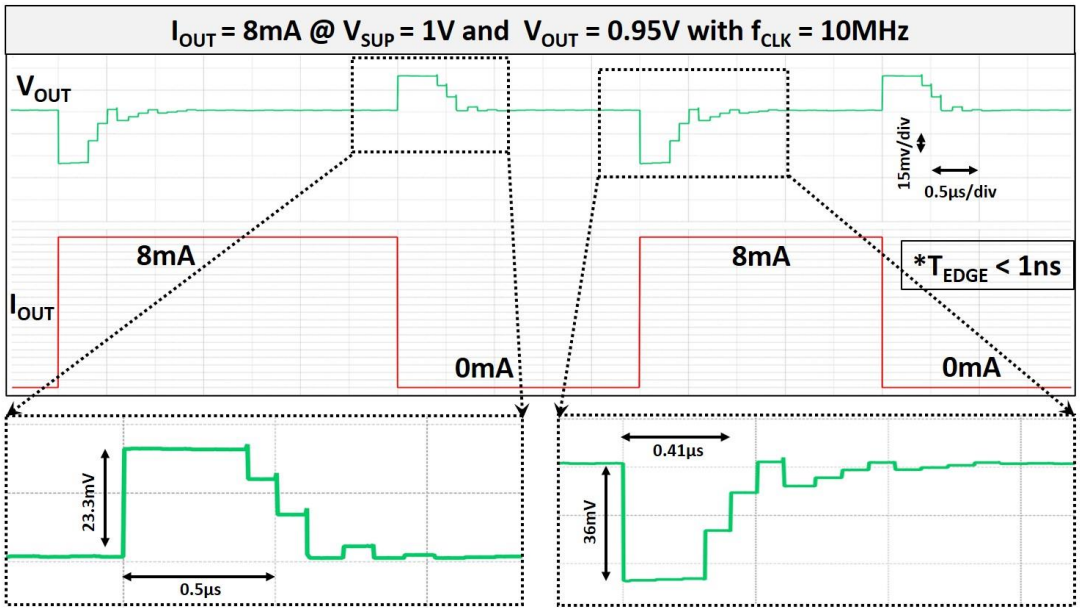


Fig. 4.7(b). Measured load transient response

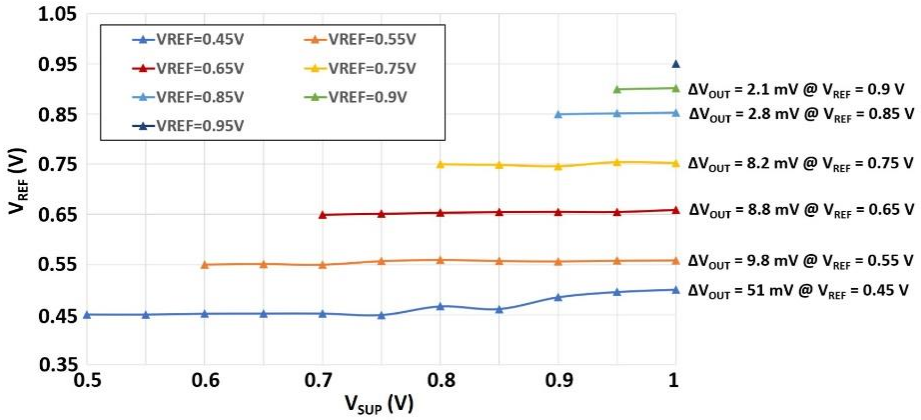
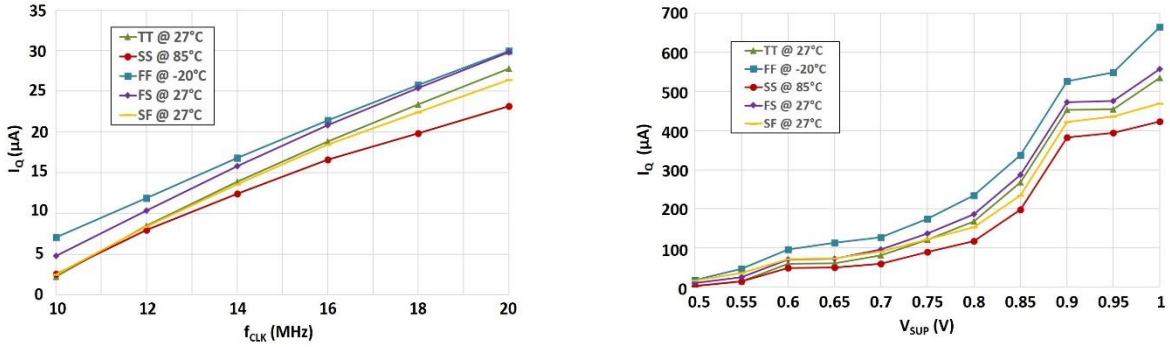
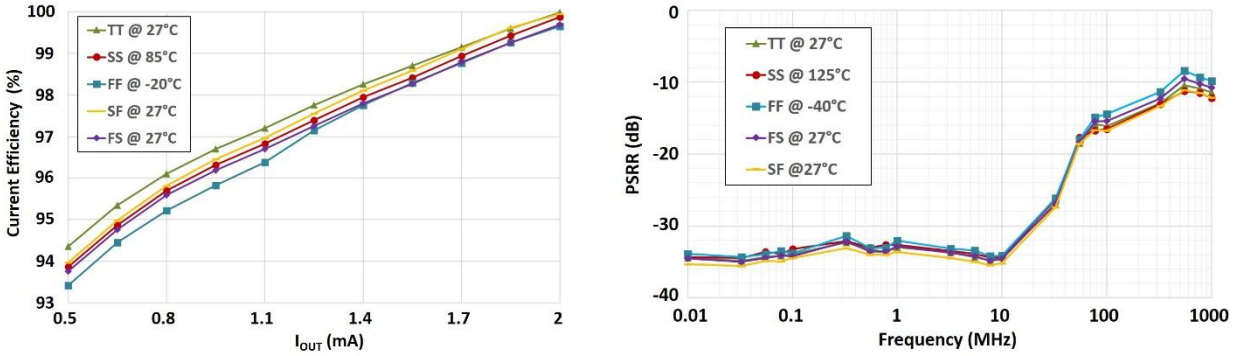


Fig. 4.8. V_{OUT} variations with respect to supply voltage at different V_{REF} levels at I_{OUT} = 2mA.



(a) (b)

Fig. 4.9. Measured I_Q at V_{REF} = 0.45V with respect to (a) f_{CLK} at V_{SUP} = 0.5V, and (b) V_{SUP} at f_{CLK} = 10MHz.



(a) (b)

Fig. 4.10. Simulation of FS-LDO across various process corners with V_{SUP} = 0.5V, and V_{REF} = 0.45V: (a) η vs I_{OUT}, and (b) PSRR curve.

Fig. 4.8 shows the variation of V_{OUT} in relation to supply voltage at f_{CLK} = 10MHz. The peak deviation of V_{OUT} is 51mV for V_{REF} = 0.45V when V_{SUP} is increased from 0.5V to 1V. When V_{SUP} increases from 0.5V at VREF = 0.45V, the V_{OUT} tends to increase linearly with V_{SUP}. To keep V_{OUT} = V_{REF}, the LDO changes its tuning from quivering (in steady-state) to coarse. When V_{SUP} reaches 0.9V or higher, the dropout voltage becomes equal to or greater than V_{OUT}. The number of tri-state buffers in each TBA section of the proposed architecture is determined under the assumption that the dropout voltage will always be less than V_{OUT}. As soon as this condition is violated, V_{OUT} follows V_{SUP}. For this reason, when V_{SUP} exceeds 0.9V, V_{OUT} deviates significantly from 0.45V.

The I_Q, for the proposed FS-LDO, is measured using (4.1) and plotted at various CLK frequencies and V_{SUP} levels as shown in Fig. 4.9. The proposed design consumes an I_Q of 2.2µA at V_{SUP} = 0.5V, V_{REF} = 0.45V and f_{CLK} = 10MHz under TT (27°C) corner. If V_{SUP} is increased to 1V with all other inputs held at the same value, I_Q increases 664.3µA. Under the same conditions, changing V_{SUP} to 1V with V_{REF} = 0.95V, this LDO draws an I_Q of 25.2µA.

$$I_Q = I_{IN} - I_{OUT} \tag{4.1}$$

The η of the proposed LDO is calculated using (4.2) and is plotted at various I_{OUT} values on different process corners, as shown in Fig. 4.10(a). This design achieves η of 99.89%, 99.87%, and 99.64% at TT@27°C, SS@85°C, and FF@-20°C, respectively with I_{OUT} = 2mA.

$$\eta = \frac{I_{OUT}}{(I_{OUT} + I_Q)} \times 100 \tag{4.2}$$

Table 4.1. Performance comparison of proposed FS-LDO with prior-art

Paper	**[21]**	**[24]**	**[28]**	**[29]**	**[38]**	**[46]**	**[50]**	**[52]**	**[59]**	**[60]**	**[61]**	**[62]**		**FS-LDO**
Architecture	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	Digital	ED	Analog		Digital
Synthesizable	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	Partially	No		Fully
Tech. [nm]	65	28	65	130	110	65	28	22	65	130	65	65		45
Area [mm^2]	0.034	0.021	0.01	0.114	0.04	0.291	0.019	0.165	0.012	0.114	0.029	0.16		0.0064
Load Cap. [nF]	0.1 (on-chip)	23.5	1	900000	1	2 (on-chip)	0.15 (on-chip)	7	0.1 (on-chip)	_	0.4 (on-chip)	0.04	0.04	0.05
V_{SUP} [V]	0.5-1	1.1	0.6-1.1	0.5-1.2	0.6-1.2	0.6-1	0.6-0.65	0.55-1.2	0.5-1	0.5-1.2	0.5-1	0.2	0.6	0.5-1
V_{OUT} [V]	0.45-0.95	0.9	0.4-1	0.45-1.14	0.5-0.9	0.55-0.95	0.55-0.6	0.5-1.15	0.35-0.95	0.45-1.14	0.45-0.95	0.05-0.15	0.3-0.55	0.45-0.95
ΔV_{OUT} [mV]	105	120	55	40	53	250	56	10	46	40	40	34.8	133.9	140
Max. I_{OUT} [mA]	12	200	100	4.6	80	500	5-25	0.4-2000	2.8	3	7.2-3511	0.1	50	2-8
I_Q [µA]	3.2	110	82	24-221	12-32	350	28	2400	45.2	24	12.5-216	0.41	32	2.2-25.2
f_{CLK} [MHz]	10	1000	500	100	1	-	10	200	12	10	200	1	1	10
Transient Time [µs]	1	10	0.7	1	38	0.1	10	80	0.037	3	80	-		1.2
Load Reg. [mV/mA]	2.3	120	0.06	10	0.3	0.15-2	20	0.2	46	10	100	34.8	133.9	1.0072
Current Eff. [%]	95.5	99.94	99.92	98.3	99.98	99.93	99.6	99.76	98.4	98.3	96.3	99.59	99.93	99.89
FOM [ps]	0.23	7.75	0.43	36	0.26	0.7	0.59	0.198	67.1	0.0765	1.11	227.8	1.68	0.708*

* FOM measured at V_{SUP} = 1V

Fig. 4.10(b) depicts the PSRR plot at various frequencies using its definition in (4.3). For frequencies less than 10MHz, the measured PSRR with an off-chip load capacitance of 50pF is less than -30dB across the process corners.

$$\text{PSRR} = \frac{V_{OUT}\ \text{Variations}}{V_{SUP}\ \text{Variations}} \tag{4.3}$$

$$\text{FOM} = \frac{C_{OUT} \times \Delta V_{OUT} \times I_Q}{I_{MAX} \times \Delta I_L} \tag{4.4}$$

Table 4.1 illustrates the performance parameters of the presented FS-LDO design and compares them with the preceding studies. The proposed FS-LDO attains fast-TR by employing tri-loop design. A commonly used figure of merit (FOM) [27] is calculated using (4.4) and produces FOM of 3.85ps and 0.708ps at V_{SUP} levels of 0.5V and 1V, respectively, for the proposed design. This design attains a high output dc accuracy by incorporating quivering control at steady-state as compared to the published work.

4.5 SUMMARY

This chapter presented a high-performance FS-LDO for ultra-low power applications. The fully-synthesizable comparator circuit senses the load changes and controls the tri-loop architecture with the help of digital controller for achieving high η, reducing V_{OUT} ripples and achieving fast-TR. The proposed method reduces the transient response time, improves V_{OUT} dc accuracy and minimizes the I_{LC} in TBA. In steady state, quivering minimizes the level of LCO. The proposed FS-LDO can be easily integrated with other digital circuits using traditional digital design flow. The measured V_{OUT} is 0.45V with a voltage drop of 50mV at V_{SUP} = 0.5V. For a load change from 0.5mA to 2mA, a low I_Q and fast-TR of 2.2µA and 1.2µs, respectively are measured with operating frequency of 10MHz. The load regulation of 1.007mV/mA and line regulation of 23.8mV/V are observed at V_{SUP} = 0.5V. The maximum attained η is 99.89% with output voltage ripples less than 1mV. The presented FS-LDO occupies 6,394µm^2 area in 45nm CMOS process.

CHAPTER 5

TRANSIENT-ENHANCED FULLY-SYNTHESIZABLE LDO

5.1 INTRODUCTION

This chapter demonstrates a transient-enhanced fully-synthesizable digital low dropout regulator (TFS-LDO) which can be described using a Verilog code. The proposed TFS-LDO can work with low V_{SUP} values (0.5V) close to the sub-threshold range. Some important design approaches are presented to attain fast-transient response with high current efficiencies and output dc accuracy. The fully-synthesizable comparator (FS-COM) proposed in chapter 3 is used to detect load changes. A pattern recognition circuitry is employed to switch between different loops. When freeze-mode is activated in steady-state, two voltage references V_{REFH} and V_{REFL}, defining higher and lower voltage reference limits, respectively, are used to detect the variations in load current (I_{OUT}). To attain a fast-transient response with low I_Q, a quad-loop architecture is adopted. Further to demonstrate this whole design using CMOS standard-cells, an array of tri-state buffers is employed instead of using power MOSFET array (PMA).

5.2 ARCHITECTURE OF PROPOSED TFS-LDO

The comparator in the baseline D-LDO [22] compares V_{REF} and V_{OUT}, and controls Bi-SR. The comparator instructs the Bi-SR to turn on/off the transistors in PMA to maintain $V_{OUT} = V_{REF}$ [96]. The time-to-digital converter, clocked comparator, 1-bit ADC, and other similar circuits are used to compare V_{OUT} and V_{REF}, and enhance the LDO performance [101–103]. Such circuits are designed using either semi-custom or full-custom analog design approaches.

The proposed TFS-LDO employs a Resistor-Transistor Logic (RTL) based FS-COM. The P-MOSFETs are replaced with tri-state buffers to implement the whole design using digital design flow. The entire structure is described in an RTL code and is executed with standard synthesis and Place-and-Route (PnR) tools. The TFS-LDO can be integrated into other digital circuits by defining their connections in RTL coding.

Fig.2 depicts TFS-LDO's architecture. It is comprised of digital logic controller (D-CTRL), tri-state buffer array (TBA), and FS-COM. The architecture includes four different tuning

mechanisms: coarse-tuning (CT), medium-tuning (MT), fine-tuning (FT), and quivering (QT) to reduce leakage current and achieve fast-transient response. This architecture uses tri-state buffers from the standard-cell library to drive the load. The maximum strength of the tri-state buffer determines transient response time and load deriving capability of the TFS-LDO, while its lowest strength determines the output accuracy.

A freeze-mode is enabled in steady-state to suppress V_{OUT} oscillations and save power. The CT is established using high-strength (x64) tri-state buffers, whereas MT, FT, and QT are accomplished using tri-state buffers of x16, x4, and x1 strengths, respectively. The CT is implemented using thirteen bits <12:0>, with each bit used to enable/disable a single tri-state buffer. Similarly, each MT<3:0>, FT<3:0> and QT<3:0> controls four tri-state buffers.

An overshoot/undershoot detector (OUD), consisting of two FS-COMs and an exclusive NOR cell, is used to sense load variations in the steady-state.

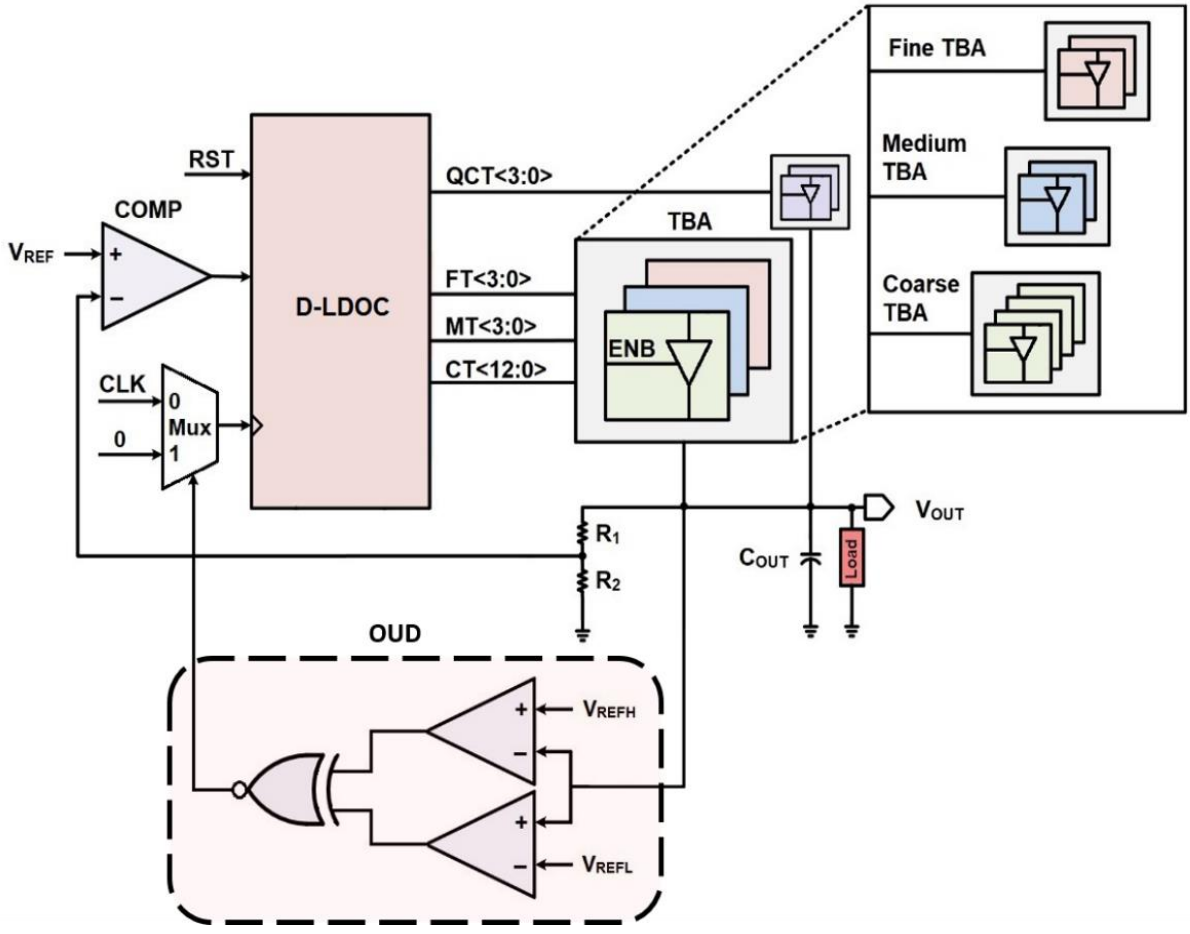


Fig. 5.1. Complete architecture of proposed TFS-LDO.

5.2.1 Operating principle

The operation of TFS-LDO can be understood with the aid of a conceptual output waveform shown in Fig. 5.2. When I_{OUT} changes, the D-CTRL enables QT. If V_{OUT} cannot be restored within next four clock (CLK) cycles, D-CTRL activates CT, then MT, and then FT. The QT is turned on after FT to improve V_{OUT} accuracy in steady-state. The OUD activates the freeze-mode to reduce dynamic power consumption at steady-state.

If V_{OUT} fluctuates in steady-state, the OUD disables freeze-mode and allows QT to counter the fluctuations. The QT quickly recovers the slight variations of V_{OUT}. Once the QT brings the V_{OUT} within V_{REFH} (100.2% of V_{REF}) and V_{REFL} (99.8% of V_{REF}) limits, the OUD locks the V_{OUT} level by activating freeze-mode. The resolution of QT determines the levels of V_{REFH} and V_{REFL}. After a load change, if QT fails to restore V_{OUT} within next four CLK cycles, D-CTRL repeats the same process to retrieve the V_{OUT} by activating the CT, MT, FT, QT and freeze-mode one by one.

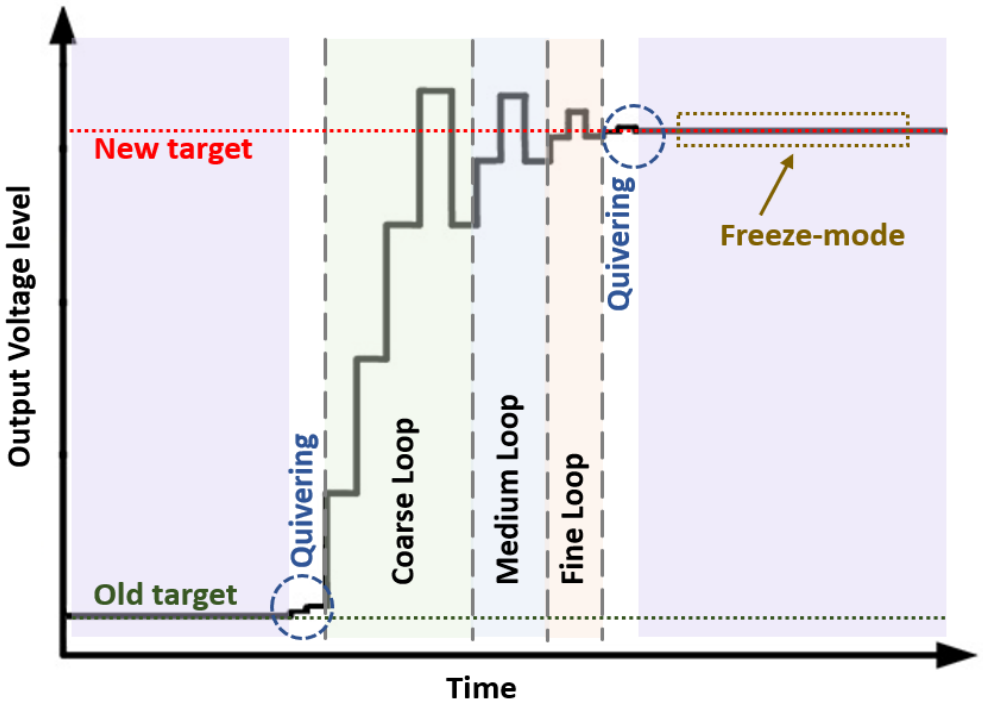


Fig. 5.2. Conceptual output waveform of the proposed TFS-LDO.

The traditional D-LDO employs a long Bi-SR, which results in slow transient response. Moreover, all P-MOSFETs in PTA are turned-on at full load condition, resulting in high leakage current. To address these issues, the TFS-LDO adopts a quad-loop architecture.

The quad-loop architecture provides different voltage step resolutions (V_{RES}) to recover the V_{OUT} after a load change. The coarse TBA has a higher V_{RES} compared to medium TBA. In comparison to medium TBA, fine TBA has a lower V_{RES}. The fine TBA also has a higher V_{RES} than quivering. A Bi-SR is assigned to each TBA section. The quad-loop architecture employs short-length Bi-SRs to decrease the associated leakage current. The use of multiple V_{RES} aids in the enhancement of transient response. In the steady-state, freeze-mode reduces dynamic power dissipation.

5.3 ARCHITECTURE OF SUB-BLOCKS

5.3.1 D-CTRL architecture

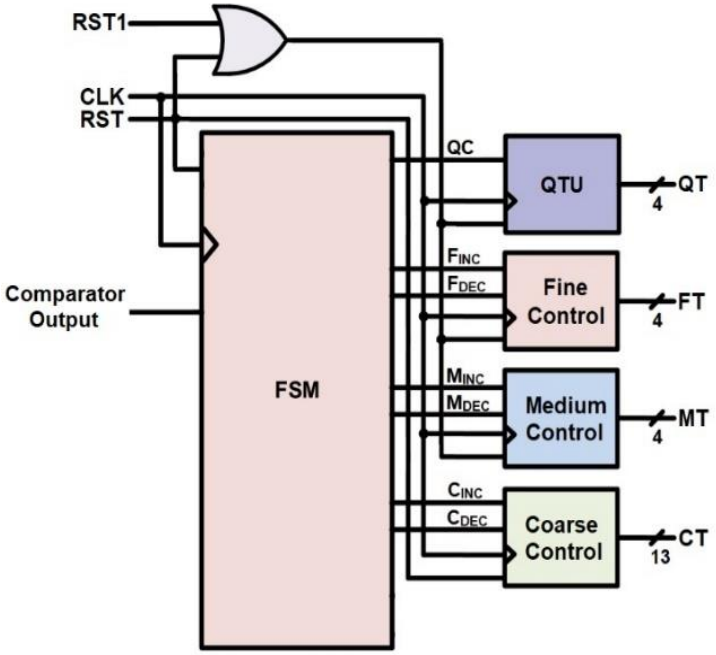
D-CTRL is the central control unit in TFS-LDO design. It processes OUD and FS-COM output signals and generates CT, MT, FT and QT signals to control TBA sections, quivering, and freeze-mode. The Fig. 5.3 depicts architecture of D-CTRL. It is made up of finite state machine (FSM), tuning control units (TCU) and QT unit (QTU). The FSM generates CT, MT, FT, and QT through their respective control units, as shown in Fig. 5.3(a).

Fig. 5.3(b) depicts architecture of a TCU. The TCU receives the INC/DEC signal from FSM and generates control signal for its TBA section. It is comprised of logic cells, a parallel-in parallel-out Bi-SR, and a pattern detector.

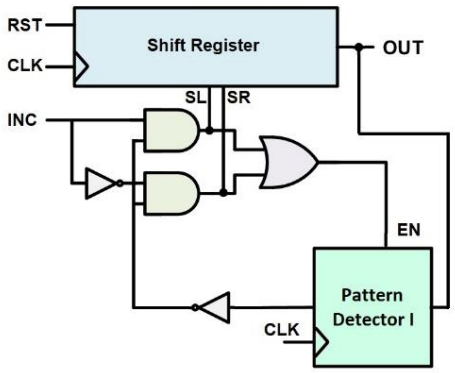
When TFS-LDO is powered on, the Bi-SR gets loaded with zeros to initialize all tri-state buffers in a high-impedance state. To raise V_{OUT} to V_{REF} level, Bi-SR data is shifted one bit to the left, and then a 1 is inserted into the register on the far right. This operation sequentially enables the tri-state buffers until V_{OUT} arrives at its target level.

For $V_{OUT} > V_{REF}$, the Bi-SR data is shifted to the right by one bit, then a 0 is inserted into the register on the far left. Increasing 0's in Bi-SR lowers the V_{OUT} level by disabling tri-state buffers.

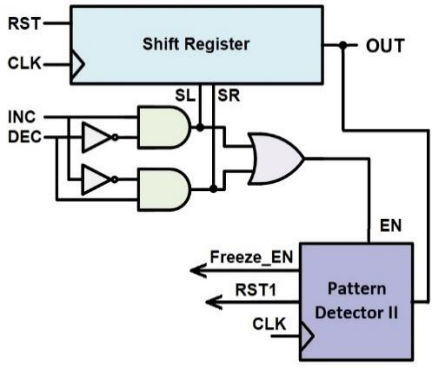
Fig. 5.3(c) shows the QTU block. This block controls the lowest-strength tri-state buffers to provide the most refined V_{OUT} tuning. It generates freeze-mode control signal. When V_{OUT} begins to oscillate around target level, the QTU locks the Bi-SR data and activates the freeze-mode.



(a)



(b)



(c)

Fig. 5.3. Architecture of DLDOC (a) FSM (b) loop control logic (c) QCU

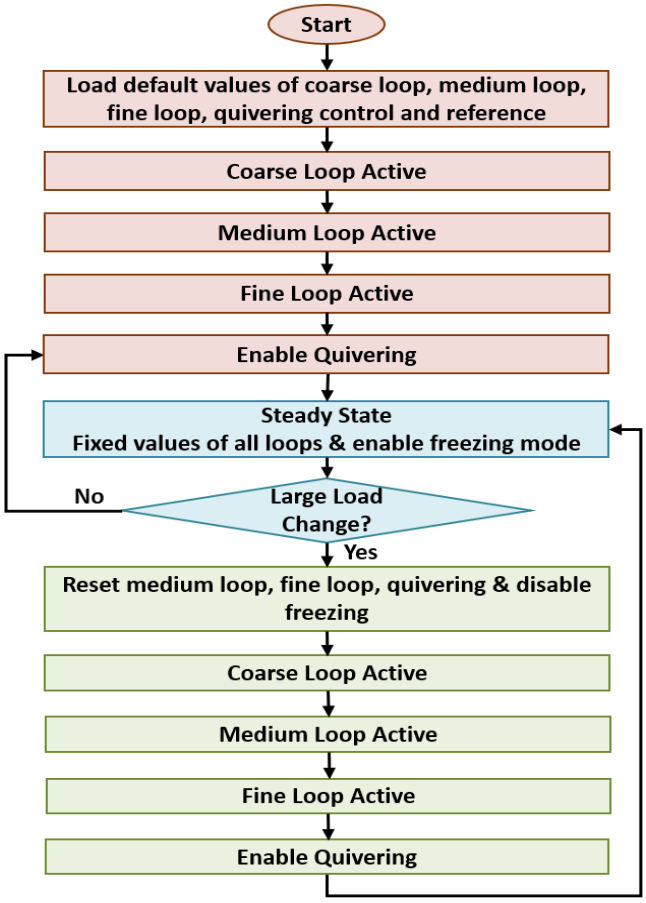


Fig. 5.4. Flow chart diagram of DLDOC

The flowchart in Fig. 5.4 presents the D-CTRL operation. When the TFS-LDO is turned on, all the Bi-SRs in the design are loaded with zeros, setting V_{OUT} to zero. The FSM initiates CT to raise V_{OUT} to its target level quickly. When V_{OUT} reaches its target level and oscillates, the pattern detector (Pattern Detector I) disables the CT. Simultaneously, FSM allows the MT to provide more accurate V_{OUT}. When V_{OUT} begins to oscillate around the target level, the MT is deactivated, and FT is activated concurrently. When the FT is completed, FSM activates QT to improve dc accuracy in steady-state. The freeze-mode is enabled when V_{OUT} starts quivering around target level.

When there is a fluctuation on V_{OUT} due to a load change, OUD disables freeze-mode and enables QT to recover V_{OUT}. If QT fails to retrieve V_{OUT} within next four CLK cycles, the CT comes into action. Simultaneously, the FSM loads zeros into the Bi-SRs that control MT, FT, and QT. After CT, the subsequent tunings and freeze-mode are activated to achieve $V_{OUT} = V_{REF}$.

5.3.2 Pattern detector

The pattern detector is a digital circuit, which plays a critical role in switching between CT, MT, FT and QT. The pattern detector generates the control signals based on the sequence of FS-COM's outputs.

When TFS-LDO is powered-on, CT raises the V_{OUT} to its target level. As V_{OUT} starts to oscillate around its target level, the comparator produces an output pattern – "01010…". When the pattern detector observes "01" at the comparator output, it freezes CT and enables MT. Following the same process, when the comparator output sequence is detected as "01", the MT is disabled, and FT is enabled.

Similarly, QT is enabled after FT. When V_{OUT} starts quivering around the target level, the OUD activates freeze-mode, which lowers dynamic power consumption. When V_{OUT} fluctuates at steady-state, freeze-mode is disabled, and QT is activated. If FS-COM output doesn't toggle within next four CLK cycles during quivering, FSM switches the control to CT.

5.4 SIMULATION RESULTS

The TFS-LDO's layout shown in Fig. 5.5 occupies 6,708µm² area. To verify the performance of TFS-LDO, I_{OUT} is switched between 500µA and 2mA with an edge time less than 1ns. The input stimuli are kept as follows: V_{SUP} = 500mV, V_{REF} = 450mV, V_{REFH} = 450.9mV and V_{REFL} = 449.1mV. The Fig. 5.6 shows the TFS-LDO's response to load transients at f_{CLK} = 10MHz.

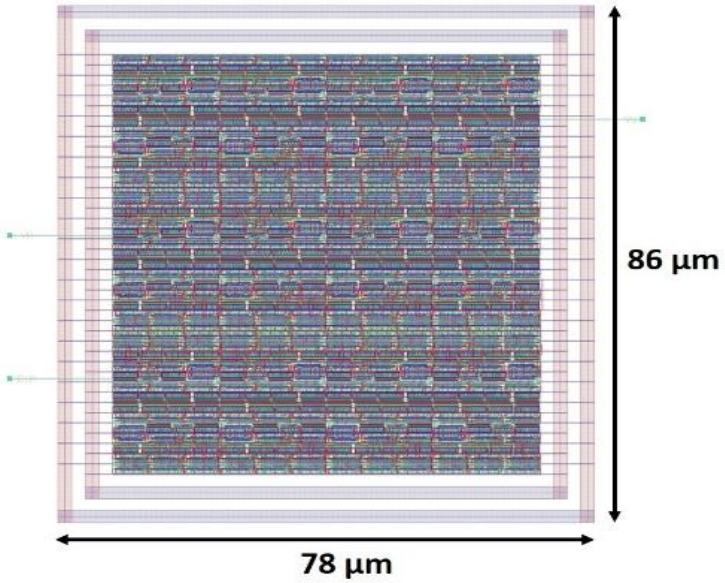


Fig. 5.5. TFS-LDO layout.

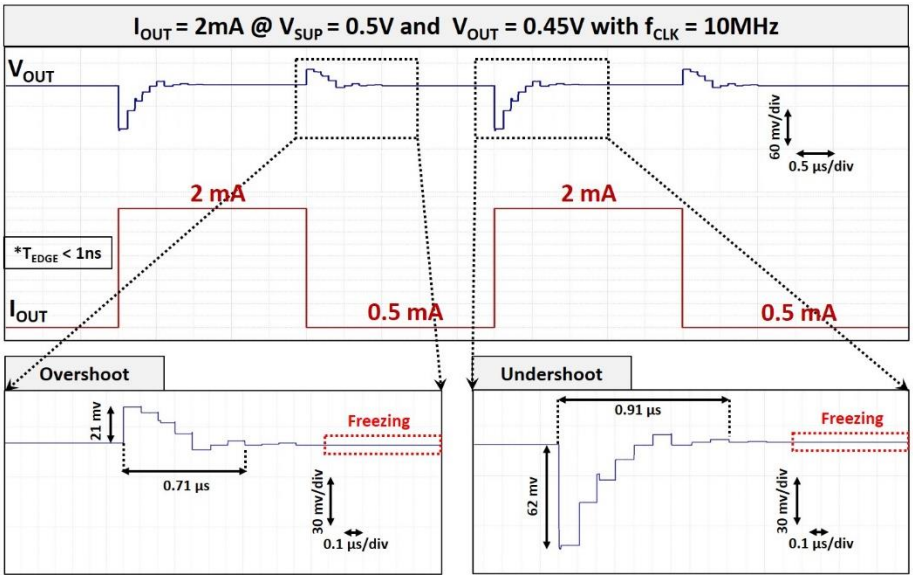


Fig. 5.6 (a). Measured load transient response at V_{SUP} = 0.5V

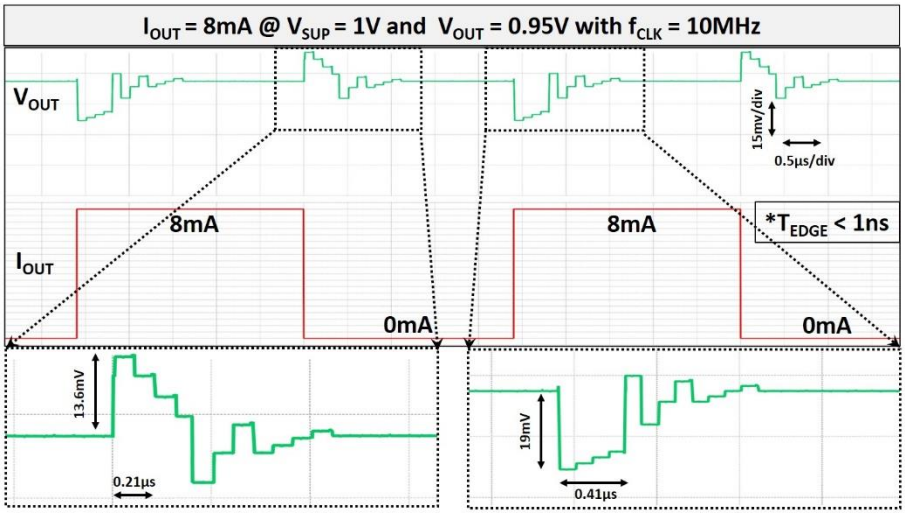


Fig. 5.6 (b). Measured load transient response at V_{SUP} = 1V

When I_{OUT} is switched from 2mA to 500µA, an overshoot of 21mV is observed. An undershoot of 62mV is observed during I_{OUT} transition from 500µA to 2mA. For I_{OUT} = 2mA, the V_{OUT} deviates by a maximum of 11.9mV from its target level when V_{SUP} is raised from 500mV to 1V, as shown in Fig. 5.7.

The I_Q of a voltage regulator decides its power consumption during device standby mode. The lower this I_Q, the longer the battery life of the device. The I_Q of TFS-LDO can be obtained using (5.2). The I_Q rises with f_{CLK}, as shown in Fig. 5.8(a). For delivering I_{OUT} = 2mA, the TFS-LDO consumes an I_Q of 1.96µA at f_{CLK} = 10MHz. The I_Q rises proportionally to V_{SUP} for a constant V_{REF} level, as shown in Fig. 5.8(b).

$$I_Q = I_{IN} - I_{OUT} \tag{5.1}$$

The PSRR and current efficiency graphs for TFS-LDO are plotted at different process and temperature corners, using (5.2) and (5.3).

$$\text{PSRR} = \frac{V_{OUT}\ \text{Variations}}{V_{SUP}\ \text{Variations}} \tag{5.2}$$

$$\text{Current efficiency} = \frac{I_{OUT}}{(I_{OUT} + I_Q)} \times 100 \tag{5.3}$$

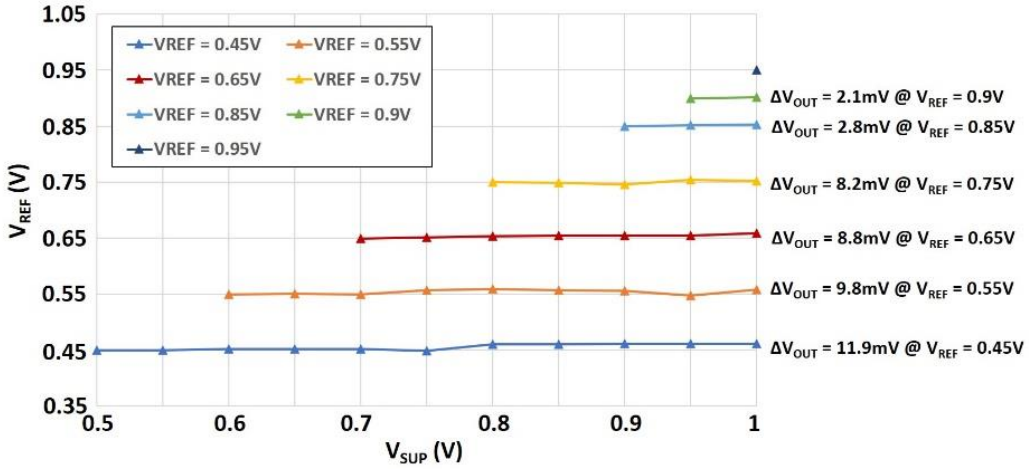
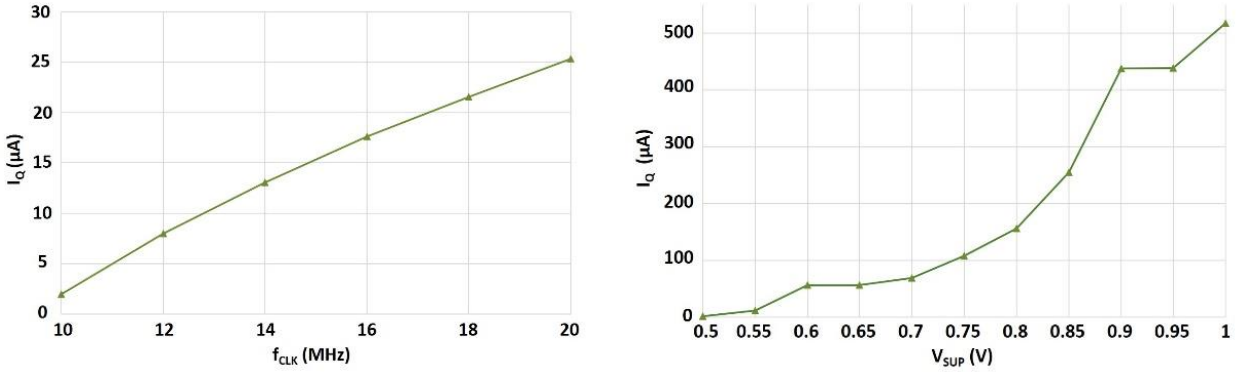


Fig. 5.7. V_{OUT} variations with respect to supply voltage at different V_{REF} levels.



(a) (b)

Fig. 5.8. Measured I_Q with respect to (a) f_{CLK} at V_{SUP} = 0.5V and V_{REF} = 0.45V, and (b) V_{SUP} at V_{REF} = 0.45V and f_{CLK} = 10MHz.

Table 5.1. Performance comparison of TFS-LDO with prior-art

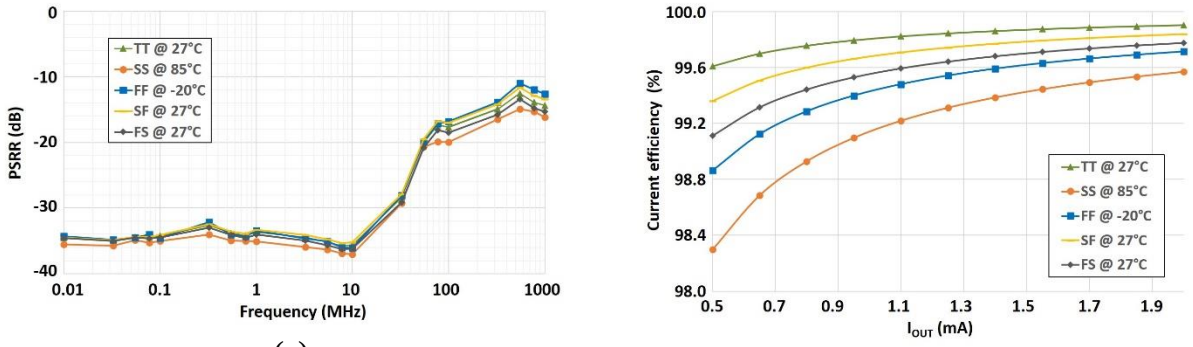
Paper	**[21]**	**[24]**	**[28]**	**[29]**	**[38]**	**[46]**	**[49]**	**[50]**	**[52]**	**[59]**	**[60]**	**[61]**	**[62]**		**FS-LDO (Ch. 4)**	**TFS-LDO**
Architecture	Digital	Digital	Digital	Digital	Digital	Digital	ED[C]	Digital	Digital	Digital	Digital	ED	Analog		Digital	Digital
Synthesizable	Part.	Part.[A]	Part.	Part.	Part.	Part.	Part.	Part.	Part.	Part.	Part.	Part.	No		Fully	Fully
Tech. [nm]	65	28	65	130	110	65	65	28	22	65	130	65	65		45	45
Area [mm^2]	0.034	0.021	0.01	0.114	0.04	0.291	0.113	0.019	0.165	0.012	0.114	0.029	0.16		0.0064	0.0066
Load Cap. [nF]	0.1 (OC)	23.5	1	900000	1	2 (OC[B])	0.1 (OC)	0.15 (OC)	7	0.1 (OC)	_	0.4 (OC)	0.04	0.04	0.05	0.05
V_{SUP} [V]	0.5-1	1.1	0.6-1.1	0.5-1.2	0.6-1.2	0.6-1	1.2	0.6-0.65	0.55-1.2	0.5-1	0.5-1.2	0.5-1	0.2	0.6	0.5-1	0.5-1
V_{OUT} [V]	0.45-0.95	0.9	0.4-1	0.45-1.14	0.5-0.9	0.55-0.95	0.5-1	0.55-0.6	0.5-1.15	0.35-0.95	0.45-1.14	0.45-0.95	0.05-0.15	0.3-0.55	0.45-0.95	0.45-0.95
ΔV_{OUT} [mV]	105	120	55	40	53	250	130	56	10	46	40	40	34.8	133.9	140	62
Max. I_{OUT} [mA]	12	200	100	4.6	80	500	700	5-25	0.4-2000	2.8	3	7.2-3511	0.1	50	2	2
I_Q [µA]	3.2	110	82	24-221	12-32	350	254	28	2400	45.2	24	12.5-216	0.41	32	2.2-25.2	1.96-21.3
f_{CLK} [MHz]	10	1000	500	100	1	-	-	10	200	12	10	200	1	1	10	10
Transient Time [µs]	1	10	0.7	1	38	0.1	12	10	80	0.037	3	80	-		1.2	0.91
Load Reg. [mV/mA]	2.3	120	0.06	10	0.3	0.15-2	0.1	20	0.2	46	10	100	34.8	133.9	1.0072	0.66
Current Eff. [%]	95.5	99.94	99.92	98.3	99.98	99.93	99.95	99.6	99.76	98.4	98.3	96.3	99.59	99.93	99.89	99.90
FOM [ps]	0.23	7.75	0.43	36	0.26	0.7	0.00674	0.59	0.198	67.1	0.0765	1.11	227.8	1.68	0.708*	0.316*

[A] Part. = Partially

[B] OC = On - chip

[C] ED = Event - driven

* FOM measured at V_{SUP} = 1V



(a) (b)

Fig. 5.9. Simulation of TFS-LDO across various process corners: (a)PSRR plot, and (b) η vs I_{OUT}.

The PSRR of TFS-LDO indicates its ability to tolerate noise on V_{SUP}. For frequencies below 10MHz, the obtained PSRR, as depicted in Fig. 5.9(a), is lower than -32dB across different process and temperature corners. For I_{OUT} = 2mA, the TFS-LDO attains a peak current efficiency of 99.90% at TT@27°C corner, as shown in Fig. 5.9(b).

Table 1 presents TFS-LDO's performance parameters and their comparison to the state-of-the-art. A well-known measure of LDO's performance, the figure of merit (FOM), is determined using (5.4) [27]. The TFS-LDO yields a FOM of 2.025ps and 0.316ps at V_{SUP} levels of 0.5V and 1V, respectively.

$$\text{FOM} = \frac{C_{OUT} \times \Delta V_{OUT} \times I_Q}{I_{MAX} \times \Delta I_L} \tag{5.4}$$

5.5 SUMMARY

This chapter presented a transient-enhanced low-power TFS-LDO for ultra-low-power applications. The TFS-LDO's performance is dependent on strength of used logic cells. The highest strength of tri-state buffers available in standard-cell library determines transient response time and load deriving capability of TFS-LDO, while its lowest strength determines the output accuracy. The FS-COM is used to detect the fluctuations on V_{OUT}. The D-CTRL managed the quad-loop architecture based on the FS-COM output. The quad loop architecture contributed to high current efficiency, ripple-free V_{OUT}, and fast-transient response. The proposed approach reduced transient response time, improved dc V_{OUT} accuracy, and reduced leakage current flow in the TBA. The freeze-mode eliminated oscillations in the steady-state. The TFS-LDO layout is

generated using PnR tools. The proposed TFS-LDO occupied a 6,708µm^2 area in TSMC CMOS 45nm process. The TFS-LDO can operate with V_{SUP} ranging from 0.5V-to-1 V and regulate V_{OUT} with a 50mV dropout voltage. At V_{SUP} = 500mV, f_{CLK} = 10MHz and I_{OUT} = 2mA, the TFS-LDO drawn I_Q of 1.96µA at steady-state and achieved fast-transient response time of 0.91µs measured with 1% settling time. The TFS-LDO achieved a steady-state I_Q of 21.3µA and achieved a fast-settling time of 0.41µs with V_{SUP} = 1V, f_{CLK} = 10MHz, and I_{OUT} = 2mA. The TFS-LDO achieved load and line regulations of 0.66mV/mA and 23.83mV/V, respectively. This design achieved peak current efficiency of 99.90% with a ripple-free output. The low-power consumption and fast-transient response of proposed TFS-LDO make it a preferred choice for ultra-low-power applications, including IoT and mobile devices.

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

From the analysis and simulation results performed and reported in the previous chapters, following conclusions have been drawn. The decisive notes are encompassed in the following section along with the limitations and future scope of the work.

6.1 CONCLUSION

The DLDOs have gained significant attention due to their fewer stability issues at sub-threshold voltage levels. In addition, their low area and power requirements make them more attractive compared to its analog counterparts. Several studies examining different DLDO architectures are included in the literature review in Chapter 2. The available DLDOs are partially synthesized and require tedious manual design. In addition, at low voltage levels, the existing DLDOs are slow to respond to load variations. After reviewing the literature and drawing inspiration from research gaps, three research goals are defined in chapter 2. The design and outcome of each goal are covered in detail one-by-one in Chapters 3, 4, and 5. The proposed DLDOs are not only fully synthesizable, but also have a reasonably fast-transient response at low supply levels.

In chapter 3, a fully-synthesizable clocked comparator (FS-COM) is proposed. The proposed design's operation has been demonstrated through post-layout simulations for the full swing analog input signals for a supply voltage ranging from 0.3V to 1.8V in 45nm CMOS process. Since the proposed design can be scripted through Verilog coding, it can be adopted as a substitute for its analog counterpart in analog-mixed signal vendors. The fast response time and low voltage operation of the proposed clocked comparator with a low input offset make it a suitable option for high-speed ultra-low power devices including low dropout voltage regulators, ADCs, and IoT devices. The chapter 4 presented a fully-synthesizable digital voltage regulator (FS-LDO) suitable for applications consuming up-to tens of microamps. The proposed design used an FS-COM to monitor the output voltage (V_{OUT}) and a synthesizable controller to control a tri-loop structure. The tri-loop structure minimized the ripples on V_{OUT} and provided a fast-transient response (TR). The tri-loop structure required short bi-directional shift registers (Bi-SR) to achieve fast-TR, which reduced the overall power consumption. A quivering control is introduced to minimize the V_{OUT} oscillations in steady-state. A tri-state buffer array (TBA) is

employed instead of conventional PMOS switch array to make this design fully-synthesizable. Signal pattern detectors are used to switch between different loops. The proposed prototype occupied 6,394μm^2 area in 45nm CMOS technology. The entire design is implemented using conventional synthesis and place-and-route (PnR). For a supply voltage (V_{SUP}) of 0.5 – 1V, a regulated V_{OUT} is attained with a dropout voltage of 50mV. At 10MHz clock frequency (f_{CLK}), the proposed LDO achieved a quiescent current (I_Q) and fast-TR of 2.2μA and 1.2μs, respectively. A maximum current efficiency (η) of 99.89% has been attained with output ripples < 1mV. The chapter 5 introduced additional circuitry to FS-LDO to improve its transient response and achieve a ripple-free output. The modified FS-LDO (TFS-LDO) supported freeze-mode to regulate a ripple-free V_{OUT} and minimize power consumption at steady-state. The layout is created using digital design flow in CMOS 45nm process, which occupied 6,708μm^2 area. For a V_{SUP} of 0.5-to-1V, the TFS-LDO can provide regulated V_{OUT} with a 50mV dropout voltage. At V_{SUP} = 500mV and f_{CLK} = 10MHz, the proposed regulator achieved a transient response time of 0.91μs. This prototype achieved a peak η of 99.90% and produced a ripple-free V_{OUT} at steady-state.

6.2 FUTURE SCOPE OF WORK

As the proposed designs are entirely made up of logic cells from a standard-cell library, their performance is entirely reliant on the cell-strengths available in a given technology. The characteristics of the proposed designs can vary widely across technologies due to differences in cell-strengths.

In case of FS-COM, higher the strength of logic cells used in design, smaller is the input offset voltage. If the cell-strengths are too weak, the FS-COM may not produce expected outputs when sampling rate is high. For FS-LDO, the highest available strength of tri-state buffers determines transient response time and load deriving capability, while lowest available strength determines the output accuracy. In future, more ways could be explored to improve the functionality of FS-COM designed with low or medium strength logic cells. The FS-LDO can be investigated further to provide a tunable output, while maintaining its fully-synthesizability.

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