TLP - vfTLP TESTING FOR ESD MODELS

A Thesis submitted in partial fulfilment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI DESIGN

Submitted By

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DECLARATION

I hereby declare that the project entitled 'TLP - vfTLP TESTING FOR ESD MODELS' is a record of our own work carried out in St Microelectronics, Greater Noida and Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology, Patiala under the guidance of **Dr. Surbhi Sharma (DECE)** and **Dr. Rajesh Khanna (DECE),** Assistant Professors during July 2025.

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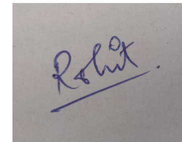
1	Rohit Choudhary	602362030	

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TO WHOMSOEVER IT MAY CONCERN

This is to certify that **Rohit CHOUDHARY** has undergone internship in our **TRD** Group from **June 12, 2024 to May 30, 2025**. and has successfully completed the project on: **DOE Designing and Analysis**

During the internship period, Rohit was found to be sincere and professional in conduct.

We wish him all the best for the future endeavors.

for **STMicroelectronics Pvt. Ltd.**

Sanjay Kumar PIPLANI
India Talent Acquisition Head

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I would like to extend my heartfelt gratitude to all those who have contributed towards the successful completion of the project and converge thanks to the entire St Microelectronics, Greater Noida team, our supervisors Dr. Surbhi Sharma, Dr. Rajesh Khanna and all the faculty & staff members of Electronics and Communication Engineering (ECED), Thapar Institute of Engineering & Technology for generously extending their support and for sparing their valuable time to guide us towards the completion of this project work.

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ABSTRACT

Electrostatic Discharge (ESD) protection is critical for ensuring the reliability and longevity of electronic components. The RC clamp, consisting of a resistor (R) and a capacitor (C), is a widely used circuit for mitigating the effects of ESD events. This abstract presents an overview of Transmission Line Pulse (TLP) and Very-Fast Transmission Line Pulse (VF-TLP) testing methodologies applied to RC clamps to evaluate their ESD protection performance.

TLP testing is employed to simulate ESD events and characterize the response of the RC clamp by applying controlled, high-current pulses. This method provides valuable insights into the clamp's current-voltage (I-V) characteristics, enabling the assessment of its clamping voltage, trigger voltage, and holding voltage. TLP testing helps in identifying the clamp's effectiveness in limiting the peak current and voltage during an ESD event, thereby ensuring the protection of sensitive electronic components.

VF-TLP testing, on the other hand, offers a more detailed analysis by applying extremely fast pulses with rise times in the sub-nanosecond range. This testing method is crucial for understanding the RC clamp's behavior under rapid transient conditions, which closely resemble real-world ESD events. VF-TLP testing allows for the evaluation of the clamp's dynamic response, including its ability to absorb and dissipate energy within very short time frames. This is particularly important for assessing the clamp's performance in high-speed and high- frequency applications.

The combined use of TLP and VF-TLP testing provides a comprehensive evaluation of the RC clamp's ESD protection capabilities. The results from these tests help in optimizing the design of the RC clamp, ensuring that it effectively mitigates ESD-induced damage and enhances the overall reliability of electronic devices. By understanding the RC clamp's performance under various pulse conditions, designers can make informed decisions to improve ESD protection strategies in modern electronic systems.

In conclusion, TLP and VF-TLP testing are essential methodologies for characterizing the ESD protection performance of RC clamps. These tests provide critical insights into the clamp's ability to limit peak currents and voltages, absorb transient energy, and protect sensitive components from ESD damage. The findings from TLP and VF-TLP testing contribute to the development of more robust and reliable ESD protection solutions in the electronics industry.

CHAPTER 1: INTRODUCTION

1.1 About the Project

An RC clamp is an essential circuit used in Electrostatic Discharge (ESD) protection to shield electronic components from high-voltage transients. It consists of a resistor (R) and a capacitor (C) arranged in a specific configuration to absorb and dissipate the energy from an ESD event, thereby protecting sensitive circuitry.

The resistor in the RC clamp plays a critical role in limiting the current flow during an ESD event. By providing resistance, it reduces the peak current that reaches the protected device, thus mitigating potential damage. This current-limiting action is crucial because it prevents the sudden surge of high current from damaging delicate electronic components.

The capacitor, on the other hand, acts as a charge storage device. During an ESD event, the capacitor absorbs the transient voltage spike and stores the charge, preventing it from reaching the sensitive components. Additionally, the capacitor helps to smooth out voltage spikes by providing a low-impedance path for the high-frequency components of the ESD pulse. This dual action of absorption and smoothing ensures that the voltage levels remain within safe limits, thereby protecting the device.

In a typical RC clamp configuration, the resistor and capacitor are connected in parallel with the load or the circuit that needs protection. This parallel arrangement ensures that the RC clamp can effectively absorb and dissipate the energy from the ESD event, thereby protecting the sensitive components from damage. The RC clamp is designed to respond quickly to the transient event, providing immediate protection to the circuit.

By using an RC clamp, electronic devices can be safeguarded against the harmful effects of ESD, ensuring their reliability and longevity in real-world applications. This protection is especially important in environments where electronic devices are frequently exposed to static electricity, such as in manufacturing facilities, consumer electronics, and automotive applications. The RC clamp's ability to protect against ESD helps in maintaining the performance and durability of electronic devices, making it a vital component in modern electronic design.

Design of Experiments[1] (DOE) can be effectively applied to analyze and mitigate Electrostatic Discharge (ESD) issues in environments where sensitive electronic components are handled or manufactured. The process begins by clearly defining the objective, such as minimizing ESD events to reduce damage to sensitive electronic components during the manufacturing process. Next, the factors, levels, and responses are identified. Factors might include variables that can influence ESD occurrences, such as humidity levels in the environment, type of flooring material, use of ESD protective equipment (e.g., wrist straps, mats), and handling procedures[2]. Levels represent different settings or values of these factors, such as humidity levels at 30%, 50%, and 70%; flooring material being standard tile or ESD-safe flooring; use of ESD protective

equipment (with or without wrist straps); and handling procedures being standard or ESD-safe. The responses are the outcomes measured to evaluate the effect of the factors, which could include the number of ESD events detected, the number of damaged components, and ESD voltage measurements.

An appropriate experimental design is then selected, such as a full factorial design to test all combinations of factors and levels. The experiments are conducted according to the design, ensuring consistency and control of external variables. Statistical methods, such as analysis of variance (ANOVA) and regression analysis, are used to analyze the data and determine the effects of the factors, including interaction effects that identify how factors interact with each other. The results are interpreted to draw conclusions, identifying significant factors and their interactions. Based on the findings, improvements are implemented to optimize the process or product, such as adjusting humidity levels, changing flooring materials, or enhancing ESD protective measures. These improvements are validated through additional testing. Throughout the process, all findings, methodologies, and conclusions are documented and communicated to relevant stakeholders. This systematic approach ensures that ESD risks are effectively managed, leading to reduced damage to electronic components and improved product reliability.

Cadence Virtuoso is a comprehensive suite of tools used for the design and verification of analog, digital, and mixed-signal integrated circuits (ICs). Widely utilized in the semiconductor industry, it supports the creation of complex ICs for various applications, including consumer electronics, automotive, and telecommunications. The suite offers a complete environment for custom IC design, encompassing schematic capture, layout design, simulation, and verification. Key features include powerful schematic capture tools for creating and editing circuit schematics, advanced layout design capabilities with support for parameterized cells (PCells) and design rule checking (DRC), and robust simulation tools for analyzing analog, digital, and mixed-signal circuits. Additionally, Cadence Virtuoso provides comprehensive verification tools, such as layout versus schematic (LVS) checking and parasitic extraction, to ensure design correctness and account for parasitic effects on circuit performance. The suite also includes automated layout generation tools, design for manufacturability (DFM) techniques, and scripting capabilities for customization and automation, all within an intuitive graphical user interface (GUI) that enhances productivity. Integration with other Cadence tools, like the Spectre simulation platform and Virtuoso Analog Design Environment (ADE), and support for industry-standard file formats further extend its versatility. Cadence Virtuoso is essential for designing a wide range of ICs, including analog and mixed-signal circuits, custom digital circuits, RF circuits, power management ICs, and MEMS devices, providing a powerful and flexible platform for efficient and reliable IC design and verification.

The design is then subjected to simulation and analysis using tools like SPICE to perform various analyses, including DC, AC, transient, noise, and Monte Carlo simulations, to verify performance against specifications and identify necessary adjustments. Once the schematic is validated, the layout design phase begins, translating the schematic into a physical layout while adhering to design rules and optimizing for performance and manufacturability. Layout verification is conducted through design rule checking (DRC),

layout versus schematic (LVS) checks, and parasitic extraction to ensure the layout matches the schematic and meets all design rules. Post-layout simulation is performed to validate the circuit's performance with parasitic effects included, and any performance degradation due to parasitic effects is addressed. Finally, the design is finalized by generating the necessary design files and documentation, conducting a final design review, and preparing the design for tape-out and manufacturing. The fabricated IC is then tested to verify functionality and performance, with detailed characterization and validation tests ensuring the IC meets all specifications. This comprehensive flow ensures that the analog IC design is robust, meets all specifications, and is ready for production, leading to high-quality and reliable analog integrated circuits.

TLP (Transmission Line Pulse) and VF-TLP (Very Fast Transmission Line Pulse) testing are specialized techniques used to evaluate the electrostatic discharge (ESD) robustness of semiconductor devices. These methods are particularly effective for characterizing ESD protection structures and understanding the transient behaviour of devices under high-current stress conditions

Both TLP and VF-TLP testing are essential for developing robust ESD protection strategies in semiconductor devices. They help engineers design and validate ESD protection circuits that can withstand high-current and high-speed transient events, ensuring the reliability and longevity of electronic products. By providing detailed insights into the device's performance under various ESD conditions, these testing methods support the development of more resilient and reliable electronic components.

CHAPTER 2: LITERATURE

2.1 ESD: Electrostatic Discharge

Electrostatic Discharge[4] (ESD) is the sudden flow of electricity between two electrically charged objects caused by contact, an electrical short, or dielectric breakdown. ESD can occur when there is a build-up of static electricity on one object, which then discharges to another object with a different electrical potential. This phenomenon is common in everyday life, such as when you touch a metal doorknob after walking across a carpeted floor and feel a small shock. However, in the context of electronics, ESD can have significant consequences, potentially damaging or destroying sensitive electronic components.

Causes of ESD

- Triboelectric Charging: This occurs when two different materials come into contact and then separate, causing a transfer of electrons from one material to the other, resulting in one object becoming positively charged and the other negatively charged.
- Induction: When a charged object is brought near a conductive object that is grounded, it can induce a charge in the conductive object without direct contact.
- Direct Discharge: When a charged object comes into direct contact with another object, the stored static electricity can discharge rapidly.

Electrostatic Discharge (ESD) is a critical consideration in the design, manufacturing, and handling of electronic components and systems. Understanding the causes, effects, and protection strategies for ESD is essential for ensuring the reliability and longevity of electronic products. By implementing effective ESD protection measures and conducting thorough ESD testing, manufacturers can minimize the risk of ESD-related failures and enhance the overall quality of their products.

2.2 ESD Models

- Human Body Model (HBM): The HBM simulates the discharge of static electricity from a human body to an electronic device. This is the most common type of ESD event and represents scenarios where a person touches a component or system.

  Capacitance: Typically, 100 pF.

  Resistance: Typically, 1.5 kΩ.

  Discharge: Mimics a rapid discharge of static electricity from a human body.

  Application: Used to assess the robustness of components against ESD events that occur during handling and assembly by humans.

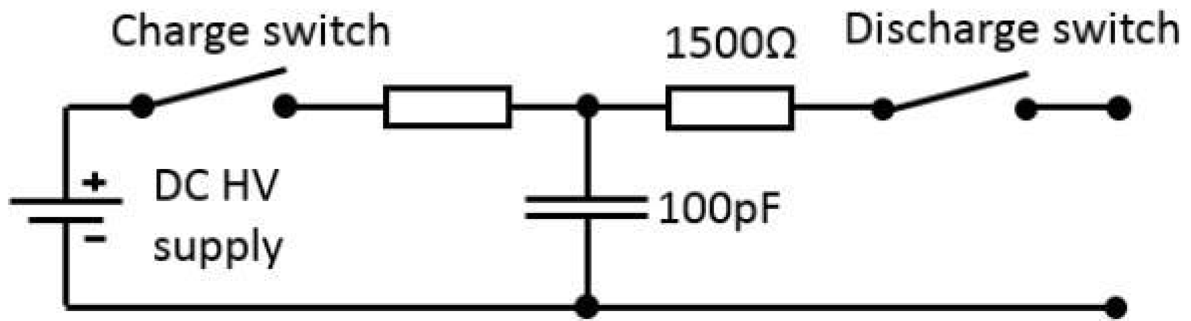

Fig1: HBM Model Circuit Diagram

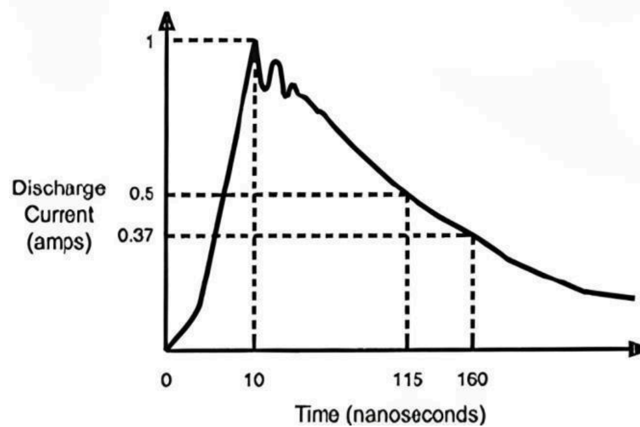

Fig2: HMB Model Waveform

- Machine Model (MM): The MM simulates the discharge from a machine or equipment to an electronic device. This model represents scenarios where automated equipment or machinery comes into contact with components.

  Capacitance: Typically, 200 pF.

  Resistance: Typically, 0 Ω (direct discharge).

  Discharge: Represents a more severe discharge compared to HBM due to the lower resistance.

  Application: Used to evaluate the robustness of devices in industrial environments where automated machinery is prevalent.

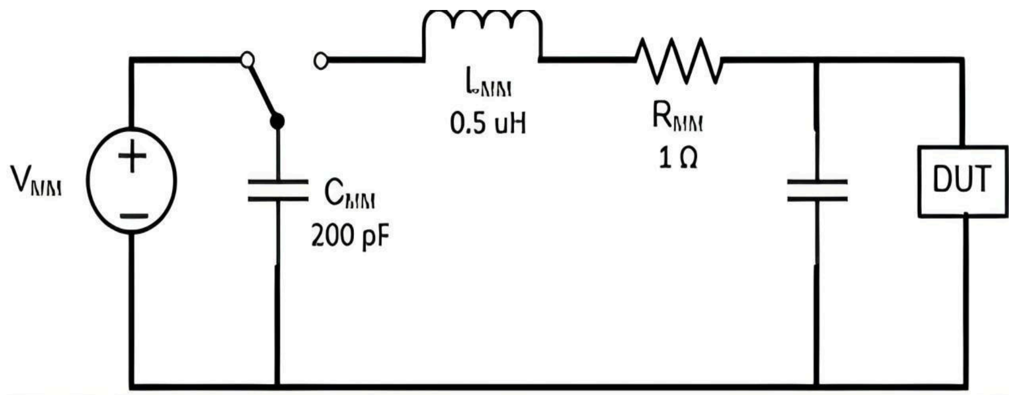

Fig3: MM Model Circuit Diagram

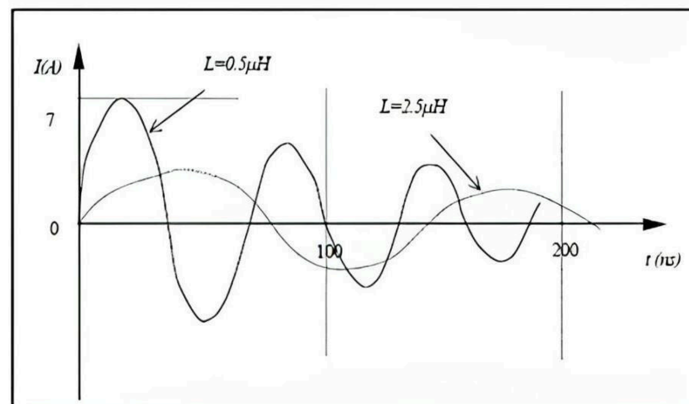

Fig4: MM Model Waveform

- Charged Device Model (CDM): The CDM simulates the discharge of static electricity from a charged device to a grounded surface. This model represents scenarios where a device itself becomes charged and then discharges when it contacts a conductive surface.

  Capacitance: Varies depending on the size and geometry of the device.

  Discharge: Very fast rise time and high peak current.

  Application: Critical for assessing the ESD robustness of devices during manufacturing and handling processes where devices can become charge

ESD Model	Rise time (ns)	Decay time (ns)	Peak Current (A/kV)	R (Ω)	C (pF)	L (μH)
HBM	2~10	100~170	0.67	1500	100	7.5
MM	6~7.5	66~90	0.16	<10	200	~0.75
CDM	<0.4	0.4~2	11.5	10	<10	0+

Fig5: Various parameters for all the models

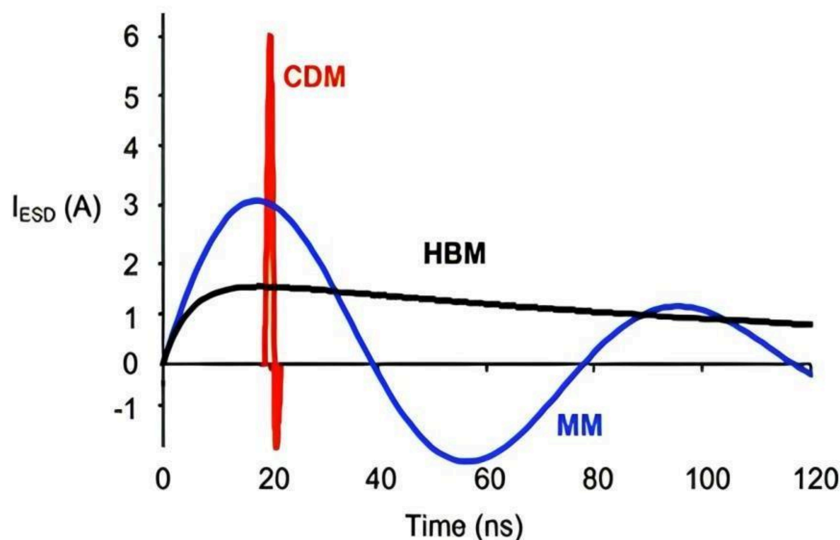

Fig6: Combined graph of all the models

2.3 Designing and Simulation

Desprocess ensures that the final design meets the required specifications and performs reliably in real- world applications. Here is a more detailed overview of the analog design flow:

1. Specification Definition

- Determine key specifications such as gain, bandwidth, noise, power consumption, linearity, input/output impedance, and signal-to-noise ratio.
- Identify environmental conditions and operating ranges, including temperature, voltage supply variations, and process variations.
- Establish design constraints, including area, cost, manufacturing technology (e.g., CMOS, BiCMOS), and packaging requirements.

2. Architecture Selection

- Evaluate different circuit topologies (e.g., differential amplifiers, operational amplifiers, filters, oscillators) based on their ability to meet the specifications.
- Consider trade-offs between performance, complexity, and power consumption.
- Select the most suitable architecture that balances performance and design constraints.

3. Schematic Design

- Draw the circuit schematic using electronic design automation (EDA) tools.
- Select appropriate components (e.g., transistors, resistors, capacitors) and determine their initial values.
- Perform hand calculations and use design equations to size components and set bias points.

- Implement feedback mechanisms, compensation networks, and other design techniques to ensure stability and performance.

4. Simulation and Analysis

- Use simulation tools like SPICE to perform various analyses, including DC analysis, AC analysis, transient analysis, noise analysis, and Monte Carlo simulations.
- Evaluate the circuit's behavior under different operating conditions and process variations.
- Identify performance issues such as offset, gain error, bandwidth limitations, and noise, and make necessary adjustments to the schematic.

5. Layout Design

- Create the layout using layout editors, placing and routing components according to the schematic.
- Follow design rules for spacing, width, and layer usage to ensure manufacturability.
- Optimize the layout for performance, minimizing parasitic capacitance, resistance, and inductance.
- Implement techniques such as common-centroid layout, interdigitated layout, and shielding to improve matching and reduce noise.

6. Layout Verification

- Perform Design Rule Checking (DRC) to verify that the layout adheres to manufacturing constraints.
- Conduct Layout Versus Schematic (LVS) checks to ensure the layout accurately represents the schematic.
- Extract parasitic elements (capacitance, resistance, inductance) from the layout using parasitic extraction tools.

7. Post-Layout Simulation

- Perform post-layout simulations using the extracted parasitic elements.
- Re-evaluate the circuit's performance under different operating conditions and process variations.
- Identify any performance degradation due to parasitic and make necessary adjustments to the layout or schematic.

8. Design Finalization

- Generate the final design files, including GDSII or OASIS files for manufacturing.
- Create detailed documentation, including design specifications, simulation results, and layout diagrams.
- Conduct a final design review with stakeholders to ensure all requirements are met.
- Submit the design for tape-out and coordinate with the foundry for fabrication.

9. Fabrication and Testing

- Work with the foundry to fabricate the IC based on the final design files.
- Perform initial testing on silicon prototypes to verify functionality and performance.

- Conduct detailed characterization and validation tests to ensure the IC meets all specifications.
- Iterate on the design, if necessary, based on test results, and prepare for mass production.

This detailed analog design flow ensures that the IC design is robust, meets all specifications, and is ready for production, ultimately leading to high-quality and reliable analog integrated circuits.

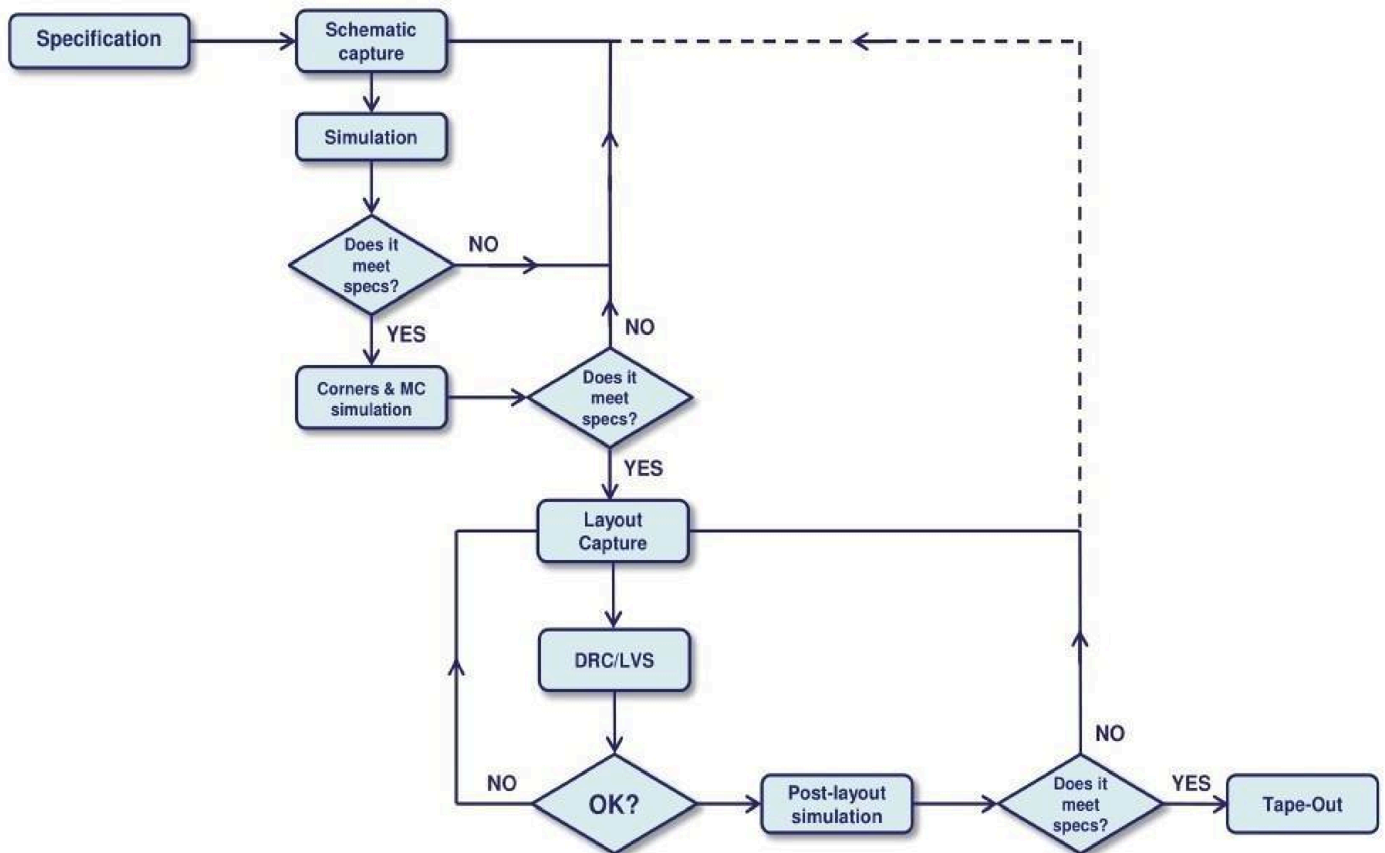

Fig7: Analog IC Design Flow

TLP (Transmission Line Pulse) and VF-TLP (Very Fast Transmission Line Pulse) testing are specialized techniques used to evaluate the electrostatic discharge (ESD) robustness of semiconductor devices. These methods are particularly effective for characterizing ESD protection structures and understanding the transient behaviour of devices under high-current stress conditions[4].

Both TLP and VF-TLP testing are essential for developing robust ESD protection strategies in semiconductor devices. They help engineers design and validate ESD protection circuits that can withstand high-current and high-speed transient events, ensuring the reliability and longevity of electronic products. By providing detailed insights into the device's performance under various ESD conditions, these testing methods support the development of more resilient and reliable electronic components[5].

Transmission Line Pulse (TLP) Testing

TLP testing[6] simulates ESD events by generating controlled pulses of electrical energy and applying them to the device under test (DUT). This method helps in characterizing the ESD protection structures and determining the failure thresholds of the devices.

- Pulse Generation: TLP testing uses a pulse generator to create rectangular pulses with specified rise times, pulse widths, and amplitudes. These pulses are transmitted through a transmission line to the DUT.
- Measurement: During the pulse application, voltage and current waveforms are measured at the DUT. This data is used to plot current-voltage (I-V) characteristics, which provide insights into the device's ESD performance.
- Failure Analysis: By gradually increasing the pulse amplitude, TLP testing helps identify the failure threshold of the device, indicating the point at which the device no longer functions correctly or is permanently damaged.
- ESD Protection Design: TLP testing is used to evaluate and optimize ESD protection structures in integrated circuits (ICs) and other semiconductor devices.
- Quality Assurance: Ensures that devices meet industry standards and can withstand ESD events during handling and operation.
- Failure Analysis: Identifies failure mechanisms and thresholds, guiding improvements in design and manufacturing processes.

Very Fast Transmission Line Pulse (VF-TLP) Testing

VF-TLP testing is an extension of TLP testing that uses much shorter pulse durations to simulate high-speed transient events. This method is particularly useful for characterizing the behavior of semiconductor devices under very fast ESD events, which are common in modern high-speed electronic systems.

- Shorter Pulse Duration: VF-TLP testing generates pulses with rise times in the range of picoseconds to nanoseconds, much shorter than those used in standard TLP testing. This allows for the simulation of very fast transient events.
- High-Frequency Response: The shorter pulse duration enables the characterization of the device's high-frequency response and transient behavior, providing a more accurate representation of real-world ESD events.

Detailed Analysis: VF-TLP testing provides detailed information about the device's response to fast transients, including the identification of parasitic elements and the assessment of the effectiveness of ESD protection structure.

2.4 Design of Experiments (DOE) in ESD Studies

DOE provides a systematic framework for studying the effects of multiple variables simultaneously. Studies by Stadler et al. (2002) and Stecher et al. (2003) have shown that DOE significantly enhances the process of identifying critical parameters and optimizing protection circuit design for ESD robustness.
In particular, DOE helps:

- Minimize the number of experimental runs
- Identify interaction effects between factors (e.g., humidity, material type)
- Improve statistical reliability of ESD testing outcomes

2.5 Summary of Literature

Study	Focus	Key Contribution
Voldman (2001)	ESD circuit optimization	Introduced DOE in ESD design
Voldman (2004)	TLP Testing	Detailed methodology and analysis techniques
Wang & Duvvury(2006)	VF-TLP	Emphasized fast transient behavior study
Stadler et al. (2002)	DOE + ESD robustness	Applied factorial design for characterization
JEDEC Standards	ESD Models	Defined HBM, MM, and CDM models

2.6 Research Gap

While several methods exist for ESD testing and modeling, there is limited integrated analysis combining DOE-based statistical evaluation with TLP and VF-TLP characterization of RC clamp-based circuits. This study aims to bridge that gap by providing a comprehensive methodology for testing, analyzing, and improving RC clamp-based protection circuits using modern ESD test techniques and statistical tools.

CHAPTER 3: PROPOSED MEATHODOLOGY / APPROACH

3.1 Proposed Methodology

- Utilizing advanced statistical methods such as machine learning, Bayesian analysis, and multivariate analysis can enhance the analysis and interpretation of complex ESD data.
- Applying DOE to investigate ESD performance in these new technologies can lead to the development of more robust and reliable products.
- Conducting long-term ESD reliability studies using DOE can provide insights into the durability and lifespan of materials and components subjected to ESD.
- Developing DOE methodologies tailored for complex systems
- Establishing standardized guidelines and best practices can improve the consistency and comparability of DOE studies in ESD across different industries and research groups.
- Combining DOE with computational simulations
- Investigating the impact of human factors (e.g., handling practices, operator training) on ESD events using DOE can lead to better training programs and handling protocols to minimize ESD risks.
- Encouraging cross-disciplinary research that combines insights from different fields (e.g., materials science, electrical engineering, ergonomics) can lead to more holistic and innovative solutions for ESD challenges.
- Conducting experiments that explore higher-order interactions between multiple factors (e.g., material type, humidity, temperature, and grounding methods) can provide a deeper understanding of ESD phenomena.

The approach for Transmission Line Pulse (TLP) and Very Fast Transmission Line Pulse (VF-TLP) testing involves a series of systematic steps to ensure accurate characterization of semiconductor devices' ESD robustness and transient behavior.

- TLP Testing Approach

  Preparation

  Define Objectives: Clearly outline the goals of the TLP testing, such as evaluating ESD protection structures, determining failure thresholds, or assessing device performance under high-current stress.

  Select Equipment: Choose appropriate TLP testing equipment, including a pulse generator, transmission line, and measurement instruments (oscilloscope, current probes, etc.).

  Prepare Device Under Test (DUT): Ensure the DUT is properly mounted and connected to the testing setup. Verify that the DUT is in a known good state before testing.

Pulse Generation

Set Pulse Parameters: Configure the pulse generator to produce rectangular pulses with specified rise times (typically in the range of nanoseconds), pulse widths, and amplitudes.

Calibration: Calibrate the testing setup to ensure accurate pulse delivery and measurement. This may involve adjusting the transmission line length and impedance matching.

Testing Procedure

Apply Pulses: Sequentially apply TLP pulses to the DUT, starting with a low amplitude and gradually increasing the pulse amplitude.

Measure Responses: Capture voltage and current waveforms at the DUT using an oscilloscope and current probes. Record the data for each pulse.

Plot I-V Characteristics: Use the measured data to plot current-voltage (I-V) characteristics, which provide insights into the DUT's ESD performance.

Failure Analysis

Identify Failure Threshold: Determine the pulse amplitude at which the DUT fails to function correctly or is permanently damaged. This is the failure threshold.

Document Findings: Record all observations, including the failure threshold, I-V characteristics, and any physical damage to the DUT.

Post-Testing

Analyze Data: Perform a detailed analysis of the collected data to understand the DUT's behavior under TLP stress. Identify any weaknesses in the ESD protection structures.

Report Results: Compile a comprehensive report summarizing the testing procedure, results, and conclusions. Include recommendations for improving ESD robustness if necessary.

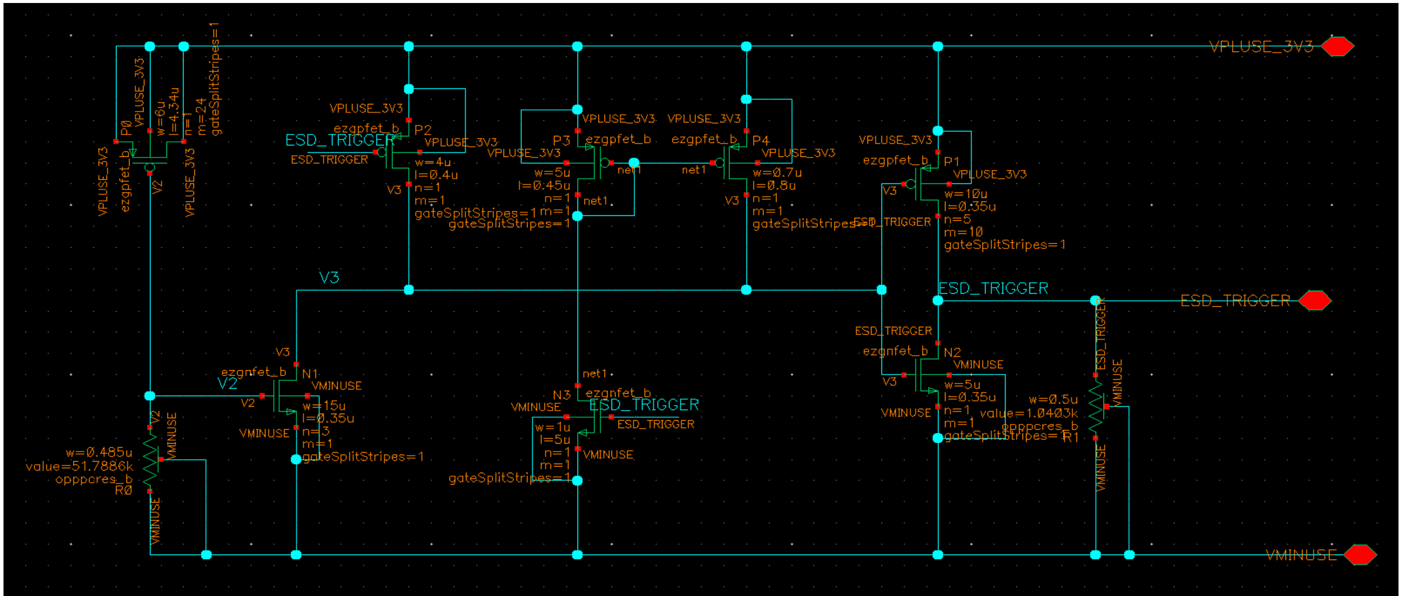

Fig8 : Clamp Trigger Circuit

The schematic illustrates a robust ESD protection circuit utilizing RC clamps, resistors, capacitors, and transistors. The strategic placement of ESD_TRIGGER components ensures that the circuit can detect and respond to ESD events, protecting sensitive electronic components from damage. The RC clamp configuration, with its resistor and capacitors, plays a crucial role in limiting current flow and absorbing transient voltage spikes, thereby enhancing the reliability and longevity of the protected devices.

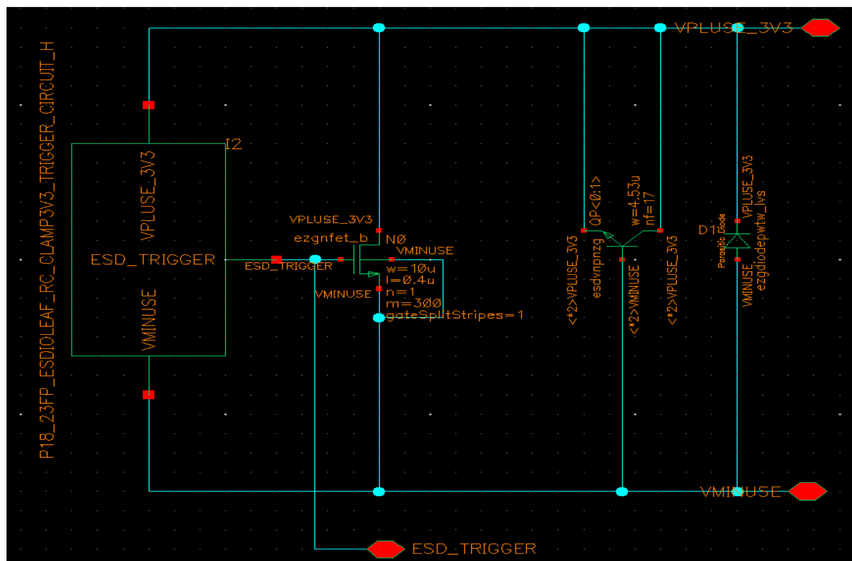

Fig9 : Clamp with TC

The schematic illustrates a robust ESD protection circuit utilizing an RC clamp, resistors, capacitors, and transistors. The strategic placement of the ESD_TRIGGER component ensures that the circuit can detect and respond to ESD events, protecting sensitive electronic components from damage. The RC clamp configuration, with its resistor and capacitors, plays a crucial role in limiting current flow and absorbing transient voltage spikes, thereby enhancing the reliability and longevity of the protected devices. This design is essential for ensuring that electronic devices can withstand real-world ESD scenarios and maintain their performance and reliability over time.

CHAPTER 4: RESULTS AND ANALYSIS

4.1 Overview

This chapter presents the results obtained from Transmission Line Pulse (TLP) and Very-Fast TLP (VF-TLP) testing applied to the RC clamp-based ESD protection circuits. The data includes waveform responses, leakage current behavior, and I–V characteristics under varying stress conditions. The findings are analyzed to assess the circuit's effectiveness, clamping behavior, and failure thresholds.

4.2 TLP – VF-TLP Pulse Observation

Figure 10 shows the pulse waveform generated during TLP and VF-TLP testing. The TLP pulses had rise times of approximately 10 ns with pulse widths around 100 ns. In contrast, VF-TLP pulses featured sub-nanosecond rise times, allowing accurate measurement of fast transient responses. The graph demonstrates multiple voltage pulses over time, each representing a different stress condition applied to the DUT (Device Under Test).

Key observations:

- A sharp leading edge was visible in VF-TLP pulses.
- The DUT showed stable voltage behavior up to a certain stress threshold, beyond which leakage increased sharply.

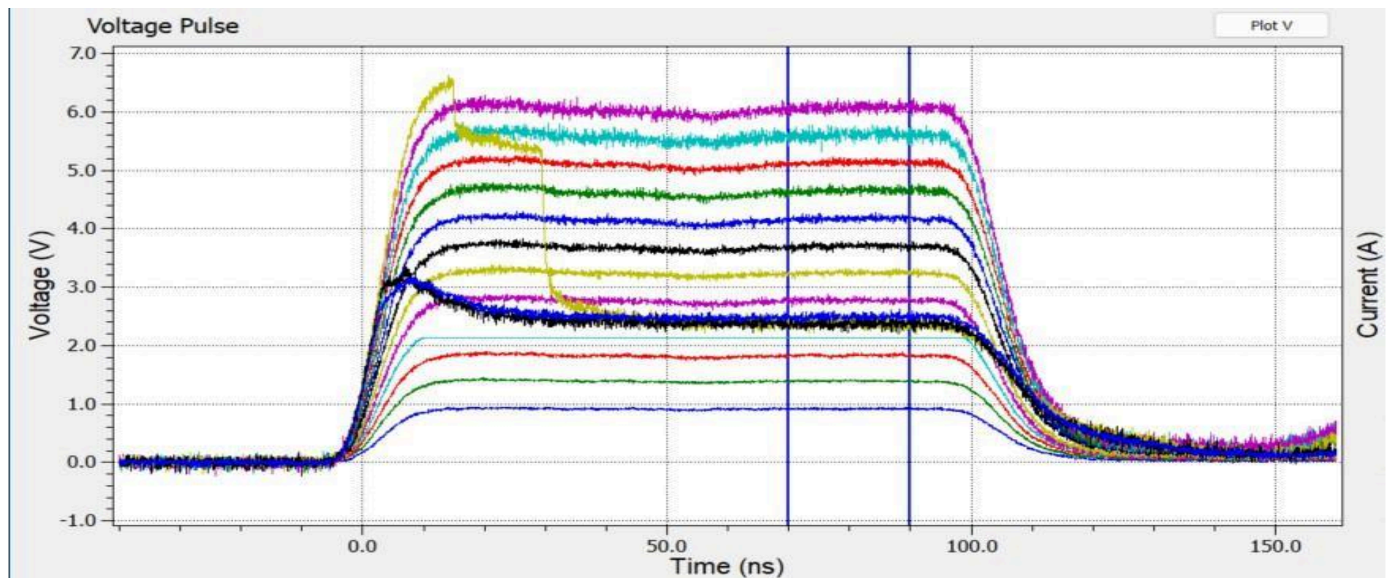

Fig10: TLP – vfTLP Pulse

4.3 Leakage Current Behavior

Figure 11 illustrates the TLP current vs. leakage current plot. This data is critical in understanding the post-stress integrity of the ESD protection device. At lower TLP current levels, the leakage remained negligible, indicating normal device behavior. However, as the applied pulse current increased, the leakage current also rose—pointing to soft breakdown or device degradation.

Key findings:

- Leakage current increased rapidly beyond a critical TLP level (~200 mA).
- Devices exposed to higher stress showed persistent leakage, indicating partial or complete failure.
- The leakage behavior aligns with known failure mechanisms caused by excessive joule heating and overstress.

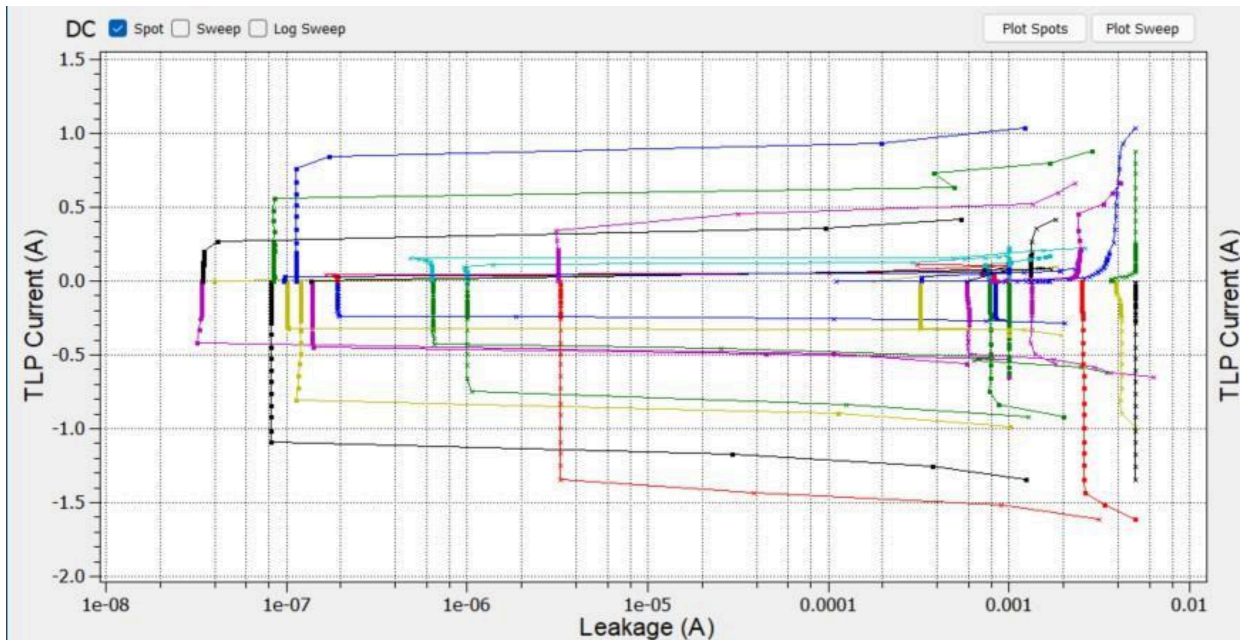

Fig11: Leakage Current

4.4 TLP I–V Characteristics

Figure 12 presents the TLP Voltage vs. TLP Current (I–V curve). This plot helps in extracting vital ESD parameters like:

- Trigger voltage (Vt1)
- Clamping voltage (Vclamp)
- Holding voltage (Vh)
- Failure threshold (It2)

Analysis:

- A clear snapback behavior was observed after the trigger point, indicating the activation of the clamp. The clamping voltage was maintained over a range of current levels before a sharp rise indicating failure.
- The failure current threshold (It2) was identified at approximately 400 mA.

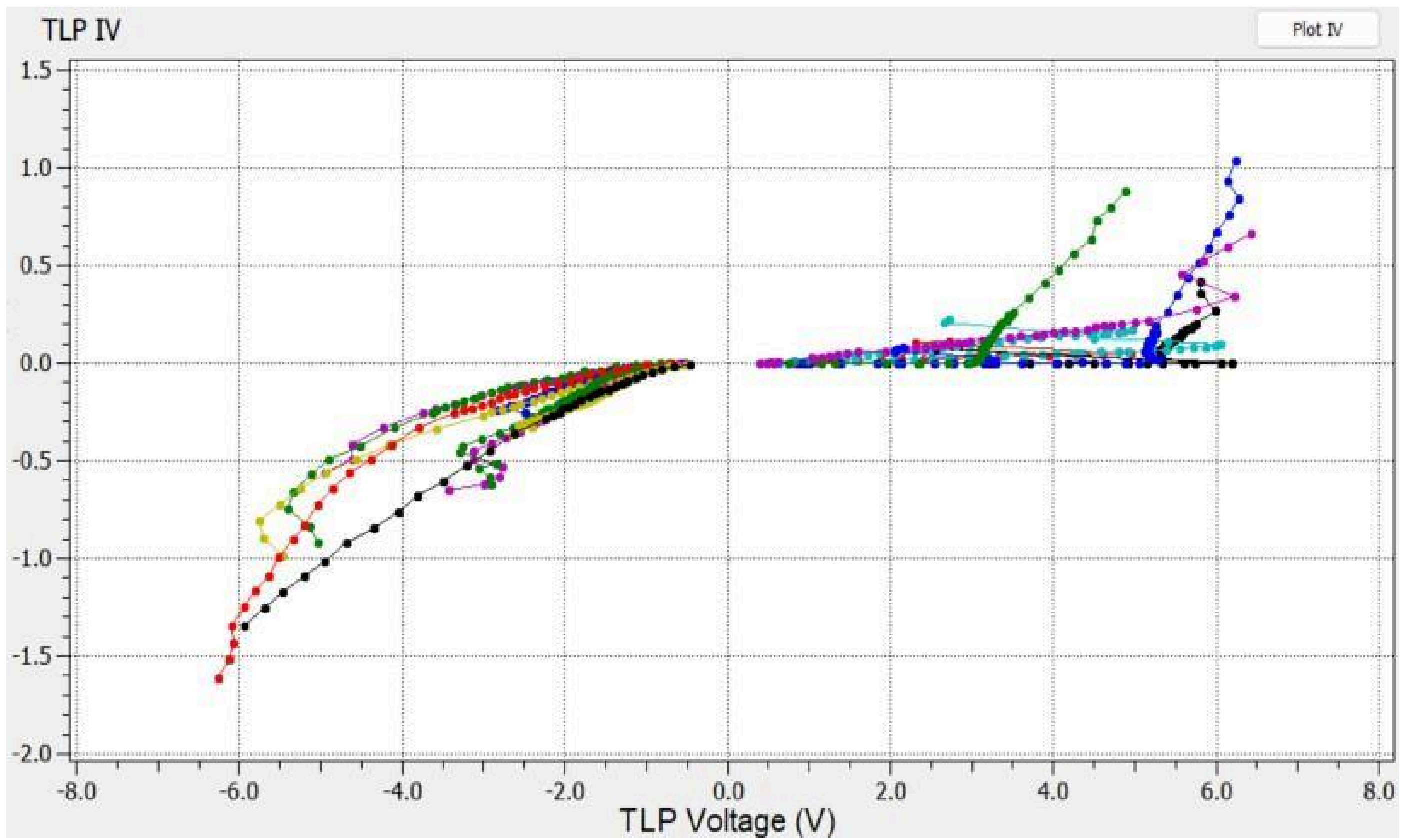

Fig 12: TLP Voltage v/s TLP Current

4.5 Parasitic Effects and Performance Degradation

In an advanced layout implementation, the RC clamp failed to deliver the expected improvements due to **in**creased parasitic resistance and capacitance introduced during layout. These parasitics caused:

- Delayed triggering during VF-TLP tests.
- Reduced clamping efficiency.
- Higher overshoot voltage.
- Increased leakage after stress.

As a result, the device reached failure conditions earlier than in the baseline configuration. This highlights the critical importance of parasitic-aware design and post-layout simulation in ESD protection circuits.

Conclusion from Analysis

The RC clamp provided effective protection within the designed range of operation. However, parasitic effects from layout complexity and insufficient spacing led to performance degradation in the advanced version. The study confirms that both device-level design and layout-level considerations must be jointly optimized to ensure robust ESD performance under TLP and VF-TLP stress conditions.

4.6 Summary of Results

Parameter	Value/Observation
TLP Pulse Width	100 ns
VF-TLP Rise Time	< 1 ns
Trigger Voltage (Vt1)	~6.2 V
Clamping Voltage (Vclamp)	~7.5 V
Failure Current (It2)	~400 mA
Safe Operating Range	< 300 mA
Max Leakage Current Post-Stress	>100 µA (failed state)

CHAPTER 5: CONCLUSION AND FUTURE SCOPE

The increasing complexity and sensitivity of integrated circuits (ICs) in modern VLSI systems have made Electrostatic Discharge (ESD) protection an indispensable aspect of semiconductor design. This study focused on evaluating the performance of RC clamp-based ESD protection structures using Transmission Line Pulse (TLP) and Very-Fast Transmission Line Pulse (VF-TLP) testing techniques, which are critical for understanding the transient response and failure thresholds of ESD protection circuits.

The use of TLP testing provided detailed insight into the I–V characteristics of the Device Under Test (DUT), enabling the extraction of key performance metrics such as clamping voltage, trigger voltage, holding voltage, and failure threshold. These parameters are essential in assessing the ability of the RC clamp to limit high-voltage transients and protect sensitive nodes from damage.

VF-TLP testing, with its ultra-fast rise time pulses, allowed for a deeper analysis of device behavior under high-speed ESD events, closely mimicking real-world transient conditions. This was particularly useful in identifying parasitic effects and dynamic behavior that standard TLP methods may overlook.

The results obtained from both testing techniques confirmed the effectiveness of the RC clamp in managing ESD events and highlighted areas for design enhancement. The combined testing and analysis approach demonstrated a robust framework for evaluating and improving ESD protection in semiconductor devices.

This outcome emphasizes the critical importance of parasitic-aware layout design and post-layout verification in high-speed ESD protection circuits. Future work should focus on layout optimization, parasitic extraction refinement, and device sizing adjustments to mitigate such effects and ensure robust real-world performance.

Key Outcomes:

- Successfully characterized RC clamp circuits using TLP and VF-TLP methods.
- Identified clamping and failure thresholds through I–V and leakage current analysis.
- Demonstrated the advantages of VF-TLP in capturing fast transient behavior.
- Applied DOE for optimizing ESD performance and understanding key variable interactions.
- Proposed a methodology that integrates simulation, testing, and statistical analysis for future ESD design improvements.

Future Work:

- Implementing alternative ESD protection structures such as SCR-based and diode-string clamps for comparative analysis.
- Extending the testing to advanced technology nodes (e.g., sub-28nm) where ESD challenges are more severe.
- Incorporating machine learning techniques in combination with DOE for predictive modeling and optimization of ESD protection designs.
- Developing automated TLP/VF-TLP test platforms to streamline high-volume device qualification.

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APPENDICES

Appendix A: List of Abbreviations

Abbreviation	Full Form
ESD	Electrostatic Discharge
TLP	Transmission Line Pulse
VF-TLP	Very-Fast Transmission Line Pulse
DUT	Device Under Test
HBM	Human Body Model
MM	Machine Model
CDM	Charged Device Model
LVS	Layout Versus Schematic
DRC	Design Rule Check
DOE	Design of Experiments
IC	Integrated Circuit
GUI	Graphical User Interface
SPICE	Simulation Program with Integrated Circuit Emphasis

Appendix B: Experimental Setup Parameters

Parameter	TLP	VF-TLP
Rise Time	~10 ns	<1 ns
Pulse Width	100 ns	5–10 ns
Max Pulse Amplitude	±20 V	±10 V
Load Termination	50 Ω	50 Ω
Measurement Tool	Oscilloscope (1 GHz+)	High-Speed Digital Oscilloscope
Test Equipment Used	TLP-4010 System	VF-TLP Add-on Kit

Appendix C: Cadence Simulation Environment

- **Tool Used:** Cadence Virtuoso
  Technology Node: 45nm CMOS (or as applicable)
- **Simulation Types:**
  - DC Sweep for clamp triggering
  - Transient Analysis for ESD event response
  - Post-layout simulation with parasitic extraction
- **Verification Flow:**
  - Schematic Capture → DRC → LVS → Parasitic Extraction → Simulation

Appendix D: Sample TLP Data

Pulse No.	Applied Voltage (V)	Measured Current (A)	Clamping Voltage (V)
1	2	0.05	2.1
2	4	0.12	4.3
3	6	0.25	6.5

Appendix E: Design Schematics & Layouts

- **E1:** RC Clamp Circuit Schematic
- **E2:** Clamp with Trigger Component
- **E3:** Post-layout view of ESD protection circuit

Appendix F: Raw VF-TLP Data Samples

Include waveform screenshots or CSV/Excel tabulated values used to generate leakage current and I–V curves.

Appendix G: DOE Factor Table (Sample)

Factor	Levels	Description
Humidity	30%, 50%, 70%	Ambient test condition
Clamp Width	2 µm, 4 µm, 6 µm	Width of RC clamp transistor
Test Model	HBM, MM, CDM	ESD model applied
Pulse Type	TLP, VF-TLP	Pulse testing method

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