Real Time Simulation of a PFC Rectifier Based EV Charger Employing CC/CV Mode of Charging

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DECLARATION

I hereby certify that the work which is being present in the dissertation entitled **"Real Time Simulation of a PFC Rectifier Based EV Charger Employing CC/CV Mode of Charging"** in partial fulfilment of the requirement for the award of degree of Master of Engineering in Power Systems submitted in the Electrical and Instrumentation Engineering Department of Thapar Institute of Engineering and Technology, Patiala is an authentic record of my own work carried out under the guidance of Dr. Mukesh Singh, Associate Professor, EIED.

The matter presented in the dissertation has not been submitted for the award of any other degree of this or any other university

Place: Patiala

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief

Date: 15/7/19

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ABSTRACT

Automobile industry has displayed an inclination towards establishment of Electric Vehicles (EVs) in the market. However, charging of EVs throws inevitable challenges due to inclusion of non-linear charger circuitry. The conventionally utilized AC-DC rectification in charger poses ruinous effects to Grid and EV structure in the form of harmonics interference and obnoxious spikes in current. Thus, repercussions of elevated THD can be witnessed in poor efficiency and deterioration of EV charger. Furthermore, harmonics in input inductor current produce harmonics in rectifier's output voltage. This can lead to DC link voltage fluctuation and adversely affecting of DC/DC converter functioning. Henceforth, a Power Factor Correction (PFC) rectifier based charger has been proposed that eliminates unwanted harmonics from input current and reduces THD. Moreover, harmonics in rectifier's output voltage are reduced and constant DC link voltage is obtained. Sinusoidal input current is maintained by Critical Conduction Mode (CrCM) and hysteresis current control application for power factor improvement. These are achieved using inner current and outer voltage control loop method. The former produces sinusoidal current wave in phase with input voltage to improve power factor. Whereas, the latter helps in achieving constant DC link voltage. Hence, THD factor of 1.30% and power factor of 0.9998 are recorded. In addition, model inculcates CC/CV charging algorithm to control overcharging of battery. Here, battery charges at Constant Current (CC) initially. Once, maximum voltage is reached, charging occurs at Constant Voltage (CV). It is governed by two isolated PI controllers. The collaborated work of PFC and CC/CV helps in recording model's efficiency of 96.8%. Furthermore, a 2 kW charger prototype is analysed using real time simulation and validated through Hardware-in-loop (HIL) results in OPAL-RT.

Keywords: CC/CV, CrCM technique, Hysteresis current control, OPAL-RT, PFC rectifier, Power factor improvement, THD reduction.

Chapter 1

INTRODUCTION

1.1 OVERVIEW

Recent years have witnessed a massive decline in the fossil fuels. Therefore, an inclination towards battery operated vehicles is noticeable [1] [2]. This transition from the conventional fossil fuel based vehicles to the EVs can be affiliated to the various merits of EVs over its counterparts. Electricity is a cleaner and greener source of energy with the advantages of wide availability, zero emission and lesser running cost. Hence, it proves to be beneficial for vehicle application [3].

EV requires a battery which can exhibit high density and promise longevity. Hence, Lithium-ion battery is preferred due to numerous advantages offered over respective counterparts. Owing to its low self discharge rate it showcases high efficiency in nature [4] . Moreover, it doesn't lose its usable capacity even if charged repeatedly on being partially discharged. This means no memory effect is present which is a rare commodity in other batteries such as lead acid battery. These attributes provide an upper hand to the Lithium-ion battery.

The complicated structure of battery demands a charger which can repeatedly charge it without affecting its performance. Therefore, it is important to take various parameters into consideration while developing charging infrastructure for battery. It should provide facilities of high power factor, low THD injection, good efficiency and controlled charging of the battery [5] [6]. Power electronics circuit used in charger should not generate harmonics in Grid and EV side. In addition, it should ensure sinusoidal nature of input current such that power factor is improved.

Various charging strategies have been talked about in the past but the rudimentary strategy opts

an AC-DC approach. Therefore, EV charger can be termed as an amalgamation of AC-DC and DC-DC converter. But, rectification of AC to DC value and further stepping down of obtained DC involves power electronics circuitry. Its non linear nature is responsible for harmonic injection and elevation of THD [7]. As an outcome, the Grid side output consists of ripples which affects the power factor leading to loss of useful power. Therefore, the charger's design is crucial for EV battery charging.

Evidently, battery charging mechanism is segregated into two halves. The first stage is responsible for generating stable DC link voltage, minimum THD and less harmonic injection into Grid [8] [9]. Since, the output of first stage acts as input for second stage, its non linearity can lead to fluctuations in the battery charging current and voltage. This can result in increased spikes and poor power factor.

In order to curb the drawbacks of first stage, it is imminent to design a special type of rectifier called PFC rectifier that is capable of delivering various benefits over traditional circuit. It will aid in eliminating the chances of production of extensive harmonics and offensive distortions in the supply current. This can be achieved by generating a sinusoidal input inductor current waveform in phase with input voltage. Hence, improvement in power factor can be observed and THD can be reduced. The charger should not be bulky in nature, should incur less losses, must be highly efficient and less costly.

Power Factor can be corrected by following either of the two methods listed as below:

1. Passive Power Factor Correction This method involves incorporation of inductors and capacitors for power factor improvement in case of capacitive and inductive loads respectively. This aids in offsetting the poor power factor generated by load.

2. Active Power Factor Correction This method involves semiconductor devices such as MOSFET, IGBT etc. for refining the power factor. There can be further two topologies of active power factor correction. These are described below:

- Buck converter is known to reduce the output voltage immediately when compared to the magnitude of input voltage. This results in reliability enhancement adding robustness to the system. But, buck converter is generally not preferred for improving power factor due to the 'inherent cross-over distortions' in the current waveform. Moreover, there is no direct path

from AC input to capacitor resulting in its less efficiency and increase in size. This is evident from Fig. 1.1 that there are distortions present in the current which will eventually lead to the poor power factor. Furthermore, the converter can be operated when the output voltage is lesser in magnitude than input voltage which leads to line current distortions

- Boost converter on the other hand is known to increase the output voltage magnitude in comparison to the input voltage magnitude. It is a favoured topology as a higher switching frequency can be achieved, therefore, low THD is obtained. As, the switch is not referenced to ground, the driver circuitry is easy to implement. Also, there is direct link between AC input and the capacitor, thus, reducing its size and increasing efficiency. The switch is turned off and on so rapidly that the input current is forced to follow the sinusoidal voltage and hence tending to make power factor unity.

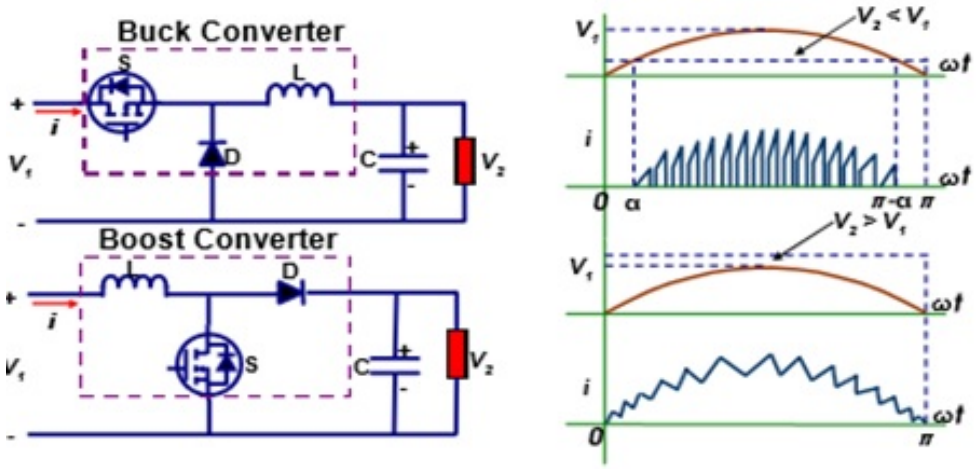


Figure 1.1: Comparison between buck and boost topology [14]

The second stage is responsible for ensuring controlled charging of battery, eliminating chances of overcharging and improving its longevity. Therefore, in order to generate controlled charge to battery various algorithms were devised such as Constant-Current (CC) and Constant-Voltage (CV). CC method showcases the ability to quickly charge the battery but it poses a problem of overcharging. The CV approach eliminates the problem of overcharging but increases the charging time. Hence, considering the drawbacks of both CC and CV modes, it is vital to implement a method which eliminates the flaws of algorithms and exhibits desirable controlled charging of

battery. Fig. 1.2 shows the basic structure of PFC rectifier in EV charger.

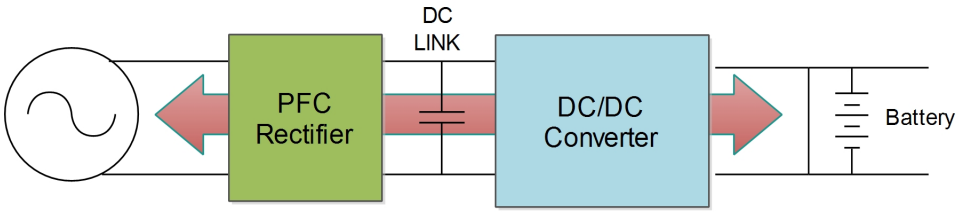


Figure 1.2: PFC rectifier in EV charger

1.1.1 NEED ANALYSIS

Power factor correction and hence its improvement is the basic necessity while developing the electric vehicle battery charger. This not only reduces the wastage of power but also manages to remove the periodic spikes and harmonics occurring in the input current waveforms. This is possible only if the power factor is corrected. It will help in safeguarding the components and hence maintaining the efficiency of the charger. The output of the battery will be free from harmonics and will not affect the electric vehicle. Also, the inclusion of controlled battery charging is necessary for smooth operation of the EV charger. It reduces the chances of over charging of the battery leading to loss of its effective capacity.

Therefore, the basic aim is to develop a power factor correction system that helps in developing nearly unity power factor by generating in phase voltage and current waveforms. Moreover, its objective includes incorporation of CC/CV charging of battery that helps in reduction of excess charging of battery. Boost converter due to its advantages over the buck converter is chosen to implement the active power factor correction topology for nonlinear loads.

1.2 LITERATURE SURVEY

Researchers have worked upon different PFC topologies to improve the power factor and quality of supply current. To make compact circuit, Liu and Chang [10] proposed reduction in inductor size by including an extra winding in transformer's primary of flyback converter. However, its use increased the size of the rectifier circuit. A boost PFC converter with its relevant control technique

had been proposed by Zhang and Xu [11]. It was operated in pseudo continuous conduction mode (PCCM) which provided fast transient response but failed to provide low THD. Therefore, a control technique based on discrete energy function was used by Das $et\ al.$ [12], that allowed PFC to run with quick dynamic response while maintaining a unity power factor. Also, a discontinuous conduction mode based PFC rectifier had been analysed by Lee and Chae [13], but it involved numerous switches making the system bulky. Hence, according to Yang $et\ al.$ [14], CrCM technique was preferable due to its easy implementation and zero requirement of creating pseudo limits because the switching of switch occurs at zero and peak of current. Also, the successful execution of PFC is possible when input inductor current and input voltage are in phase with respect to each other [15].

Apparently, among a number of PFC topologies, the boost topology was estimated to perform more efficiently, offering no inherited cross over distortions in the input current, smooth control and less THD in output [16]. Hence, present investigation aims at proposing a model which is a combination of diode bridge coupled with boost converter. Egan $et\ al.$ [17], discussed about its implementation using divider and multiplier circuits, peak and zero identification of voltage. The necessary calculations of L and C as provided in by Erickson and Maksimovic [18] and Hart [19] proved relevant.

Considering the second stage and keeping in view the limitations of CC and CV algorithm implementation, a new charging algorithm was devised that combined the advantages of both techniques. Therefore, for controlled charging of battery Constant-Current Constant-Voltage (CC-CV) has been utilised that charges the battery under two stages. In CC phase, the battery is charged with high constant current that is controlled to maintain around reference current value. Meanwhile, the voltage of battery keeps rising until it reaches a pre-set value, after which the charging mode is switched to CV charging [20] [21]. In this stage, it is the battery voltage which is held constant at pre-set value which results in a gradual decrease of charging current. Besides, a suitable control technique is required to regulate the charging current for the CC mode and the charging voltage for CV mode. Hence, two different PI controllers are employed to undertake this task.

It can be deduced from previous research work that limited focus has been put on incorporation of both PFC rectifier and CC/CV charging algorithm in EV charger. A few researchers have designed charger circuits by combining PFC rectifier with CC/CV charging. Faa-Jeng Lin $et\ al.$ [22]

proposed a charger which employed a PFC boost rectifier and a phase shift full bridge (PSFB) converter. They replaced the PI controllers with a probabalistic fuzzy neural network (PFNN) controller for implementing the CC/CV charging technique. Though, the authors were able to establish smooth transition between CC and CV modes but the input current THD was recorded at 4.1%. Later, a full bridge LLC based PEV charger was presented by Haoyu Wang $et\ al.$ [23] where an interleaved PFC rectifier was used and the THD was dropped down to a value of 3.6%. Chuan Shi $et\ al.$ [24] reduced the THD to as low as 2.72% and their proposed charger could recharge fully depleted batteries as well. Another charger with PFC and CC/CV charging was presented by Jun-Young Lee $et\ al.$ [13]. Their proposed PFC rectifier was based on discontinuous conduction mode (DCM) and a two stage DC-DC converter was employed for CC/CV charging.

However, all the above mentioned designs employed numerous switches and diodes which resulted in several losses and a bulky charger. Moreover, this paper has achieved a THD of 1.30% with an efficiency of 96.8% which is an improvement over all the above mentioned approaches. Radha Kushwaha $et\ al.$ [25] designed a charger based on PFC Sheppard Taylor converter and incorporated CC/CV charging in the circuit. They decreased the THD to 1.69% but used many switches and diodes to attain that feature. M.G. Eggan $et\ al.$ [17] have designed a power factor corrected single stage charger implementing resonant power conversion technique but, the overall efficiency obtained was 70%. Furthermore, authors in [24] have utilised sepic converter but, the THD value could be reduced to 2.72% and the efficiency was maintained between 88.5%-93.5%.

The proposed circuit which is a combination of boost PFC rectifier and DC-DC converter exhibits low THD and high efficiency. However, less literature is available on real time simulation of authors' proposed models that could provide verification of results. Few researchers have talked about real time analysis of their circuit. In [26], though the researchers have carried out real time simulation but, they failed to analyse their simulated and HIL results. Moreover, the battery takes huge number of hours to fully charge as the chosen current rating is very low. Therefore, the response time of simulated circuit is slow. The researchers in [27], have performed real time analysis of EV charger, however, inclusion of PFC circuit in the model is missing which eventually led to high THD factor. Also, the battery is charged at 1/3 C rate using only CC algorithm leading to slow charging of the battery. Hence, under this paper, real time simulation of the circuit has been carried out using OPAL-RT simulator that verifies the simulated and hardware results. The Analog

IN/OUT facility of OPAL-RT has been utilised and the results are observed on DSO.

1.2.1 MOTIVATION

A lot of research in literature has been contributed towards EV charging. Some of the key features can be referred as CC/CV charging algorithm and PFC rectification. EV charger devoid of PFC rectifier and controlled charging will be a source of harmonics, spike generations and over charging of battery. Though numerous researches had been focussed on PFC rectification and CC/CV charging, few is dedicated to inclusion of CrCM technique of correcting power factor. Moreover, the researchers were able to reduce the THD upto 2.72% with the attained efficiency of 93.5%. In addition, very few authors have included real time analysis of their model. Hence, this motivated the authors to amalgamate real time analysed controlled circuitry of PFC Rectifier and CC/CV mode of charging. This not only provides high power factor and efficiency but attains less THD and harmonic injection.

1.2.2 CONTRIBUTIONS

The major contributions of this paper are listed as follows.

- Detailed modelling, design and operational analysis of PFC rectifier is done to accomplish 0.9998 power factor, 1.30% THD and efficiency of 96.8% by optimal selection of control strategy and components.
- Controlled charging of battery is obtained through implementation of CC/CV algorithm using PI controller technique, ensuring fast charging and longevity of battery.
- Investigation of system is carried out through Matlab Simulink and experimental validation is done through hardware-in-loop (HIL) real time simulations in OPAL-RT.

1.2.3 ORGANISATION

The further thesis is organised as follows. The chapter 2 discusses about the system framework where working of the model is depicted. It tells the detailed working of the PFC circuit in collaboration with the controlled battery charging stage. The chapter 3 is regarding problem formulation

where the mathematical modelling of the system is discussed. It includes all the mathematical operations used for controlling and modelling of the proposed model of PFC rectifier based EV charger. Chapter 4 deals with developing of model on the OPAL-RT platform. Here, the simulation under real time analysis and the hardware implementation of the set up is carried out and the results are recorded. Chapter 5 discusses the results where the simulation and hardware waveforms are compared and verified. Finally, the thesis is concluded with future scope and work plan.

Chapter 2

SYSTEM FRAMEWORK

The proposed model is a PFC based EV charger which aims at reducing THD, improving power factor and efficiency to a great extent. This is achieved through realisation of CrCM based Boost PFC Rectifier that obeys zero current switching (ZCS). As a result, minimal switching losses are observed during turn on. Hence, output power comparable to input power can be generated resulting in improved efficiency. Moreover, the developed control strategy aims at reducing THD to a value of 1.30%. This is achieved through controlled co-ordination and accurate stabilization of outer voltage and inner current control by applied PI controllers. Furthermore, controlled charging of battery is attained through CC-CV charging whose functioning is balanced by two isolated PI controllers.

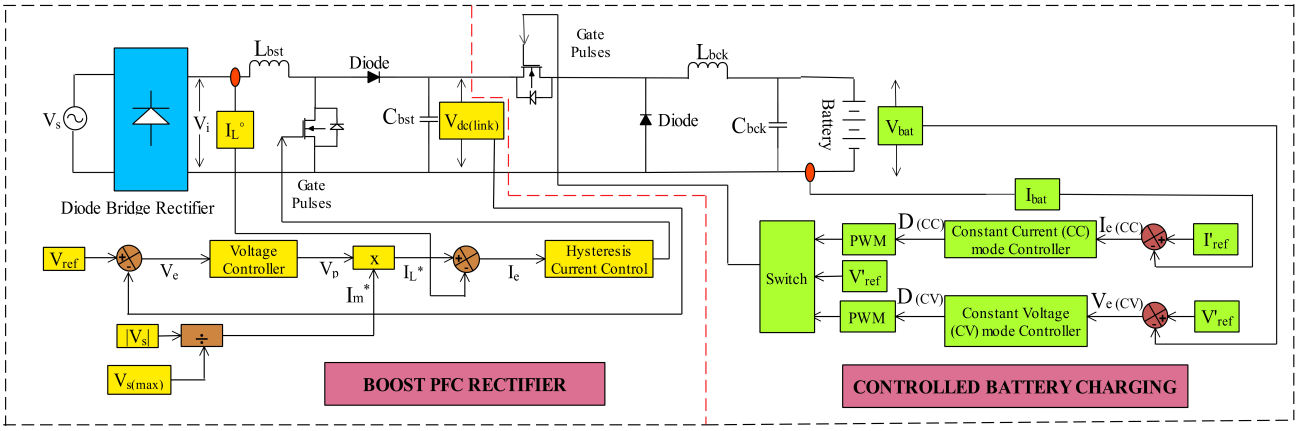


Figure 2.1: Block diagram of proposed charger

It can be observed from Fig. 2.1 that block diagram of PFC based EV charger charges the

battery in two stages. The first stage is the Boost PFC Rectifier stage whereas, the second stage is of Controlled Battery Charging using DC/DC buck converter. Considering first stage of Fig. 2.1, it involves diode bridge rectifier, boost converter and its control strategy. They perform in collaboration so that harmonics are eliminated from input inductor current, power factor is improved and constant DC link voltage is generated across boost capacitor, C_{bst}. The detailed working mechanism of first stage can be found as below.

2.1 BOOST PFC RECTIFIER STAGE

Initially, the source voltage V_{s} is converted to a pulsating DC voltage V_{i} via diode bridge rectifier as depicted in Fig. 2.1. This V_{i} acts as input for the boost converter of PFC rectifier. Boost converter plays a pivotal role as it adds a resistive load to the non linear rectifier's circuitry. Therefore, it aims to produce sinusoidal input inductor current in phase with the input voltage by eliminating harmonics and improving power factor.

The performance of boost converter is highly dependent on accurate execution of control strategy. It is further sectioned into two parts namely, outer voltage control loop and inner current control loop. The outer voltage control loop is responsible for generating constant DC link voltage at the output of boost converter. Whereas, the inner current control loop is responsible for generating sinusoidal input current in phase with the input voltage. Hence, proposed control strategy is capable of satisfying both objectives simultaneously.

Taking into account the outer voltage control loop, it involves voltage sensing circuit which generates constant DC link voltage across C_{bst}. Here, a reference voltage V_{ref} is set which is compared with the voltage $V_{\text{dc(link)}}$ sensed from C_{bst}. The obtained error behaves as input for the voltage controller mentioned in Fig. 2.1. This controller produces an output referred as peak voltage V_{p} that determines the peak magnitude of the input voltage.

Meanwhile, to generate accurate sinusoidal input inductor current in phase with respect to input voltage, inner current control loop begins its operation. For its implementation, a programmed current signal ${I_{\text{m}}}^*$ is produced as shown in Fig. 2.1. It is a replica of input voltage waveform but of unit magnitude in nature. Hence, this programmed signal when multiplied with V_{p}, generates reference current denoted as ${I_{\text{L}}}^*$. It has waveshape of input voltage and exhibits equivalent mag-

nitude. Now, the current signal from inductor, $I_L{}^0$ is sensed via implementation of high side direct sensing. Here, a shunt resistor is placed in series with the source and inductor. The voltage drop across the resistor denotes the sensed current which is compared with the reference current signal. This is done to give a sinusoidal waveshape to the inductor current by allowing it to follow reference current. The model follows CrCM operation to achieve an input inductor current sinusoidal and in phase with input voltage. Under this mechanism, the switch is turned on at zero current crossing and turned off when it touches peak. This leads to elimination of harmonics and generation of smooth current waveform. Furthermore, the error obtained after their comparison is send to hysteresis current controller. Here, the error produced is compared with the limit band. As a result, output in the form of pulses is observed which is used to drive the switch of boost converter. The advantage can be seen in less switching losses and easy control strategy implementation.

Hence, it can be observed that PFC rectifier serves two purposes. It utilizes outer voltage control loop to produce a constant DC link voltage and simultaneously uses inner current control loop to eliminate harmonics and thus, reduces THD. The power factor is improved by generating current waveform in phase with input voltage. THD factor is reduced to great extent by shaping input current waveform in sinusoidal nature. The proposed PFC rectifier block diagram is as shown in Fig. 2.2

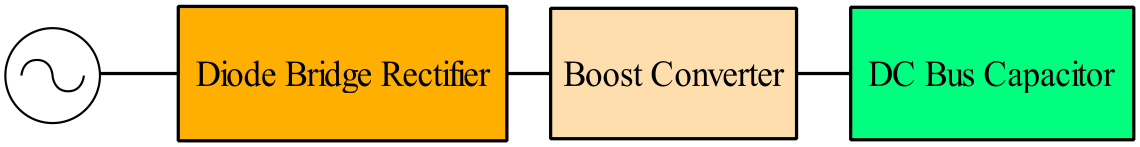


Figure 2.2: Proposed PFC rectifier topology

2.1.1 FUNCTIONING OF BOOST PFC RECTIFIER STAGE

2.1.1.1 AC TO DC SIGNAL

The 220 V AC signal is converted to 12 V AC signal via a step down transformer which is further converted to 10.8 V DC signal via a bridge rectifier. The obtained output acts as input to the boost converter.

2.1.1.2 BOOST CONVERTER

The boost converter portrays a pivotal role in PFC rectifier infrastructure. It emphasizes on managing unity power factor through rapid switching of switch utilizing duty cycle variation approach. However, the duty cycle is monitored through comparison of detected error with sawtoothwave signal, hence, generating controlled pulses. This phenomenon allows the input current, I_l^0, to trace the sinusoidal path followed by the input voltage. The converter generally works in two stages as shown in Fig. 2.3 and Fig. 2.4.

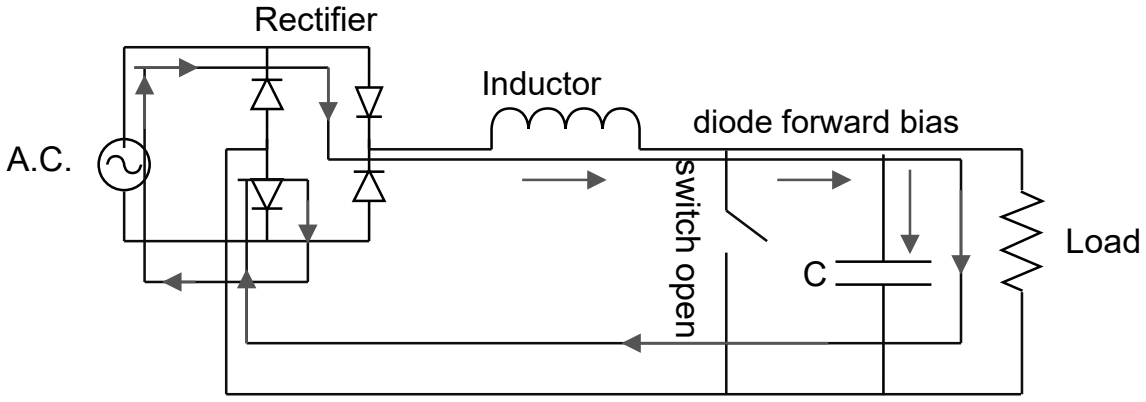


Figure 2.3: Boost converter with open switch

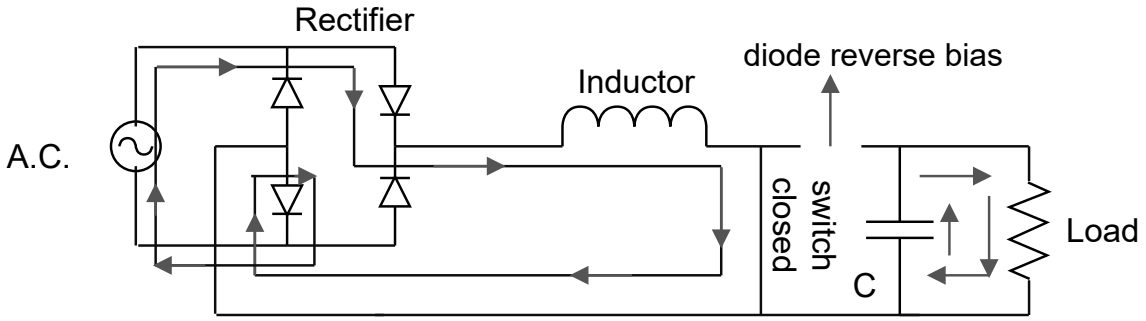


Figure 2.4: Boost converter with closed switch

2.1.1.3 CRITICAL CONDUCTION MODE TECHNIQUE

In this system, the boost PFC Rectifier works under the implementation of CrCM technique. This ensures the switching of switch to occur whenever the current flowing in the system reaches peak or zero of the current limit. Moreover, the diode current follows the envelope. Hence, there is no requirement of maintaining the current within its specified limits. As an outcome, an easy

control strategy can be employed as no virtual bands have to be designed for ensuring current not to exceed zero and peak. Whereas, in the Continuous Conduction Mode, the switching operation occurs between peak and zero current crossing. Therefore, upper and lower pseudo limits have to be drawn that do not allow current to surpass the virtually created bands. This makes, control strategy′s implementation tedious in nature and the circuitry becomes complex. Henceforth, CrCM technique has been used for the model and its pictorial view is depicted in Fig. 2.5.

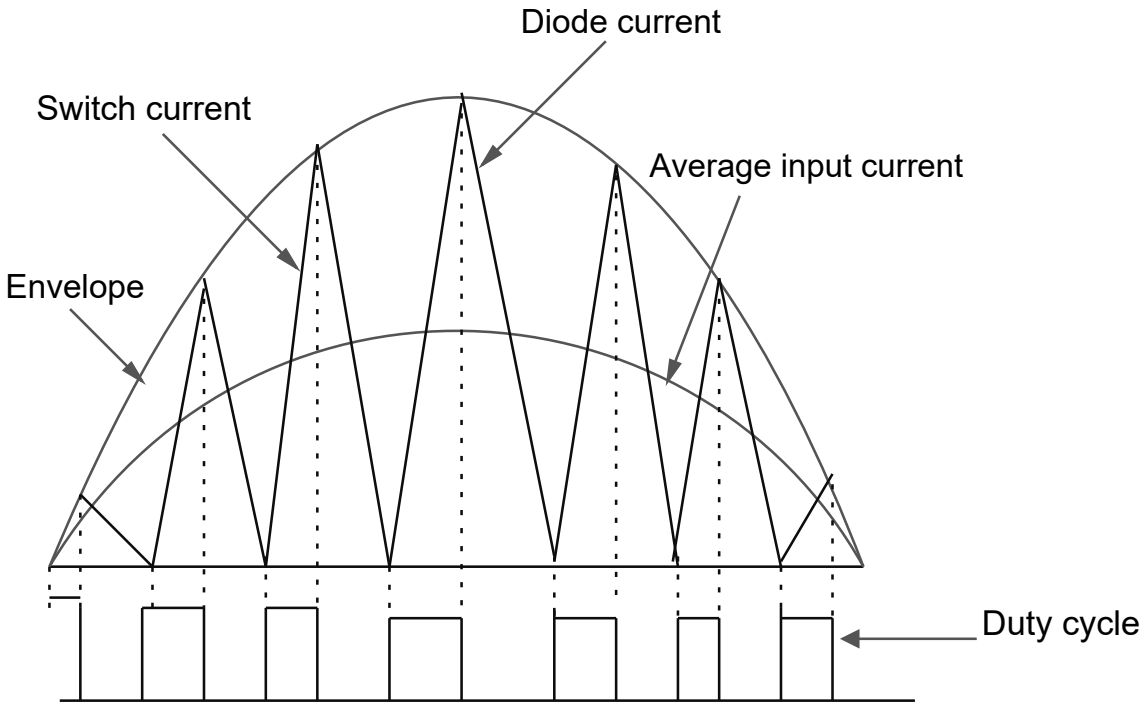


Figure 2.5: CrCM technique

2.1.1.4 VOLTAGE SENSING

For accurate working of the model, a constant and harmonic free voltage has to be generated at DC link. The harmonic free DC link voltage is achieved by ensuring elimination of harmonics from V_{i}. In order to generate a constant DC link voltage, it is compared with a reference voltage V_{ref}. The outer voltage control loop is responsible for producing constant DC link voltage.

2.1.1.5 CURRENT SENSING

The basic objective of including PFC is to generate a sinusoidal input inductor current which is in phase with input voltage. Hence, current ${I_{\mathrm{L}}}^{0}$ is sensed at the inductor which is compared with the reference current signal ${I_{\mathrm{L}}}^{*}$. The error generated is tuned using an inner current control loop. This helps in producing an input inductor current sinusoidal in nature which is in phase with input voltage.

2.1.1.6 PULSE GENERATION

A Hysteresis current control technique is utilised in this model to generate controlled pulses to switch. The error generated after comparison of ${I_{\mathrm{L}}}^{*}$ and ${I_{\mathrm{L}}}^{0}$ is compared with the limits of hysteresis band. Hence, triggering pulses are generated to the switch. This helps in snubbing of harmonics present in the current waveform by forcing it to follow reference current waveform which is sinusoidal in nature.

2.1.2 FUNCTIONING OF CONTROLLED BATTERY CHARGING STAGE

The second stage of proposed EV charger as depicted in Fig. 2.1, is of controlled battery charging. It utilizes DC/DC buck converter to charge the battery using CC/CV mode of charging. Its working mechanism is explained as follows.

The constant voltage at the DC link namely V_{dc} behaves as input for the buck converter. Nominal, maximum and cut-off voltages are assigned to the battery according to the requirement of designed model. The limits of PI controller are assigned in a way that charging voltage doesn't violate maximum and cut-off voltage range. Intially, the charging of battery is carried out in CC mode because it charges the battery at faster rate achieving almost 80% of total charging. Here, a current refernce, ${I'}_{\mathrm{ref}}$ is set and compared with current sensed from battery, I_{bat}. Since, during charging the value of sensed current will vary, a Constant Current (CC) mode Controller is employed which will tune the error according to reference value. This controller generates pulses to drive buck converter's switch during CC mode.

However, during this phenomenon, the battery's SoC rises quickly and the charging voltage gradually increases. The increasing battery voltage, V_{bat} is compared with refernece voltage, ${V'}_{\mathrm{ref}}$.

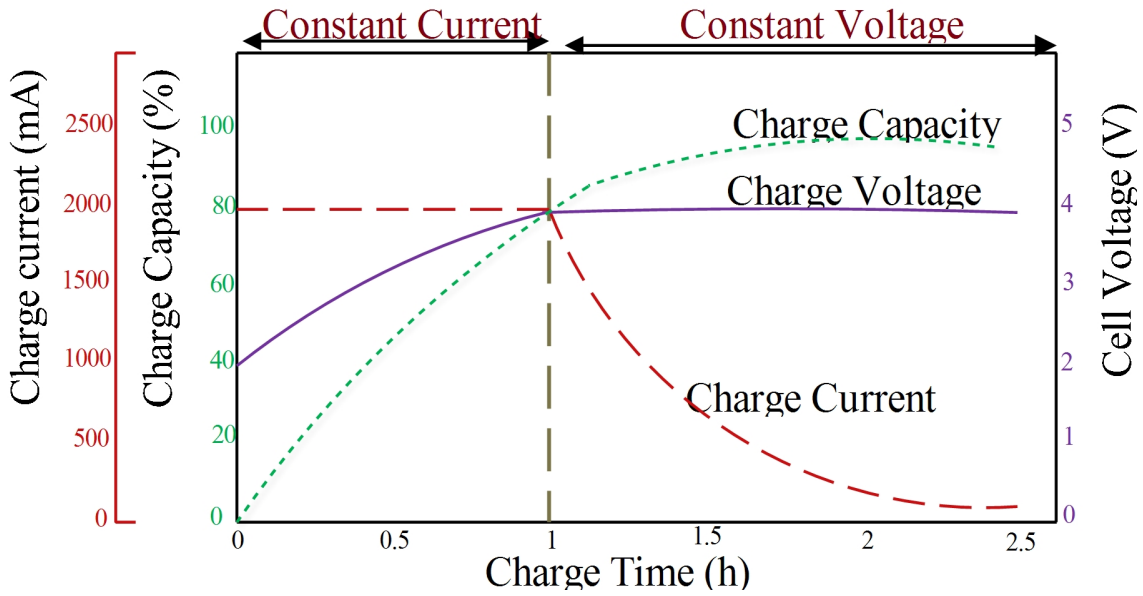


Figure 2.6: Characteristics curve of constant current and constant voltage

Once, V_{bat} reaches V'_{ref} or the maximum voltage, it is held constant at that value. At that instant, the threshold switch makes transition from CC to CV mode. This is incorporated to eliminate chances of excessive charging. Constant Voltage (CV) mode Controller is employed to tune the error according to reference value. This controller is responsible for generating pulses to drive buck converter's switch during CV mode. As the charging current drops exponentially to a value $1/10^{\text{th}}$ of the I'_{ref}, the difference between battery voltage and charging voltage decreases.

Hence, it can be analysed that the proposed model of EV charger aims at reducing harmonic content through its implemented control strategy. By generating in phase sinusoidal input current and voltage, it manages to improve the power factor. Also, the controlled charging battery by employing CC/CV charging algorithm through PI controller helps in eliminating the chances of over charging of battery.

Chapter 3

PROBLEM FORMULATION

This section focusses on modelling details of proposed EV charger. Here, emphasis is laid on developing simple and fast control strategy for the proposed model. The objective is to achieve high power factor, high efficiency, low THD factor and minimised switching losses. Hence, the equations are formulated in order to meet specifications as mentioned in Table. 5.1. This section is divided into two parts namely, Boost PFC Rectifier and Controlled Battery Charging each with further subcategories. Their mathematical and operational analysis is carried out separately as below.

3.1 BOOST PFC RECTIFIER

Observing the block diagram of Boost PFC rectifier from Fig. 2.1, a compact design has been obtained by keeping minimum number of switches. This block aims at reducing the harmonic interference and THD thereby, improving power factor. Therefore, the foremost target is to realise near sinusoidal input inductor current waveform. To achieve this, the controlling and modelling equations of PFC rectifier are discussed below.

3.1.1 CONTROLLING OF BOOST PFC RECTIFIER

The AC signal namely the source voltage V_{s} received from Grid, is converted to pulsating DC input voltage V_{i} at the diode bridge rectifier's output with the help of following equation.

$$V_i = 0.9 * V_{rms} \tag{3.1}$$

where V_{s} is,

$$V_s = V_{s(max)} sinwt \tag{3.2}$$

In order to generate a current signal of magnitude and shape as V_{i}, its maximum value has to be identified. Therefore, RMS value of source voltage denoted by V_{rms} is utilised for obtaining maximum value of V_{s} using the below stated equation.

$$V_{s(max)} = V_{rms} * \sqrt{2} \tag{3.3}$$

Further, using (3.2) and (3.3), ${I_{\mathrm{m}}}^*$ is obtained as suggested in in the following equation. It is a signal having waveshape of input voltage but, of unit magnitude and pulsating DC nature.

$${I_m}^* = \frac{|V_s|}{V_{s(max)}} = \frac{|V_{s(max)} sinwt|}{V_{s(max)}} \tag{3.4}$$

In order to generate a constant voltage at DC link an outer voltage control loop is designed. For its successful implementation, V_{ref} as observed from Fig. 2.1 is compared with $V_{\mathrm{dc(link)}}$. The error generated denoted by V_{e}(t) after comparison can be analysed using following equation.

$$V_e(t) = V_{ref} - V_{dc(link)} \tag{3.5}$$

Now, this error behaves as input to voltage controller as mentioned in Fig. 2.1. It is reduced by implementing PI controller as mentioned in (3.6). Here, the output received after tuning of controller is referred as peak voltage waveform, V_{p}. It is pulsating DC in nature with a magnitude comparable with V_{i}.

$$V_p = K_{p1} * V_e(t) + \frac{K_{p1}}{T_i} * \int V_e(t) dt \tag{3.6}$$

where, K_{p} is the proportional constant and $\mathrm{K_p/T_i}$ is the integral constant.

For realising a sinusoidal input current waveform, a reference current signal has to be generated which is replica of V_{i} in shape and magnitude. It is achieved through inner current control loop. Thus, V_{p} and ${I_{\mathrm{m}}}^*$ as obtained using (3.6) and (3.4) respectively, are used to generate ${I_{\mathrm{L}}}^*$ according to (3.7). The peak voltage waveform when multiplied with a unit magnitude signal produces an output of peak voltage magnitude. Thus, ${I_{\mathrm{L}}}^*$ received is pulsating DC in nature.

$$ {I_L}^* = V_p * {I_m}^* \tag{3.7} $$

Furthermore, current signal sensed from the input inductor is compared with the reference current waveform. Henceforth, ${I_{\mathrm{L}}}^*$ as obtained from (3.7) is compared with ${I_{\mathrm{L}}}^0$ for error detection. The error denoted by I_{e}(t) can be analysed using the following equation.

$$ I_e(t) = {I_L}^* - {I_L}^0 \tag{3.8} $$

In order to generate controlled pulses to switch, the error I_{e}(t) has to be minimised. Hence, it is fed as input to hysteresis current control loop. The error is compared with upper and lower limit of hysteresis loop. The output received in the form of pulses drives switch of boost converter whose duty ratio can be expressed as,

$$ V_{dc(link)} = \frac{V_i}{1 - D} \tag{3.9} $$

The power factor of proposed EV charger after implementation of Boost PFC rectifier stage can be calculated using the following equation which can be found in [18].

$$ P.F. = g * cos(\alpha) \tag{3.10} $$

Where, 'g' is the distortion factor and '$cos(\alpha)$' is the displacement factor and 'g' can be expressed as,

$$ g = \frac{1}{\sqrt{T.H.D.^2 + 1}} \tag{3.11} $$

3.1.2 MODELLING OF BOOST PFC RECTIFIER

A CrCM based boost converter has been modelled. It includes a boost converter that aids in power factor improvement by implementation of CrCM and hysteresis current control technique. The modelling of boost converter includes calculation of inductance 'L' and capacitance 'C' parameters. The mathematical value of L_{bst} lies between $L_{\text{bst(min)}}$ and $L_{\text{bst(max)}}$ which are evaluated as below.

$$L_{bst(min)} = \frac{V_i * D}{2 * f_s * I_{L(avg)}} \tag{3.12}$$

$$L_{bst(max)} = \frac{V_i * D}{f_s * \triangle I_L} \tag{3.13}$$

where, f_{s} is switching frequency, $\triangle\ I_{\text{L}}$ represents the permissible current ripple and $I_{\text{L(avg)}}$ denotes average inductor current. The relation between $\triangle\ I_{\text{L}}$ and $I_{\text{L(avg)}}$ can be found in the following equation.

$$\frac{\triangle I_L}{2} = I_{L(avg)} \tag{3.14}$$

Since, under CrCM operation the switch begins to conduct when current flowing through it touches zero. Hence, it can be deduced that current through L touches zero momentarily. Thus, in CrCM the L_{bst} will be assigned $L_{\text{bst(min)}}$. Therefore, (3.12) will be used to calculate mathematical value of L_{bst}.

In practical applications, the $I_{\text{L(avg)}}$ is calculated as,

$$I_{L(avg)} = 5\% * I_{source} \tag{3.15}$$

The capacitance 'C' of the boost converter can be found by using the equation as mentioned under.

$$C = \frac{V_{dc(link)} * D}{\triangle V * R * f_s} \tag{3.16}$$

Here, 'R' is the load resistance.

This formulates the mathematical controlling and modelling operations of the PFC rectifier stage. These equations can be implemented easily and have less complex strategy.

3.2 CONTROLLED BATTERY CHARGING STAGE

Battery is charged using CC/CV mode of charging algorithm. It is charged intially with Constant Current with voltage rising. When this voltage crosses the pre-set voltage, charging of the battery resumes with constant voltage mode. Here, voltage is held constant while the current starts to drop touching zero. The detailed explanation can be found underneath.

3.2.1 CONTROLLING OF BATTERY CHARGING

In CC mode, the current flowing to the battery has to be kept constant. Thus, I_{bat} is compared with the reference current I'_{ref} to generate error $I_{\text{e(cc)}}$(t) to CC controller. This is represented using the following equation.

$$I_{e(cc)}(t) = I_{bat} - I'_{ref} \tag{3.17}$$

The error produced acts as input for the CC mode controller which generates PWM pulses to the buck converter switch after verification of criteria. The duty cycle D_{CC} will be generated via condition switch till I_{bat} and I'_{ref} are equal. It verifies the condition of incrementing voltage touching pre-set voltage. If the condition is false, D_{CC} will be passed to buck converter switch. It is obtained as,

$$D_{CC} = K_{p(CC)} * I_{e(CC)}(t) + \frac{K_{p(CC)}}{T_i} * \int I_{e(CC)}(t)dt \tag{3.18}$$

Once, the voltage sensed from the battery V_{bat} becomes equal to the reference voltage V'_{ref}, the condition in the 'condition switch' becomes true. As a result, D_{CV} will be generated to the buck converter switch. The equation is obtained as under.

$$V_{e(CV)}(t) = V_{bat} - V'_{ref} \tag{3.19}$$

$$D_{CV} = K_{p(CV)} * V_{e(CV)}(t) + \frac{K_{p(CV)}}{T_i} * \int I_{e(CV)}(t)dt \tag{3.20}$$

3.2.2 MODELLING OF BUCK CONVERTER

The model incorporates a buck converter to charge the battery. This is necessary to step down value of $V_{\text{dc(link)}}$ to a value which is battery compatible. The modeling of inductance L_{bck} and capcitance

C_{bck} can be calculated using the follwing equations.

$$L_{bck} = \frac{(V_{in} - V_0) * D}{\triangle I_L * f_s} \tag{3.21}$$

$$C_{bck} = \frac{\triangle I_L}{8 * f_s * \triangle V_0} \tag{3.22}$$

The efficiency, η, of proposed EV charger can be evaluated as mentioned in below equation. Since, V_{bat} and I_{bat} vary, the output power vary. Therefore, it affects the input power. However, at any point of time, the ratio of P_{out} and P_{in} remains constant.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{bat} * I_{bat}}{V_s * I_s * cos(\alpha)} \tag{3.23}$$

It can be deduced that the implementation of proposed model relies on proper execution of various equations of control strategy and appropriate selection of the components. It is the synchronisation of both the stages that will provide desired outputs.

Chapter 4

SYSTEM MODELLING IN OPAL-RT PLATFORM

The model of the system is prepared using OPAL-RT for real time simulationa and hardware-in-loop results. The need of modelling the system in OPAL-RT is to achieve real time analysis of the system. This helps in evaluation and validation of simulated and the hardware-in-loop results. Hence, the model is intially simulated in OPAL-RT and finally hardware results are observed on DSO through application of Analog and digital IN/OUT pins. The main features of OPAL-RT are numerous. It is compact and powerful with 2U real time target with upto 4 Intel processor cores 3.3 GHz. The real time operating system is either QNX or Linux Redhat. It uses Xilinx Kintex 7 FPGA. It consists of total of 96 fast I/O channels with 16 analog in, 16 analog out, 32 Dout and 32 Din. It also includes Rear DB37 connectors and RS422 DB9 connectors. The optical interface is 4-optional 2G-bits SFP. It has synchronised connectors with detailed status display of LEDs. Fig. 4.1 depicts the OPAL-RT.

Figure 4.1: OAL-RT System [28]

4.1 OPAL-RT SIMULATION

Considering the various steps involved in processing of OPAL-RT model are listed as below:

- Create a Matlab Simulink model of the system. This involves modifications in powergui as the OPAL-RT platform runs under discrete fixed time step.
- Once, the Simulink model is prepared, it is important to include it in a broader project. Here, more than one models can be included under a single project. In RT-lab enivironement, click on File>New> RT-Lab Project.
- Open the Simulink model and keep the GUI interface such as scope, display etc. at one end while the plant model on one side.
- Now, select the plant and create one subsystem. Similarly, select all the scopes whose data has to be recorded and create another subsystem.
- Referring to Fig. 4.2, the plant model is renamed as SM_model and the GUI part is renamed as SC−scope. It can be explained that 'M' stands for Master whereas, 'C' stands for console.
- The SM−model can be further sectioned in subsystems. Referring to Fig. 4.3, the SM is divided into plant and controller. The plant model consists of the developed circuitry for the charger. On the other hand, the controller consists of the control circuitry for the charger.
- Considering the SC subsystem, here, the communication has to be developed between the master and console for obtaining the outputs. Hence, an Opcomm block is kept between the inputs received from the master and outputs present in console.
- Once, it is done the OPAL-RT developed model is run under its environement. Now, each model will behave as a target in RT-LAB environment. This is necessary for the OPAL-RT and Host PC to communicate with each other.
- Under the master subsystem, an 'opctrl' block can be added. Under this block a .mat file will be there which save all the necessary data that can be retrieved after the simulation is over. Also, an 'Opwrite' block is added through which the inputs are taken whose data has to be

saved in .mat file. If it is more than one, then a MUX is used which will receive all inputs and send it to opwrite block for data analysis.

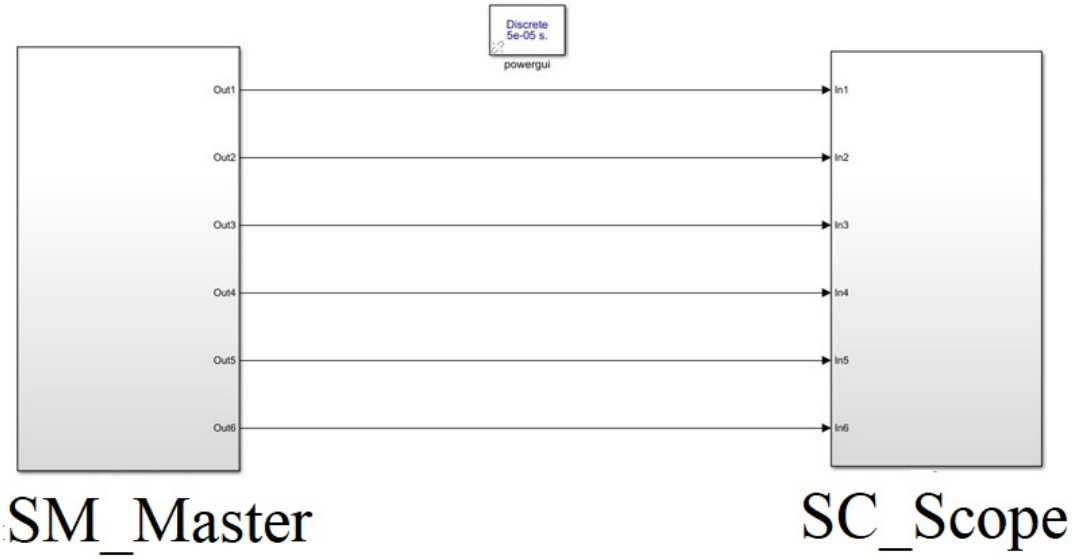


Figure 4.2: Modelling of OPAL-RT subsystem

- After that click on 'Build'. This helps in transforming the matlab simulated model into a complete real time simulation model. It is necessary to click on this every time any changes are incorporated in the matlab model.

- Once, the building of the model is complete, click on 'load' which will be activated just after the successful building of model. It is used for preparation of real time target to perform the simulation.

- The loading of the model will consume some time as the matlab model is loaded in the OPAL-RT for its execution. Click on 'Excecute' which will start the excecution of real time simulation on the target. The real time excecution of the model will start and the values will be stored in a .mat file.

- Once, the execution of the model is over, the data is saved in the OPAL-RT and has to be retrieved back to host PC for its analysis. Hence, click on the 'reset' which will be activated once execution is over. This will retrieve the data and save it on matlab environment.

Therefore, by following various steps involved, the OPAL-RT simulation can be carried and the results can be recorded.

The Fig. 4.2 shows master and console subsystems. The master contains plant and controller subsystems of EV charger that runs in OPAL-RT and console contains the scope which runs in the Host PC after loading of model. The communication between the two occurs through OpComm. The simulated results are verified with the DSO results. For the DSO results, Opctrl and analog out are used and board type TE0741 is used in 2B1 module of OPAL-RT. The plant model contains the EV charger and PFC circuitry whereas controller consists of CC/CV algorithm implementation and DC link voltage control. Fig. 4.3 shows the OPAL-RT developed plant and controller model.

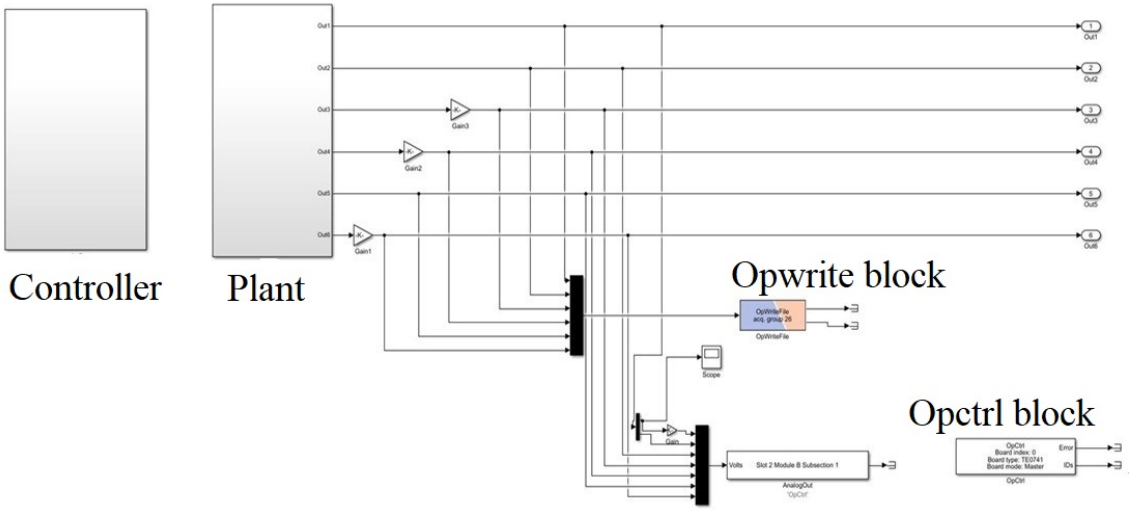


Figure 4.3: Plant and controller subsystem in OPAL-RT

4.2 HARDWARE-IN-LOOP

The hardware-in-loop refers to the testing and building of complicated models under real time analysis environment. It is platform where the complex plant model can be tested for the control action implemented. The Fig. 4.4 shows the various ports available for hardware in loop execution. It can be observed that it consists of 2 groups which have different slots. The group 1 has Module A and Module B. Also, group 2 has Module A and Module B. The RT-Lab's Simulink blocks used to access the I/O's in the OPAl4510 simulator use the following ID nomenclature, $SlotX.ModuleY.SubsectionZ$.

Figure 4.4: Channel configuration of OPAL-RT [28]

For the result analysis of the system, both analog and digital I/Os are required. Hence, there are various steps involved for performing hardware-in-loop mechanism. Analog inputs are utilised for receiving and sensing battery voltage and current. Hence, input 2A module is used. One set of pins are used for directly obtaining the signals. On the other hand, digital output has to be send in the form of pulses to the switch. Hence, in order to satisfy this prerequisite 1B module is utilised. The steps that have to included in the OPAL-RT hardware are as follows:

- After resetting of the model and storing simulation results, connections have to be made in analog and digital boards. Firstly, analog and digital blocks have to kept in the master subsystem.
- In the analog block, add the conf. file name which and select the board type. Choose the number of channels where the connections will be made and save the changes.
- Similarly for the digital output block, add the conf. file and make the changes in the prt from where output has to be received.
- Connect both the boards in the respective slots behind OPAL-RT and build, load, execute the model. This can be run for infinite time.
- Observe the waveforms on DSO for the verification of the results.

Thus, both simulation and hardware-in-loop results are necessary and can be taken by following the procedure involved in this section.

Chapter 5

RESULTS AND DISCUSSION

This section draws comparison between simulated and hardware-in-loop (HIL) results according to the model specifications mentioned in Table. 5.1. The simulation results are carried out using OPAL - RT under Matlab Simulink environment. These real time simulated results are validated through HIL introspection of model. A 2 kWh EV battery charger is simulated and experimentally analyzed for the desired outputs. The detailed discussion is described in the sections following.

Table 5.1: Design paramerters of proposed EV charger

Symbol	**Quantity or device**	**Specification**
V_s	Source Voltage	230 V/50 Hz
V_{ref}	Reference Voltage	300 V
L_{bst}	Boost Inductor	40.738 mH
C_{bst}	Boost Capacitor	0.03875 F
K_{p1}	Proportional Constant for PFC Rectifier stage	0.03
K_{i1}	Integral Constant for PFC Rectifier stage	0.3
L_{Bck}	Buck Inductor	0.096
C_{Bck}	Buck Capacitor	0.625 uF
f_s	Switching Frequency	5 kHz
V'_{ref}	Reference Battery Voltage	134 V
I'_{ref}	Reference Battery Current	15 A
$K_{p(CC)}$	Proportional Constant for CC mode Controller	10
$K_{i(CC)}$	Integral Constant for CC mode Controller	0.095
$K_{p(CV)}$	Proportional Constant for CV mode Controller	5
$K_{i(CV)}$	Integral Constant for CV mode Controller	0.01

5.1 SIMULATION RESULTS

A Lithium - Ion EV battery of 15 Ah capacity with 120 V as the nominal voltage is charged at 1C rate utilizing Boost PFC rectifier and controlled battery charging. The source voltage is 230 V/50 Hz sinusoidal wave. Each of the diodes used in the circuit has an ON state resistance of 0.001 ohms. The forward voltage drop in each diode is 0.8 V. The active switches used in the charger are N channel MOSFETs having ON state resistance of 0.1 ohms. The simulated results are sectioned into two categories which are further described.

5.1.1 BOOST PFC RECTIFIER STAGE

Initially, the source voltage is converted to rectified pulsating DC voltage V_{i} using diode bridge rectifier. The Fig. 5.1 represents sinusoidal source voltage V_{s} of RMS 230 V and its equivalent output after rectification is depicted in Fig. 5.2 denoting rectified pulsating DC voltage, V_{i} .

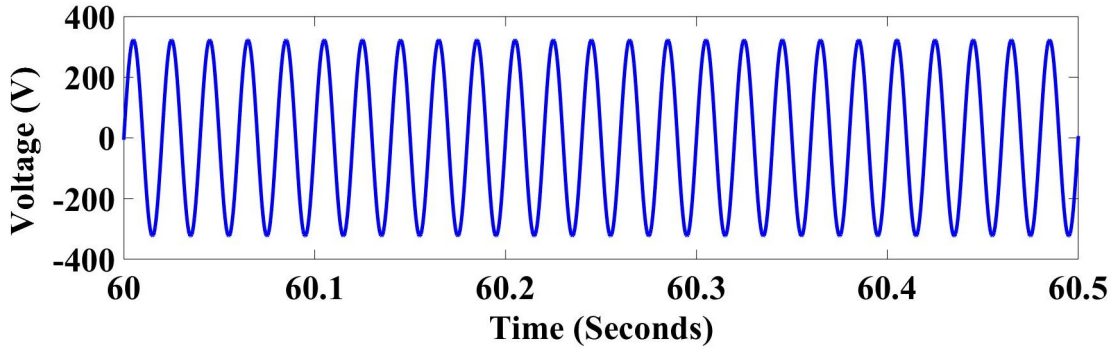


Figure 5.1: Source Voltage

This figure illustrates that the source voltage having the maximum voltage of 325 V has been received while performing the real time simulation. It shows that the source voltage is sinusoidal in nature as practically observed, hence supporting the rms value of 230 V. On the other hand, after rectification, the number of cycles have increased but the amplitude remains the same as per source voltage amplitude. It suggests accurate rectification of the source voltage.

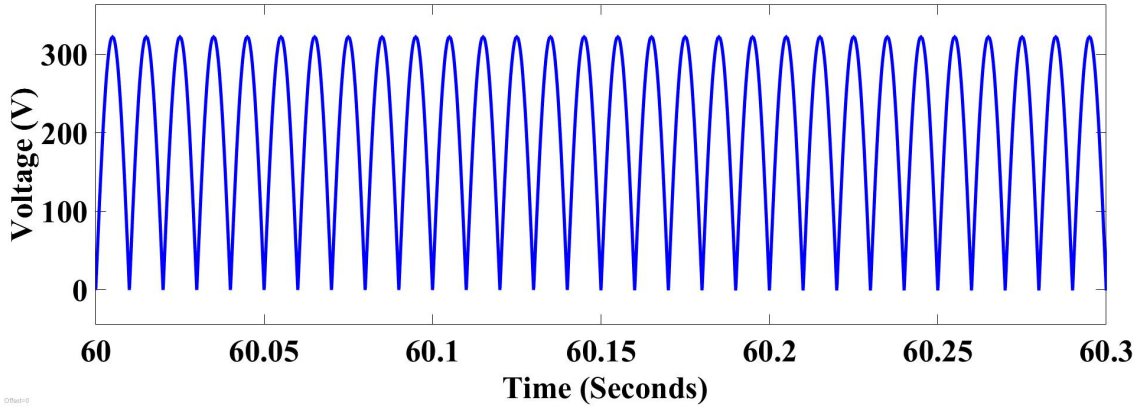


Figure 5.2: Rectified pulsating DC voltage

The PFC rectifier stage is responsible for improving power factor, generating constant DC link voltage and reducing THD by input current's waveshaping. To achieve these objectives, the control strategy is segregated into outer voltage and inner current control loop as explained through Fig. 2.1 in section II. The outer voltage control loop is responsible for generating constant DC link voltage across C_{bst}. Hence, it focuses on maintaining $V_{\text{dc(link)}}$ about set V_{ref}. It can be observed from Fig. 5.3 that the voltage control loop has successfully produced a constant DC link voltage of 300 V after initial transient state. It assures fast response and constant input to the buck converter owing to the accuracy of controlling of the voltage control loop.

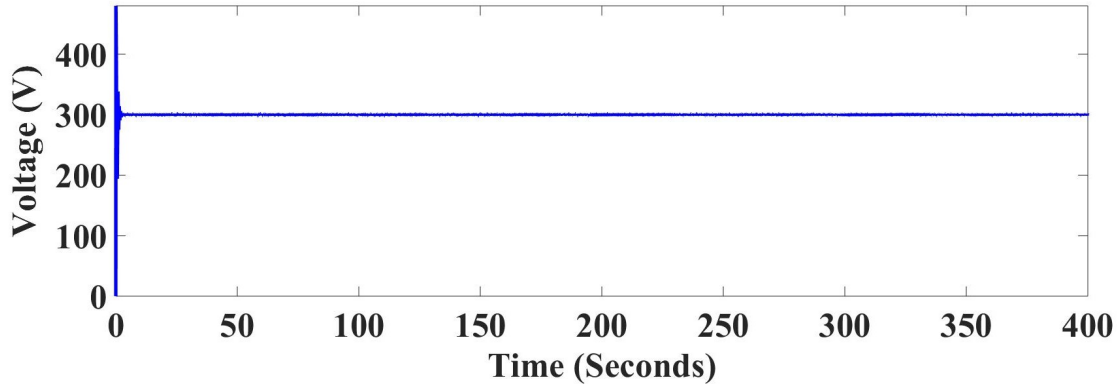


Figure 5.3: DC link voltage

Furthermore, the inner current control loop is responsible for producing pulsating DC input inductor current. It is dedicated towards waveshaping of the current and removing harmonic contents in the signal. Hence, it is evident from Fig. 5.4 that current waveform of pulsating DC nature is successfully obtained via accurate controlling of the current control loop. This futher aids in

deduction of harmonic interference with the EV circuitry.

In addition, the input inductor current generated should be in phase with respect to the rectified voltage. It is necessary for boosting the power factor of the system. This is realised by allowing inductor current to follow the voltage waveform. Hence, it can be observed from Fig. 5.5 both are in phase with each other achieving zero phase lag between them.

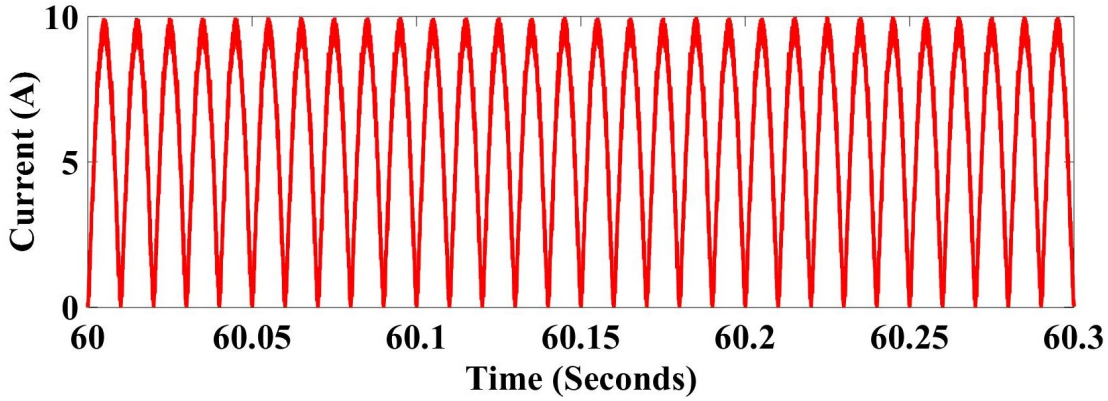


Figure 5.4: Input inductor current

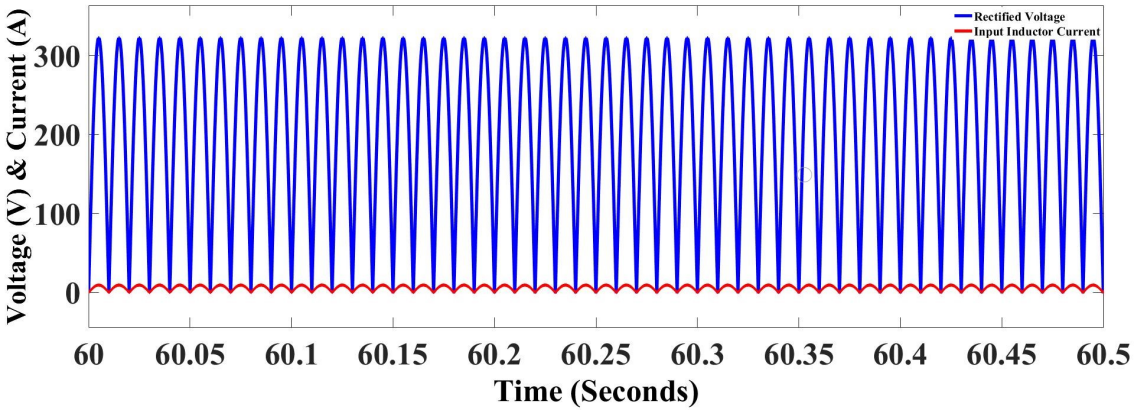


Figure 5.5: In-phase input inductor current and rectified voltage

Moreover, the generation of pulsating DC input inductor current and sinusoidal source current leads to the reduction of harmonics entering into the EV charger. These waveforms are recorded during CC mode of charging battery. Evidently, Fig. 5.4 and Fig. 5.6 showcase accuracy of inner current control loop as harmonics are reduced extensively due to the realization of sinusoidal nature of current signals. This eventually leads to the reduction of THD factor.

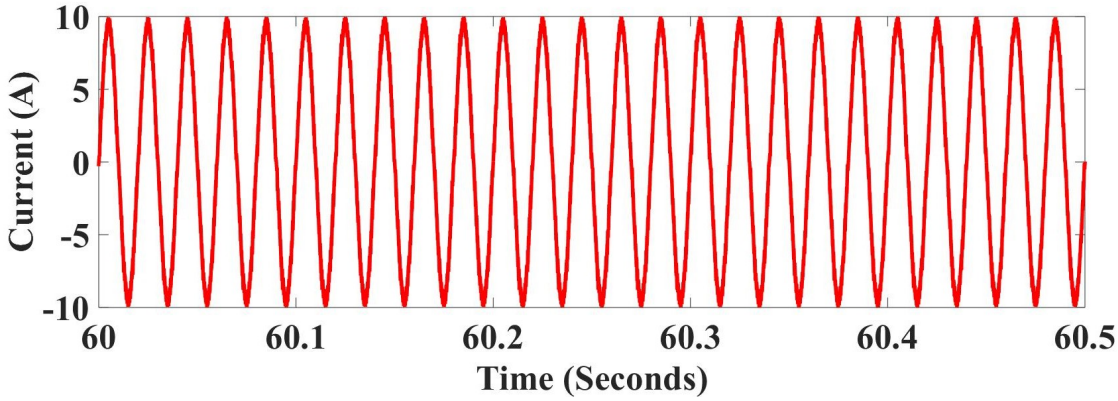


Figure 5.6: Source Current

As an outcome of harmonic minimisation, power factor of the model is improved. It can be observed from the Fig. 5.7 that source voltage and source current are in phase with each other. The zero crossing of source voltage coincides with the zero crossing of source current. Thus, it can be said that there is zero phase angle between voltage and current and displacement factor is unity. Also, Fig. 5.2 and Fig. 5.4 support high power factor as both input voltage and input current are in phase with each other. Therefore, a resistive load is achieved with the inclusion of PFC rectifier which clearly indicates high power factor. The recorded power factor was found to be equal to 0.9998.

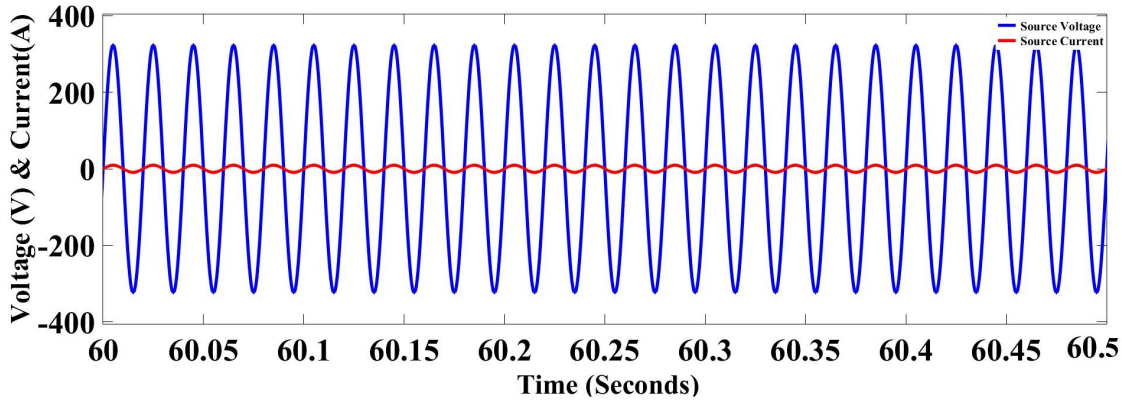


Figure 5.7: In-phase source voltage and source current

Thus, the implementation of Boost PFC Rectifier proves beneficial in eliminating harmonic intereference, improving power factor and producing constant DC link voltage input for the second stage.

5.1.2 BATTERY CHARGING STAGE

The basic objective of the second stage is to supply controlled charge to the battery by employing CC/CV mode of charging algorithm. Two digital isolated PI controllers are employed to regulate charging current and voltage in the two phases of charging. CC mode controller works when constant current charging has to be carried out. Whereas, CV mode controller works when charge has to be provided at constant voltage.

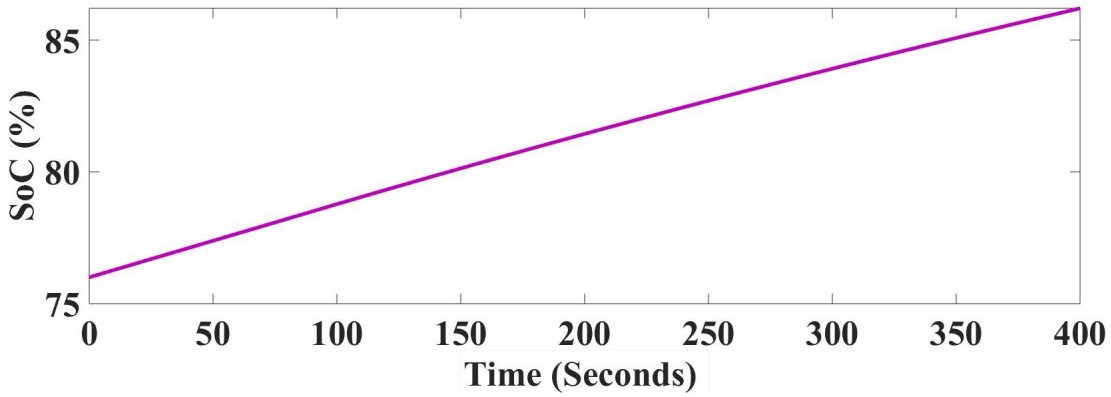


Figure 5.8: State of Charge

Before intiation of battery charging, its SOC is set at 76% as depicted in Fig. 5.8. Taking into consideration Fig. 5.9 and Fig. 5.10, it can be observed that charging of battery occurs at current of 15 A (I'_{ref}) initially for approximately 90 seconds. Here, the current is held constant and the battery is charged under CC mode. Whereas, the voltage rises exponentially during that interval. The charging of the battery occurs at a faster rate when battery is charged at constant current. But, in order to avoid chances of over charging of battery, it is shifted from constant current to constant voltage charging.

Once, the rising battery voltage reaches 134 V (V'_{ref}), the charging of the battery shifts from CC to CV mode. Here, the voltage is held constant at reference value while the current starts dropping. But, charging at constant voltage is a slow process. Hence, it can be observed from Fig. 5.8, that the SoC reaches 86% at 400 seconds. Thus, it is important to include both CC and CV mode charging algorithms in order to curb the drawbacks of individual algorithms.

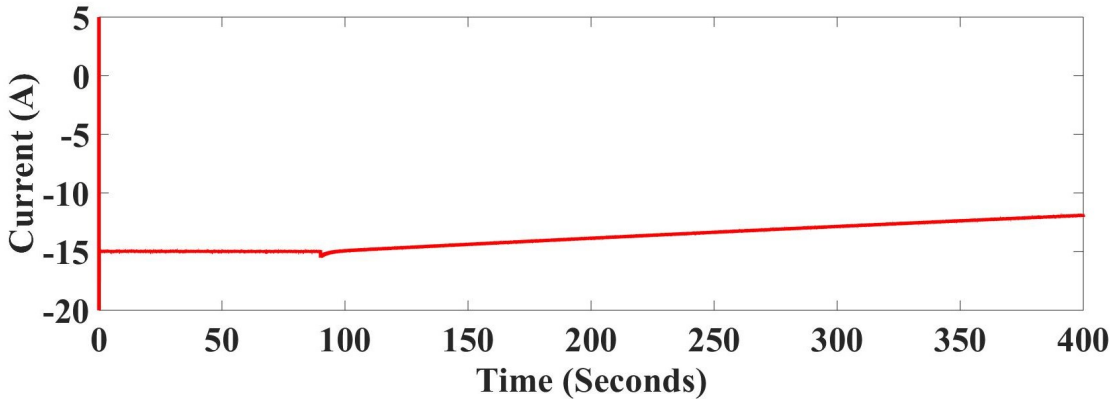


Figure 5.9: Battery Current

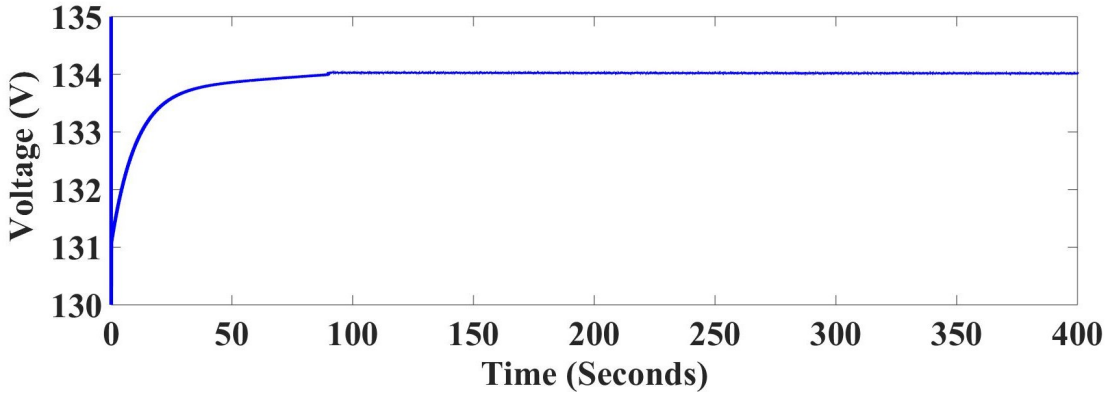


Figure 5.10: Battery Voltage

As mentioned previously, the model works under CC and CV modes. Therefore, THD factor variation is observed when the battery is charged through constant current and constant voltage. Fig. 5.11 and Fig. 5.12 consist of source current signal and FFT analysis of THD factor present in it. Considering the former figure, the source current signal lies in 60 to 61.8 seconds.

Hence, this is the CC mode. It can be observed from FFT analysis of signal that THD factor of 1.31% is achieved. On the other hand, in latter figure, the source current signal lies between 150 to 151.8 seconds. Therefore, this is the CV mode. It can be analysed from the FFT analysis of the signal that there is a minor decrease in THD factor when battery is charged at constant voltage. A decrease of 0.01% was recorded under CV mode of charging. Hence, THD factor of 1.30% was obtained with the proposed charger.

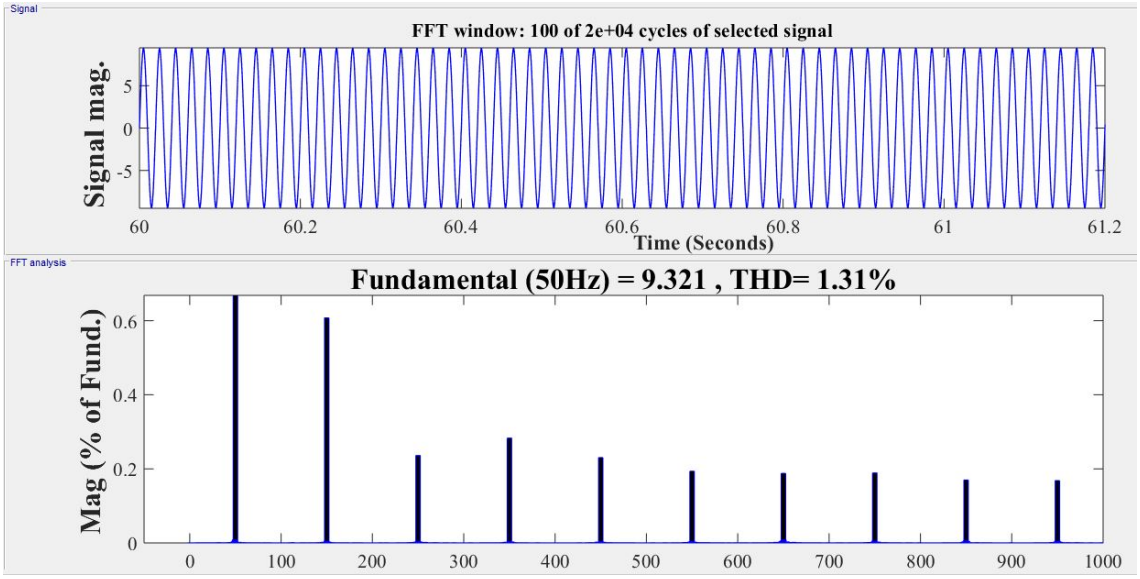


Figure 5.11: THD Factor in CC mode

It can be deduced from the simulated results that reduction of harmonics has led to decrement of THD factor irrespective of battery charging in CC or CV mode. The model is not affected by charging shifting from constant current to constant voltage. It can also be observed that THD reduction occurs at a constant rate throughout functioning of model. Hence, the PFC Rectifier based EV charger satisfies its basic objectives without making the system bulky and complex control strategy.

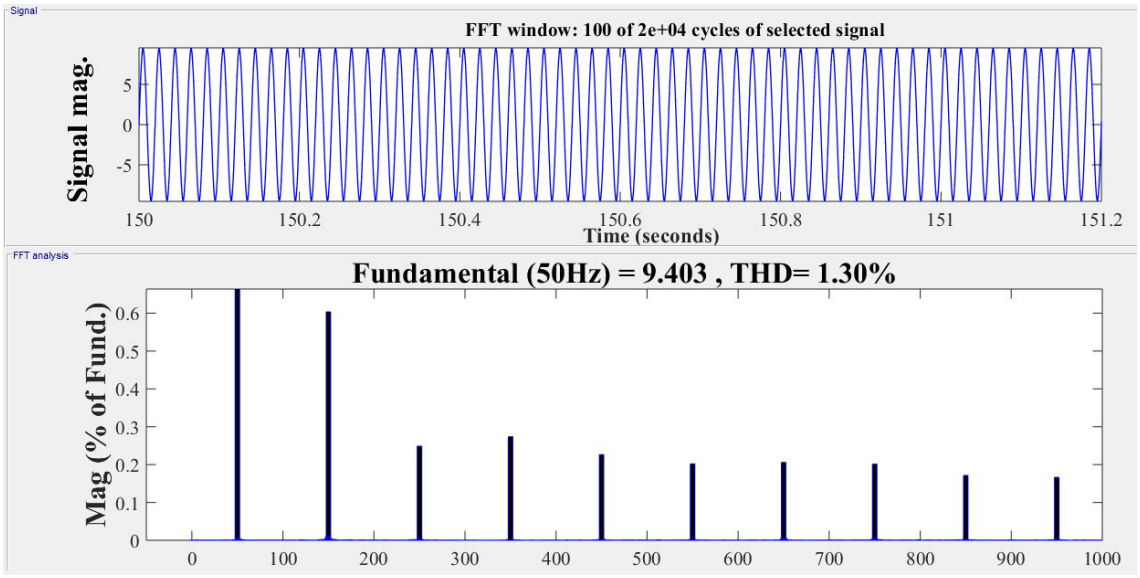


Figure 5.12: THD Factor in CV mode

5.2 HARDWARE-IN-LOOP RESULTS

The real time simulated results are supported by hardware-in-loop verification of EV charger prototype. OPAL - RT behaves as controller for the EV charger prototype, while the respective waveforms are observed on DSO. The laboratory setup of the PFC based EV charger prototype is depicted in Fig. 5.13. In this figure, the two stgaes of battery charging as mentioned in Fig. 2.1 can be evidently identified. AC signal is fed to the bridge rectifier whose output is fed to the boost converter. The voltage received across C_{bst} behaves as input for buck converter which charges the battery. In order to implement CC/CV charging, it is important to sense and hence, control battery's voltage and current. This is prerequisite for controlled battery charging.

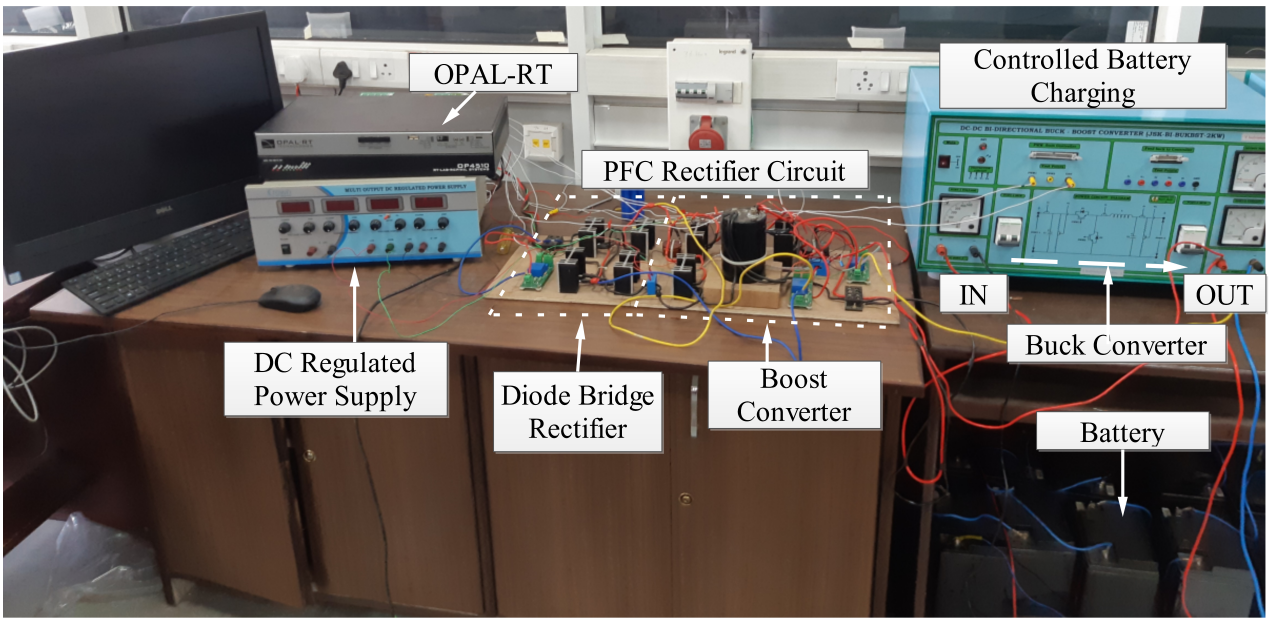


Figure 5.13: Laboratory prototype of proposed PFC based EV Charger

Hence, the Analog inputs such as V_{bat} and I_{bat} are sensed via voltage and current sensors and fed to the OPAL-RT. The model runs into CC or CV mode of charging according to current and voltage level of battery and generates pulses to the switch of buck converter. The digital output port of OPAL-RT is used to feed pulses to switch in CC and CV modes of battery charging.

For the initial PFC rectification stage, the source voltage and source current are observed individually as shown in Fig. 5.15. It can be observed from figure that source voltage is sinusoidal in nature verifying the waveform as observed in Fig. 5.1. The source voltage signal as received under simulation is scaled down by a factor of 10 in order to obtain signal on DSO. It can be observed

from figure that the maximum value of voltage, V_{max} is 15.5 V after multiplying it by scaling factor of 1/10. In addition, its peak to peak value, $V_{\text{Pk-Pk}}$ is obtained as 30.8 V. Also, it can be verified from the figure that source current is sinusoidal in nature with its maximum value C_{max} as 11.6 A. The observed peak to peak value of the signal $C_{\text{Pk-Pk}}$ is 22.5 A.

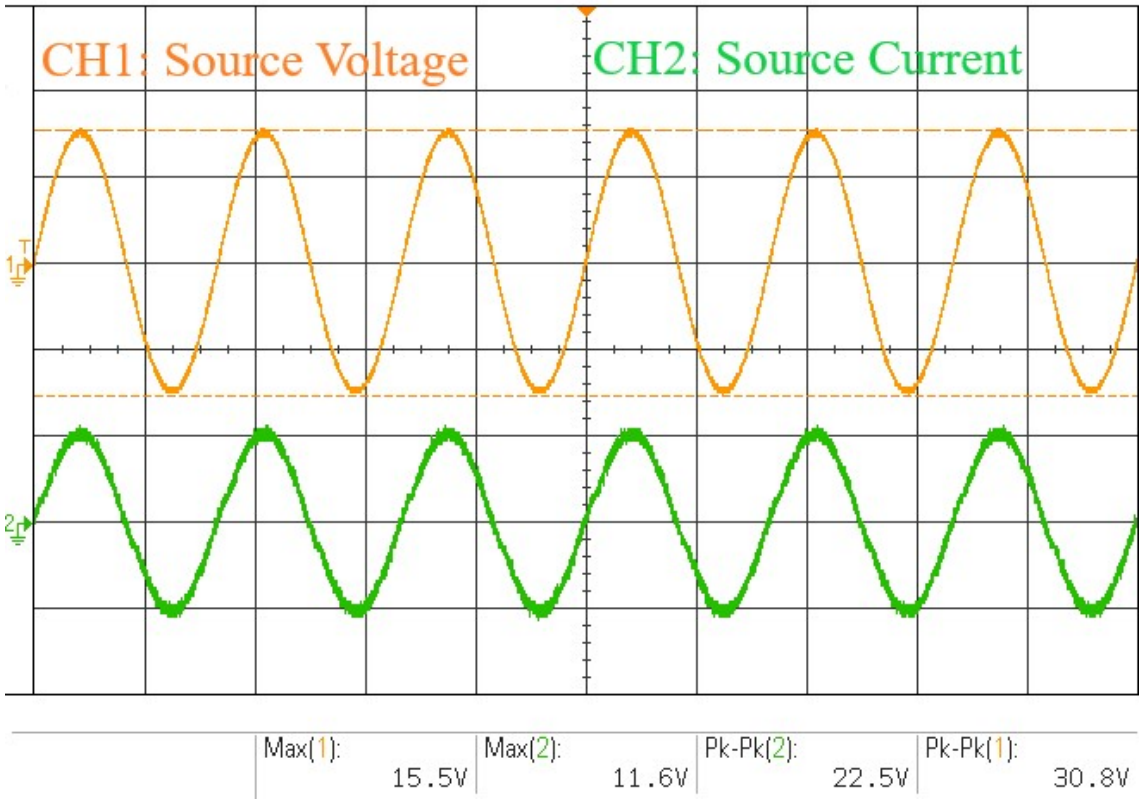


Figure 5.14: Source voltage and source current

The realisation of nearly sinusoidal nature helps in harmonic reduction and hence minimisation of THD factor. Therefore, the Fig. 5.14 shows that voltage and current are in phase with respect to each other as depicted in simulated result of Fig. 5.7. It is in accordance with zero phase angle between voltage and current hence, strengthening the power factor and eliminating chances of wasting useful power.

This is achieved through proper execution of the voltage and current control loop. The voltage control loop will generate a reference voltage signal, whereas, the current control loop will take care of elimination of harmonics by smoothening of source current waveform. Thus, it is evidently visible from figure that proper execution is achieved.

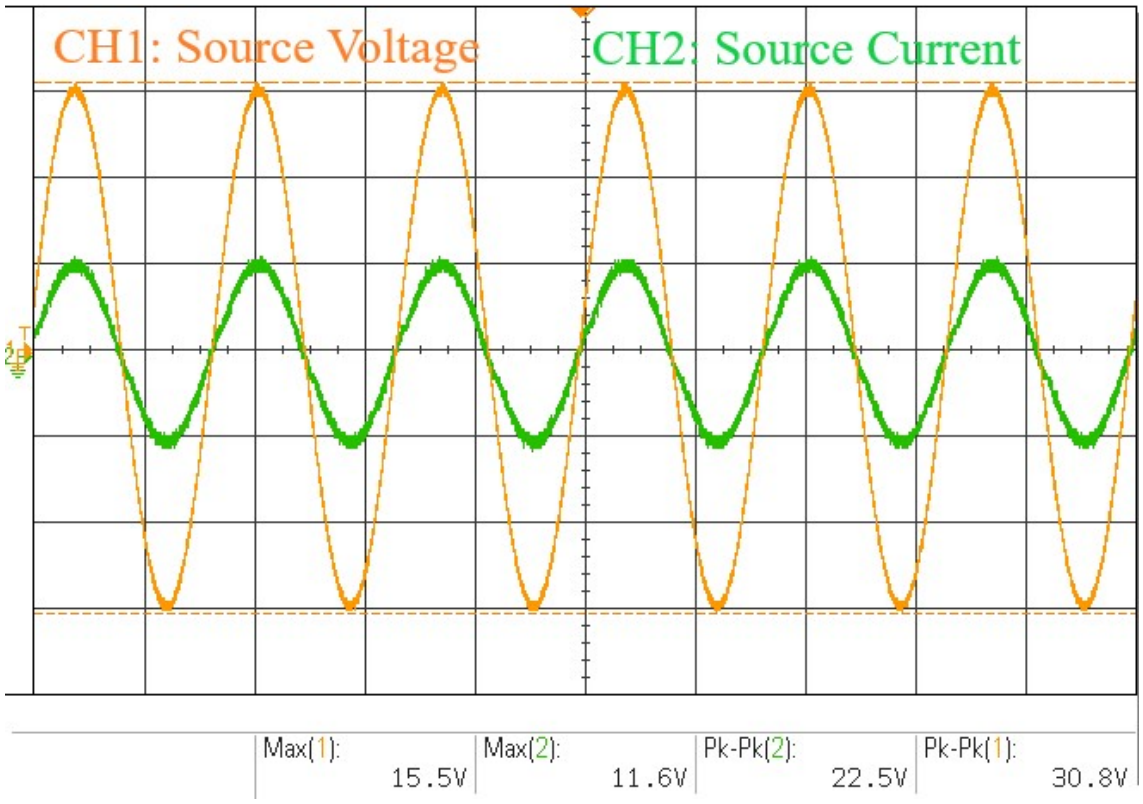


Figure 5.15: In-phase source voltage and source current

Fig. 5.16 indicates rectified input voltage and input inductor current via CH1 and CH2 respectively. This figure shows that current follows rectified voltage achieving a pulsating dc nature. It also exhibits accordance with Fig. 5.2 and Fig. 5.4 of simulation results. This clearly indicates that reduction of THD factor and harmonic interference is achieved through proposed model. It can be observed from the figure that V_{max} is 11.2 V whereas, $V_{\text{Pk-Pk}}$ is 11.3 V. Furthermore, the maximum value of current signal, C_{max} is 11.3 A and its peak to peak value, $C_{\text{Pk-Pk}}$ is recorded at 10.7 A. Here, both the signals are in phase which means that the wastage of power is eliminated by improving the power factor of the system. The resistive load is realised by controlling of current loop. As, the resistive load does not have phase difference between the current and voltage, therefore, the objective was to achieve a resistive load nature. The power factor improved to 0.9998.

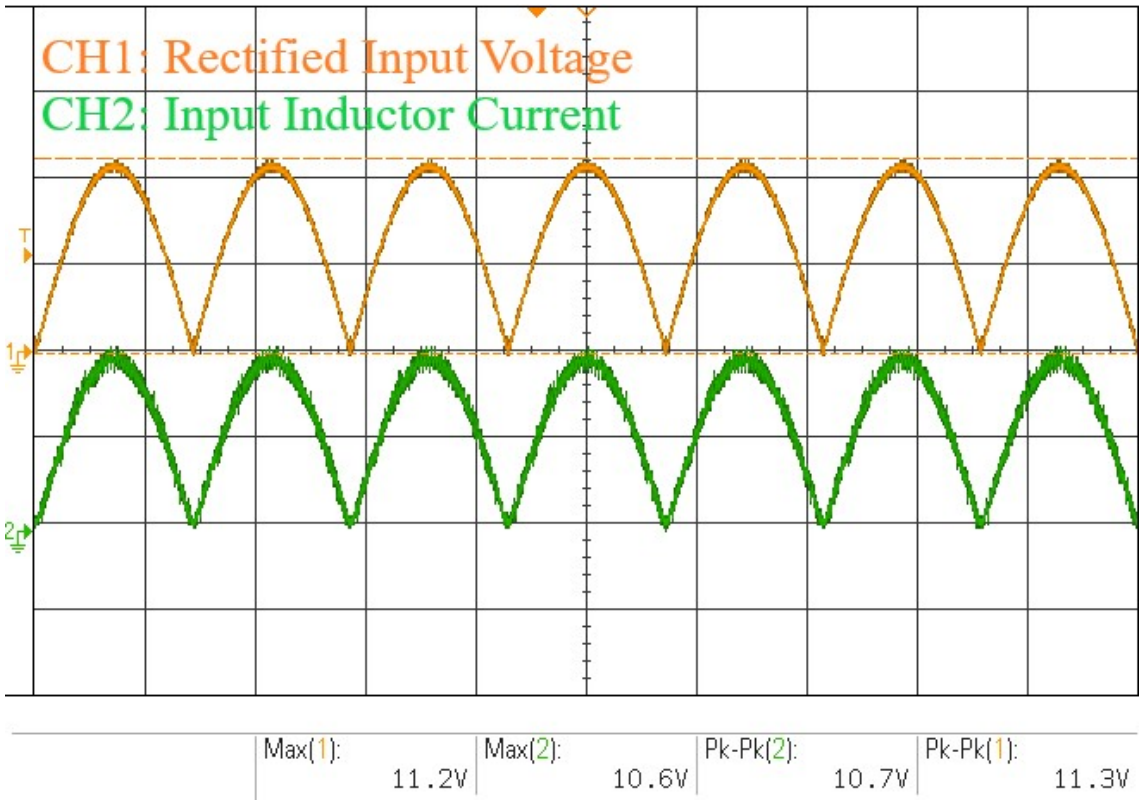


Figure 5.16: Rectified input voltage and input inductor current signals

It also suggests that voltage and current signals are in phase with respect to each other. This is achieved by realising zero phase lag between the signals hence, modelling a resistive load for the prototype. Eventually, it aids in high power factor attainment. The output of the rectifier is recorded and evaluated. The rectified voltage is similar to as observed in simulation results. The need for input inductor current being in phase with the rectified voltage was that it will generate a harmonic free output to the buck converter charger. This will not harm the input circuitry of the EV charger by introducing obnoxious spikes in the source current. The lesser will be the harmonic present in the current waveform, the better will be the output voltage waveform. This will not prove to be dangerous for the charger and vehicle circuit.

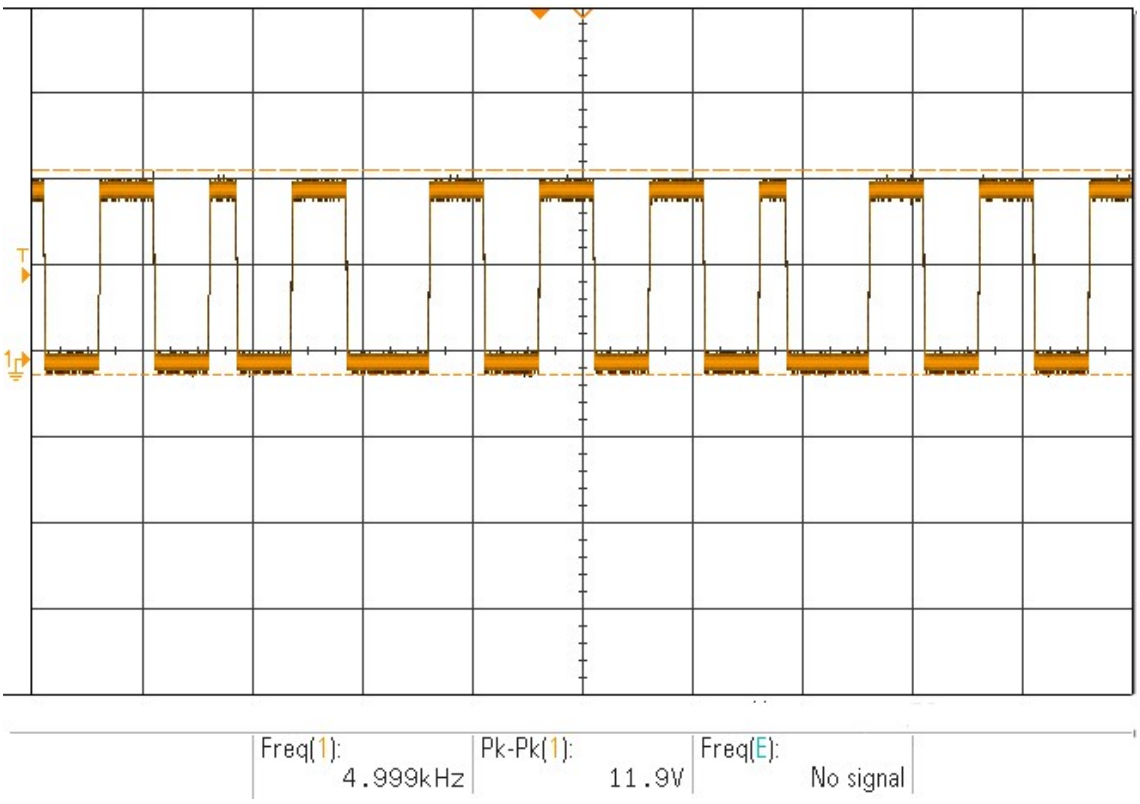


Figure 5.17: Pulses during CC mode

Furthermore, pulses during CC and CV mode of battery charging are observed and are depicted in Fig. 5.17 and Fig. 5.18 respectively. The pulses are observed before 100 seconds when the battery is charged under constant current. However, the pulses are recorded after 100 seconds when the battery is charged at constant voltage. It can be seen that similar kind of pulses are observed during CC and CV mode. Moreover, the frequency at which buck converter's switch operates is constant in nature. Switching frequency of 4.999 kHz is recorded while shifting from CC to CV mode. Thus, it can be deduced from various simulation and HIL results that efficiency of the model is recorded as 96.8% with power factor of 0.9998 and THD factor of 1.31% under CC mode and 1.30% in CV mode of battery charging.

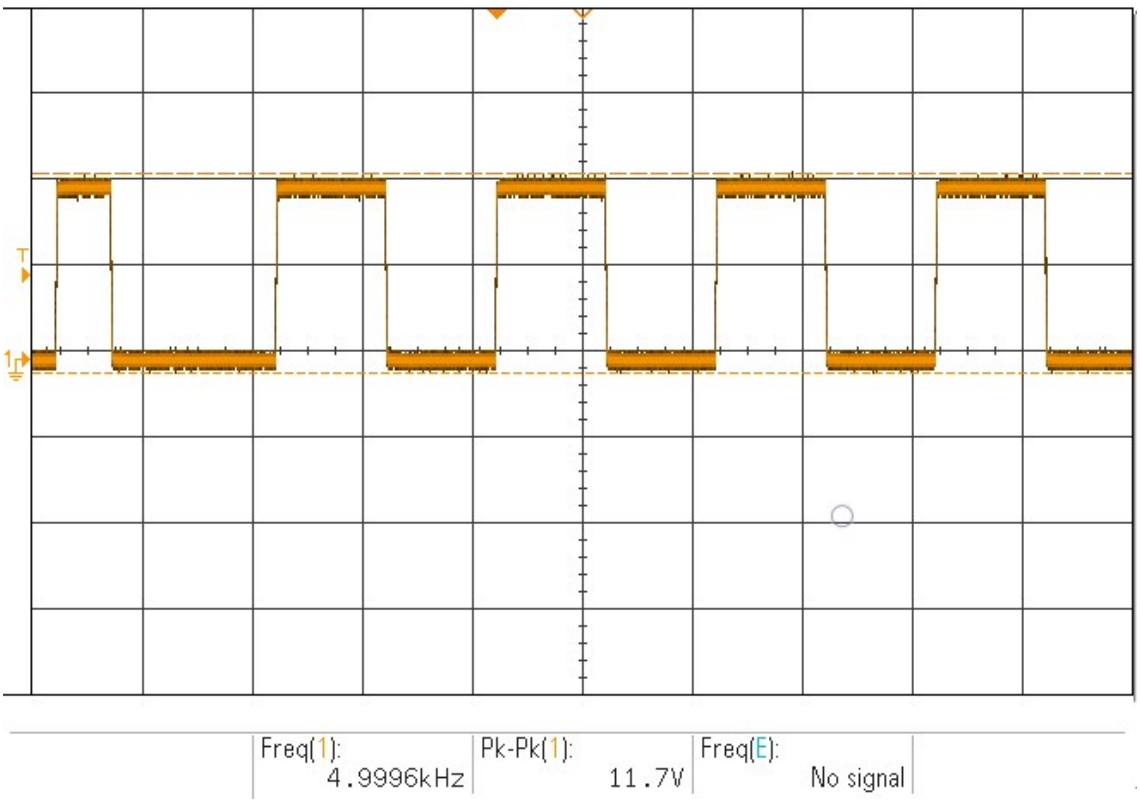


Figure 5.18: Pulses during CV mode

These pulses are observed during when the battery is charged during the constant voltage mode of charging algorithm. Here, the charging duirng CV mode starts when the model achieves 100 seconds. Hence, these pulses are recorded after 100 seconds of charging of battery. As, the pulses are similar in nature, smooth shifting from CC to CV mode is observed at a constant frequency of PWM generation. Though the pulses may not be of equal size but, they are generated at constant frequency. However, this may tend towards that the charging is not a constant procedure. The charging of battery and operation of switch is is controlled by these pulses. The turn on and off of switch is pulse dependent hence, battery may not be charging at the same rate under different mode of charging algorithm. Thus, during CC mode the charging is fast process, whereas, in CV mode charging is a long process and time consuming in nature.

Thus, the simulation and hardware-in-loop results are similar to each other verifying each other nature and waveforms. The hardware results are scaled down by factor and are observed on DSO, whereas, simulation is done under real time simulation.

Chapter 6

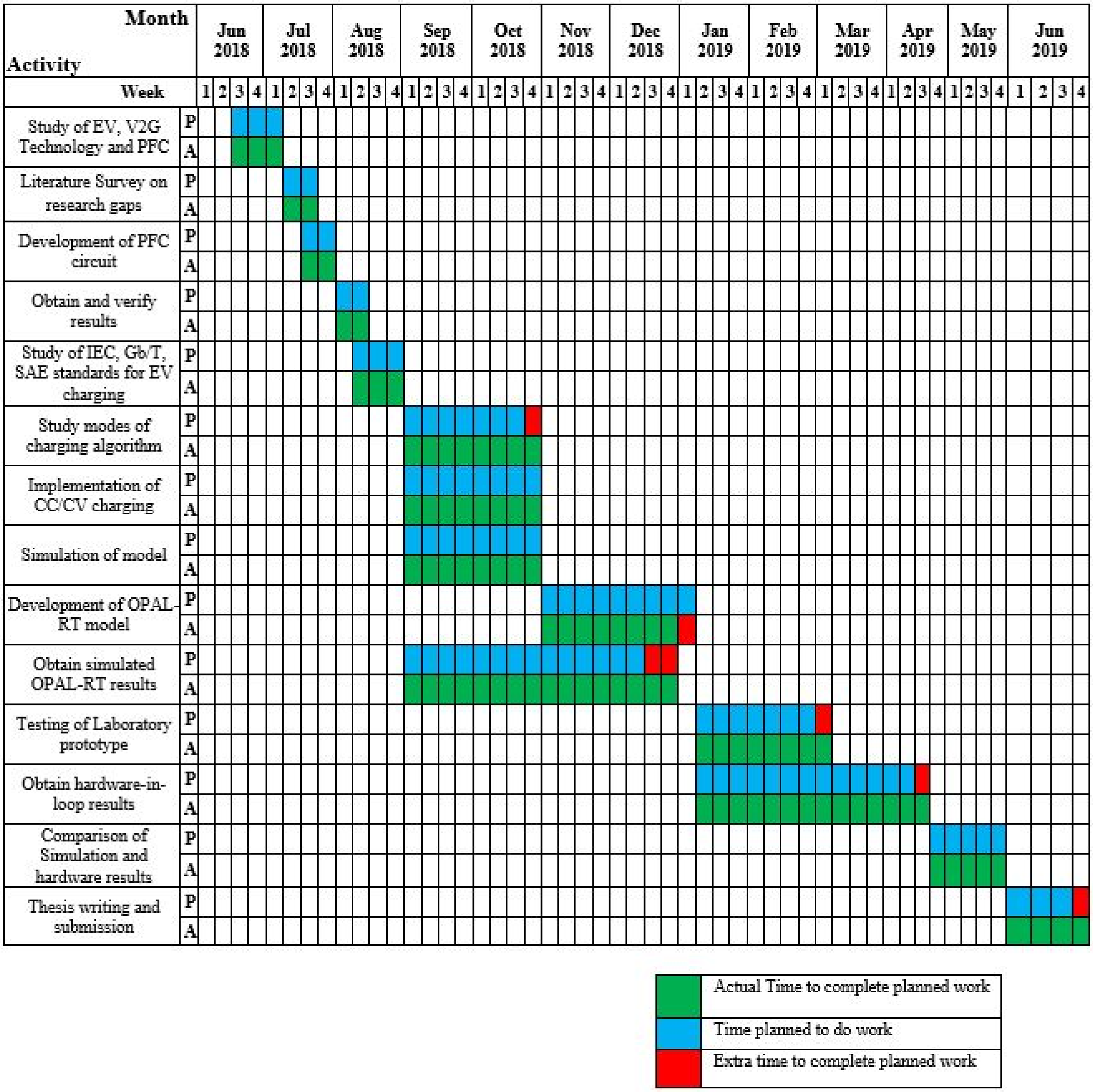
CONCLUSION AND FUTURE SCOPE

A 2 kWh EV charger is proposed in this paper. It employs a PFC rectifier and implements CC/CV mode of charging. The boost PFC rectifier improves power factor at the grid side and removes input current harmonics. Moreover, the outer voltage and inner current control loop ensures a constant DC link voltage at the bus capacitor and sinusoidal input inductor current. This helps in achieving good power quality. This regulation is achieved by PI controllers. The second stage comprises of Controlled Battery charging that charges the battery using CC/CV algorithm implemented through PI controllers. The effectiveness of the proposed design has been validated by OPAL-RT with HIL. The charger achieves input power factor of 0.9998, THD equal to 1.30% and 96.8% efficiency. Moreover, in comparison with similar designs, the proposed scheme accomplishes higher harmonic reduction and power factor while keeping the circuit compact, easy control strategy and efficient.

6.1 FUTURE SCOPE

Furthermore, there can be improvements made in the controlled battery charging stage where a smooth transition can be obtained and fast charging of the battery can be included. There are various different methods that can further reduce the losses and charge the battery at a faster rate. This can be done by keeping in view, excess charging of battery and fast charging of battery.

6.2 WORK PLAN


Month
Activity
Jun 2018
Jul 2018
Aug 2018
Sep 2018
Oct 2018
Nov 2018
Dec 2018
Jan 2019
Feb 2019
Mar 2019
Apr 2019
May 2019
Jun 2019
Week
Study of EV, V2G Technology and PFC
Literature Survey on research gaps
Development of PFC circuit
Obtain and verify results
Study of IEC, Gb/T, SAE standards for EV charging
Study modes of charging algorithm
Implementation of CC/CV charging
Simulation of model
Development of OPAL-RT model
Obtain simulated OPAL-RT results
Testing of Laboratory prototype
Obtain hardware-in-loop results
Comparison of Simulation and hardware results
Thesis writing and submission
Actual Time to complete planned work
Time planned to do work
Extra time to complete planned work

Chapter 7

ACHIEVEMENTS/PUBLICATIONS

1. Research paper entitled as "**A PFC Rectifier based EV Charger for Harmonic Reduction**", has been presented in International Federation of Automatic Control (IFAC) workshop on Control of Smart Grid and Renewable Energy Systems (CGRES) held in Jeju, South Korea on 10-12th June, 2019 and to be published in Science Direct (under proceeding).

2. Delivered a guest lecture on "**Overview of Electric Vehicle Charging Infrastructure**" at National Institute of Technical Teachers Training and Research (NITTTR), Chandigarh on 10th Jan, 2019.

3. Research paper entitled as " **Real Time Simulation of a PFC Rectifier Based EV Charger Employing CC/CV Mode of Charging**" has been submitted for publication in IEEE Transactions of Transportation Electrification.

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