Design & Development of BLDC Motor Controller

A Dissertation submitted in the partial fulfillment for

the requirement of the Degree of

MASTER OF ENGINEERING

in

Power Systems

Submitted by

Hemant Kumar
801742012

Under the Guidance of
Dr. Santosh Sonar
Assistant Professor, EIED

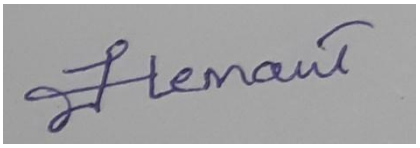
THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

2019

Electrical and Instrumentation Engineering Department
Thapar Institute of Engineering & Technology, Patiala
(Declared as Deemed-to-be-University u/s 3 of the UGC Act., 1956)
Post Bag No. 32, Patiala – 147004
Punjab (India)

DECLARATION

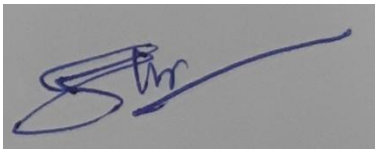
I hereby certify that the work which is presented in dissertation entitled, "**Design & Development of BLDC Motor Controller**", in partial fulfillment of the requirements for the award of the degree of Master of Engineering in Power Systems, submitted to Electrical & Instrumentation Engineering Department of Thapar Institute of Engineering & Technology (Deemed to be University) is an authentic record of my own work carried under the supervision of **Dr. Santosh Sonar**. It refers others researcher's work which are duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part or in full to any other degree to any other university or institute except as reported in text and references.



Place: PATIALA **HEMANT KUMAR**

Date: 07-08-2019 **801742012**

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.



Date: 07-08-2019 **Dr. Santosh Sonar**

Assistant Professor

Department of Electrical & Instrumentation Engineering

Thapar Institute of Engineering & Technology, Patiala

ACKNOWLEDGEMENT

Words are often less to express one's deep regards. With an understanding that work like this can never be the outcome of a single person. I take this opportunity to express my profound sense of gratitude and respect to all those who helped me throughout the duration of this work.

I express my deep sense of gratitude towards **Dr. R.S. Kaler**, Head of the Department of Electrical & Instrumentation Engineering, Thapar Institute of Engineering and Technology, Patiala who has been a constant source of inspiration for me throughout this work.

I would like to express my gratitude and thanks to supervisor, **Dr. Santosh Sonar**, Assistant Professor, Department of Electrical and Instrumentation Engineering, Thapar Institute of Engineering and Technology, Patiala and **Mr. Arunendra Kumar** Proprietor, **Alasa Electronics** for the patient guidance and support through this work. It is indeed an honor and privilege to work under them as a student.

I am also thankful to my batch mate and project partner **Jahangeer Ahmad Dar** who devoted his valuable time with me for the successful completion of this report. I extend my gratitude to my B.Tech Final Year Electrical Engineering friends **Vikramjit Singh** and **Sultan Singh** for their valuable inputs during technical report writing and making presentation. I found their guidance to be extremely valuable.

Lastly, I would like to thank my parents and brother for their years of unyielding love and encouragement.

Hemant Kumar

(801742012)

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF FIGURES

LIST OF FIGURES (Continued)

LIST OF TABLES

LIST OF ABBREVIATIONS

ACRONYMS	FULL FORM
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated-Gate Bipolar Transistor
THD	Total Harmonic Distortion
AC	Alternating Current
DC	Direct Current
PFC	Power Factor Correction
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
RMS	Root Mean Square
CM	Common Mode
PI	Proportional Integral
BLDC	Brush Less Direct Current
PM	Permanent Magnet
EMI	Electromagnetic Interference
PF	Power Factor
HF	High Frequency
BL	Bridgeless
VSI	Voltage Source Inverter

ABSTRACT

Electrical machines are used in commercial and industrial applications since last many decades. The fast-dynamic response and high-performance control of electrical machines can be driven by motor drives due to rapid advances in the semiconductor area, such as microcontrollers and power switching devices such as MOSFETs, IGBTs, *etc*. The stepper motor leads in particular to the permanent synchronous magnet motor and the brushless DC motor (BLDC), which have various advantages like elevated efficiency, little size, reduced rotor losses etc. This thesis work is introducing the design and development of the BLDC motor controller. The three-phase voltage inverters supply the BLDC motor which operates by simultaneously activating two of its three-phase windings, which in turn makes best use of the windings to develop an increasing value of torque. The excitation of the stator windings is closely related rotor position. Hall sensors are used to indicate the position of the rotor. Depending on the rotor position, the switching devices present in the inverter are switched after every 60° interval. The inverter supplies the desired voltage & frequency output by controlling the on and off times using the most appropriate PWM technique. Currently, there are several PWM techniques present, including the sinusoidal and space vector based PWM methods that are mainly used today, and interestingly the SVPWM based inverter improves the use of DC bus voltage, reduces switching losses and offers better harmonic performance then the other PWM techniques. The SV-PWM technique and the BLDC motor speed control are simulated using the PSIM software.

Keywords: - SVPWM, Brushless DC Motor (BLDCM), PSIM, MOSFETs, IGBTs

CHAPTER 1

INTRODUCTION

In electromechanical energy conversion, the electric machine acts as an energy conversion bridge between the mechanical and electrical systems as represented in Fig. 1.1. Electrical machine can work as an either generator or a motor. For any electrical motor, the voltage and the current behave as representative of the incoming electrical energy and the output is the mechanical energy transferred to a mechanical load, which is portrayed by the speed and the torque.

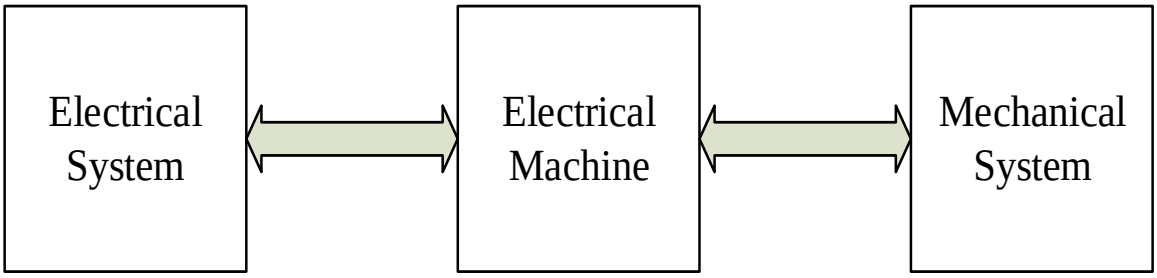


Fig. 1.1 Energy Conversion Process

A simple and clear block diagram of an electric unit shown in Fig. 1.2. It consists mainly of power supply, converter, machine (motor), detection module and control module. Energy can be provided from either an AC power source or a DC source battery. The engine has the desired characteristics demanded by the load and with its ability to share energy from the source to the load. The most frequently used electric machines are DC motors, BLDC motors, stepper motors and switched reluctance motors.

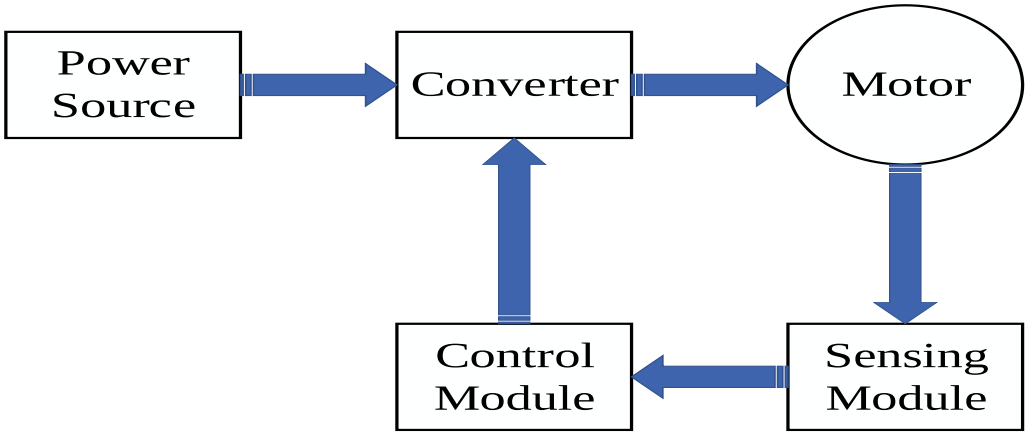


Fig. 1.2Block Diagram of an Electrical Drive

The converters are used to convert the electrical energy from the input source into desirable form for the machine. Relying on the energy demanded by the input power supply and the motors, by the AC to DC converters, by the DC to DC converters (upper or lower converters), the inverters and the cycle converters are commonly used in the design of electric drives. The detection module is assigned to sense the rotor position, speed and motor terminal voltages. It is necessary for the requested manipulated closed-loop operation. The control module is the central component of the entire drive unit.

In last one decade, due to the rapid development in the area of power electronics and semiconductor tools, the adaptable speed unit, like the BLDC motor units, has been well progressed and extensively used for various applications. The utilization of the BLDC motor BLDCM for low-power devices is on the rise due to its elevated efficiency, broad speed range and very little maintenance. Switching to a Permanent Magnet BLDC Motor (brushless DC motor with permanent magnets) is performed by solid-state switches of a three-phase supply voltage inverter (VSI) [1].

A classical block diagram of the brushless DC motor (BLDC) including the power factor correction circuit is shown in Fig. 1.3.

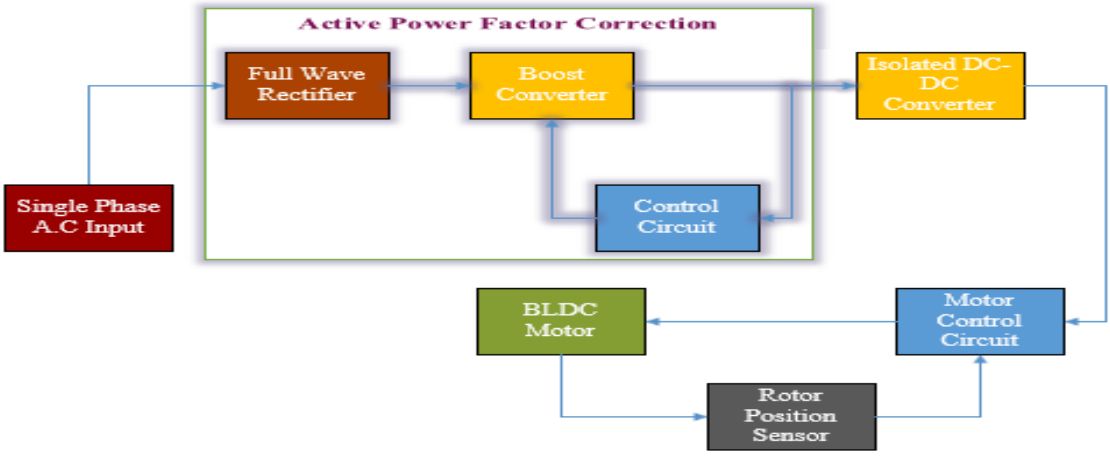


Fig.1.3Block Diagram Representation of PFC based Isolated Converter fed BLDC Motor Drive

CHAPTER 2

LITERATURE SURVEY

2.1 POWER FACTOR CORRECTION

2.1.1 INTRODUCTION

In the terminology of power engineering, the power factor is interpreted as the ratio between the actual power engrossed by the load and the apparent power fluently flowing into the circuit. It is a dimensionless quantity, represented as

$$\cos\theta = \frac{\textbf{Real power (Watt)}}{\textbf{Apparent Power(VA)}} \quad \textbf{(2.1)}$$

Energy processors generally consist of some phases of energy conversion in which the operation of these phases is instantaneously decoupled by employing energy storage elements like as inductors or capacitors or both. Hence, the immediate input power is unequal when compared with immediate output power. Therefore, a converter is considered as a fundamental module of electronic power supply arrangement. It uses semiconductor devices supervised by electronic circuitry and possible energy storage elements, like inductors and capacitors. All devices receive current pulses from the AC grid and most power supplies are supplied with an input rectifier bridge and a filter capacitor. The value of current in the output has fundamental as well as odd harmonics [2]. The harmonic content is undesirable thereby creating problems for the energy system. For the deterioration of the power factor, the current present in the distribution element becomes even higher. In the absence of power correction circuits, the capacitive filter extracts the pulsed current from the AC grid, causing a drop-in power quality and the high harmonic content which creates an unacceptable effect for other users powered by the same line [3].

The harmonic content present in the alternating current must be eliminated to meet international energy quality standards. In 1982, the International Electrotechnical Committee (IEC) presented its IEC 555-2 standard which was later embraced in 1987 by the European Committee for Electrotechnical Standardization (CENELEC) as a European standard EN 60555-2. The IEC 555-2 was later renamed IEC 1000-3-2 in the year 1995.

A power factor correction circuit is required to configure the input current as a function of half the rectified sinusoidal voltage detected at the rectifier bridge output. The circuit increases the real power absorbed by the electric network and therefore reduces the harmonic voltage caused by the current harmonics in the system. The various disadvantages of the power factor are the following

• High harmonic input current

• Low efficiency of the rectifier due to the high RMS current value

• Distortion in the AC input voltage due to the maximum currents

Another reason to use the PFC circuit is to comply with international standards, such as IEC 61000-3-2 [4].

2.1.2 POWER FACTOR CORRECTION STRATEGIES

2.1.2.1 Passive Power Factor Correction (PFC)

This technique is utilized for small power supplies of around 100 W or less. A productive passive filter abolishes harmonics in the current and revamp the caliber of the energy and the power factor.

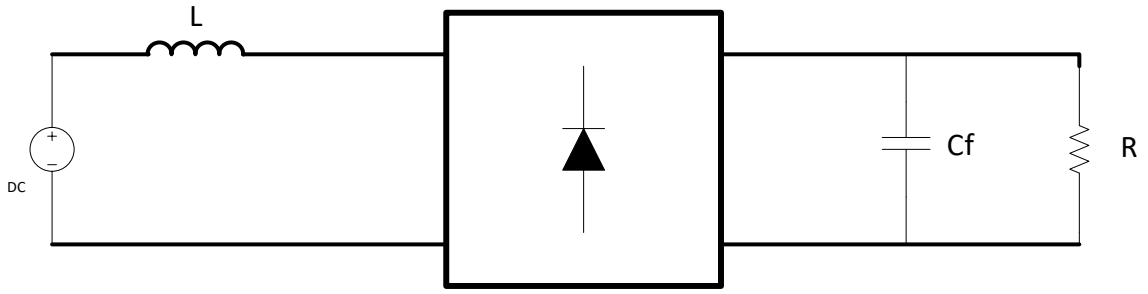


Fig.2.1 – Passive Power Factor Correction (PFC)

Passive PFCs, as shown in Fig. 2.1, are straightforward, strong and reliable for low power applications. Furthermore, they do not initiate any sort of EMI in the system. But they are large and hefty due to the size of the inductor.

ADVANTAGES

- Simple Construction
- Reliability
- Well organized
- Inexpensive

DISADVANTAGES

- Hefty and large size
- Poor dynamic response
- Input current shape depends upon load
- No voltage regulation below 200 W limits the use of passive power factor correction technique

2.1.2.2 Active Power Factor Correction (PFC)

This method is preferred for energy sources above 100W. This technique uses different types of filters to greatly reduce the power factor. If the inductor of large value is selected then it reserves a large amount of energy that keeps the rectifier for the entire half cycle. Consequently, it curtails the harmonic distortion caused due to the intermittent conduction of the rectifiers. This method furnishes a more well organized, lighter and very small voluminous correction.

This method has variety of active filters including the hybrids and PFC circuits such as boost, buck and fly back converters. An active filter improves the energy quality by eliminating the current harmonics [3]. Non-linear load current and voltage waveforms can be identified so that the input supply current can be easily adjusted. Active filters are normally adapted in high-power applications including the three-phase power systems due to their expensive nature and a intricate control circuit. The circuit involved in this technique is used betwixt the line and the non-linear load which can provide a settled output voltage output and an elevated-power factor on the input side. This intelligent function of the PFC circuit makes it furthermore striking and an option for energy sources of various energy conversions or in dissimilar energy sources of the devices. Therefore, different types of control and topological processes have been evolved and assessed to improve energy quality and improve the power factor. The PFC reinforcement topology was used to ameliorate power quality and abetter control method was designed to minimize the power factor to a lower level and even total harmonic distortion.

2.1.2.2.1 Buck Converter based Active PFC

This converter works when the instantaneous input is greater than the value of output voltage, as shown in Fig. 2.2. The circuit operates in discontinuous driving mode [5].

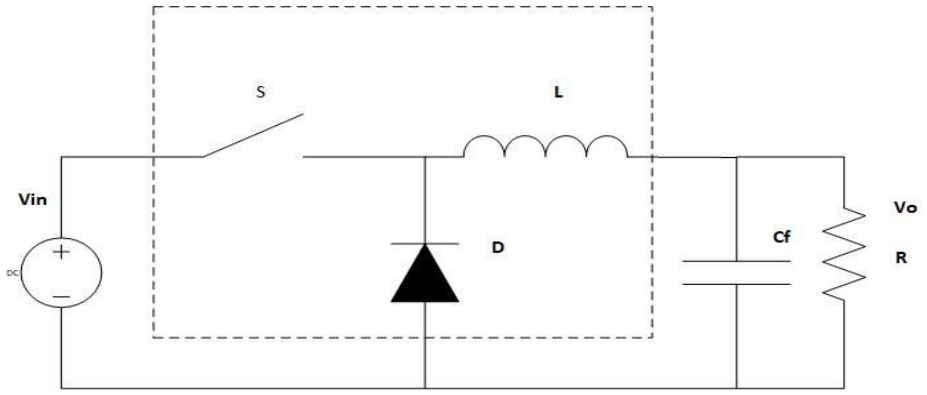


Fig.2.2 – Buck Converter

ADVANTAGES

• There is robustness and reliability due to the decrease in voltage

• Due to the low voltage at the PFC converter output, there is a low noise of CM

• In Buck PFC it is not necessary to limit the initial start-up current, since it has an initial start limitation intrinsic

• There is a flexibility of control that helps to get THD and PF coupons

LIMITATIONS

• THD and PF performance is limited because the AC line crosses the current distortion

• Overvoltage management is complicated as there is no direct path from the AC inlet to the ground receptacle storage capacitor

• Due to the small output voltage, it is a less efficient bulk storage capacitor

• Less waiting times

• The ripple voltage percentage of the bus in the buck type is more than an increase in the PFC

2.1.2.2.2 Boost Converter based Active PFC

Often, for the PFC circuit a boost converter is selected due to its filtered input current, high efficiency and high-power factor capacity, as shown in Fig. 2.3. This approach can produce elevated efficiency and quite significantly improved power factor, but it is not susceptible to converter miniaturization in low, low or medium power DC applications, because

1) It is difficult to significantly reduce the volume of the auxiliary circuit (for example, through high frequency operation) due to loss restrictions, high inductance (*e.g.* High impedance characteristic) and high value of parasitic capacitance(for example, large switching output capacity) [6].

2) The DC-DC converter operates at elevated voltage and has a high conversion rate of the reduction voltage, so it is still tough to design it at high frequency with a small volume

3) The capacity of the capacitor which is buffer in energy is large.

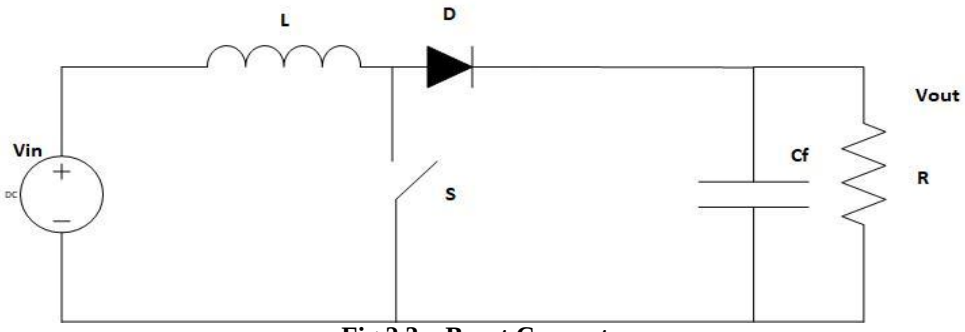


Fig.2.3 – Boost Converter

ADVANTAGES

• Low THD (total harmonic distortion) and the best possible power factor

• Due to the high output voltage, the size of the storage capacitor is efficient

• Respect in terms of waiting time

• The booster switch is easy to use and current detection is simple

• Thanks to the direct path between the input and the output capacitor, it provides excellent surge management

LIMITATIONS

• The output voltage should always be greater than the instantaneous peak value of input voltage

• Requires an isolation stage to minimize the voltage

• Due to the increased bus voltage, common mode noise is more

2.2FLY BACKCONVERTER

2.2.1Introduction

These days, thanks to its coherence, low number of components and minimum cost, the Fly-back converter is greatly used [7-8]. But, the voltage at the switch is soaring for this circuit topology and it increases more and more as the work cycle becomes nearer to the unit. Consequently, it is a challenge for conventional flight return, as shown in Fig. 2.4, to operate with a high duty cycle value, with advantages in the reduced voltage in the output rectifier and a magnetization inductance reduced current values and polarization of the bias current. Moreover, the dispersion energy of the transformer generates a maximum voltage through the MOSFET, whose magnitude could be the root of its collapse [9-11]. The more soaring the energy in the output, the more energy is deposited in the leakage inductance, which limits the high value of power of the converter. Furthermore, the MOSFET present in the Fly-back converter is modified by force. Eventually, in the condition of CCM operation (CC mode), a reduced smaller limit is given to the magnetization inductance [12]. All the above problems greatly restrict the regulation of the converter, which is why it is acceptable for very low power applications. The main features of the return converters are:

• The design of the high frequency transformer (coupled inductor) is simple for low power applications.

• Low cost due to the low number of components.

• The blocking voltage does not occur in the output diode, so the cost of the diode is reduced.

• There is no additional inductor in the output circuit. This simplifies the use of multiple outputs.

• The transient response is rapid due to the absence of the output inductor

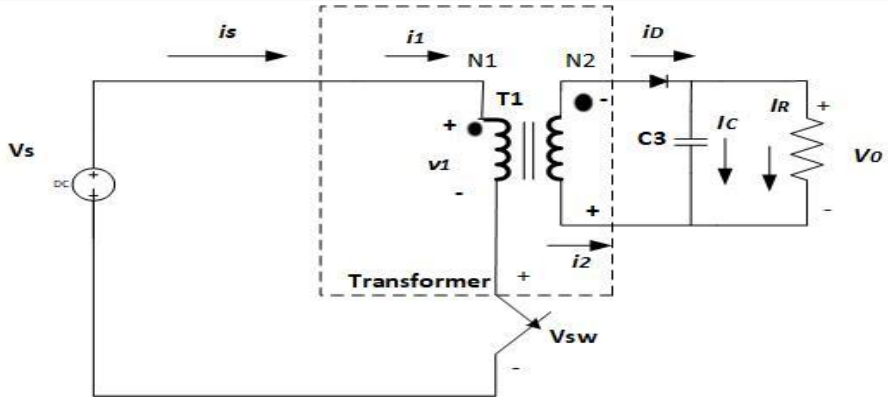


Fig. 2.4 – Fly Back Converter

Fly-back converters (applications)

• Cell Phone/Laptop Charger

• High Voltage Source for CRTs

• Photocopy machines, lasers

• Isolated Driver Circuits

2.2.2 Basics of Fly Back Converter

The Fly back converter basically operates in two periods: -

1) **Switch ON Period**

During the activation period, the primary winding is powered by a voltage that provides a primary current to produce the magnetic flux. The magnetic flux in the transformer core increases to store energy in the transformer as shown in Fig. 2.5. The output voltage on the secondary side is negative, which causes the diode to have reverse bias and there is no voltage present on the output side.

Time Interval 0≤t≥T i.e. MOSFET is ON

$$V_1 = V_S \tag{2.2}$$

$$V_2 = \frac{N_2}{N_1} V_1 = aVs \tag{2.3}$$

During this period, the secondary side is open and takes only the magnetizing current without increasing load from I_{min} to I_{max} to store the energy in the transformer.

2) **Switch OFF Period**

During the OFF period, the primary current and the magnetic flux decrease, resulting in a positive secondary voltage. The output diode is in forward biased position and the current flow to be charged is as shown in Fig. 2.6

Time Interval $T_{ON} \leq t \leq T$ i.e. MOSFET is OFF

The output of the fly back converter during off time is

$$V_0 = \frac{N_2}{N_1} \frac{D}{D-1} V_S \tag{2.4}$$

Where duty cycle of the switch is represented by D

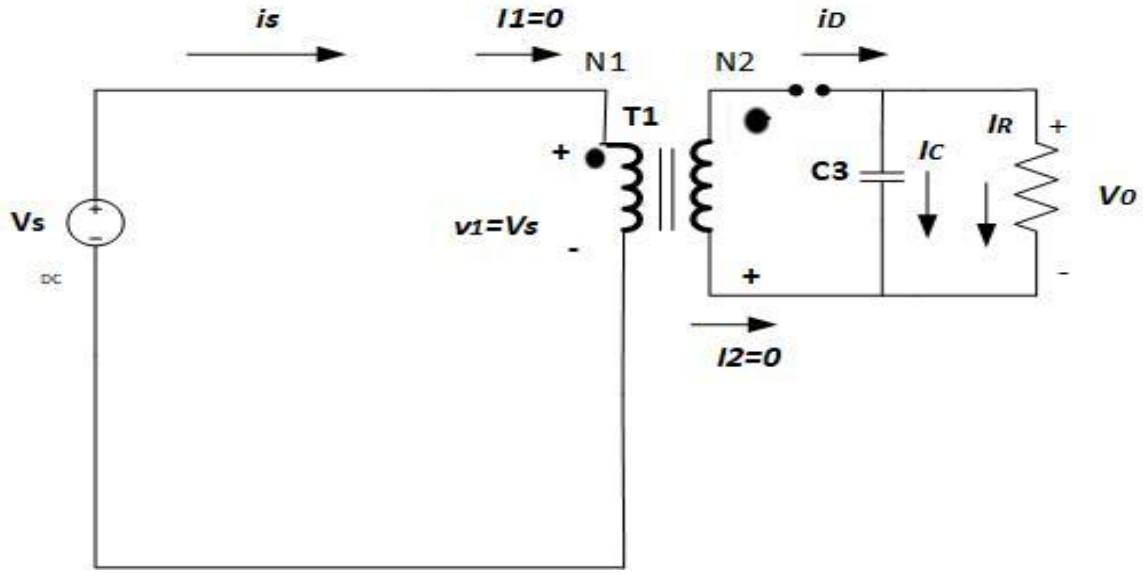


Fig. 2.5 – ON state equivalent circuit of Fly Back Converter

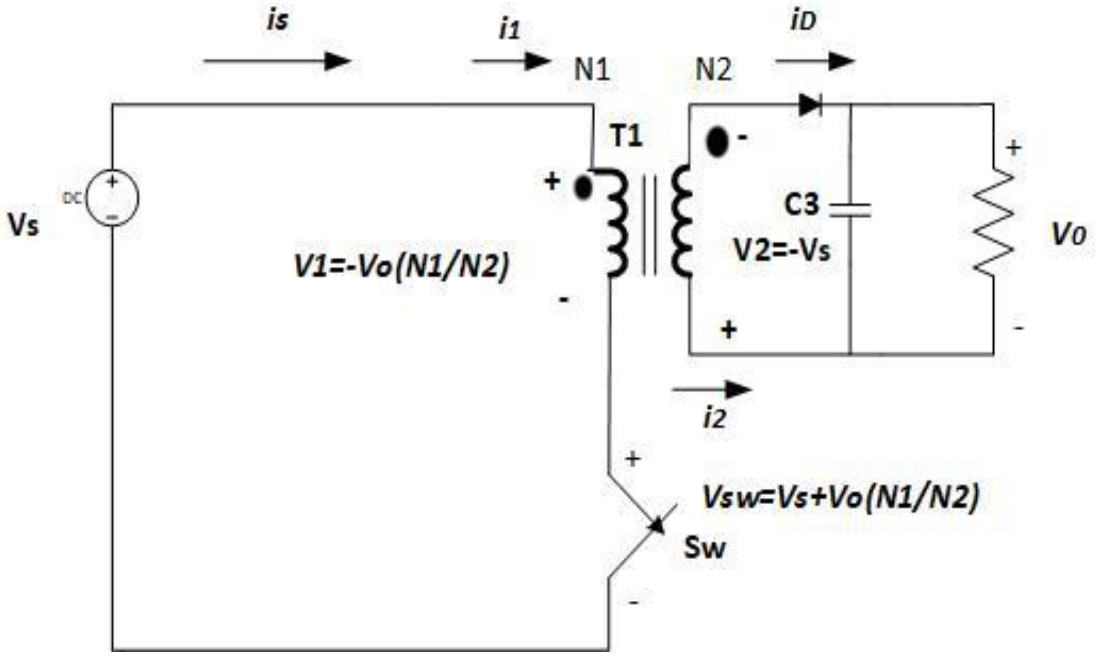


Fig. 2.6 – OFF state equivalent circuit of Fly Back Converter

2.3 BRUSHLESS DC MOTOR

The applications of the brushless DC motor (BLDCM) in low-power devices are on the rise owing to its elevated efficiency, broad speed range and very minimum maintenance. It is a powerful three-phase synchronous motor ascribing to the use of PM in the rotor coil. The activation of a PMBLDCM is performed by solid-state semiconductor switches of a three-phase supply voltage inverter (VSI).

[13] proposed a Cuk DC-DC converter in the form of a single-stage power factor correction converter for a brushless DC motor (BLDCM) powered by a diode rectifier bridge from a single-phase AC network. A three-phase VSI was used for electronic switching to utilize the BLDCM which drives an air conditioning compressor.

The compressor speed is manipulated to obtain an optimal air conditioning using the idea of manipulating the voltage in the intermediate circuit in proportion to the desirable speed of the BLDCM. The stator currents present in the BLDCM throughout the step change in the reference speed are manipulated within the identified limits by the inclusion of a speed limiter in the reference voltage of the intermediate circuit. The proposed voltage-controlled converter, a Cuk DC-DC converter is used as a PFC converter thanks to its continuous input and output currents, its small output filter and its wide range of output voltages with respect to other converters. Furthermore, in addition to improving the PQ in the AC network, it controls the voltage in the intermediate circuit for the desired speed, if necessary.

It can also be used on BLDC motor fans on trains introduced not a long time ago on the railways network. These BLDC motor fans have indistinguishable PQ problems, since they use a single-phase diode rectifier and do not have speed control. These fans also have current problems. All these PQ problems of the bad power factor, inrush current and speed control in these fans in India's railroad trains can be mitigated by the PFC-based BLDCM with the proposed voltage control.

[14] presented a brushless DC motor driven by a Cuk bridgeless converter (BLDC) for an air conditioning system. A unique approach is proposed to control the speed of the BLDC motor by controlling the voltage on the DC bus using a single voltage sensor. A BLDC motor electronic switch was used using a fundamental VSI frequency switching, which reduces the associated losses and switching speed. The proposed inverter uses a bridgeless Cuk bridge

converter that operates in discontinuous induction mode (DICM) for power factor correction (PFC) and better power quality (PQ) in the AC network for a wide range of speed control. The Cuk bridgeless converter operating in a DICM provides an intrinsic PFC and requires a simple voltage follower approach to control the voltage. The bridgeless converter topology is designed to achieve low conduction losses and the requirement of the small heat sink for circuit breakers. The proposed system is designed and its performance is observed so that an air conditioning system operates in a wide range of speed control with a power factor close to the unit in the AC network.

[15] suggested a brushless DC motor (BLDC) without bridge, with power factor correction (PFC) without bridge (BL) as an economical solution for low power applications. An approach to controlling the speed of the BLDC motor by controlling the intermediate voltage of the voltage source inverter (VSI) is used with a single voltage sensor. This facilitates the operation of VSI in fundamental frequency switching by electronic switching of the BLDC motor, which reduces switching losses. A BL configuration of the buck-boost converter is proposed which offers the elimination of the rectifier diode bridge, which reduces the conduction losses associated with it. A PFC BL buck-boost converter is designed to operate in discontinuous induction mode (DICM) to provide an intrinsic PFC in the AC network. The performance of the proposed engine is evaluated through a wide range of variable speed power supply and control (90-265 V universal AC network) with improved power quality in the AC network. The proposed scheme has shown satisfactory performance and is a recommended solution applicable to the low power BLDC motor.

[16] proposed a brushless DC motor driven by a switching cell converter (CSC) based on the power factor correction (PFC) (BLDC) for low power domestic applications. The BLDCM speed is controlled by varying the DC bus voltage of the voltage source inverter (VSI). The BLDCM is electronically switched to reduce switching losses in VSI due to low frequency switching. A canonical switching cell converter (CSC) is used in the front that operates in the discontinuous induction current (DICM) mode to control the DC bus voltage with the power factor of the unit in the AC network. A single sensor is used to detect the DC bus voltage for the proposed development of the inverter, which makes it an economical solution. A prototype of the proposed configuration was developed and its performance was validated with the results of speed control tests in a wide range with a power factor of the unit in the universal AC network.

[17] presented a brushless DC motor driven by a Cuk converter based on the power factor correction (PFC) as an economical solution for low power applications. The speed of the BLDC motor is controlled by varying the voltage of the DC bus of a voltage converter (VSI) which uses low-frequency VSI switching (electronic switching of the BLDC motor) for low switching losses. A diode bridge rectifier is used followed by a Cuk converter that operates in discontinuous conduction mode (DCM) to control the intermediate circuit voltage with the power factor of the unit in the AC network. The performance of the PFC Cuk converter in four different operating conditions in batch mode (DCM) and in continuous mode (CCM) is explored for the development of the BLDC motor with the PF unit in the AC network. Finally, a more suitable mode of the Cuk converter with output inductor current has been selected which operates in the DICM for experimental tests and has shown satisfactory results in all respects and is a recommended solution for low power BLDC motor drives.

[18] suggested a brushless DC motor driven by a canonical converter with bridge switching cells (BL-CSC) with power factor correction (PFC). The proposed BL-CSC converter operates in batch inductor current mode and is used to obtain a unit power factor in the AC network using a single voltage sensor. The BLDC motor speed is controlled by varying the DC bus voltage of the voltage source inverter (VSI) which supplies the BLDC motor through a PFC converter. In this way, the BLDC motor is electronically switched, so that the VSI operates with fundamental frequency switching to reduce switching losses. Furthermore, the non-bridged configuration of the CSC converter offers low conduction losses due to the partial removal of the diode bridge rectifier in the front. The proposed configuration shows a significant increase in efficiency compared to the conventional scheme. The best energy quality is achieved in the AC network for a wide range of control speeds and supply voltages and the energy quality indexes obtained are within the acceptable limits of IEC 61000-3-2.

[19] presented a Luo brushless DC motor (BL-Luo) based on power factor correction (PFC). A single voltage sensor is used to control the speed of the BLDC motor and the PFC in the AC network. The voltage follower control is used for a BL-Luo converter that operates in discontinuous induction mode. The speed of the BLDC motor is controlled by a variable voltage intermediate circuit approach, which allows a low frequency switching of the inverter from the voltage source for the electronic switching of the BLDC motor, which offers lower switching losses. The proposed BLDC motor is designed to operate in a wide range of speed control with

improved power quality in the AC network. The energy quality indexes thus obtained are lower than the limits recommended by IEC 61000-3-2. The performance of the proposed disk drive was experimentally verified in a developed hardware prototype. The satisfactory performance of the proposed inverter has been achieved and is a recommended solution for low consumption applications.

[20] proposed a brushless DC motor driven by the Cuk converter (BLDC) without bridge, without bridge, with power factor correction (PFC). An intermediate circuit voltage (VSI) of the variable voltage converter is used which supplies the BLDC motor for speed control. This allows the VSI operation in fundamental frequency switching to achieve an electronic commutation of the BLDC motor to reduce switching losses. A bridgeless configuration of an isolated Cuk converter is derived from the removal of the front diode rectifier bridge to reduce conduction losses therein. The Cuk-based unbalanced PFC converter is designed to operate in batch induction current mode to obtain an intrinsic PFC in the AC supply network. The proposed engine is controlled by a single voltage sensor to develop an economical solution. A prototype of the proposed prototype was implemented using a DSP. Better energy quality is achieved in power supply networks with energy quality indexes within the limits of the IEC 61000-3-2 standard.

[21] suggested a single-ended primary inductance converter based on power factor correction (PFC-SEPIC) which powers a brushless DC motor (BLDC) for low power devices. In a conventional BLDC motor diagram, the speed is varied by controlling the working ratio of the modulation signals of the high frequency amplification, which increases the switching losses in the inverter of the voltage source (VSI) which supplies the BLDC motor. The study presents a BLDC motor whose speed is controlled by adjusting the DC bus voltage of the BLDC motor of the VSI power supply. Furthermore, a fundamental VSI switching frequency is used to reduce switching losses when driving the BLDC motor in electronic switching. A PFC based SEPIC is designed to operate in discontinuous inductor current mode, so that voltage control is obtained from a single voltage sensor with PFC inherent to the AC power supply network; which also makes it an economical solution for low power applications. An intrinsic PFC was achieved thanks to the design of the PFC converter in DICM. The proposed drive is implemented in the inverter developed for performance evaluation. This unit is highly efficient compared to

conventional BLDC motor drive schemes with satisfactory performance of power quality at various speeds compatible with IEC 61000-3-2.

[22] presented a new configuration of the Landsman converter based on the power factor adjustment (PFR) which powers a brushless DC motor (BLDCM) for applications with low power equipment. Speed control is obtained by adjusting the DC bus voltage of the voltage source inverter (VSI) which supplies a BLDCM. Furthermore, low-frequency switching signals are used for the electronic switching of BLDCM, which reduces the switching power losses of six VSI solid-state switches. This front-end power factor corrector based on the Landsman converter that operates in discontinuous inductor current mode is used to control the DC bus voltage and the PFR is intrinsically achieved. The adjustable voltage control of the VSI DC bus was used to control the speed of the BLDCM which eventually gave the freedom to use the VSI in the low frequency switching operation for minimal switching losses.

The frequency converter DC bus voltage is controlled by the use of a single DC voltage sensor. To evaluate the performance of the proposed model, a prototype was developed in the laboratory. The operation of the BLDCM was also analyzed to determine its operation at a variable AC network voltage (90-265 V). The results of the experience relating to energy quality indexes fall within the limits of the IEC 61000-3-2 energy quality standard.

[23] proposed a Landsman converter based on a power factor correction (PFC) in a bridgeless (BL) configuration that powers a brushless DC motor (BLDCM) for low power equipment. The conduction losses associated with the diodes are reduced by the BL configuration and the switching losses of the solid-state switches of the inverter are reduced by the use of low frequency switching signals in the electronic switching for BLDCM. The Landsman BL converter based on the front PFC operating in the current mode of the batch inductor is used to control the intermediate circuit voltage and the PFC is naturally reached with reduced conduction losses and switching voltage. A single voltage sensor is used to control the DC bus voltage.

A Landsman PFC BL converter motor has been designed and developed for low power and speed adjustable domestic applications for the universal AC network. A prototype was developed to study system performance for range speed control and energy quality improvement. The BLDCM operation is also analyzed to determine its operation at a variable AC mains voltage (90-265 V) to comply with the limits defined by the IEC 61000-3-2 standard.

CHAPTER 3

DESIGN OF COMPONENTS

3.1 DESIGN OF PFC CIRCUIT

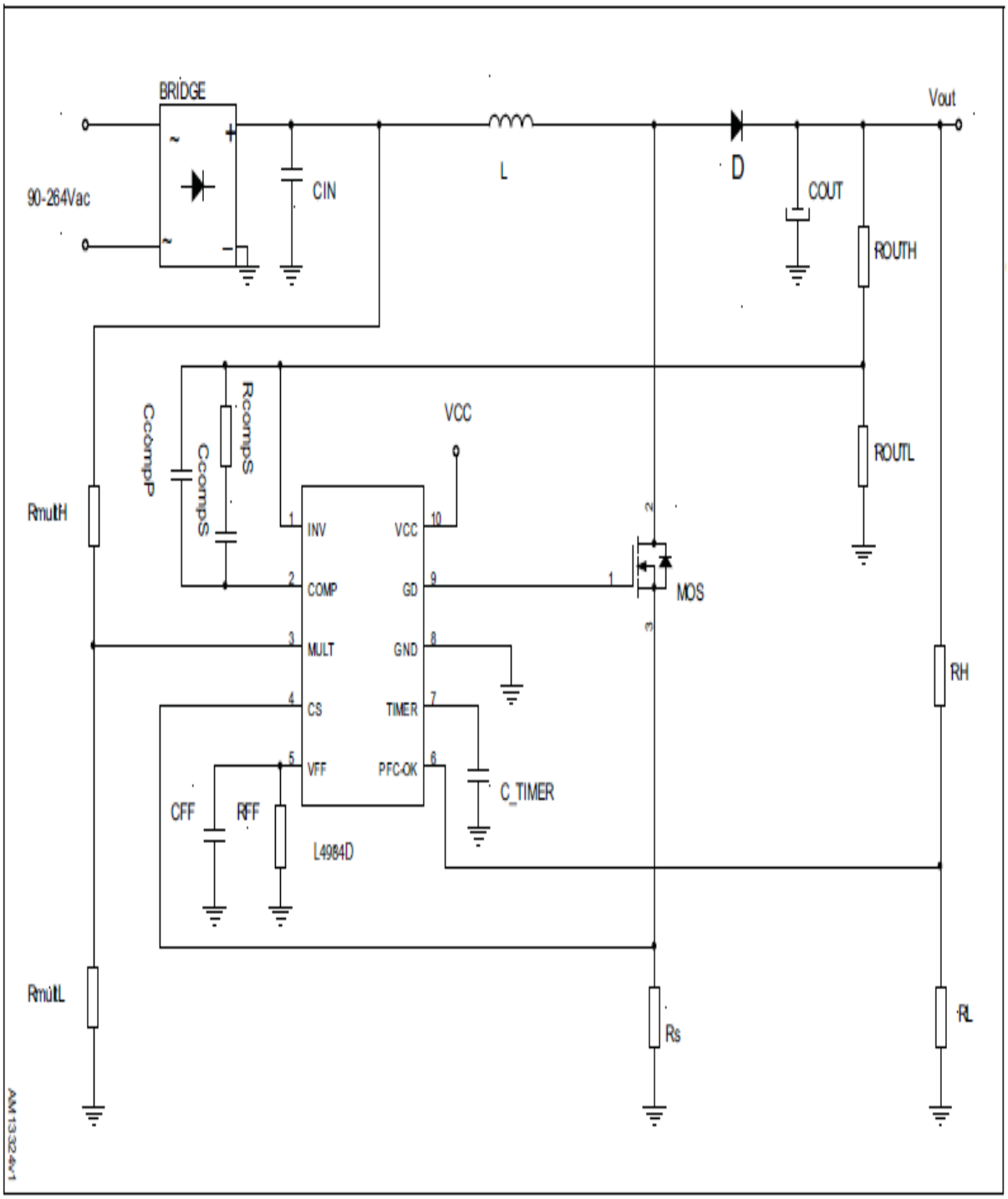


Fig. 3.1 Design of PFC Circuit

Table 3.1: INPUT PARAMETERS

PARAMETERS	VALUE
Mains Input Voltage	$V_{AC_{min}}$=100V, $V_{AC_{max}}$=300V
Minimum Mains Frequency (f_{min})	47-52 Hz
Rated Output Power *(W)*	140W
Regulated DC Output Voltage (Vdc)	450V
Expected Efficiency (%)	92%
Expected Power Factor	0.99
Maximum Output Voltage (Vdc)	480 V
Maximum Output Low Frequency Ripple (Peak-To-Peak)	22.5 V
Minimum Output Voltage After Line Drop (Vdc)	350V
Hold-Up Time (ms)	15 ms
Ripple Factor(Kr)	0.3
Maximum Ambient Temperature	50°C
Switching Frequency(fsw)	50 kHz

PART A: INPUT PARAMETERS

1. Mains Voltage Range (Vac_{rms}):

$$\text{Vac}_{\text{min}} = 100 \text{ V} \quad \textbf{(3.1)}$$

$$\text{Vac}_{\text{max}} = 300 \text{ V} \quad \textbf{(3.2)}$$

2. Minimum Mains Frequency:

$$F_{line} = 47 \text{ Hz} \quad \textbf{(3.3)}$$

3. Rated Output Power (P_0):

$$P_0 = 140 \text{ W} \quad \textbf{(3.4)}$$

4. Regulated Dc Output Voltage (V_{dc}):(It has to be higher than the maximum rectified input voltage)

$$V_{dc} = \sqrt{2} * \text{Vac}_{\text{max}} \quad \textbf{(3.5)}$$

$$= \sqrt{2} * 300 = 425 \text{ V}$$

***Chosen Value is 450V**

5. Expected efficiency (%):

$$\eta = \frac{\text{Po}}{\text{Pin}} = 92\% \quad \textbf{(3.6)}$$

6. Expected Power Factor($p.f$):

$$\text{p.f.} = 0.9 \quad \textbf{(3.7)}$$

7. Maximum Output Voltage (V_{dc}):

$$\text{Maximum output voltage } (V_{dc}) \text{ or } V_{OVP} = 480 \text{ V} \quad \textbf{(3.8)}$$

8. Maximum output low frequency ripple (peak-to-peak):

The ripple in the output voltage is generally selected 2-8% .The ratios of 5% is chosen for the output voltage ripple *i.e.* 22.25V

$$\Delta \text{Vout} = 22.5\text{V} \quad \textbf{(3.9)}$$

9. Minimum output voltage after line drop (Vdc):

$$V_{\text{out min}} = 350\ \text{V} \quad \textbf{(3.10)}$$

10. Hold-up time (ms):

$$\text{tmin} = 15\ \text{ms} \quad \textbf{(3.11)}$$

11. Ripple Factor:

$$\text{Kr} = 0.30 \quad \textbf{(3.12)}$$

12. Maximum ambient temperature (℃):

$$\text{Tamb} = 50℃ \quad \textbf{(3.13)}$$

13. Switching Frequency

$$\text{fsw} = 50\ \text{KHz} \quad \textbf{(3.14)}$$

PART B: OPERATING CONDITIONS

The first step is to define the main parameters of the circuit, using the specifications given in PART A:

1. **RATED DC OUTPUT CURRENT**:

$$\text{Iout} = \frac{\text{Pout}}{\text{Vout}} = \frac{140}{450} = 0.32\text{A} \quad \textbf{(3.15)}$$

2. **MAXIMUM INPUT POWER:**

$$\text{Pin} = \frac{\text{Po}}{\eta} = \frac{140}{.92} = 152.17\ \text{W} \quad \textbf{(3.16)}$$

3. **MAXIMUM RMS INPUT CURRENT:**

$$\text{Iin} = \frac{\text{Pin}}{\text{V}_{\text{AC}_{\text{min}}} * \text{p.f}} \quad \textbf{(3.17)}$$

$$\text{Iin} = \frac{152.17}{100*0.99} = 1.53\text{A}$$

4. **In particular $kmin$ and $kmax$ refer to the ratio of the minimum and the maximum input voltage to the output voltage, respectively.**

$$\text{kmin} = \frac{\sqrt{2} * \text{Vacmin}}{\text{Vout}} \quad \textbf{(3.18)}$$

$$kmin = \frac{\sqrt{2}*100}{450} = 0.32\text{A}$$

$$\text{kmax} = \frac{\sqrt{2} * \text{Vacmax}}{\text{Vout}} \quad \textbf{(3.19)}$$

$$\text{kmax} = \frac{\sqrt{2}*300}{450} = 0.94\text{A}$$

5. MAXIMUM LINE PEAK CURRENT:

$$\text{Ipkmax} = \frac{2 * \text{Pin}}{\text{Kmin} * \text{Vout}} \quad \textbf{(3.20)}$$

$$\text{Ipkmax} = \frac{2 * 152.17}{0.32 * 450}$$

$$\text{Ipkmax} = 2.14\ \text{A}$$

6. MAXIMUM INDUCTOR PEAK CURRENT:

$$\text{ILpkmax} = \frac{\sqrt{2} * \text{Pin}}{\text{VACmin} * \text{PF}}\left(1 + \frac{\text{Kr}}{2}\right) \quad \textbf{(3.21)}$$

$$\text{ILpkmax} = \frac{\sqrt{2} * 152.17}{100 * 0.99}\left(1 + \frac{0.3}{2}\right)$$

$$\text{ILpkmax} = 2.50$$

7. INDUCTOR PEAK-TO-PEAK RIPPLE CURRENT:

$$\Delta\ \text{ILpkmax} = \text{ILpkmax} * \text{Kr} \quad \textbf{(3.22)}$$

$$\Delta\ ILpkmax = 2.50 * 0.30$$

$$\Delta\ \text{ILpkmax} = 0.75$$

PART C: POWER SECTION DESIGN

1. INPUT CAPACITOR

The Cin capacitor is placed at the output of bridge rectifier to smooth the high frequency ripple and must sustain maximum instantaneous input voltage.

$$\mathrm{Cin} = 2.5 * 10^{-3}\mu\mathrm{F} * \mathrm{Pout} \quad \textbf{(3.23)}$$

$$Cin = 2.5 * 10^{-3}\mu F * 140$$

$$C\mathrm{in} = 350\ \mathrm{nF}$$

*** Chosen $330nF/630V$**

2. OUTPUT CAPACITOR

The value of output capacitor(Co) depends on the regulated DC output voltage, output power, the RMS current, output ripple and hold-up time.

$$\mathrm{Co} = \frac{2 * \mathrm{Pout} * \mathrm{thold}}{\left(\mathrm{Vout} - \frac{\Delta \mathrm{Vout}}{2}\right)^2 - \mathrm{V}^2{}_{\mathrm{out\ min}}} \quad \textbf{(3.24)}$$

$$Co = \mathbf{60\ \mu F}$$

*In our circuit we have chosen three **68µF/450V** capacitor

3. BOOST INDUCTOR

$$\mathrm{L(Vacmin)} = \frac{\mathrm{Vout} - \sqrt{2} * \mathrm{Vacmin)}}{\Delta\ \mathrm{ILpk(Vacmin)}} * \mathrm{Toff(Vacmin)} \quad \textbf{(3.25)}$$

- To find the value of L, first T_{OFF} needs to be calculated.

According to the datasheet of the L4984D, the linear operating range is between 0 to 3 V, so the maximum value of the multiplier input ($V_{MULT_{max}}$) is equal to 3 V.

$$\mathrm{kp} = \frac{\mathrm{Vmultmax}}{\sqrt{2} * \mathrm{Vacmax}} \quad \textbf{(3.26)}$$

$$kp = \frac{3}{\sqrt{2}*300} = 7.08*10^{-3}$$

- The switching frequency is determined by a capacitor connected between the TIMER pin and ground, charged by an accurate internal generator (**ITIMER) of 156 µA**, during the OFF time, generating a voltage ramp.

$$\mathrm{Ct} = \frac{\mathrm{ITIMER}}{\mathrm{Kp} * \mathrm{Vout} * \mathrm{Fsw}} \quad \textbf{(3.27)}$$

$$Ct = \frac{156\mu\mathrm{A}}{7.08 * 10^{-3} * 450 * 50khz}$$

$$\mathrm{Ct} = 1\mu\mathrm{f}$$

The maximum OFF-time at $VACmin$ is then:

$$\mathrm{Toff(Vacmin)} = \frac{\mathrm{Ct} * \mathrm{Kp}\sqrt{2} * 100}{\mathrm{ITIMER}} \quad \textbf{(3.28)}$$

$$\mathrm{Toff(Vacmin)} = \frac{1\mathrm{uf} * 7.08 * 10^{-3} * \sqrt{2} * 100}{156\mu\mathrm{A}}$$

$$\mathrm{Toff(Vacmin)} = 6.42\mu\mathrm{s}$$

The value of the inductance L required for the boost inductor at $V_{AC_{min}}$ can now be

$$\mathrm{L(Vacmin)} = \frac{\mathrm{Vout} - \sqrt{2} * \mathrm{Vacmin})}{\Delta\ \mathrm{ILpk(Vacmin)}} * \mathrm{Toff(Vacmin)} \quad \textbf{(3.29)}$$

$$\mathrm{L(Vacmin)} = \frac{450-\sqrt{2}*100}{0.75} * 6.42\mu\mathrm{s} = 2700\ \mu\mathrm{H}$$

*In the design we have used 3200 µH

PART D: L4984D BIASING CIRCUIT

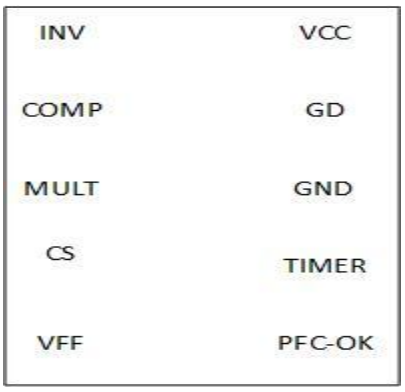


Fig. 3.2 – Pin Diagram of L4984D

This section describes the selection of the circuitry around the L4984D IC.

- **Feedback and OVP**

Pin 1 (INV): this pin is connected both to the inverted input of the E/A and to the OVP circuits. A resistive divider must be connected between the regulated output voltage of the reinforcement and this pin. The internal reference of the non-inverting input of E/A is generally 2.5 V; the output voltage (V_{out}) of the PFC pre-controller is set to the nominal value for the resistance ratio of the feedback output divider. R_{out_H} and R_{out_L} will be selected considering the desired nominal output voltage and the desired output power dissipated in the output splitter [24].

For 25mW output divider dissipation:

$$R_{outH} = \frac{(V_{out}-2.5V)^2}{25mW} = 8.2\ M\Omega \quad \textbf{(3.30)}$$

Here are three 2.7MΩ resistors in series have been selected.

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5V} - 1 = 179 \quad \textbf{(3.31)}$$

$$R_{outL} = \frac{V_{out}}{179} = \frac{9M\Omega}{179} = 50.3k\Omega \quad \textbf{(3.32)}$$

For R_{outL} a value of 130kΩ in parallel to an 82kΩ has been selected.

Pin 6 (PFC_OK - Protection against feedback faults): the PFC_OK pin has been dedicated to controlling the output voltage of a separate resistance divider. This divider is selected so that the voltage on the pin reaches 2.5 V if the output voltage exceeds a preset value (V_{ovp}), generally greater than the maximum V_{out} that can be expected, including even the line / load transients in the worst of the cases. For a maximum output voltage $V_{out_{max}}$ of 480 V and select a current of 30μA in the divider:

$$R_L = \frac{V_{REF\_PFC\_OK}}{I_{divider}} = \frac{2.5V}{30\mu A} = 83k\Omega \quad \textbf{(3.33)}$$

By selecting a commercial value of 82k**Ω**

$$R_H = R_L\left(\frac{V_{OUT\_MAX}}{V_{REF\_PFC\_OK}} - 1\right) = 82k\Omega\left(\frac{480V}{2.5V} - 1\right) = 15.6\ M\Omega \quad \textbf{(3.34)}$$

- **Current Sense Resistor**

Pin 4(CS):- Pin 4 is the inverting input of the current direction comparator. Through this pin, the L4948D detects the instantaneous current of the inductor, converted into a proportional voltage by an external sensing resistor (Rs) [24].

$$R_s = \frac{V_{sc(min.)}}{I_{LPK(max.)}} \quad \textbf{(3.35)}$$

$$R_s < \frac{0.84}{2.14} = 0.39\ m\Omega \quad \textbf{(3.36)}$$

I. I_{Lpk} is the maximum peak current in the inductor

II. $V_{csm\ in}$ = 0.84V is the minimum value of the L4984D current sense reference clamp

$$IL_{pks} = \frac{0.93}{0.39} = 2.38A$$

The calculated $I_{L_{pks}}$ will be the value at which the reinforcement inductor will not be saturated and will be used to calculate the number of turns and the length of the air space of the inductor.

Pin 5(VFF): - The L498D uses capacitor C_{FF} and a resistor R_{FF}, to implement voltage feed-forward technique and to complete the internal peak maintenance circuit providing a DC voltage equal to the peak of the rectified sine wave applied on the MULT pin (PIN3).

$$\mathbf{C_{FF} = 1\mu F \text{ and } R_{FF} = 1M\Omega}$$

Pin 3(MULT):

$$R_{multL} = \frac{V_{MULT\,max}}{I_{MULT}} = \frac{3.00V}{64\mu A} = 47k\Omega \quad \textbf{(3.37)}$$

$$R_{multH} = \left(\frac{1 - k_p}{k_p}\right) R_{multL} \quad \textbf{(3.38)}$$

$$R_{multH} = \left(\frac{1-7.08*10^{-3}}{7.08*10^{-3}}\right)47k\Omega = 6.6M\Omega$$

3.2 DESIGN OF FLYBACK CONVERTER

Each SMPS project begins to determine the system requirements and specifications. The following parameters must be defined and determined.

Table 3.2 System Specifications

PARAMETERS	VALUE
$\mathbf{V_{DCMIN}}$	425
$\mathbf{V_{DCMAX}}$	450
$\boldsymbol{Fsw}$	50kHz
EFFICIENCY	90%
$\mathbf{V_{out}}$	31 V
Pout	120 W
Duty Cycle	0.3947
Input Power	133.34W
Output Ripple voltage	0.12 V

STEP-1: -TO DECIDE THE PRIMARY REFLECTIVE VOLTAGE OF THE FLIGHT (V_R) AND THE VALUE OF THE MOSFET$V_{DS_{max}}$: -

The primary reflected voltage V_R plays an important role in determining the activation point of the valley V_{DS}. In the case of Fly-back, the choice of the V_R value greatly affects many important parameters and electrical parameters of the converter (for example, the V_{DS} classification of the MOSFET). Similarly, it is true for QR, but in addition, the V_R value also determines the V_{DS} valley.

The higher the value of V_R, the lower the valley and the lower the ignition losses in the MOSFET.

Considering voltage spike due to leakage inductance, the maximum drain to source voltage is:

$$\mathbf{V_{Dsmax} = V_{DCmax} + V_R + V_{Spike}} \quad \textbf{(3.39)}$$

Where: V_{spike} is the peak voltage caused by the leakage inductance of the Fly-back transformer. For a starting point, suppose that V_{spike} is 30% of$V_{DS_{max}}$.

The following table 3.3lists a recommended reflected voltage based on a nominal 650V or 800V MOSFET [25]. As a starting point, choose V_R that is not greater than 100 V for a broad-spectrum input voltage source. The choice of the reflected voltage is a compromise between the primary MOSFET and the secondary rectifier voltage. If set too high, by means of a higher rpm ratio, it would mean a MOSFET with a higher V_{DS} value to be used in the primary voltage but lower in the secondary rectifier. If set to a value too low, for a lower rotation ratio, $V_{DS_{max}}$ would decrease but the secondary rectifier voltage would increase.

Table 3.3 Recommended V_R on 650 and 800V MOSFET

V_{IN}	MOSFET $V_{DS_{max}}$	Recommended Max V_R
Low Line Input	600 V	150 V
Wide Range AC Input 85-150 V_{AC}	650 V	100 V
Wide Range AC Input 85-264 V_{AC}	800 V	250 V
Input from High Voltage DC 400 V_{DC}	800 V	250 V

STEP 2:- CALCULATION OF PARAMETERS

Assuming a 30% loss in peak, the maximum expected V_{DS} is equal to: (V_r=230 V)

$$V_{DS_{max}} = V_{DC_{max}} + V_R + V_{spike}\ (30\%\ \text{of}\ \mathrm{V_{DCmax}})$$

$$= 450+150+30\%\ \text{of}\ 450$$

$$= 735\ \mathrm{V}$$

STEP 3:-Determining $Dmax$ based on V_R and V_{dcmin}

The maximum duty cycle will be displayed during$V_{DC_{min}}$, in this condition we will design the transformer which will be in the limit of DCM and CCM. The duty cycle here is given by

$$\mathrm{Dmax} = \frac{\mathrm{V_R}}{\mathrm{V_R} + \mathrm{V_{dcmin}}} \quad \textbf{(3.40)}$$

$$\mathrm{Dmax} = \frac{150}{150 + 230}$$

$$\mathrm{Dmax} = 0.3947$$

STEP 4: - Determining the peak current ($\mathrm{I_{Peak}}$) and Primary inductance ($\mathrm{L_{max}}$)

$$\mathrm{Ipeak/Ipri} = \frac{2 \times \mathrm{Pinmax}}{\mathrm{V_{dcmin}} \times \mathrm{Dmax}} \quad \textbf{(3.41)}$$

$$\mathrm{Ipeak/Ipri} = \frac{2 \times 133.34}{230 \times .3947}$$

$$\mathrm{Ipeak/Ipri} = 2.93\mathrm{A}$$

$$\mathrm{Lpri} = \frac{\mathrm{Vdcmin} \times \mathrm{Dmax}}{\mathrm{Fsw} \times \mathrm{Ipeak}} \quad \textbf{(3.42)}$$

$$\mathrm{Lpri} = \frac{230 \times .3947}{50 * 10^3 \times 2.93}$$

$$\mathrm{Lpri} = 620\mu\mathrm{H}$$

*By increasing the inductance beyond the calculatedL_{pri}, it is also possible to push the converter into CCM mode.

DCM Fly back Transformer Design: Steps 5- Step 12

STEP 5: - Choose the type and size of the right core

ETD39

16-Pin, THT, Horizontal

Core gap 1.2mm

Inductance Factor-A_l=122nH/n

Ae=124.70mm^2

b_{max}=320

Take 80% of b_{max}*i.e.* 256

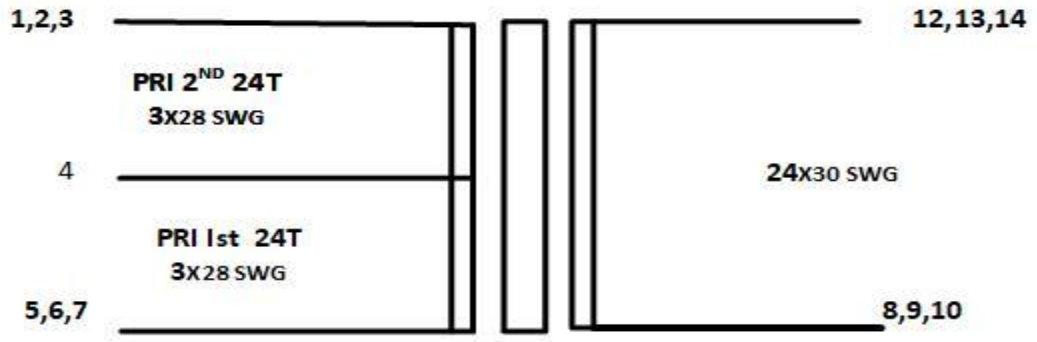


Figure 3.3Fly Back Transformer Core

STEP6:-Determination of minimum primary turns

The minimum number of turns in the primary is a function of the area of the magnetic core and the density of the operating flow allowed for the chosen material

$$\mathrm{Np} = \frac{\mathrm{Lp} * \mathrm{Ipri}}{\mathrm{Bmax} * \mathrm{Ae}} \quad \textbf{(3.43)}$$

$$\mathrm{Np} = \frac{620 * 2.93}{256 * 124.70}$$

$$\mathrm{Np} = 57$$

Where $b_{max}$the maximum is operational flow density, L_P is the primary inductance, I_{pri} is the maximum primary current and A_e is the area of the cross section of the type of core chosen.

It is important that the performance of b_{max}doesnot exceed the density of the saturation flow (V_{sat}) contained in the main data sheet. The ferrite of the ferrite core varies depending on the core material and temperature, but most of them have a closed b_sat classification at 400mT. If no more reference data are used b_{max} = 300mT. Maggiore b_{max} allows fewer primary turns due to less driving loss, but with greater core loss.

STEP 7: Determines the number of turns for the secondary main (Ns)

CALCULATION OF TURN RATIO

$$\mathrm{n} = \frac{\mathrm{V_R}}{\mathrm{V_{out}} + \mathrm{V_D}} \quad \textbf{(3.44)}$$

$$n = \frac{150}{31 + .5}$$

$$n = 4.76$$

V_{out} is the output voltage and V_D is the voltage drop of the secondary diode, typically 0.5 V for schottky diode with a low to moderate current value.

NOW CALCULATION OF SECONDARY NUMBER OF TURNS

$$\mathrm{Ns} = \frac{\mathrm{Np}}{\mathrm{n}} \quad \textbf{(3.45)}$$

$$\mathrm{Ns} = \frac{57}{4.76} \sim 12 = 58$$

***So, we choose Primary turns (Np) = 58; Secondary turns (Ns) =12**

STEP 8:-Determination of the cable size for each output windings

$$\text{Primary Winding RMS Current:}\quad \text{Iprms} = \text{Ip} \times \sqrt{\frac{\text{Dmax}}{3}} \tag{3.46}$$

$$\text{Iprms} = 2.93 \times \sqrt{\frac{0.3947}{3}}$$

$$\text{Iprms} = 1.06\text{A}$$

$$\text{Isecpk} = \text{Ip} \times \frac{\text{Np}}{\text{Ns}} \tag{3.47}$$

$$\text{Isecpk} = 1.06 \times \frac{58}{12}$$

$$\text{Isecpk} = 5.136\ \text{A}$$

$$\text{Secondary Winding RMS Current Isecrms} = \text{Isecpk} \times \sqrt{\frac{\text{Dmax}}{3}} \tag{3.48}$$

$$\text{Isecrms} = 5.136 \times \sqrt{\frac{1 - .3947}{3}}$$

$$\text{Isecrms} = 2.30\ \text{A}$$

STEP 9: - Output Capacitor Selection

$$\text{Cout} = \frac{\text{Iout} * \text{ncp}}{\Delta\text{Vout} * \text{Fsw}} \tag{3.49}$$

$$\text{Cout} = \frac{3.87 * 20}{0.12\text{V} * 50\text{khz}}$$

$$\text{Cout} = 13\ \mu\text{F}$$

*$N_{cp}$is the number of internal clock cycles that the control loop must reduce the duty cycle from the maximum to the minimum value. This usually takes about 10-20 switching periods. I_out is the maximum output current.

ESR (Equivalent series resistance):-

$$\text{Resr} = \frac{\Delta V_{out}}{\text{Isecpk}} \quad \textbf{(3.50)}$$

$$\text{Resr} = \frac{0.12}{13.14}$$

$$\text{Resr} = 9.14 \text{ mili ohm}$$

STEP 10: - Output filter Design:-

$$\text{Lout} = 20\mu H$$

$$C = \frac{(\text{Cout} * \text{Resr})^2}{\text{Lout}} \quad \textbf{(3.51)}$$

$$C = \frac{(13uf * 9.14mohm)^2}{20uh} = 706\ \mu F$$

CHAPTER 4
CONTROL STRATEGIES

4.1 POWER FACTOR CORRECTION

The power factor correction is used to model the input current and there are several control strategies to achieve the same. The techniques described below are adopted for boost converter and can be further implemented for other converter topologies.

4.1.1 PEAK CURRENT CONTROL with CCM mode

The peak current control strategy for the boost converter is shown in fig. 4.1. It represents the waveform of the input current that is formed to obtain the power factor correction. In the peak current control strategy, the switch is turned on and off at a constant frequency. The switch is OFF when the sum of the positive ramp of the inductor current (switch current) reaches the reference value. The sinusoidal reference is obtained by multiplying a rectified sinusoidal half Vg of the rectifier bridge output with the output of the error amplifier that determines the current reference. The current reference signal is naturally synchronized and is always proportional to the line voltage, which is the main condition for reaching the power factor of the unit. In the peak current control, the inverter operates in continuous conduction mode (CCM). The additional advantage of the peak current control is the low current voltage and the input filter requirement [26].

ADVANTAGES

- Constant switching frequency
- Detection of the input current based on the current of the switch
- The error amplifier and its compensation network are not required.
- Impulse current limit increases reliability and speed

DISADVANTAGES

- The control action is sensitive to noise.
- For work cycles greater than 50%, there are sub harmonic oscillations for which a compensation network is required

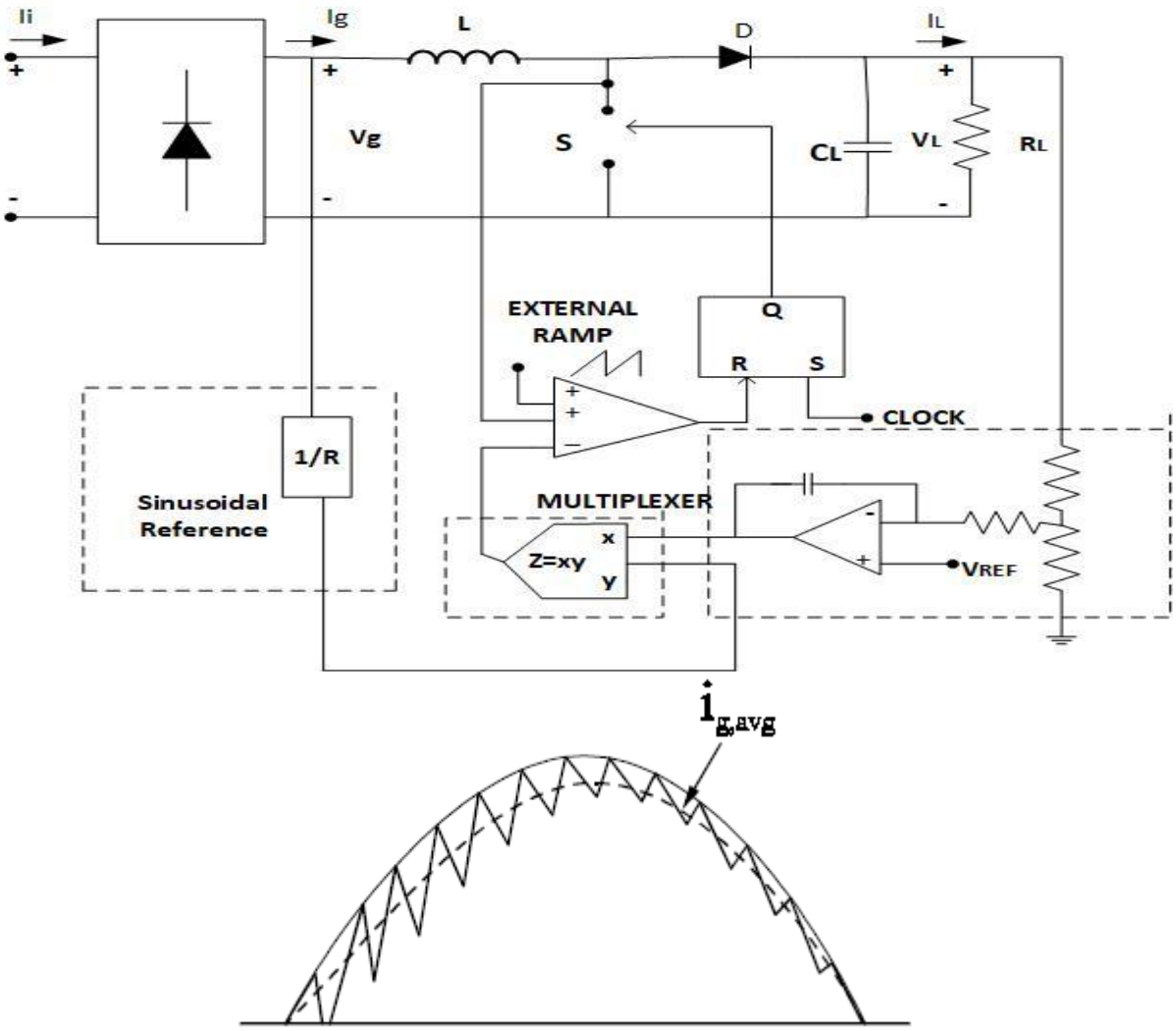


Fig. 4.1: - Peak Current Control Scheme

4.1.2 AVERAGE CURRENT CONTROL

When checking the average current, the average converter current is controlled by detecting the inductor current as shown in Fig. 4.2. The inductor current is filtered by an error amplifier whose output controls the PWM modulator. When the average current is controlled, the converter operates in continuous conduction mode (CCM) [27], [28].

ADVANTAGES

- Constant Switching Frequency
- For duty cycle greater than 50%, there is no requirement of ramp
- Control technique is less prone to communication
- The input current waveform is better than the peak current control technique

DISADVANTAGES

- Detection of inductor current is compulsory
- A current error amplifier is required and its compensation network design must take into account the different operating points of the converter during the line cycle

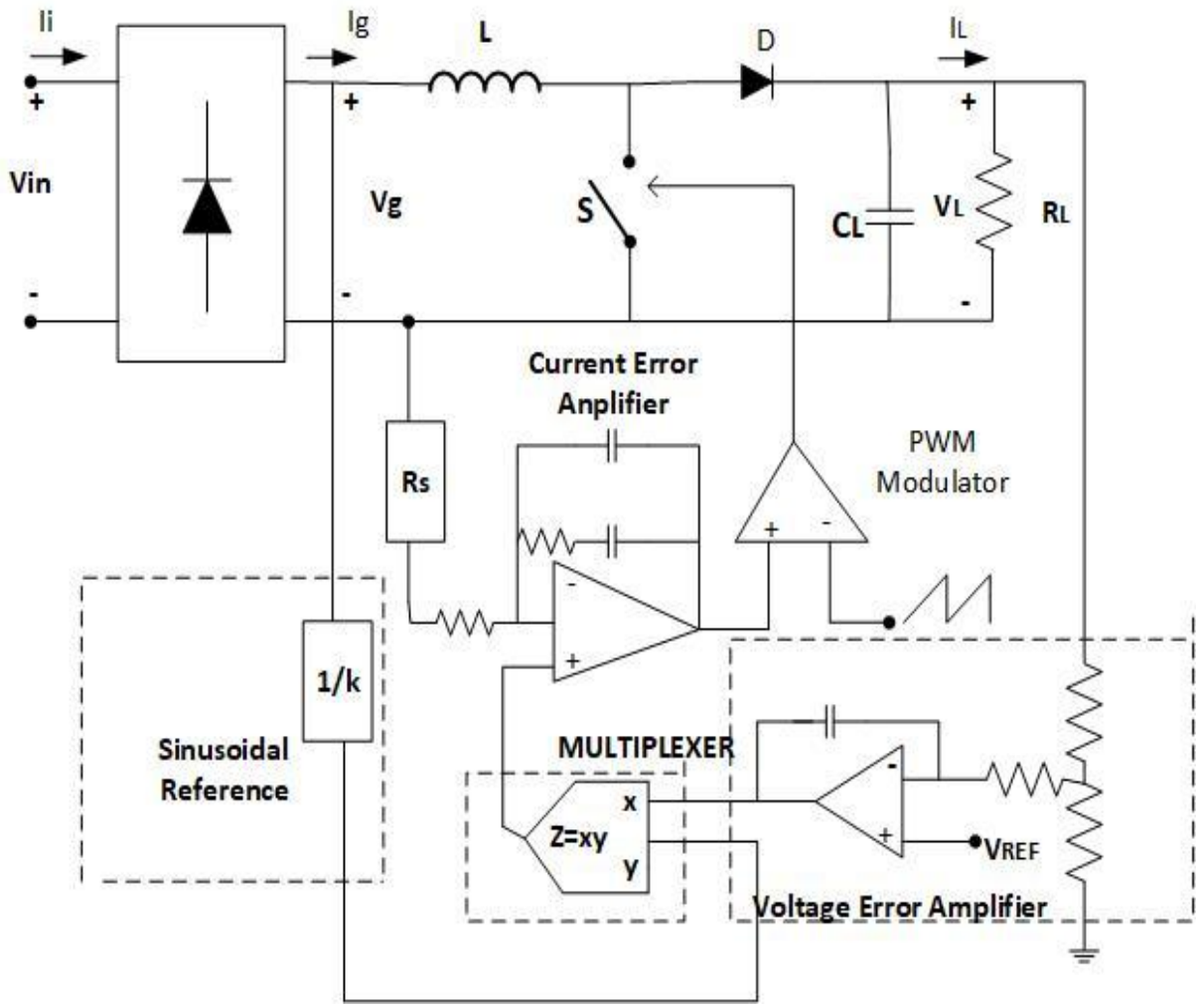


Fig. 4.2: - Average Current Control Scheme

4.2 SPACE VECTOR PULSE WIDTH MODULATION

Currently there are several control strategies implemented in digital systems and, therefore, digital modulation techniques are also available. The technique of modulation based on space vectors is a digital technique and is very different from traditional PWM methods. With PWMs, the inverter can be considered as three phases of thrust and traction, which independently create each phase waveform. Space-Vector PWM, however, considers the inverter as a single unit; specifically, the investor can be guided in eight unique states. The modulation is accompanied by the switching of the inverter status. Control strategies are implemented in digital systems. SV-PWM is a digital modulation technique in which the objective is to generate PWM load line voltages that are on average equal to a given load line voltage (or reference). This occurs in each sampling period by correctly selecting the switching states and calculating the appropriate time period for each state. The selection of states and their time periods is carried out by transforming the space vector (SV) [29].

4.2.1 SPACE-VECTOR TRANSFORMATION

Any three-time functions that satisfy

$$u_{a(t)} + u_{b(t)} + u_{c(t)} = 0 \quad \textbf{(4.1)}$$

It can also be represented in a two-dimensional space. The coordinates are similar to those of three-phase voltages, so the vector $[u_a\ 0\ 0]^T$ is placed along the x axis, the vector$[0\ u_b\ 0]^T$ is changed in phase 120°, and the vector$[0\ 0\ u_c]^T$ moves in phase at 240°. The space vector (SV) in complex notation is then given by

$$\text{u(t)} = \frac{2}{3}[u_a + u_b e^{j(2/3)\pi} + u_c e^{-j(2/3)\pi}] \quad \textbf{(4.2)}$$

where 2/3 is a scale factor. The preceding equation can be written in real and imaginary components in the α-β domain like

$$\text{u(t)} = u_\alpha + \text{j}u_\beta \quad \textbf{(4.3)}$$

Using the equations (4.2) and (4.3), we can obtain the transformation of the coordinates from the a-b-c axis to the α-β axis as indicated by

$$\begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} = \frac{2}{3}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}\begin{pmatrix} u_a \\ u_b \\ u_c \end{pmatrix} \quad \textbf{(4.4)}$$

which for a balanced system can also be written as: -

$$u_\alpha = \frac{2}{3}[v_a - 0.5(v_b + v_c)] \quad \textbf{(4.5)}$$

$$u_\beta = \frac{1}{\sqrt{3}}(v_b - v_c) \quad \textbf{(4.6)}$$

For each pole, two states are possible. Either '0' or '1'. We have total 2^3 states and using the combination of these states we have to generate the PWM pulse.

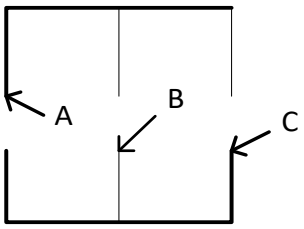


Fig. 4.3:- Switching Sequence (100)

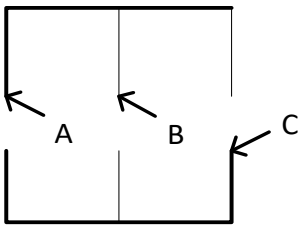


Fig. 4.4:- Switching Sequence (110)

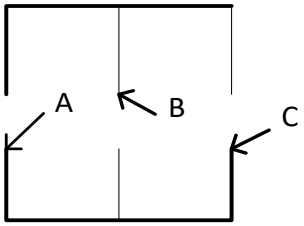


Fig. 4.5:- Switching Sequence (010)

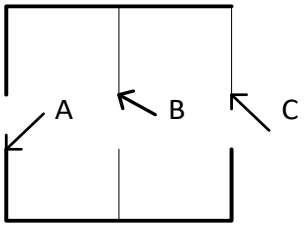


Fig. 4.6:- Switching Sequence (011)

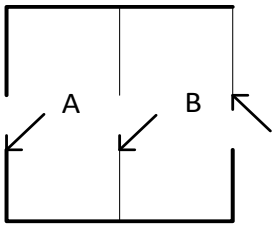


Fig. 4.7:- Switching Sequence (110)

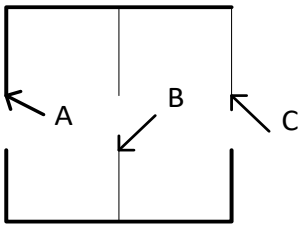


Fig. 4.8:- Switching Sequence (101)

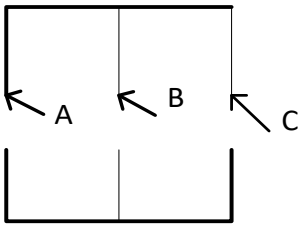


Fig. 4.9:- Switching sequence (111)

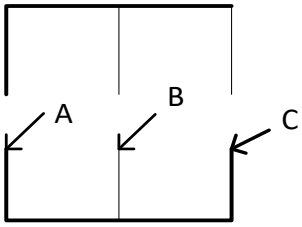


Fig. 4.10:- Switching Sequence (000)

The Fig. (4.3) - (4.8) are called active states (or vectors) producing non-zero output states. And switching sequences represented in Fig. (4.9), (4.10) are referred to as zero state vectors. Also, Fig. 4.11 represents the combined representation of active and zero switching states which in turn trace a hexagon shaped structure. All the six active voltage vectors (states) lie along the radii of the hexagon. The mean variation of the space voltage vector or the tip of the space voltage vector should move along a circular path as shown in Figure 4.12, i.e. a circle drawn with a uniform speed.

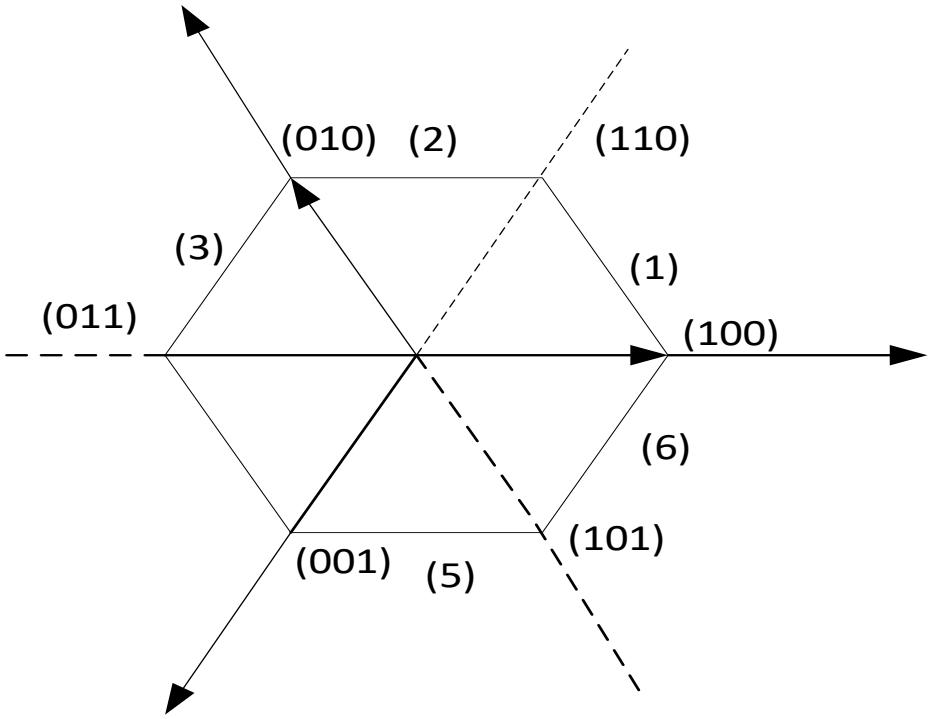


Fig. 4.12Active and Zero Switching State Representation

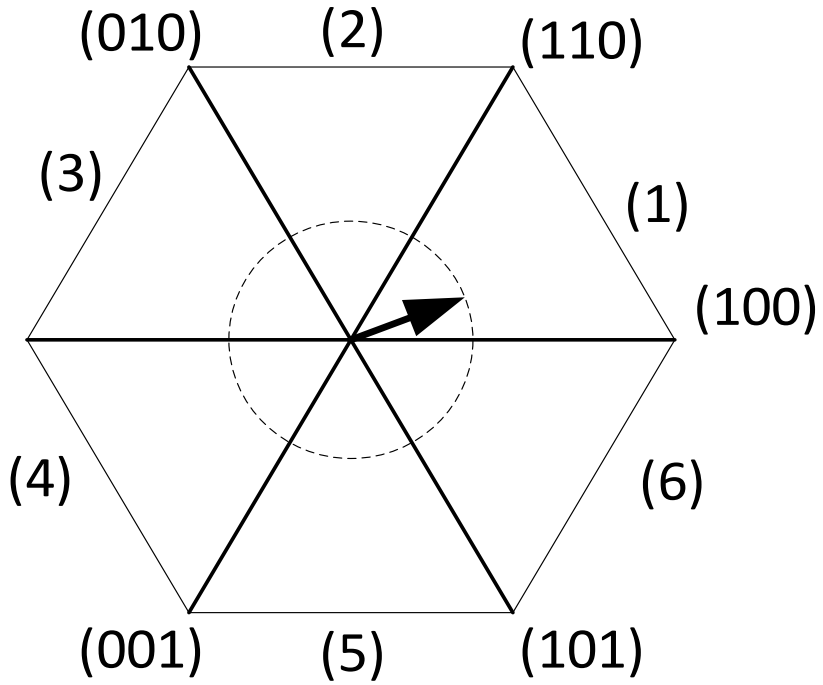


Fig. 4.12 Space Vector Representation (V_S)

We will take samples of the space vector Vs at high sampling frequency. The continuous sinusoidal variation will result in very high sampling rate in such a manner that it will result in reduction in switching losses [30]. Using volt-sec balance equation as represented in Fig. 4.13 along α and β axis respectively

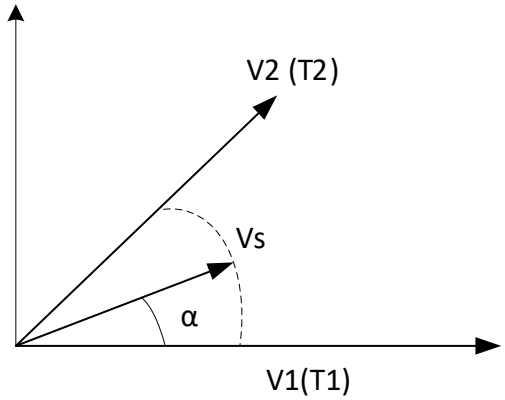


Fig. 4.13 Volt-Sec Balance (in Sector-1)

X and Y-Axis in the above figure represents V_α and V_β axis respectively.

$$T_0 = T_S - (T_1 + T_2) \quad \textbf{(4.7)}$$

Volt-sec balance along α-axis

$$V_1 T_1 + [V_2 \cos 60^0] T_2 = V_S T_S \cos \alpha \quad \textbf{(4.8)}$$

Volt-sec balance along β-axis

$$0 + [V_2 \sin 60^0] T_2 = V_S T_S \sin \alpha \quad \textbf{(4.9)}$$

Now Assuming $V_1 = V_2 = V_S$

The value of T_1 and T_2 from the above two equations can be calculated as

$$T_1 = \frac{2T_S V_S}{\sqrt{3} V_{DC}} \sin(60^0 - \alpha) \quad \textbf{(4.10)}$$

$$T_2 = \frac{2T_S V_S}{\sqrt{3}V_{DC}} \sin(\alpha) \quad \textbf{(4.11)}$$

To restrict the switching losses to the lowest level we aim for minimum switching for all the sectors in inverter operation [30]. Also, during sampling period *i.e.* sub interval between two sectors switching sequence is decided in such a way that only one phase is changed and the stress is minimum on the switches.

$$V_{A_0(avg.)} = \frac{V_{DC}/2}{T_S}\left[-\frac{T_0}{2} + T_1 + T_2 + \frac{T_0}{2}\right] \quad \textbf{(4.12)}$$

$$V_{B_0(avg.)} = \frac{V_{DC}/2}{T_S}\left[-\frac{T_0}{2} - T_1 + T_2 + \frac{T_0}{2}\right] \quad \textbf{(4.13)}$$

$$V_{C_0(avg.)} = \frac{V_{DC}/2}{T_S}\left[-\frac{T_0}{2} - T_1 - T_2 + \frac{T_0}{2}\right] \quad \textbf{(4.14)}$$

The preceding equations clearly indicate that the zero vector voltages do not correspond to the average variation and that only the voltages of the poles contribute to it [30].Also, the $V_{A_0(avg.)}$ & $V_{B(avg.)}$ are plotted according to sector switching sequence as show in Fig. 4.14.

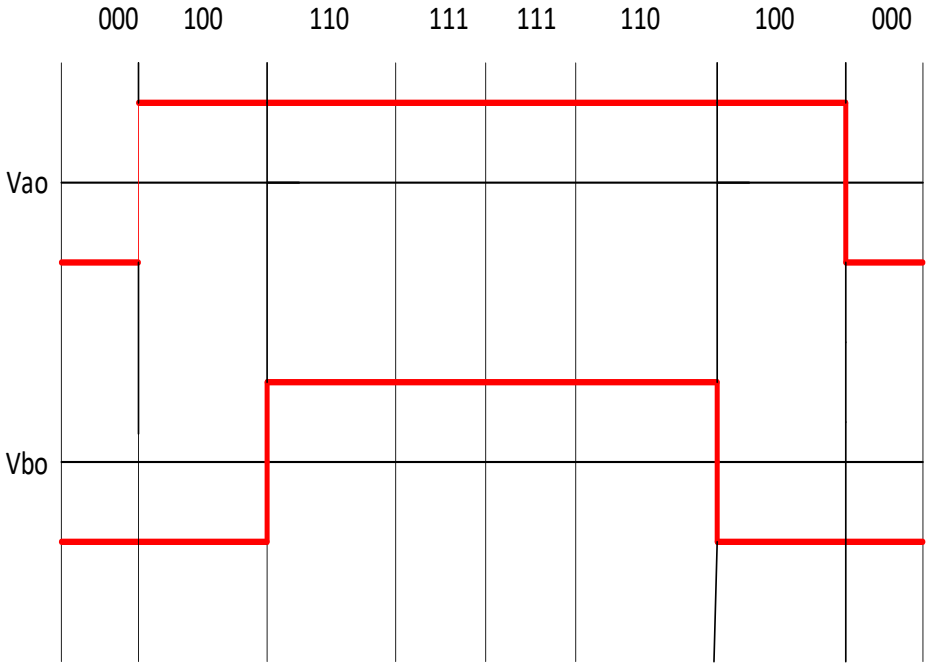


Fig. 4.14 Sector Switching Sequence (0-1-2-0-0-2-1-0)

$$V_{A_0(avg.)} = \frac{V_{DC}/2}{T_S}[\,T_1 \;+\; T_2] \tag{4.15}$$

$$V_{B_0(avg.)} = \frac{V_{DC}/2}{T_S}[-T_1 \;+\; T_2] \tag{4.16}$$

$$V_{C_0(avg.)} = \frac{V_{DC}/2}{T_S}[-T_1 \;-\; T_2] \tag{4.17}$$

T_1 and T_2 represented in the above equations indicate time taken by active states in a sector for reference space vector having a general angle.

By substituting the values of T_1 and T_2 from equations (4.10) and (4.11) into equations (4.15), (4.16) and (4.17) we get

$$V_{A_0(avg.)} = \frac{V_S}{\sqrt{3}}[\sin(60^0 - \alpha) + \sin(\alpha)] \tag{4.18}$$

$$V_{B_0(avg.)} = \frac{V_S}{\sqrt{3}}[-\sin(60^0 - \alpha) + \sin(\alpha)] \tag{4.19}$$

$$V_{C_0(avg.)} = \frac{V_S}{\sqrt{3}}[-\sin(60^0 - \alpha) - \sin(\alpha)] \tag{4.20}$$

Using the identity

$$\sin(A) + \sin(B) = 2\sin\left(\frac{A+B}{2}\right)\cos\left(\frac{A-B}{2}\right) \tag{4.21}$$

The equations (4.18), (4.19), (4.20) can be rewritten as

$$V_{A_0(avg.)} = \frac{V_S}{\sqrt{3}}\sin(60^0 + \alpha) \tag{4.22}$$

$$V_{B_0(avg.)} = V_S \sin(\alpha - 30^0) \tag{4.23}$$

$$V_{C_0(avg.)} = -V_S \sin(60^0 + \alpha) = -V_{A_0(avg.)} \tag{4.24}$$

Hence, if we know the average variation for 90^0 we can repeat the sequence for other sectors also.

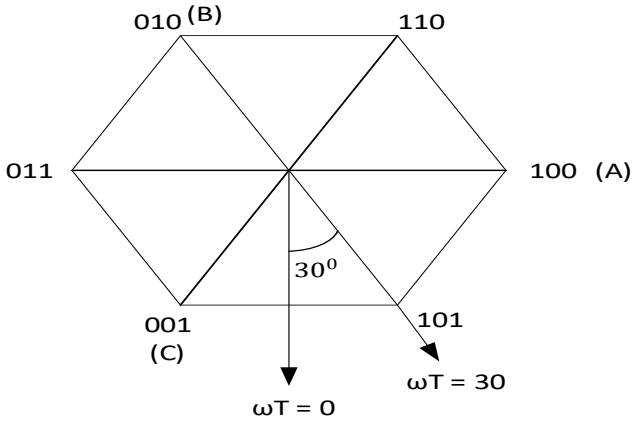


Fig. 4.15 Switching Sample (in Sector - 5 $\omega t = 0^o$ to $\omega t = 30^o$)

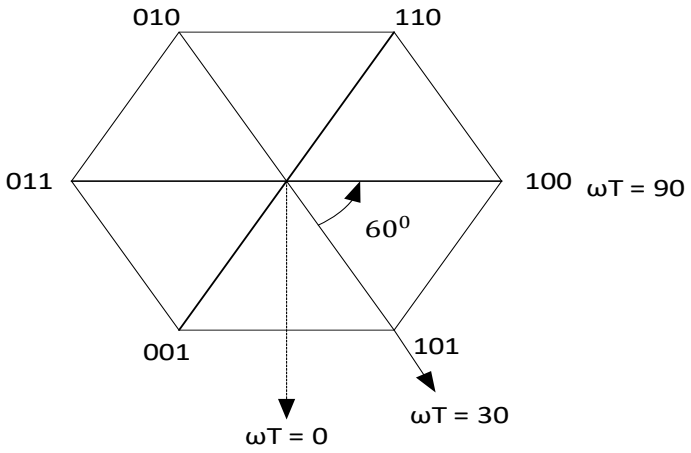


Fig. 4.16 Switching Sample (in Sector - 6 $\omega t = 30^o$ to $\omega t = 90^o$)

In sector 5, for $0 \leq \omega t \leq 30^0$as shown in Fig. 4.15 the $V_{A_0(avg.)}$ is the same as the $V_{B_0(avg.)}$ in sector 1.

i.e. $V_{B_0(avg.)} = V_S \sin(\alpha - 30^0)$ and $\alpha = \omega t + 30^0$

Hence the expression for $V_{A_0(avg.)}$ can be written as and equal to $V_S \sin(\alpha - 30^0)$

$$V_{A_0(avg.)} = V_S \sin(\omega t + 30^0 - 30^0) = V_S \sin(\omega t) \quad \textbf{(4.25)}$$

In sector 6, for $30^0 \leq \omega t \leq 90^0$as shown in Fig. 4.16 the $V_{A_0(avg.)}$ is the same as the $V_{B_0(avg.)}$ in sector 1.

i.e. $V_{A_0(avg.)} = \frac{V_S}{\sqrt{3}} \sin(\alpha - 30^0)$ for $30^0 \leq \omega t \leq 90^0$ or $0^0 \leq \alpha \leq 60^0$

Hence the expression for $V_{A_0(avg.)}$ can be written as $\frac{V_S}{\sqrt{3}} \sin(\omega t + 30^0)$.

4.3 BRUSHLESS DCMOTOR CONTROL

4.3.1 BLDC MOTOR Fundamentals

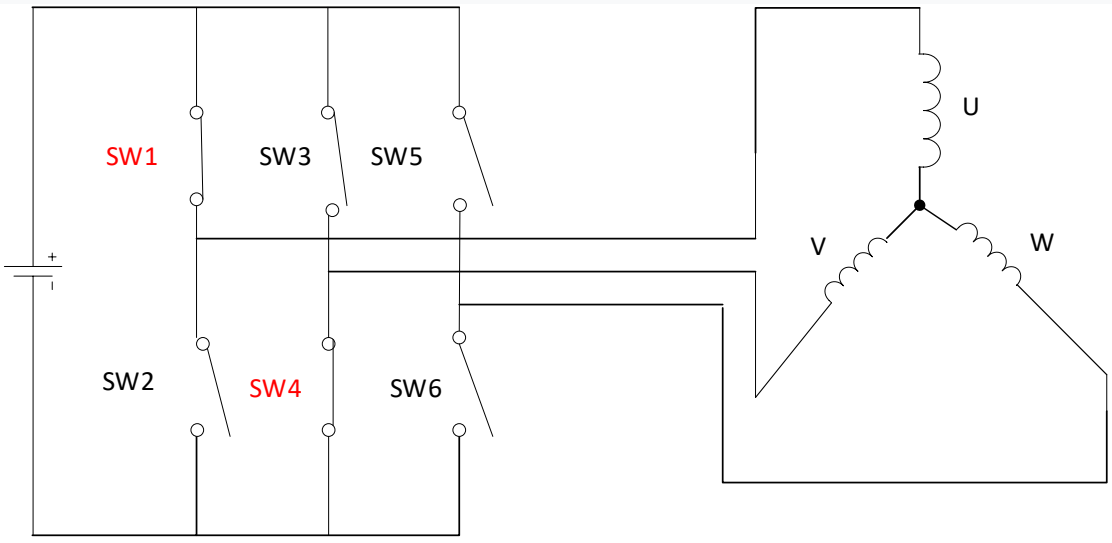
In order to make operation more reliable, more efficient, less noisy the recent trend has been of using brushless DC motor. They are also lighter as compared to brushed motors with same power output. The brushes in conventional DC motors wear out over the time and may cause sparking. Thus, the brushed DC motor should never be used for operations that demand long life and reliability. The rotor of a BLDC motor is a permanent magnet and the stator has a three-phase coil arrangement. By applying DC power to the coil, the coil will energize and will become an electromagnet. The operation of a BLDC motor is based on simple force center action between the permanent and the electromagnet, in this condition when any one random coil A is energized the opposite poles of rotor and stator are attracted to each other. As the rotor nears the energized coil, the adjacent coil B is energized and as the rotor nears coil B the coil C is energized. After that the coil A is again energized but with opposite polarity, this process is repeated and the rotor continues to rotate. Even though the motor will work in above condition but it has one drawback i.e. at any given instant only one coil is energized and the two dead coils greatly reduce the power output of the motor. To overcome this problem, two coils are energized in such a way that one coil always remain behind another coil and will push the rotor, for this incident, same polarity current is passed through the second coil, the combined effect produces more torque and power output from the motor. The combined force also makes sure that the BLDC motor has constant torque nature. Instead of energizing two separate coils, by making small modification to the stator coil we can simplify this process. The only thing required to be done is to connect the one free end of both coils together, when the power will be applied between those two coils the current flowing through the coils will be just like separately energized state. That’s how a BLDC motor works. In a BLDC motor we use an electronic controller whose sensor determines the position of the rotor which determines which stator coils to energize and when to energize. Most often a Hall Effect sensor is used for that purpose.

4.3.2 ELECTRONIC COMMUTATION PRINCIPLE

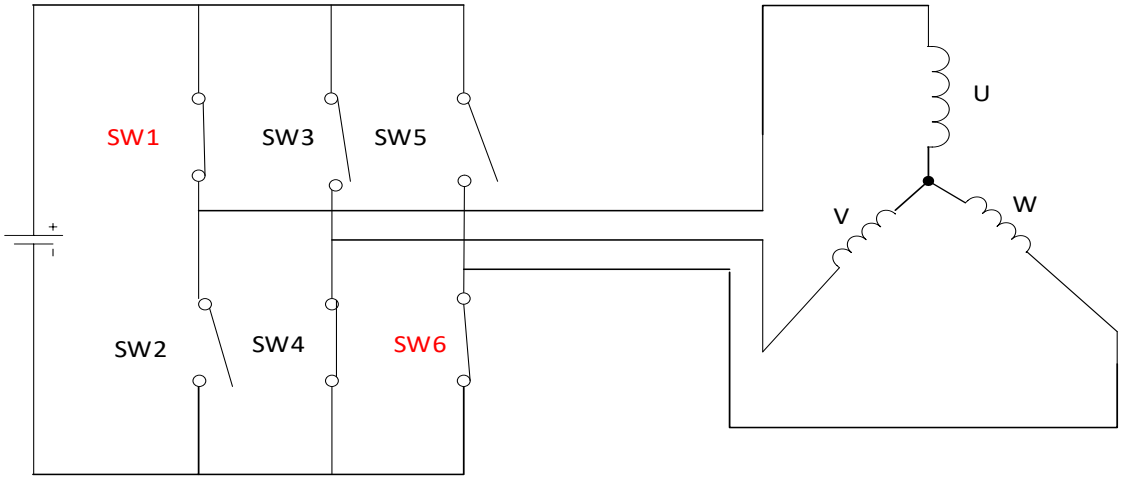
In a three-phase BLDC motor we need three Hall-effect sensors to detect the rotor position. Depending on the physical position of the Hall sensors, two types of output can be obtained: a phase variation of 60° and a phase variation of 120°. Once all the signals from the Hall Effect sensor have been combined, it is possible to determine the exact switching sequence.

The following figure 4.18 shows the switching sequence of a three-phase BLDC motor control circuit for counterclockwise rotation. The corridor sensors "a", "b" and "c" are positioned in the stator at 120° intervals, while the three-phase windings are star-shaped. For each 60° rotation, any room sensor changes its state as shown in Fig. 4.18; Six phases are necessary to complete a complete electrical cycle. In synchronous mode, the phase current switching is updated every 60°. At each step, a motor terminal moves upwards, another motor terminal is lowered, with the arrangement to keep the third winding in floating position. The separate controls of the units for the high and low regulators allow high, low and floating units in each motor terminal.

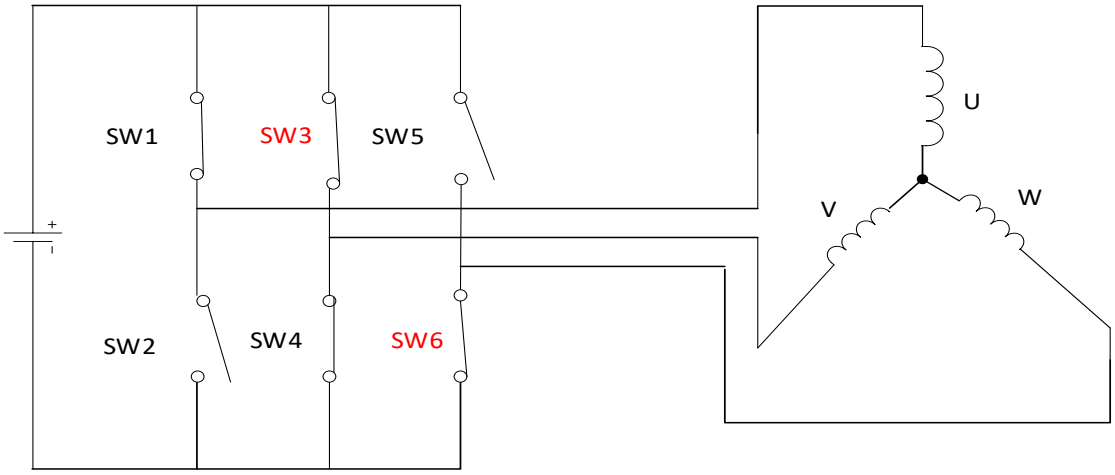
However, every single signal cycle may not be related to the completion of the entire mechanical revolution. The total number of signal cycles to complete a mechanical rotation is decided by the number of pole pairs of the rotor, each pair of rotor poles needs a signal cycle in a mechanical rotation. Therefore, the number of cycles of the signal is equal to the polar pairs of the rotor.



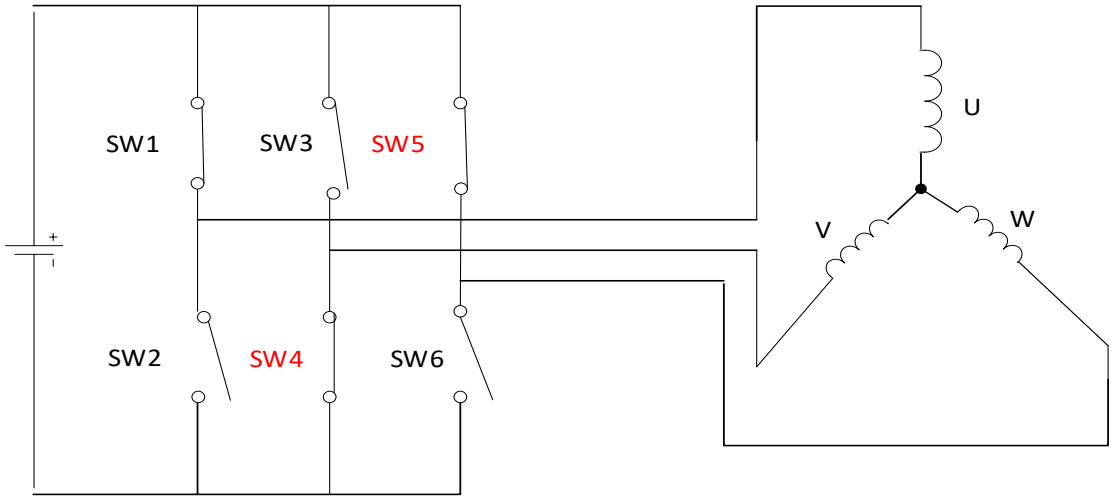
(a)


SW1
SW3
SW5
SW2
SW4
SW6
U
V
W

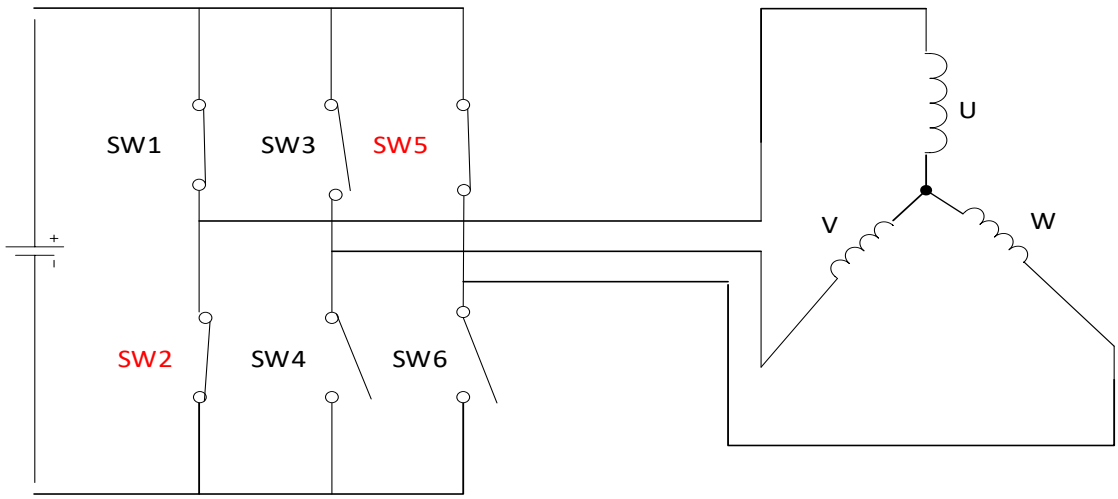
(b)


SW1
SW3
SW5
SW2
SW4
SW6
U
V
W

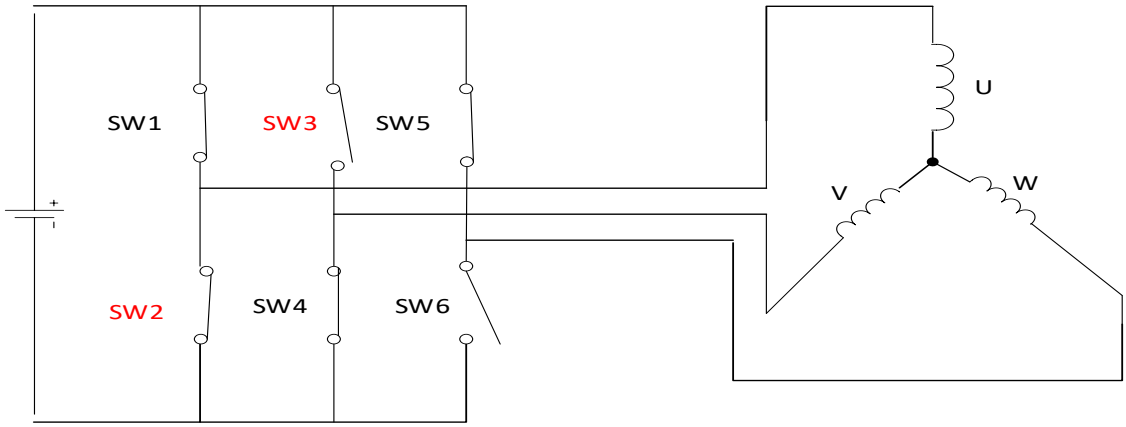
(C)


SW1
SW3
SW5
SW2
SW4
SW6
U
V
W

(d)



(e)



(f)

Fig. 4.17: Hall Sensor Position (a) 001 (b) 101(c) 100 (d) 110 (e) 010 (f) 011

Figure 4.18 shows the time diagrams in which the phase windings - U, V and W are excited or fluctuating, according to the signals a, b and c of the Hall sensor. One for example is a signal from the nearby sensor that has a 120° phase shift between them, where the motor rotates counterclockwise. Starting a Hall signal with a phase change of 60° or rotation of the motor in a clockwise direction requires a different time sequence. To modify the rotation speed, the amplitude modulation signals based on space vectors on the switches at a frequency much higher than the motor rotation frequency, mainly, the SV-PWM frequency must be at least 10 times higher than the maximum frequency of motor rotation. Another advantage of the SV-PWM technique is that if the voltage of the DC bus is much higher than the nominal voltage of the motor, limiting the duty cycle of the PWM signal to satisfy the rated voltage of the motor dominates the motor.

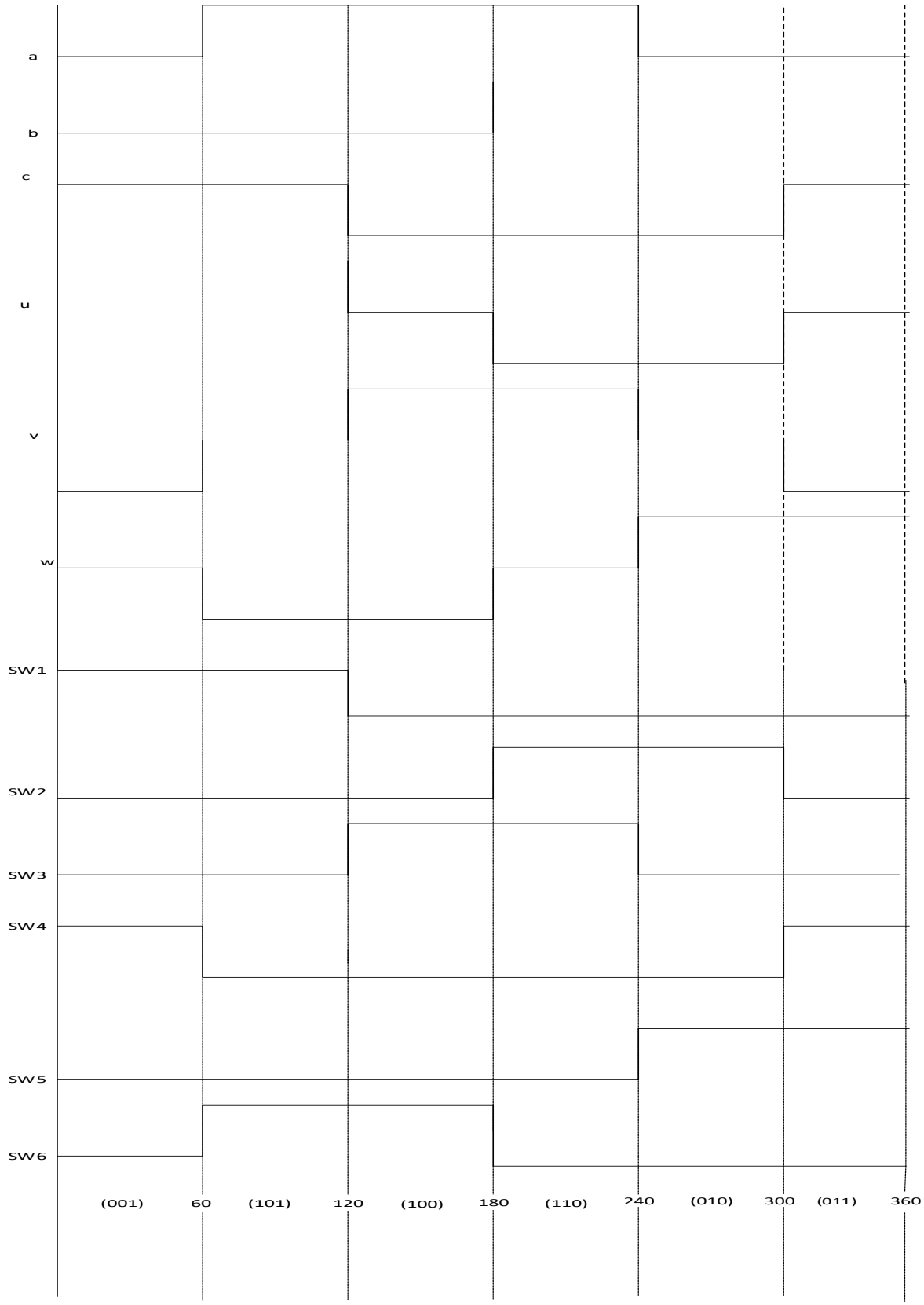


Fig. 4.18 Three-Phase BLDC Motor sensor vs drive timing

CHAPTER 5

PROTOTYPE and SIMULATION RESULTS

5.1 POWER FACTOR CORRECTION (PFC)

The circuit contains some important elements, the power factor correction circuit, fly back (isolated DC-DC conversion), space vector pulse width modulation and the brushless DC motor (BLDC). The design calculations for all subsequent stages have been discussed and mentioned in chapter -3. The following waveform, Fig. 5.1, indicates the voltage and current of an AC-DC converter without the power factor correction technique.

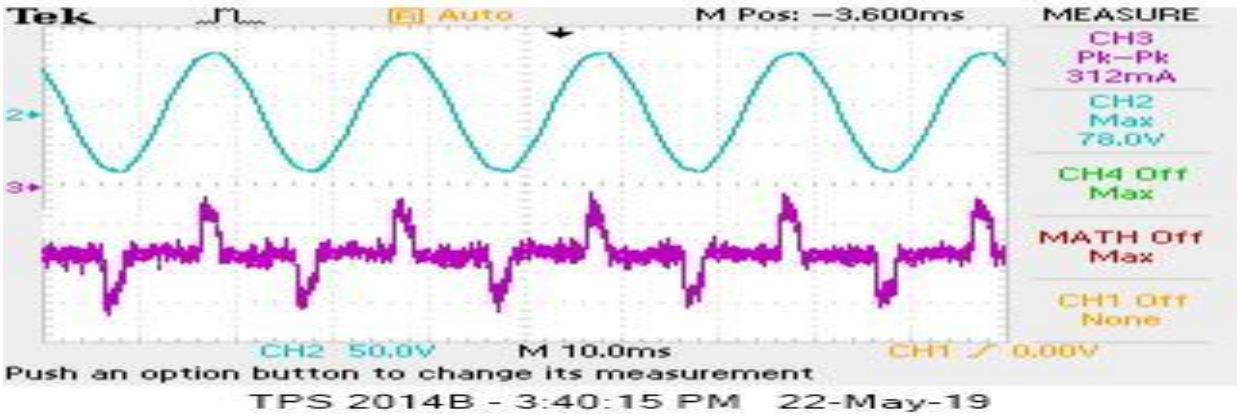
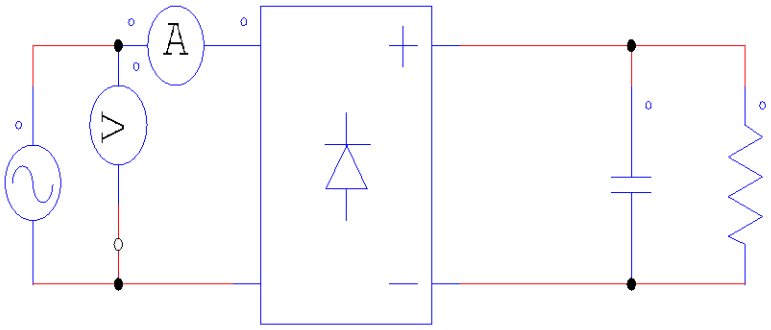
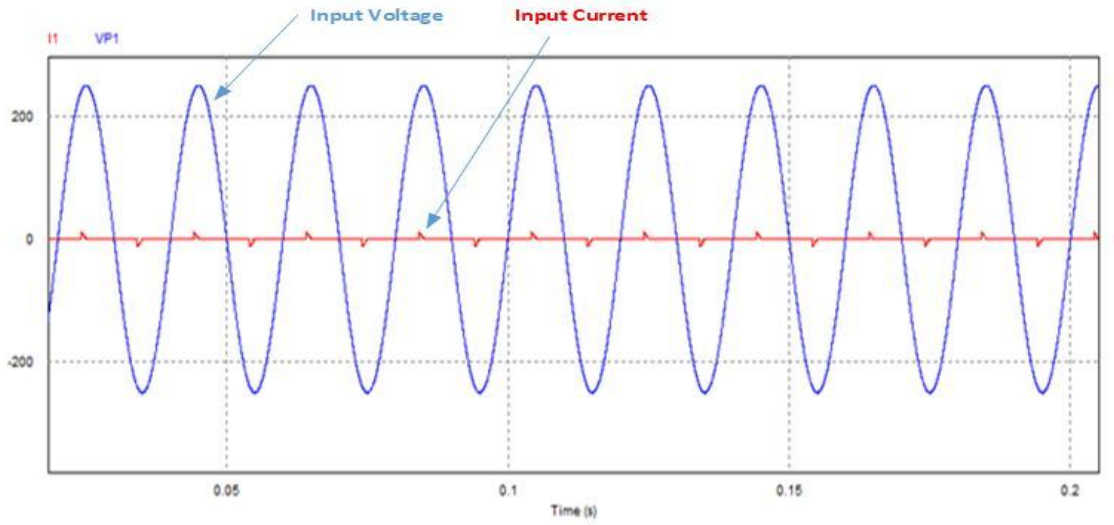


Fig. 5.1: current and voltage input waveform of the AC-DC converter without PFC



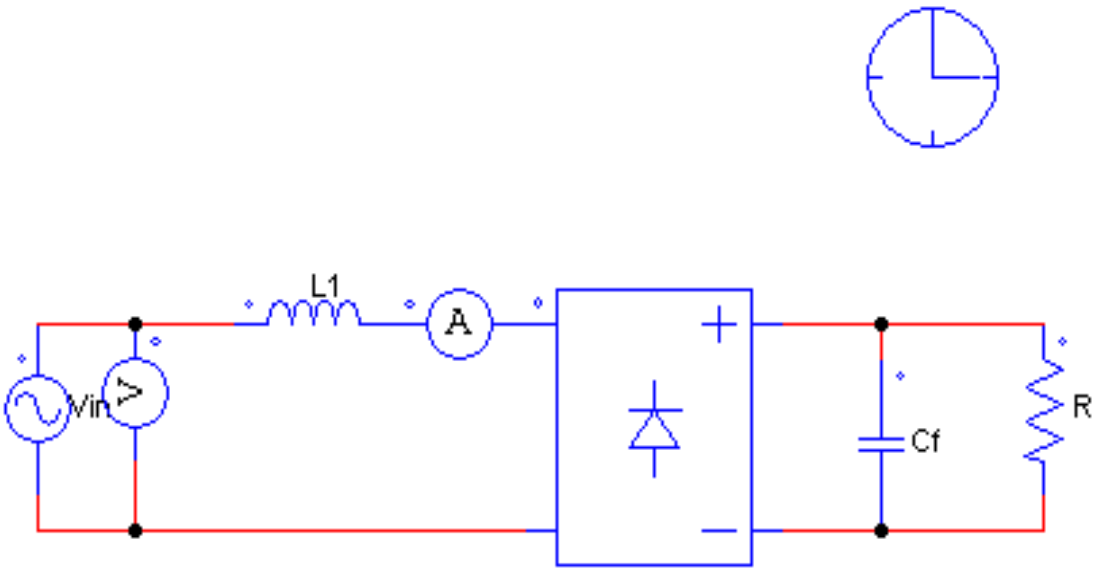
(a)



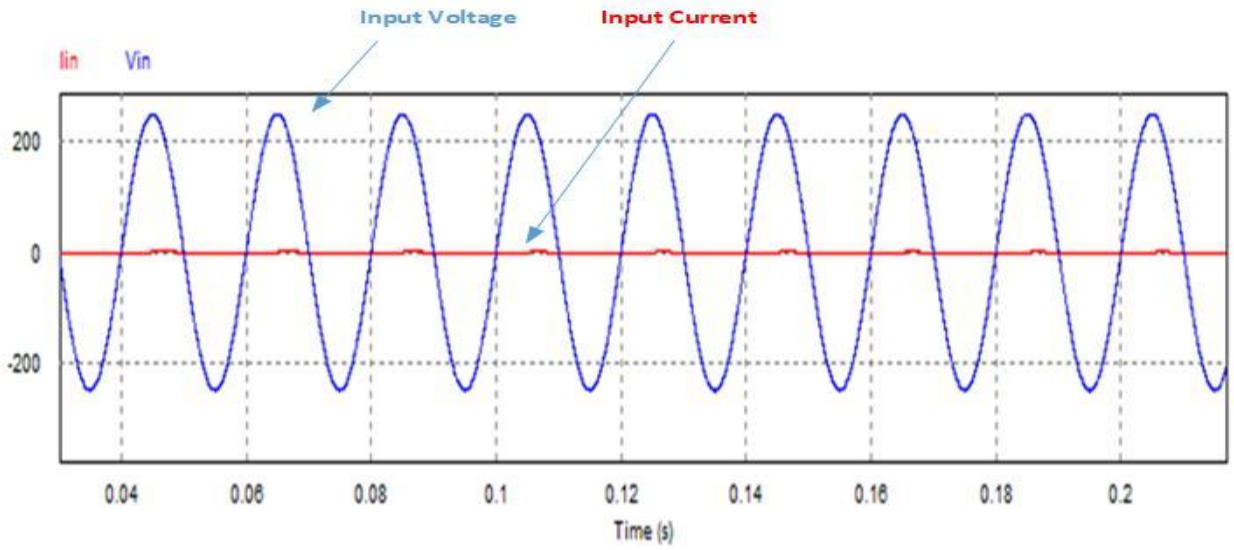
(b)

Fig. 5.2: Bridge Rectifier (without PFC) Simulation (a) Schematic (b) Input Line Voltage and Current with V_{in} = 220 V, R = 500 Ω and C_f = 470 µF

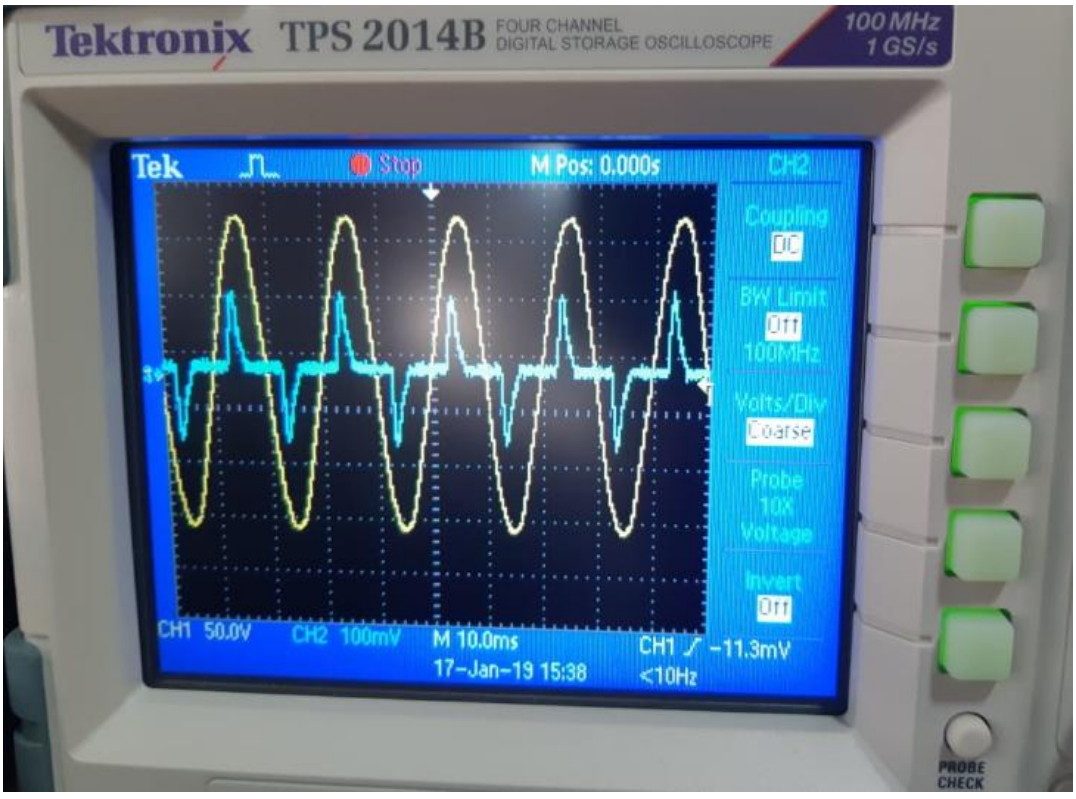
The below Figure 5.3 clearly indicates the requirement of another promising technique for power factor correction. The input power factor is found to be close to 0.5.



(a)

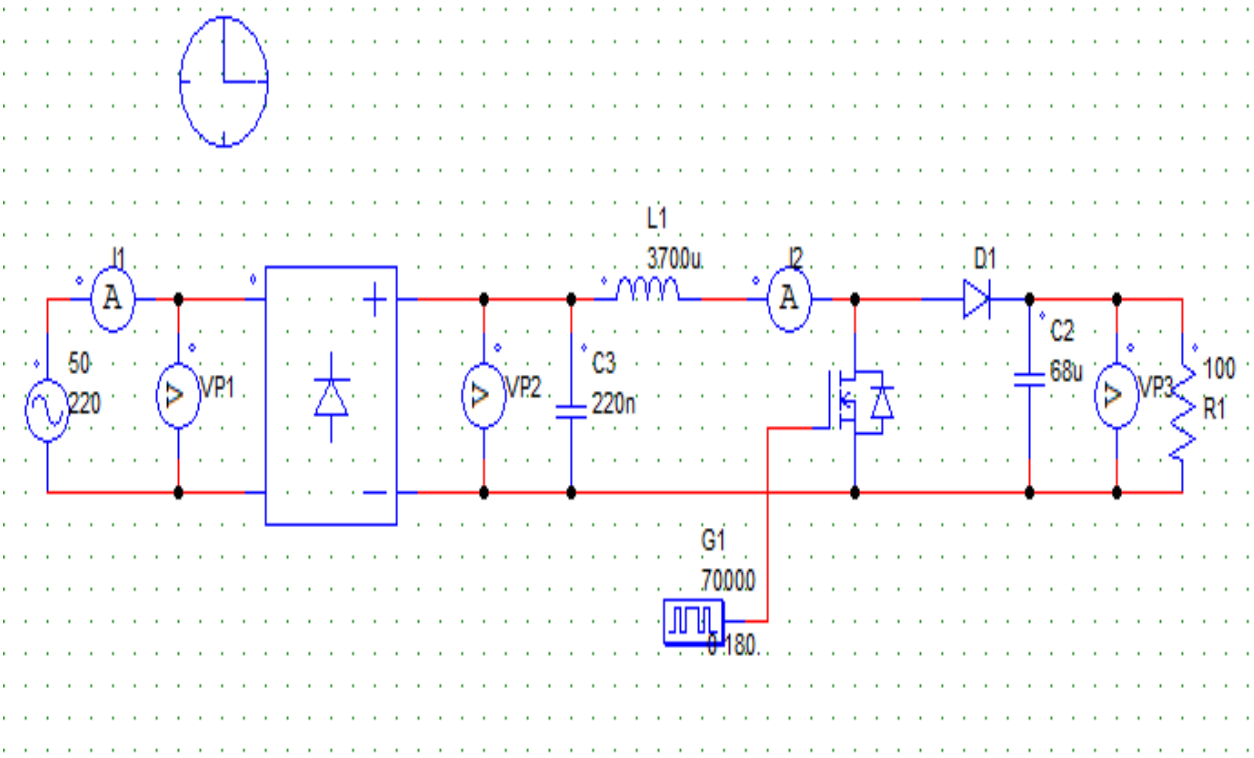


(b)

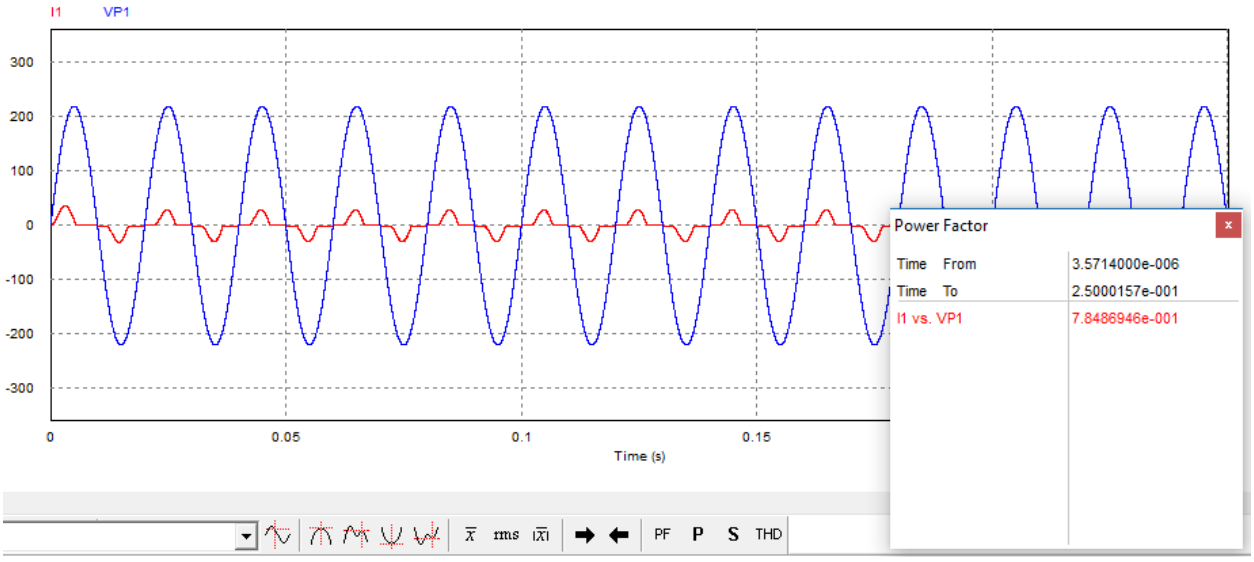


(c)

Fig. 5.3: Bridge Rectifier (with inductor filter) Simulation(a) Schematic (b) Input Line Voltage and Current with V_{in} = 220 V,L_1 = 130mH, R = 500 Ω and C_f = 470 µF(c) Passive PFC (Hardware) Result



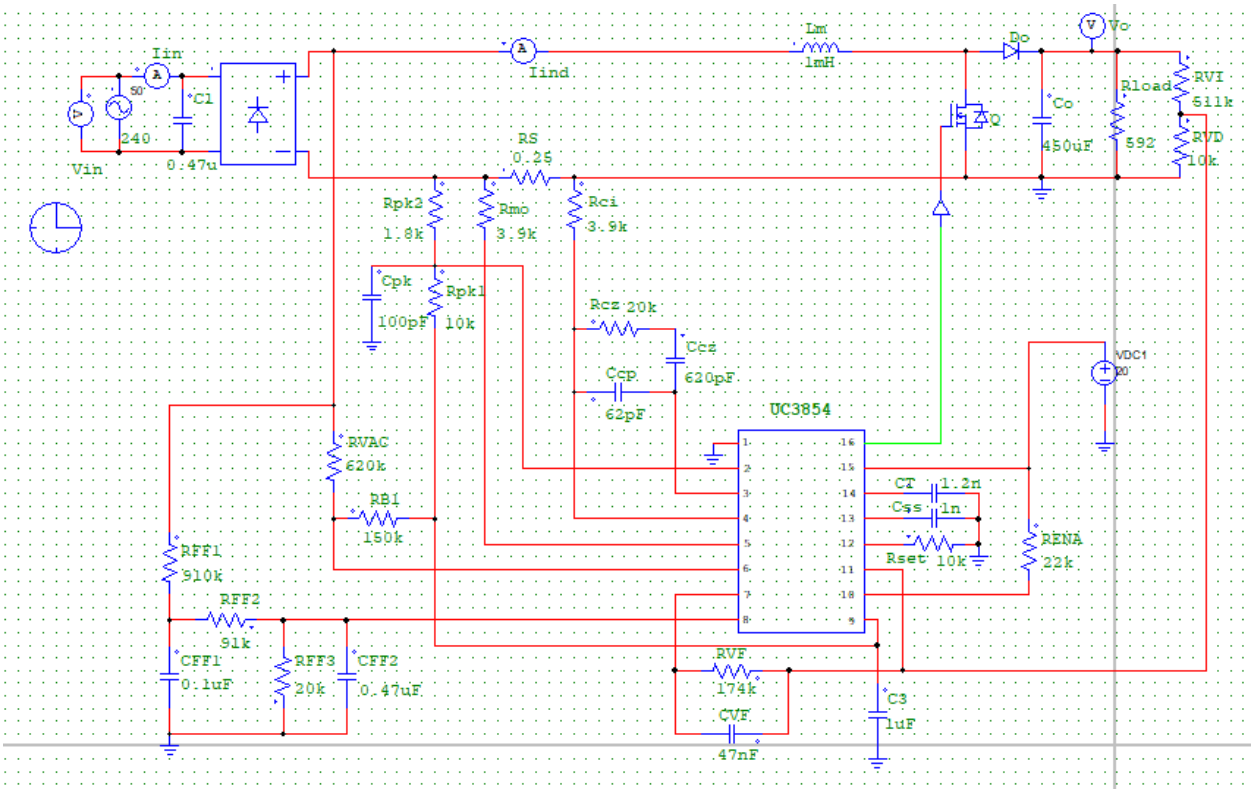
(a)



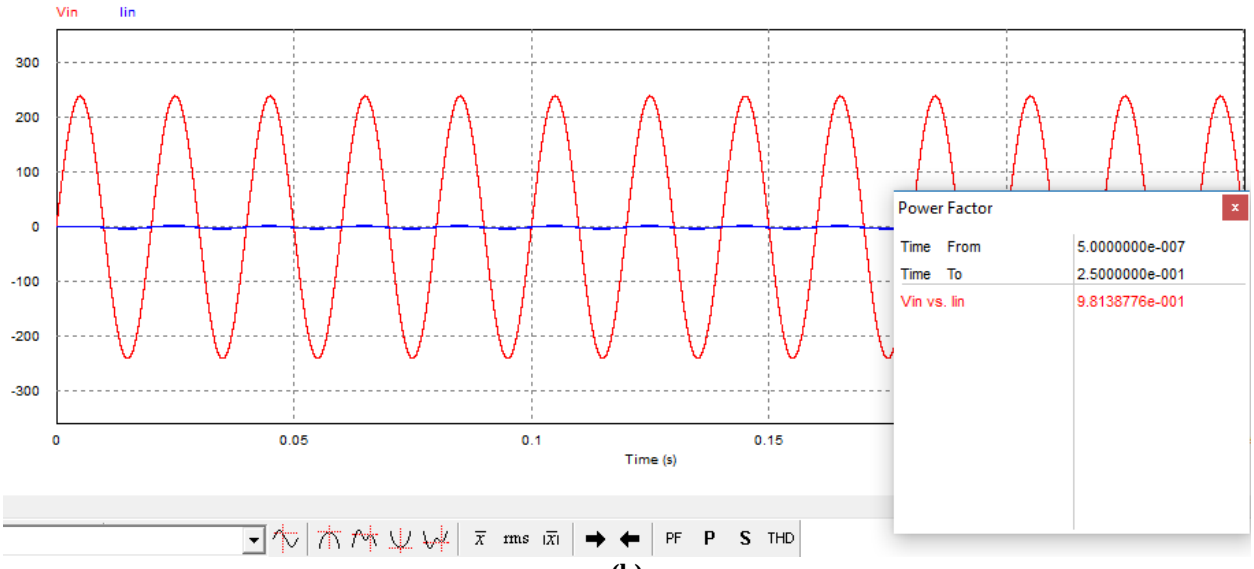
(b)

Fig. 5.4: Bridge Rectifier (with inductor filter) Simulation Active PFC without UC 3854 (a) Schematic (b) Input Line Voltage and Current

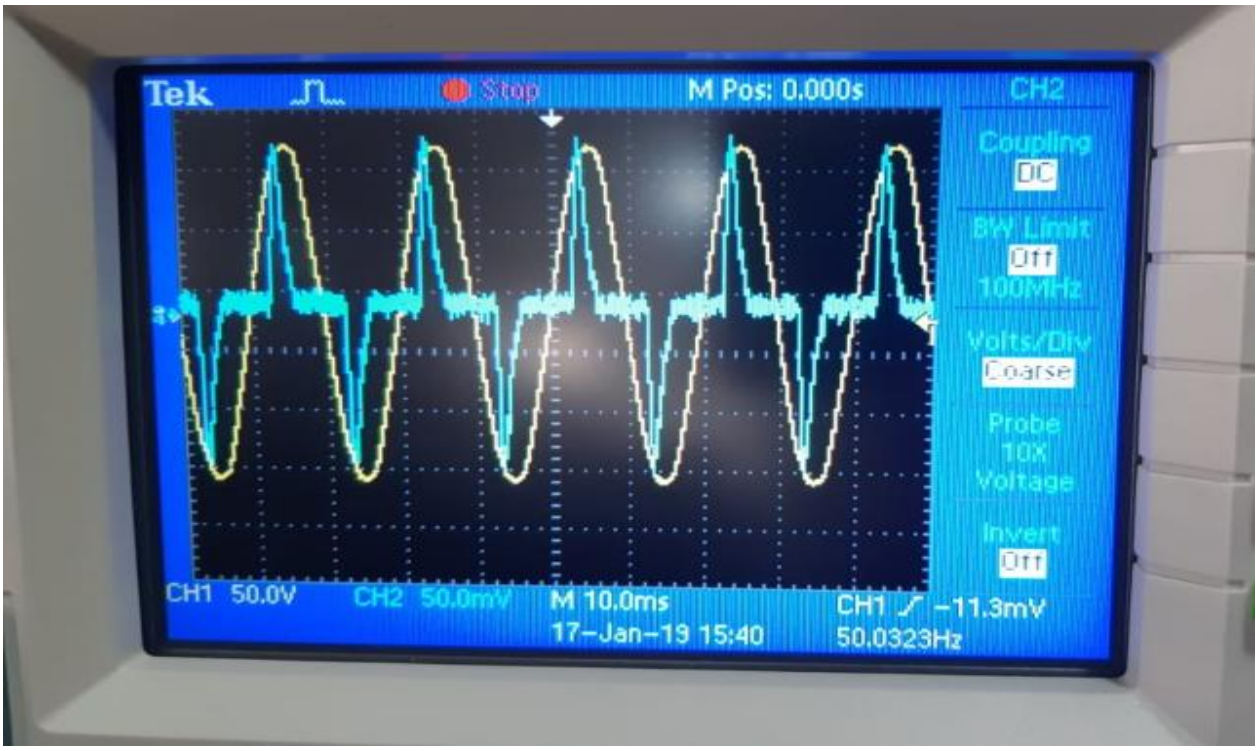
The above Figure 5.4 indicates the implementation of active power factor correction technique without the requirement of UC 3854 i.e. biasing circuit. So, the results shown have some improvement in the input power factor. Input power factor is 0.784. It can be further improved using suitable power factor correction technique.



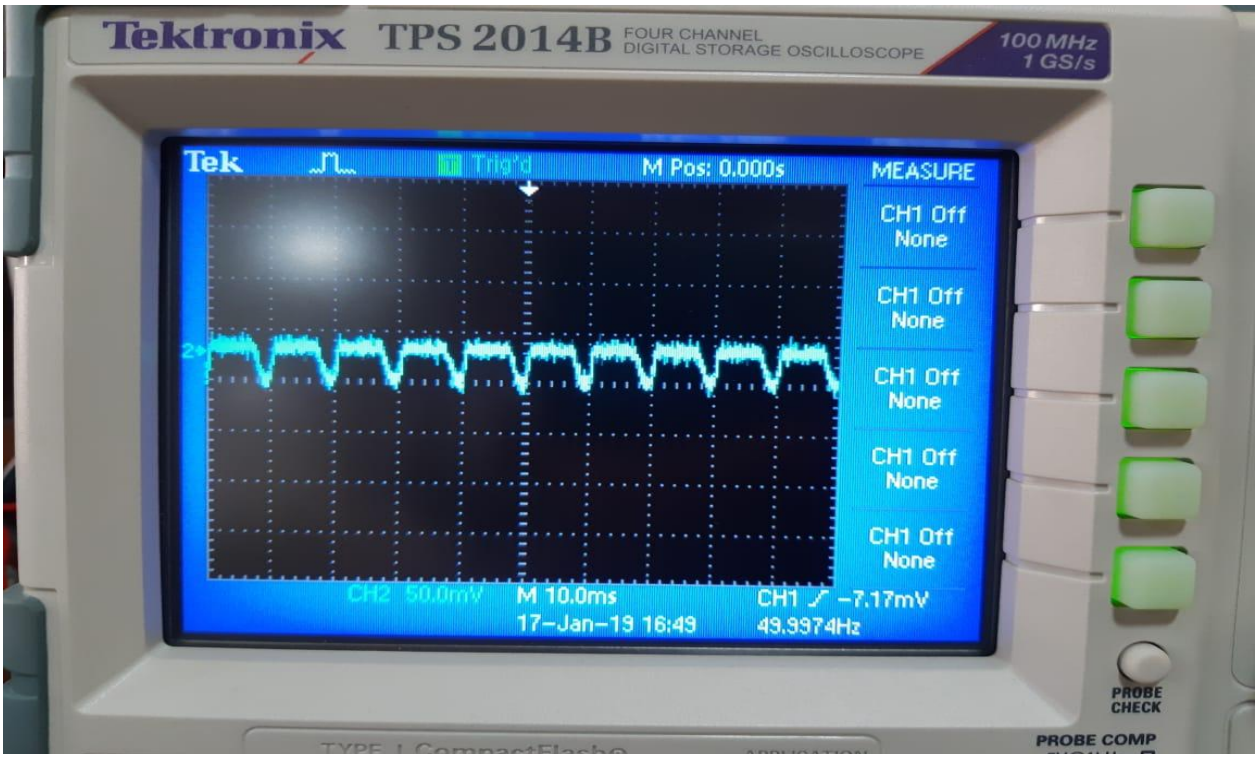
(a)



(b)



(c)



(d)

Fig. 5.5: Bridge Rectifier (with inductor filter) Simulation ACTIVE PFC with UC 3854 (a) Schematic (b) Input Line Voltage and Current (c) Active PFC (Hardware) Result (d) Inductor Current

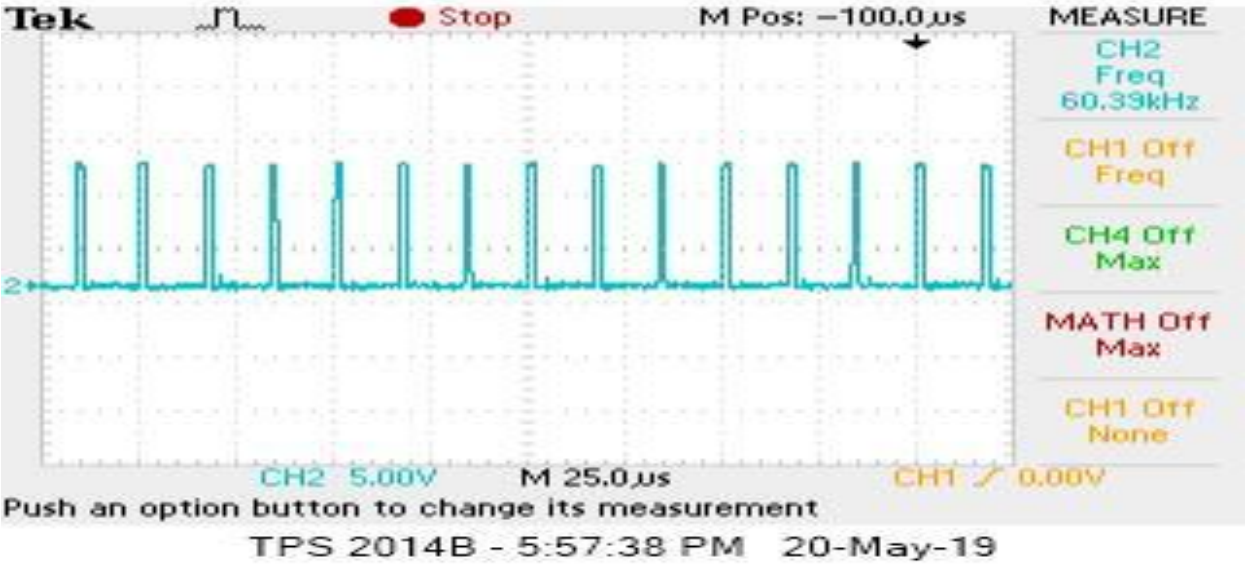


Fig. 5.6: PFC MOSFET (PWM Pulse)

The above Figure 5.6, the pulse generated from the switch *i.e.* MOSFET connected in the PFC circuit. It is variable quantity based on the input supply. The switching frequency was designed for 60 kHz. Also, it is shown in Fig. 5.7 the magnitude of output voltage at the other end of flybackconverter.

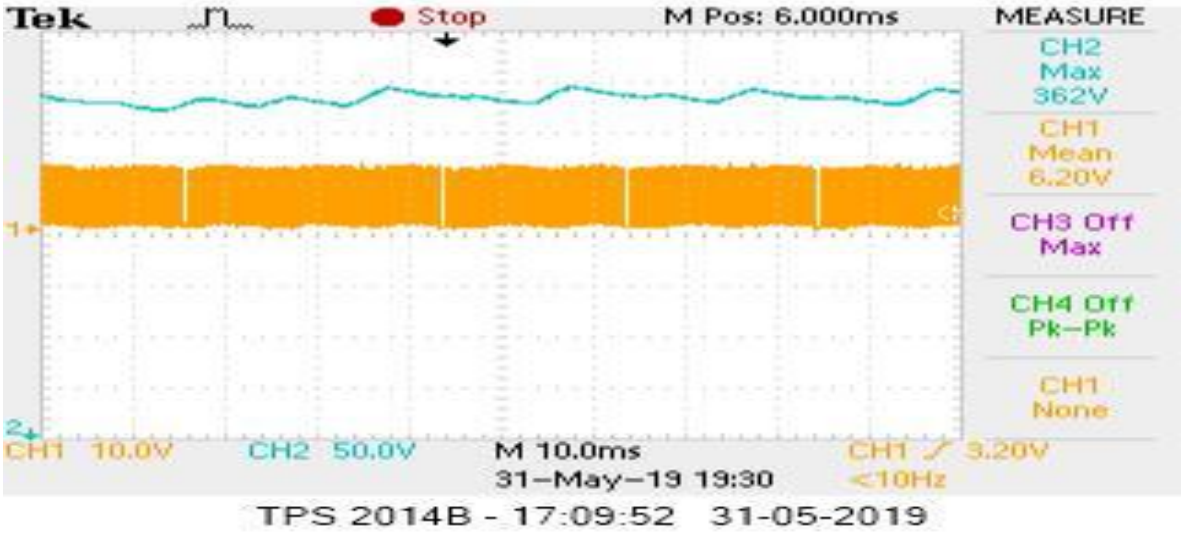
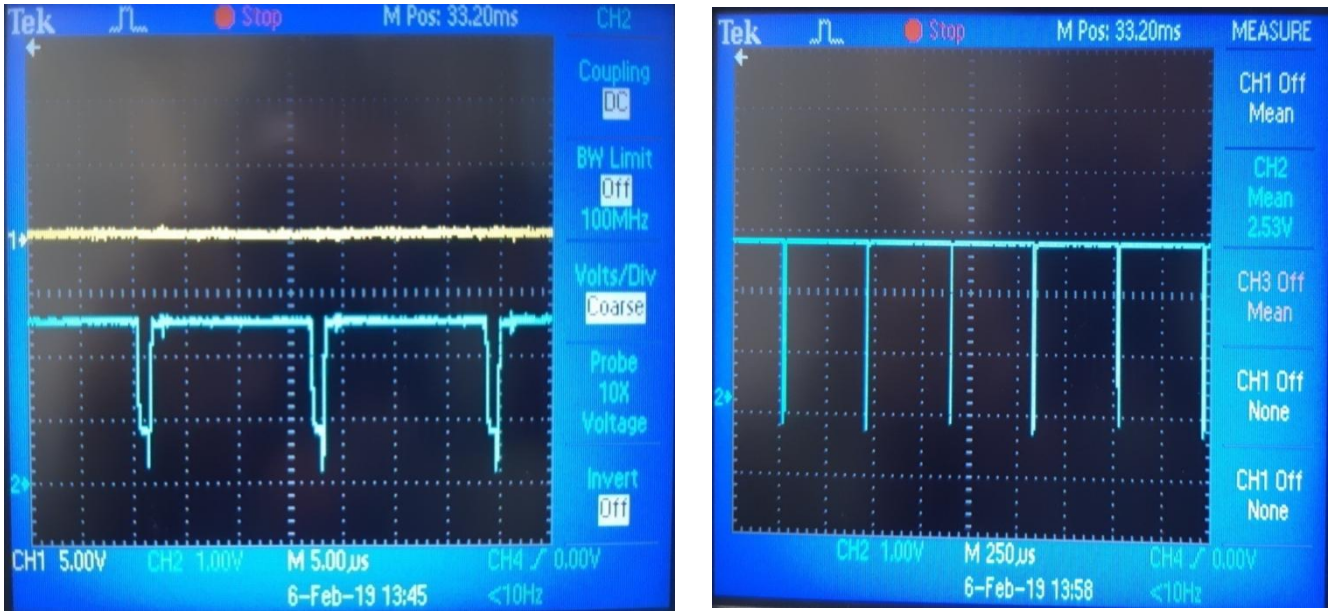


Fig. 5.7: PFC OUTPUT (Loaded Condition)

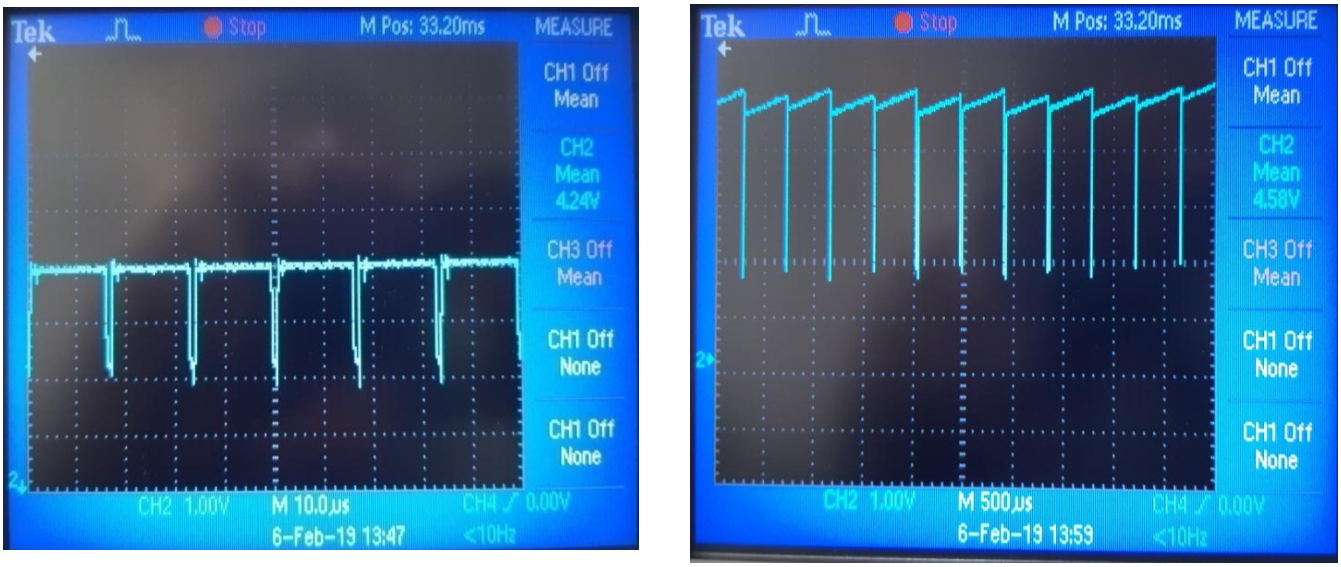
5.2 L4984D BIASING CIRCUIT

PFC based microcontroller associated circuitry is designed and waveform across different pins are analyzed. Typical waveforms Fig. (5.8) – (5.13) are given below of each pin in the open loop as well as loaded conditions.



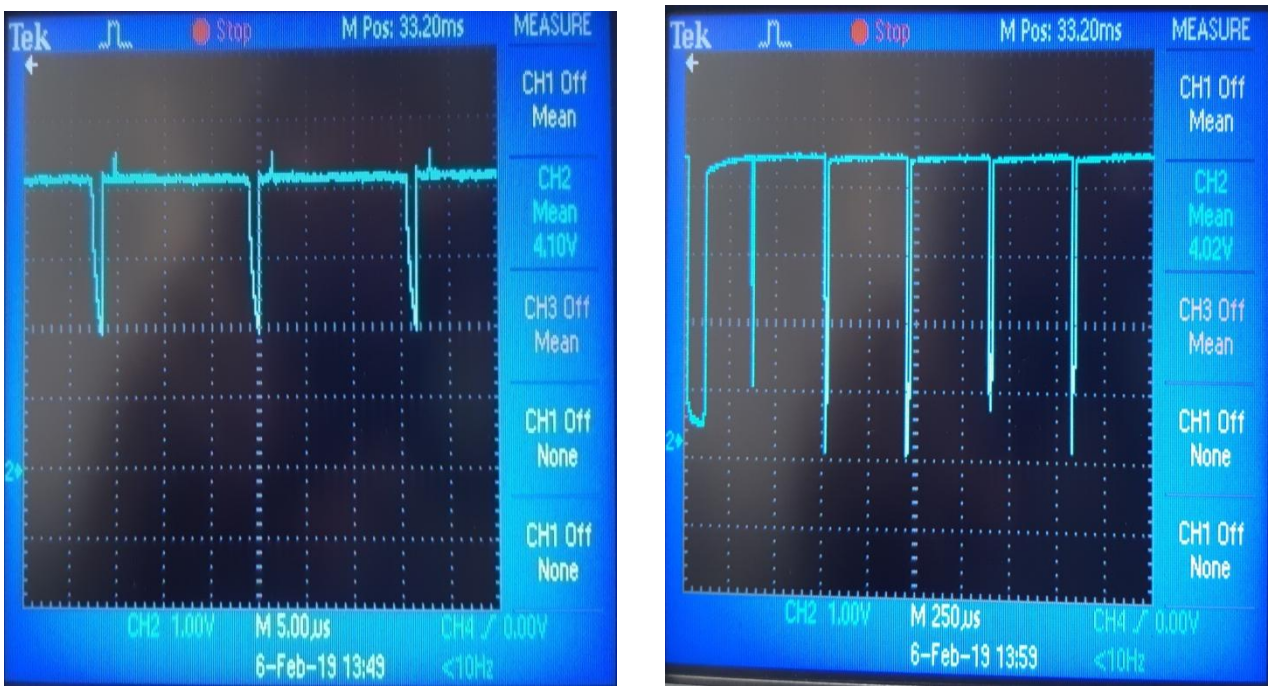
(a) **(b)**

Fig. 5.8: INV pin waveform (a) loaded condition (b) no load condition



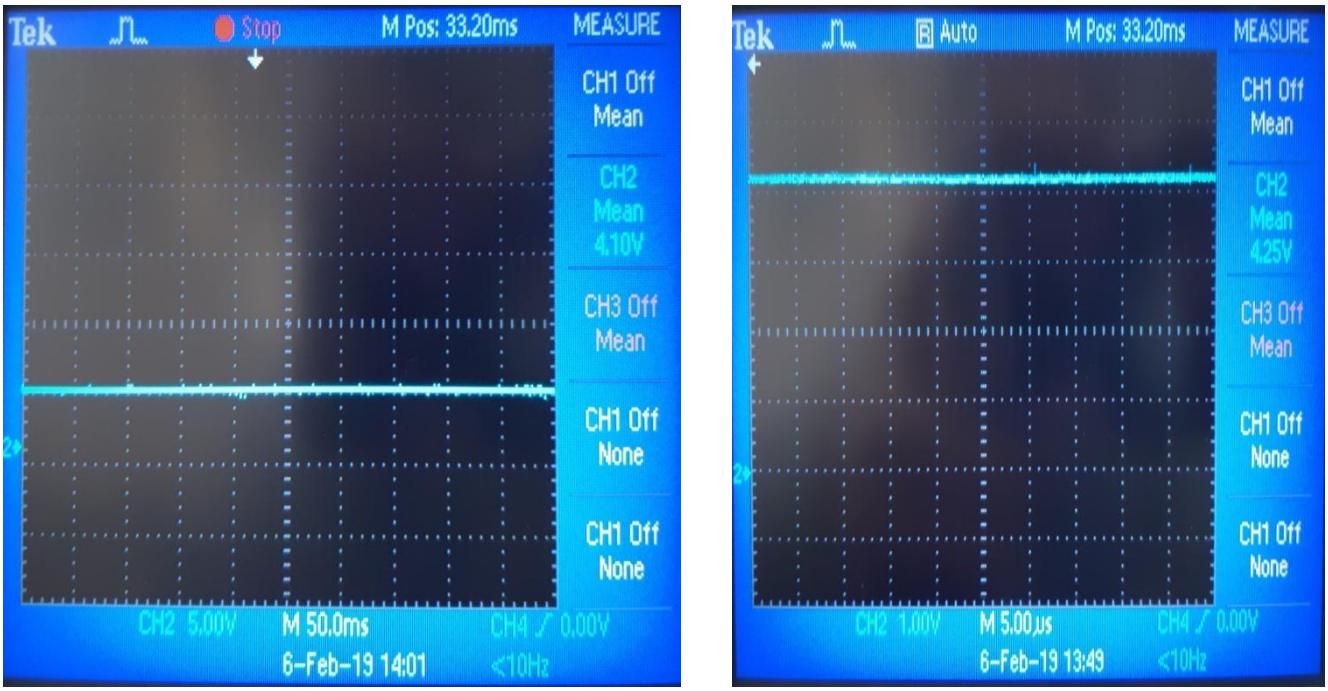
(a) **(b)**

Fig. 5.9: COMP pin waveform (a) loaded condition (b)no load condition



(a) **(b)**

Fig. 5.10: MULT Pin waveform (a) loaded condition(b) no load condition



(a) **(b)**

Fig. 5.11: V_{FF} Pin waveform (a) loaded condition (b) no load condition

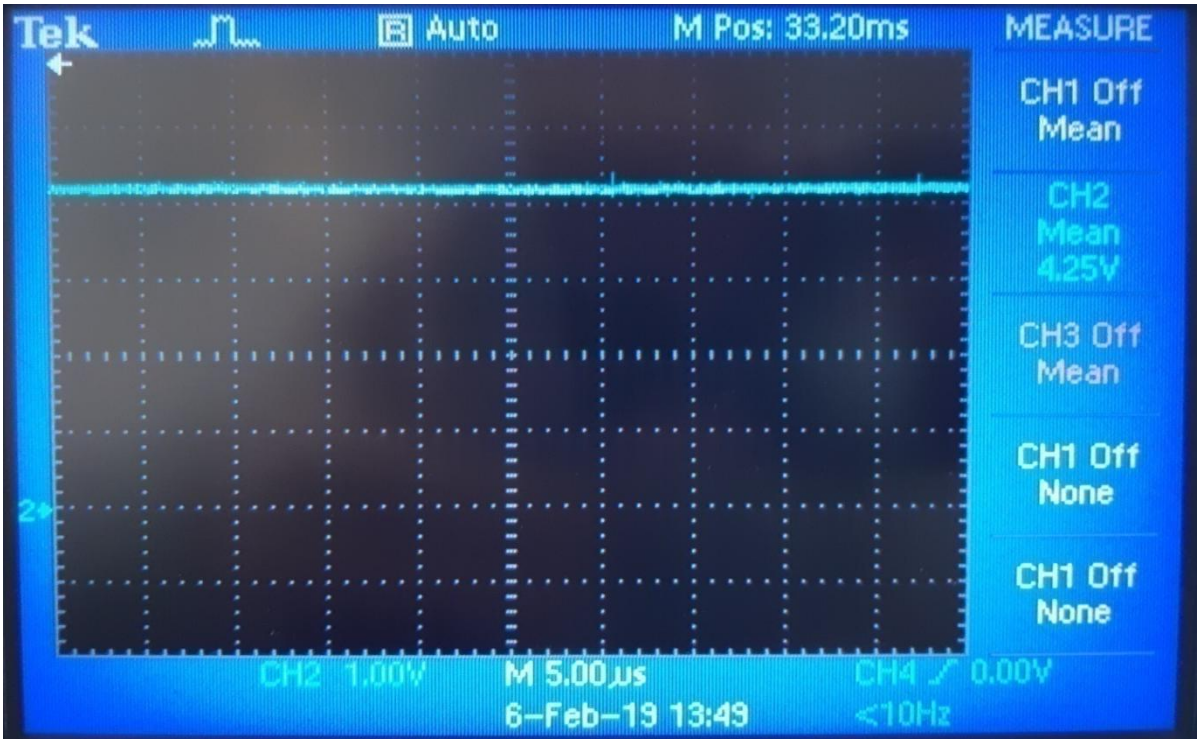


Fig. 5.12: PFC_OK Pin waveform (loaded condition)

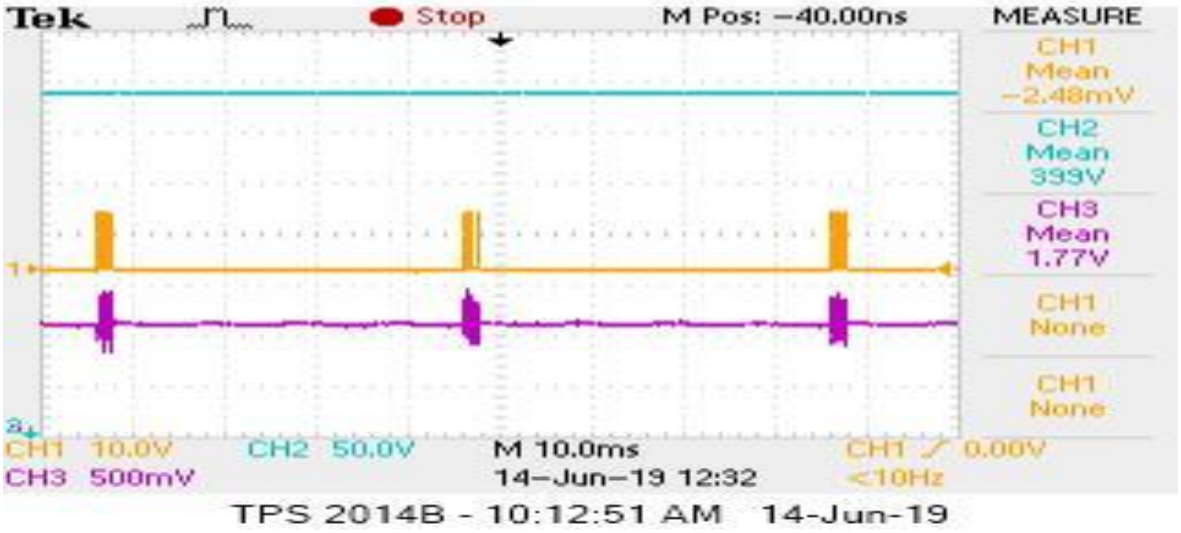


Fig. 5.13: L4984D IC (Burst Mode)

The Figure 5.13 represents the switching pulses in burst mode. In this mode the input voltage is high and corresponding boosting of output DC link voltage requirement is very low.

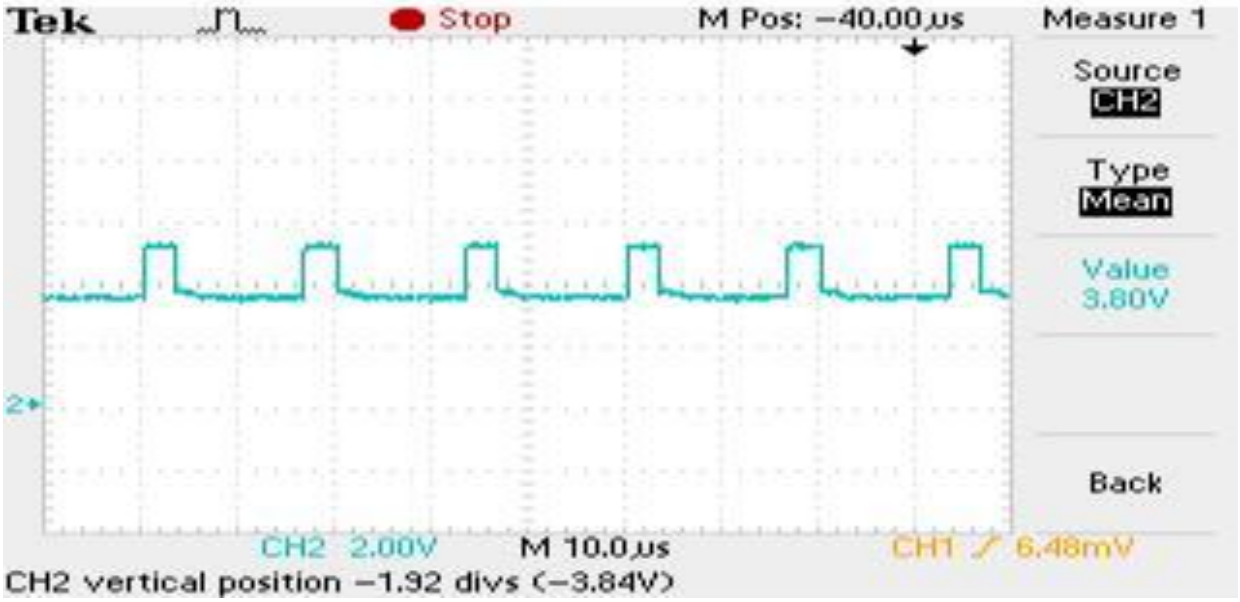


Fig. 5.14: STM32FO70RB PWM Pulse

The Figure 5.14 represents the switching pulses generated from STM32F070RB microcontroller. These pulses are fed to switch associated with Fly-back Transformer primary. The corresponding switching frequency is 60 kHz. The duty cycle is variable based on the requirement of secondary output voltage.

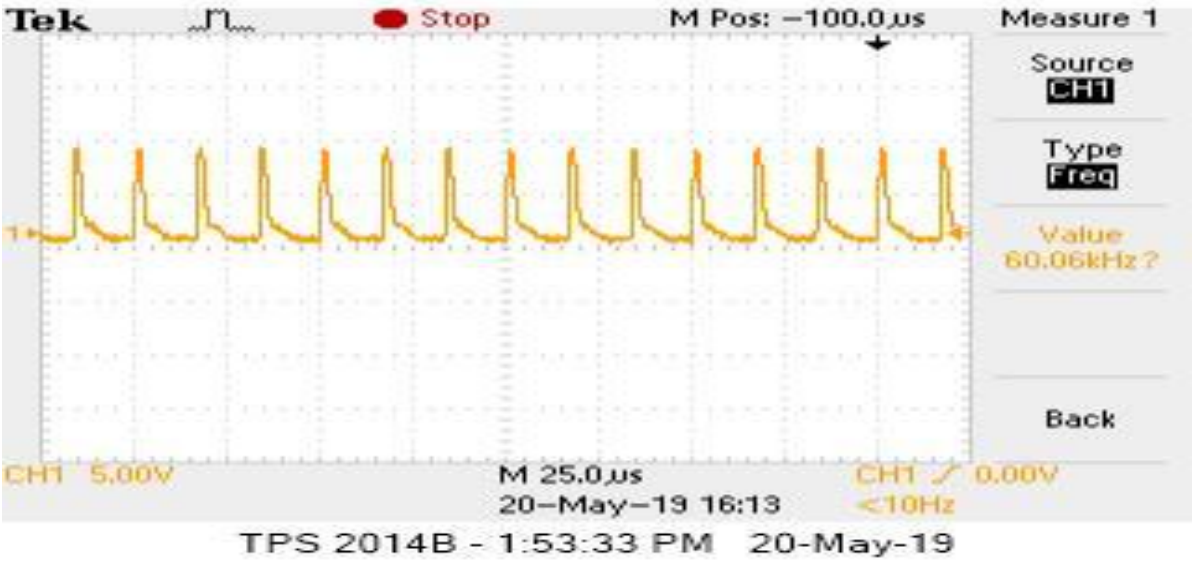


Fig. 5.15: Driver Circuit PWM Pulse

The strength of the PWM pulses generated from the STM microcontroller is very low, not enough to drive the Fly-back MOSFET. So, a driver circuit is developed to meet the requirement. Fig 5.15 represents the boosted switching pulses to drive the fly-back MOSFET.

5.3 FLY BACK CONVERTER

A fly-back converter is simulated in PSIM environment. RC clamping is used to suppress the voltage spike. In Fig 5.16 it shows the schematic of the fly back converter. Fig 5.17 shows the ripple free stepped down dc output voltage. This voltage is the input of a BLDC motor controller without PFC.

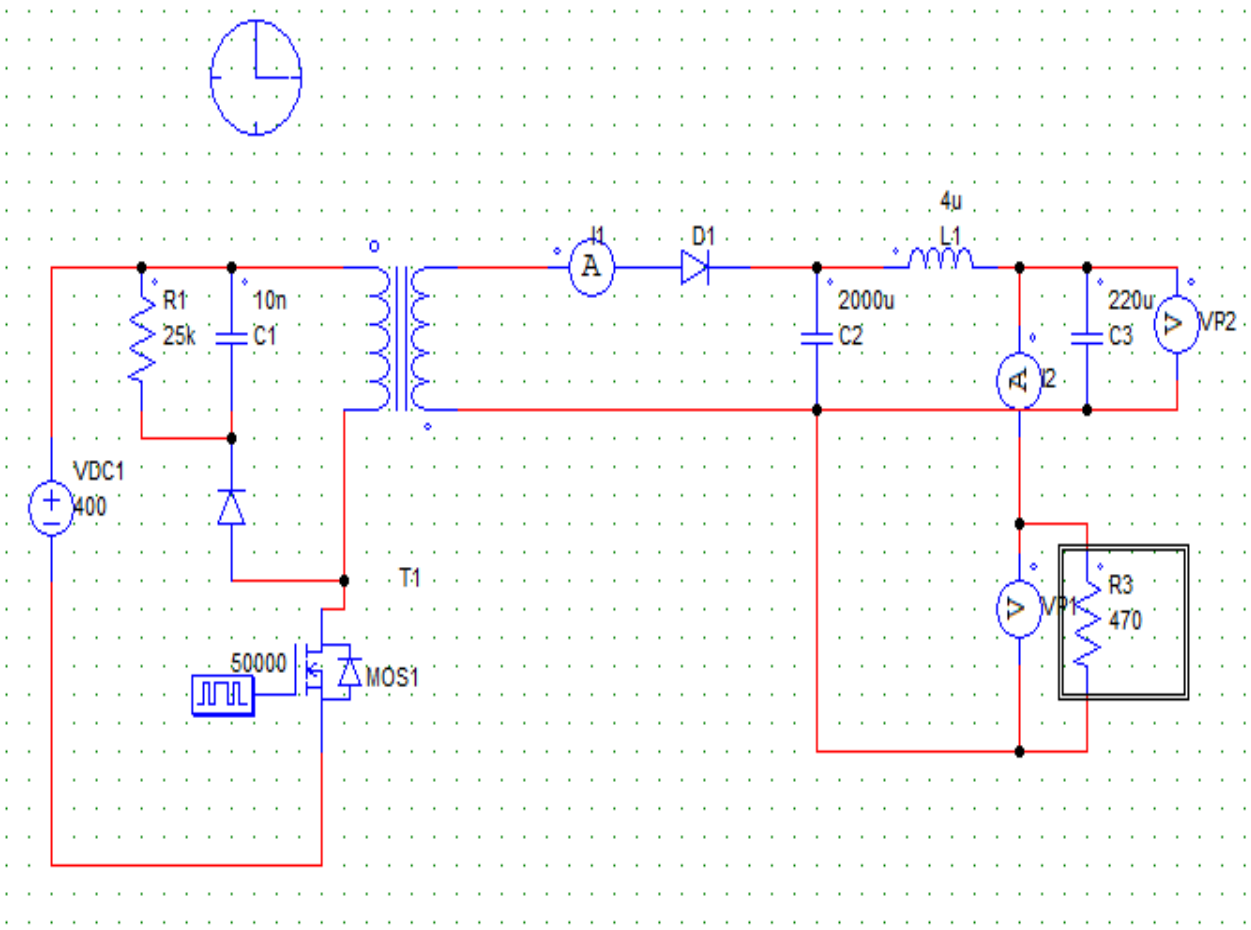


Fig. 5.16: Fly Back Converter Layout

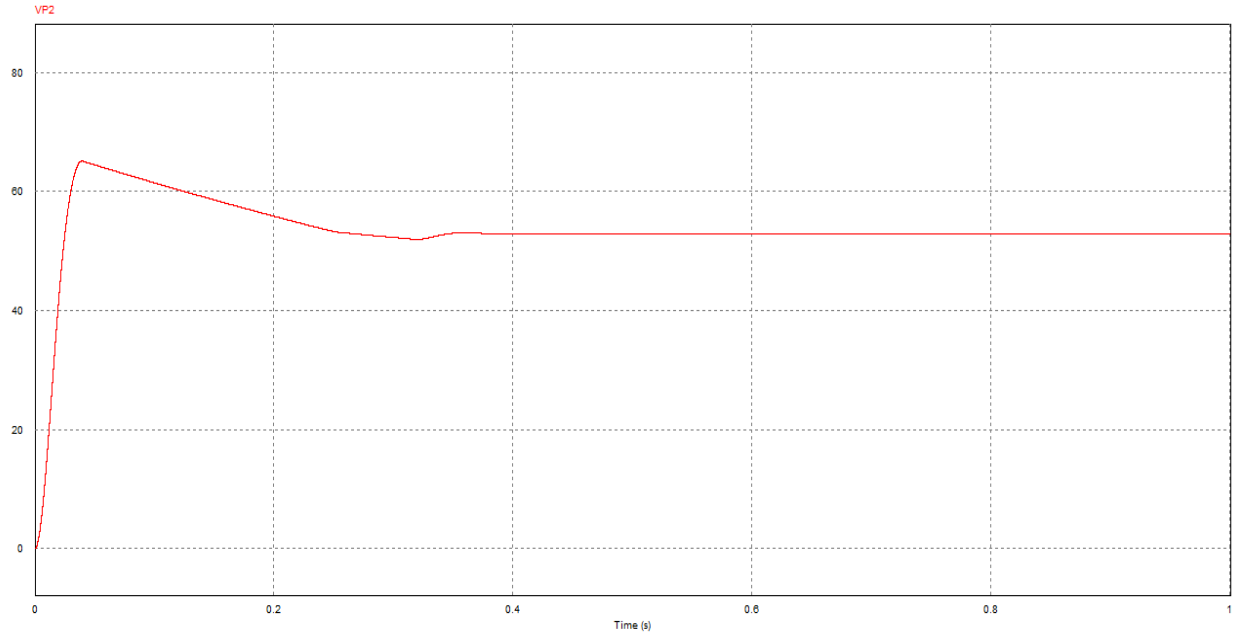


Fig. 5.17: Fly Back Converter Output

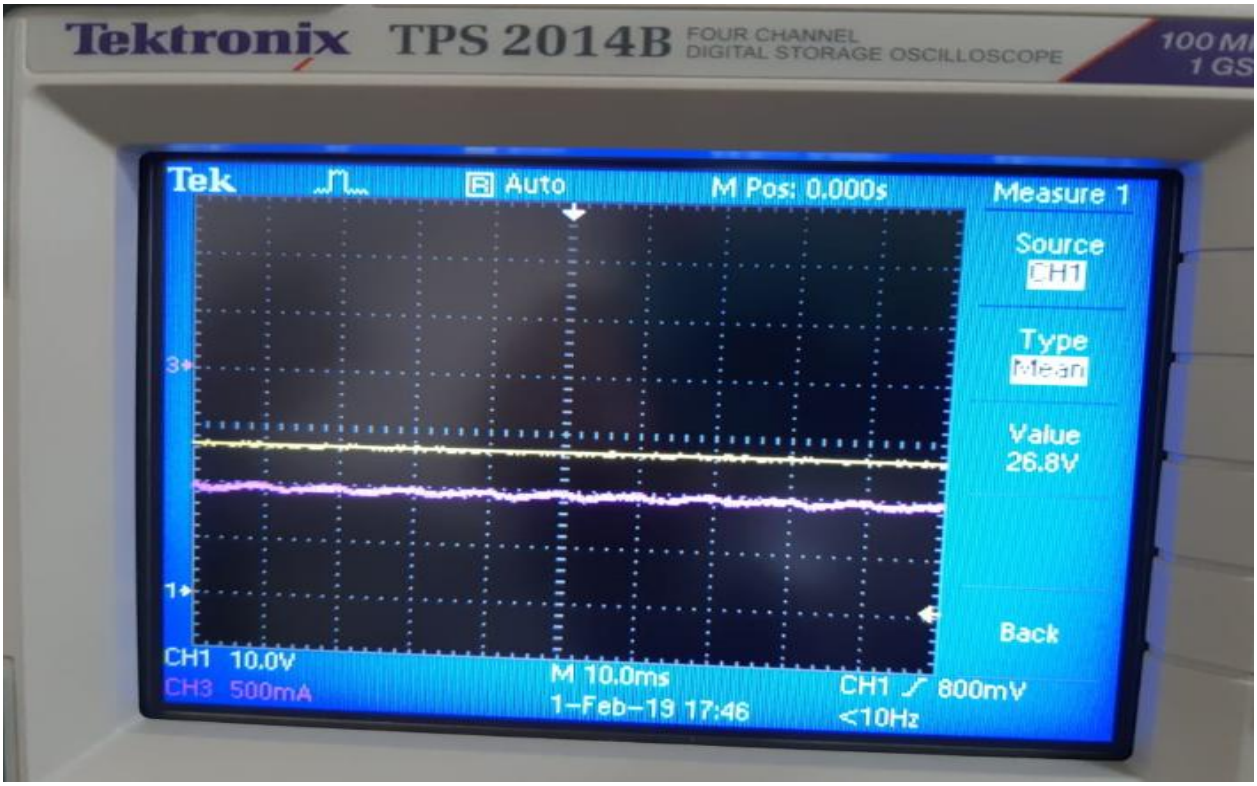


Fig. 5.18: Fly Back Converter (Prototype) Output

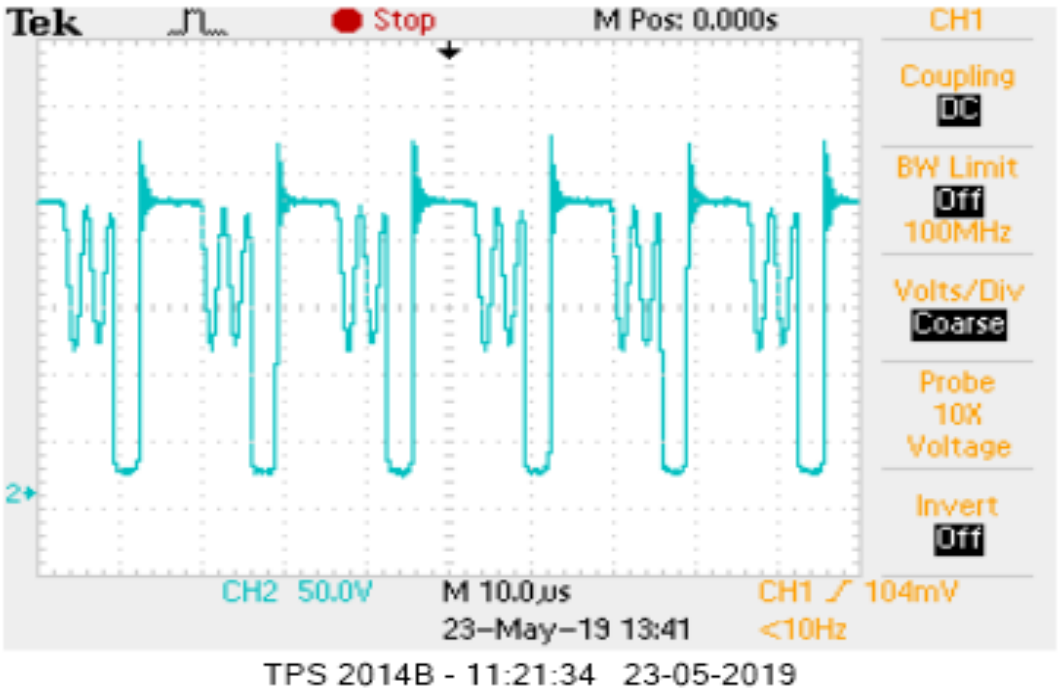


Fig. 5.19:V_{DS} (Drain-Source Voltage) Fly Back MOSFET

The Fig. 5.19 shows the drain-source voltage across the Fly back MOSFET. This drain-source voltage helps in analyzing the level of voltage stress across the switch.

5.4 SPACE VECTOR PULSE WIDTH MODULATION

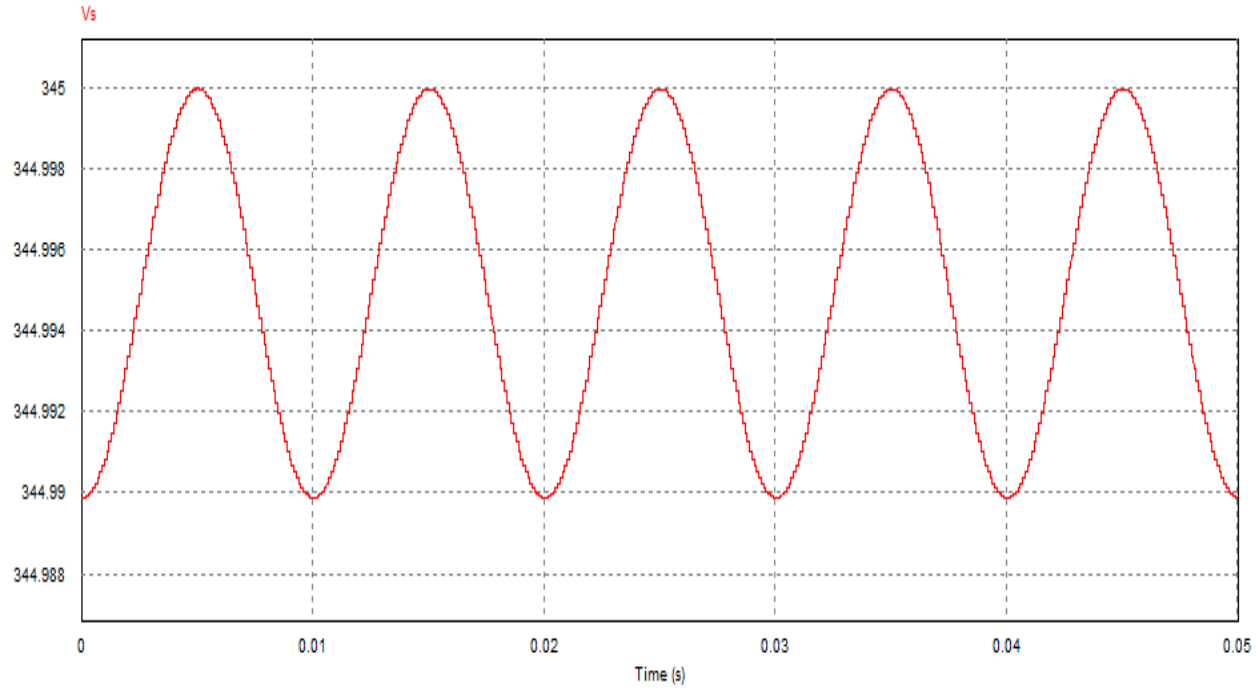


Fig. 5.20: Voltage Space Vector

Table 5.1: SWITCHING SEQUENCE (0-1-2-0-2-1-0) Sector – 1

Sector 1	S1	S2	S3	S4	S5	S6	
T0/2	0	1	0	1	0	1	1 sample
T1	1	1	0	0	0	1	3 Switching
T2	1	1	1	0	0	0	THD=76%
T0/2	1	0	1	0	1	0	CMV=226

Table 5.2: SWITCHING SEQUENCE (0-1-2-0-2-1-0) Sector – 2

Sector 1	S1	S2	S3	S4	S5	S6	
T0/2	1	0	1	0	1	0	1 sample
T1	1	1	1	0	0	0	3 Switching
T2	0	1	1	1	0	0	THD=76%
T0/2	0	1	0	1	0	1	CMV=226

The Fig. 5.20 & 5.22 represents the magnitude and phase difference of the voltage space vector. The magnitude of phase difference is always measured from the start of the sector. The time required to trace the active space vector (T_1&T_2) and zero state space vector (T_0) in every sector.

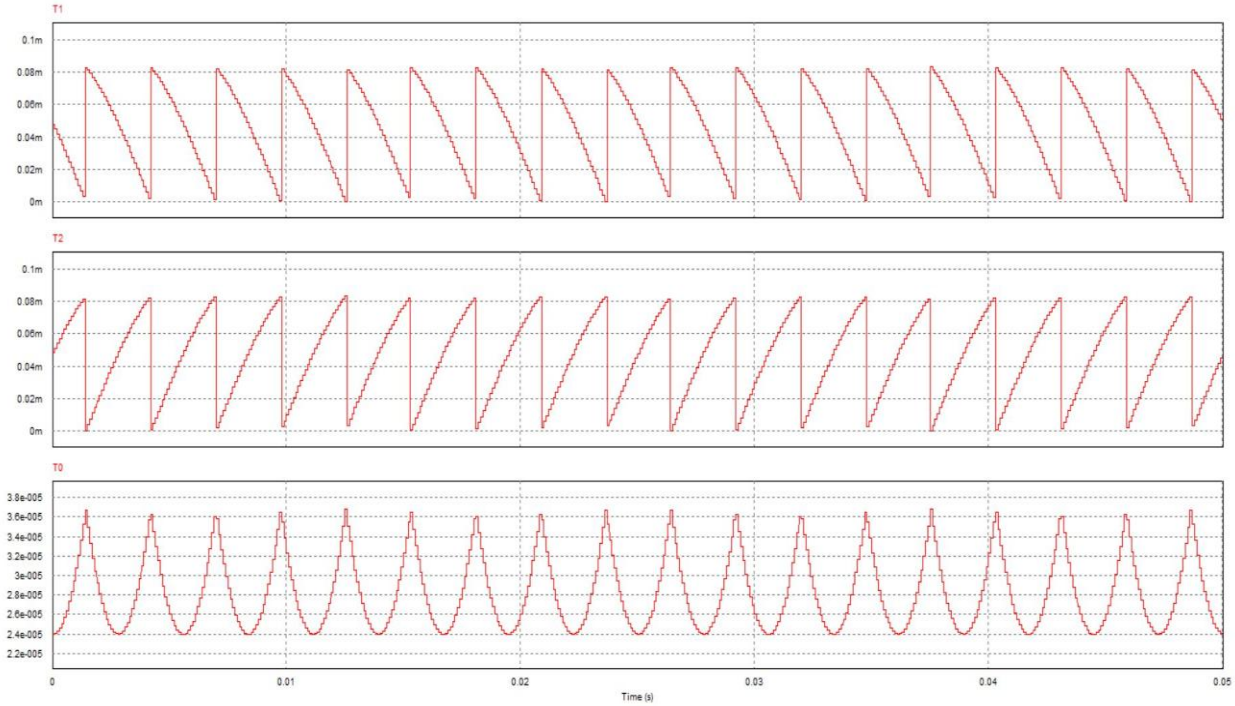


Fig. 5.21: Active (T_1&T_2) and Zero (T_0) State Vector Timing Sequence

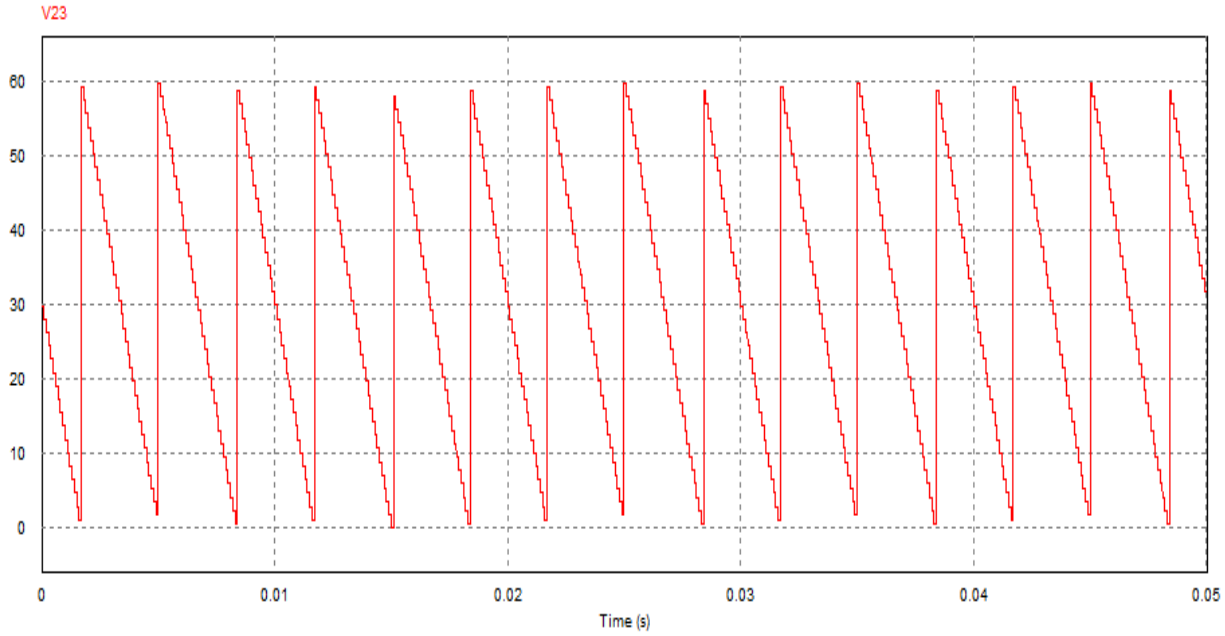


Fig. 5.22: Variation of α angle

For switching sequence (0-1-2-0-2-1-0) the selection of sector for movement of voltage space vector is shown in Fig. 5.23

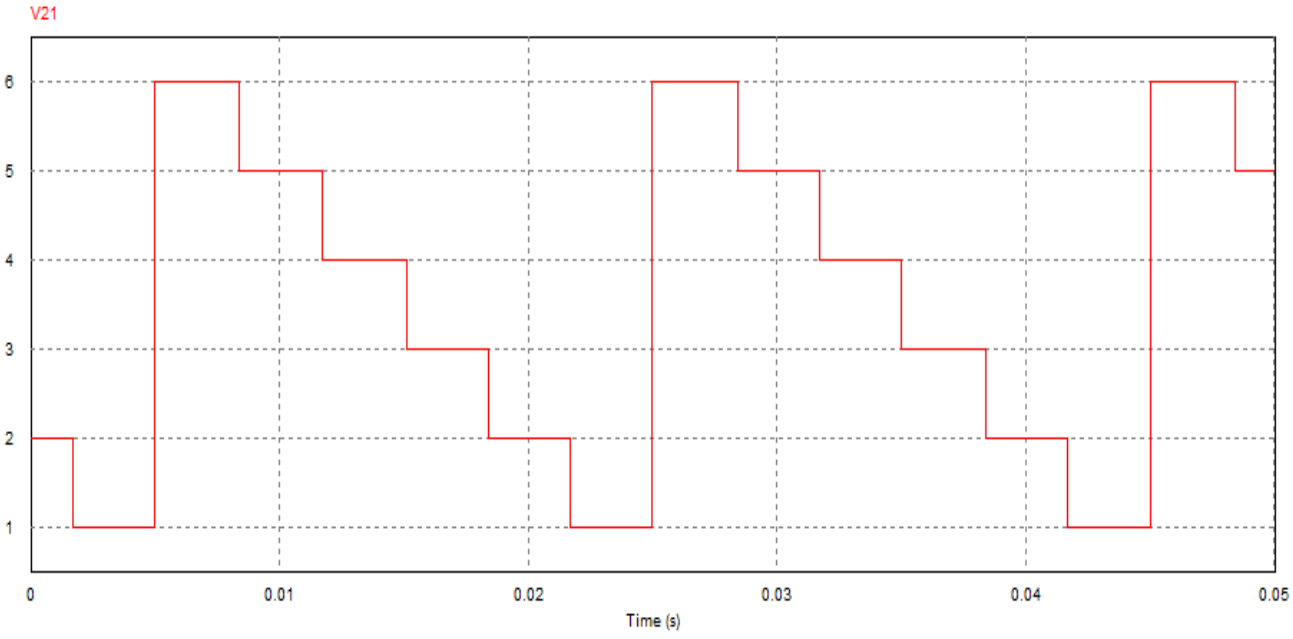


Fig. 5.23: Sector Selection

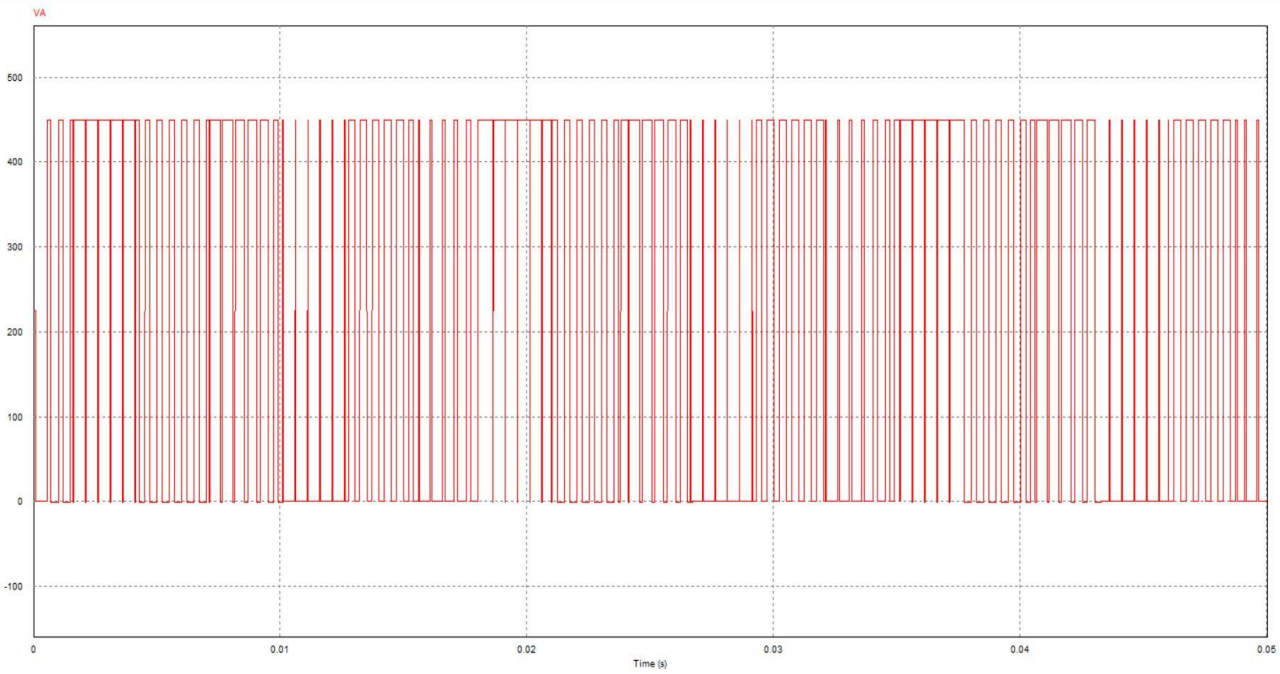


Fig. 5.24: Phase Voltage (V_{ph})

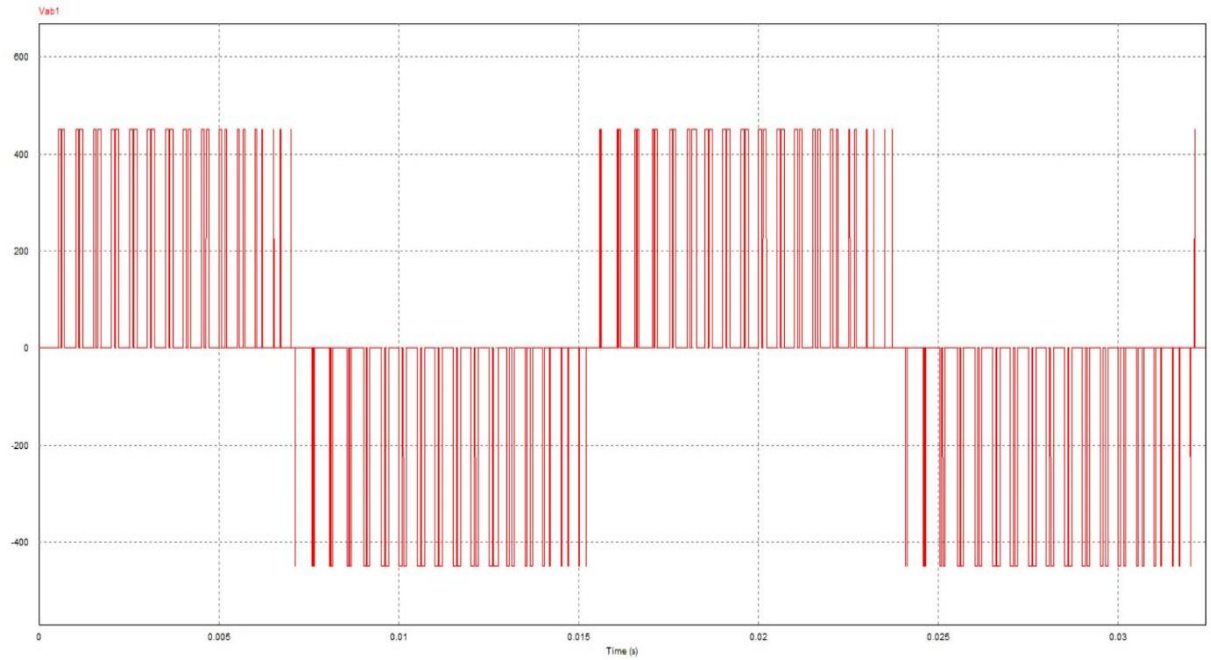


Fig. 5.25: Line-to-Line Voltage (V_{ab})

The Fig. 5.24 & 5.25 shown above represents magnitude of the phase and line-to-line voltage across each phase.

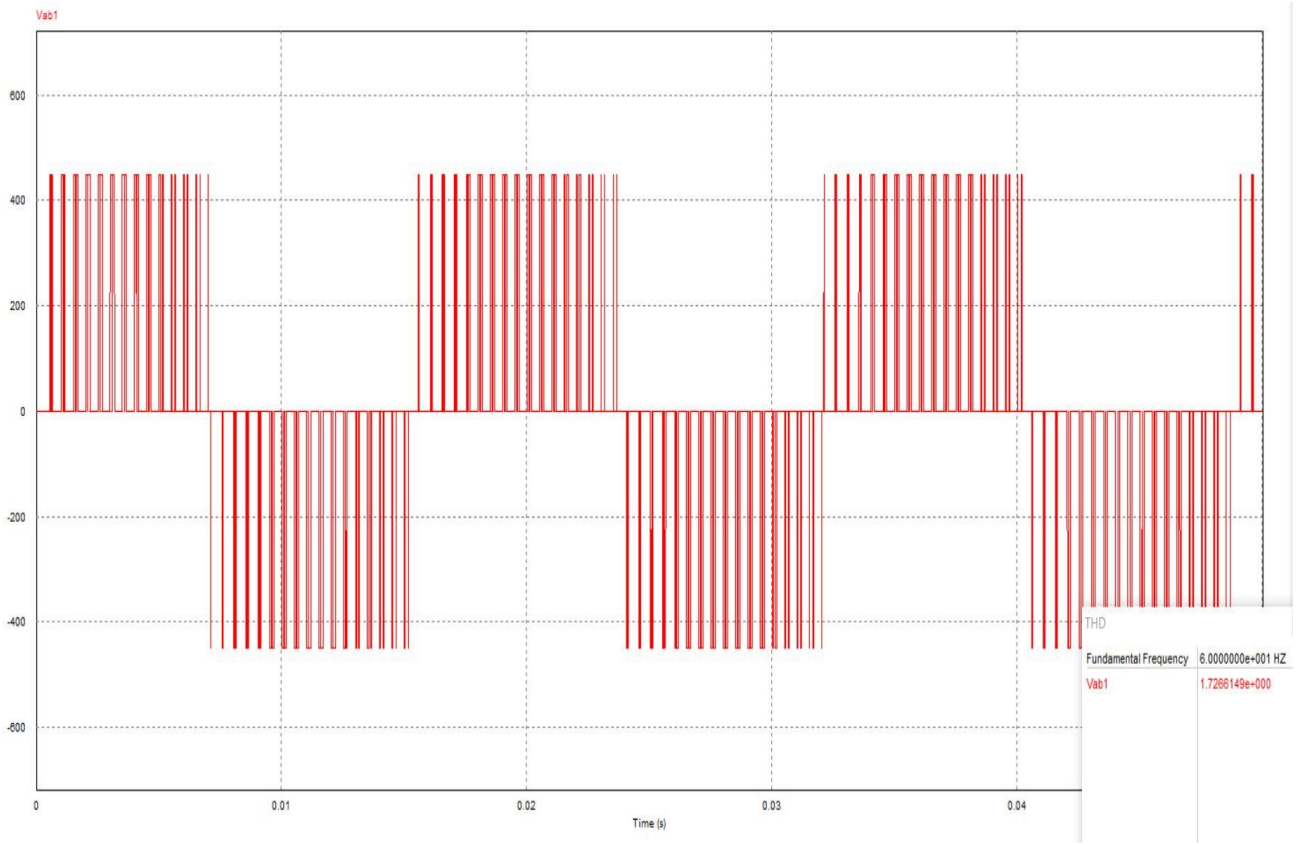


Fig. 5.26: Total Harmonic Distortion (0-1-2-0-2-1-0)

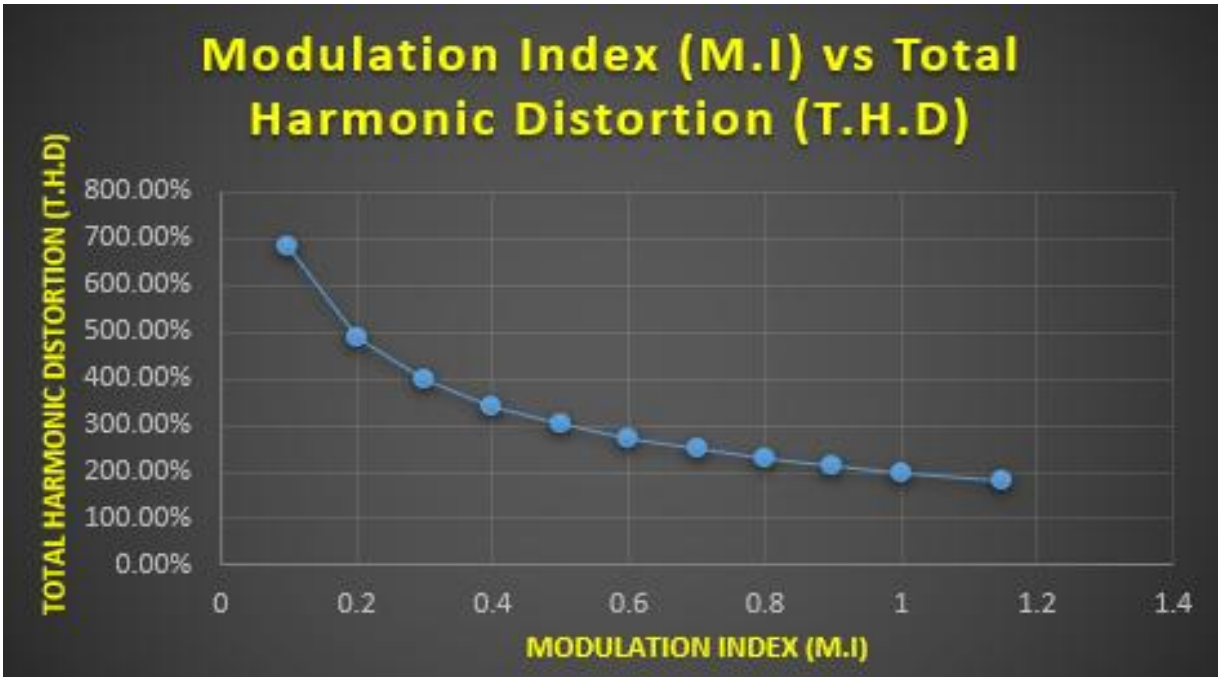


Fig. 5.27: Modulation Index (M.I) vs Total Harmonic Distortion (T.H.D)

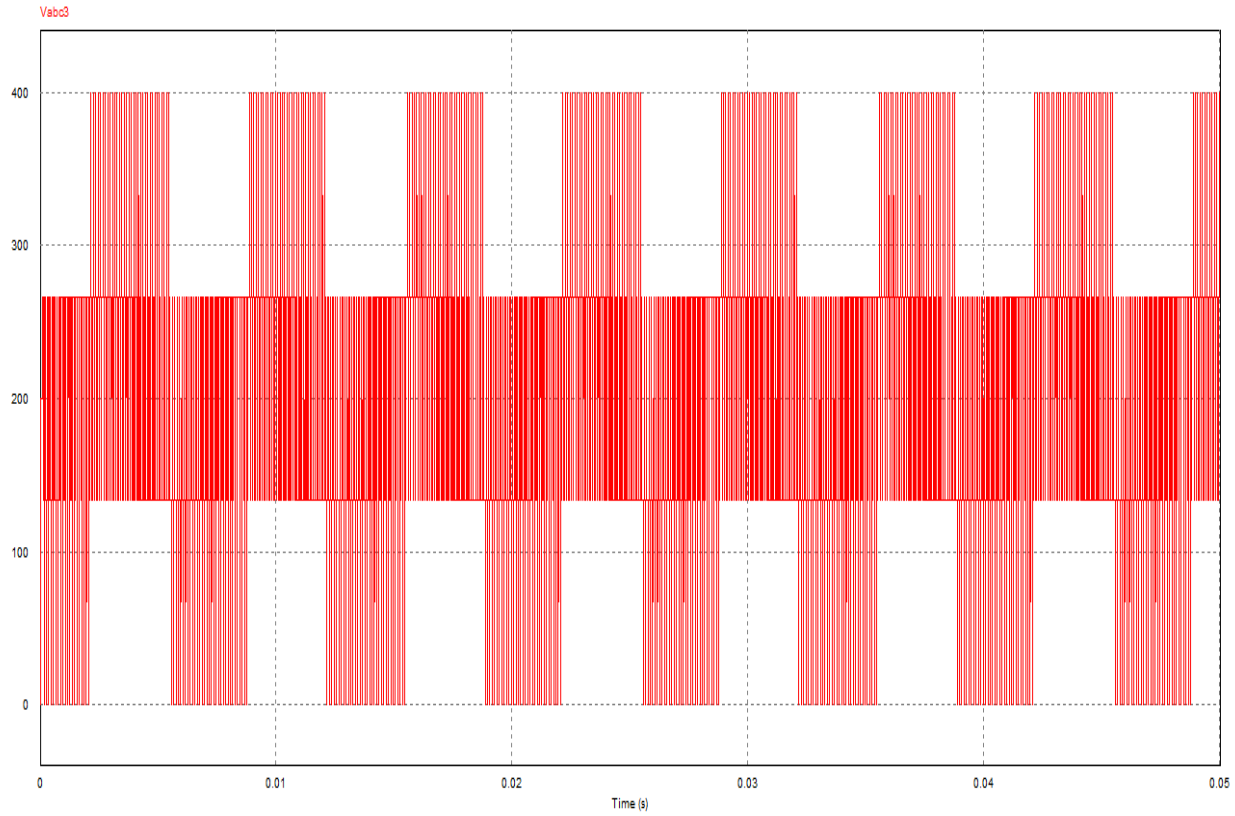


Fig. 5.28: Common Mode Voltage

5.5 BRUSHLESS DC MOTOR

5.3.1Input & Output Power (Resistive Load)

The output three-phase power (in case of star connection) will be given by the relation: -

$$P_{out} = \sqrt{3}V_L I_L \cos\theta$$

$$V_L = 324.69 \text{ V}$$

$$I_L = 5.86 \text{ A}$$

Hence the three-phase output power is calculated as –

$$P_{out} = \sqrt{3}V_L I_L \cos\theta$$

$$P_{out} = \sqrt{3}V_L I_L \cos\theta$$

$$P_{out} = \sqrt{3}*324.69*5.86*0.8$$

$$P_{out} = 2.636 \text{ kW}$$

On the input side of the inverter connected with brushless DC motor since the voltage and current are having DC nature then the expression for input power will be given by

$$P_{in} = V_{DC} I_{DC}$$

$$V_{DC} = 400 \text{ V}$$

$$I_{DC} = 8.29 \text{ A}$$

$$P_{in} = 400*8.29$$

$$P_{in} = 3.316 \text{ kW}$$

Hence the expression of efficiency of inverter will be represented by: -

$$\text{Efficiency} = \frac{\text{Output Power } (P_{out})}{\text{Input Power } (P_{in})}$$

$$\text{Efficiency} = \frac{2.636 \text{ kW}}{3.316 \text{ kW}}$$

$$\text{Efficiency} = 79.493 \%$$

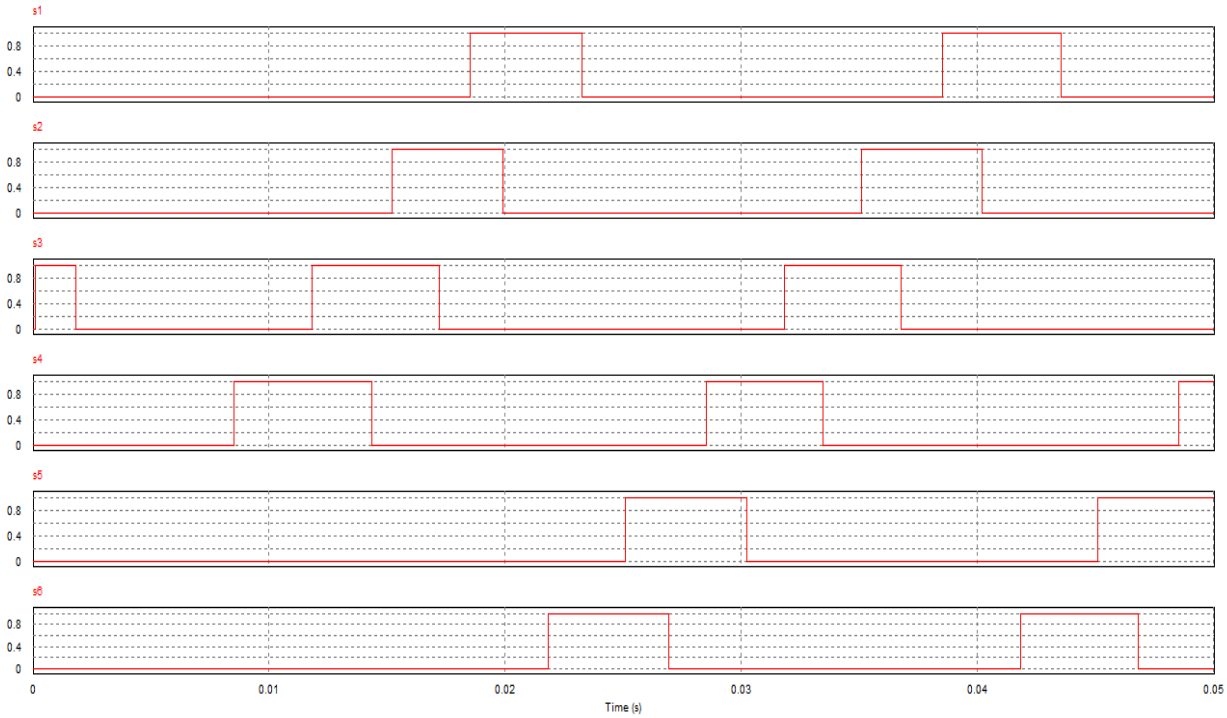


Fig. 5.29: Inverter Switching Pulses

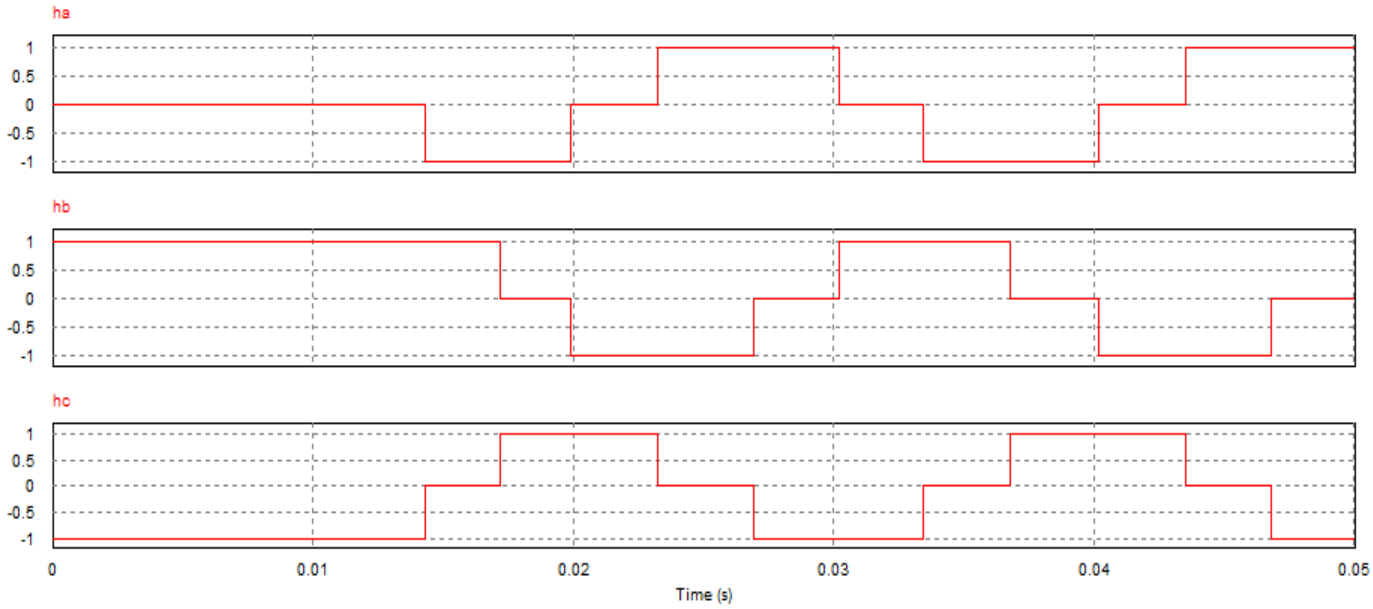


Fig. 5.30: Hall Effect Sensors (h_a, h_3, h_c)

The Fig. 5.29 & 5.30 mentioned above indicates the switching pulses across all switches of inverter and Hall Effect sensor positions indicating the position of rotor crossing each energized winding respectively.

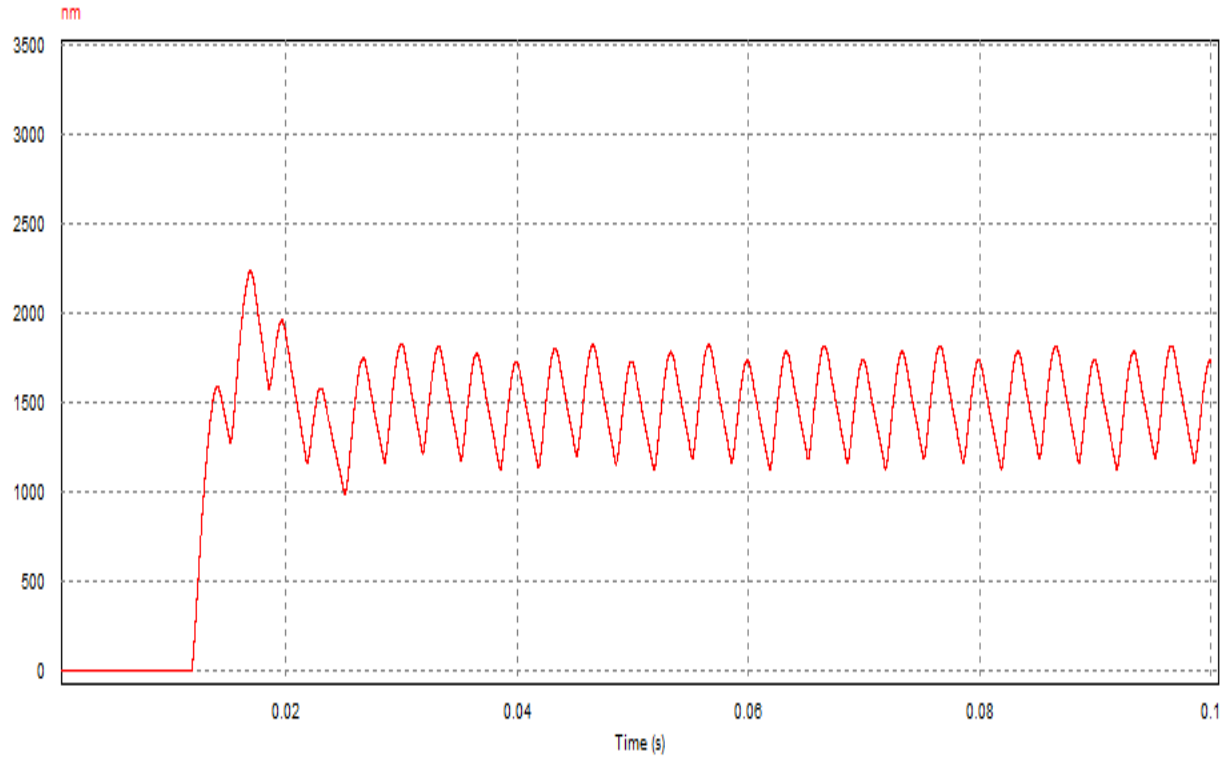


Fig. 5.31: BLDC Motor Speed Curve

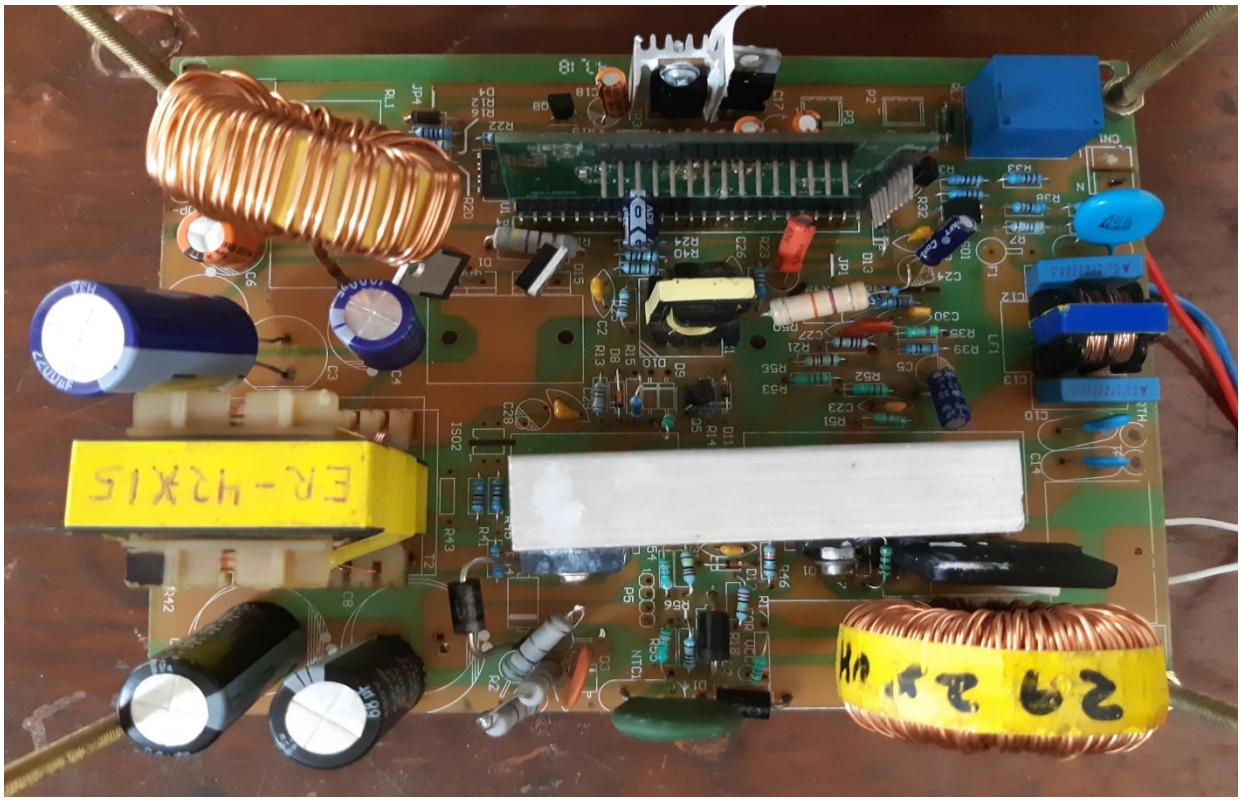


Fig. 5.32: Prototype

The Fig. 5.31 & 5.32 represents the speed curve of brushless DC motor and the pictorial representation of the prototype of the design respectively.

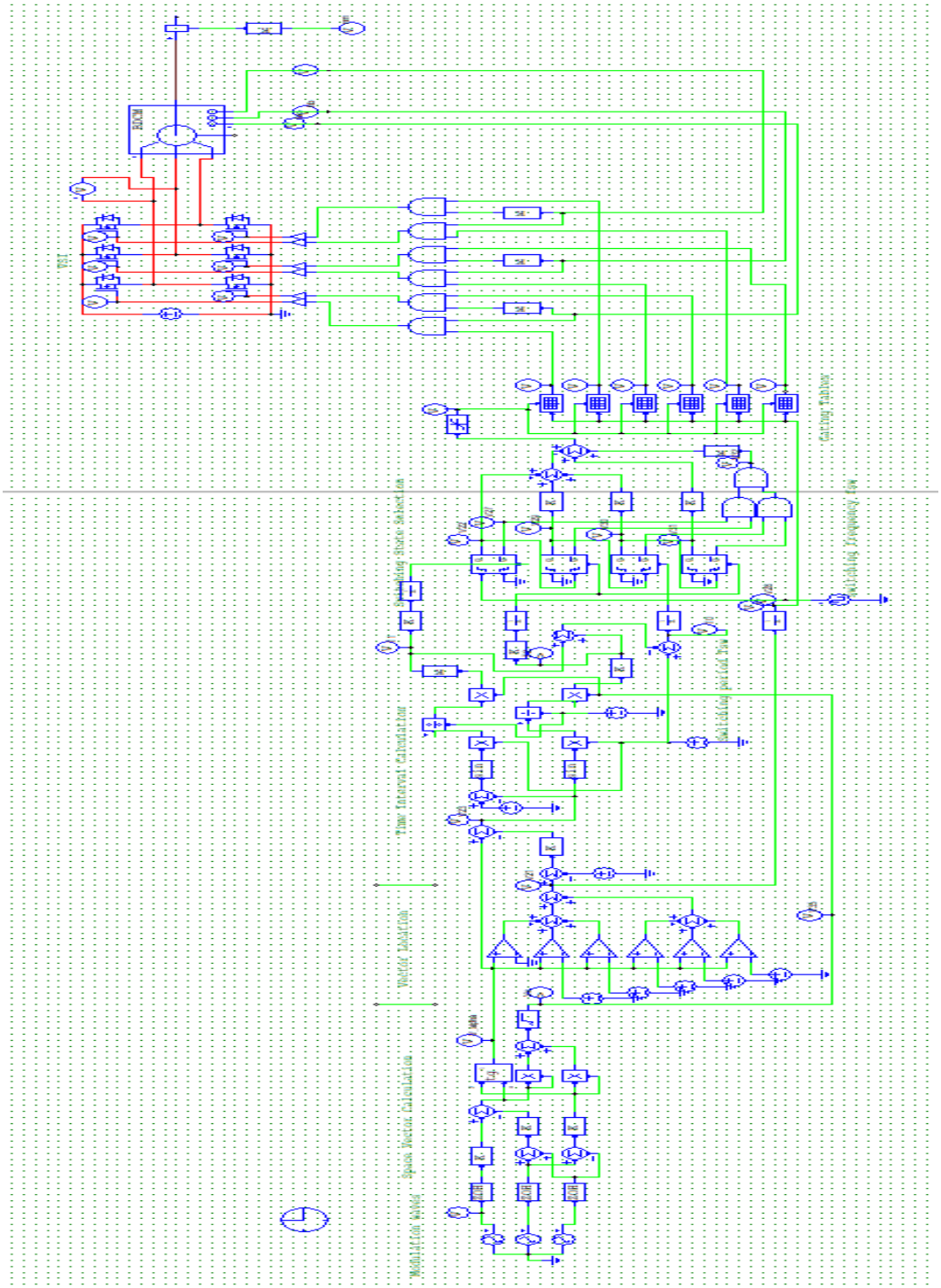


Fig. 5.33: SV-PWM based BLDC Motor Drive Layout

CHAPTER - 6

CONCLUSIONS & FUTURE SCOPE

6.1 CONCLUSIONS

In this thesis the modeling and simulation of the entire BLDC motor drive system is mentioned. Using the PSIM software package, the inverter system based on Space Vector PWM was implemented which drives the BLDC motor (with the prediction of the power factor correction). Furthermore, the SV-PWM technique used the intermediate circuit voltage more efficiently than the other PWM techniques. The BLDC motor speed control with the 120° switch in inverter mode and the use of the SVPWM inverter has been implemented in the PSIM software. With the SV-PWM based inverter technique we get better control of the voltage and current supplied to the motor.

6.2 FUTURE SCOPE

To implement the design of the BLDC motor controller using the SV-PWM-based inverter with the adaptation of the power factor correction techniques using the Texas Instruments C2000 microcontroller model TMS320F2802 which will optimize processing, detection and detection operations to improve the closed-loop performance of the complete system. Furthermore, the ripple of the speed curve of the brushless DC motor can be reduced by correctly synchronizing the Hall Effect sensors and the pulses generated by the spatial vector - modulation of the pulse width.

REFERENCES

[1] Ho, T.Y., 2018. The Design of Motor Drive for Brushless DC Motor. *Electric Machines for Smart Grids Applications: Design, Simulation and Control*, p.73.

[2] Genç, N. and İskender, İ., 2012. Teaching of power quality phenomenon based on modeling and simulation of boost type PFC converters. *Computer Applications in Engineering Education*, *20*(1), pp.149-160.

[3] Wang, K., Lee, F.C. and Lai, J., 2000. Operation principles of bi-directional full-bridge DC/DC converter with unified soft-switching scheme and soft-starting capability. In *APEC 2000. Fifteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No. 00CH37058)* (Vol. 1, pp. 111-118). IEEE.

[4] Azazi, H.Z., El-Kholy, E.E., Mahmoud, S.A. and Shokralla, S.S., 2010, December. Review of passive and active circuits for power factor correction in single phase, low power AC-DC converters. In *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)* (p. 217).

[5] F II, I., 1993. IEEE recommended practices and requirements for harmonic control in electrical power systems. *New York, NY, USA*

[6] Lim, S., Otten, D.M. and Perreault, D.J., 2015. New AC–DC power factor correction architecture suitable for high-frequency operation. *IEEE Transactions on Power Electronics*, *31*(4), pp.2937-2949.

[7] A. I. Pressman, “Switching power supply design”. McGraw-Hill, Second edition, Ch. 4.

[8] K. Billings,” Switch mode power supply handbook,” New York, 1989.

[9] R. Ridley, “Fly back converters with no snubbers,” Switching power magazine.

[10] “Snubber circuits suppress voltage transient spikes in multiple output DC-DC Fly back converter power supplies,” Application note 848 Maxim Nov. 2001.

[11] M. Milanovic, J. Korelic, A. Hren, F. Mihalic, P. Slibar, “The RCRCD clamp circuit for fly-back converter,” in Proceedings of the IEEE International Symposium on Industrial Electronics, 2005, Vol. 2, pp. 547- 552.

[12] S. Howimanporn; C. Bunlaksananusorn, “Performance comparison of continuous conduction mode (CCM) and discontinuous conduction mode (DCM) flyback converters,” in Proc. IEEE Power Electronics and Drive Systems Conf., 2003, Vol.2, pp. 1434 - 1438.

[13] S. Singh and B. Singh, "A Voltage-Controlled PFC Cuk Converter-Based PMBLDCM Drive for Air-Conditioners", *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 832-838, 2012.

[14] B. Singh and V. Bist, "Improved power quality bridgeless Cuk converter fed brushless DC motor drive for air conditioning system", *IET Power Electronics*, vol. 6, no. 5, pp. 902-913, 2013.

[15] V. Bist and B. Singh, "An Adjustable-Speed PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive", *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 2665-2677, 2014.

[16] V. Bist and B. Singh, "A PFC-Based BLDC Motor Drive Using a Canonical Switching Cell Converter", *IEEE Transactions on Industrial Informatics*, vol. 10, no. 2, pp. 1207-1215, 2014.

[17] V. Bist and B. Singh, "PFC Cuk Converter-Fed BLDC Motor Drive", *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 871-887, 2015.

[18] B. Singh and V. Bist, "A BL-CSC Converter-Fed BLDC Motor Drive with Power Factor Correction", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 172-183, 2015.

[19] B. Singh, V. Bist, A. Chandra and K. Al-Haddad, "Power Factor Correction in Bridgeless-Luo Converter-Fed BLDC Motor Drive", *IEEE Transactions on Industry Applications*, vol. 51, no. 2, pp. 1179-1188, 2015.

[20] V. Bist and B. Singh, "A Unity Power Factor Bridgeless Isolated Cuk Converter-Fed Brushless DC Motor Drive", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 7, pp. 4118-4129, 2015.

[21] V. Bist and B. Singh, "Reduced sensor configuration of a power factor correction based single-ended primary inductance converter fed brushless DC motor drive", *IET Power Electronics*, vol. 8, no. 9, pp. 1606-1615, 2015.

[22] P. Singh, B. Singh and V. Bist, "Brushless DC motor drive with power factor regulation using Landsman converter", *IET Power Electronics*, vol. 9, no. 5, pp. 900-910, 2016.

[23] P. Singh, B. Singh, V. Bist, K. Al-Haddad and A. Chandra, "BLDC Motor Drive Based on Bridgeless Landsman PFC Converter with Single Sensor and Reduced Stress on Power Devices", *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 625-635, 2018.

[24] L4984D “CCM PFC Controller” IC Datasheet

[25] Infineon “IPA60R099P7 MOSFET” 600V CoolMOS P7 Power Transistor Datasheet

[26] C. Silva, "Power Factor Correction with the UC3854," Application Note, Unitrode Integrated Circuit

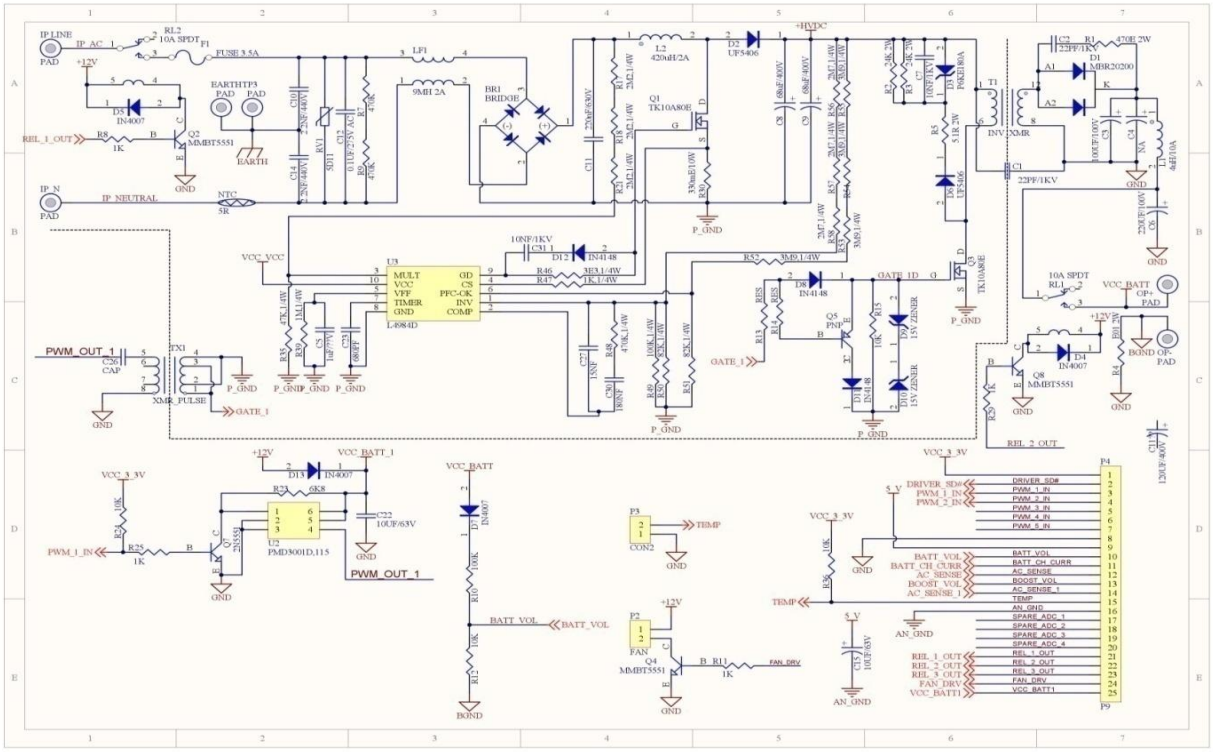
[27] R. Redl, L. Balogh, "RMS, DC, Peak, and Harmonic Currents in High-Frequency Power-Factor Correctors with Capacitive Energy Storage," APEC Conf. Proc., 1992, pp. 533-540

[28] Zhang, W., Zhang, W., Yang, J. and Al-Naemi, F., 2013. Comparisons between CRM and CCM PFC. Energy and Power Engineering, 5(4B), pp.864-868.

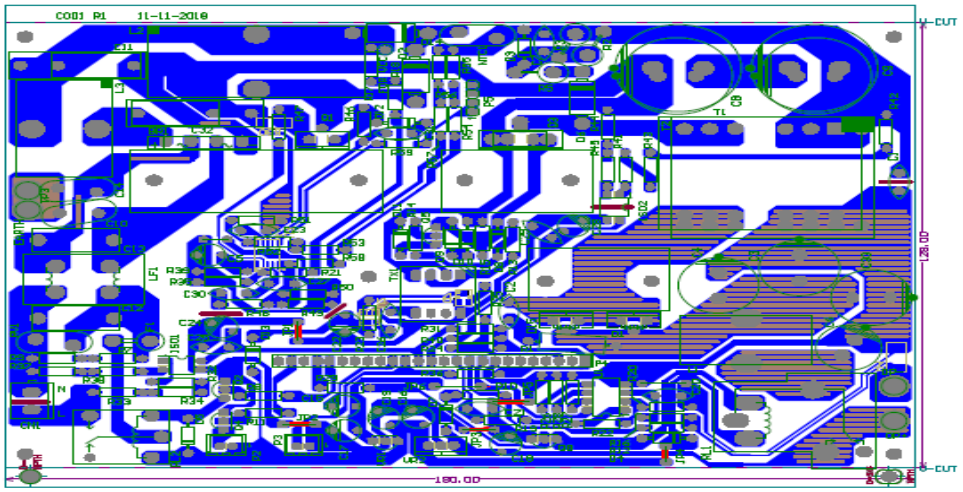
[29] Holmes, D.G., 1996. The significance of zero space vector placement for carrier-based PWM schemes. *IEEE Transactions on Industry Applications*, *32*(5), pp.1122-1129.

[30] “Space Vector Pulse Width Modulation” NPTEL Video Lectures by Prof. K. Gopakumar Dept. of Electronic Systems and Engineering, India Institute of Science (IISc) Bangalore.

APPENDIX-A
HARDWARE SCHEMATIC & PCB DESIGN



Symbol	Hit Count	Tool Size	Plated	Hole Type
▽	59	0.9mm (35.433mil)	PTH	Round
□	186	1mm (39.37mil)	PTH	Round
○	67	1.2mm (47.244mil)	PTH	Round
⊞	9	1.3mm (51.181mil)	PTH	Round
⊠	28	1.4mm (55.118mil)	PTH	Round
◇	13	1.5mm (59.055mil)	PTH	Round
▽	6	1.7mm (66.929mil)	PTH	Round
⊕	6	2mm (78.74mil)	PTH	Round
□	1	2.1mm (82.677mil)	PTH	Round
◇	5	2.2mm (86.614mil)	PTH	Round
⊠	4	2.6mm (102.362mil)	PTH	Round
◇	11	3mm (118.11mil)	PTH	Round
⊕	2	4mm (157.48mil)	NPTH	Round
	394 Total			



APPENDIX-B
LIST OF COMPONENTS

Component	Designation	Type
0.1uF/50V	C20,C21,C25,C29	Capacitor
0.47uF/63V	C26	Capacitor
10NF/50V	C31	Capacitor
10NF/1KV	C7	Capacitor
2.2nF/2KV	C1	Capacitor
22PF/100V	C2	Capacitor
22NF /100V	C27	Capacitor
270NF	C30	Capacitor
680PF/50V	C23	Capacitor
10uF/63V, ALU	C15,C22	Capacitor
1uF/16V,ALU EECTRO	C24,C28	Capacitor
1uF/63V, ALU EECTRO	C5	Capacitor
22uF/50V, ALU	C16,C17,C18,C19	Capacitor
220uF/50V, ALU	C6	Capacitor
820uF/50V, ALU	C3,C33	Capacitor
NU	C4	Capacitor
270uF/250V, ALU	C8,C9	Capacitor
1uF/305V AC-X2 FILM CAP BOX TYPE	C12,C13	Capacitor
330nF/630V, MPP	C11,C32	Capacitor
2N2F/1KV	C10,C14	Capacitor
240mE/1W	R30	Resistor
E01 2W	R4	Resistor
100E,1/4W, MFR	R14	Resistor
100K,1/4W,MFR	R10,R49	Resistor
10E,1/4W,MFR	R13	Resistor
10K,1/4W,MFR	R12,R15,R24,R36	Resistor
1K,1/4W,MFR	R11,R16,R19,R20,R25,R26,R27,R28,R29,R47,R8	Resistor
1M,1/4W,MFR	R39	Resistor
2K4,1/4W,MFR	R31,R40	Resistor
2M2,1/4W,MFR	R17,R18,R21	Resistor
2M7,1/4W,MFR	R56,R57,R58	Resistor
300K,1/4W,MFR	R48	Resistor
33K,1/4W,MFR	R22	Resistor
3E3,1/4W,MFR	R46	Resistor
2M4,1/4W,MFR	R52,R53,R54,R55	Resistor
470K,1/4W,MFR	R7,R9	Resistor

47K,1/4W,MFR	R35,R59	Resistor
68K,1/4W,MFR	R33,R34,R37,R38,R42,R43,R44,R45,R23,R32,R41	Resistor
82K,1/4W,MFR	R51	Resistor
6K8,1/4W,MFR	R23,R32,R41	Resistor
82K,1/4W,MFR	R50	Resistor
82K,3W,MOR	R2	Resistor
NU	R3	Resistor
470E 2W/MOR	R1	Resistor
5.1R 2W,MOR	R5	Resistor
IN4007	D13,D4,D5,D7	Diode
IN4148	D11,D12,D8	Diode
NU	D3	Diode
IN5406	D14	Diode
STTH3R06RL OR MUR460	D2	Diode
STTH110	D6	Diode
SR20H200C	D1,D15	Diode
FUSE 4A	F1	Fuse
GBU4J OR RBU406M	BR1	Bridge rectifier
CONTROL CARD	P4	HEADER25X1
MOV,310V	RV1	PITCH,7.5MM
NTC 5R	NTC1	NTC
PC814	ISO1	Photo coupler
PC814	ISO2	Photo coupler
BA10358F-E2	U1	PDIP8
PMD3001D,115	U2	SOT23-6
BC847	Q7	SOT23-BCE
PFC INDUCTOR,1831mH/2A	L2	TOROIDAL Inductor
70uH/2A	L3	TOROIDAL Inductor
3mH EMI LINE FILTER	LF1	Emi Filter
PULSE TRANSFORMER	TX1	XMR_PULSE
4uH/10A, OUT PUT FILTER	L1	TOROIDIAL
TRANSFORMER,EER42	T1	ALSA_XMR
L4984D	U3	SSO10
2N5401	Q5	TO92-CBE
MMBT5551	Q2,Q4,Q8	TO92-CBE
LP2950	VR1	Voltage Regulator
STF18N65M5	Q1	MOSFET

CURRICULUM VITAE

Hemant **Kumar**

MTECH · POWER SYSTEMS

314/3, XVII-4, Kathuria Bhawan, Subhash Nagar, Hisar, Haryana (Pin Code-125001)

(+91) 9650517501 | happykathuria2009@gmail.com | hemant-kumar-23720795

"Be the change that you want to see in the world."

Career Objective

Aiming to use my knowledge and work in a friendly environment which benefits both the organisation as well as my skills through which in turn i can serve the society

Work Experience

Power Grid Corporation India Limited — *Gurugram*

INTERN — *Jun 2016 - Dec 2016*

- Data Analysis of information decoded from each frame of logs of Balipara 400 KV substation
- Information decoded represents state of data flowing between RTU and MCC using IEC 60870-05-104 protocol

BSNL — *Hisar, Haryana*

INTERN — *Jun. 2015*

- Studied functionality of biggest telecommunication giant in India
- Learned about networks, wireless communication system and its development, 3G, 4G network

Conferences Attended

NATIONAL

2018 **NATIONAL CONFERENCE ON ADVANCES IN POWER, CONTROL AND COMMUNICATION SYSTEMS,** Presented paper on "CONSTRUCTION AND DESIGN FEATURES OF GAS INSULATED SYSTEM(GIS) — *Kurukshetra*

Key Projects

Design & Development of BLDC Motor Controller

INDIVIDUAL — *June 2018 - Current*

- PFC converter operating in DCM is used to control the converter via an voltage follower approach which requires a single sensor for PFC and DC link voltage control.
- The speed of BLDC motor is controlled by adjusting the DC link voltage of the VSI feeding PMBLDC motor which allows the VSI To operate in fundamental frequency switching for reducing the losses in VSI
- Simplicity in control,reducing the number of sensors and cost and increasing the overall efficiency of the system.
- Implementation of Space Vector (SV) Pulse Width Modulation Strategy for a 180 degree based voltage source inverter (VSI)

MATLAB Simulation of CHOPPER fed DC Drive

INDIVIDUAL — *Sept 2017 - Dec 2017*

- Speed of DC Motor successfully controlled by using chopper as converter
- PI type speed and current control based on closed loop model of DC Motor

Implementation of Control Strategies for Power Quality Improvement using D-STATCOM in MATLAB

INDIVIDUAL — *Sep 2017 - Dec 2017*

- Power Quality improvement through level and phase shifted modulation techniques

Power Load Balancing using FUZZY Logic concept

INDIVIDUAL — *Oct 2017 - Dec 2017*

- Each phase loading can be expanded to design load balancing systems for variable loads in future

Design Three Phase Stator

TEAM LEADER — *Jan 2016 - Apr 2016*

- Designed the stator for 24 slots 4 pole and 36 slots 6 pole

Design and Fabrication of 1 KV Transformer

TEAM MEMBER *Aug 2014 - Nov 2014*

- Designed the transformer of rating 220/110 V

Fire Alarm

TEAM MEMBER *Sep 2014 - Nov 2014*

- Designed and Implemented a circuit on printed circuit board to detect the unwanted presence of fire by monitoring environmental changes associated with combustion

Rain Water Alarm

TEAM LEADER *Mar 2014 - Apr 2014s*

- Design and Implemented a circuit on PCB to detect rain and make alert
- Simple and reliable circuit of rain water alarm was developed at very low cost

Positions of Responsibility

IEEE STUDENT MEMBER TIET CHAPTER *January 2019-Present*

CLASS REPRESENTATIVE

CLASS LEAD *Apr 2015 - May 2017*

- Handled planning and organisation of various campus placement drives in college
- Actively and Successfully organized guest lectures, sport events, industry visit, talks

COLLEGE TECHNICAL REPRESENTATIVE at TECHNICHE, IIT GUWAHATI

VOLUNTEER *Sept 2015 and Sept 2016*

- One team secured 3rd Position in ESCALADE 3.0 (Zonal Level)
- Organised and managed various events and workshops for selection of college team for participation in different competetions

CONTINGENT LEADER at MOOD INDIGO, IIT BOMBAY

MANAGER *Dec 2014*

- Led a team of enthusiastiic students and partcipated in variety of competetions

Education

Thapar Institute of Engineering and Technology *Patiala, Punjab*

MTECH IN POWER SYSTEMS *Aug 2017 - Present*

- CGPA 8.35 (Till Third Semester)

YMCA University of Science and Technology *Faridabad, Haryana*

BTECH IN ELECTRICAL ENGINEERING *Aug 2013 - May 2017*

- CGPA 7.918

Campus School,CCS HAU Hisar *Hisar, Haryana*

INTERMEDIATE 10+2 *Apr 2011- Mar 2012*

- Percentage: 77.80

Campus School,CCS HAU Hisar *Hisar, Haryana*

MATRICULATION *Apr 2009- Mar 2010*

- CGPA 8.6

Extracurricular Activity

Media and Marketing team at Elements Culmyca 2017

CORE MEMBER *Mar 2017*

3rd Position in framed competition

PARTICIPANT *Mar 2016*

- Secured 3rd Position in framed competition organised by JHALAK(photography club) during ELEMENTS CULMYCA 2016

MATLAB and Image Processing

PARTICIPANT *Mar 2015*

- Participated in MATLAB and Image processing workshop at Tryst 2015 IIT Delhi

PLAGIARISM CERTIFICATE

BLDC Motor

ORIGINALITY REPORT

28%	23%	18%	21%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	www.stmicroelectronics.com.cn Internet Source	4%
2	repository.ias.ac.in Internet Source	2%
3	www.mouser.com Internet Source	2%
4	digital-library.theiet.org Internet Source	2%
5	Submitted to Swinburne University of Technology Student Paper	1%
6	Submitted to College of Engineering, Pune Student Paper	1%
7	Praveen Kumar Singh, Bhim Singh, Vashist Bist, Kamal Al-Haddad, Ambrish Chandra. "BLDC Motor Drive Based on Bridgeless Landsman PFC Converter with Single Sensor and Reduced Stress on Power Devices", IEEE Transactions on Industry Applications, 2017	1%

	Publication	
8	ethesis.nitrkl.ac.in Internet Source	1 %
9	yz-car.ci.cqvip.com Internet Source	1 %
10	www.intechopen.com Internet Source	1 %
11	documents.mx Internet Source	1 %
12	tii.ieee-ies.org Internet Source	1 %
13	Submitted to IIT Delhi Student Paper	1 %
14	Submitted to Jawaharlal Nehru Technological University Student Paper	1 %
15	www.irjet.net Internet Source	1 %
16	Kim, Yoon-Ho, and Seong-Je Kim. "Prediction of 2-Level PWM Inverter Efficiency Using MATLAB/SIMULINK", International Journal of Electronics, 2014. Publication	1 %
17	www.ijmetmr.com Internet Source	1 %

18	Submitted to Sardar Vallabhbhai National Inst. of Tech.Surat Student Paper	1 %
19	ijsetr.org Internet Source	<1 %
20	Singh, Sanjeev, and Bhim Singh. "A Voltage-Controlled PFC Cuk Converter-Based PMBLDCM Drive for Air-Conditioners", IEEE Transactions on Industry Applications, 2012. Publication	<1 %
21	Submitted to SASTRA University Student Paper	<1 %
22	pen2print.org Internet Source	<1 %
23	Submitted to Hanyang University Graduate School Student Paper	<1 %
24	Submitted to Indian Institute of Technology, Madras Student Paper	<1 %
25	Submitted to Higher Education Commission Pakistan Student Paper	<1 %
26	Nasir Coruh, Satilmis Urgun, Tarik Erfidan. "Design and implementation of flyback	<1 %

converters", 2010 5th IEEE Conference on Industrial Electronics and Applications, 2010
Publication

27	www.elektrinis-dviratis.eu Internet Source	<1%
28	Submitted to University of Greenwich Student Paper	<1%
29	Submitted to New York Institute of Technology Student Paper	<1%
30	A. Bharathi Sankar, R. Seyezhai. "Simulation and implementation of sensored control of three-phase BLDC motor using FPGA", 2014 International Conference on Science Engineering and Management Research (ICSEMR), 2014 Publication	<1%
31	Khizir Mahmud, Lei Tao. "Power factor correction by PFC boost topology using average current control method", 2013 IEEE Global High Tech Congress on Electronics, 2013 Publication	<1%
32	Submitted to Malaviya National Institute of Technology Student Paper	<1%
33	Submitted to Savitribai Phule Pune University Student Paper	<1%

34	G. M. Ponzo. "An improved Flyback converter", 2009 6th International Conference on Electrical Engineering/Electronics Computer Telecommunications and Information Technology, 05/2009 Publication	<1%
35	S. Mahdiuon-Rad, M. R. Azizian, S. Soleimanpour. "Modeling, simulation and implementation of a sensorless commutation method for brushless DC motors without phase shifter", The 6th Power Electronics, Drive Systems & Technologies Conference (PEDSTC2015), 2015 Publication	<1%
36	archive.org Internet Source	<1%
37	jpinfotech.org Internet Source	<1%
38	ijireeice.com Internet Source	<1%
39	asokatechnologies.blogspot.com Internet Source	<1%
40	docplayer.net Internet Source	<1%
41	Singh, Bhim, Vashist Bist, Ambrish Chandra, and Kamal Al-Haddad. "Power Factor	<1%

	Correction in Bridgeless-Luo Converter-Fed BLDC Motor Drive", IEEE Transactions on Industry Applications, 2015. Publication	
42	www.ijareeie.com Internet Source	<1%
43	Submitted to University Tun Hussein Onn Malaysia Student Paper	<1%
44	www.sdaengineering.com Internet Source	<1%
45	M. Peterson, B. Singh. "Design, Control, and Simulation of a Novel Power Conversion System", 2006 IEEE PES Power Systems Conference and Exposition, 2006 Publication	<1%
46	www.st.com Internet Source	<1%
47	Submitted to University of Western Sydney Student Paper	<1%
48	file.allitebooks.com Internet Source	<1%
49	www.scribd.com Internet Source	<1%
50	Submitted to Universiti Teknikal Malaysia	

	Melaka Student Paper	<1%
51	Praveen Kumar Singh, Bhim Singh, Vashist Bist, Kamal Al-Haddad, Ambrish Chandra. "BLDC Motor Drive Based on Bridgeless Landsman PFC Converter With Single Sensor and Reduced Stress on Power Devices", IEEE Transactions on Industry Applications, 2018 Publication	<1%

Exclude quotes	On	Exclude matches	< 16 words
Exclude bibliography	On		