

COMPARATIVE STUDY OF CMOS VOLTAGE CONTROLLED OSCILLATORS

A Thesis

Submitted towards the partial fulfillment of requirements for the award of the degree of

Master of Technology (VLSI Design & CAD)

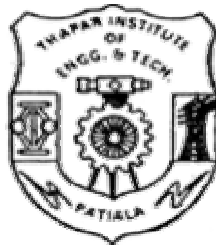
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Declaration

I hereby certify that the work which is being presented in the thesis entitled, **“Comparative Study of CMOS Voltage Controlled Oscillators”** in partial fulfillment of the requirements for the award of degree of M.Tech. (VLSI Design and CAD) at Electronics and Communication Department of Thapar Institute of Engineering and Technology (Deemed University), Patiala, is an authentic record of my own work carried out under the supervision of Dr. Ravinder Agarwal, Assistant Professor, EIED & Head, USIC and Mrs. Alpana Agarwal, Assistant Professor, ECED.

The matter presented in this thesis has not been submitted in any other University/ Institute for the award of any degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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Acknowledgement

To discover, analyze and to present something new is to venture on an untrodden path towards an unexplored destination is an arduous adventure unless one gets a true torchbearer to show the way. I would have never succeeded in completing my task without the cooperation, encouragement and help provided to me by various people. The enlightening guidance, I found in my revered guide Dr. Ravinder Agarwal, Assistant Professor, EIED & Head, USIC, Thapar Institute of Engineering & Technology (Deemed University), Patiala, without whose patronization it was never possible to give final shape to this thesis. I wish to express my deep gratitude towards him for providing individual guidance and support throughout the Thesis work.

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Abstract

Oscillators are integral part of many electronic systems. An oscillator is an electronic device used for the purpose of generating a signal. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillators topologies and performance parameters. Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges. This paper deals with the analysis and design of CMOS oscillators more specifically voltage controlled oscillators (VCOs).

A VCO is an oscillator, where the control voltage controls the oscillator output frequency. VCOs are perhaps the most ubiquitous element in all communication systems, wired or wireless. In a wireless system the quality of the communication link is determined in large part by the characteristics of the VCO and in today's wireless communication systems greater frequency range is required by the VCOs. Traditionally, relaxation oscillators using CMOS technology have been used for low frequency applications, but submicron processes have allowed CMOS oscillators to achieve frequencies in the gigahertz range. This range is made possible with the use of automatic swing control. The available transistors during the 1960's were in the 2 GHz range; today in our designs we use Bipolar transistors and FETS at frequency to 18 GHz.

VCO can be built using many circuit techniques. Primarily, there are two methods of designing CMOS VCOs, one uses a ring oscillator and other uses a schmitt trigger. Though there are so many design requirements of a VCO, which are phase stability, large electrical tuning range, linearity of frequency verses control voltage, large gain factor, capability of accepting wideband modulation and low cost but the most important factor in designing the VCO is the linearity, on the basis of which the comparison between CMOS VCOs is described. With respect to digital phones that use these circuits, low power consumption, small size and low fabrication costs are important design factors. In order to achieve a higher quality factor, CMOS relaxation oscillators have been designed in the form of ring oscillators.

Apart from communication systems, VCOs are an integral part of Biomedical Systems, especially in Pacemakers. In pacemaker, a low frequency VCO is required to control the frequency of the pulses coming from the heart, so as to obtain the desired frequency.

Efforts have been made to achieve the frequency as low as possible, so that the VCO can be utilized for the pacemaker application.

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Chapter 1

INTRODUCTION

1.1 Objective of the Thesis work

Voltage Controlled Oscillators (VCOs) are perhaps the most ubiquitous element in all communication systems, wired or wireless. They appear in many analog and RF signal processing systems. Wireless and optical communication systems have shown an explosive growth during the last few years. This exponential growth has driven the need for more compact, more cost-effective, fully integrated, low noise, low power voltage-controlled oscillator (VCO). Apart from communication systems, VCOs are an integral part of biomedical applications. As the feature size gets smaller, CMOS technologies became attractive for the realization of high speed and high frequency ICs.

This thesis is a step forward to this rapidly growing communication systems and biomedical field. The objective of the work was to design a low frequency VCO for pacemaker application. For this, number of CMOS VCOs are designed by using two techniques, and their comparative study is done on the basis of their linearity. The VCO which obtained the best linearity, is chosen for pacemaker circuit. Thus it is seen that VCOs occur in many applications and make possible circuits and subsystems that perform very useful functions.

1.2 Abbreviations and Color Schemes used

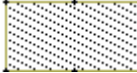
The abbreviations used in this report are listed below followed by the color scheme used while drawing layout:


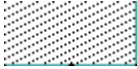

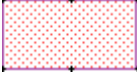





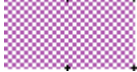
AC	Alternating Current
CAD	Computer Aided Design
SPICE	Simulation Program with Integrated

	Circuit Emphasis
CMOS	Complementary Metal Oxide Semiconductor
PMOS	P- Channel Metal Oxide Semiconductor
NMOS	N- Channel Metal Oxide Semiconductor
DC	Direct Current
Hz	Hertz
IC	Integrated Circuit
MHz	Mega Hertz
VCO	Voltage Controlled Oscillator
VGA	Variable Gain Amplifier
RC	Resistive-Capacitive
LC	Inductive-Capacitive
W	Width of transistor
L	Length of transistor
C	Capacitor
R	Resistance

The color scheme used while drawing layout is shown in Table 1.1.

Table1.1 Colour scheme used in drawing the layout

	Poly		N Well
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	Active		N Select
	Metal1		P Select
	Metal2		Via
	Poly Contact		Overglass
	Active Contact		Pad Comment

1.3 Contribution and Organization of Thesis

Main contributions of this thesis are:

- Study of Pacemaker and need of VCO in it.
- Design and simulation of CMOS VCOs by the use of two circuit techniques.
- Comparative study of CMOS VCOs, based on their linearity, which is observed from voltage-frequency plot.
- Selection of VCO for pacemaker application.
- Design of a low frequency VCO for pacemaker application.

The thesis report is organized into six chapters. The chapter wise detail is given below:

Chapter 1: In this chapter, the objective of the thesis work is presented along with the abbreviations used in the report and the color scheme followed during the layout.

Chapter 2: This chapter presents introduction of pacemaker and the need of VCO in it.

Chapter 3: In this chapter, basic theory of Oscillators and its types are discussed.

Chapter 4: In this chapter, brief introduction to the Tanner EDA tool is presented.

Chapter 5: This chapter discusses the design and comparison of CMOS VCOs with results of the schematic and layout simulations. It also presents the design of VCO for pacemaker application.

Chapter 7: This chapter presents the conclusion of the work done and future scope.

1.4 Operating System and EDA Tool used

The software and tool used in thesis are as follows

Operating System	: Windows XP
Tools	: Tanner EDA Tool
	S-Edit
	T-Spice Pro
	W-Edit
	L-Edit Pro

Chapter 2

VCO: AN INTEGRAL PART OF PACEMAKER

2.1 Introduction

Heart Pacemakers have now been in use for nearly ten years and during this time have become a powerful therapeutic tool. Developments in semiconductor microelectronics have resulted in increasingly sophisticated pacing circuitry, beginning with the use of two transistors in the first implantable pacemaker in 1958. During the first years, a rather high incidence of pacemaker failures was experienced. Integrated circuits were first used in a pacemaker in 1971 and were quickly adopted as the standard for pacemaker design. Since then, reliability has been improved by selecting highly reliable components for the circuits and by carefully testing each device before implantation. The trend toward increasing levels of integration in design has continued. Whereas IC's in 1980 had device geometry on the order of several microns, IC's today may have device geometry on the order of 1um or less Hybridisation has contributed to miniaturization of modern pacemakers. Pacemakers have required more processing power and memory to carry out an increasing number of functions; more circuitry, often several IC's assembled into very large –scale (VLSI) applications, and interconnections between those circuits were needed. The VLSI were at first only mounted on one side of substrate, later on both sides. Now chips are placed atop one another, involving very dense packaging; and double –sided hybrids are state-of- the- art. So nowadays, pacemakers are designed in CMOS. In today's era, CMOS IC'S with low power consumption and high reliability have replaced bipolar technology. Digital and analog functions can be designed on the same chip. The requirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. Low-power design of digital integrated circuits has emerged as a very active and rapidly developing field of CMOS design.

2.2 Definition of Pacemaker

The heart's "natural" pacemaker is called the sinoatrial (SA) node or sinus node. It produces the electrical impulses that cause your heart to beat. Heart rhythm problems may occur when the natural pacemaker is defective, causing the heartbeat to be too fast, too slow or irregular. Main purpose of pacemaker is to keep the electrical system from going too slow and thereby prevent the problems associated with slow heart rhythms (passing out, congestive heart failure, and others including death). Pacemaker is used to electronically stimulate the heart to contract during periods when intrinsic cardiac electrical activity is inappropriately slow or absent and thus to pump blood throughout the body. Thus the term "Artificial pacemaker" is used for a small battery-operated

device that helps the heart beat in a regular rhythm and is implanted into the body specifically in the heart [11].

2.3 Need of Artificial Pacemaker

Pacemakers are required for many different reasons which are below-

- Brady arrhythmias or slow heart rhythms are caused either due to failure of the pacemaker cells to generate appropriate electrical impulses (disorders of automaticity) or failure to propagate electrical impulses appropriately (heart block) [8].
- Failure of SA node automaticity, resulting in an insufficient number of electrical impulses (sinus bradycardia) is the most common cause of the bradyarrhythmias.
- Heart block implies abnormalities of conduction velocities and/or refractory periods. It ranges from first degree block to third degree block.
- Tachyarrhythmias or fast heart rhythms are caused by three mechanisms which are automaticity, reentry, and triggered activity [30].

2.4 Implantable Pacemakers

Implantable pacemaker, along with its electrodes is designed to be entirely implanted beneath the skin its output leads are connected directly to heart muscle.



Figure 2.1 Implantable Pacemaker

Basic requirements of implantable pacemaker are-

- The miniature components used in the circuit should be highly reliable
- The power should be in a position to supply sufficient power to the circuit over prolonged periods of time.
- The circuit should be covered with a biological inert material so that the implant is not rejected by the body.
- The unit should be covered in such a way that body fluids do not find a way inside a circuit and thus short circuit the batteries or result in other malfunctioning of the circuit [26].

2.5 Functional Blocks in the Pacemaker

A pacemaker is capable of producing stimuli either synchronously with ventricular depolarization signal or at a fixed rate when ventricular depolarization signal fails. As pacemaker is used to achieve desired amplitude and frequency of heart pulses, by which the heart beats normally. Thus there is a need to control two parameters from pacemaker which are amplitude and frequency of the pulses generated by it, so that heart should beat at a normal rate. From the extensive study of pacemaker circuits, it is found that the pacemaker typically consists of three main blocks as shown in the figure 2.2. These are mentioned below.

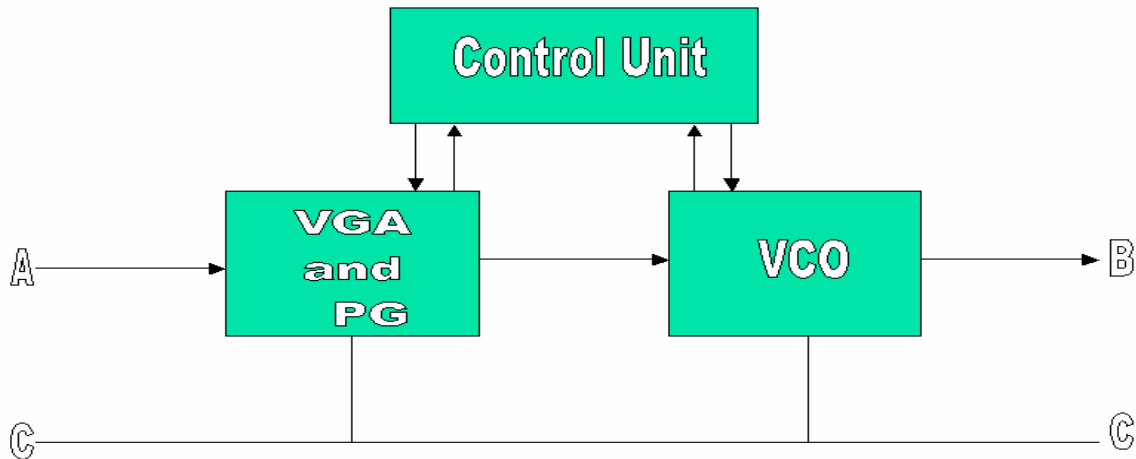


Figure 2.2 Block Diagram of Pacemaker

1) Variable gain Amplifier (VGA) and Pulse generator circuit - It amplifies any signal of physiological origin, VS (ventricular depolarization signal) appearing at the input of the circuit, here it is present between the terminals a and c and makes it able to synchronize external stimuli. Pulse generator determines the frequency and duration of the impulses.

2) Multivibrator or Voltage Controlled Oscillator (VCO) - As there is a need to control the frequency of the pulses to be generated, voltage controlled oscillator is required which controls the frequency of the pulses through input voltage. It generates the pulses which are synchronized with the original pulses. When there is spontaneous generation of heart pulses the rate of which is not less than predetermined value, the pulses generated by the VCO are synchronized with original pulses. When there is no signal generated by the heart or the rate is too slow, the VCO circuit takes over and delivers pulses at a fixed rate. This circuit supplies signal ES (external stimuli) between terminals b and c for heart simulation [8].

3) Control Unit–The Control Unit generates control signals, which control the operation of both amplifier and pulse generator unit and voltage controlled oscillator unit. Basically, this unit consists of other circuitry required for the full operation of the pacemaker.

Apart from above mentioned three blocks, there are some other functional components required for the pacemaker operation are below-

- Encapsulation and Power Source
- Leads
- ***Electrodes***

In view of pacemaker application, design and comparative study of CMOS VCOs is done in the next chapters, so that best VCO can be selected for this application.

Chapter 3

STUDY OF OSCILLATORS

3.1 Introduction

Wave Generators play a prominent role in the field of electronics. They generate signals from a few hertz to several gigahertz (10^9 hertz). Modern wave generators use many different circuits and generate such outputs as sinusoidal, square, rectangular, sawtooth, and trapezoidal waveshapes. These waveshapes serve many useful purposes in the electronic circuits. For example, they are used extensively throughout the television receiver to reproduce both picture and sound. One type of wave generator is known as an **Oscillator**. An oscillator can be regarded as an amplifier which provides its own input signal. It is an electronic device used for the purpose of generating a period electrical waveform at a particular frequency. Oscillators occur in many, many applications and make possible circuits and subsystems that perform very useful functions. They are found for example in computers, wireless receivers and transmitters, and audio-frequency equipment, and music synthesizers.

3.2 The Basic Oscillator

An oscillator can be thought of as an amplifier that provides itself (through feedback) with an input signal. By definition, it is a nonrotating device for producing alternating current, the output frequency of which is determined by the characteristics of the device. The primary purpose of an oscillator is to generate a given waveform at a constant peak amplitude and specific frequency and to maintain this waveform within certain limits of amplitude and frequency [12].

3.2.1 Requirements for an oscillator

a) First, amplification is required to provide the necessary gain for the signal. Every oscillator has at least one active device. This active device acts as an amplifier. An amplifier provides an output that is a replica of the input and is capable of amplifying at the frequency of interest.

b) Second, sufficient regenerative feedback is required to sustain oscillations. In an oscillator, a portion of the output is fed back to sustain the input, as shown in Figure 3.1. Enough power must be fed back to the input circuit for the oscillator to drive itself as does a signal generator. To cause the oscillator to be self-driven, the feedback signal must also be regenerative (positive). Regenerative signals must have enough power to compensate for circuit losses and to maintain oscillations

c) Third, a frequency-determining device or a resonator is needed to maintain the desired output frequency. This device acts as a filter, allowing only the desired frequency to pass. The resonator may contain transformers or other impedance transforming components such as coupling capacitors. Without a frequency-determining device, the stage will oscillate in a random manner, and a constant frequency will not be maintained.

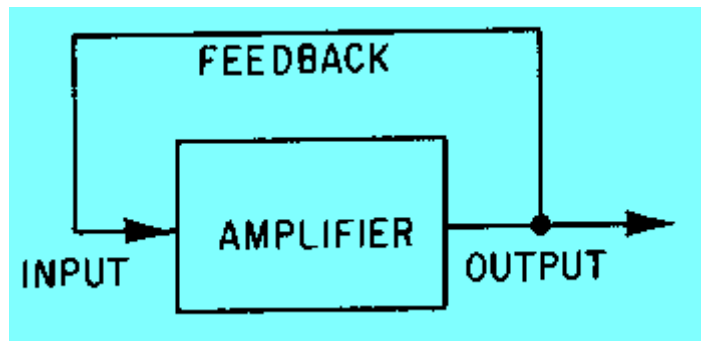


Figure 3.1 Basic oscillator block diagram

Oscillation occurs when an amplifier is furnished with a feedback path that satisfies two conditions:

- Amplitude Condition -- The cascaded gain and loss through the amplifier / feedback network must be greater than or equal to unity.
- Phase Condition -- The frequency of oscillation will be at the point where loop phase shift totals 360 (or zero) degrees.

The oscillator loop gain is given by:-

$$A_f = A / (1-A\beta) \dots \dots \dots (3.1)$$

where A_f = gain after feedback, A = open loop gain and β = feedback factor

The gain A_f will be infinite when the loop gain $A\beta$ is unity and the phase shift is 360° . This is known as the Barkhausen criterion for oscillation in a positive feedback circuit. For a negative feedback circuit we require a phase shift of 180° and these type of circuits are used in CMOS oscillator designs.

In most oscillator circuits, oscillation builds up from zero when power is first applied, under linear circuit operation. However, limiting amplifier saturation and other non-linear effects end up keeping the oscillator's amplitude from building up indefinitely. There will be no output when power is initially applied, but even if the amplifier were noise free, noise would still be generated in the resonator at the resonant frequency. This noise will be applied to the input of the amplifier where it will be amplified and fed back in phase at the resonant frequency and further amplified, building up each time. Eventually the signal will cause the amplifier to limit, ensuring that the oscillator output power eventually peaks, usually at the saturated output power of the amplifier. The basic oscillator requirements, in addition to the application, determine the type of oscillator to be used. The factors that account for the complexity and unique characteristics of oscillators are described below [10].

3.3 Oscillator Stability

Oscillator stability can be divided into long term and short term. Long term stability is the relatively slow change in frequency with time; it can be measured easily using a frequency counter. Short term stability is for exceedingly small time periods and must be measured in the frequency domain using a spectrum analyzer or phase noise measuring equipment. Short term stability is discussed under oscillator noise. Long term stability is a simple parameter to compare.

3.3.1 Amplitude Stability and Frequency Stability

Virtually every piece of equipment that uses an oscillator has two stability requirements. Amplitude stability refers to the ability of the oscillator to maintain a constant amplitude in the output waveform. The more constant the amplitude of the output waveform, the better the amplitude stability. Frequency stability refers to the ability of the oscillator to maintain its operating frequency. The less the oscillator varies from its operating frequency, the better the frequency stability. The various factors which affect the stability of oscillator are mentioned below-

- Variations in load, bias, and component characteristics- Load variations can greatly affect the amplitude and frequency stability of the output of an oscillator. Therefore, maintaining the load as constant as possible is necessary to ensure a stable output.
- Transistor biasing - Bias variations affect the operating point of the transistor. These variations may alter the amplification capabilities of the oscillator circuits as well. A well-regulated power supply and a bias-stabilizing circuit are required to ensure a constant, uniform signal output.
- Environmental conditions-As a result of changing temperature and humidity conditions, the value or characteristics of components such as capacitors, resistors, and transistors can change. The changes in these components also cause changes in amplitude and frequency.
- Output power- This is another consideration in the use of oscillators. Generally, high power is obtained at some sacrifice to stability. When both requirements are to be met, a low-power, stable oscillator can be followed by a higher-power Buffer Amplifier. The buffer provides isolation between the oscillator and the load to prevent changes in the load from affecting the oscillator.

3.4 Oscillator Noise AM and FM (phase)

The perfect oscillator produces a signal whose spectrum would consist of a single line of infinitesimal width. No perfect oscillator has yet been discovered, consequently, oscillators have noise spectra in accordance with well established theory. AM noise is generally far enough below FM noise in an oscillator that it is of little concern. FM noise can vary considerably from one manufacturer to another and should not be taken for granted since it can be the limiting factor in applications like narrow band communications links, frequency synthesizers, Doppler radars, etc. It limits the range resolution, sensitivity, and channel spacing of these systems. FM noise may be due to discrete modulation signals such as power line frequencies and mechanical vibrations. These produce discrete sideband noise at the frequency of modulation; they are also

called spurious signals. FM noise can also be due to random type modulation caused by thermal vibrations and flicker noise within the device, the Q of the tank circuit, etc.

3.5 Classification of Oscillators (generators)

Oscillators can be classified in two broad categories which are below-

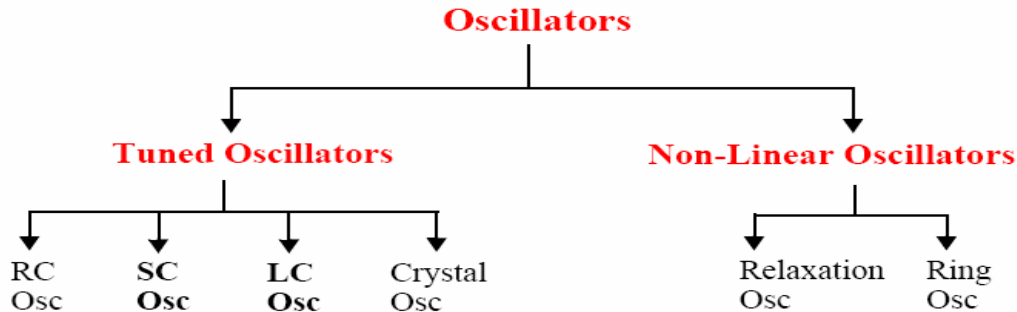


Figure 3.2 Classification of oscillators

3.5.1 Tuned or Linear Oscillators

These employ a positive feedback loop consisting of an amplifier and an RC or LC frequency selective network. The amplitude of generated sine waves is limited, or set using a nonlinear mechanism, implemented either with a separate circuit or using the nonlinearities of the amplifying device itself. These circuits which generate sine waves utilizing resonance phenomena, are known as linear oscillators or sinusoidal oscillators also.

3.5.2 Non-Linear Oscillators

Circuits that generate square, triangular, pulse waveforms are called nonlinear oscillators or function generators. These are basically nonsinusoidal oscillators which employ circuit building blocks known as multivibrator. Relaxation and ring oscillators also fall under this category [18].

3.6 Classification of Oscillators Depending upon their Waveshapes

Oscillators are classified according to the waveshapes they produce and the requirements needed for them to produce oscillations. Oscillators can be classified into two broad categories according to their output waveshapes as below-

- Sinusoidal Oscillators
- Nonsinusoidal Oscillators

3.7 Sinusoidal Oscillators

A sinusoidal oscillator produces a sine-wave output signal. Ideally, the output signal is of constant amplitude with no variation in frequency. The degree to which the ideal is approached depends upon such factors as class of amplifier operation, amplifier characteristics, frequency stability, and amplitude stability. Sine-wave generators produce signals ranging from low audio frequencies to ultrahigh radio and microwave frequencies. There are three types of sinusoidal oscillators which are as below-

- RC Oscillators
- LC Oscillators
- Crystal-Controlled Oscillators

3.7.1 RC Oscillators

Electronic oscillators are often designed around an LC tank circuit, a tuned circuit formed with an inductor and a capacitor. The tuned circuit can also be built by using just resistors and capacitors. Many low-frequency generators use resistors and capacitors to form their frequency-determining networks and are referred to as an RC oscillators. They are widely used in the audio-frequency range. Three configurations of RC oscillators are common which are discussed below.

a) Wien bridge Oscillator

It is a type of electronic oscillator that generates sine waves without having any input source. It can output a large range of frequencies. In this circuit, two RC circuits are used, one with the RC components in series and one with the RC components in parallel. This is often used in audio signal generators because it can be easily tuned using a two-section variable capacitor. The frequency of oscillation is given by:

$$f = 1/(2\pi RC) \dots \dots \dots (3.2)$$

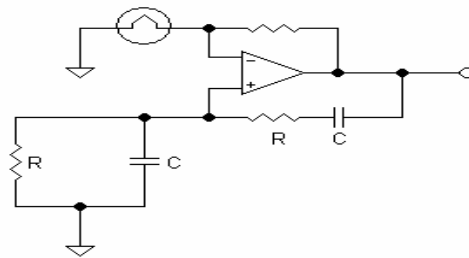


Figure 3.3 Circuit of Wien bridge oscillator

b) Phase shift Oscillator

It is a simple sine wave electronic oscillator. It contains an inverting amplifier, and a feedback filter which 'shifts' the phase by 180 degrees at the oscillation frequency. The filter must be designed so that at frequencies above and below the oscillation frequency, the signal is shifted by either more or less than 180 degrees. This results in constructive superposition for signals at the oscillation frequencies, and destructive superposition for all other frequencies. The most common way of achieving this kind of filter is using 3 cascaded resistor-capacitor filters, which produce no phase shift at one end of the frequency scale, and a phase shift of 270 degrees at the other end [2].

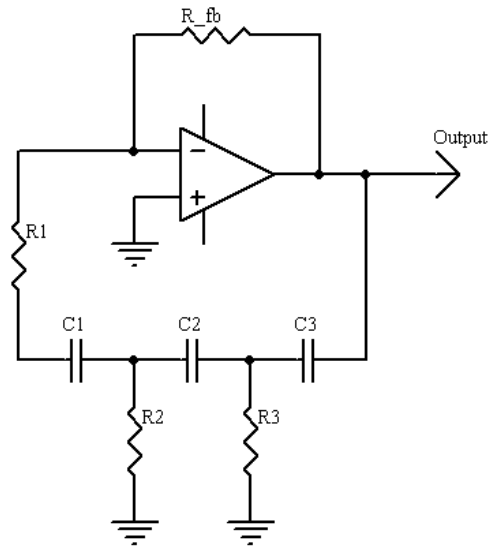


Figure 3.4 Circuit of Phase shift oscillator

In the above figure, if $R_1 = R_2 = R_3 = R$, and $C_1 = C_2 = C_3 = C$, then:

$$f_{\text{Oscillation}} = 1/(2\pi RC\sqrt{6}) \dots \dots \dots (3.3)$$

and Oscillation criteria: $R_{\text{feedback}} = 29R$

c) "Twin-T" Oscillator

The second common design is called a "Twin-T" oscillator as it uses two "T" RC circuits operated in parallel. One circuit is an R-C-R "T" which acts as a low-pass filter. The second circuit is a C-R-C "T" which operates as a high-pass filter. Together, these circuits form a bridge which is tuned at the desired frequency of oscillation.

If they are to produce an undistorted sine wave, RC oscillators usually require some form of amplitude control. Many common designs simply use an incandescent lamp in the feedback circuit. These oscillators take advantage of the fact that the resistance of the tungsten filament increases in proportion to its temperature. Operated well below the point at which the filament actually illuminates, increased amplitude of the feedback signal causes increased current flow in the filament thereby increasing the resistance of the filament. The increased resistance of the filament reduces the feedback signal, limiting the oscillator's signal to the linear range. (That is, clipping is prevented.) More-sophisticated oscillators measure the output level and use this as feedback to control the

gain of the voltage-controlled amplifier within the oscillator. If the amplitude detector has a flat frequency response, then this negative feedback of the amplitude measurement will ensure that the oscillator has a constant output amplitude no matter what frequency it is set to generate.

3.7.2 LC Oscillators

Another type of sine-wave generator uses inductors and capacitors for its frequency-determining network. This type is known as the LC Oscillator. LC oscillators, which use tank circuits, are commonly used for the higher radio frequencies. They are not suitable for use as extremely low-frequency oscillators because the inductors and capacitors would be large in size, heavy, and costly to manufacture. There are several configurations for LC oscillators. The most common are the Hartley, Colpitts and Clapp oscillators.

a) Hartley Oscillator

It is an LC electronic oscillator that derives its feedback from a tapped coil in parallel with a capacitor (the tank circuit). A Hartley oscillator is therefore a type of inductively coupled variable frequency oscillator. Hartley oscillators may be series or shuntfed. The oscillation frequency in hertz(cycles per second) for the circuit in the figure 3.5 is

$$f_0 = \frac{1}{2\pi\sqrt{L_{eq}C}} \dots\dots\dots(3.4)$$

where $L_{eq} = L_1+L_2+2M$ and M is the mutual coupling between inductors L1 and L2.

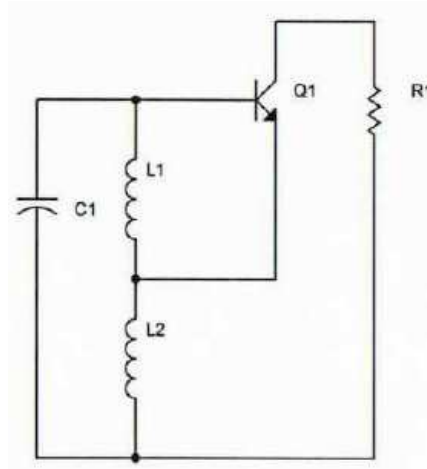


Figure 3.5 Circuit of Hartley LC Oscillator

Advantages

- Frequency varied using a variable capacitor
- Output amplitude remains constant over the tunable frequency range
- Feedback ratio of tapped inductor remains constant

Disadvantages

- Harmonic-rich content
- Not suitable for a pure sine wave

b) Colpitts Oscillator

It is somewhat similar to the shunt fed Hartley circuit except the fact that instead of having a tapped inductor, it utilizes two series capacitors in its LC circuit. With the Colpitts oscillator the connection between these two capacitors is used as the centre tap for the circuit. The oscillation frequency in hertz (cycles per second) for the circuit in the figure 3.6, is

$$f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}} \dots\dots\dots(3.5)$$

where $C_{eq} = C1 C2 / (C1 + C2)$ [25]

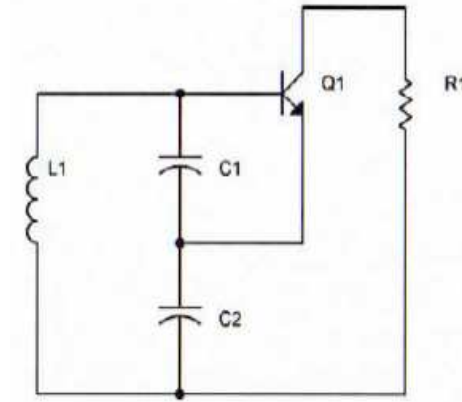


Figure 3.6 Circuit of Colpitts LC Oscillator

Advantages

- *Simplicity and robustness*
- *Capacitively coupled circuit that provides better frequency stability than the Hartley oscillator*

Disadvantages

The voltage divider contains the variable capacitor (either C1 or C2) which causes the feedback voltage to be variable as well, sometimes making the circuit less likely to achieve oscillation over a portion of the desired frequency range.

c) Clapp Oscillator

It is one of several types of electronic oscillator constructed from a transistor (or vacuum tube) and a positive feedback network, the network is comprised of a single inductor and three capacitors, with two capacitors (C1 and C2) forming a voltage divider that determines the amount of feedback voltage applied to the transistor input. The Clapp oscillator is a Colpitts oscillator with an additional capacitor placed in series with the inductor. The oscillation frequency in hertz (cycles per second) for the circuit in the Figure 3.7, is

$$f_0 = \frac{1}{2\pi\sqrt{L\left(\frac{1}{C1} + \frac{1}{C2} + \frac{1}{C3}\right)}} \dots\dots\dots(3.6)$$

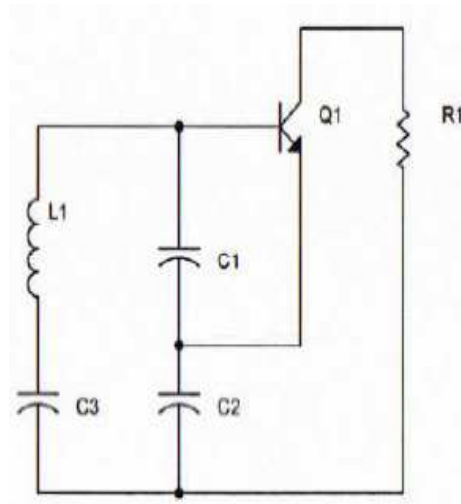


Figure 3.7 Circuit of Clapp LC Oscillator

Advantages

- Preferred over a Colpitts circuit for constructing a variable frequency oscillator (VFO)
- Uses a single variable capacitor to adjust the frequency.
- By using fixed capacitors in the voltage divider and a variable capacitor (C3) in series with the inductor, there is no problem in achieving oscillation over a portion of the desired frequency range.
- Higher loaded Q than the Colpitts oscillator.

The Colpitts and clap oscillators are capacitively coupled circuits that provide better frequency stability than the Hartley oscillator. In each design, a transistor is used as a signal amplifier and a resistor is used as a feedback device.

3.7.3 Crystal-Controlled Oscillators

A third type of sine-wave generator is the Crystal-Controlled Oscillator. A crystal oscillator (sometimes abbreviated to XTAL on schematic diagrams) is an electronic circuit that uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. This frequency is commonly used to keep track of time (as in quartz wristwatches), to provide a stable clock signal for digital integrated circuits, and to stabilize frequencies for radio transmitters. Using an amplifier and feedback, it is an especially accurate form of an electronic oscillator. The crystal used therein is sometimes called a "timing crystal". This oscillator provides excellent frequency stability and is used from the middle of the audio range through the radio frequency range. These are oscillators where the primary frequency determining element is a quartz crystal. Because of the inherent characteristics of the quartz crystal the crystal oscillator may be held to extreme accuracy of frequency stability. Crystal oscillators are usually, fixed frequency oscillators where stability and accuracy are the primary considerations. Temperature compensation may be applied to crystal oscillators to improve thermal stability of the crystal oscillator [25].

Crystal oscillator types and their abbreviations:

- MCXO — microcomputer-compensated crystal oscillator
- OCVCXO — oven-controlled voltage-controlled crystal oscillator
- OCXO — oven-controlled crystal oscillator
- RbXO — rubidium crystal oscillators (RbXO), a crystal oscillator (can be a MCXO) synchronized with a built-in rubidium standard which is run only occasionally to save power
- TCVCXO — temperature-compensated voltage-controlled crystal oscillator
- TCXO — temperature-compensated crystal oscillator
- VCXO — voltage-controlled crystal oscillator

- TSXO — temperature-sensing crystal oscillator, an adaptation of the TCXO

3.8 Nonsinusoidal Oscillators

Nonsinusoidal oscillators generate complex waveforms, such as square, rectangular, trigger, sawtooth, or trapezoidal. Because their outputs are generally characterized by a sudden change, or relaxation, they are often referred to as Relaxation Oscillators. The signal frequency of these oscillators is usually governed by the charge or discharge time of a capacitor in series with a resistor. Some types, however, contain inductors that affect the output frequency. Thus, like sinusoidal oscillators, both RC and LC networks are used for determining the frequency of oscillation. Within this category of nonsinusoidal oscillators are Multivibrators, Blocking Oscillators, Sawtooth Generators and Trapezoidal Generators.

3.8.1 Multivibrators

Multivibrators are circuit which change their state constantly between different states (usually two states) at predefined rate. These are usually used to generate square wave clocksignals, but they can be used also for other applications. These are electronic circuits which are used to implement a variety of simple two-state systems such as oscillators, timers and flip-flops. The most common form is the astable or oscillating type, which generates a square wave - the high level of harmonics in its output is what gives the multivibrator its common name. In its simplest form the multivibrator circuit consists of two cross-coupled transistors. Using resistor-capacitor networks within the circuit to define the time periods of the unstable states, the various types may be implemented. Multivibrators find applications in a variety of systems where square waves or timed intervals are required, but the simple circuits tend to be fairly inaccurate, so are rarely used where precision is required. An integrated circuit multivibrator, the 555, is very common in electronics. It uses a more sophisticated design to overcome some of the precision issues with the simpler circuits.

There are three types of multivibrator circuit:

- astable, in which the circuit is not stable in either state - it continuously oscillates from one state to the other. Another name for this type of circuit is relaxation oscillator.
- monostable, in which one of the states is stable, but the other is not - the circuit will flip into the unstable state for a determined period, but will eventually return to the stable state. Such a circuit is useful for creating a timing period of fixed duration in response to some external event. This circuit is also known as a one shot. A common application is in eliminating switch bounce.
- bistable, in which the circuit will remain in either state indefinitely. The circuit can be flipped from one state to the other by an external event or trigger. Such a circuit is important as the fundamental building block of a register or memory device. This circuit is also known as a flip-flop [2].

3.9 Need of Controllable Oscillator

Most electronic signal processing systems require frequency or time reference signals. To use the full capacity of communication channels, e.g. wireless, wired and optical channels, transmitters modulate the baseband message signal into different parts of the spectrum to exploit better propagation characteristics or to frequency multiplex several messages, and the receivers downconvert them for demodulation. These operations require accurate frequency reference signals. Digital circuits and mixed mode circuits (A/D and D/A converters e.g.) pace and synchronize their operations using a clock signal as a time reference signal. For the lower end of the spectrum one can use the stable properties of quartz crystals as a resonator to build very accurate fixed frequency or time reference signals. For higher frequencies (> few hundred MHz) the quality of the crystal resonators degrades due to physical limitations and material properties. Many communications applications require programmable carrier frequencies and the cost and board space of a multitude of crystals would be prohibitive.

Indirect frequency synthesis techniques based on a phase-locked-loop (PLL) are preferred to generate programmable carriers and RF frequencies. A less accurate RF oscillator whose frequency can be controlled with a control signal is embedded in a feedback loop and its output frequency is locked to an accurate low frequency reference.

These loops are typically implemented as a phase-locked loop as shown in figure 3.8. A phase locked loop consists of a voltage controlled oscillator (VCO), frequency divider, phase detector (PD), charge pump (CP) and lead-lag loop filter; the VCO's output frequency is set to a multiple of the reference oscillators frequency depending on the divider ratios (N & R).

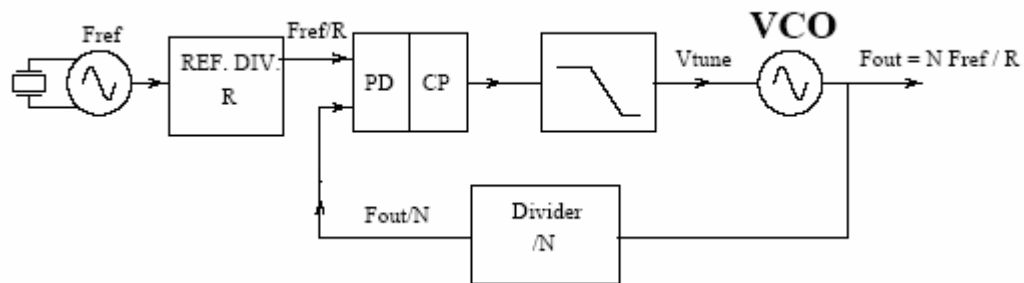


Figure 3.8 A phase locked loop

Two basic types of controlled oscillators exist: voltage controlled oscillators (VCO) with a voltage control signal and current controlled oscillators (ICO) with a current control signal. The main concern here is on VCOs. In some instances like data communications, the data rate is very accurately standardized. Still a local clock signal is derived from the incoming data signal with a clock recovery circuit to track small variations in the senders clock rate and to align the phase of the local clock for optimal data recovery [4]. This again requires an oscillator whose frequency is controllable. Another important application of VCOs is for the modulation or demodulation of frequency or angle modulated carriers. Open loop modulation and demodulation as well as closed loop schemes are very popular for portable wireless handsets.

3.10 Voltage Controlled Oscillators

Voltage-controlled oscillator or VCO is an electronic circuit that uses amplification, feedback, and a resonant circuit to generate a repeating voltage waveform. The frequency, or rate or repetition per unit of time, is variable with an applied voltage, while alternating current audio or other signals may be fed into the VCO to generate frequency modulation (FM). For high-frequency VCOs, the voltage-controlled element is commonly a varicap connected in an ordinary LC oscillator of some form. For low-frequency VCOs,

other techniques can be used. A version using a quartz [crystal](#) is sometimes found in [radio transmitters](#) for frequency-modulating an [input signal](#). The [piezoelectric effect](#) of quartz causes it to vibrate at a very high [frequency](#), producing [radio waves](#). VCOs are also used in the production of [electronic music](#), to generate variable tones.

3.10.1 Design Factors

The design requirements of VCO are:

- Phase stability
- Large electrical tuning range
- Linearity of frequency verses control voltage
- Large gain factor
- Capability of accepting wideband modulation
- Low cost

With respect to digital phones that use these circuits, low power consumption, small size and low fabrication costs are important design factors [6].

3.10.2 Specifications of a VCO

Apart from a controllable frequency, the other requirements for VCOs; the specification sheet of a VCO typically has the following entries:

- **Center Frequency:** It is the output frequency f_0 of the VCO with its control voltage at its center value and is expressed in [Hz].
- **Tuning Range:** It is the range of output frequencies that the VCO oscillates at over the full range of the control voltage.
- **Tuning Sensitivity:** It is the change in output frequency per unit change in the control voltage, typically expressed in [Hz/V]. VCOs intended for frequency synthesis applications can have a nonlinear relationship between control voltage and oscillation frequency so that several values are quoted or min/max boundaries are given. VCOs for (de)modulation will quote the linearity of the tuning input and the bandwidth of the tuning input.

- **Spectral Purity:** It can be specified depending on the application, in the time domain in terms of jitter or in the frequency domain in terms of phase noise or carrier/noise ratio.
- **Load Pulling:** It quantifies the sensitivity of the output frequency to changes in its output load. In some applications the output load of the VCO is switched while the VCO must remain at the same frequency to avoid frequency errors when in open loop or to avoid transients in the PLL. This spec depends strongly on the isolation provided by the output stage in the oscillator.
- **Supply Pulling:** It quantifies the sensitivity of the output frequency to changes in the power supply voltage and is expressed in [Hz/V]. The power up or down of other circuits can create significant transients in the power supply voltage and it is again desirable that the VCO frequency remains undisturbed.
- **Power Consumption:** It specifies the DC power drain by the oscillator and its output buffer circuits.
- **Output Power:** It is the power the oscillator can deliver to a specified load. The variation of the output power over the tuning range is also specified.
- **Harmonic suppression:** It specifies how much smaller the harmonics of the output signal are compared to the fundamental component and is typically expressed in [dBc] [4].

3.11 Classification of VCOs

Oscillators are autonomous circuits that produce a stable periodically time varying waveform. They have at least two states and they cycle through those states at a constant pace. There are three different topologies for controlled oscillators on silicon ICs:

- Ring Oscillators
- Relaxation Oscillators
- Tuned or LC Oscillators

3.11.1 Ring Oscillators

Ring oscillators consist of an odd number of single-ended inverters or an even/odd number of inverters with the appropriate connections and this is described in detail in the next chapter. It is primarily employed in some applications due to its wide tuning-range, high integration and small layout area. The oscillation frequency is directly related to the delay time of each inverter, resulting in high sensitivity to process and temperature variations. Its nonlinear voltage-to-frequency transfer characteristic gives high VCO gain at low frequencies.

3.11.2 Relaxation Oscillators

Relaxation oscillators alternately charge and discharge a capacitor with a constant current between two threshold levels.

3.11.2.1 RC Relaxation Oscillator

It consists of two cross coupled transistors with their emitters connected to two ends of a capacitor [22]. Fig 3.9 shows a bipolar version of the oscillator. Q3 and Q4 are emitter follower buffers. The emitters of Q1 and Q2 are connected to voltage controlled current sources (normally identical bipolar transistors Q7 and Q8). When Q1 is on, its collector voltage holds Q2 off and the emitter current of Q1 charges the capacitor. When the emitter voltage of Q1 rises above two V_{be} drops from V_{cc} Q1 turns off, Q2 turns on and the emitter current of Q2 charges the capacitor. The amount of current that flows into the capacitor is dependent upon the voltage controlled current source (the collector currents of Q7 and Q8).

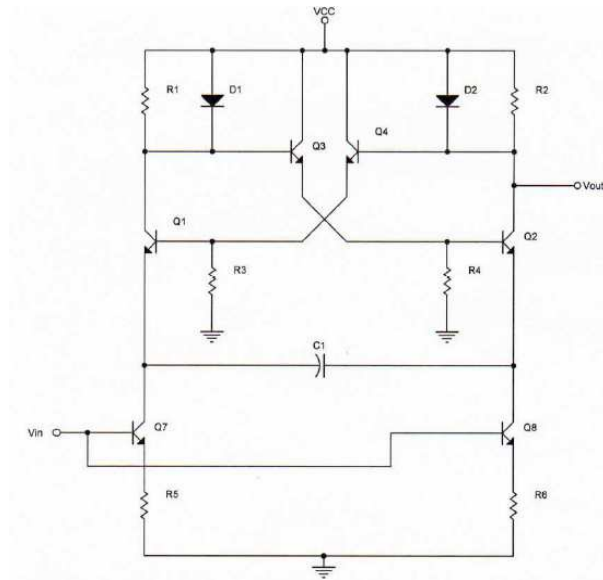


Figure 3.9 An emitter coupled relaxation voltage controlled oscillator

The active components of the simplest relaxation oscillators consist of four transistors. The transistors can either be emitter-coupled or collector coupled. Emitter coupled circuits exhibit sudden voltage jumps at both ends of the capacitor. The voltage jumps create excessive current spikes and possible substrate injection [17]. Sudden voltage jumps do not occur in collector-coupled circuits. Variations of the circuit have used schmitt triggers or SR latches to drive the capacitor. If the output is referenced at one of the collector nodes then the measured signal will be a square wave (with peaks between V_{cc} and ground) whereas the voltage across the capacitor will be a saw-tooth with its mean voltage at zero volts. The output frequency of the relaxation oscillators is also dependent on the circuit temperature. V_{be} is inversely proportional to temperature. Therefore, as capacitor temperature increases the oscillation frequency will increase when the input voltage remains constant. The frequency at which the capacitor voltage oscillates is given by

$$F_{osc} = \frac{I * V_{in}}{4 * V_{be} * C} \dots\dots\dots(3.7)$$

$I (V_{in})$ is the current from voltage controlled current source. V_{be} is known as a swing voltage (the maximum voltage across C before the transistors switch).

Advantages

- *Large frequency tuning range*
- *Low cost*
- *A very linear frequency verses voltage relationship*
- *Requirement of only a single reactive component*
- *All of the components of this oscillator can be fabricated on a single IC*

Disadvantages

- *Poor frequency stability at high frequencies*
- *More susceptible to phase noise compared to LC oscillators*
- *cannot generate a pure sine wave [21].*

Above two realizations are very easy to integrate on a monolithic IC and are very compact. Their frequency is controlled by a current or voltage and linear tuning characteristics can be obtained. Moreover, frequency tuning can be done over several orders of magnitude. These are typically very sensitive to noise in the switching thresholds and charging currents.

3.11.3 Tuned or LC Oscillators

Tuned oscillators contain a passive resonator- LC tank, transmission line resonator, crystal, SAW - that serves as the frequency setting element. They are harder to integrate primarily because of the lack of high quality passive inductors in standard IC technologies and because of their large size. However, they have a much higher frequency stability and spectral purity since it is set by the passive resonator [16]. They generate their AC waveform with the assistance of an inductor–capacitor tank. Feedback to an amplifier is used to help maintain oscillation and to reduce damping. The frequency of the oscillator output is determined by the equation:

$$F_{osc} = \frac{1}{2\pi\sqrt{LC}} \dots\dots\dots(3.8)$$

An input voltage can tune the frequency if a varactor (a semiconductor device with a voltage dependent capacitance) is used in place of the capacitor.

Advantages of LC oscillators

- High phase stability
- Low susceptibility to noise.

Disadvantages of LC oscillators

- Lower tuning range
- Higher cost compared to relaxation oscillators.

3.12 Jitter Noise and Active Components

The most important design consideration is the effect of noise on the circuit. Relaxation oscillators are subject to fluctuations in the period of their output, known as jitter. Jitter limits the frequency range of the oscillator, timing accuracy and signal-to-noise ratio (with respect to frequency translation). As the capacitor is charging, the gain of the voltage sensing devices (the switching transistors) is small but becomes unboundedly large as the switching threshold is approached. This gain amplifies noise on the bias current thereby causing the capacitor to switch at random times. This causes the output to be a randomly pulsewidth modulated waveform. The magnitude of jitter noise is defined as:

$$\text{Jitter} = \sigma(T) / \mu(T) \dots\dots\dots(3.9)$$

$\sigma(T)$ and $\mu(T)$ are the standard deviation and mean of the pulse width respectively [1]. The value of jitter can be shown to be dependent on the design of the oscillator and can be measured using the following equations:

$$\sigma(T) = \alpha * \left(\frac{RC}{I_o - I_r} \right) \sigma(I_n) \dots\dots\dots(3.10)$$

$$\sigma(T) = \alpha * \sqrt{6} * \left(\frac{V_n(rms)}{S} \right) \dots\dots\dots(3.11)$$

α is a constant dependent upon the slope of the capacitor voltage ramp and the rms noise voltage. R is the load resistor of the switching transistor. C is the charging capacitor. I_o is the voltage controlled tail current. $I_r = V_t/2R$ (where V_t is the thermal voltage). $\sigma(I_n)$ is the standard deviation of the noise current. $V_n(rms)$ is the rms of the noise voltage. S is the slope of the capacitor voltage at the switching point. It can be seen that increasing tail current, I_o can minimize jitter noise in a relaxation oscillator. However, this method may conflict with a low power consumption requirement for the circuit.

The active devices used in an oscillator add to the phase noise. The more active components that are used in a circuit, the more susceptible that circuit is to noise. The noise sources in the active devices include their inherent flicker and thermal noise. LC oscillators have an advantage over relaxation oscillator in this respect. The oscillation frequency of the LC circuit is dependent on the passive devices (inductors and capacitors) and a single active transistor as opposed to multiple transistors used by relaxation oscillator.

3.13 Q Factor

The quality factor Q of the oscillator determines the level of damping of the output signal and the susceptibility of the circuit to phase noise. A definition of Q that applies to most oscillators is

$$Q = (\omega_0/2) (d\Phi/d\omega) \dots \dots \dots (3.12)$$

ω_0 is the resonance frequency and $d\Phi/d\omega$ is the slope of phase with respect to frequency [4]. A high Q factor implies that there is small damping factor and the signal is better able to maintain oscillation. If the phase slope is high then a phase shift (as caused by phase noise) in a closed loop system (like a phase lock loop) will force the oscillator to return to the resonance frequency. If the phase slope is low then there is weaker tendency to maintain resonance frequency when phase deviations occur. As a result a high Q helps to make the circuit less susceptible to noise. LC oscillators have a high Q factor by nature of its design: a good quality inductor and a minimal number of active components. LC oscillators have a high Q factor that is typically four times the Q factor of a relaxation oscillator [20]. High frequency applications require oscillators with high Q factors. Traditional relaxation oscillators have been limited in their use at high frequencies due to their lower Q factor and subsequent noise susceptibility therefore LC oscillators have been favored. However large Q inductors have to be used off-chip thereby sacrificing size requirements.

3.14 Design Improvements

Early VCOs were constructed with discrete components and were rarely part of integrated circuits. IC oscillators had poor stability and frequency compared to their discrete counterparts [6]. In the last few years, significant development has been made to improve IC VCO limitations.

3.14.1 Relaxation Oscillators

Early relaxation oscillators had an upper tuning range in the tens of megahertz. Today's circuits have frequency limits in the gigahertz range while still maintaining voltage-to-frequency linearity. This range is made possible with the use of automatic swing control [17]. When voltage across capacitor reaches the switching point, there is a delay before the capacitor starts to charge in the opposite direction. This is due to an inherent delay in the transistors to change states. The delay is dependent upon temperature and process factors. During the delay, the capacitor continues to charge in the same direction. The voltage across the capacitor is no longer fixed at this point and the current-frequency linearity is affected. This limits the maximum frequency that can be reached linearly. The ASC applies a feedback to the VCO that replaces the fixed swing voltage with one that compensates for the swing increase caused by the delay. An applied reference voltage determines the maximum peak of the capacitor voltage. The added feedback stabilizes the peak amplitude allowing the oscillator to achieve a maximum frequency of:

$$f_{lim} = 1/4 * T_d \dots \dots \dots (3.13)$$

T_d is the switching delay of the transistors.

For a given current, oscillation frequency is higher with ASC feedback than without ASC. The signal amplitude is also more stable and the current-frequency is more linear for higher frequencies. For frequencies below the maximum frequency, the circuit is less sensitive to temperature variations and power supply variations (around 1 % frequency change for a 5% power change).

Traditionally relaxation oscillators using CMOS technology have been used for low frequency applications, but submicron MOS processes have allowed CMOS oscillators to

achieve frequencies in the gigahertz range. In order to achieve a higher quality factor, CMOS relaxation oscillators have been designed in the form of ring oscillators. A ring oscillator consists of a number of CMOS delay cells (either single ended or differential inverters) connected in series. The output signal of the n th cell is connected to the input of the 1st cell for feedback. The frequency of the ring oscillator is determined by:

$$F=1/(2*n*T_{delay})\dots\dots\dots(3.14)$$

T_{delay} is the switching delay of a single cell and n is the total number of cells in the circuit. The use of multiple inverter integrators provides a higher Q than for a single stage relaxation oscillator [20]. CMOS VCOs designed as ring oscillators can achieve higher frequencies and better phase noise performance (comparable to monolithic LC oscillators) than other CMOS VCO designs and low power consumption than VCOs designed using compatible technologies.

3.14.2 LC oscillators

One of the drawbacks of the LC oscillator is that early models could not be fully monolithic since inductors could not be fabricated on the chip. The size of the required inductors tended to be too large to fit on ICs therefore they were included as discrete components. This allows circuit to occupy a single chip, however the addition of the active components increases the circuit's susceptibility to phase noise. Larger capacitors and more power are needed to compensate for the noise. Another alternative is to use a bondwire. Bondwire has an associated parasitic inductance of \around 1nH per mm length. This provides finite inductance that can be fabricated on the chip, but great care is needed in fabrication as the bondwires must be kept straight and have a constant separation from each other in order for them to provide the expected inductance [15]. The repeatability of the bondwire technique prevents it from being widely used.

Within the last decade, improvements in integrated circuit fabrication have allowed spiral inductors to be fabricated on ICs. The technique involves laying out two metal layers in the form of a rectangle spiral where each layer is on the either side of silicon substrate. The result has been that LC oscillators have become more compact. The quality factor of

the LC oscillator is limited by the inductors and therefore it is dependent on the fabrication process. The metal traces have a series resistance that affects the inductor's reactance. Also the coil has a parasitic capacitance to the substrate that limits its maximum frequency. The combination of added resistance and capacitance places a maximum limit to the achievable inductance, reduces the quality factor and reduces phase stability of the circuit. These problems are less prominent when the circuit is fabricated with more advanced process technology (such as using etching techniques to remove the silicon substrate) [14]. The available chip area is another limiting factor. For example, if the required inductance demands that the fabricated coils take up an area that does not leave room for the rest of the circuit then the oscillator cannot be fabricated in its entirety on a single chip.

3.15 Applications of VCO

VCOs are used in:

- function generators
- the production of electronic music, to generate variable tones
- phase-locked loops
- frequency synthesizers used in communication equipment
- spread spectrum, RF and wireless systems - In the wireless transmission systems, the VCO is used for the frequency synthesizer to generate the local oscillating signal for the modulation and demodulation of the RF signal [9].
- optical communication systems - In digital optical transmission systems, VCOs are used as the core circuit of the clock recovery circuit, whose output signal is used for data decision and regeneration [13].

Chapter 4

INTRODUCTION TO TANNER TOOL

4.1 Introduction

Tanner Tool is a SPICE Computer Analysis Programmed for Analog Integrated circuits. Tanner Tool consists of the following Engine Machines:

1. S-EDIT (Schematic Edit)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)

Using these Engine tools, SPICE Programmes provides facility to the user to design and simulate new ideas in analog integrated circuits before going to the time consuming and costly process of chip fabrication.

4.2 *S-EDIT (Schematic Edit)*

S-Edit is hierarchy of files, modules and pages. It introduces symbol and schematic modes. S-Edit provides the facility of:

1. Beginning a design
2. Viewing, drawing and editing of objects
3. Design connectivity
4. Properties, net lists and simulations
5. Instance and browser schematic and symbol mode

In S-Edit, the available components from the library can be selected to make the schematic of the desired circuit. It explains the design process in detail in terms of file module operation and module [29]. Effective schematic design requires a working knowledge of the S-Edit design files consist of modules. A module is a functional unit of design such as a transistor, a gate and an amplifier. Modules contain two components:

- a) Primitives – Geometrical objects created with drawing tools.
- b) Instances – References to other modules in file. The instanced module is the original.

Two viewing modes of the S-Edit are:

- a) Schematic mode – This mode helps in creating or viewing a schematic.
- b) Symbol mode – It represents symbol of a larger functional unit such as operational amplifier.

4.3 T-EDIT (Simulation Edit)

The heart of T-Spice operation is the output file (also known as the circuit description, the net list and the input deck). This is a plain text file that contains the device statement and simulation commands, drawn from the SPICE circuit description language with which T-Spice constructs a model of the circuit to be simulated. Input files can be created and modified with any text editor.

T-Spice is a tool used for simulation of the circuit. It provides the facility of

- a) Design Simulation
- b) Simulation commands
- c) Device Statements
- d) User-defined External Models
- e) Small Signal and noise models

T-spice uses Kirchoff's Current Law (KCL) to solve circuit problems. To T-Spice, a circuit is a set of devices attached to the nodes. The voltage at all nodes represents the circuit state. T-Spice solves for a set of node voltage that satisfied KCL (implying that sum of currents flowing into each node is zero).

In order to evaluate whether a set of node voltages is a solution, T-Spice computes and sums all the current flowing out of each device into nodes connected to it (its terminals). The relationship between the voltages at device terminals and the currents through the terminal is determined by the device model for a resistor of resistance R is $I = \Delta V/R$

Where ΔV represents the voltage difference across the device.

4.3.1 DC Operating point analysis

DC operating point analysis finds a circuit's steady-state condition, obtained (in principle) after the input voltages have been applied for an infinite amount of time. The **.include** command causes T-Spice to read in the contents of the model file `ml2_125.md` for the evaluation of transistors `m1n` and `m1p`. This file (which must be in the same directory as `invert1.sp`) consists of two **.model** commands, describing two MOSFET models called `nmos` and `pmos`:

```
.model nmos nmos
+ Level=2 Ld=0.0u Tox=225.00E-10
+ Nsub=1.066E+16 Vto=0.622490 Kp=6.326640E-05
+ Gamma=0.639243 Phi=0.31 Uo=1215.74
+ Uexp=4.612355E-2 Ucrit=174667 Delta=0.0
+ Vmax=177269 Xj=0.9u Lambda=0.0
+ Nfs=4.55168E+12 Neff=4.68830 Nss=3.00E+10
+ Tpg=1.000 Rsh=60 Cgso=2.89E-10
+ Cgdo=2.89E-10 Cj=3.27E-04 Mj=1.067
+ Cjsw=1.74E-10 Mjsw=0.195

.model pmos pmos
+ Level=2 Ld=0.03000u Tox=225.000E-10
+ Nsub=6.575441E+16 Vto=-0.63025 Kp=2.635440E-05
+ Gamma=0.618101 Phi=0.541111 Uo=361.941
+ Uexp=8.886957E-02 Ucrit=637449 Delta=0.0
+ Vmax=63253.3 Xj=0.112799u Lambda=0.0
```

+ Nfs=1.668437E+11 Neff=0.64354 Nss=3.00E+10
+ Tpg=-1.000 Rsh=150 Cgso=3.35E-10
+ Cgdo=3.35E-10 Cj=4.75E-04 Mj=0.341
+ Cjsw=2.23E-10 Mjsw=0.307

ml2_125.md assigns values to various Level 2 MOSFET model parameters for both *n*- and *p*-type devices. When read by the input file, these parameters are used to evaluate Level 2 MOSFET model equations, and the results are used to construct internal tables of current and charge values. Values read or interpolated from these tables are used in the computations called for by the simulation. Two transistors, m1n and m1p, are defined in invert1.sp. These are MOSFETs, as indicated by the key letter m, which begins their names. Following each transistor name are the names of its terminals. The required order of terminal names is: drain–gate–source–bulk. Then the model name (nmos or pmos in this example), and physical characteristics such as length and width, is specified. The **.op** command performs a DC operating point calculation and writes the results to the file specified in the Simulate > Start Simulation dialog. The output file lists the DC operating point information for the circuit described by the input file.

4.3.2 DC Transfer analysis

DC transfer analysis is used to study the voltage or current at one set of points in a circuit as a function of the voltage or current at another set of points. This is done by *sweeping* the source variables over specified ranges, and recording the output. The **.dc** command, indicating transfer analysis, is followed by a list of sources to be swept, and the voltage ranges across which the sweeps are to take place.

For example, for inverter with dc input vin and output out, vin will be swept from 0 to 3 volts in 0.02 volt increments, and vdd will be swept from 2 to 4 volts in 0.5 volt increments. The transfer analysis will be performed as follows: vdd will be set at 2 volts and vin will be swept over its specified range; vdd will then be incremented to 2.5 volts and vin will be reswept over its range; and so on, until vdd reaches the upper limit of its range. The **.dc** command ignores the values assigned to the voltage sources vdd and vin in the voltage source statements, but they must still be declared in those statements. The

results for nodes in and out are reported by the **.print** dc command to the specified destination.

4.3.3 Transient analysis

Transient analysis provides information on how circuit elements vary with time. The basic T-Spice command for transient analysis has three *modes*. In the *default* mode, the DC operating point is computed, and T-Spice uses this as the starting point for the transient simulation.

```
.tran 2n 600n  
.print tran in out
```

For the commands shown above, The **.tran** command specifies the characteristics of the transient analysis to be performed: it will last for 600 nanoseconds, with time steps no larger than 2 nanoseconds..

4.3.4 AC Analysis

AC analysis characterizes the circuit's behavior dependence on small-signal input frequency. It involves three steps: (1) calculating the DC operating point; (2) linearizing the circuit; and (3) solving the linearized circuit for each frequency.

```
Vin1 in1 GND 2  
Vdd Vdd GND 5.0  
vbias vbias GND 0.8  
vdiff in2 in1 -0.0007 AC 1 90  
.ac DEC 5 1 100MEG  
.print ac vdb(out)  
.print ac vp(out)  
.acmodel opamp1m.out {*}
```

For the commands shown above, three voltage sources (besides Vdd) are defined. `vdiff` sets the DC voltage difference between nodes `in2` and `in1` to -0.0007 volts; its AC magnitude is 1 volt and its AC phase is 90 degrees.

- `Vin1` sets node `in1` to 2 volts, relative to GND.
- `vbias` sets node `vbias` to 0.8 volts, relative to GND.

The `.ac` command performs an AC analysis. Following the `.ac` keyword is information concerning the frequencies to be swept during the analysis. In this case, the frequency is swept logarithmically, by decades (DEC); 5 data points are to be included per decade; the starting frequency is 1 Hz and the ending frequency is 100 MHz. The two `.print` commands write the voltage magnitude (in decibels) and phase (in degrees), respectively, for the node `out` to the specified file. The `.acmodel` command writes the small-signal model parameters and operating point voltages and currents for all circuit devices (indicated by the wildcard symbol `*`) to the file `opamp1m.out`. This example will generate two output files: `opamp1.out`, specified by the Simulate > Start Simulation command, and `opamp1m.out`, specified by the `.acmodel` command.

4.3.5 Noise Analysis

Real circuits, of course, are never immune from small, “random” fluctuations in voltage and current levels. In T-Spice, the influence of noise in a circuit can be simulated and reported in conjunction with AC analysis. The purpose of noise analysis is to compute the effect of the noise associated with various circuit devices on an output voltage or voltages as a function of frequency. Noise analysis is performed in conjunction with AC analysis; if the `.ac` command is missing, then the `.noise` command is ignored. With the `.ac` command present, the `.noise` command causes noise analysis to be performed at the same frequencies: starting at 1 Hz, ending at 100 MHz, 5 data points per decade. The `.noise` command takes two arguments: the *output* at which the effects of noise are to be computed, and the *input* at which the noise can be considered to be concentrated for the purposes of estimating the equivalent noise spectral density [28].

4.4 W- EDIT (Waveform Edit)

The ability to visualize the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding and improving these circuits. W-Edit is a waveform viewer that provides ease of use, power and speed in flexible environment designed for graphical data representation. The advantages of W-Edit include;

- a) Tight integration with T-Spice, Tanner EDA's circuit level simulator. W-Edit can chart data generated by T-Spice directly, without modification of the output text data files. The data can also be charted dynamically as it is produced during the simulation.
- b) Chart can automatically configure for the type of data being presented.
- c) A data is treated by W-Edit as a unit called a trace. Multiple traces from different output files can be viewed simultaneously in single or several windows; traces can be copied and moved between charts and windows. Trace arithmetic can be performed on existed tracing to create new ones.
- d) Chart views can be panned back and forth and zoomed in and out, including specifying the exact X-Y co-ordinate range.
- e) Properties of axes, traces, rides, charts, text and colors can be customized.

Numerical data is input to W-Edit in the form of plain or binary text files. Header and comment information supplied by T-Spice is used for automatic chart configuration. Run time update of results is made possible by linking W-Edit to a running simulation in T-Spice. W-Edit saves data with chart, trace, axis and environment settings in files with the WDB (W-Edit Database) [28].

4.5 L-EDIT (Layout Edit)

It is a tool that represents the masks that are used to fabricate an integrated circuit. It describes the layout design in terms of files, cells and mask primitives. On the layout level the component parameters are totally different from schematic level. So, it provides the facility to the user to analyze the response of circuit before forwarding it to the time consuming and costly process of fabrication. There are rules for designing layout diagram

of a schematic circuit using which user can compare the output response with the expected one [28].

4.5.1 L-Edit: An Integrated Circuit Layout Tool

In L-Edit layers are associated with masks used in fabrication process. Different layers can be conveniently represented by different colors and patterns. L-Edit describes a layout design in terms of files, cells, instances and mask primitives. One may load as many files as desired into memory. A file may be composed of any number of sets. These cells may be hierarchically related, as in a typical design, or they may be independent, as in a “library” file. Cells may contain any number or combination of mask primitives and instances of other cells.

Cells: The Basic Building Blocks

The basic building block of the integrated circuit design in L-edit is a cell.

Design layout occurs within cells. A cell can:

- ...Contain part or all of entire design.
- ...Be referenced in other cells as a sub-cell, or instance.
- ...Be made up entirely of instances of other cells.
- ...Contain original drawn objects, or primitives.
- ...Be made up entirely of primitives or a combination of primitives and instances of other cells.

Hierarchy

L-Edit supports fully hierarchical mask design. Cells may contain instances of other cells. An instance is a reference to a cell; should you edit the instanced cell, the change is reflected in all the instances of that cell. Instances simplify the process of updating a design, and also reduce data within the instanced cell— instead, only a reference to the instanced cell is stored, along with the information on the position of instance and on how the instance may be rotated or mirrored. There is no preset limit to the size or complexity

of hierarchy. Cells may contain instances of other cells that in turn contain instances of other cells, to an arbitrary number of levels (subject only to hardware constraints).

L-Edit does not use a “separated” hierarchy: instances and primitives may coexist in the same cell at any level in the hierarchy. Design files are self-contained. The “pointer” to a cell contained in an instance always points to a cell within the same design file. When cells are copied from one file to another, L-Edit automatically copies across any cells that are instanced by the copied cell, to maintain the self-contained nature of the destination file.

Design Rules

Manufacturing constraints can be defined in L-Edit as design rules. Layout can be checked against these design rules.

Design Features

L-Edit is a full-custom mask editor. Manual layout can be accomplished more quickly because of L-Edit’s intuitive user interface. In addition, one can construct special structures to utilize a technology without, worrying about problems caused by automatic transformations. Phototransistors, guard bars, vertical and horizontal bipolar transistors, static structures and Schottky diodes, for example, are as easy to design in CMOS-bulk technology as are conventional MOS transistors.

Floor plans

L-Edit is a manual floor-planning tool. One has the choice of displaying in—in outline, identified only by name, or as fully fleshed-out mask geometry. When he displays his design in outline, he can manipulate the arrangement of the cells in the design quickly and easily to achieve the desired floor plan.

One can manipulate instances at any level in the hierarchy, with insides hidden or displayed, using the same graphical move/select operations or rotation/mirror commands that he use on primitive mask geometry.

Memory Limits

In L-Edit, one can make your design files as large as one like, given available RAM and disk space.

Hard Copy

L-Edit provides the capability to print hard copy of the design. A multistage option allows very large plots to be printed to a specific scale on multiple 8 ½ x 11 inch page. An L-Edit macro is available to support large-format, high-resolution, color plotting on inkjet plotters.

Variable Grid

L-Edit's grid options support lambda-based design as well as micron based and mil-based design.

Error Recovery

L-Edit's error-trapping mechanism catches system errors and in most cases provides a mean to recover without losing or damaging data.

L-Edit Module

...L-Edit™ : a layout editor

...L-Edit □ Extract™: a layout extractor

...L-Edit □ DRC™: a design rule checker

L-Edit is a full featured, high performance, interactive, graphical mask layout editor. L-Edit generates layouts quickly and easily, supports fully hierarchical design, and allows an unlimited number of layers, cells, and level of hierarchy. It includes all major drawing primitives and supports 90°, 45°, and all-angle drawing modes.

L-Edit □ Extract creates SPICE- compatible circuit netlists from L-Edit layouts. It can recognize active and passive devices, sub circuits and the most common device

parameters, including resistance, capacitance, device length, width, and area, and device source and drain area.

L-Edit □ **DRC features user-** programmable rules and handles minimum width, exact width, minimum space, minimum surround, non-exist, overlap, and extension rules. It can handle full chip and region-only DRC. DRC offers Error Browser and Object browser functions for quickly and easily cycling through rule-checking errors [28].

Chapter 5

CMOS VOLTAGE CONTROLLED OSCILLATORS

5.1 Introduction

Oscillators are integral part of many electronic systems. Applications range from clock generation in microprocessors to carrier synthesis in cellular telephones, requiring vastly different oscillators topologies and performance parameters. Robust, high performance oscillator design in CMOS technology continues to pose interesting challenges. This chapter, deals with the analysis and design of CMOS oscillators more specifically voltage controlled oscillators (VCOs). VCOs are perhaps the most ubiquitous element in all communication systems, wired or wireless [19]. In a wireless system the quality of the communication link is determined in large part, by the characteristics of the VCO and in today's wireless communication systems greater frequency range is required by the VCOs. A voltage controlled oscillator or as more commonly known, a VCO, is an oscillator where the control voltage controls the oscillator output frequency. The VCO's output is an AC waveform whose frequency is dependent upon the input voltage. VCO can be built using many circuit techniques.

5.2 Design Methods

There are two methods, which are used here to design CMOS VCOs mentioned below-

- By use of Ring oscillator
- By use of Schmitt trigger

5.3 Design of Ring oscillator

Ring oscillator is a closed-loop cascade connection of any odd number of inverters, where the output node of the last inverter is connected to the input node of the first inverter. Thus the circuit forms a voltage feedback loop and does not have a stable

operating point. The only DC operating point at which the input and output of all the inverters are equal to logic threshold V_{th} , is inherently unstable in the sense that any disturbance in the node voltages would make the circuit drift away from the DC operating point. Such a circuit will oscillate once any of the inverter input and output voltages deviate from the unstable operating point, V_{th} . Therefore, the circuit is called a Ring oscillator. Assuming the inverters are identical, the oscillation frequency is given in equation 5.1,

$$f_{osc} = 1 / (n * (t_{p_{hl}} + t_{p_{lh}})) \dots \dots \dots (5.1)$$

where n is the number of inverters in the ring oscillator and $(t_{p_{hl}} + t_{p_{lh}})$ is the propagation delay time of each inverter. The propagation delay times $t_{p_{hl}}$ and $t_{p_{lh}}$ determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively [27].

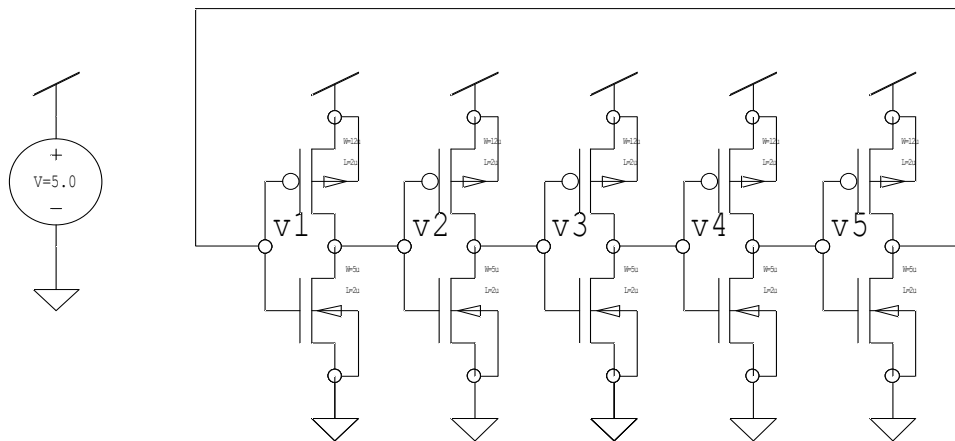


Figure 5.1 Schematic Circuit of Ring oscillator

Ring oscillator shown in figure 5.1 is designed by using five CMOS inverters having $(W/L)_p=12/2$ and $(W/L)_n=5/2$. These specifications are chosen in the relation

$$(W/L)_p = 2.5 (W/L)_n \dots \dots \dots (5.2)$$

by applying condition for symmetric inverter i.e. $K_n=K_p$ where K_n and K_p are transconductance parameters of NMOS and PMOS transistors, respectively. By taking

these values of W/L, if the DC characteristics of CMOS inverter are observed switching point is found to be closer to $2.5(V_{DD}/2=5/2)$.

After selecting values for parameters required, the transient analysis of ring oscillator is done and following waveform is obtained.



Figure 5.2 Waveform obtained after the transient analysis of ring oscillator.

5.3.1 Calculation of oscillation frequency

There are two methods of calculating oscillation frequency of ring oscillator after the simulation.

a) First Method

In this method, propagation delay times t_{phl} and t_{plh} during high-to-low and low-to-high transitions of the output are first calculated from the waveform shown above. t_{phl} is the time delay between the $V_{50\%}$ - transition of the rising input voltage and the $V_{50\%}$ - transition of the falling output voltage. Similarly, t_{plh} is the time delay between the $V_{50\%}$ - transition of the falling input voltage and the $V_{50\%}$ - transition of the rising output voltage.

From the transient analysis of ring oscillator, values of propagation delay times are calculated which are below

$$t_{\text{phl}} = 0.44 \text{ ns and } t_{\text{plh}} = 0.44 \text{ ns}$$

$$\text{So, } f_{\text{osc}} = 1/(n * (t_{\text{phl}} + t_{\text{plh}})) = 227 \text{ MHz}$$

b) Second Method

In this method, time period is directly found by calculating the difference between two points (at 50% of peak-to-peak voltage) on two consecutive rising edges or falling edges of the waveform. From the transient analysis, time period is found as

$$T = 4.42 \text{ ns}$$

As oscillation frequency is inverse of the time period

$$\text{So, } f_{\text{osc}} = 1/T = 226 \text{ MHz}$$

Thus it is proved, that the oscillation frequency found by both methods is the same.

5.4 VCOs using ring oscillator

There are six configurations of VCOs, designed using ring oscillator which are mentioned as below-

- 1) Current Starved VCO (Ist)
- 2) Current Starved VCO (IInd)
- 3) VCO with gates of PMOS transistors grounded
- 4) VCO with PMOS transistors diode connected
- 5) VCO with source voltage applied to both PMOS and NMOS transistors
- 6) VCO with NMOS transistors diode connected

5.5 Current Starved VCO (Ist)

This VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure 5.3, it is observed that MOSFETs M2 and M3

$$C_{tot} = 5/2C'_{ox} (W_pL_p + W_nL_n) \dots \dots \dots (5.4)$$

The time it takes to charge C_{tot} from zero to V_{sp} with the constant current I_{D4} is given by

$$t_1 = C_{tot} * (V_{sp}/I_{D4}) \dots \dots \dots (5.5)$$

while the time it takes to discharge C_{tot} from V_{DD} to V_{sp} is given by

$$t_2 = C_{tot} * (V_{DD} - V_{sp} / I_{D1}) \dots \dots \dots (5.6)$$

If $I_{D4} = I_{D1} = I_D$ (which is labeled as $I_{Dcenter}$ when $V_{inVCO} = V_{DD}/2$), then the sum of t_1 and t_2 is simply

$$t_1 + t_2 = C_{tot} * (V_{DD} / I_D) \dots \dots \dots (5.7)$$

The oscillation frequency of the current starved VCO for N (an odd number ≥ 5) of stages is

$$f_{osc} = 1/(N * (t_1 + t_2)) = I_D / (N * C_{tot} * V_{DD}) \dots \dots \dots (5.8)$$

Equation 5.8 gives the center frequency (f_{center}) of the VCO when $I_D = I_{Dcenter}$.

The VCO stops oscillating, neglecting subthreshold currents, when $V_{inVCO} < V_{THN}$.

Therefore, $V_{min} = V_{THN}$ and $f_{min} = 0$

The maximum VCO oscillation frequency, f_{max} , is determined by finding I_D when $V_{inVCO} = V_{DD}$. At the maximum frequency, $V_{max} = V_{DD}$. The output of the current starved VCO normally has its output buffered through one or two inverters. Attaching a large load capacitance on the output of the VCO can significantly affect the oscillation frequency or lower the gain of the oscillator enough to kill oscillations altogether.

The average current drawn by the VCO is

$$I_{avg} = (N * V_{DD} * C_{tot}) / T = N * V_{DD} * C_{tot} * f_{osc} \dots \dots \dots (5.9)$$

or $I_{avg} = I_D \dots \dots \dots (5.10)$

The average power dissipated by the VCO is

$$P_{avg} = VDD * I_{avg} = VDD * I_D \dots \dots \dots (5.11)$$

If the power dissipated by the mirror MOSFETs, M5 and M6, is also included then the power is doubled from that given by the equation above, assuming that $I_D = I_{D5} = I_{D6}$. For low power dissipation I_D should be kept low, or in other words oscillation frequency should be low [24].

5.5.2 Simulation Results

The specifications chosen for this VCO are same to that of ring oscillator, that is $(W/L)_p = 12/2$ and $(W/L)_n = 5/2$ and supply voltage $VDD = 5V$. The specifications chosen for all VCOs designed using ring oscillator are the same. After choosing the values for the parameters, transient analysis of VCO is done and following is a spice netlist file shown.

T-Spice File

```
* SPICE netlist written by S-Edit Win32 8.10
* Written on Jun 9, 2006 at 16:45:36
* Waveform probing commands
.probe
.options probefilename="NEW.dat"
+ probesdbfile="D:\jayna\current starved\NEW\NEW.sdb"
+ probetopmodule="Module0"

* Main circuit: Module0
M1 N12 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M2 v2 v1 N12 Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M3 v2 v1 N2 Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
```

```

M4 N2 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M5 N5 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M6 N5 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M7 v3 v2 N4 Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M8 N4 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M9 v4 v3 N6 Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M10 N6 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M11 v5 v4 N8 Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M12 N8 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M13 v1 v5 N10 Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M14 N10 vin Gnd Gnd NMOS L=2u W=5u AD=66p PD=24u AS=66p PS=24u
M15 v3 v2 N1 Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M16 N1 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M17 v4 v3 N7 Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M18 N7 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M19 v5 v4 N9 Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M20 N9 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M21 v1 v5 N11 Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
M22 N11 N5 Vdd Vdd PMOS L=2u W=12u AD=66p PD=24u AS=66p PS=24u
v23 vin Gnd 2.5
v24 Vdd Gnd 5.0
.tran/powerup 0.1n 80n start=0
.include "D:\tanner\TSpice91\models\ml2_125.md"
.print tran v(v1) v(v2)
.op

```

- End of main circuit: Module0

Figure 5.4 shows the waveform obtained after simulating T-Spice file, which shows the relation between the voltage and the time period.

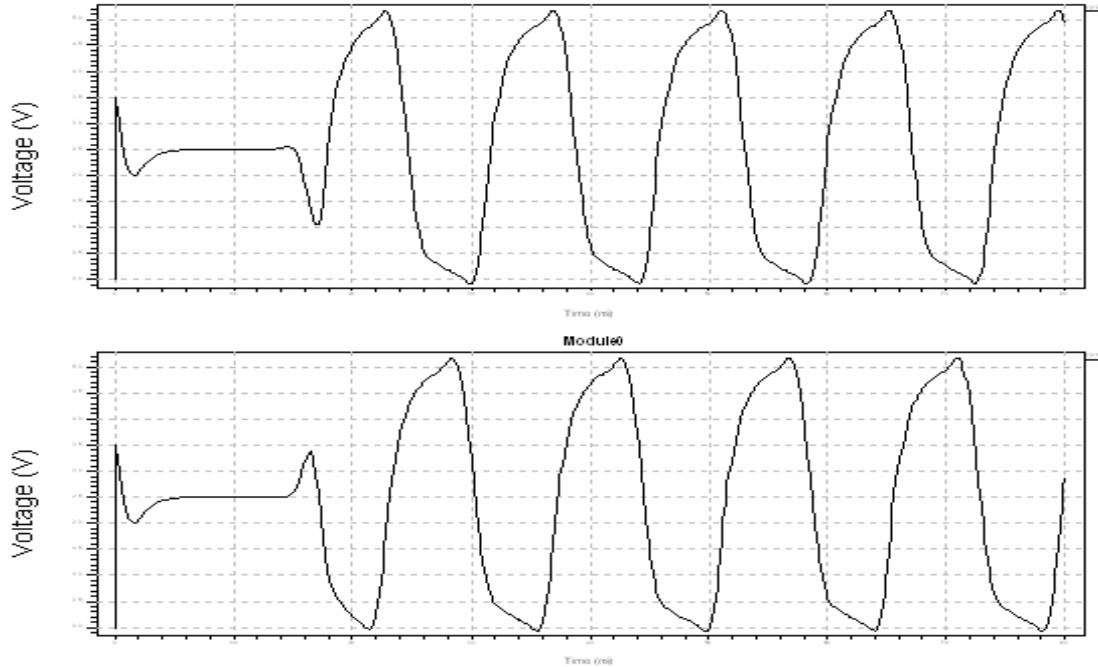


Figure 5.4 Waveform obtained after the transient analysis of Current Starved VCO (Ist) at $V_{in}=2.5V$

The input voltage is varied from 0 to 5V, in steps of 0.5V, and then time period is calculated at different values of voltages from the waveform. After that frequency is calculated by taking inverse of the time period. The Table 5.1 shows values of time periods and frequencies at different values of voltages.

Table 5.1 Simulation Results of Current Starved VCO (Ist).

Input Voltage (V_{in})	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.1 to 5.23	2.56	8.36	119
4.5	-0.1 to 5.20	2.55	8.68	115
4.0	-0.1 to 5.20	2.55	9.13	109
3.5	-0.1 to 5.20	2.55	9.87	101.3
3.0	-0.1 to 5.20	2.55	11.22	89.1
2.5	-0.1 to 5.17	2.56	14.20	70.4
2.0	-0.1 to 5.12	2.6	22.45	44.5
1.5	-0.1 to 5.06	2.56	54.67	18.2
1.0	1.4 to 5.01	2.56	304.28	3.2
0.8	2.3 to 5.0	2.5	1.09(us)	0.91

A graph is plotted between voltage and frequency, which is shown in the figure 5.5 in order to observe the relation between these two quantities.

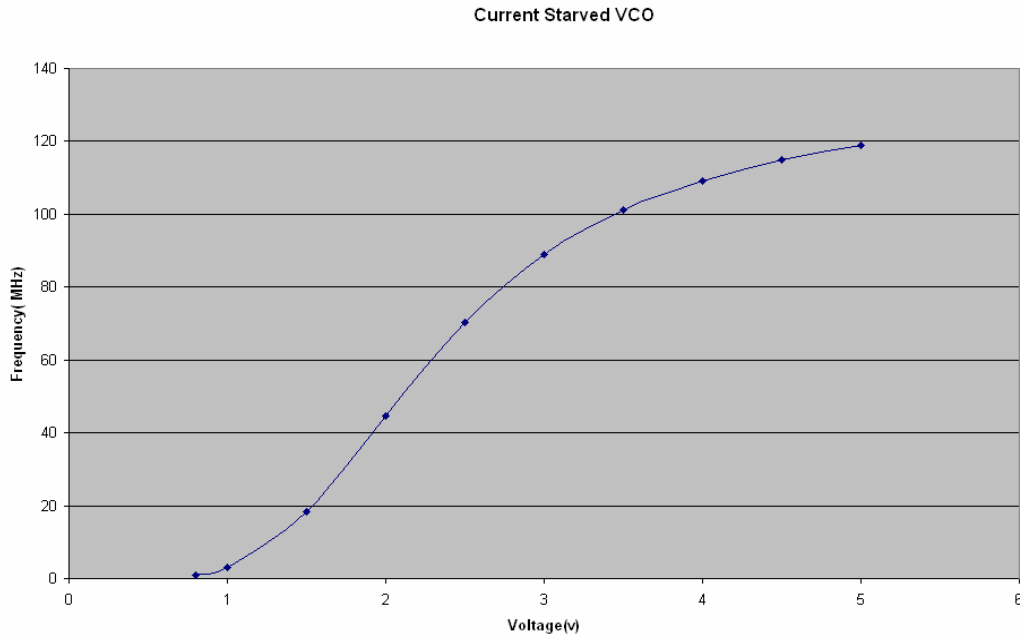


Figure 5.5 Voltage vs. Frequency Plot of Current Starved VCO (Ist).

5.6 Current Starved VCO (IInd)

Its schematic is shown in figure 5.6 which is similar to Current Starved VCO (Ist), except that here, the source voltage is applied to the gates of upper PMOS transistors and gates of all lower NMOS transistors are connected to the gate of transistor M5.

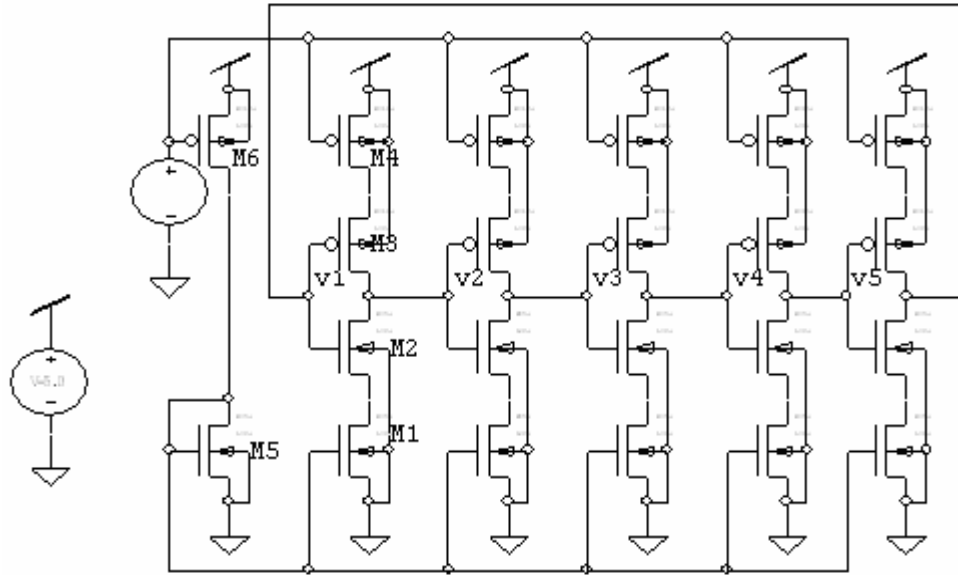


Figure 5.6 Schematic Circuit of Current Starved VCO (IInd).

5.6.1 Simulation Results

Figure 5.7 shows the waveform obtained after the transient analysis is completed.

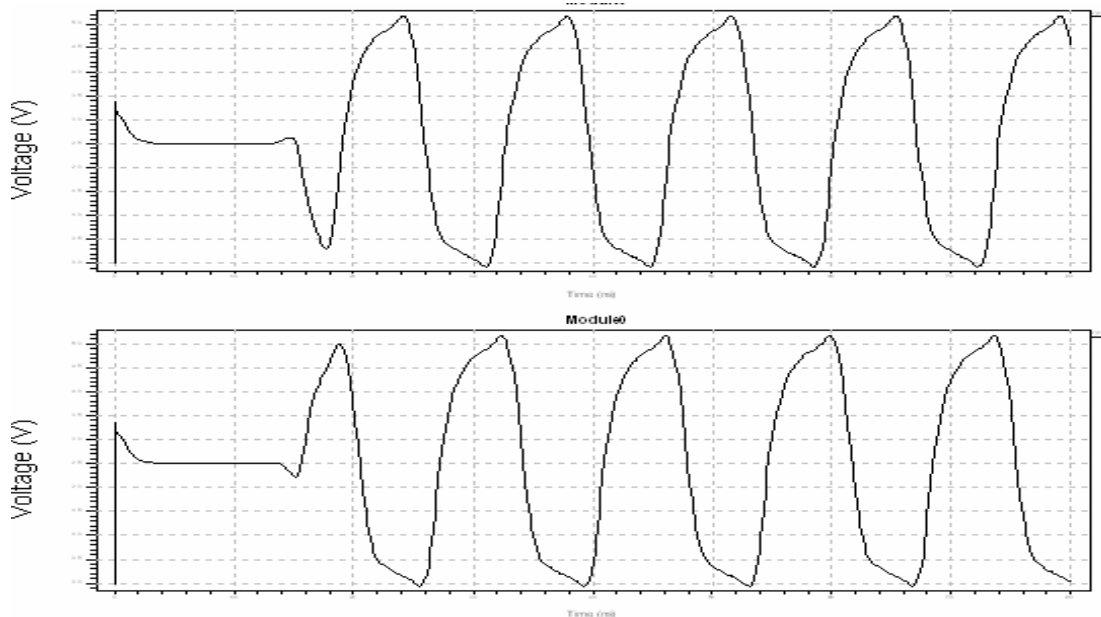


Figure 5.7 Waveform obtained after the transient analysis of Current Starved VCO (IInd) at $V_{in}=2.5V$.

Table 5.2 shows the values of time periods and frequencies at different values of input voltages for this VCO.

Table 5.2 Simulation Results of Current Starved VCO (IInd).

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
3.5	-0.036 to 5.06	2.51	55.47	18
3.0	-0.054 to 5.12	2.53	21.95	45.5
2.5	-0.08 to 5.15	2.53	13.78	72.5
2.0	-0.078 to 5.18	2.55	10.95	91.3
1.5	-0.11 to 5.19	2.54	9.65	103.6
1.0	-0.12 to 5.20	2.54	8.98	111.3
0.5	-0.10 to 5.20	2.55	8.54	117
0.0	-0.11 to 5.21	2.55	8.27	120

Figure 5.8 shows the relation between voltage and frequency of this VCO.

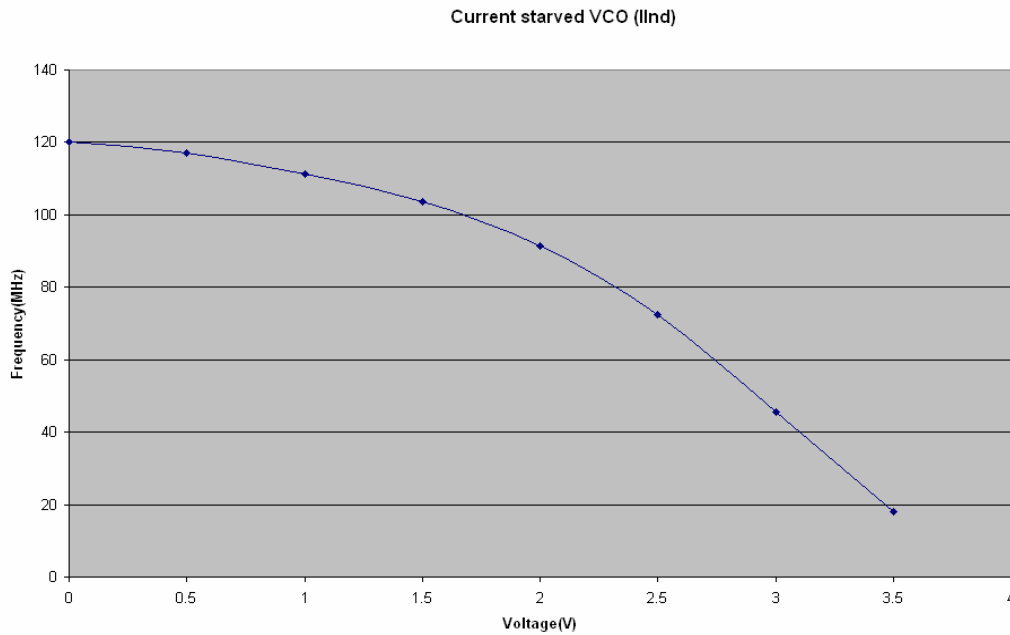


Figure 5.8 Voltage vs. Frequency Plot of Current Starved VCO (IInd).

5.7 VCO with gates of PMOS transistors grounded

In this VCO, the two transistors M5 and M6 are eliminated and gates of the upper PMOS transistors are connected to the ground. The source voltage is applied to the gates of lower NMOS transistors. The schematic is shown below for this VCO.

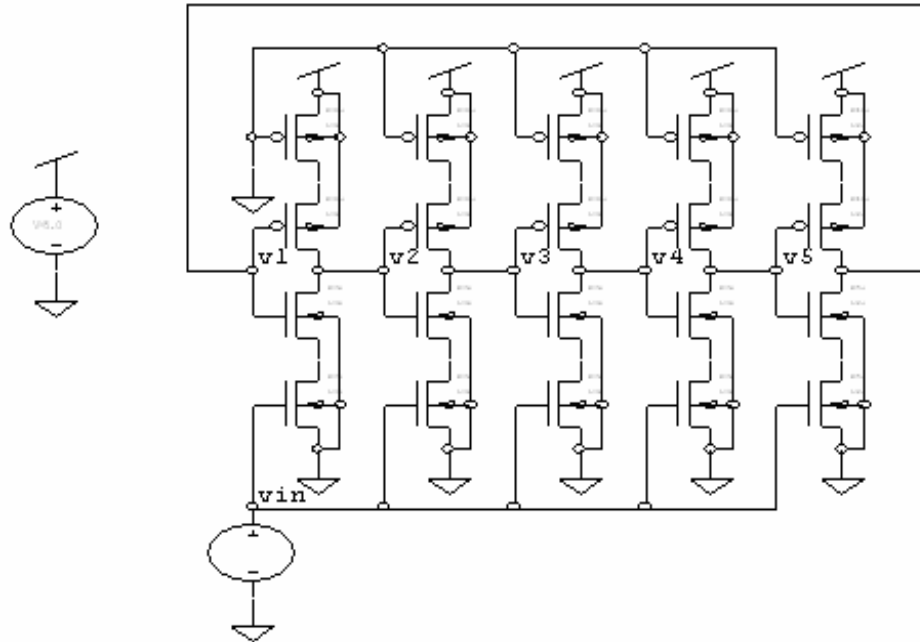


Figure 5.9 Schematic Circuit of VCO with gate of PMOS transistors grounded.

5.7.1 Simulation Results

Figure 5.10 shows the waveform obtained, after the transient analysis is completed.

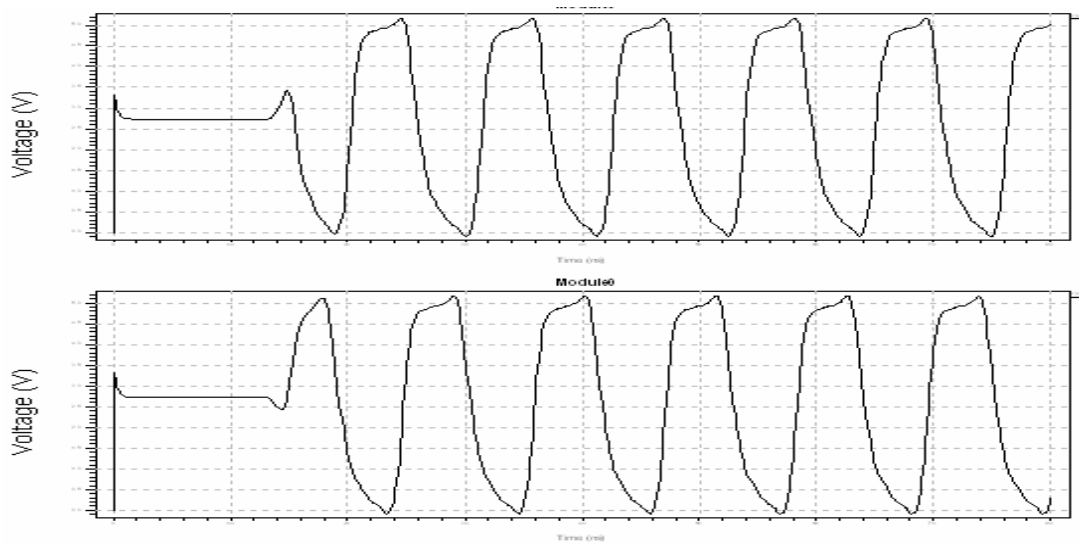


Figure 5.10 Waveform obtained after the transient analysis of VCO with gates of PMOS transistors grounded at $V_{in}=2.5V$.

The Table 5.3 shows the values of time periods and frequencies at different values of voltages for this VCO.

Table 5.3 Simulation Results of VCO with gates of PMOS transistors grounded.

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.1 to 5.2	2.55	7.45	134
4.5	-0.1 to 5.2	2.55	7.69	130
4.0	-0.1 to 5.2	2.55	7.95	125
3.5	-0.1 to 5.2	2.55	.40	119
3.0	-0.1 to 5.2	2.55	9.12	109
2.5	-0.1 to 5.2	2.55	10.89	91
2.0	-0.1 to 5.1	2.5	15.40	64
1.5	-0.1 to 5.0	2.45	27.53	36.14
1.0	1.4 to 5.0	3.2	66.95	14
0.8	2.3 to 5.0	3.625	153.29	6.52

Figure 5.11 shows the relation between voltage and frequency of this VCO.

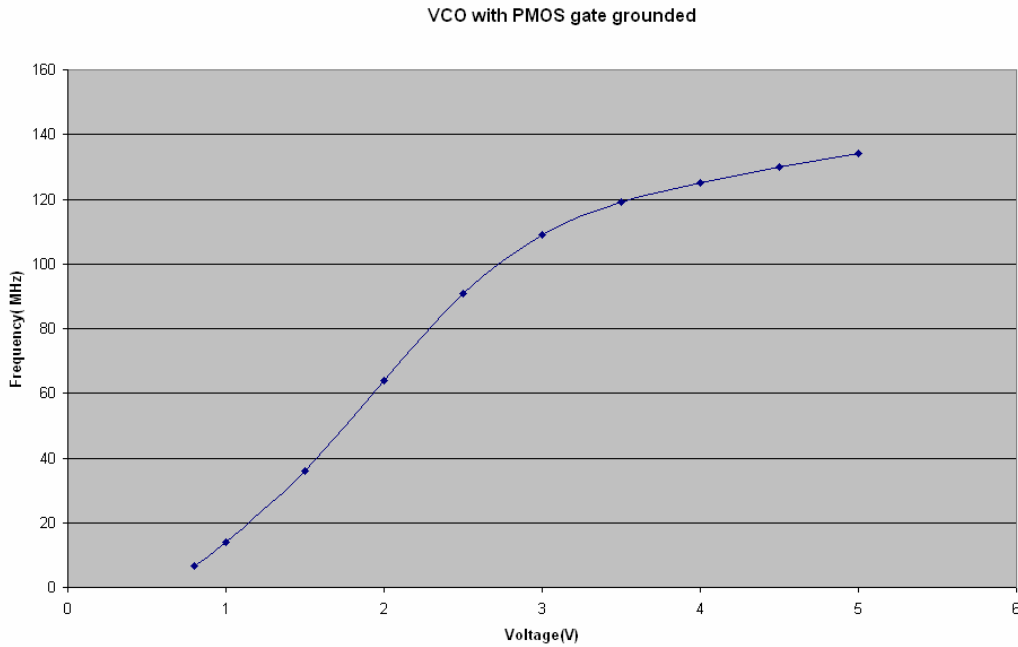


Figure 5.11 Voltage vs. Frequency Plot of VCO with gates of PMOS transistors grounded.

5.8 VCO with PMOS transistors diode connected

In this VCO, the two transistors M5 and M6 are eliminated and gates of upper PMOS transistors are connected to their drains. The source voltage is applied to the gates of lower NMOS transistors.

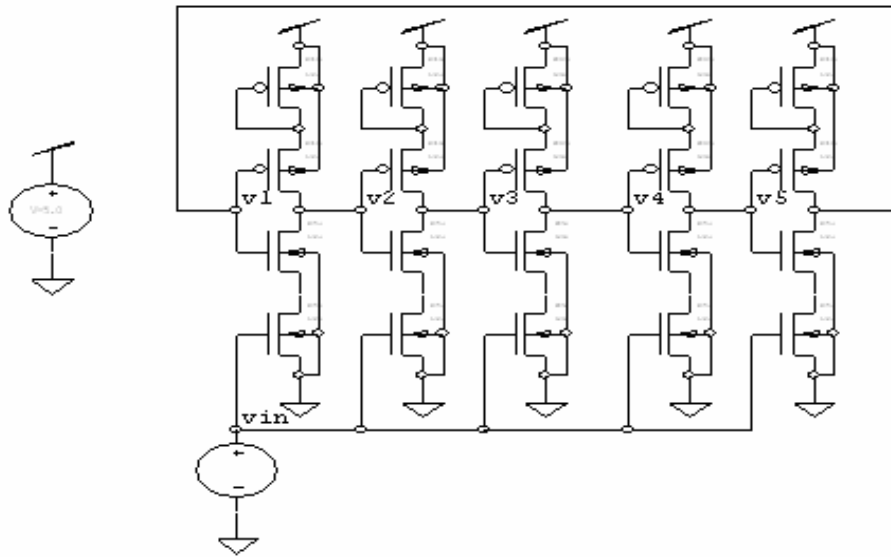


Figure 5.12 Schematic Circuit of VCO with PMOS transistors diode connected

5.8.1 Simulation Results

Following waveform is obtained, after the transient analysis is done.

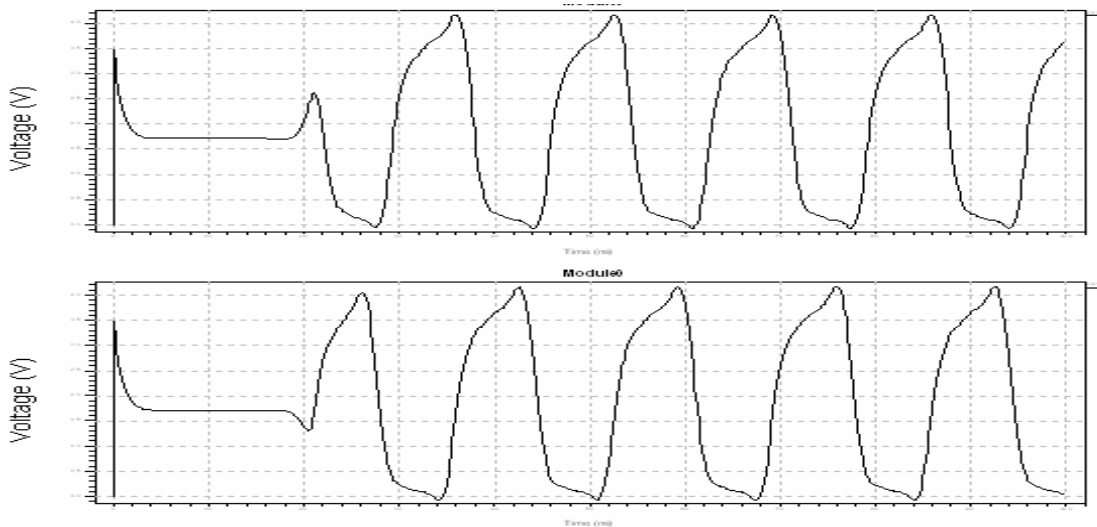


Figure 5.13 Waveform obtained after the transient analysis of VCO with PMOS transistors diode connected at $V_{in}=2.5V$

The Table 5.4 shows the values of time periods and frequencies at different values of voltages for this VCO.

Table 5.4 Simulation Results of VCO with PMOS transistors diode connected

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.1 to 4.1	2.0	13.34	74
4.5	-0.1 to 4.1	2.0	13.66	73
4.0	-0.1 to 4.1	2.0	14.03	71
3.5	-0.1 to 4.1	2.0	14.57	68
3.0	-0.1 to 4.1	2.0	15.33	65
2.5	-0.1 to 4.1	2.0	16.66	60
2.0	-0.1 to 4.2	2.05	20.15	49
1.5	-0.1 to 4.3	2.1	36.03	27
1.0	-0.1 to 4.3	2.1	116.06	8
0.8	0.9 to 4.3	2.6	234.45	4.2

Figure 5.14 shows the relation between voltage and frequency of this VCO.

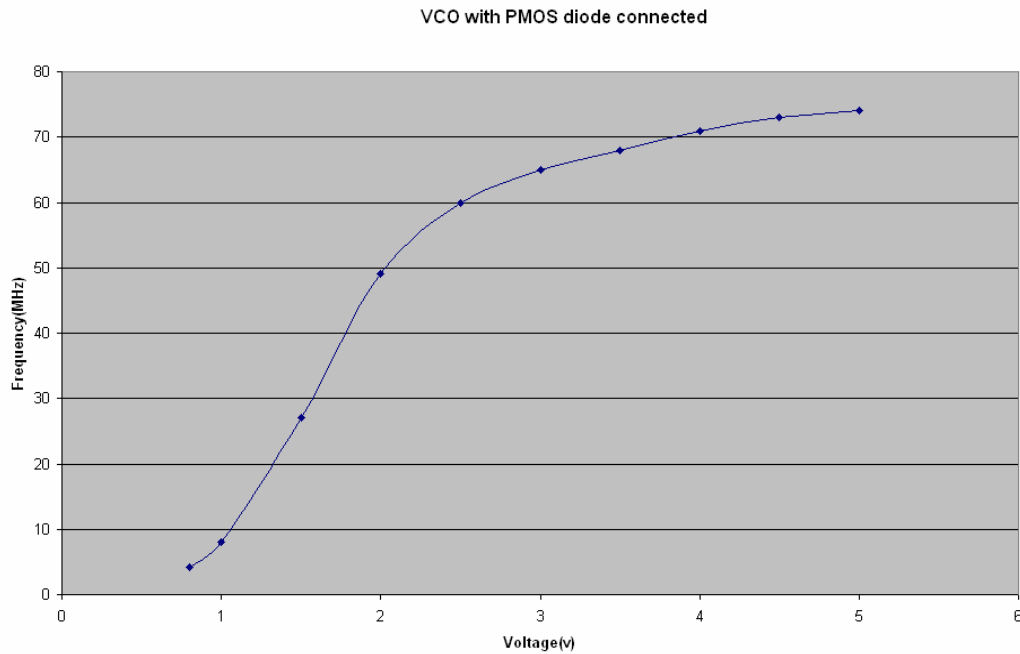


Figure 5.14 Voltage vs. Frequency Plot of VCO with gates of PMOS transistors diode connected

5.9 VCO with voltage applied to both PMOS and NMOS transistors

In this VCO, the two transistors M5 and M6 are eliminated and the source voltage is applied to the gates of both lower NMOS transistors and upper PMOS transistors.

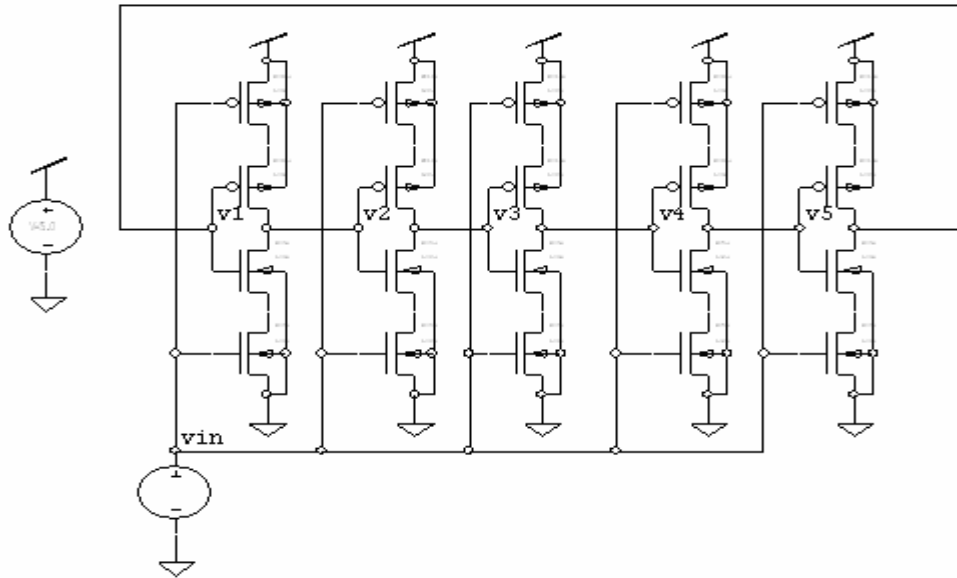


Figure 5.15 Schematic Circuit VCO with voltage applied to both PMOS and NMOS transistors

5.9.1 Simulation Results

Figure 5.16 shows the waveform obtained, after the transient analysis is completed.

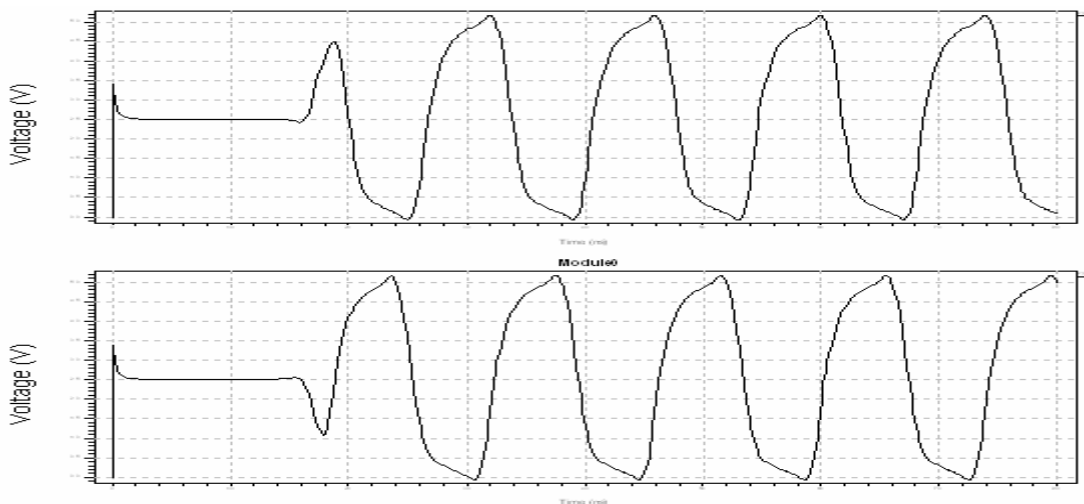


Figure 5.16 Waveform obtained after the transient analysis of VCO with voltage applied to both PMOS and NMOS transistors $V_{in}=2.5V$

The Table 5.5 shows the values of time periods and frequencies at different values of voltages for this VCO.

Table 5.5 Simulation Results of VCO with voltage applied to both PMOS and NMOS transistors

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
4.3	0.0 to 1.17	0.585	198.64	5
4.0	0.033 to 2.32	1.17	27.22	36.7
3.5	0.026 to 4.54	2.283	23.04	43.4
3.0	-0.034 to 5.1	2.53	16.60	60.2
2.5	-0.056 to 5.15	2.547	14.02	71.3
2.0	-0.059 to 5.11	2.52	17.47	57.2
1.5	-0.01 to 5.03	2.51	29.82	33.5
1.0	1.35 to 4.94	3.145	69.60	14.3
0.8	2.26 to 4.97	3.615	153.86	6.4
0.6	2.88 to 4.98	3.93	498.14	2
0.4	3.26 to 4.98	4.12	1.28(us)	0.78

Figure 5.17 shows the relation between voltage and frequency of this VCO.

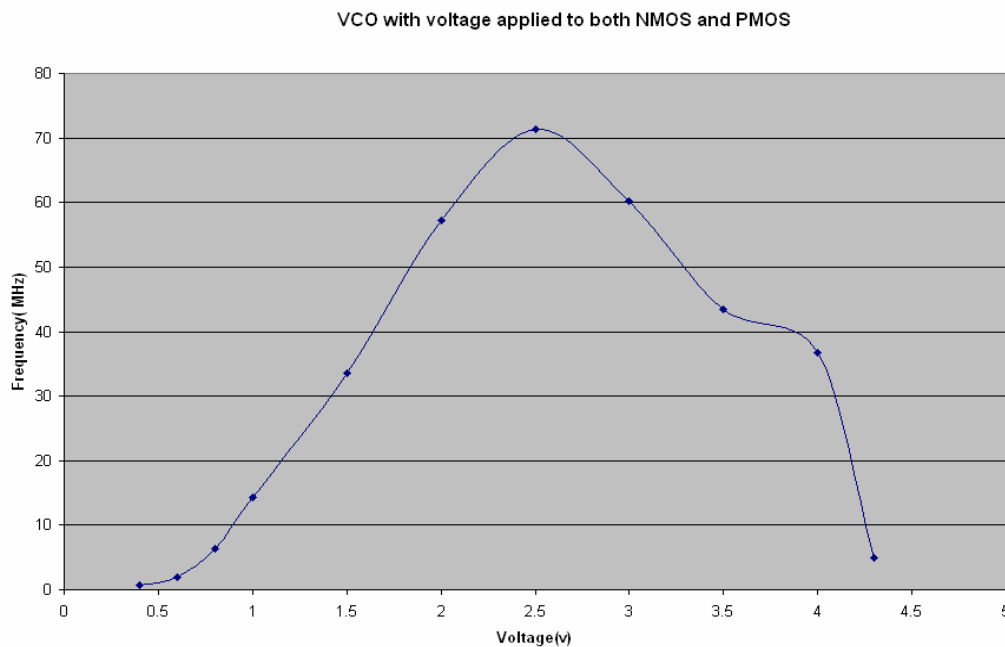


Figure 5.17 Voltage vs. Frequency Plot of VCO with with voltage applied to both PMOS and NMOS transistors

5.10 VCO with NMOS transistors diode connected

In this VCO, the two transistors M5 and M6 are eliminated and gates of lower NMOS transistors are connected to their drains. The source voltage is applied to the gates of upper PMOS transistors.

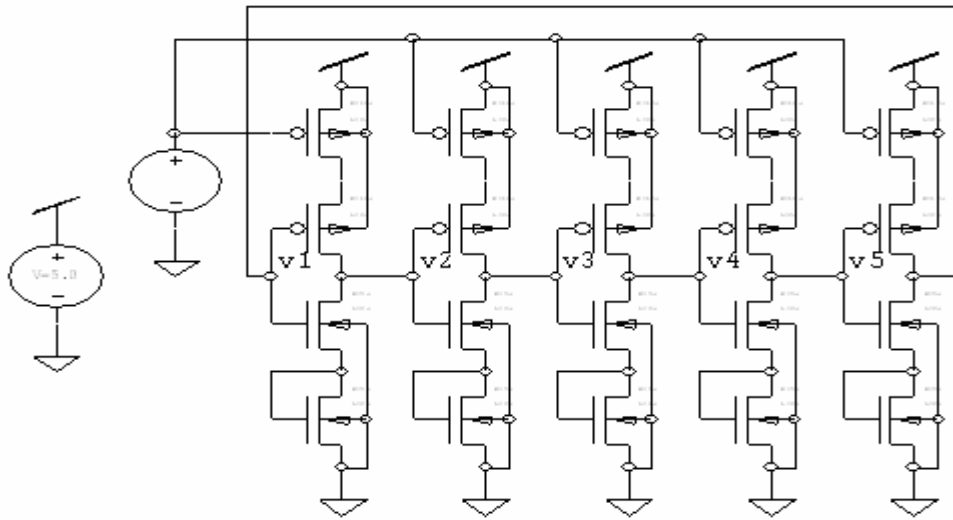


Figure 5.18 Schematic Circuit of VCO with NMOS transistors diode connected

5.10.1 Simulation Results

Following waveform is obtained, after the transient analysis is done.

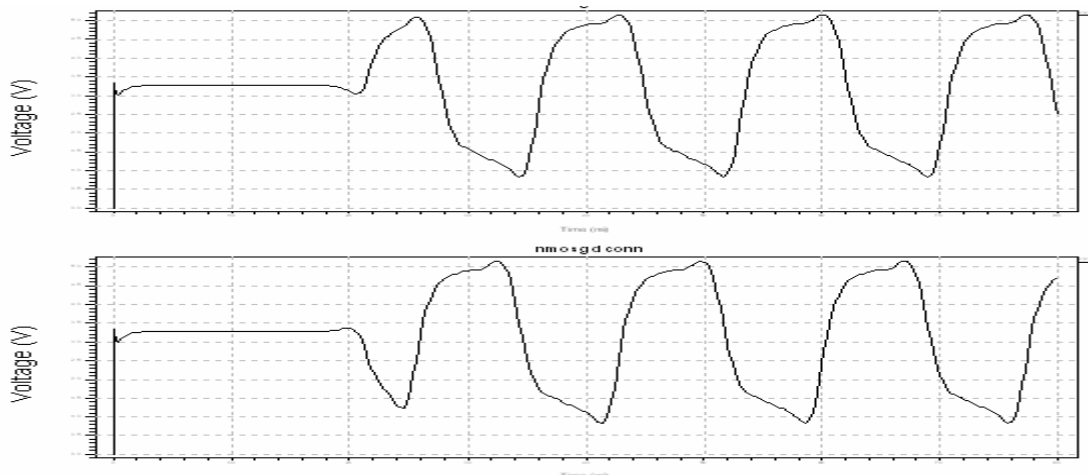


Figure 5.19 Waveform obtained after the transient analysis of VCO with NMOS transistors diode connected $V_{in}=2.5V$

The Table 5.6 shows the values of time periods and frequencies at different values of voltages for this VCO.

Table 5.6 Simulation Results of VCO with NMOS transistors diode connected

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
4.3	0.6 to 2.1	1.35	247.29	4
4.0	1.0 to 3.86	2.43	55.56	17
3.5	0.8 to 5.1	2.95	34.17	29
3.0	0.8 to 5.15	2.975	20.60	48
2.5	0.82 to 5.16	2.99	17.27	57
2.0	0.82 to 5.16	2.99	15.92	62
1.5	0.82 to 5.16	2.99	15.18	65
1.0	0.84 to 5.16	3.0	14.64	68
0.8	0.84 to 5.16	3.0	14.48	69
0.6	0.84 to 5.16	3.0	14.32	69.8
0.1	0.84 to 5.16	3.0	14.01	71

Figure 5.20 shows the relation between voltage and frequency of this VCO.

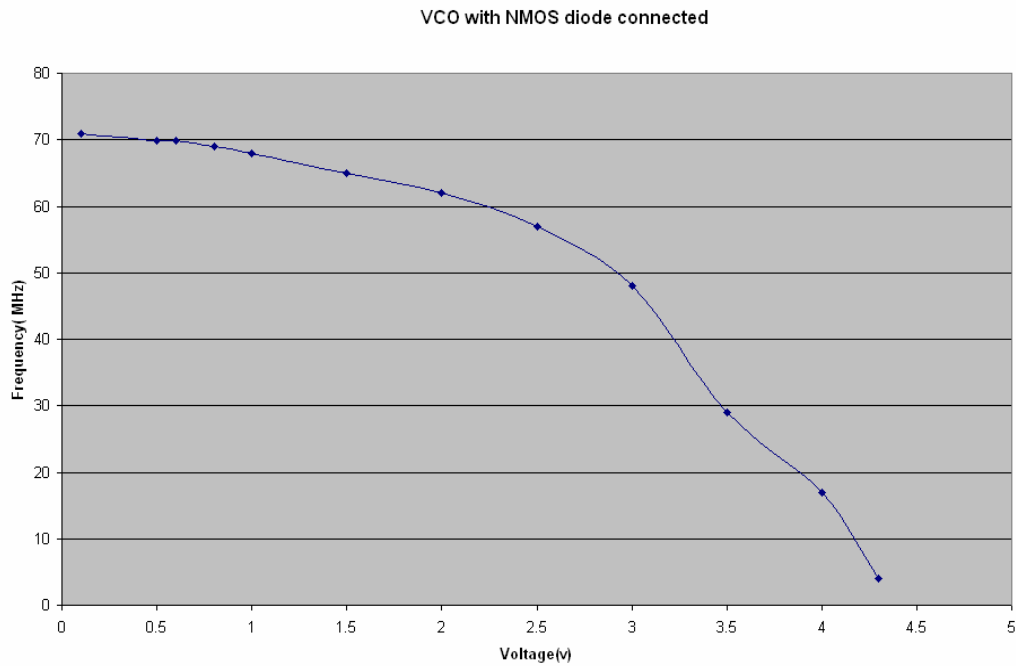


Figure 5.20 Voltage vs. Frequency Plot of VCO with NMOS transistors diode connected

5.11 Comparison of all VCOs designed using ring oscillator

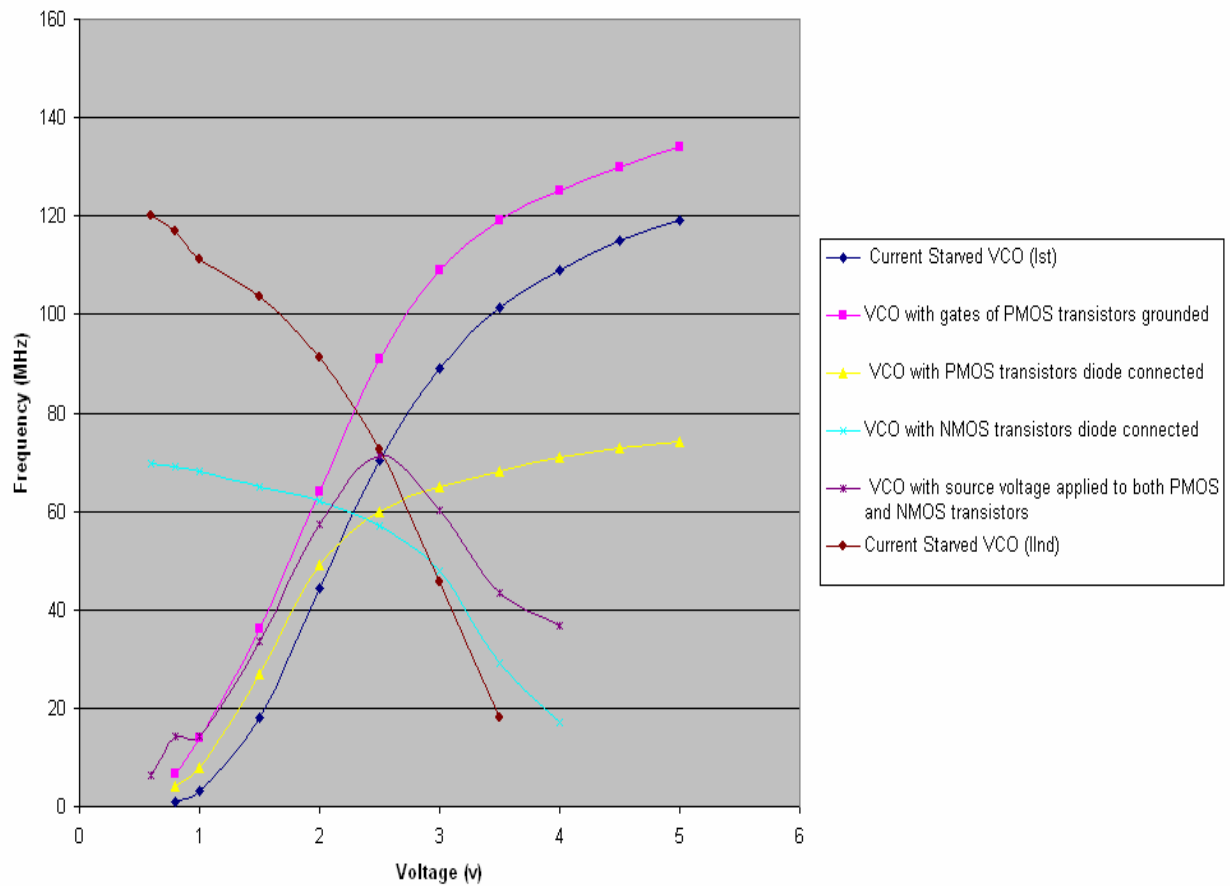


Figure 5.21 Voltage vs. Frequency Plot of all VCOs designed using ring oscillator

Figure 5.21 shows the comparison of all VCOs configurations, designed using ring oscillator in terms of linearity.

5.11.1 Conclusion

From the graph showing comparison of all configurations, it is observed that three VCOs - Current Starved VCO (Ist), VCO with PMOS gate grounded and VCO with PMOS diode connected have linear relationship between voltage and frequency means if voltage is increased, frequency is also increased. In VCO with voltage applied to both NMOS and PMOS, frequency is firstly increasing with increasing voltage, but after a point, it begins

to decrease as voltage is increased. No linearity is observed in this VCO. In rest of two VCOs - Current Starved VCO (IInd) and VCO with NMOS diode connected, it is observed that the voltage and frequency are varying in inverse relationship. Table 5.7 shows the frequency range for each VCO in which the linearity is present.

Table 5.7 Comparison of all VCOs on the basis of linearity

VCO	Frequency Range (MHz)
Current Starved VCO (Ist)	18.2-70.4
Current Starved VCO (IInd)	18-72.5
VCO with gates of PMOS transistors grounded	36-91 and 125-134
VCO with PMOS transistors diode connected	65-71
VCO with voltage applied to both NMOS and PMOS	No linearity
VCO with NMOS diode connected	62-68

From the Table 5.7, it is observed that Current starved VCO (Ist) has the linearity in maximum frequency range.

The layouts of these three VCOs which have obtained direct relationship between voltage and frequency - Current Starved VCO (Ist), VCO with PMOS gate grounded and VCO with PMOS diode connected are drawn and then extracted and simulated to check whether these are showing same results as obtained from their schematic circuits.

5.12 Layouts and their Simulation Results

5.12.1 Layout and Simulation results of Current Starved VCO (Ist)

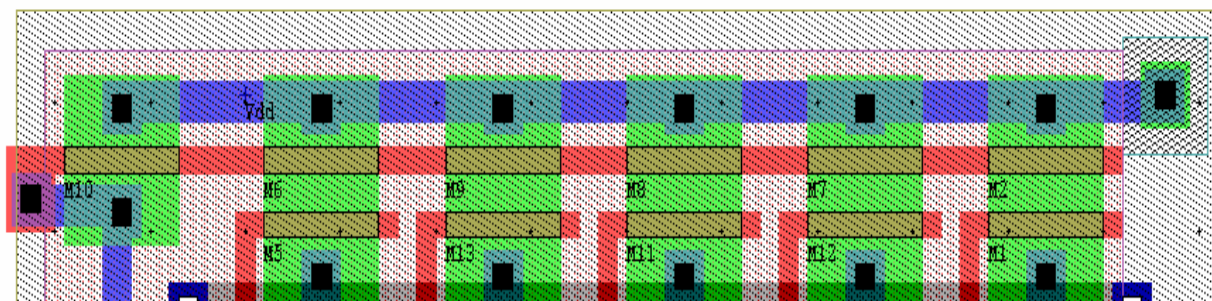


Figure 5.22 Layout of Current Starved VCO (Ist)

Table 5.8 shows the simulation results obtained by extraction and simulation of layout of Current Starved VCO (Ist).

Table 5.8 Simulation Results from the Layout of Current Starved VCO (Ist)

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.063 to 5.11	2.52	13.86	72
4.5	-0.062 to 5.11	2.52	14.44	69.2
4.0	-0.060 to 5.11	2.52	15.2	65.7
3.5	-0.057 to 5.10	2.52	16.51	60.5
3.0	-0.054 to 5.10	2.52	18.95	52.7
2.5	-0.046 to 5.09	2.52	24.35	41.06
2.0	-0.034 to 5.06	2.51	38.98	25.6
1.5	-0.021 to 5.03	2.50	94.21	10.6
1.0	-0.0178 to 5.0	2.49	505.07	1.98

A graph is plotted between voltage and frequency, which is shown in the figure 5.23 in order to observe the relation between these two quantities.

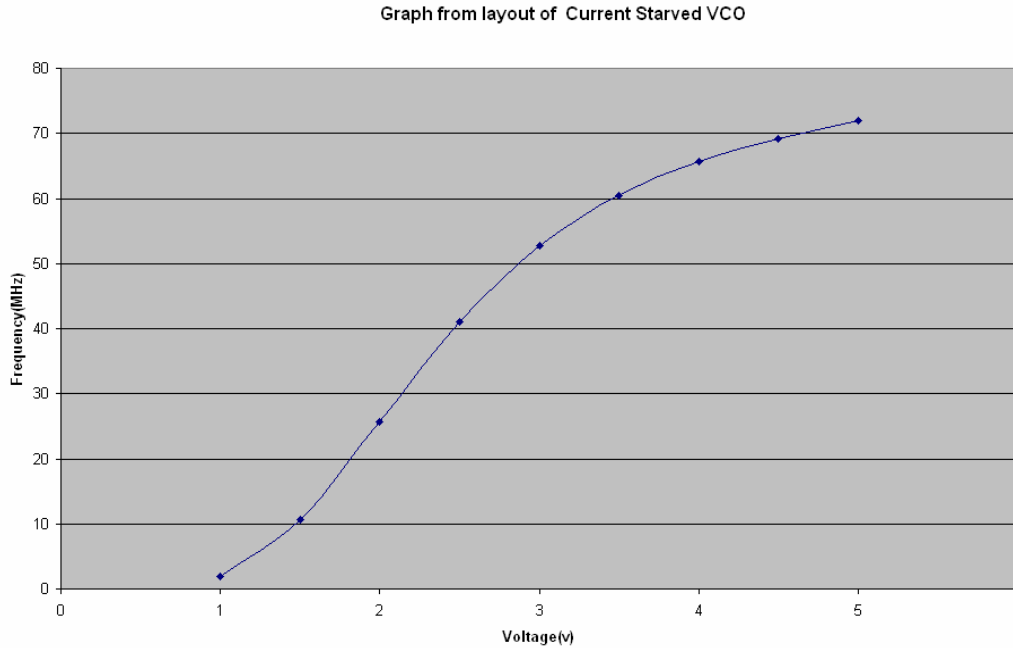


Figure 5.23 Voltage vs. Frequency Plot from Layout of Current Starved VCO (Ist)

By comparing the above layout graph of Current Starved VCO (Ist) with its schematic graph, it is observed that the plot from layout shows same relationship between voltage and frequency as found in the schematic plot, with the exception that here the maximum frequency is decreased from 119 MHz to 72 MHz. This is due to the parasitic capacitances, which increases the time period of waveform obtained after the simulation of the layout and inturn decreases the frequency.

5.12.2 Layout and Simulation results of VCO with gates of PMOS transistors grounded

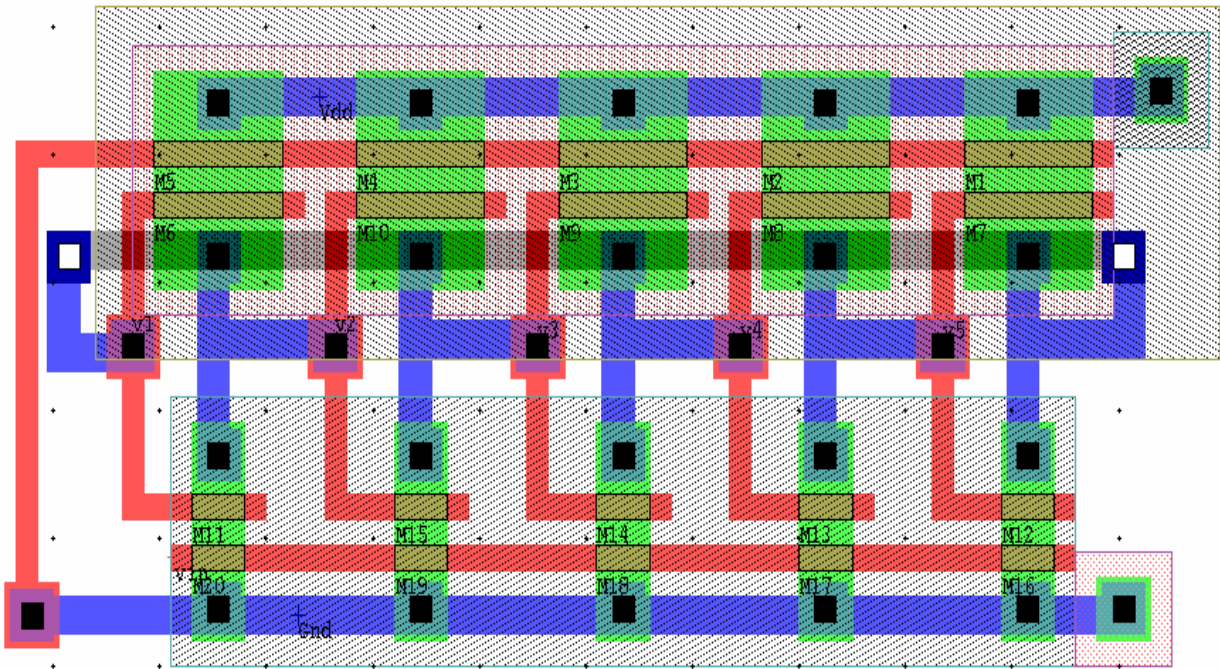


Figure 5.24 Layout of VCO with gates of PMOS transistors grounded

Below is the Table, which shows the simulation results obtained by extraction and simulation of the layout in figure 5.24.

Table 5.9 Simulation Results from the Layout of VCO with gates of PMOS transistors grounded

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.062 to 5.1	2.51	12.69	78.8
4.5	-0.062 to 5.1	2.51	13.08	76.4
4.0	-0.061 to 5.1	2.51	13.56	73.7
3.5	-0.059 to 5.09	2.51	14.33	69.7
3.0	-0.056 to 5.09	2.51	15.63	63.9
2.5	-0.049 to 5.07	2.50	19.14	52.5
2.0	-0.038 to 5.04	2.49	27.37	36.5
1.5	-0.007 to 5.0	2.49	50.06	19.9
1.0	0.95 to 4.96	2.95	134.13	7.45

A graph is plotted between voltage and frequency, which is shown in the figure 5.25 in order to observe the relation between these two quantities.

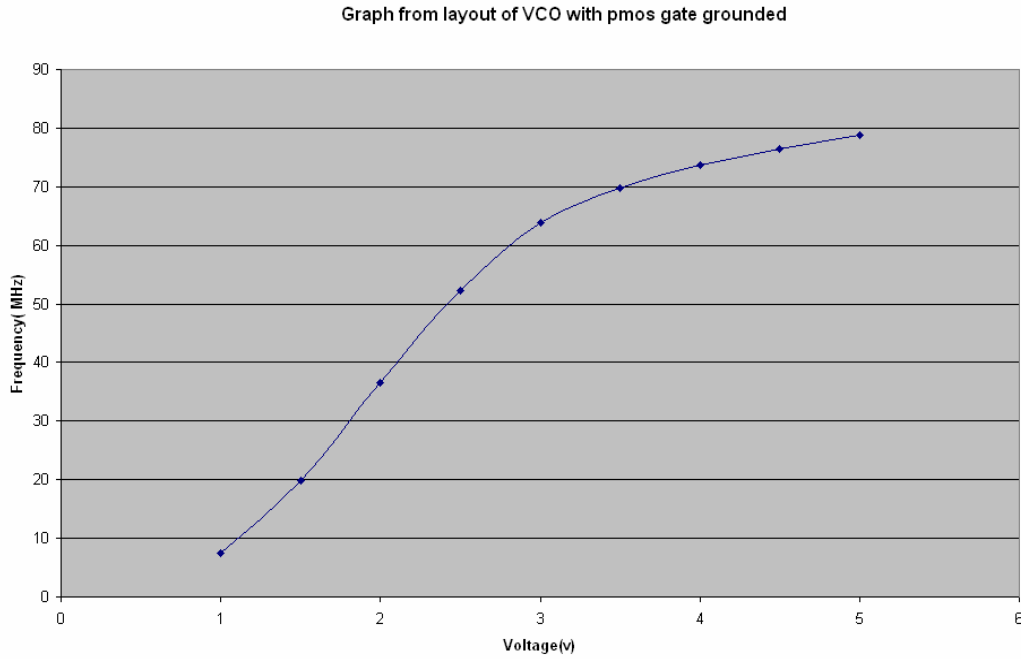
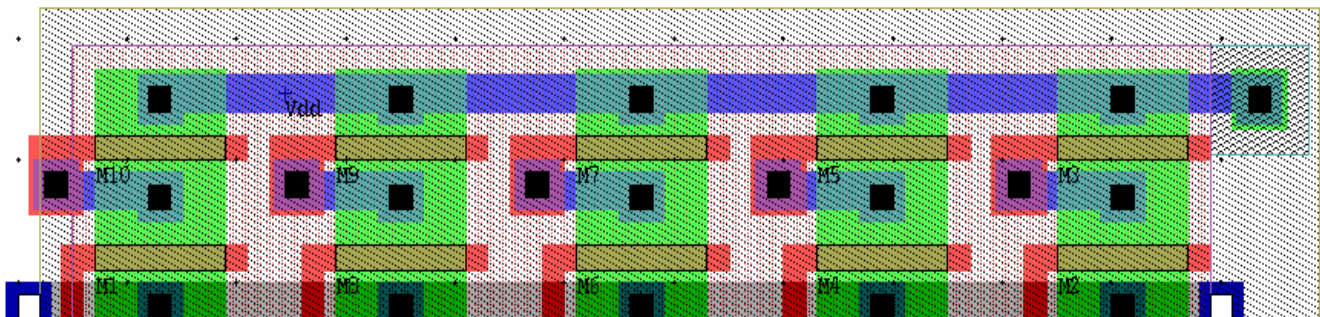


Figure 5.25 Voltage vs. Frequency Plot from layout of VCO with gates of PMOS transistors grounded

Comparison of the above layout graph of VCO with its schematic graph, shows same relationship between voltage and frequency with the exception that here the maximum frequency is decreased.

5.12.3 Layout and Simulation results of VCO with PMOS transistors diode connected



Current Starved VCO (Ist)

Figure 5.26 Layout of VCO with PMOS transistors diode connected

The simulation results obtained by extraction and simulation of above layout are shown in the table 5.10.

Table 5.10 Simulation Results from the Layout of VCO with PMOS transistors diode connected

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	-0.03 to 3.95	1.96	21.67	46.1
4.5	-0.023 to 3.94	1.95	22.15	45.1
4.0	-0.04 to 3.95	1.95	22.81	43.8
3.5	-0.041 to 3.97	1.96	23.73	42.1
3.0	-0.041 to 3.99	1.97	24.95	40
2.5	-0.027 to 4.02	1.99	27.30	36.6
2.0	-0.028 to 4.09	2.03	33.18	30.1
1.5	-0.029 to 4.22	2.09	60.84	16.4
1.0	-0.014 to 4.3	2.14	207.47	4.8
0.8	0.314 to 4.28	2.29	491.11	2

A graph is plotted between voltage and frequency, which is shown in the figure 5.27 in order to observe the relation between these two quantities.

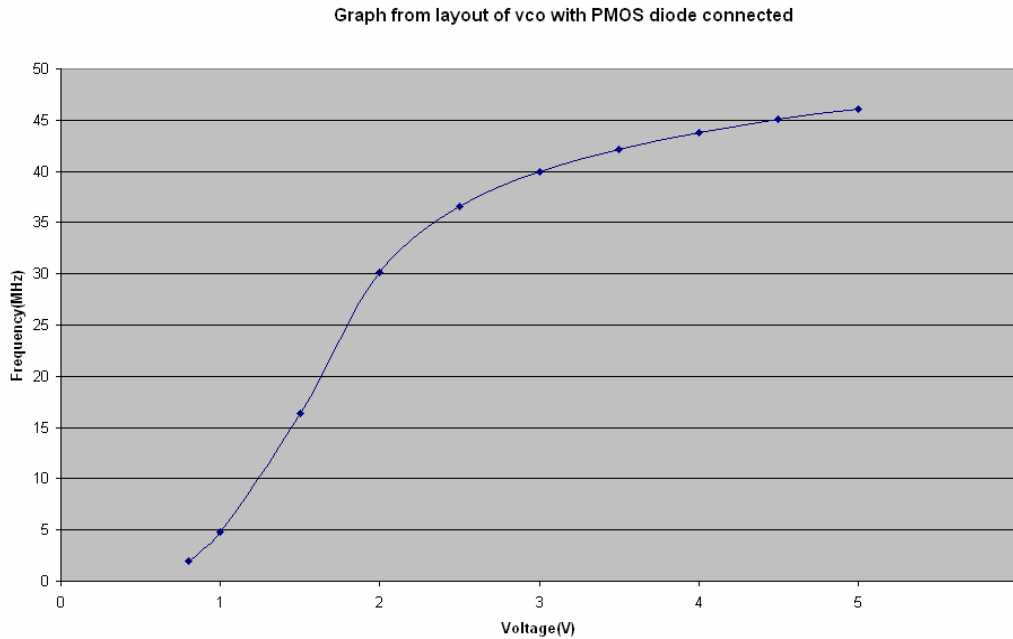


Figure 5.27 Voltage vs. Frequency Plot from layout of VCO with PMOS transistors diode connected

Comparison of the above layout graph of VCO with its schematic graph, shows same relationship between voltage and frequency with the exception that here the maximum frequency is decreased.

5.13 Schmitt Trigger

It is a circuit useful in generating clean pulses from a noisy input signal or in designing the oscillator circuits. Its transfer characteristics are similar to that of inverter with the exception of a steeper transition region. When the output is high and the input exceeds V_{SPH} (high switching point voltage), the output switches low. However, input voltage must go below V_{SPL} (low switching point voltage) before the output can switch high again. The DC analysis of Schmitt trigger by sweeping the input from 5V to 0 gives V_{SPL} which is shown in Figure 5.30 and by sweeping the input from 0 to 5V gives V_{SPH} which is shown in Figure 5.31.

The hysteresis of Schmitt trigger is defined by

$$V_H = V_{SPH} - V_{SPL} \dots\dots\dots(5.12)$$

The hysteresis present in the transfer curves is what sets the schmitt trigger apart from the basic inverter [5].

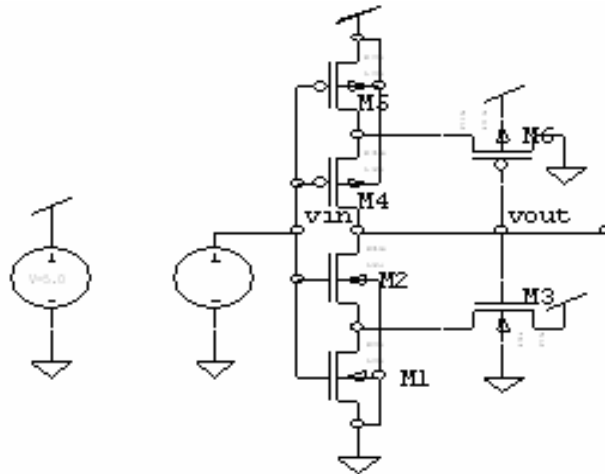


Figure 5.28 Schematic Circuit of Schmitt Trigger

5.13.1 Design of Schmitt Trigger

The schematic circuit can be divided into two parts, depending on whether the output is high or low. If the output is low, then M6 is on and M3 is off and p-channel portion is used in calculating the switching point voltages, while if the output is high, M3 is on and M6 is off and n-channel portion is used to calculate the switching point voltages. Also, if the output is high, M4 and M5 are on, providing a DC path to VDD. Now assume that output is high (=VDD) and the input is low (=0V). Figure 5.29 shows the bottom portion of the schmitt trigger in calculating the upper switching point voltage, V_{SPH} .

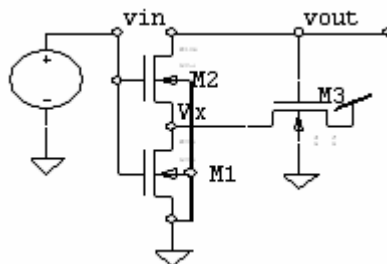


Figure 5.29 Portion of Schmitt Trigger used to calculate V_{TH}

MOSFETs M1 and M2 are off, with $V_{in} = 0V$ while M3 is on. The source of M3 floats to $V_{DD} - V_{THN}$, or approximately 4V for $V_{DD} = 5V$. This point is labeled as V_x as shown in the figure 5.29. With V_{in} less than the threshold voltage of M1, V_x remains at approximately 4V. As V_{in} is increased further, M1 begins to turn on and the voltage, V_x , starts to fall toward ground. The high switching point voltage is defined when

$$V_{in} = V_{SPH} = V_{THN2} + V_x \dots \dots \dots (5.13)$$

or when M2 starts to turn on. As M2 starts to turn on, the output starts to move toward ground, causing M3 to start turning off. This in turn causes V_x to fall further, turning M2 on even more. This continues until M3 is totally off and M2 and M1 are on. This positive feedback causes the switching point voltage to be very well defined [24]. When Eq. (5.13) is valid, the currents flowing in M1 and M3 are essentially the same. Equating these currents gives

$$(\beta_1(V_{SPH} - V_{THN})^2)/2 = (\beta_3(V_{DD} - V_x - V_{THN3})^2)/2 \dots \dots \dots (5.14)$$

Since the sources of M2 and M3 are tied together, $V_{THN2} = V_{THN3}$ the increase in the threshold voltages from the body effect is the same for each MOSFET. The combination of equations (5.13) and (5.14) yields

$$\beta_1/\beta_3 = [(V_{DD} - V_{SPH})/(V_{SPH} - V_{THN})]^2 \dots \dots \dots (5.15)$$

The threshold voltage of M1, given by V_{THN} in this equation, is zero body bias threshold voltage. A general design rule for selecting the size of M2, that is, β_2 , is to require that

$$\beta_2 > 5\beta_1 \text{ and } 5\beta_3 \dots \dots \dots (5.16)$$

A similar analysis is used to determine the lower switching point voltage, resulting in following equation

$$\beta_5/\beta_6 = [V_{SPL}/(V_{DD} - V_{SPL} - V_{THP})]^2 \dots \dots \dots (5.17)$$

Here, values for high switching point voltage and low switching point voltage are assumed that is $V_{SPH} = 3.0V$ and $V_{SPL} = 1.99V$. By putting these values, the ratios of β_1 to β_3 and β_5 to β_6 are calculated as below. The threshold voltage values for NMOS and PMOS transistors are $V_{THN} = 0.62V$ and $V_{THP} = 0.63V$. From equation

$$\beta_1/\beta_3 = [(5-3)/(3-0.62)]^2 = 0.7 = W_1L_3/W_3L_1$$

from equation (5.17)

$$\beta_5/\beta_6 = [1.99/(5-1.99-0.63)]^2 = 0.699 \cong 0.7 = W_5L_6/W_6L_5$$

To satisfy above two equations values for W/L are chosen which are as follows

$$W_1/L_1 = W_5/L_5 = 3/3\mu m$$

$$W_2/L_2 = W_4/L_4 = 10/2\mu m$$

$$W_3/L_3 = W_6/L_6 = 10/7\mu m$$

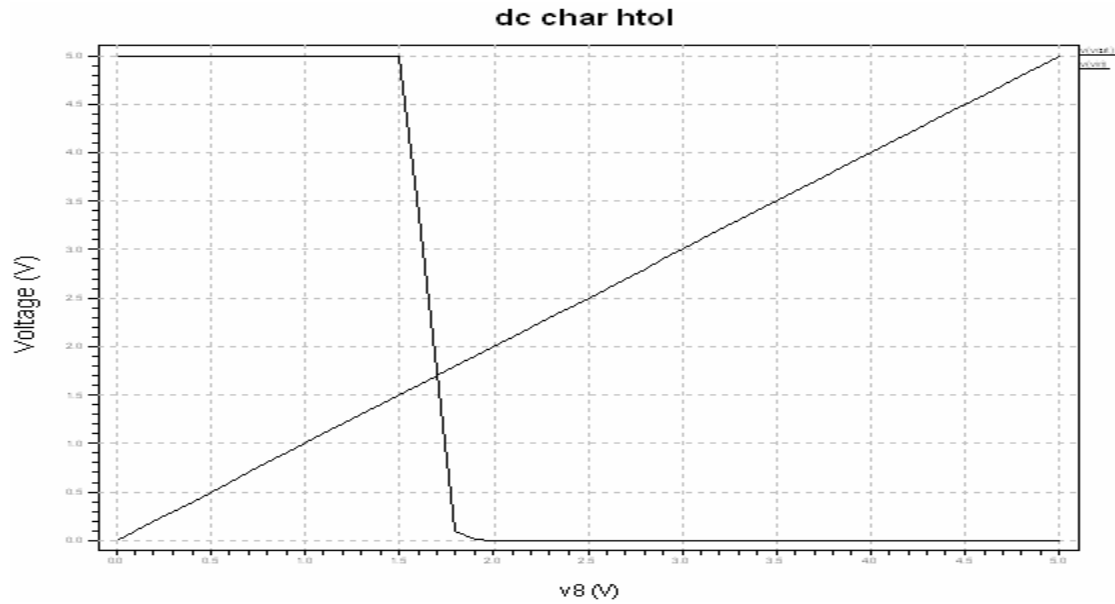


Figure 5.30 DC characteristics showing input sweep is from 5V to 0

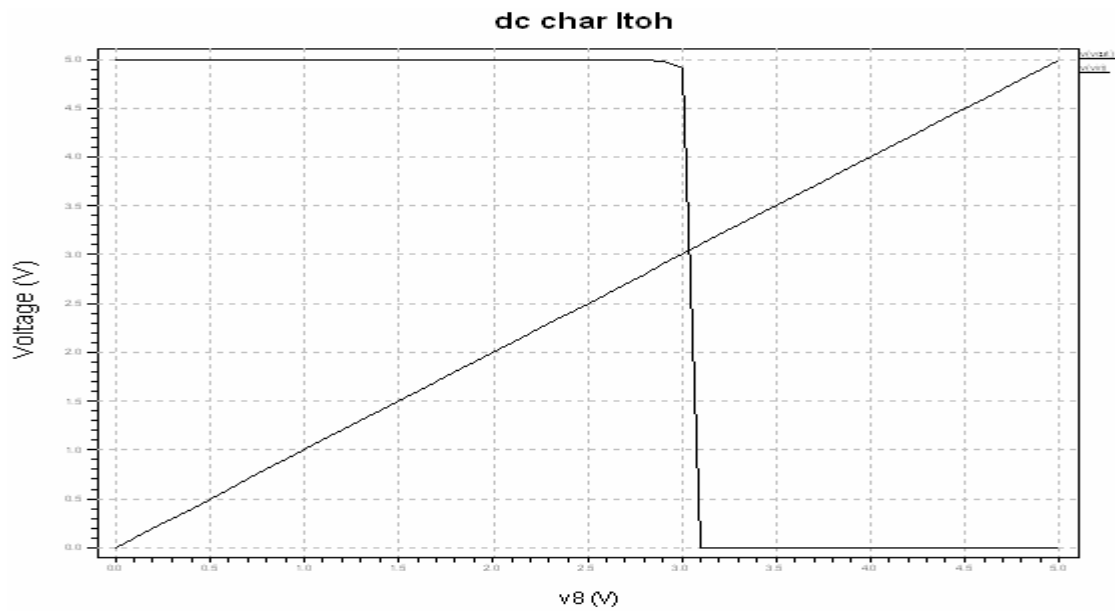


Figure 5.31 DC characteristics showing input sweep is from 0 to 5V

5.14 Design of VCO using Schmitt Trigger

An alternative oscillator using schmitt trigger is shown in Figure 5.32. Here the MOSFETs behave as current sources mirroring the current in M5 and M6. When the output of the oscillator is low, M3 is on and M2 is off. This allows the constant current

from M4 to charge C. When the voltage across C reaches V_{SPH} , the output of the Schmitt trigger swings low. This causes the output of the oscillator to go to high and allows the constant current from M1 to discharge C. When C is discharged down to V_{SPL} , the schmitt trigger changes states. This series of events continues, generating the square wave output. If the drain currents of M1 and M4 are labeled as I_{D1} and I_{D4} , time it takes the capacitor to charge from V_{SPL} to V_{SPH} is estimated as

$$t_1 = C * (V_{SPH} - V_{SPL}) / I_{D4} \dots \dots \dots (5.18)$$

and time it takes to discharge from V_{SPH} to V_{SPL} is

$$t_2 = C * (V_{SPH} - V_{SPL}) / I_{D1} \dots \dots \dots (5.19)$$

The period of the oscillation frequency is, as before, the sum of t_1 and t_2 . This type of oscillator is termed as voltage –controlled oscillator since the output frequency can be controlled by an external voltage. The currents I_{D1} and I_{D4} , are directly controlled by the control voltage [23].

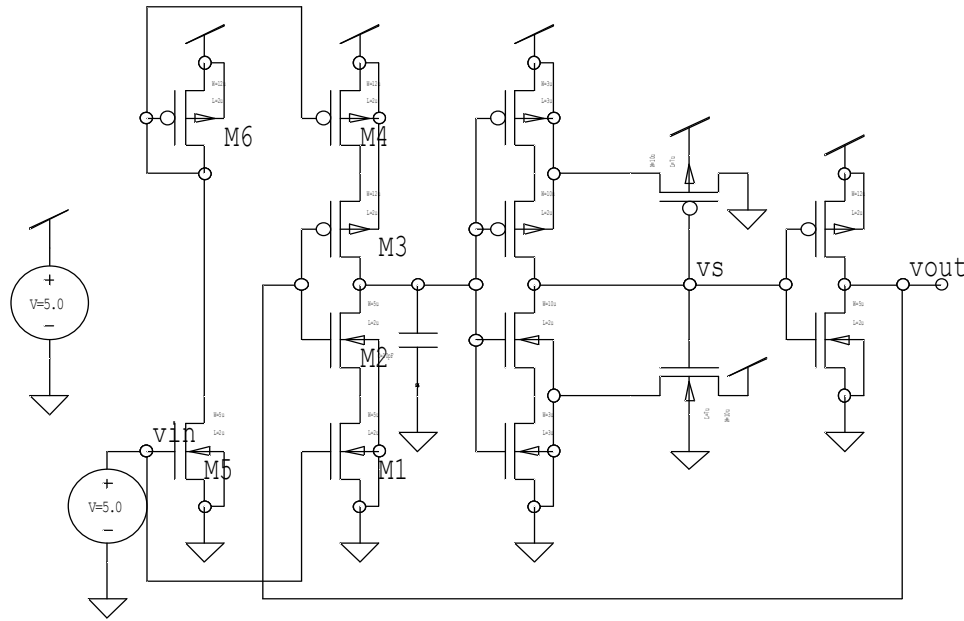


Figure 5.32 Schematic Circuit of VCO designed using Schmitt Trigger

5.14.1 Simulation Results

Figure 5.33 shows the waveform obtained, after the transient analysis is done.

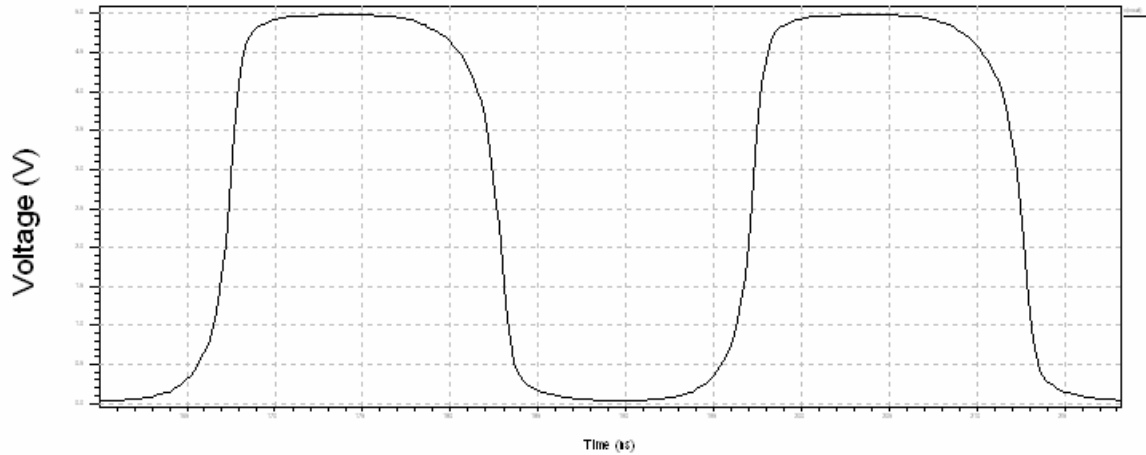


Figure 5.33 Waveform obtained after the transient analysis of VCO designed using Schmitt Trigger

Table 5.11 shows the values of time periods and frequencies at different values of voltages for this VCO.

Table 5.11 Simulation Results of VCO designed using Schmitt Trigger

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ns)	Frequency (MHz)
5.0	0.0243 to 4.97	2.49	29.83	33.5
4.5	0.0265 to 4.97	2.49	30.51	32.7
4.0	0.0290 to 4.97	2.49	31.47	31.77
3.5	0.0306 to 4.98	2.5	33.12	30.19
3.0	0.0258 to 4.98	2.49	36.8	27.17
2.5	0.0205 to 4.98	2.49	43.8	22.83
2.0	0.0397 to 4.97	2.49	53.28	18.7

Figure 5.34 shows the relation between voltage and frequency of this VCO designed using schmitt trigger.

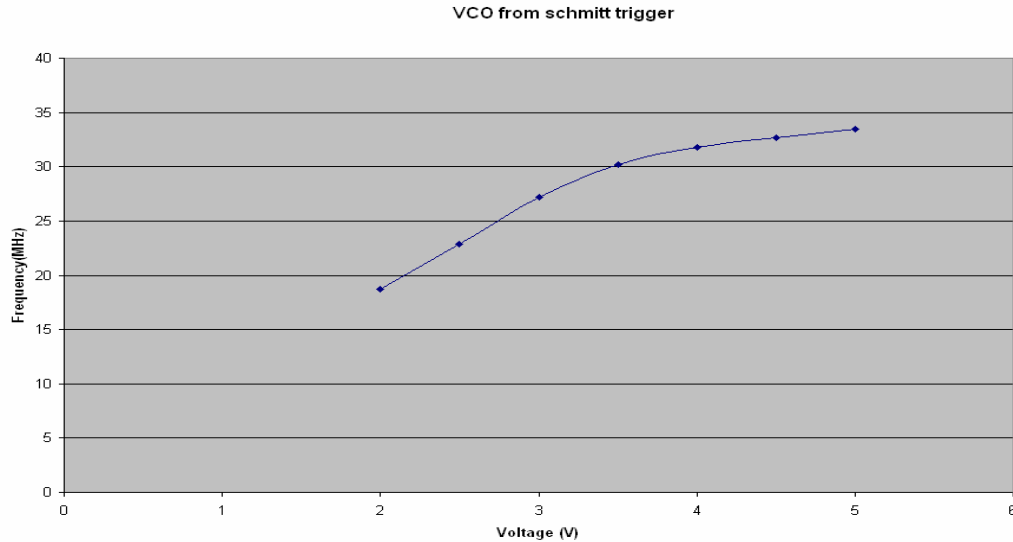


Figure 5.34 Voltage vs. Frequency Plot of VCO designed using Schmitt Trigger

5.14.2 Conclusion

As observed from the above graph, it is found that as voltage is increased, frequency is also increased and the range in which linearity is observed is 18-27 MHz.

5.15 VCO for Pacemaker Application

From the comparative study of VCOs using ring oscillator, it is found that Current starved VCO shows linearity for highest range among all VCOs. So this VCO is selected to be used for pacemaker circuit. For pacemaker, a low frequency VCO is required. The normal rate at which heart beats is 72 beats/min. It is found that time period of one pulse is $60/72$ seconds. Therefore, frequency of pulses needed is $72/60 = 1.2$ Hz. In the present investigation, the frequency of the Current Starved VCO is being lowered by doing some modifications in it i.e., by placing the capacitors (1nf) in the circuit after each inverter stage, by increasing the length of the transistors and by decreasing the width of the transistors (figure 5.35). Specifications chosen for this VCO are –

$$(W/L)_p = 4.8/50$$

$$(W/L)_n = 2/50$$

and value of capacitor $C = 1\text{nf}$

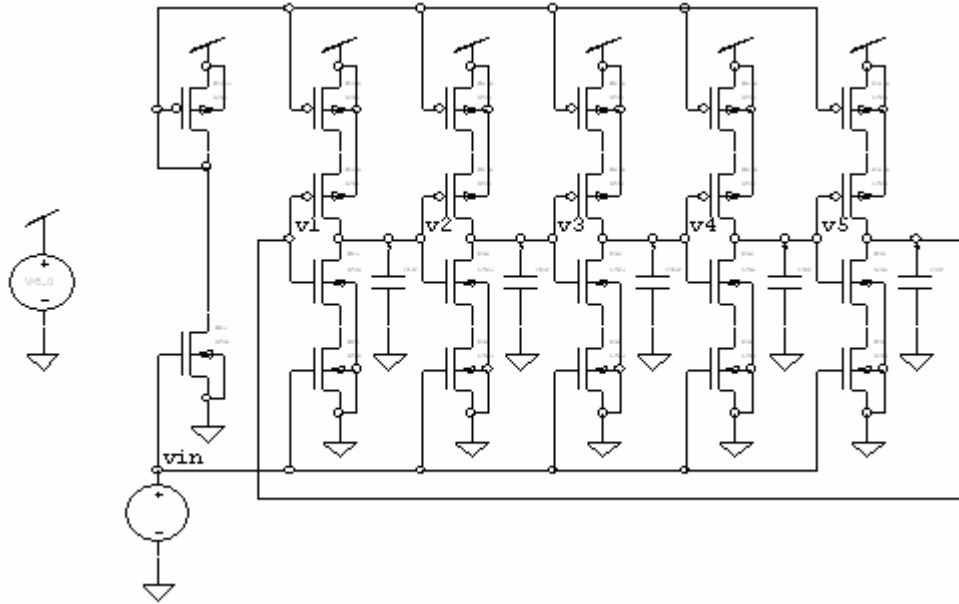


Figure 5.35 Schematic Circuit of VCO used in pacemaker

The input voltage is varied in steps of 0.5V and transient analysis is carried out.

5.15.1 Simulation Results

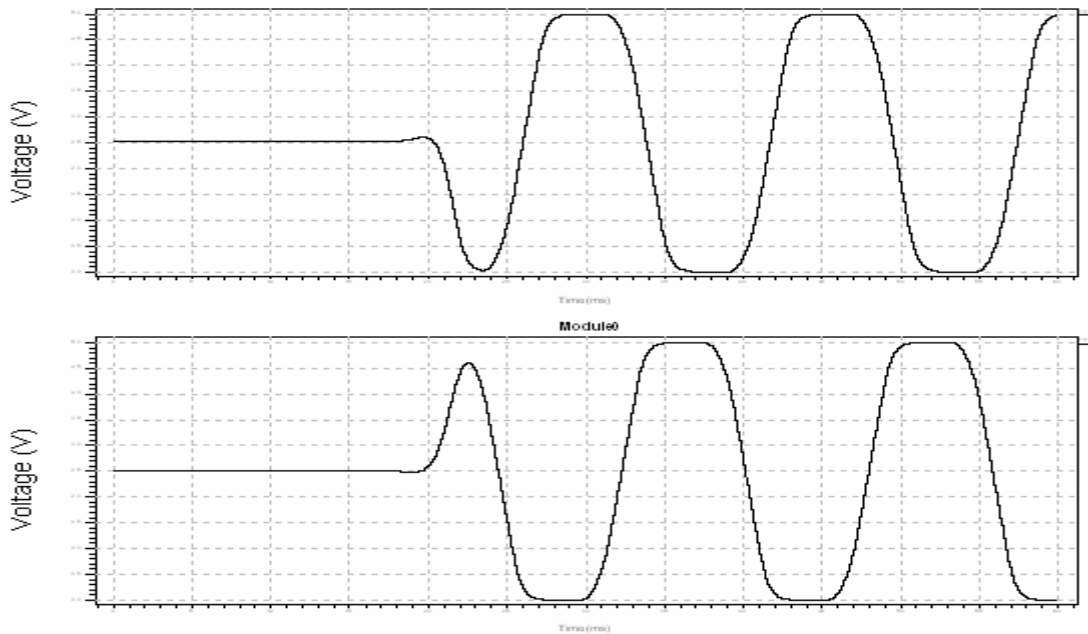


Figure 5.36 Waveform obtained after the transient analysis of VCO used in Pacemaker

Table 5.12 shows the values of time periods and frequencies at different values of voltages, after the transient analysis is done.

Table 5.12 Simulation Results of VCO used in Pacemaker

Input Voltage (v)	Peak-to-peak voltage (v)	50% of P-to-P voltage	Time Period (ms)	Frequency (Hz)
5.0	-0.0098 to 4.98	2.48	4.78	209
4.5	-0.0096 to 4.98	2.48	4.98	200
4.0	-0.0094 to 4.98	2.48	5.28	189
3.5	-0.00930 to 4.98	2.48	5.73	174
3.0	-0.0953 to 4.98	2.50	6.65	150
2.5	-0.0103 to 4.98	2.48	8.94	111
2.0	-0.01084 to 4.98	2.48	15.7	63

Figure 5.37 shows the relation between voltage and frequency for this VCO used in the pacemaker.

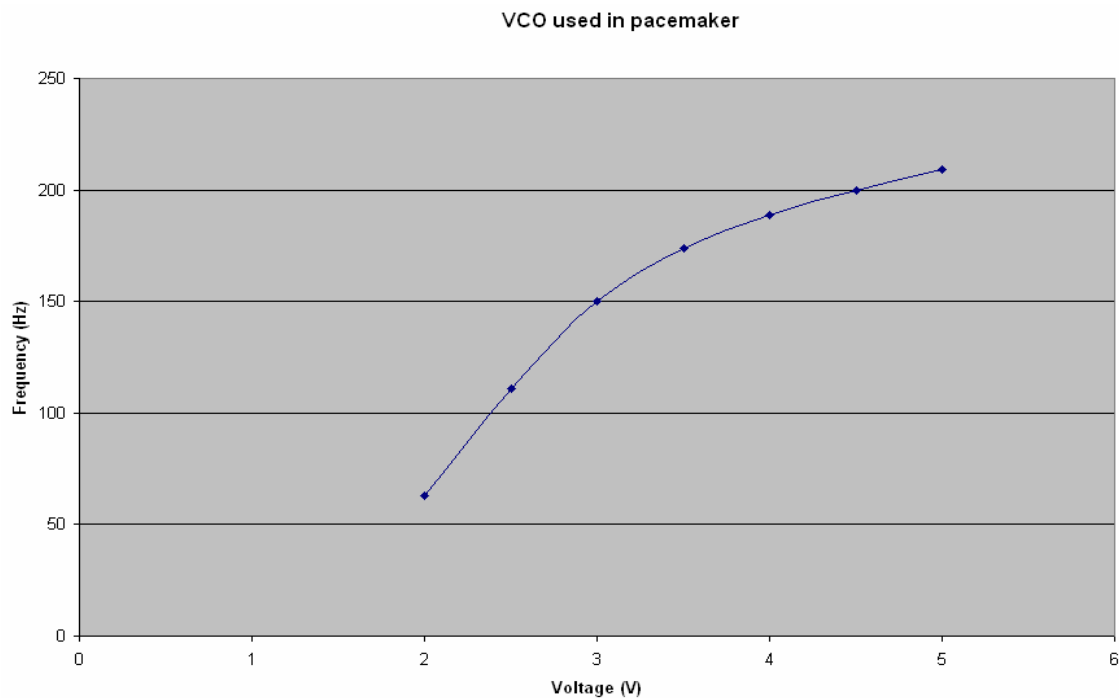


Figure 5.37 Voltage vs. Frequency Plot of VCO used in Pacemaker

5.15.2 Conclusion

As observed from the above graph, it is found that as voltage is increased, frequency is also increased and the range in which linearity is observed is 189-209 Hz. From the simulation results, it is observed that the minimum frequency achieved is 63 Hz at a control voltage of 2.0 V. But the actual frequency required for pacemaker circuit is 1.2 Hz, which is very low. By employing some new techniques or by the use of frequency dividers, frequency of VCO can be decreased further to obtain the desired frequency, so that it can be utilized for pacemaker application.

Chapter 6

CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

In the present work, a deep detailed study of different CMOS Voltage Controlled Oscillators(VCO) is carried out. Based upon the study, the VCO which has obtained best linearity, is selected for design of VCO for pacemaker application.

CMOS VCOs are designed using two circuit techniques. Primarily there are two methods to design VCO. One uses ring oscillator and other uses Schmitt trigger. In recent years, ring oscillators have become an essential building block in VCO's. They can provide a wide operating range, a small layout area and ease of integration. Six configurations of VCOs are designed using ring oscillator and then transient analysis is carried out to observe the linearity of each VCO. Though there are many design requirements of a VCO, but the most important design factor is linearity on the basis of which, comparative study of all VCOs is carried out. The best linearity is found in both configurations of Current Starved VCO means these are linear in the maximum frequency range as compared to other VCOs. Linearity is measured by drawing voltage-frequency plot for each VCO and from the plot it is observed that, Current Starved VCO (Ist) has direct relationship between voltage and frequency and is linear in the frequency range (18.2-70.4) MHz but Current Starved VCO (IInd) has inverse relationship between voltage and frequency and is linear in the frequency range (18-72.5) MHz. So both, can be used depending upon the application, whether positive characteristics (direct) are required or negative characteristics (inverse) are required. A VCO using schmitt trigger circuit is also designed in CMOS. And then a low frequency VCO is designed for pacemaker application. For this purpose, Current Starved VCO (Ist) is selected. As calculated from normal pulse rate of heart, the frequency of VCO required in pacemaker should be 1.2 Hz which is very low. The frequency of the Current Starved VCO is being lowered by doing some modifications in it i.e., by placing the capacitors (1nf) in the circuit after each inverter stage, by increasing the length of the transistors and by

decreasing the width of the transistors. Finally, the minimum frequency of 63 Hz is achieved at the control voltage of 2 V. The efforts are being made to make the frequency, as low as possible and this can be done by employing frequency dividers or by the use of some new techniques so that the VCO can be utilized for pacemaker application.

6.2 Future Scope

As the communication industry evolves, especially in the wireless domain, there will be greater demand for faster data rates, smaller devices and low power consumption. These demands will push the envelope of VCO design beyond today's limitations. The biggest challenge for designers is to find an optimal balance between these requirements.

Faster switching devices will be necessary to drive oscillators at higher frequencies. Enhanced phase noise reduction circuitry will be needed to ensure the stability of multi-gigahertz signals without sacrificing low power requirements. As CMOS fabrication techniques continue to advance, relaxation oscillators designed as ring oscillators will be able to meet these demands with performance comparable to LC oscillators but with the benefit of being constructed on smaller surface areas.

For LC oscillators, improved fabrication techniques will allow high Q factor inductors to occupy less space on the integrated circuit and will allow the inductance value more repeatable during the manufacturing process. An added benefit will be a wider range of inductor values that can be generated for use on chip thereby increasing the tunable frequency range of the oscillator.

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APPENDIX

Paper Published:

During this work the following review paper was accepted in the National conference on Wireless Networks & Embedded Systems (WNES-2006) to be held on 28th July 2006 at Chitkara Institute of Engineering & Technology, Rajpura.

1. Jayna Chawla, Ravinder Agarwal and Alpana Agarwal, "Comparitive study of CMOS VCOs" *National conference on Wireless Networks & Embedded Systems (WNES-2006)*, July 2006.