DESIGN OF CMOS OSCILLATOR

A Thésis Submitted in Partial Fulfilment of the Requirements for the Award of the Degree of

Master of Technology

In VLSI Design

Submitted By

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DECLARATION

I, **Jayanti Kanwar** hereby declare that the work presented in this thesis entitled **"Design of CMOS Oscillator"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at the **Electronics and Communication Department, Thapar Institute of Engineering & Technology, Patiala** is an authentic record of work carried out under supervision of **Dr. Rahul Upadhyay (Lecturer (Ph.D.), Electronics and Communication Department. Thapar Institute of Engineering & Technology, Patiala)** from June 2018 to July 2019. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 11th July 2018

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It is certified that the above statement made by student is correct to the best of my knowledge and belief.

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CERTIFICATE

This is to certify that **Jayanti Kanwar (601762008),** a student of M.Tech (VLSI), Thapar Institute of Engineering & Technology, Patiala, has successfully completed one year (June 2018 – June 2019) internship program in **STMicroelectronics Pvt. Ltd., Greater Noida**. Her title of dissertation is **“Design of CMOS Oscillator”.**

During the period of her internship program, she was punctual and hardworking. I wish her every success in life.

Mr. Vikas Rana
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ABSTRACT

Non-Volatile Memories (NVM's) are an indispensable part of every System-on-Chip (SoC) for retaining the data when the power goes off. The large inaccuracy in oscillation frequency will result in unreliable modify operation and may cause failure in read-write operations. The memory operations do need the on-chip generation of high voltage by charge pump and to drive it the clock is used. The generally utilized high exactness clock references are acknowledged by crystal oscillators, as they are resistant to the process, voltage and temperature variations, however coordinating those alongside on-chip circuits can build the general expense and power of the framework. Clearly, it is important to explore the high accuracy on-chip clock generation strategies for low cost as well as low power applications.

In this dissertation, a comparative study of CMOS Oscillator and a unique design is presented. A 98MHz, conventional five stages Oscillator is compared to proposed current-starved ring oscillator of 98MHz., 40µW-65µW of power dissipation, approx. ±15%, frequency Variation within the temperature range of -40° to 150°C and supply voltage variation of ±10%, across all process Corners. CMOS oscillators are presented in 90nm BCD10 Technology for low power application. The presented PVT compensated oscillator consumes significant lesser power as well as area compared to traditional crystal counterparts. A trimming bit is used for making it compensated across temperature and process. The frequency reference is tried to be made immune to large supply variations.

ACKNOWLEDGMENT

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LIST OF ABBREVIATIONS

1.	MOS	Metal Oxide Semiconductor
2.	MOSFET	Metal Oxide Semiconductor Field Effect Transistors
3.	CMOS	Complementary Metal Oxide Semiconductor
4.	PMOS	P-type Metal Oxide Semiconductor
5.	NMOS	N-type Metal Oxide Semiconductor
6.	DMOS	Double Diffused Metal Oxide Semiconductor
7.	SOC	System On Chip
8.	IP	Intellectual Property
9.	PVT	Process Voltage Temperature
10.	NVM	Non Volatile Memory
11.	Pwell	P-type Well
12.	IREF	Reference Current
13.	CAP	Capacitor
14.	VCO	Voltage Controlled Oscillator
15.	DFF	D Flip Flop
16.	CLK	Clock
17.	GND	Ground
18.	MIM	Metal Insulator Metal
19.	PLL	Phase loop Locked

CHAPTER 1

INTRODUCTION

Unique and Trending Applications in most unexplored consumer electronics and automobiles have over-and-above magnified the embedded applications for NVM. Most adequate circuit design techniques also have to be investigated to achieve excellent product goals. PVT induced variation in memory is important for both memory technology as well as circuit design, in consideration with expeditious downward scaling off feature size of the memory device by technology and on the contrary extravagant increase in a number of storage elements per unit area. In the NVM IP's clock is required for driving another analog block charge pump, which is used as a voltage doubler. On-chip high voltages are generated for performing various memory operations.

As today's integrated circuits are converging towards CMOS because it's low power and other advantages. The design of sturdy and high-performance superior CMOS oscillators plays a really vital role in an IP, achieving it as PVT compensated is like a cherry on the cake. It provides frequency stability across a range and also let the circuitry to be utilized as per the tolerable Variations and PVT ranges. Bipolar-CMOS-DMOS (BCD) process technology is typically accustomed to building products wherever high power or voltage is required. STMicroelectronics has invented this family of silicon processes in the mid-eighties, which do combine the strengths of three completely different and fundamental functions: sensing protection, power devices, and their drive circuits and learning analog circuits and digital logic. Sensors together with native feedbacks for protection and analog signal conditioning are usually accomplished using superior bipolar circuits. CMOS digital control is accountable for the interaction among all elements. DMOS transistors are responsible for handling high-voltage and high-currents**.**

1.1 BCD TECHNOLOGY

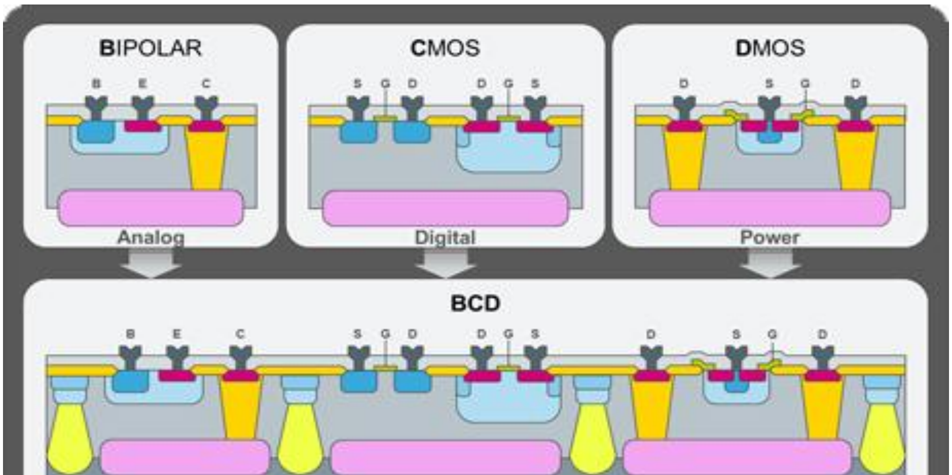

Figure 1.1-1 Bcd Technology [1]

BCD (Bi-Polar CMOS-DMOS) is invented by STMicroelectronics. BCD is a superset of silicon processes, in which potency of three different process technologies is, clubbed together, a single platform which allows the implementation of bipolar, CMOS, Double-diffused MOS all together. Bipolar devices are used for precise analog function design, for low current applications, CMOS i.e. Complementary Metal Oxide Semiconductor preferred for digital design, are for high power functions and DMOS i.e. double diffused Metal Oxide Semiconductor for power and high voltage devices. The benefits of bringing in all the three technologies are higher energy potency, reduced electromagnetic interference and improved reliability, in order that reduced chip area further as better power management will be achieved. BCD is improving day by day to address a wide range of applications. Typical BCD products have a prime feature of all three variants power, analog and digital. To tackle application specific urgency with best possible factors, BCD offers an optimized trade-off between performance, cost, and functionality. BCD technology is continually innovating for better performance, introducing new technology modules, requires finer lithography for emerging memory solutions. In this Triple well, Technology is being used.

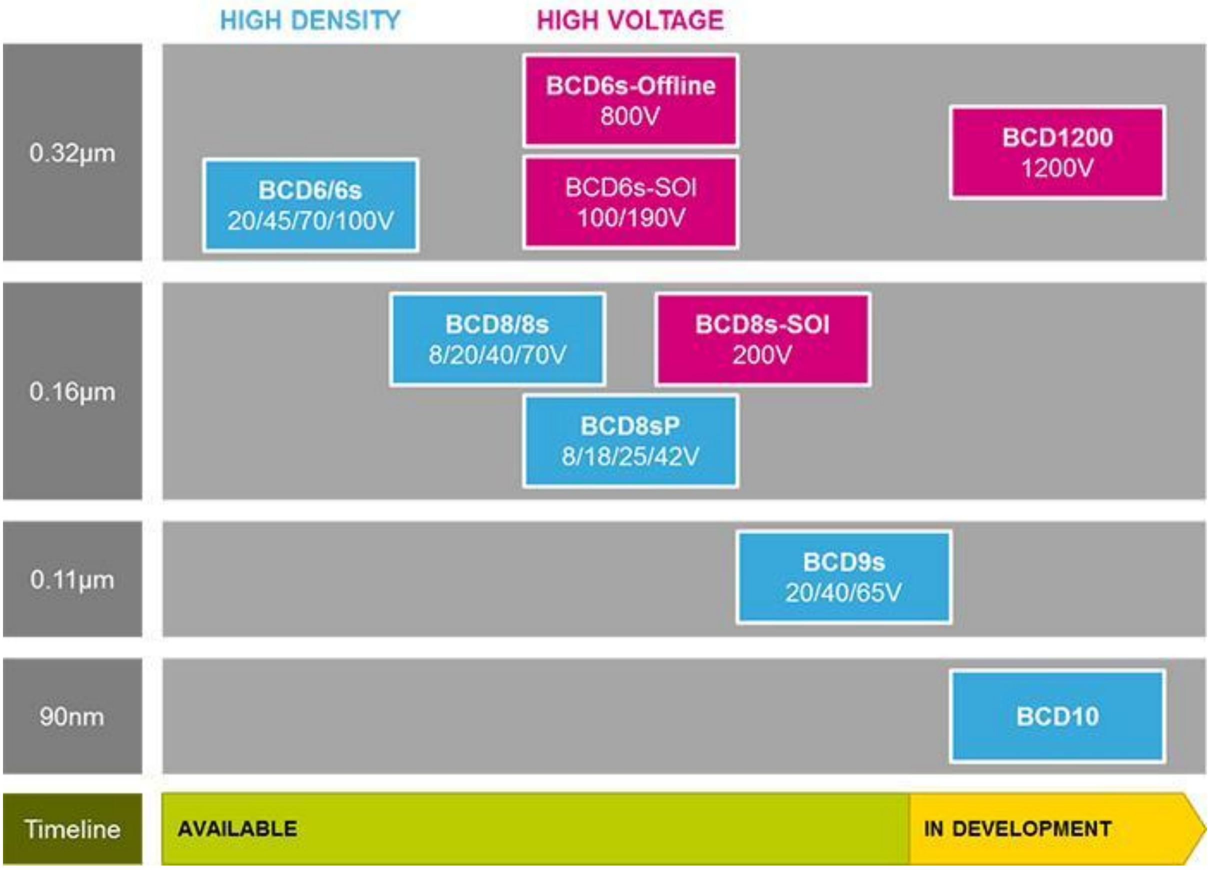

Figure 1.1-2 Roadmap of BCD technology [1]

1.1.1 TRIPLE WELL TECHNOLOGY:

In CMOS technology, Nwell with P-type substrate and Pwell with N-type substrate were used. Whereas twin tub technology uses a common P-type substrate with different Pwell and Nwell for different connections. The isolation layer is used between Pwell and Nwell; still, it fails to provide more efficiency. In this twin tub technology, the virtual NPN and PNP back to back transistors are self-generated. It causes latch-up. The continuous direct path from Power supply to the ground with low Resistances Rwell i.e. R_w and Rsubstrate i.e. R_S is self-generated which leads to excessive power dissipation as shown in the figure below.

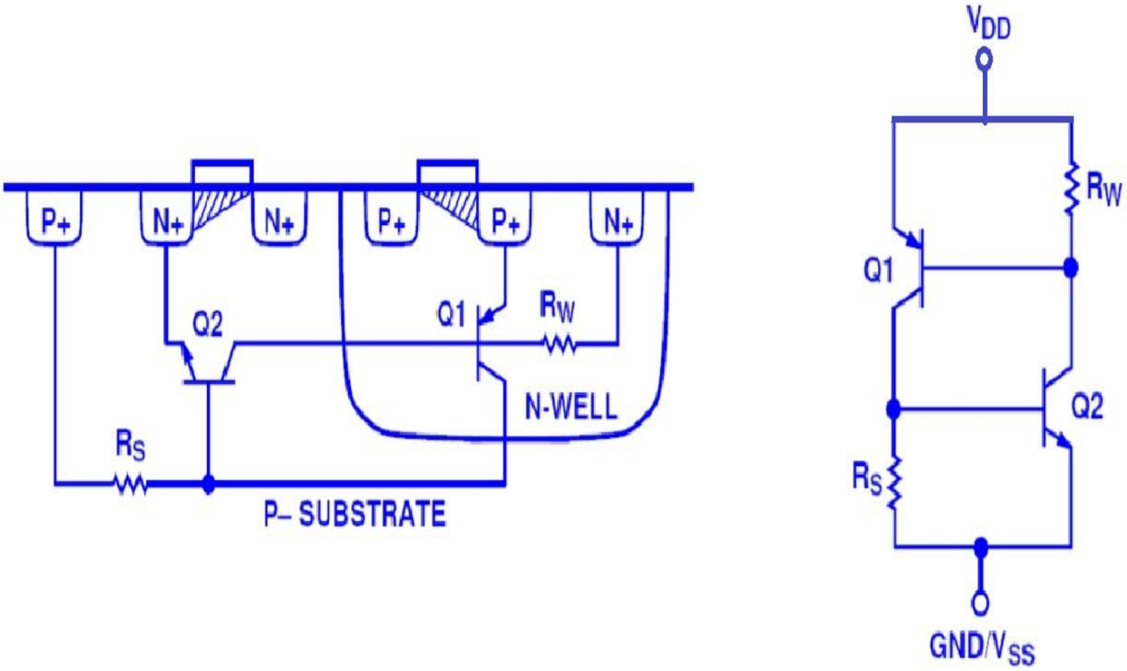

Figure 1.1-3 Latchup in Twin-tub technology

To avoid latch-up, one-way is to increase the width of MOSFET; it will reduce the overall current. Another way is the use of Guard Rings; where Nwell is surrounded by NTAPS connected to VDD supply similarly PTAPS can be connected to ground. Furthermore, R_w and R_S as shown in the figure above can be increased by the means of doping. Triple well technology avoids this latch-up problem and provides additional advantages also. It allows us to have different Pwells so that different body potentials can also be provided. The elaboration of BCD technology is described in the Figure below.

1.2 NON – VOLATILE MEMORY

Semiconductor memories can be categorized as: the RAM i.e. Read Access Memories and ROM i.e. Read Only Memories. When the power is switch-off RAM lose its content while the data of ROM's does not alter. Besides that there is also one factor which distinguishes the two type of memories : the data of RAM can be altered in a less duration of time and also unlimited number of times, and in case of Read Only Memories i.e. ROM, it's data can-not be altered. Memory is combination of write property of RAM's and ROM's then non-volatile memory was introduced. Non-volatile memory works on principle of a floating gate in which storing of charges is done in the conductive metal layer which is in between the channel and the gate and it is surrounded by insulator. The reason behind this is storing the information in the form of charges and hence in the form of threshold voltage.

In the NVM there are two types of cells being used as follow:

- OTP i.e. One time programmable. Only the read and write operations can be performed. Data once written cannot be erased.
- FTP i.e. Few time programmable. In FTP, five operation were being performed: program, read, write, erase and soft program.

1.2.1 FEW-TIME PROGRAMMABLE:

In FTP, for erase operations several mechanisms are being used. CHE and FN tunneling are few preferred much. For the FN tunneling, high voltage is required which is generated onc-chip by the means of charge pump. The charge pump needs the clock signal for the voltage doubling. Apart from other applications of Oscillator, this is a beneficial purpose. Then for the Verification purposes the clock generated by the Oscillator is traced at the output ports by the means of DFT block. DFT is nothing but Design for testability block. This block has all the critical signals of IP in this to be tested including PLS.

1.3 NEED OF OSCILLATOR

In digital electronics most of the devices like Flip-Flop, Registers need a clock pulse for their operation. This clock pulse or a clock signal is nothing but an oscillating signal. Even the CPU of the computer needs a clock pulse.

Mainly lately, the foremost stable and reliable clock generation technique is the use of Quartz based Crystal oscillator. It is used as a clock generator for any sort of SoC. However, preferring these crystal oscillators is a matter of an extremely high-ticket and an inconvenient answer for chip integration. Secondly, most of clock generation techniques based on PLL are often used. PLL based techniques provide synchronization but somehow, they use huge semiconducting material space i.e. silicon area. Furthermore, high on-chip power is generated by them. These PLL based clocks do require a specific reference clock for system lockup. The oscillating signals have a frequency that is why they are used for many applications. Few of applications where we need oscillator are Watches, Radio Circuits, Smartphone, Computer laptops, Stun guns, and Ultrasonic machines.

1.3.1 WHY CURRENT STARVED OSCILLATOR?

Power consumption is extraordinarily necessary for transportable devices, mobile applications such as laptops, cellular phones, and power banks wherever a battery do supply the power. Lesser the power consumed; more the battery life will sustain. A low power design can enhance the lifetime of battery the same that of the merchandise. CMOS Current Starved ring oscillator on addition with BCD technology provides a better solution with less power consumption and chip area. But the tricky challenge with this sort of design is to make it PVT compensated. Attaining a stable clock with variations in supply voltage, temperature and process is a matter of concern. So; a solution is required, to make it compensated of either all three of them i.e. PVT, or any of them can be achieved. Current Starved architecture, the current is fixed and power depends on only two factors; Current and voltage. In this thesis, I will discuss various aspects in oscillator to reduce power and make it compensated and my own proposed circuitry will be explained.

1.4 LITERATURE REVIEW

In Past and recent years, many authors had proposed the different strategies to design the CMOS oscillator in BCD technology and few of them are listed below:

- A 7 MHz PVT compensated three-stage ring oscillators with $\pm 2.6\,\%$ Variations for Temp range -40^0 to 125^0C be designed in 250nm CMOS technology [6]. It used a voltage regulator to generate a stable supply for oscillator and associated bias circuits. The voltage controlled differential cells are used in the ring oscillator to achieve the reference frequency. The control voltage V_{CTRL} of differential cell is produced by a threshold voltage detector reference circuit, additionally used for achieving the process compensation [6]. In order to increase the noise immunity, by the use of a process independent voltage comparator, the output of the oscillator is converted to full swing rail to rail signal. It does consume a significant amount of on-chip area as well as power. Studying this paper gave me an idea of bias circuitries.

- It is another design of 10 MHz temperature compensated ring oscillator presented in 180nm CMOS technology [7]. This design consists of a supply regulated ring oscillator, which does use the differential amplifier in place of the inverter. It employs frequency to voltage conversion circuit in a feedback loop to convert the frequency of oscillator into a reference voltage which is compared with band-gap generated reference voltage to generate an error signal and this error signal drives the VCO. This design incorporates low power techniques and generates reference voltage in the sub-threshold region. It exhibits a frequency variation of $\pm 0.4\%$ across the temperature range of $-55^0\ to\ 125^0C$ and $\pm 0.04\%$ across supply voltage of 1.1 to 3.3V. The following design was very helpful for having a motivation current requirement for different low power techniques.

- A 150 KHz Mobility based Frequency reference is designed in 65nm CMOS technology which is Temperature Compensated [11]. It utilizes relaxation oscillator, controlled by a current which is proportional to mobility and a temperature sensor on a single chip to realize a temperature compensated oscillator. Oscillator’s output frequency is used as a reference of a phase-locked loop (PLL), which comprises of a voltage-controlled oscillator, frequency divider circuit, and a phase detector. For compensation in process, digital trimming bits are also introduced in design for the accuracy of the oscillation frequency. It exhibits the frequency variation of ± 0.5 % across a temperature range of $-55^0\ to\ 125^0C$. This design exhibits significantly less temperature sensitivity at a cost of low operational frequency. This was totally based on temperature compensation and hence gave me an idea of reducing temperature variations in an easy manner. Somehow, I preferred the digital trim methodology.

- In this architecture, relaxation oscillator of 1 MHz is designed in 130nm CMOS technology [12]. It consists of biasing reference circuit to generate reference current, timing circuit to generate delay, the comparator generates the rail-to-rail output and latches to store the output value. Relaxation oscillator's output frequency relies on the product of resistor and capacitor hence, for temperature insensitive operation, it uses resistors which are having zero temperature coefficient and fixed metal-insulator-metal (MIM) capacitor. The latch is also redesigned so that its delay becomes independent of temperature as well as the process. Frequency variation of $\pm 5\%$ across the operating temperature range of $-25^0\ to\ 180^0C$ is reported in this work. The MIM capacitors along with Poly-resistors do require large on-chip area. This is the lowest frequency generating oscillator; I overviewed this for having the idea of temperature variation reductions.

- Another closed loop design of 30 MHz temperature and supply compensated frequency reference is presented in 350nm CMOS technology [9]. The operation principle of this oscillator is somewhat similar to [7], but here a current controlled oscillator is used in a feedback loop. Instead of frequency to voltage converter used in [7], frequency to current converter unit is used. The output of frequency to current converter block generates an oscillator's frequency equivalent current that is compared with temperature and supply compensated reference current. The error signal is a difference in these two currents and it drives the current controlled oscillator. This design exhibits a frequency variation of $\pm 0.5\%$ across the operating temperature range of $-20^0\ to\ 100^0C.$ As per the author, the work done does not report the frequency variation characteristics above 100, which makes this design less suitable for automotive based applications. This was a very useful paper as it enlightened the idea of frequency variation range and the voltage compensations.
- A 2-MHz clock oscillator fully based on differential three-stage ring oscillator, for applications like brand-new wireless biomedical implantable systems-on-chip [13]. The design of oscillator consists of a process detection circuit, replica of feedback bias and a peculiar differential comparator for saving power and area. The frequency variations with supply were measured at 0.11%. An ultra-low-power comparator design is followed in which a digital logic compatible rail to rail clock output with the extraordinary duty cycle is

achieved. The power consumption is quite less i.e. 12µW, appropriate for biomedical applications. This paper was studied for designing conventional oscillator for the same required frequency. In order to compare the conventional with the proposed one.

- A 13.56MHz CMOS ring oscillator for dc to dc converter is designed in 110nm 1P5M CMOS process [15]. It dissipates the power of 6.8mW and has $\pm 0.88\%$ frequency variation against temperature range of $0^0\ to\ 125^0 C.$ In this, the C, R, RC type Oscillators are being compared considering C type. It concludes that C type oscillator has large trans-conductance which after certain offset does degrade the phase noise. If the current bias is made optimized with respect to temperature, then the frequency stability may be acquired for temperature variations, besides the point of the ratio of resistor and trans-conductance in the ring oscillator. This was a typical methodology and used conventional methods, it enlightened the comparative study of the different oscillators and how one can use various external blocks at the cost of size enlargement.

- A balanced frequency of 20 MHz is produced by this oscillator designed in BCD9S (110nm) process across PVT conditions [17]. It uses current starved architecture. It provides temperature range within $-40^0\ to\ 160^0 C$ and supply variation from 3V to 5.5V. It results in the variation of frequency within $\pm 4.5\%$ range. It do consumes all over average current of 68µA. Area required for this oscillator is very less than usual. This was most essential for my work; it used the earlier technology of BCD only. Hence, power reduction methods were learned by this. This oscillator had very less variation with frequency but circuitry was bit complicated and size was 110nm. This let me had an idea of using the MOS capacitance in a unique manner. Few layouts based concerned of extrails and intrails were learned by this paper for the modifications and further reductions in size and power.

1.5 THESIS ORGANIZATION:

The thesis is organized as follows.

Chapter 2 describes detailed working of Conventional Oscillator circuit. It also includes the effect of temperature, voltage and process over the Frequency. Description of Current Mirrors and MOS as a CAP is also included. Finally, chapter concludes with the exploration of various variations with respect to the Process, voltage and Temperature.

Chapter 3 has detailed discussion and comparative study of different techniques for making the Oscillator PVT compensated such that operating at stable frequency. It presents Current controlled Circuitry. Uncompensated and compensated current starved ring oscillator and their operation of work, various limiting factors of this. Description of PVT compensating schemes utilized and also talks about the simulated results extracted across various process temperature and voltage.

Chapter 4 includes the proposed circuitry and its working along with digital trimmings and D flip flop in the picture. Various simulation results of the different stages is been shown. Results for specific temperature and voltage range across all corners are shown.

Finally the Chapter 5 includes the conclusions by comparing the performance of proposed design with other designs and discuss about the future work for improving the scope in low power applications.

CHAPTER 2

CMOS OSCILLATOR

An oscillator is a sovereign system that generates a recurrent output with none input applied to that. A prompt clock generation is a crucial part of any prevailing electronic system. Formerly, Crystal oscillator was followed up as they do provide excellent stability with the process, voltage and temperature variation, however, they're unsuitable with on-chip integration when attempted to made PVT compensated it resulted in the extra cost and all-over size of the system. Ring oscillators are regularly used either as a voltage-controlled oscillator or current controlled oscillator in clock recovery circuits, phase-locked loops and to drive charge pump. CMOS Ring Oscillator provided a solution to integrated clocking. But the substantial challenge with these designs is to attain stable clock which outcomes as a stable frequency yet with variations in process, supply voltage, and temperature. Here I have done some comparative study on the discrete oscillator and numerous ways to compensate the frequency variation with the process, temperature and supply variation.

2.1 WORKING PRINCIPLE

An oscillator is viewed as an amplifier in positive feedback. An oscillator does not require any input and still produces an output which is periodic; this generated output is mostly in the term of voltages. Consider a unity gain negative feedback based amplifier. Ring oscillators are designed as the multiple inverter stages cascaded in such a way composing a ring. Odd numbers of inverters are used in ring oscillator such that, the output of the first stage is opposite of the output of the last stage and vice versa. However, single stage inverter does not oscillate because it cannot provide a frequency dependent phase shift of $0° \, or \, 360°$ in a loop.

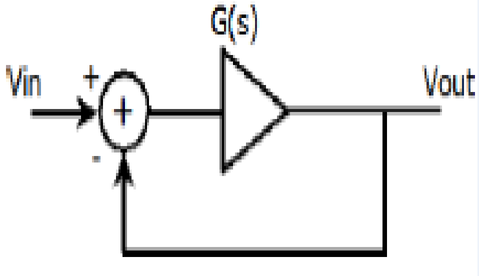

Figure 2.1-1 Feedback system

Its transfer function can be written as Feedback System.

$$H(s) = G(s)\frac{G(s)}{1+G(s)} \tag{2.1}$$

If the amplifier exhibits so much phase shift at high frequencies such that overall feedback becomes positive and it starts oscillating. Can be explained as, for s =$j\omega_o$, G ($j\omega_o$) = -1, closed loop gain H(s) approaches infinity at 'ω_o'. The input of oscillator is a noise component at ω_o which experiences a gain of 1 with a phase shift of '180°'.

For oscillations to begin feedback loop gain G ($j\omega_o$) has to follow two loop conditions:
If I am assuming that the Amplifier circuit has a gain of A and feedback circuit has gain ofβ, with the input voltage V_{in} , feedback voltage V_f and output voltageV_{out}. Then
$V_f = \beta V_{out}$ and V_{out} = AV_{in} $(for\ \beta\ input\ is\ V_{out}\ and\ output\ is\ V_f)$ So, $V_f = \beta A V_{in}$
This $A\beta$ is loop gain.
Case1. If | $A\beta < 1$|: One gets damped oscillations which mean oscillations are continuously reducing.
Case2. If | $A\beta >1$|: Oscillations are continuously increasing because V_{out} keeps on increasing due to an increase in V_f .
Case3. If | $A\beta =1$|: Oscillations are sustained and undamped because $V_f = V_{in}$, V_{out} remains stable, no change in amplitude is observed.

- The loop gain of unity or greater is necessary i.e. |G ($j\omega_o$) ≥ 1| or | $A\beta$ ≥ 1|.
- The frequency-dependent phase shift of 180° should be contributed by the amplifier circuit and more 180° will be contributed by the feedback network, the whole sum up will result in 360°. These conditions are necessary conditions for oscillations only but if I am talking about compensated ones then these are not sufficient for generating balanced oscillation across variations in process, voltage, and temperature. In order to assure the oscillation across PVT variations, the loop gain of at least twice or thrice the required value is selected.

2.2 EFFECTS OF TEMPERATURE ON CMOS CIRCUITS

When the circuit is used for the long run, it does dissipate power and generates heat, also. Another is when the product is used in an IP which is used in cold countries like Norway where the temperature is more cold than usual, or maybe in hot countries like Mexico, then the factors which are dependent on temperature do varies. Also, when the products are used for example in cell phones then the long run use of the product also dissipates excessive power which outcomes the rise in temperature. One of them is Threshold voltage (V_{th}) of the device and another one is the mobility of the carriers (µ) which varies significantly with temperature. The effects of these two parameters are discussed in detail:

2.2.1 VARIATION OF MOBILITY (µ)

Silicon materials when used at very high temperature, the mobility of charge carriers like electron or holes is adversely affected by the fundamental scattering mechanism in which the carriers spread out, commonly known as lattice scattering. The crystal lattice is dependent on the spacing of ions for conductivity. With the rise in temperature, the lattice vibration directly increases referred as thermal vibrations also; more vibrations do scatter the charge carrier this spreading reduces the mobility of carriers as the temperature keeps on increases [18]. The carrier mobility (υ) (cm2/V s) defines the drift velocity of the carrier in the electric field. As the operating temperature increases the probability of scattering of the carrier with crystal lattice increases, this causes a reduction in mobility of the carriers at the high temperature [12].

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-1.5} \tag{2.2}$$

2.2.2 VARIATION OF THRESHOLD VOLTAGE(V_{th})

The threshold is the minimum voltage required to switch the transistor on. A MOS threshold voltage amount decreases with the rise in temperature [13]. The threshold voltage for an n-channel MOSFET is defined as the positive value of gate-source voltage, at which the same concentration of minority charge carriers from the p-substrate are collected beneath gate in-order to mirror back the potential forming a capacitor C_{ox} with gate oxide in-between as the dielectric. [12].

$$V_{TH}(T) = p_0.T + q_0 \tag{2.3}$$

Where p_0 in V/◦CK are a negative value for NMOS transistors and a positive value for PMOS transistors. q_0 Is the threshold voltage of the device at 0°K.

$$V_{th} = V_{fb} - 2\varphi_f + \frac{\sqrt{4\varepsilon_s q N_a \varphi_f}}{C_{ox}} \tag{2.4}$$

Here; V_{fb}, φ_f, ε_s , C_{ox} , K, q are flat band voltage, surface potential, the permittivity of silicon, oxide capacitance, Boltzmann’s Constant and charge of electron respectively.
N_i , N_a Are the intrinsic silicon carrier and substrate doping concentrations respectively [13].

Clearly, V_{th} depends strongly on Fermi potential φ_f.

$$\varphi_f = \frac{KT}{q}\ln\frac{N_a}{N_i} \tag{2.5}$$

Eq(1.3) Factors affecting φ_f are N_a, N_i and thermal voltage $\vartheta_t = \frac{KT}{q}$.

The concentration of electrons becomes equal to the concentration of holes within the channel when the potential difference between channel and substrate becomes equivalent to twice the Fermi potential [2].

φ_f is directly dependent on temperature. Moreover V_{th}, due to its strong dependence on $-2\varphi_f$ the term, it decreases with a boost in temperature. It can be considered that the threshold voltage (V_{th}) is a prime parameter of both process and temperature dependencies. Thus, the Process and Temperature compensated oscillator architecture is required to stabilize the output frequency and so that one can control V_{th} variations.

2.3 CURRENT MIRROR METHOD

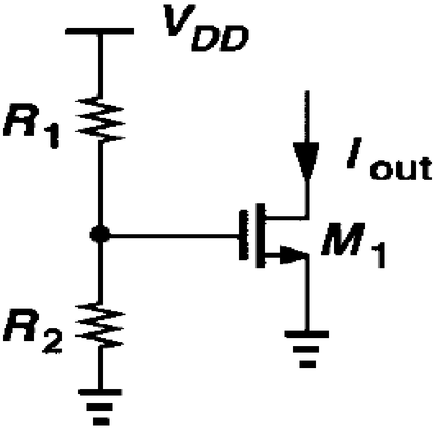

Figure 2.3-1 Current by the means of a resistive ladder

MOS with its diverse functionality, It itself plays the role of many components all alone. Capacitor, Resistor or it may be a current source; MOS can be individually used for this. Now the question is how to bias the MOS in such a way so that it may behave as a stable current source. The equation for figure 2.3-1 says as here, both V_{TH} and μ_N exhibit temperature dependency. Thus, in this way I_{OUT} is very poorly defined. Eq. (1.5) shows the calculation of drain current for saturation region [23].

$$I_{OUT} = \frac{1}{2}\mu_N C_{ox}\frac{w}{l}\left(\frac{R_2}{R_1+R_2}V_{DD} - V_{TH}\right) \tag{2.6}$$

$$I_{OUT} = \frac{1}{2}\mu_N C_{ox}\frac{w}{l}(V_{GS} - V_{TH})^2 \tag{2.7}$$

This structure of M_1 and M_2 is called as “Current Mirror” considering Both MOS’s to be in saturation and similar. This copying of current has no dependence on process and temperature as it only depends on the size of the Mosfet i.e. w/l. So the copied current is the multiple of w/l of M1.

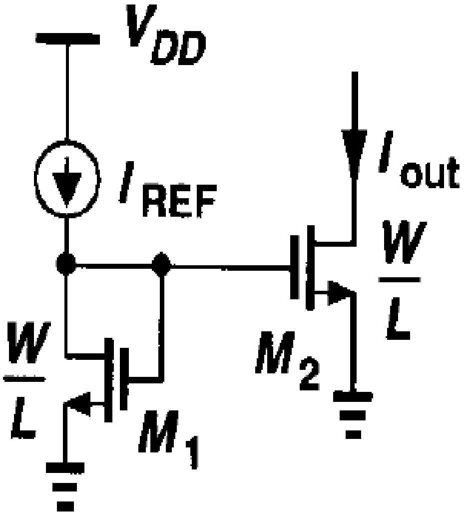

Figure 2.3-2 Current Mirror

$$I_{OUT} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \tag{2.8}$$

This way current mirror helps in biasing the circuit and instead of generating current again and again for the different requirements, that too by the single transistor only.

2.4 MOS CAPACITANCE

MOSFET is a versatile component. It can act as a resistor as well as capacitor apart from its conventional operation. It can also act as a voltage-dependent capacitor as it will depend on the gate voltage applied to it. The estimation of its capacitance relies upon operating region of MOSFET; therefore it may also be termed as a variable capacitor (var-cap). The gate layer and charge layer which is present in the substrate, both of them together act as two parallel plates of a capacitor and thin gate oxide layer in-between them behaves like a dielectric layer between two capacitor plates. Consider an NMOS present in Figure 2.4-1, its gate voltage is varied from -*Vhigh* to *Vhigh.* Initially when the gate is biased to *Vhigh,* wide depletion region is available, since the gate is negative biased at -Vhigh, positive holes present in the substrate are accumulated below the oxide layer, hence effective width of the capacitor is equal to the width of the oxide layer. In this region, NMOS is operating in the accumulation region, since holes present in the substrate are accumulated in the channel region. When the gate starts rising from negative voltage; it could be only –*Vosc* to *Vosc* but for a wide range, I have considered (–*vhigh* to *vhigh*) range towards positive voltage. The majority of positive holes present at the oxide-substrate interface are chased away by the positive gate potential and pushed back into the substrate. Meanwhile, the immobile carriers are accumulated beneath the gate creating a depletion layer. This depletion layer mirrors back the applied positive charge on the gate terminal and continues expanding, till the time gate voltage (V_g) is less than the threshold voltage (V_{th}). At that point when the channel region is free of any charge carrier then maximum separation distance will exist between two parallel plates of the capacitor. Since the value of capacitance is inversely proportional to the separation distance of parallel plates hence the minimum value of capacitance is obtained in this operating region. In this region, one can say NMOS is biased in the depletion region because the channel area is depleted of any charge. When gate voltage starts rising again and reaches *Vosc*, the channel will consist of free electrons which are accumulated below the gate-substrate interface. This free electron layer again reduces the separation distance between two plates of the capacitor; which results in high capacitance in this region. Since free electrons are available in the channel region so in this region of operation, NMOS is biased in strong inversion region. Hence, it can be considered that in strong accumulation and deep inversion region, MOS capacitance exhibits the maximum value of gate capacitance.

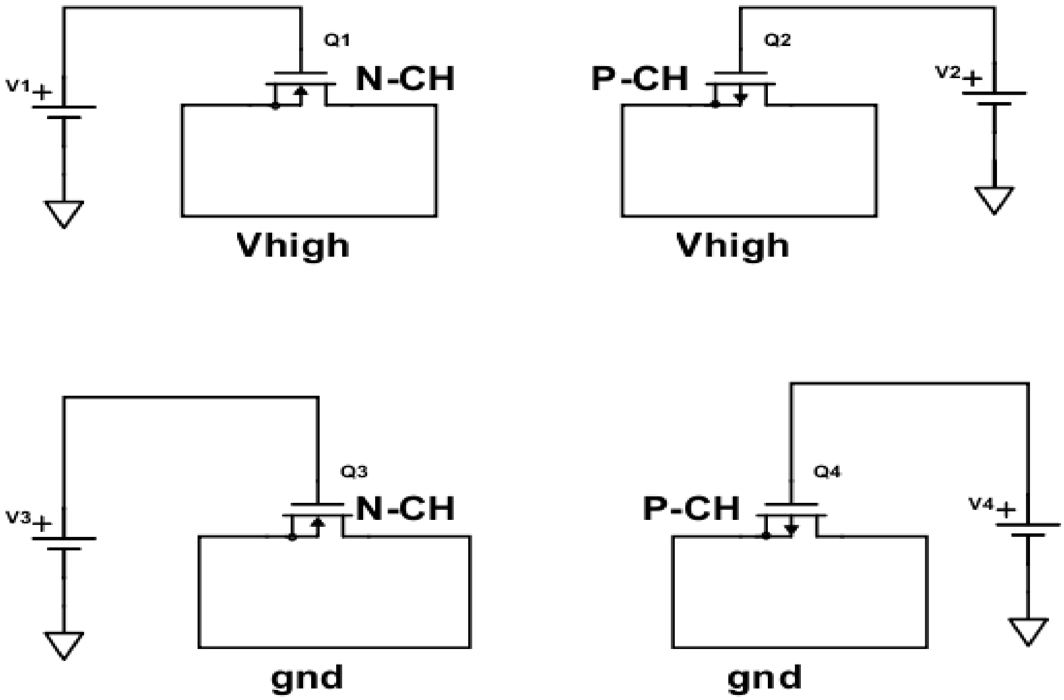

Figure 2.4-1 Behaviour of mos as a cap with gate voltage as variable

Here, in Figure 2.4-1 MOS capacitance for NMOS and PMOS, the gate voltage is varied and considered MOS in two cases for source-drain voltages, vhigh and ground. If the Q4 with its source, drain, substrate tied to ground potential, and also the gate potential is considered to be even lower than the substrate(-vhigh) then the majority holes attract towards the gate and get accumulated, considering it accumulation region.

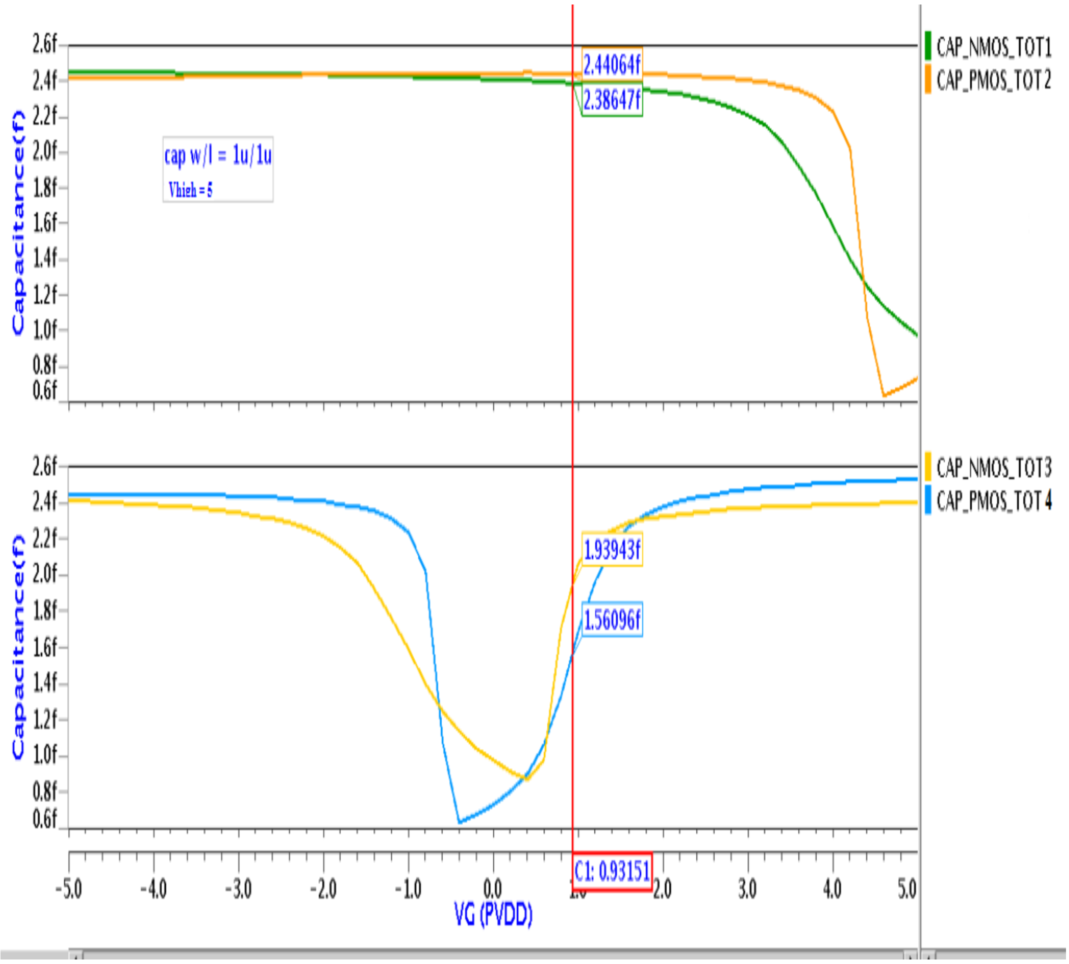

Figure 2.4-2 Mos cap with variable gate voltage for calculation of per unit capacitance

Now, while comparing these cases for Q2 and Q4, it is noticed that the accumulation region is more available in the case of Q2. The reason is the huge difference between the gate potential and the substrate potential which are acting as the two plates of the capacitor. So, here for Q2; the range is from *vhigh* to *-vhigh* and in Q4 range is *gnd* to *–vhigh*. Hence, for my work, I have considered the Q2 possibility because it leads Q1 also as shown in the Figure above. For stability of oscillator to be the prime factor, PMOS was the appropriate one for MOS capacitance.

CHAPTER 3

COMPARATIVE STUDY OF OSCILLATOR

Designing of a CMOS ring oscillator includes numerous constraints regarding area proficiency, speed, power and operational domain explicit. This exercise proposes an appropriate strategy for enhancing frequency steadiness of a CMOS ring Oscillator by contrasting the customary ring oscillator with the current starved CMOS Oscillator.

3.1 CONVENTIONAL RING OSCILLATOR:

The traditional CMOS Ring Oscillator do comprise of an odd number series of inverters (N: odd in number), which are back coupled in the form of feedback to provide an unstable state that results in oscillation *(figure 3.1-1*). The change going around the ring needs to go through every inverter twice to touch base at the beginning stage. So the frequency of oscillation is given as:-

$F = \frac{1}{2N\tau}$ Where N represents the total number of inverter stages utilized and τ is the delay produced by the single inverter.

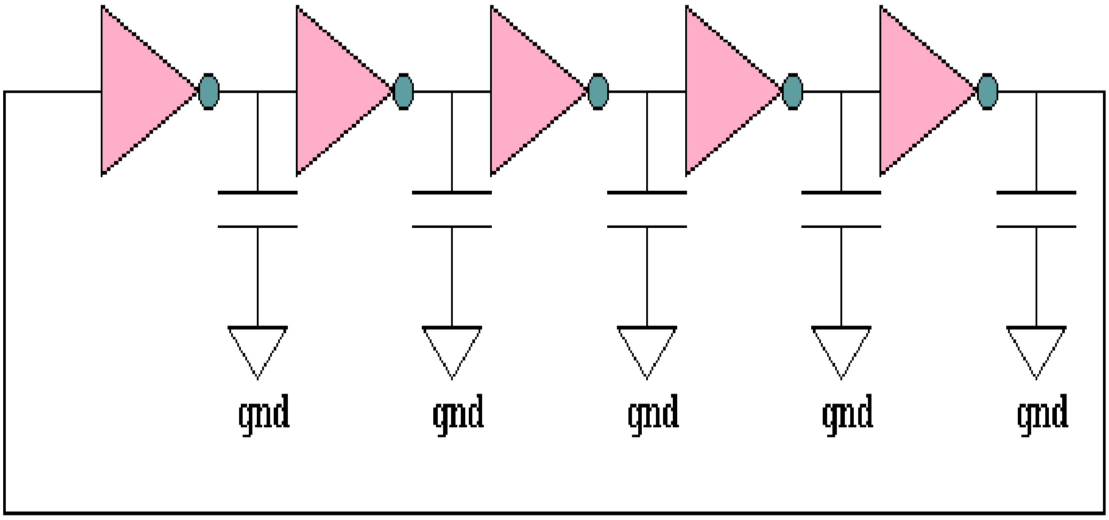

Figure 3.1-1 Five stage Ring Oscillator

3.2 PROBLEM WITH CMOS RING OSCILLATOR

- Power consumption in this circuit is very high.
- Frequency varies abruptly with supply variation.
- Apart from its frequency varies with temperature and process.

Hence instead of the basic ring oscillator, Current starved ring oscillator is preferred.

3.3 CURRENT CONTROLLED RING OSCILLATOR

Current-starved ring oscillator has an additional MOS as a capacitor. Capacitance is used by the width and length of MOS as the basic parameters to control. Hence the delay unit plays a very important role in this technique and IREF modules are providing a constant current which is required to charge and discharge the timing MOS capacitor. Figure 3.2-1 shows the delay unit of the current starved ring oscillator.

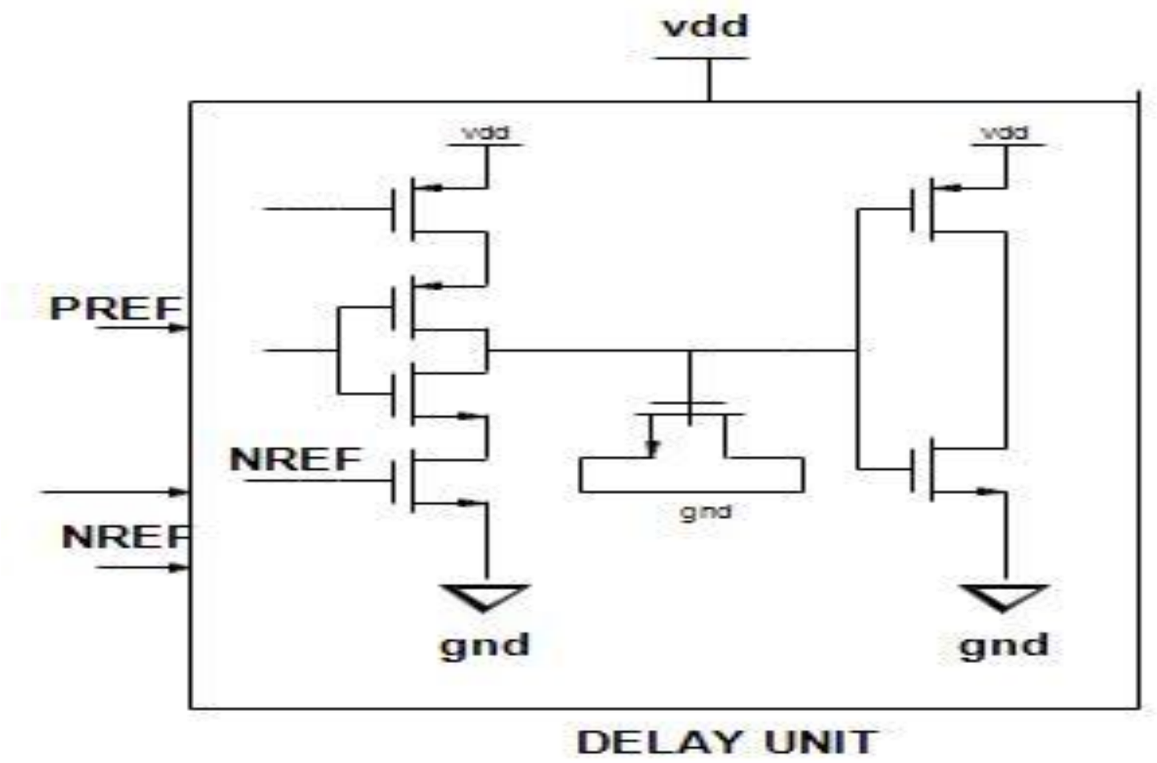

Figure 3.3-1 Delay unit of Current starved Ring Oscillator

Current and Capacitance have their different dependencies on the sizing of the Mosfet. So, if I will use large current to charge large capacitance than it will result in power dissipation. So, in this oscillator power dissipation is reduced by sizing parameters like less current is used to charge more capacitance.

$$\text{Cap} = WLC_{ox} \tag{3.1}$$

$$I = \mu C_{ox} \frac{w}{l} (V_{GS} - V_T)^2 \tag{3.2}$$

Problem with Current Starved Ring Oscillator:-

- Power consumption is decreased in the current-starved oscillator

- But frequency varies with Process, voltage and temperature variation.

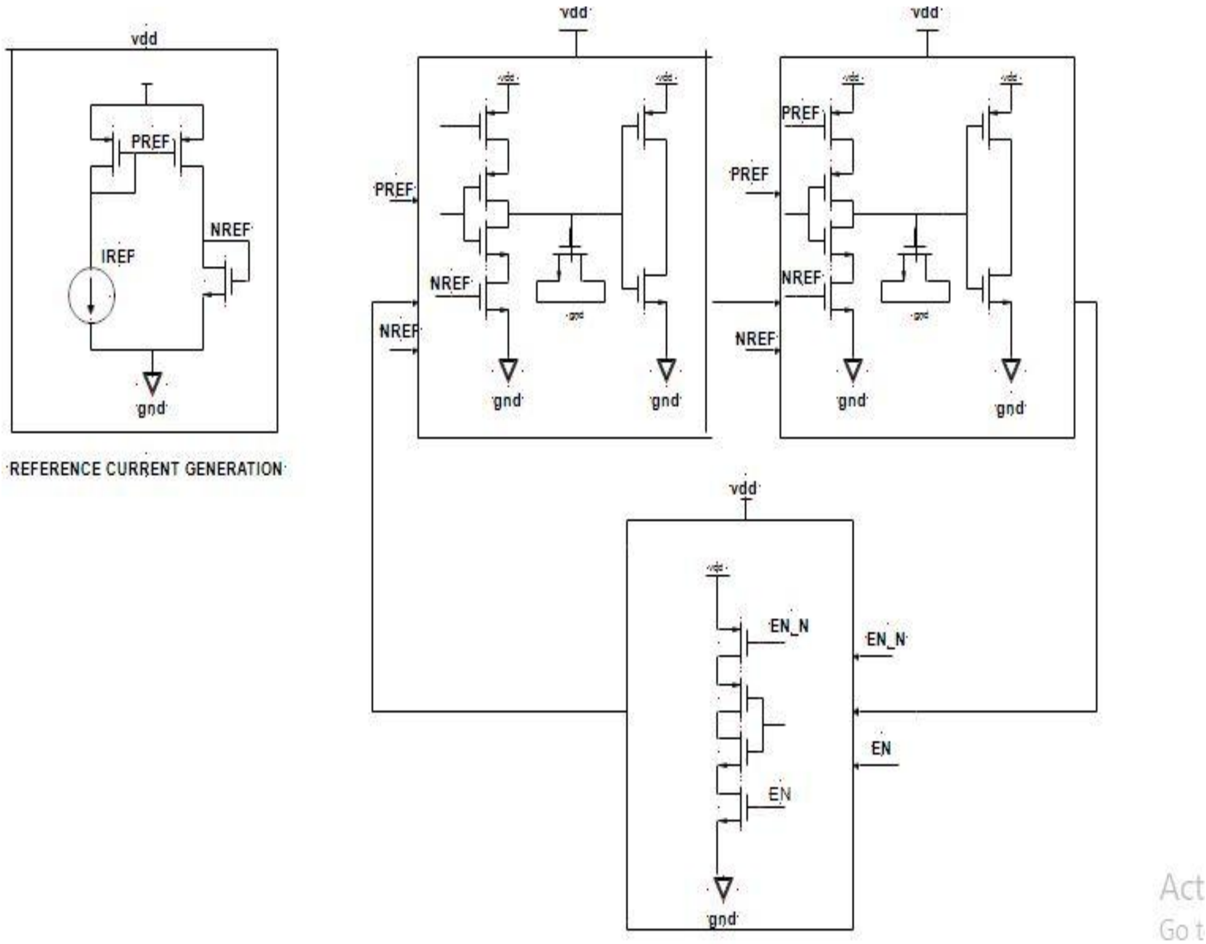

Figure 3.3-2 Uncompensated Current Starved Ring Oscillator

For supply variation, the solution is to use the constant supply voltage

3.4 REGULATED VOLTAGE OSCILLATOR

To obtain a controlled or regulated supply voltage for current-starved ring oscillator a “voltage regulator” can be preferred. Figure 3.2-3 demonstrates the Supply remunerated current-starved ring oscillator. To bring out a regulated supply voltage one reference voltage (bandgap voltage) is required. An operational amplifier in a closed loop system is utilized to produce a regulated supply voltage.

Problem with Supply compensated Current Starved Ring Oscillator:-

- Now oscillator is compensated for supply voltage
- But the process and temperature variation are still present.
- Also for supply compensation, an extra reference voltage is required.

From section 3.1 I become acquainted with the fact that a straight chain of an odd number of inverters can oscillate, however, that oscillation frequency is fixed in that case. What if I want to make it with the end goal that I can change the wavering recurrence by the means of a controlled voltage? In this, I will take a glance at certain distinctive VCO cell topologies and their merits and demerits.

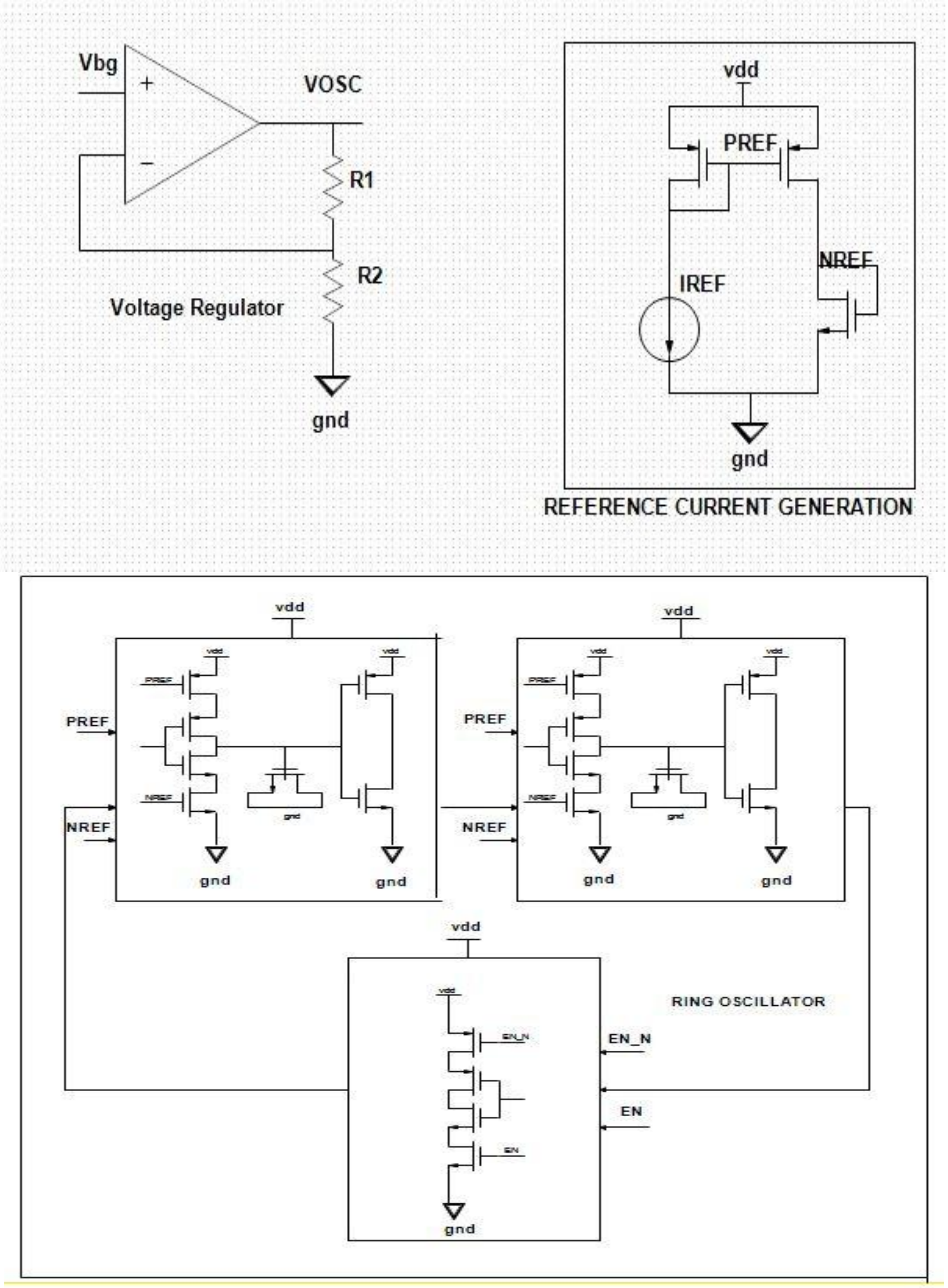

Figure 3.4-1 Supply Compensated current starved ring Oscillator

In the Current Starved Inverter, I made it possible to control the current through the inverter by the means of a voltage controlled current source so that the charging and discharging time of an inverter can be easily made under control, as portrayed in Figure 2.4-2. This control voltage, Vctrl, is driving the current source and this current along with capacitor will decide this charging and discharging time of an inverter. The custom inverter is being modified by making it starve of the current than they are ordinarily permitted to consume. Henceforth, this topology is referred to as a current-starved inverter. For making a decent oscillator an odd number of stages, current levels and correct dimensions of the current starved inverters are only needed. The oscillation frequency can be accomplished very quickly, and tuning extent is tremendous, even though the design is quite simple, due to the square Law change in current levels in the footer device. In order to avoid any type of variations in the output swing, I can resize the footer device wider. Anyway, there are numerous issues with this design. To begin with, the inverter is not capable of working at very low bias voltages, for example, zero, when the current in the inverter is being stopped. Second, the output of each stage drives two gates, which confines the maximum oscillation frequency. Third, when attempting to amplify the VCO output to full swing, the DC voltage level of the VCO output isn’t steady; this could make trouble at high frequency.

CHAPTER 4

PROPOSED CIRCUIT

4.1 WORKING OF PROPOSED CIRCUIT

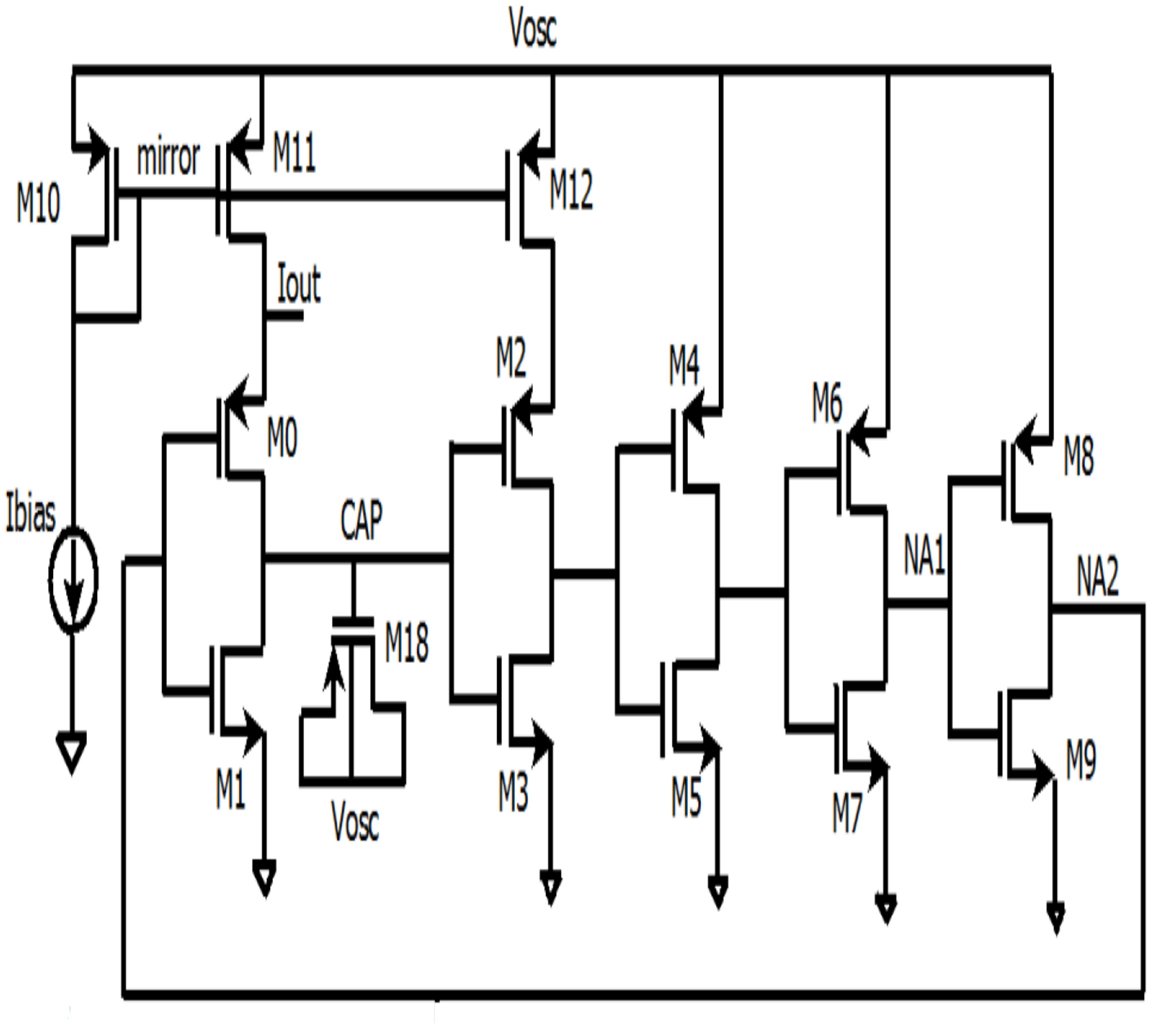

Figure 4.1-1 Circuit of proposed Oscillator.

Ring oscillator consists of an odd series of inverter stages present in such a way of forming a ring, five in this case. Each stage is Responsible for adding a frequency dependent phase shift and also provides a gain to satisfy the necessary condition of oscillation. *Figure 3.2-1* shows the circuitry of the proposed oscillator. The very first two inverter stages are made current starved which includes transistors M_0-M_3. Rest of the three stages are biased at supply voltage comprising of transistors M_4-M_9. The first current starved stage is responsible for the maximum amount of loop delay and the second current starved stage is used for the temperature compensation of the oscillator. The rest of supply biased inverter stages allows the next generated phases to have a rail to rail voltage swing. The

Transistor M_{18} a PMOS one plays a very vital role. It is a MOS used as a capacitor placed immediately after the first stage and is biased in any of its operating region either in the inversion or in accumulation region to obtain an almost fixed amount of gate capacitance. In this architecture, maximum of the total delay is obtained from the initial stage itself and is originated due to only charging of gate capacitance present at 'CAP' node; later stages do only have routing capacitance which is contributing in the delay. Moreover, other inverter output nodes have only small parasitic capacitors. The charging current (I_{cap}) of the capacitor can be written as:

$$I_{bias} = \frac{\left(\frac{W}{L}\right)_{11}}{\left(\frac{W}{L}\right)_{10}} \tag{4.1}$$

Where I_{bias} depicts the biasing or reference current this is generated on-chip by the means of the current mirror. Henceforth, it is presumed to be constant across PVT variations as it depends only on W/L which is the aspect ratio of the respective transistors. Subsequently, the charging time can be expressed as Eq 4.2

$$T_{charging} = \frac{C * V_{cap}}{I_{cap}} \tag{4.2}$$

The term V_{cap} is also equal to the gate to source voltage of device M3 and it can also be written as:

$$V_{CAP} = V_{GS3} \tag{4.3}$$

The stage two of the proposed oscillator is too made starve of current. A fixed amount of current is utilized to charge up the output node of the second stage. The output of the second stage do also comprises of some small parasitic gate capacitance of M_4 and M_5. V_{GS3} Can be expressed as Eq.(4.4), if the MOS transistors M_{11} and M_{12} are matched.

$$V_{GS3} = V_{TH3} + \sqrt{\frac{2 \cdot I_{bias}}{\mu_n C_{ox} \left({}^{W}/_{L}\right)_3}} \tag{4.4}$$

4.2 D FLIP-FLOP

For achieving the symmetry in the clock output, D-flip flop is also used as shown above. The Designed D flip flop follows conventional master slave architecture. In which transmissions gate are fully utilized. Two out of four Transmission gates are on at a time with opposite phase lock. Full rail to rail logic 0 and logic 1 is then successfully passed at a time. The outputs of the last two stages are fed to a D flip flop as inputs, in order to generate the output clock with a duty cycle of 50 %. Although this D flip flop does reduces the frequency to half in order to make duty cycle 50%. Hence the frequency calculated by delay is twice of frequency achieved after D flip flop.

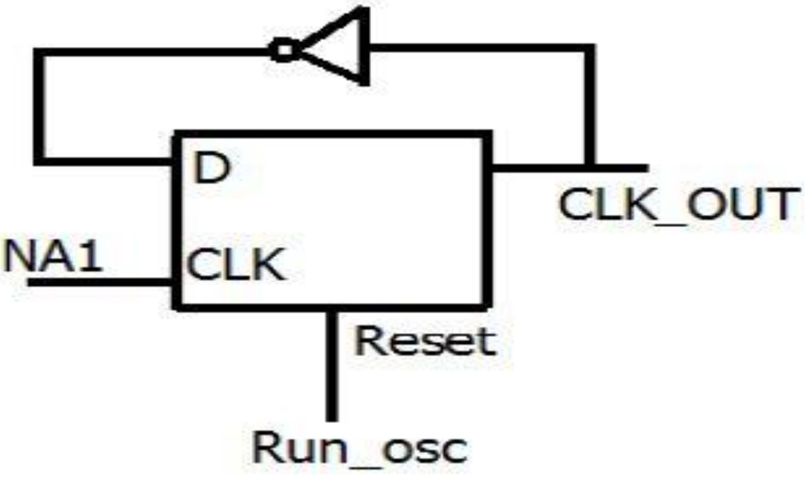

Figure 4.2-1 Basic D flipflop

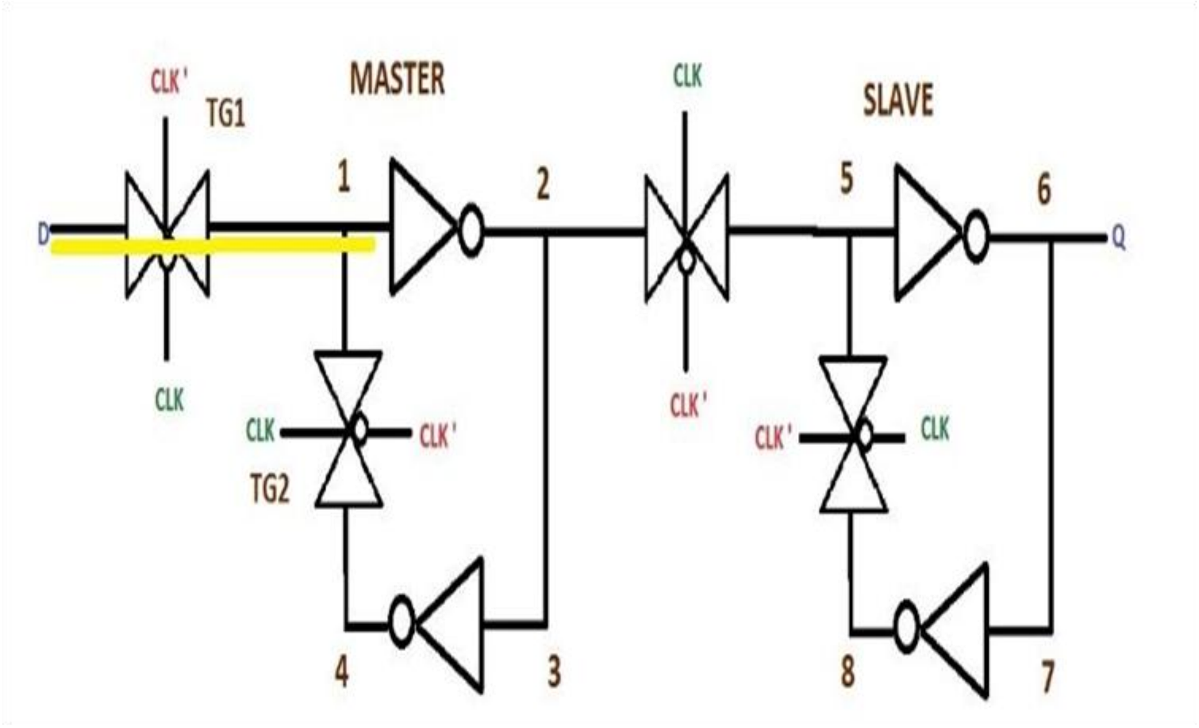

Figure 4.2-2 Basic CMOS Latch

4.3 METHOD USED FOR PROCESS VARIATION COMPENSATION

The Current Mirror Mechanism is firstly used to generate current independent of Temperature as discussed in Section 2.3. For PVT compensation, I had generated a specific Gate to Source Voltage Vgs, to generate current of 1µA. Another MOS is used as a switch to on or off, the current flow for low power consumptions.Then this block is iterated several types as per the need of current. This makes the circuitry compact and more efficient. Then these same current generating blocks are further used as trimming bits for process compensations. Lesser current required for typical and Max corner. Similarly more current required for others .The figure 4.1-1 do consists of the same block used four times.

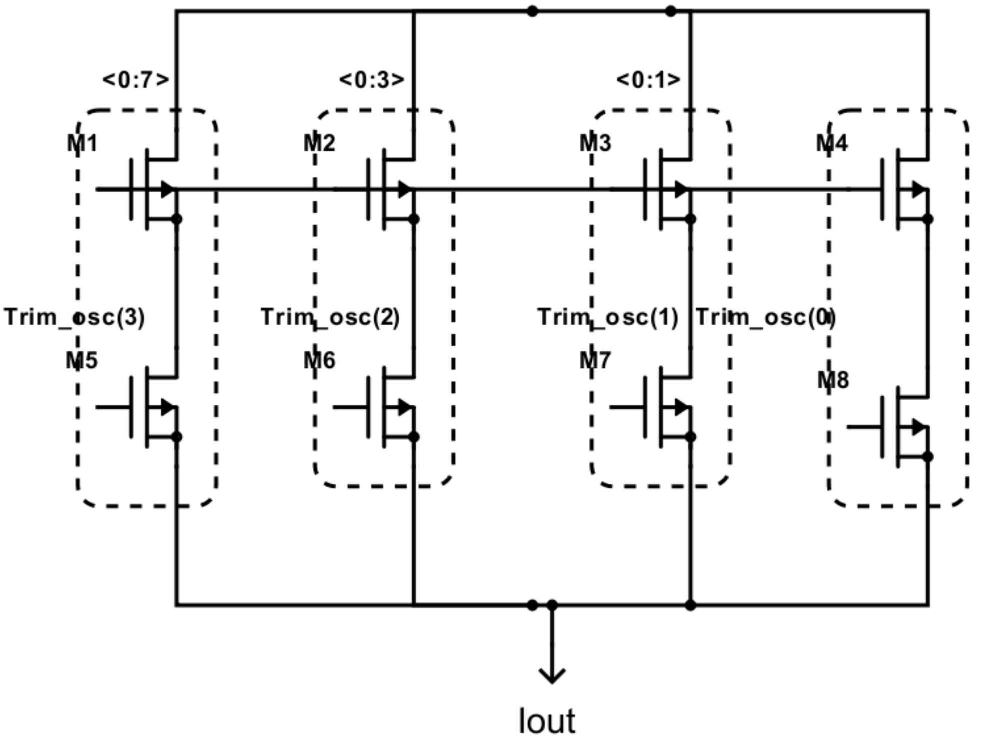

Figure 4.3-1 Trimming Bits

Moreover, Eq(4.4) also suggests that the dependence of VGS3 on the process can lead to variation in the charging time of the mos capacitor. Therefore, if the V_{cap}/I_{cap} ratio remains constant then only the charging time can be made fixed across process variations. In order to achieve this, the capacitor-charging current can be modulated using trimming bits according to different process corners. In Figure 4.1-1, $T_0 - T_4$ are the trimming bits transistors, they are used as switches for $M_{13} - M_{17}$ mos transistors. These bits modulate the equivalent width of the transistor M_{10} for the current mirror action. From Eq.(4.1) it can be figured out that for decreasing the capacitor charging current (I_{cap}), one can increase the width of the transistor M_{10} similarly, for increasing the capacitor charging current, I can increase the width of M_{11}. This programming ability in design provides the ease to the designer to correct the oscillation frequency of oscillator during calibration of the oscillator.

4.4 METHOD OF TEMPÉRATURE VARIATION COMPENSATION

From Eq. (4.2), I_{cap} current and capacitor (C) are temperature independent terms but somehow, V_{cap} is dependent on temperature variations. However, the temperature dependence of V_{cap} or V_{GS3} is Probable in Eq.(4.4). If the negative temperature coefficient of the threshold voltage is made equal to the positive temperature coefficient of the overdrive voltage of M3, then this dependence of VGSM3 on temperature can be nullified. The temperature coefficient of the threshold voltage is technology dependent [14] but the temperature coefficient of overdrive voltage is dependent on the aspect ratio of the transistor, hence proper sizing of M3 can compensate the variations arising in VGS3 due to temperature.

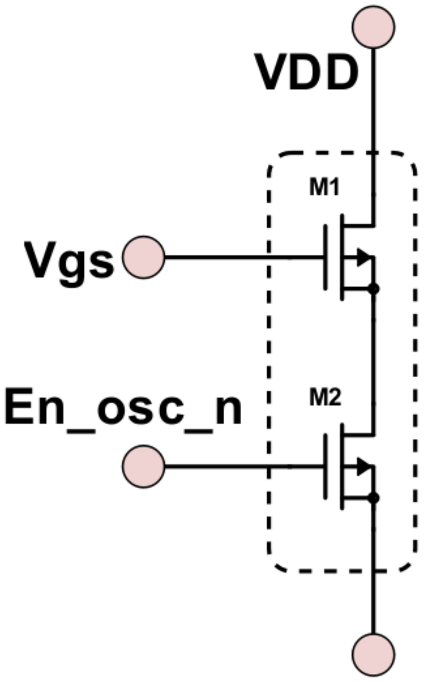

Figure 4.4-1 Current Mirror Unit

4.5METHOD OF VOLTAGE VARIATION COMPENSATION

The supply voltage variations will not have any prominent impact on the frequency of oscillation since $T_{charging}$ does not have any dependence on the supply voltage. The inverter stages biased at supply voltage will have no impact on oscillation frequency as they do not provide significant loop delay. The total loop delay (T_{delay}) and the frequency of oscillation (f_{osc}) can be expressed as:

$$T_{delay} = T_{stage1} \quad (4.5)$$

$$T_{Stage1} = T_{Charging} \quad (4.6)$$

$$f_{OSC} = \frac{1}{T_{delay}} = \frac{I_{cap}}{CV_{cap}} \quad (4.7)$$

From Eq.(4.7), it can be inferred that the frequency of the proposed ring oscillator is not a supply voltage dependent term. The process variations are compensated by varying the capacitor charging current I_{cap} across different process corners and the temperature variations that mark an impact on the term V_{cap} are compensated by proper sizing of transistor M_3.

The BCD technology is so self-made platform with the lesser power consumptions but the tradeoff is the feature size and the technology used 90nm is the smallest one achieved yet in this particular technology. Henceforth, the results obtained in order to make it PVT Compensated without much extra circuitry and without any compromise with area utilized. Here, in this proposed architecture, the worst case variation is obtained in the Max corner.

Here, in figure 4.3-1, the results of the Behavior of different stages of Oscillator have been shown. It tells about the maximum and minimum obtained due to the addition of ripples in the output. And figure 4.3-2 tells about the Behavior of MOS as a capacitor used for the proposed circuit.

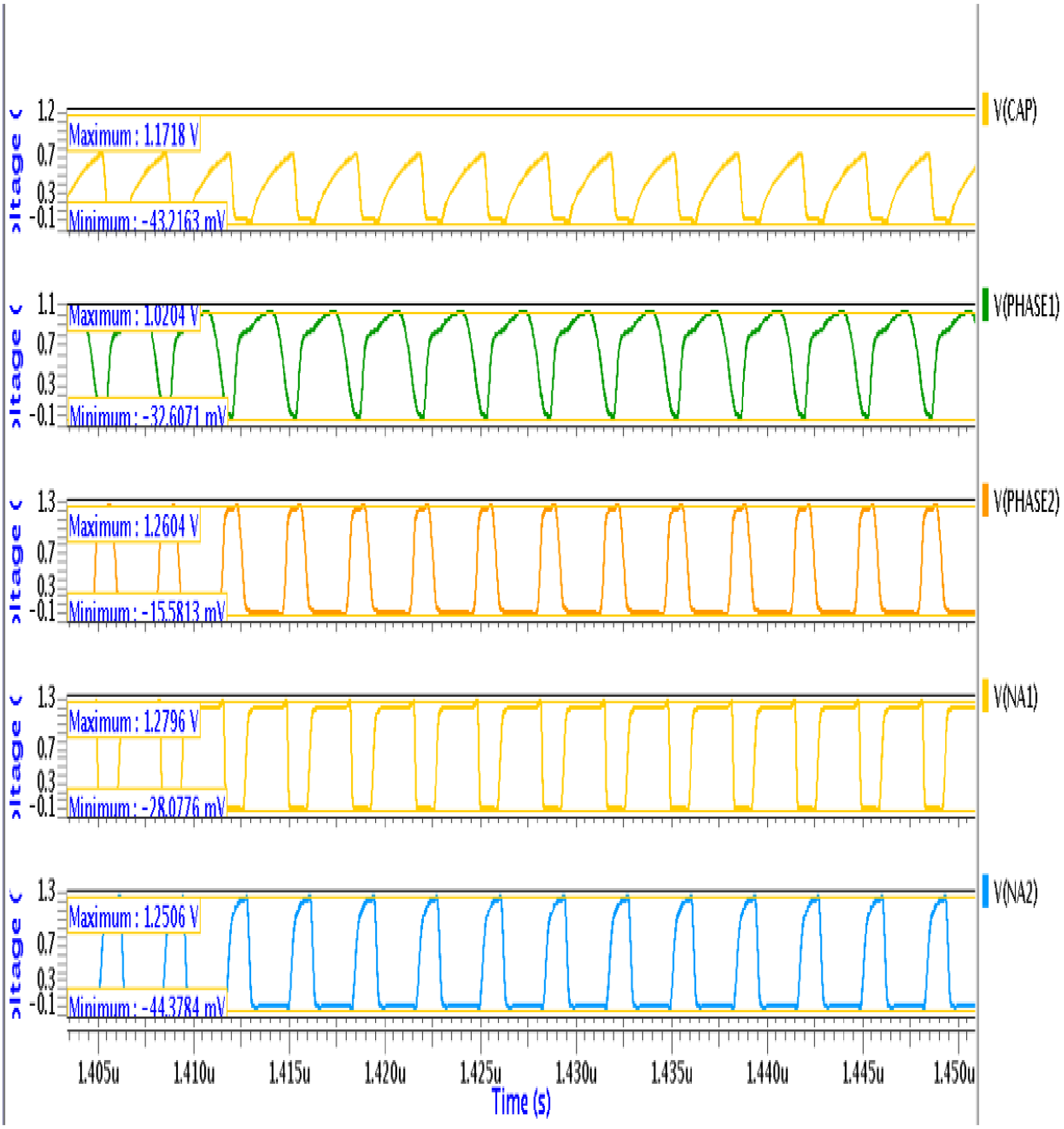

Figure 4.5-1 simulation results of 5 stages of Oscillatoire

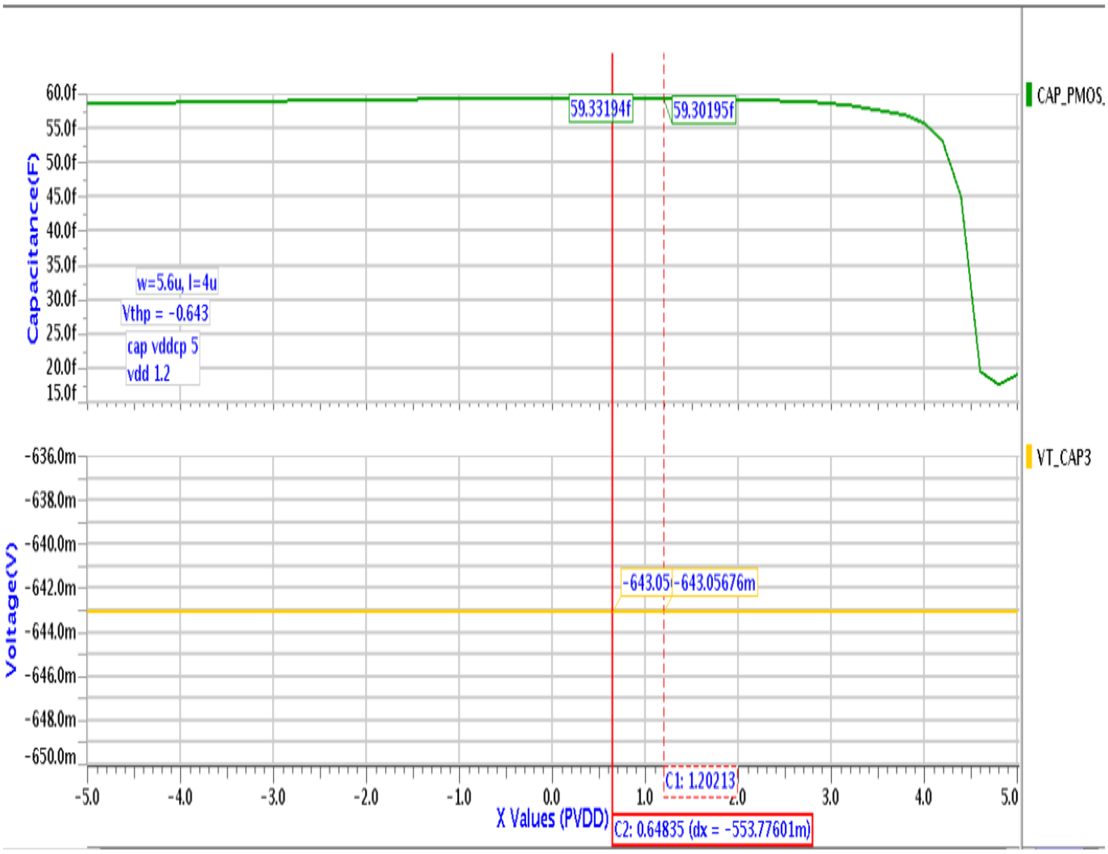

Figure 4.5-2 MOS capacitance and threshold voltage used in the proposed circuit

Mos capacitance of 60fF is used for area minimization. Here, in figure 4.3-2 the Threshold voltage variation is also shown of the MOS capacitance. Also, the Clock frequency which is prevailed after passing the output of oscillator through the D flip flop is shown in figure 4.4.3, It also includes the CLKN signal which is essential for clock gating and pass transistor purposes. Duty cycle is properly acquired and somehow few glitches are also noticeable in this at clock pulse. Figure 4.3.4 is the one showing the variation of the clock pulse in accordance with the capacitor. The method use dis previously described in chapter 2 by comparing both NMOS and PMOS for the usage. But for the easy biasing the pmos is preferred. As the current mirror used, is also designed for pmos and hence symmetry of circuit is maintained. Biasing is advantage and the region of operation is covered more in the case of pmos,for MOS as a capacitor operations.

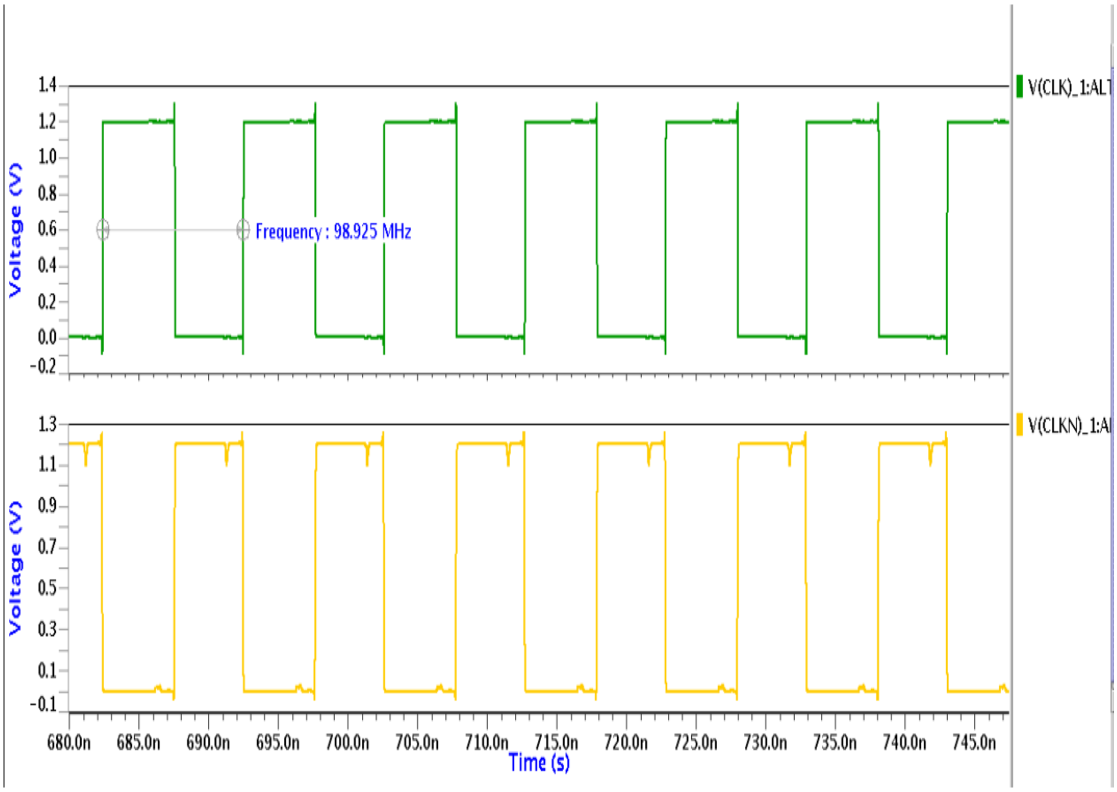

Figure 4.5-3 Operating frequency of Oscillator in typ corner

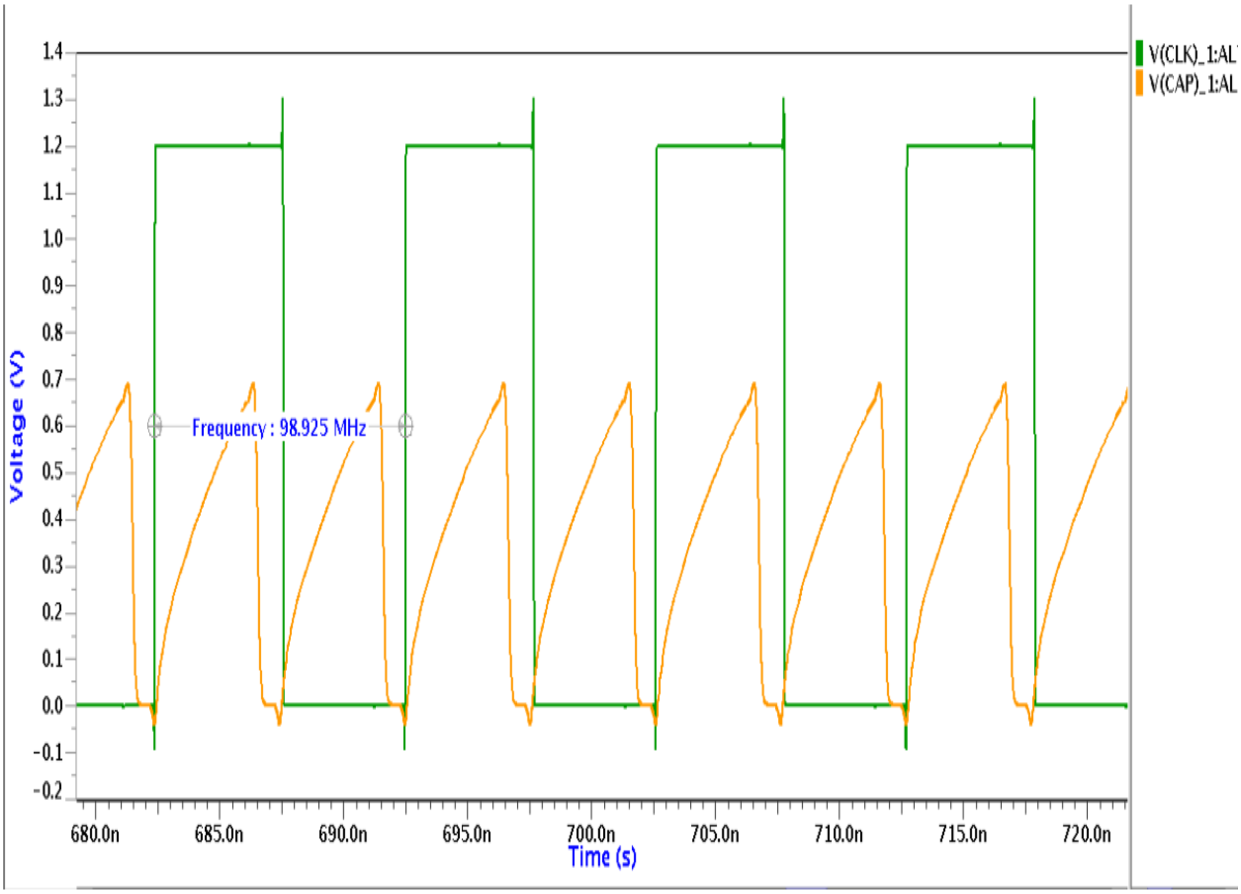

Figure 4.5-4 Variation with Cap voltage as it is twice the capacitor charge and discharge oscillation

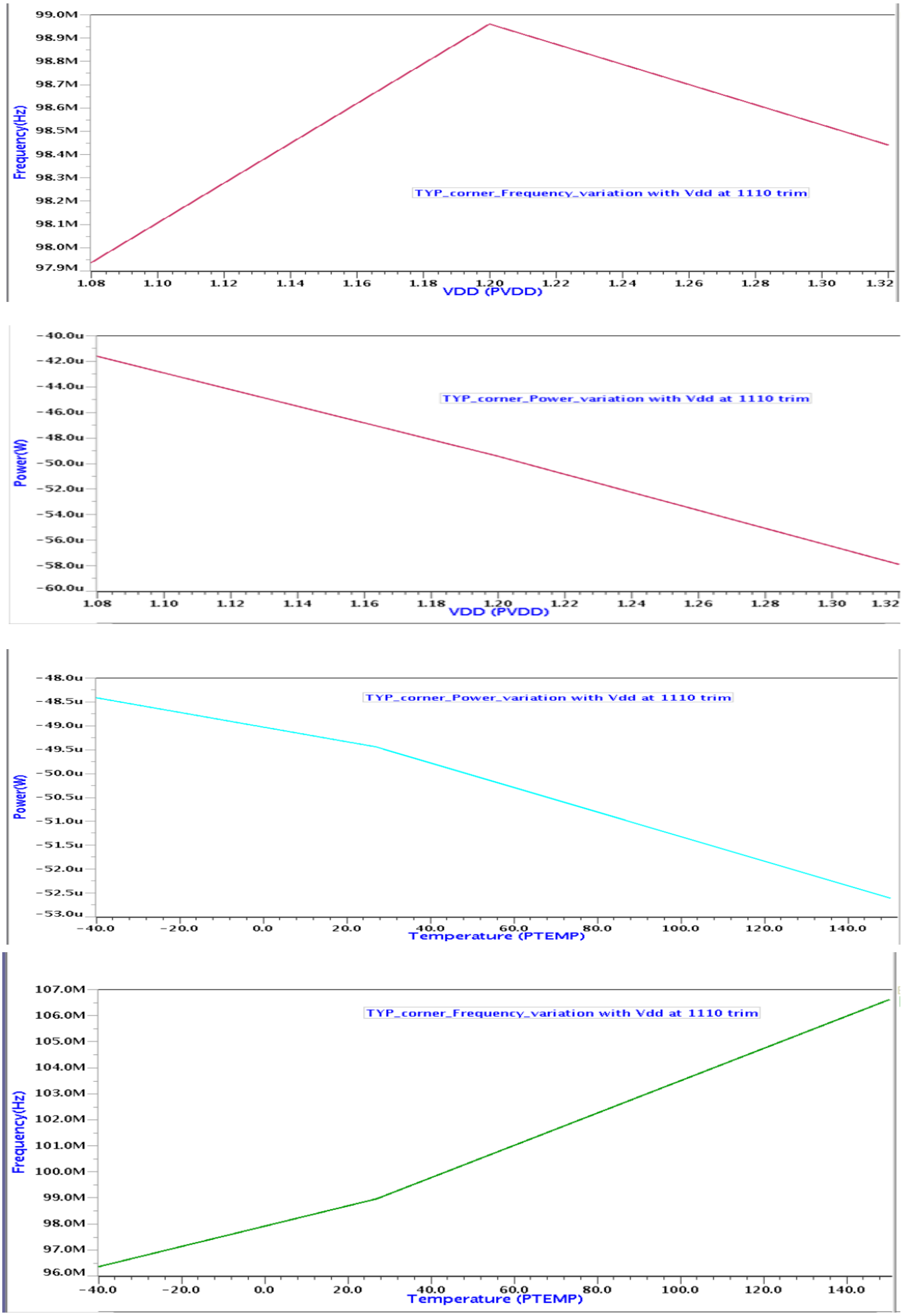

Figure 4.5-5 Variation with voltage and temperature in Typ corner at trim bit 1110

Typical Corner results with variations in Temperature and Voltage are shown above. Power variations from 42µW to 58µW in the case of supply voltage variation ranging 1.08V (minimum) to 1.32V (maximum). Whereas, for the temperature variation ranging -40° to 150°C power dissipation can be seen as 48µW to 53µW. Similarly, Frequency variations in the case of supply voltage variations corresponds to 97Mhz to 98.9Mhz and with respect to temperature variations it results to 96Mhz to106Mhz.

Maximum corner shows the variation of power from 51µW-59µW and 44µW-64µW for temperature and voltage variations respectively. Whereas, the frequency variations are from 100Mhz-113Mhz and 102Mhz to 104Mhz for temperature and Voltage variations respectively.

Minimum corner shows the variation of power from 44µW-57µW and 40µW-60µW for temperature and voltage variations respectively. Whereas, the frequency variations are from 96Mhz-102Mhz and 87Mhz to 102Mhz for temperature and Voltage variations respectively.

NmaxPmin corner shows the variation of power from 51µW-62µW and 44µW-56µW for temperature and voltage variations respectively. Whereas, the frequency variations are from 100Mhz-108Mhz and 100Mhz to 102Mhz for temperature and Voltage variations respectively.

NminPmax corner shows the variation of power from 51µW-56µW and 44µW-62µW for temperature and voltage variations respectively. Whereas, the frequency variations are from 99Mhz-107Mhz and 100Mhz to 102Mhz for temperature and Voltage variations respectively.

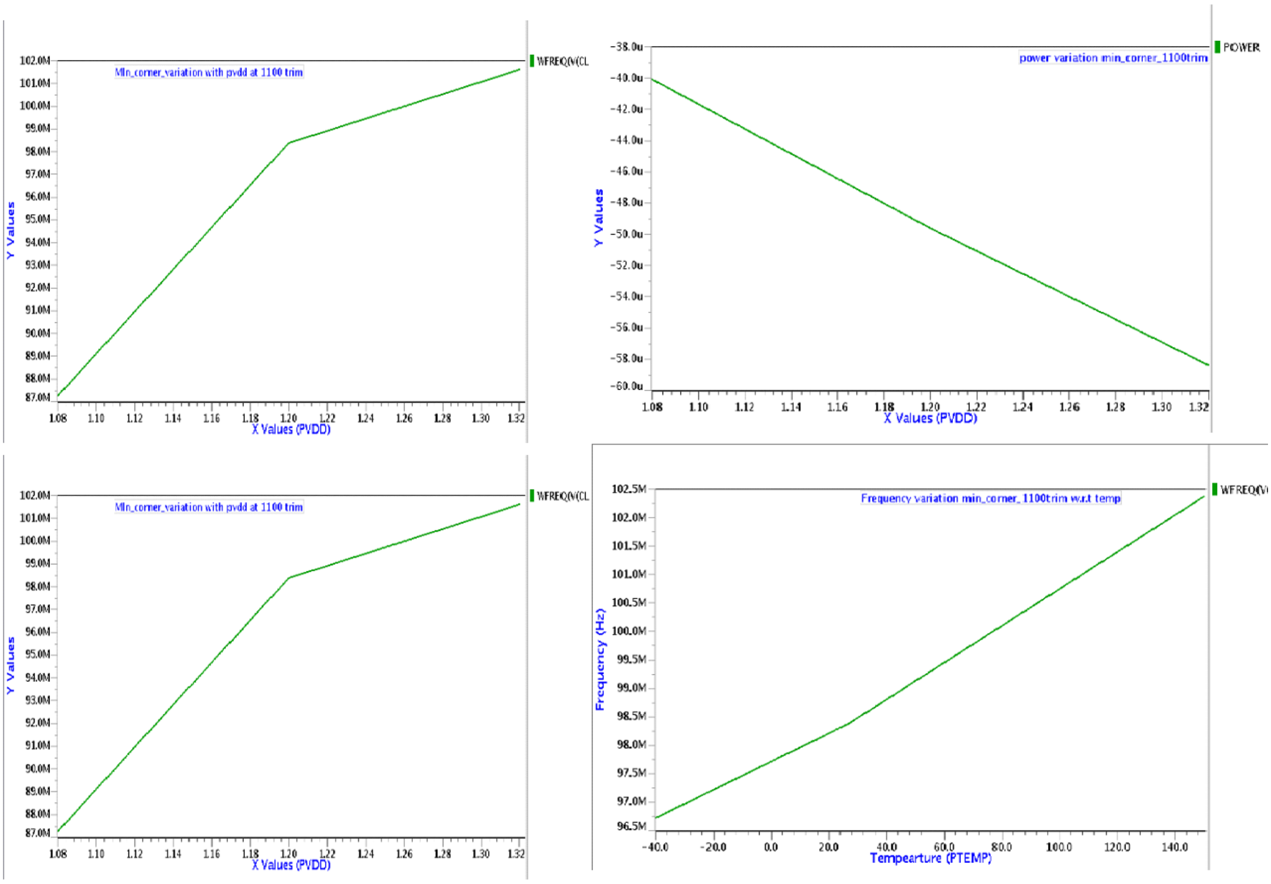

Figure 4.5-6 Variation with voltage and temperature in Min corner at trim bit 1100

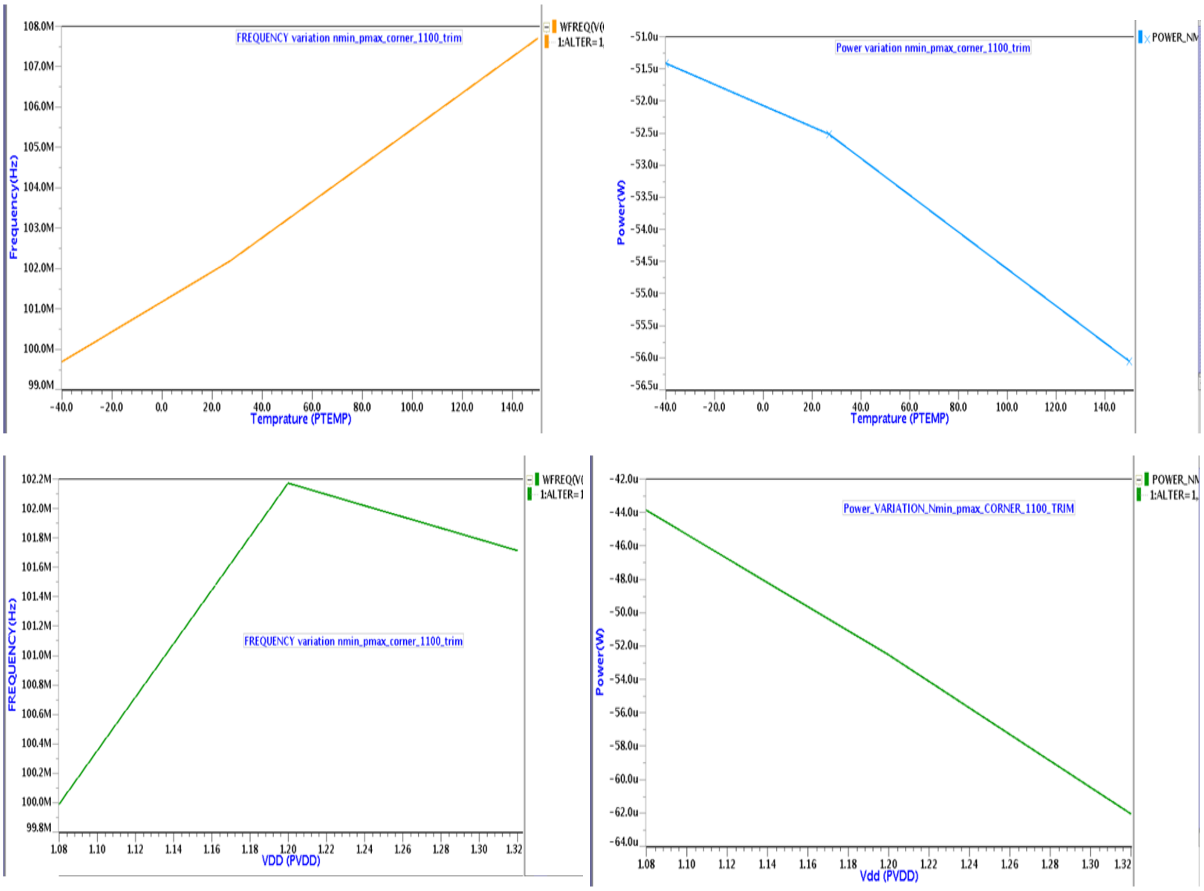

Figure 4.5-7 Variation with voltage and temperature in Nmin_Pmax corner at trim bit 1100

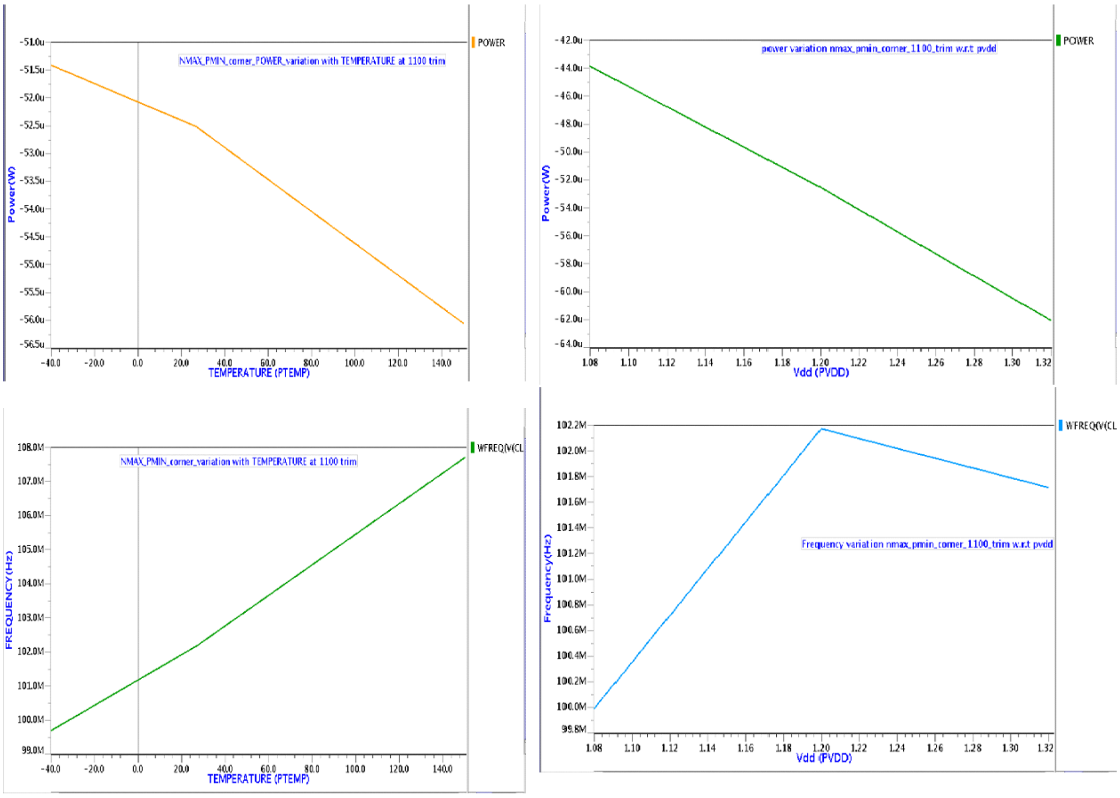

Figure 4.5-8 Variation with voltage and temperature in Nmax_Pmin corner at trim bit 1100

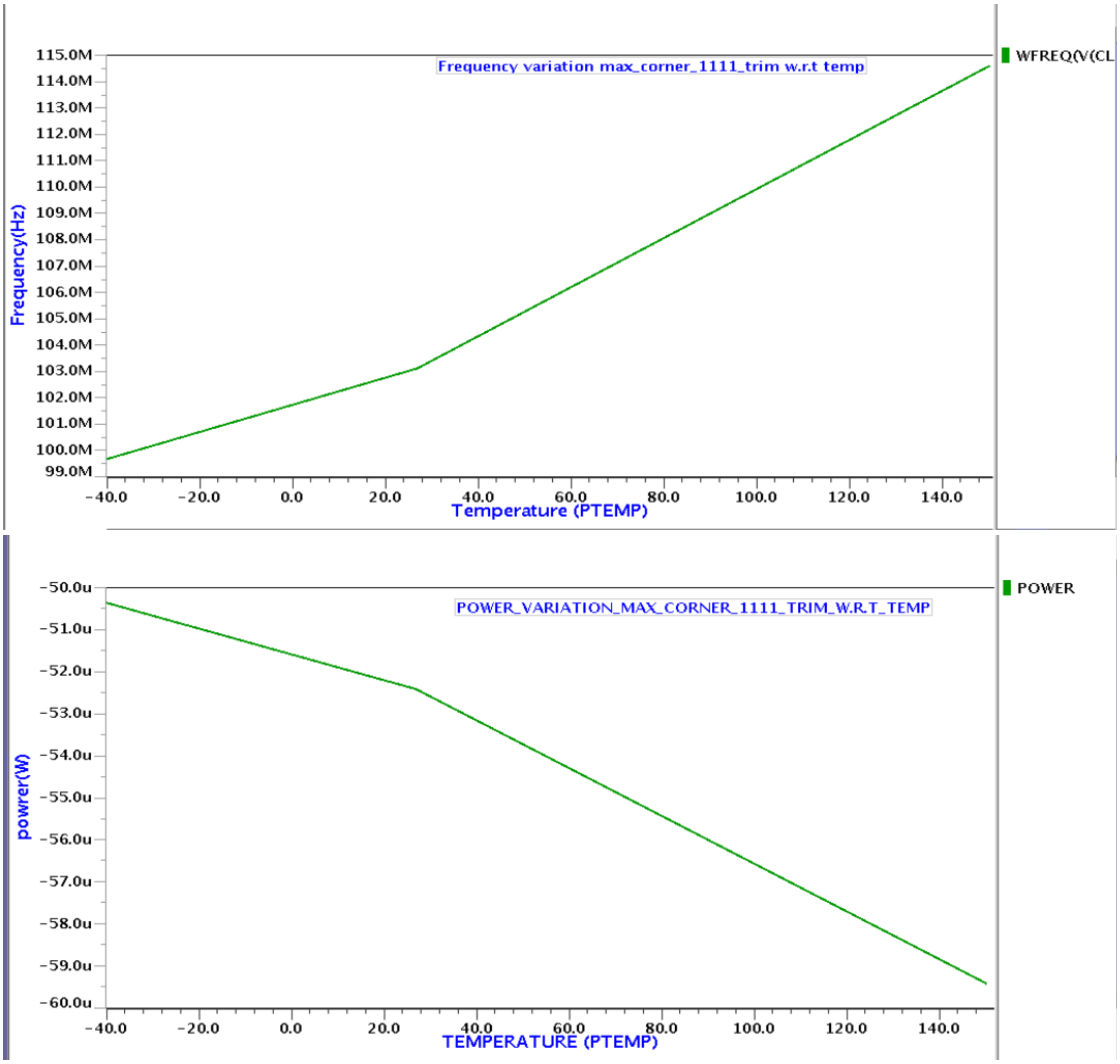

Figure 4.5-9 Variation with temperature in Max corner at trim bit 1111

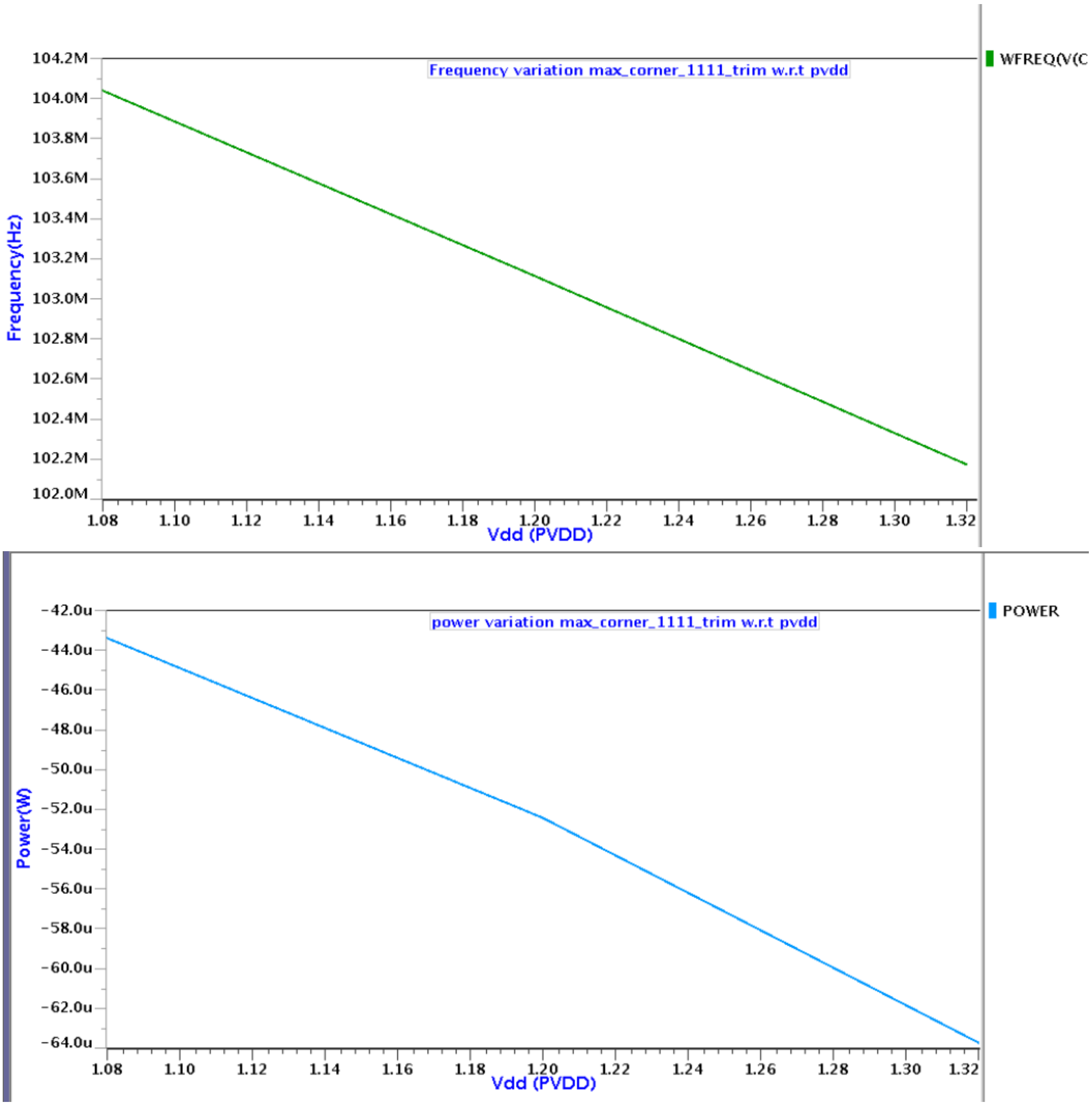

Figure 4.5-10 Variation with voltage in Max corner at trim bit 1111

Table 1 Specifications of Voltages

Load Capacitance	0-70 fF
Input Supply	1.08V – 1.32V
Reference Current	10uA - 25uA

Table 2 Comparaison of Power(W)

Sr. No	Corner	Power(W) (BASIC)	PROPOSED(W)

1	TYP	106.51u	49.442u
2	MAX	161.41u	55.001u
3	MIN	69.459u	45.937u
4	NMAX_PMIN	93.612u	51.005u
5	NMIN_PMAX	112.67u	48.293u

Table 3 Comparaison of delay

Stages	Basic OSC (delay) $Ʈ_{phl} + Ʈ_{plh}$	Proposed (delay) $Ʈ_{phl} + Ʈ_{plh}$
1	0.99ns	2.25ns
2	1.0ns	0.47ns
3	1.3ns	0.30ns
4	0.8ns	0.39ns
5	0.83ns	1.46ns

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 CONCLUSION

Two Ring oscillators are designed in 90nm BCD10 Technology for Non-Volatile Memories.

The Current starved architecture is being followed up in this. The proposed oscillator is made temperature compensated inherently, hence; does not require any extra on-chip feedback circuit or analog block for further temperature compensation. Digital trimming technique is employed for process compensation in the presented designs. The proposed strategy of ring oscillator design exhibits significant less spread with temperature variations and with the incorporation of digital trimming, the spread is reduced from conventional (untrimmed) to this for an operating temperature range of -40° to 150°C. The proposed Oscillator had power dissipation of 40µW-65µW, frequency Variation of approx. ±15%, within the temperature range of -40° to 150°C, and supply voltage variation of ±10%, across all process Corners. The total power consumed by conventional and compensated ring oscillator in the worst case is approx. 161µW and 55µW respectively. For the specific Trim bits applied, the Variation reduced to ±5% for room temperature 27° considerations. The proposed oscillators design strategy achieves significantly less temperature dependence and low power consumption than another oscillator circuit. Moreover, in the proposed technique delay is reduced by taking more of a delay from one stage only instead of distributed delay.

5.2 FUTURE WORK

This work can be extended further to perform the phase noise analysis of proposed oscillators. Moreover, More PVT compensation strategy can be employed in this as discussed in chapter 3 by using a voltage regulator, other process compensated circuits. Further few latch-based techniques or level shifter-based stages can also be used in this, by which the voltage level may also increase. Here on-chip voltage regulator design may improve this more. This improvement in compensation strategy can result in a significant reduction in on-chip compensation capacitor. The improvements in the circuitry can be added at the cost of more area, by using other compensated current starved architectures. As per the specs offered and the need of time many variations can be offered. The Voltage regulator with miller compensations and voltage buffer compensations can be used further. The Size of Mos capacitor can be varied for any further change in frequency requirements.

CHAPTER 6

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