Modeling and Performance Analysis of Double Gate Carbon Nanotube Field Effect Transistor

A Thesis

Submitted in fulfilment of the requirement for the award of the degree

of

DOCTOR OF PHILOSOPHY

In

Electronics and Communication Engineering

Submitted by

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DECLARATION

I hereby declare that the work which is presented in thesis titled, **"MODELING AND PERFORMANCE ANALYSIS OF DOUBLE GATE CARBON NANOTUBE FIELD EFFECT TRANSISTOR"** in the partial fulfillment of the requirement for the award of degree of Doctor of Philosophy in Electronics and Communication Engineering Department of Thapar Institute of Engineering and Technology, Patiala is an authentic record of my study carried out as under the supervision of **Dr. Karmjit Singh Sandha**, Associate Professor, ECED. The content presented in the thesis does not contain any matter which is previously published or written by any other person exempting the reference are provided in the text. The simulations and results presented in thesis has not been submitted by me for the award of any other degree of any other University/Institute.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief. She has worked under our supervision and fulfilled the criteria for the submission of this thesis.

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" Develop an attitude of gratitude and give thanks for everything that happens to you, knowing that every step forward is a step toward achieving something bigger and better than your current situation."

- Brian Tracy

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ABSTRACT

Since several years ago, it has been understood that silicon transistors are difficult to further shrink after a particular feature size. In next decade or two, ability to advance MOSFET technology will start to decline, necessitating a rush to find a replacement. The present research investigates the possibility for replacing traditional MOSFETs due to a variety of short channel effects including threshold voltage variations, leakage current and drain-induced barrier lowering at nanoscale. Researchers are looking at using carbon nanotubes—rolled-up graphene sheets—instead of silicon in electronic devices. Replacement of MOSFETs with this new kind of transistors, referred to as carbon nanotube field effect transistors (CNTFETs), is currently a leading technology at nanoscale. With their excellent thermal conductivities, high current drivability and superior transport characteristics, use of CNTs have emerged as a potential replacement for bulk CMOS technology. Despite all development and advancement, various challenging issues still need to be resolved. Therefore, in order to proceed in research, this thesis reviews all previously done research and explains the research that will be needed in future to produce large-scale VLSI chips using CNTFETs.

Models for design and study of CNTFETs are presented in this thesis. Applications for these transistors in emerging field of nanotechnology are being given important consideration. In this work, double gate carbon nanotube field effect transistor (DG-CNTFET) are considered to overcome various short channel effects. An analytical model that is temperature dependent has been proposed for drain current of DG-CNTFET to analyse device performance at variable temperature range. This developed model is used to obtain current-voltage characteristics of DG-CNTFET in MATLAB to compare results obtained in nano TCAD ViDES. For varying temperature ranges, several performance parameters including output characteristics, ON and OFF currents, subthreshold swing and drain conductance have also been obtained to analyze the effect of thermal environmental conditions on device performance. Subthreshold swing increases with rise in temperature and drain conductance increased by 4 times when there is increase in temperature from 250 K to 400 K.

Further, temperature dependent performance analysis of threshold voltage and channel parameters' effect on threshold voltage of DG-CNTFET are presented. To evaluate device performance under thermal environmental conditions, temperature effects have been taken into account. Also, evaluation of DG-CNTFET and DG-MOSFET's threshold voltages at varying temperatures has been performed. It was found that the DG-CNTFET has small variation in

threshold voltage at different temperatures, which makes it more appropriate to use in applications where thermal environmental conditions must be taken into account for design purposes. This is because of unique property of thermal stability found in CNTs in comparison to DG-MOSFET. These results can be effectively applied to these devices' design considerations.

CNTFETs have become prominent in arena of applications. One of the major applications in which CNTFET can be applied is SRAM cell. SRAM is a kind of memory that is frequently utilized in low power consuming gadgets. In fact, SRAM cells use the majority of transistors present in many integrated circuits, accounting for 85%–90% of integrated circuits on die used for this type of memory. Scaling down SRAM has become necessary due to increased requirement for low power, high speed devices like smartphones and tablets as well as introduction of IoT devices. Since standard CMOS devices are used to make SRAM, all issues with MOSFET scaling also exist for SRAM scaling.

This research focuses on analysis of 6T CNTFET SRAM cell, including its benefits and drawbacks when compared to CMOS based 6T SRAM cell, as well as several performance parameters including propagation delay, power dissipation and power delay product (PDP). Furthermore, CNTFET technology has been used to analyze SRAM cell and it is then a comparison is made with CMOS 6T SRAM cell. The goal is to find trends for various parameters at various technology nodes. Various findings have been obtained after the models are simulated. The results showed that 6T SRAM cell based on CNTFET outperforms CMOS based 6T SRAM cell due to its lesser power dissipation and propagation delay which can further be used for low power and high speed applications. It was concluded that CNTFETs are better contender to replace traditional MOSFETs at nanoscale in VLSI industry as it reduces several short channel effects.

LIST OF PUBLICATIONS

SCI/SCIE INDEXED

1. **Aakanksha Lakhanpal** and Karmjit Singh Sandha, "Impact of channel parameters on threshold voltage at variable temperatures of Double Gate CNTFET," *Micro and Nanostructures*, vol. 164, p. 107168, 2022. **(SCI indexed-Impact Factor-3.1)**
2. **Aakanksha Lakhanpal** and Karmjit Singh Sandha, "Impact of Thermal-Aware Enviromental Conditions on Double- Gate Carbon Nanotube FET," *Microelectronics Journal*, vol. 114, p. 105146, 2021. **(SCI indexed-Impact Factor-2.2)**
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CONFERENCES (SCOPUS INDEXED)

1. **Aakanksha Lakhanpal** and Karmjit Singh Sandha, "Impact of variable temperature on the performance analysis of CNTFET and CMOS-based SRAM Cells," in International Conference, *Recent Advancements in Communication, Computing and Artificial Intelligence (RACCAI)*, 2023. (**Accepted)**

ACRONYMS AND ABBREVIATIONS

Abbreviation	Description
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nanotube
CNTFET	Carbon Nanotube Field Effect Transistor
CVD	Chemical Vapour Deposition
DG-CNTFET	Double gate Carbon Nanotube Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
GNRFET	Graphene Nanoribbon Field Effect Transistor
IC	Integrated Circuit
ITRS	International Technology Roadmap of Semiconductor
LSI	Large Scale Integration
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSI	Medium Scale Integration
MWCNT	Multi Walled Carbon Nanotube
PDP	Power Delay Product
PTM	Predictive Technology Model
SCE	Short Channel Effects
SPICE	Simulated Program with Integrated Circuit Emphasis
SLSI	Super Large Scale Integration
SSI	Small Scale Integration
SRAM	Static Random Access Memory
SWCNT	Single Walled Carbon Nanotube
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

GLOSSARY OF SYMBOLS

Symbol	Description
a_1 and a_2	Basis Vectors
C_h	Chiral Vector
C_{ox}	Oxide Capacitance
C_q	Quantum Capacitance
d	Diameter of CNT
$D\ (E)$	Density of States
E_c	Minimum Conduction Band Energy
E_F	Fermi level of CNT
E_g	Bandgap
ΔE_F	Fermi Level
$f\ (E)$	Fermi-Dirac distribution
$g\ (E)$	Volume per unit Energy
g_d	Drain Conductance
h	Planck constant
I_{ds}	Drain Current
k	Boltzmann constant
L	Carbon Nanotube Length
L_D	Length of drain
L_G	Length of gate
L_S	Length of source
m	Particle's Effective Mass
$M\Omega$	Megaohms
N_c	Effective density of states at the edges of conduction band
$n_{cnt,i}$	Intrinsic Charge Carrier Concentration
$N\ (E)$	Number of Particles
Q_{cnt}	Charge on CNT
Q_{01} and Q_{02}	Charge on an oxide layer

Q_{subs}	Charge on a Substrate
Q_g	Charge on Gate
t_{ox}	Thickness of oxide layer
r	Nanotube' Radius
T	Operating Temperature
V_{cb}	Potential induced by Source
V_{ds}	Drain to Source Voltage
$V_{pp\pi}$	Energy of carbon π-π bond
V_{fb}	Flat Band Voltage
V_{gb}	Gate to Substrate voltage (back gate)
V_{gs}	Gate to Source Voltage
V_{th}	Threshold Voltage
ψ_{subs}	Substrate to back gate surface potential
ϕ_{ms}	Work Function of gate to substrate
ψ_{cnt}	Potential across CNT
Θ	Chiral Angle
Φ_0	Surface Potential of back gate
ξ_o	Oxide Material's dielectric constant
Ψ_{cnt}	Surface Potential of front gate

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CHAPTER 1
INTRODUCTION

1.1. OVERVIEW

With invention of various electronic devices and gadgets, the human life and their livelihood has changed a lot. These have become a boon to the human society in areas such as medicines, transportation, security and communication networks.

Around 1970s, nearly ten thousand transistors were found in an integrated chip (IC). With advancement in technology in VLSI (Very Large Scale Integration) and semiconductor industry, a single IC has a large number of transistors. In recent years (2010-2020), numbers of transistors integrated on one chip have reached around ten billions with the feature size smaller than fifteen nanometres [1]. Due to rapid advancement and enhancement in the performance, feature size, area, speed, cost and power of an IC, electronics industry has made tremendous growth for the last forty years.

A germanium based semiconductor transistor was invented in AT&T Bell Laboratory by three physicists in 1947. The reduced size and power consumption of this transistor, gave faster response and well suited for working at relatively lower temperature as compared to the vacuum tube based transistors. These advantages pave a way for solid-state electronic devices and replaced the vacuum tube transistors. Electronic industry has undergone an evolution as a result of the extensive usage of silicon based transistors in electronic circuits.

Six names were proposed by Bell Telephone Laboratories [1] for the first germanium based transistor. Initially, name given to first germanium based semiconductor transistor was ‘semiconductor triode’ which was later changed to ‘transistor’. Word ‘transistor’ is the combination of ‘transconductance’ and ‘varistor’.

Due to its better performance as compared to germanium based transistor, silicon transistor was manufactured by Dr. Gordon Kidd Teal and was made available commercially for the first time. Thus, silicon replaced the germanium as the substrate material. In 1960, an epitaxial layer was added on to the transistor to decrease the resistivity of collector. Further in the same year, planar transistor was introduced [2].

The planar transistor was manufactured in layers and has all the connections in same plane. Planar transistor had base of semiconductor material as its first layer on which some impurities

were added to form second layer. After that, centre of the second layer was etched out. When the centre of second layer was etched out, a thin layer remained on base in form of bowl which was square in shape. Also, thick edges were formed around the sides of second layer. The material of polarity which was opposite in nature as compared to other two layers were placed in the bowl. Again, the centre of layer was removed to form a bowl which was smaller in size. The similar material as that of first layer was added. Also, second, third and fourth layers were removed. When the components were well placed, only then the metal connectors were attached to transistor for conducting electricity. First layer of planar transistor was used to receive input and gives output from fourth layer. Further, third layer was used to amplify the input.

The first integrated circuit was composed of a transistor, one capacitor & three resistors wired together made up of platinum were mounted on a germanium bar of 0.5 inch and was introduced by Jack St. Clair Kilby in 1958. In 1959, the IC chip was invented which was made by etching technique depositing the aluminium film on to the oxide layer.

Dr. Gordon Earle Moore proposed Moore's Law in 1965. This law's prediction states that total number of components (including capacitors, diodes, transistors, resistors, inductors, and other components) would double every year [3]. To observe the components, increase in an integrated chip for coming generations, in the microelectronics industries, Moore's law has been frequently used [4]. But for only more than half a century, Moore's law held valid.

Moore's Law has significant implications for how rapidly technology will advance in the future—as well as its possible limitations. Computers will ultimately reach physical limitations because transistors will not be able to sustain operation in smaller circuits at increasing temperatures. This is due to the fact that cooling the transistors will require more energy than the transistors themselves are consuming.

Industry is looking for new ways of thinking to continue exponential development as the ability to scale a single chip slows. Innovation has accelerated due to growing popularity of big data and artificial intelligence applications and rising demand for "more than Moore" law. This is termed as "Post Moore's" law [4].

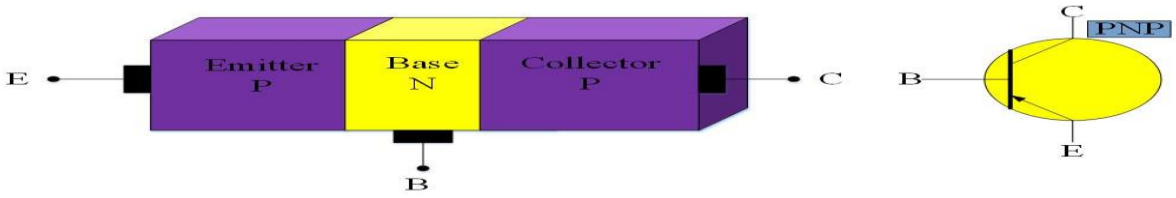
Table 1.1. Level of integration for an IC [5].

Sr. No.	Level of Integration	Year	Number of transistors in a single chip
1.	Small-scale integration (SSI)	1950	Less than 100
2.	Medium-scale integration (MSI)	1960	Between 100 and 1000
3.	Large-scale integration (LSI)	1970	Between $10^3$and 10^4
4.	Very large-scale integration (VLSI)	1980	Between 10^4 and 10^5
5.	Ultra large-scale integration (ULSI)	1990	Between $10^5$and 10^7
6.	Super large-scale integration (SLSI)	2000	Between 10^7 and 10^9
7.	Giga-scale integration (GSI)	2010	Between 10^9 and 10^{11}
8.	Tera-scale integration (TSI)	2020	Between 10^{11} and 10^{13}

Table 1.1. describes integration level for an IC. Table shows that numbers of transistors being fabricated in a chip has increased continuously throughout years. Level of integration are designated in the table in accordance with increase in transistors in every ten years. It is shown in the table that number of transistors within a semiconductor chip was around ten thousand to one lakh in the year 1980. To increase the packaging density and faster speed of device, more and more components have been fabricated in a single chip and its number raised from one billion to ten billion transistors in a single chip for the year 2010. Now a days, numbers of transistors being fabricated on a single chip are more than ten billion transistors [5].

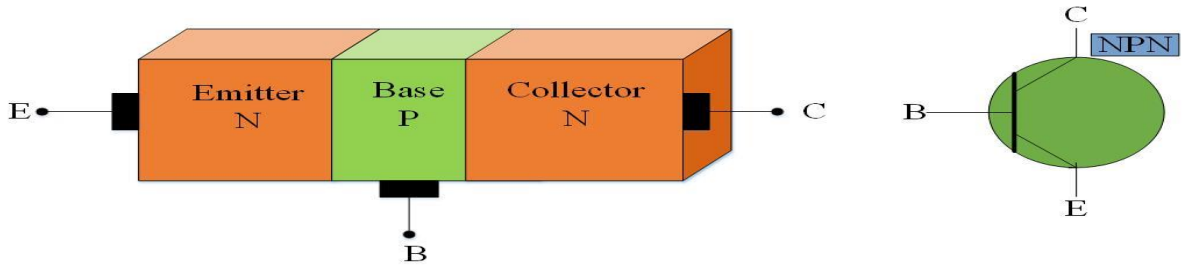
The widespread use of electronics in modern world has made it possible for transistors to be utilised in every electronic circuit in several ways. We are all familiar with the employment of transistors as switching devices and amplifiers in daily life. They are employed as amplifiers in a variety of oscillators, modulators, detectors, and almost every circuit to carry out a task. Transistors are used as switches in digital circuits. There are several varieties of transistors for different functions, such as those for working at low and high frequencies. Nowadays, the growth of nanotechnology in different fields has boosted tremendously the multidisciplinary nanoscaled research leading to the emergence of new high-performance nanodevices [198].

Based on either their design or their mode of operation, transistors have been divided into various categories since the first transistor was created. The transistors have been divided into two kinds namely bipolar junction transistors (BJT) and field effect transistors (FET).



(a) (b)

Figure 1.1. (a) Structure and (b) symbol of *pnp* -bipolar junction transistor (BJT) [6].

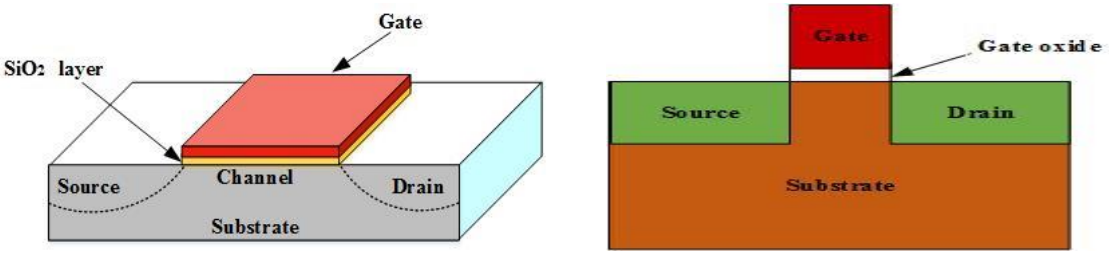


(a) (b)

Figure 1.2. (a) Structure and (b) symbol of *npn* -bipolar junction transistor (BJT) [6].

Three doped semiconductor regions constitute a BJT namely base (B), emitter (E), and collector (C). Two types of BJTs are *pnp* and *npn* and their symbols are represented in figure 1.1. and 1.2. These transistors can be used to make amplifiers because their main purpose is to amplify current. The disadvantages of BJT over FET include less thermal stability, more heat dissipation and low switching speed which makes it unsuitable for fabricating in integrated chips.

These days, transistors which are fabricated in integrated chip are mostly Metal- oxide field effect transistors (MOSFET) [7]. Planar nature of silicon based MOSFET was presented in 1963. The first CMOS logic circuit was also invented in the same year.

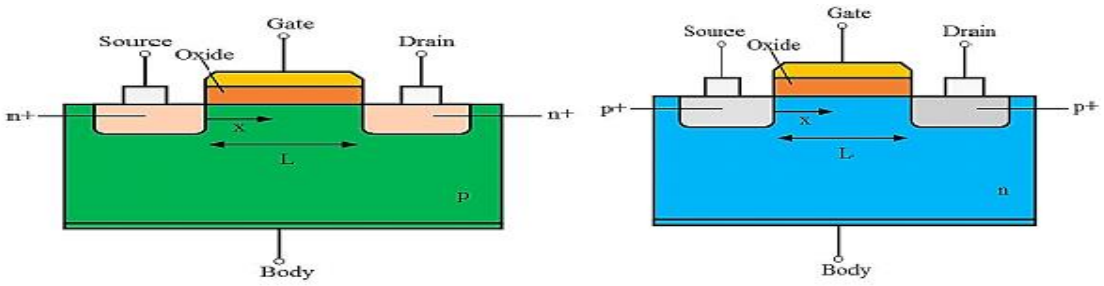


(a) (b)

Figure 1.3. (a) MOSFET structure (b) Cross-sectional view for MOSFET [7].

In electronic circuits, the MOSFET operates as a switch or an amplifier. Source (S), drain (D), gate (G) and substrate are four terminals comprising up a MOSFET, as depicted in figure 1.3. There are three layers in a MOSFET namely a layer of metal gate terminal, a layer of gate oxide and a layer of semiconductor (substrate).

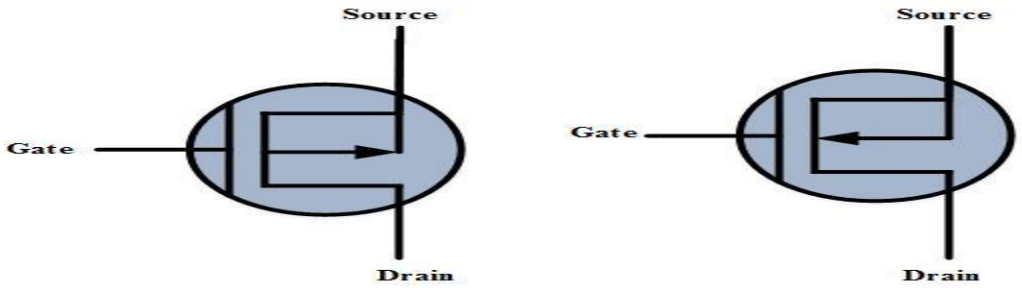
MOSFET working operation is simple and easy to understand. On applying voltage across terminals of drain and source, formation of a conducting channel between these terminals takes place that allows current to flow [7]. Charge carriers are attracted to surface of gate to oxide interface by gate to source voltage and creates a channel connecting source and drain terminals.



(a) (b)

Figure 1.4. (a) *n*-channel MOSFET (b) *p*-channel MOSFET [7].

A MOSFET is classified into two categories, *p*-channel and *n*-channel MOSFET, on the basis of dopants used in drain, source, and substrate terminals which is shown in figure. 1.4. The MOSFET is referred to as *n*-type when source and drain terminals of a *p*-type substrate are doped using donor ions, namely phosphorus or arsenic, which creates a negative channel and this channel conducts current between source and drain terminals. Whereas, p-type MOSFET is formed by doping acceptor ions (boron) in a *n*-type substrate which forms a positive channel in device.



(a) (b)

Figure 1.5. (a) *p*-type MOSFET (b) *n*-type MOSFET symbols [8].

Figure 1.5. displays symbols for *p*-type and *n*-type MOSFETs. With *n*-type MOSFET, arrow points from *p*-type substrate to *n*-type channel when there is a *n*-channel present. Arrow in case of *p*-type MOSFET points from *n*-type substrate to *p*-type channel.

1.2. SIGNIFICANCE OF SCALING

VLSI device design scaling as described by technology is process of reducing device dimensions while retaining electrical properties of device. A specific generation of the semiconductor manufacturing process is referred to as a "technology node" in semiconductor industry. It is defined by smallest feature size which can be created on a chip, which is

measured in nanometres (*nm*). The length of gate, which is used to measure MOSFET transistor size, is known as feature size or feature length. To achieve reduction in consumption of power and improvement in performance, transistors on a chip can be packed closer together as the technology node gets smaller [199]. A device produced at a technology node of 14 *nm*, for instance, will have transistors that are 14 *nm i*n size, whereas a chip produced at a node of 7 *nm* will have transistors that are 7*nm* in size.

With the advancement in VLSI industry, MOSFET devices have seen a reduction in feature size over the years. The feature size of a device was 50μm in 1960 and it has been reduced from 15 *nm* in 2017 to 7 *nm* in 2020. With the scaling of feature size there is increase in density of transistors on a single integrated chip [9].

Achieving a high transistor packing density in a single IC requires designing of VLSI chips with high density and excellent performance. So, there is a need for small sized transistors to meet considerations in area. Length of channel and device's width are reduced in size with scaling of device dimensions. A constant scaling factor '*s*' ($s > 1$) has been introduced. By dividing horizontal and vertical dimensions of transistor with large size and using scaling factor (*s*), scaled device is obtained.

International Technology Roadmap of Semiconductor (ITRS) was introduced to see evolution of technology and observe the growth of IC in VLSI industry. ITRS provides a description of feature size reduction as per the ground rules roadmap for logic device technologies and is shown in table 1.2. [10].

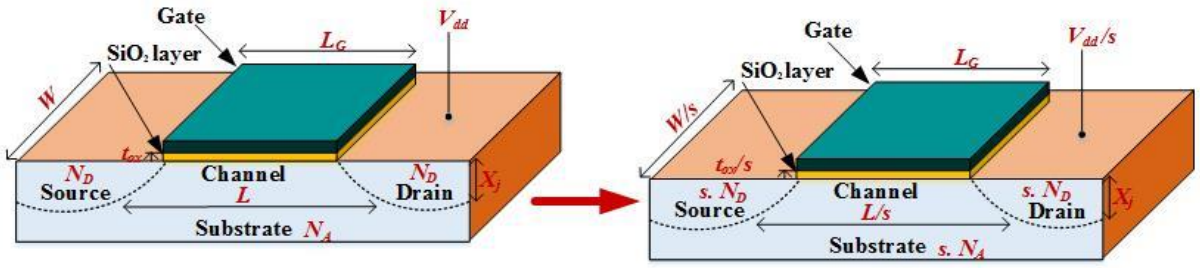
Table 1.2. Length of gate as described in roadmap for logic device technologies in ITRS [10].

Length of Gate	**Year**				
	2015	**2017**	**2019**	**2021**	**2024**
Low Performance Logic (*nm*)	24	20	16	12	12
Logic Industry "Node Range" Labeling (*nm*)	14	10	7	5	3
High Performance Logic (*nm*)	24	18	14	10	10

With the scaling of transistors, there is reduction in feature size of device to submicron and nano-regime. There is increase in switching speed and reduction in chip size & power dissipation with scaling of transistor.

Two types of scaling in which device dimensions can be scaled down are constant field scaling and constant voltage scaling [11]. Full scaling reduces the dimensions by scaling factor of *'s'*

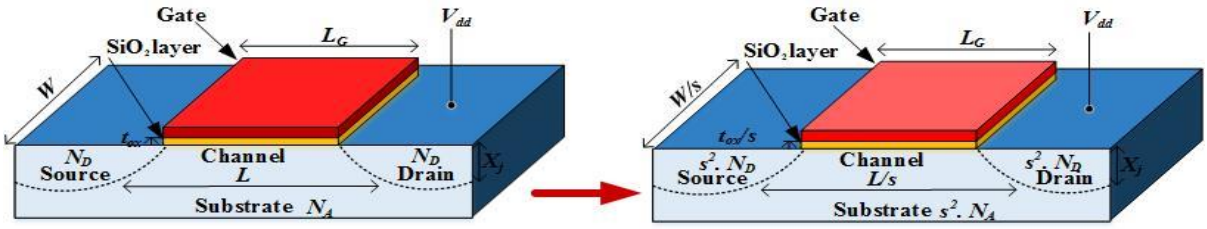
while attempting to retain MOSFET's internal electric field magnitude which is depicted in figure 1.6.



(a) (b)

Figure 1.6. (a) Original device structure for MOSFET (b) Scaled device structure for MOSFET (Constant Field Scaling) [11].

Device dimensions are decreased by a scaling factor 's' and doping concentration is raised by same scaling factor '*s*' (*s* >1). This is due to the fact as device dimensions are reduced there will be more carrier concentrations in the device. Further, current density gets reduced by scaling factor of '*s*'. All voltages at terminals and power supply voltage are scaled down in accordance with the dimensions of device, although this scaling of voltages is frequently impractical. Therefore, constant voltage scaling is much preferred over full scaling which is described in figure 1.7.



(a) (b)

Figure 1.7. (a) Original device structure for MOSFET (b) Scaled device structure for MOSFET (Constant Voltage Scaling) [11].

MOSFET's power supply and terminal voltage are unaffected, but all of its dimensions are decreased by scaling factor of '*s*'. Drain current density is raised by scaling factor of '*s*' and power density is increased by 's^3'.

Table 1.3. describes the parameters of device which are affected by constant field scaling and constant voltage scaling.

Table 1.3. Parameters of device before and after scaling of device [11].

Parameters	**Before Scaling**	**After Scaling**	
		Constant Voltage Scaling	**Constant Field Scaling**
Length of channel	L	L'=L/s	L'=L/s
Thickness of gate oxide	t_{ox}	t_{ox}'=t_{ox}/s	t_{ox}'=t_{ox}/s
Width of channel	W	W'=W/s	W'=W/s
Power supply voltage	V_{dd}	V_{dd}'=V_{dd}	V_{dd}'=V_{dd}/s
Depth of junction	X_j	X_j'=X_j/s	X_j'=X_j/s
Drain current	I_D	I_D'=s.I_D	I_D'=I_D/s
Threshold voltage	V_t	V_t'=V_t	V_t'=V_t/s
Power density	P_D/Area	P_D/Area'= s^3. P_D/Area	P_D/Area'= P_D/Area
Doping densities	N_A, N_D	N_A', N_D'=s^2.N_A,s^2. N_D	N_A',N_D'=s.N_A, s. N_D
Power dissipation	P_D	P_D'=s.P_D	P_D'=P_D/s^2

As shown in table 1.3. device dimensions are decreased by scaling factor of *'s'*. Drain current density is increased by '*s*' scaling factor and power density is increased by 's^3'. At nanometre regime, MOSFET has reached its technological and physical limits. Also, rate of failure and defects are higher at this device level [11]. At this feature size, charge distribution gets affected as the electric fields at drain and source sides are high. Driving current in channel region increases as the device's source-to-drain spacing or the MOSFET's channel length, decreases.

1.3. IMPACT OF SCALING

Device scaling causes SCEs when device's feature size is reduced to nanometres. When MOSFET's channel length reaches a point where it is roughly equal to space charge regions of drain and source junctions with substrate, a series of phenomena known as short channel effects start occurring. MOSFET scaling causes SCEs in device, namely drain-induced barrier lowering (DIBL), subthreshold leakage current, bulk punch-through, fluctuations in threshold voltage, impact- ionization, hot electrons, surface scattering and increased gate-oxide leakage [12].

1.3.1. Drain-induced barrier lowering (DIBL)

DIBL occurs as a result of positive voltage given to drain of short channel device and threshold voltage reduction is observed due to depletion region under drain region reducing the length of channel [12]. High voltage at drain to source terminal causes depletion layer to expand and extend under gate. As a result, the drain takes a greater portion of burden of

balancing the charge in depletion region, leaving gate with a smaller burden. It reduces channel length and threshold voltage resulting in DIBL decrease.

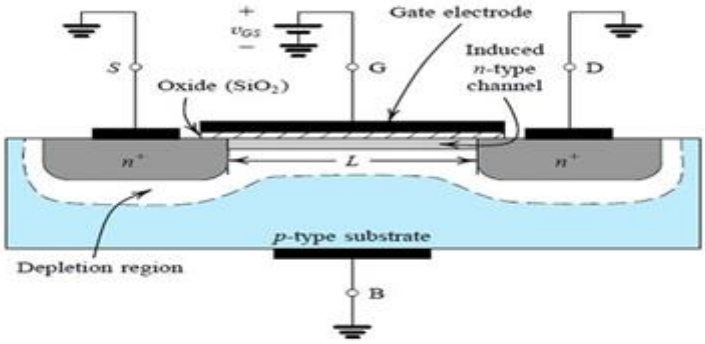


Figure. 1.8. Drain induced barrier lowering in MOSFET [12].

In a highly doped source, drain bias lowers barrier of energy between source and channel for electrons and as a result, electrons can flow into channel with ease from source side. Source-to-channel barrier lowering in long channel MOSFETs is only caused by voltage at gate; however, in MOSFETs with short channels, this is also induced by drain bias, hence termed as "drain-induced barrier lowering (DIBL)" which is described in figure 1.8.

1.3.2. Subthreshold leakage current

To preserve reliability and performance, threshold voltage should be decreased when geometry of MOSFET gets minimized. When a MOSFET is in subthreshold region (OFF state) when gate to source voltage is less than threshold voltage, some leakage current flows between source and drain as shown in figure 1.9. [13].

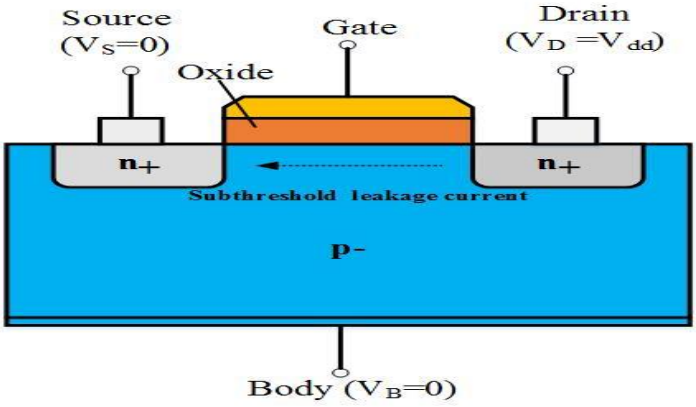


Figure. 1.9. Subthreshold leakage current in MOSFET [13].

Most unfavourable SCE is threshold voltage (V_{th}) decrease at which a device turns ON, particularly for large value of drain voltages. It is difficult to turn OFF device due to considerably increased subthreshold leakage current caused by decrease in threshold voltage.

1.3.3. Punch-through

When depletion region near drain touches source region, phenomenon named punch- through takes place. As a result, regardless of gate voltage, current flows at higher positive drain voltage which is described in figure 1.10.

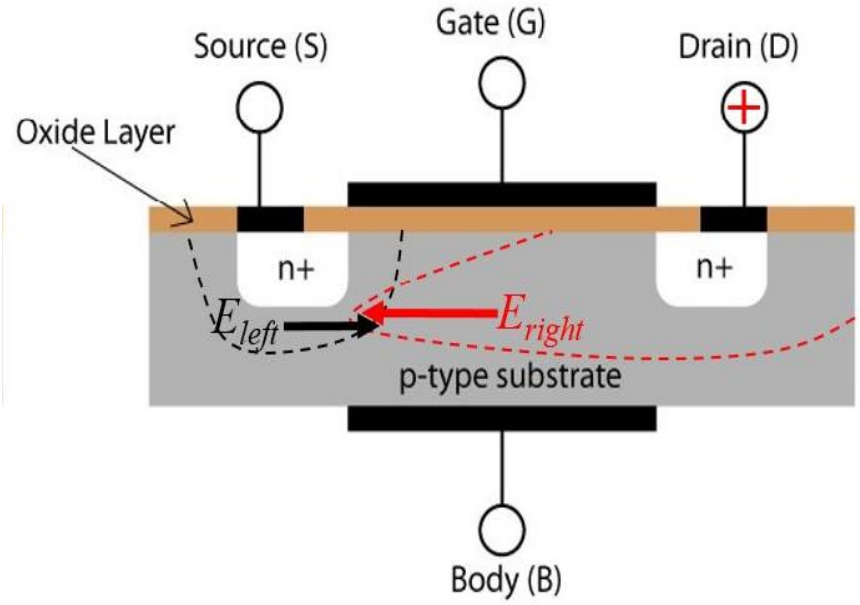


Figure. 1.10. Punch-through in *n*-type MOSFET [14].

1.3.4. Threshold voltage roll-off

Threshold voltage roll-off occurs in short channel devices. When gate length decreases, there is reduction in threshold voltage which results in threshold voltage fluctuations and this phenomenon is called threshold voltage roll-off. Electric fields from source and drain have an effect on distribution of charges in device's channel.

1.3.5. Impact-ionization

Impact ionization arises when an energetic electron collides with another electron and energy is lost, promoting the electron from valence band to conduction band that results in generation of additional electron hole pairs [14]. Generated electron-hole pairs/carriers increase the forward current in transistors which leads to heat generation and device failure.

1.3.6. Hot electrons

When electrons or holes get accelerated by a strong electric field in semiconductor devices, this gives rise to high kinetic energy. These electrons/holes get trapped into the Si-SiO_2 interface that degrades the device properties.

1.3.7. Surface scattering

Electric field's vertical component accelerates electrons in direction of surface that give rise to surface scattering and reduces carrier mobility and current in device which is shown in figure 1.11.

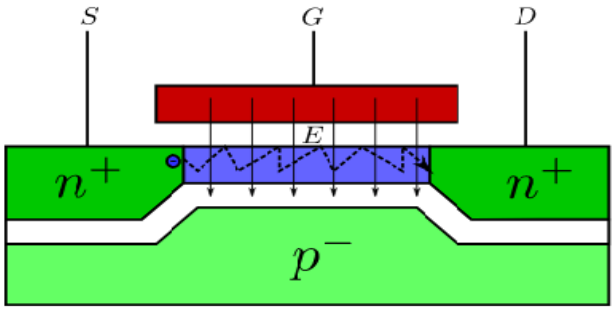
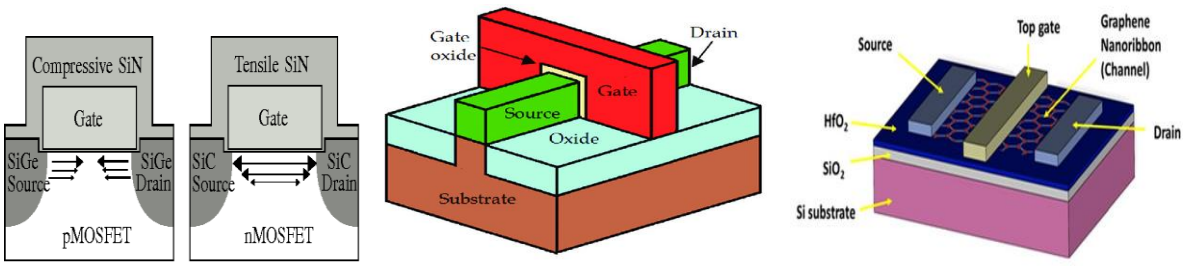


Figure. 1.11. Surface scattering in MOSFET [15].

1.4. POSSIBLE ALTERNATIVES TO SCALING

To overcome short channel effects (SCE) mentioned in the previous section, new device technologies, structures and device designs have been developed to control SCEs at very small dimensions. Some of the examples for reducing SCEs are using high –k material as gate oxide to increase electrostatic control over channel, multi-gate structures for higher drive current and using different channel materials for improving carrier mobility. New device designs include the usage of multi-gate MOSFETs, strained silicon technology and high dielectric materials, FinFETs, CNTFETs and GNRFETs [16,185,188,190,194,195] as described in figure 1.12.



(a) (b) (c)

Figure 1.12. Possible solutions to scaling (a) Strained silicon technology (b) FinFET (c) GNRFET [16,185,190].

High-k materials have dielectric constants (k) that are more valuable than conventional SiO_2 layers. High-k values also enable thicker gate insulator layers while keeping capacitance constant. These materials can therefore be employed to overcome short channel effects. High-k material based MOSFETs can be employed in Integrated Circuits (ICs), Digital Logic Gates, Analog and Mixed-Signal Circuits, Radio Frequency (RF) and Wireless Communication, Sensor and MEMS Devices and Power Electronics.

The process of strained silicon involves altering the crystal lattice structure of material to improve device performance. Using this method, silicon crystal lattice is modified and the material's electrical structure is changed to facilitate charge carriers' easy movement through the material and increase carrier mobility and control over transistor characteristics. Strained silicon technology offers a wide range of applications in semiconductor devices, particularly transistors, where improved carrier mobility and device performance are desired. Its versatility makes it suitable for use in various electronic systems across different industries, ranging from consumer electronics to high-performance computing and telecommunications.

FinFETs, double-gate MOSFETs, and nanowire FETs are examples of multi-gate structures that are made to reduce impact of SCEs in semiconductor devices. By lowering leakage current, these improve electrostatic control over channel. Multi-gate structures offer significant advantages in terms of performance, power efficiency and scalability, making them indispensable for a wide range of applications across different industries, including computing, communication, automotive, IoT, AI, and consumer electronics.

To increase device's overall performance, including faster processing speeds and reduced power consumption, DG-MOSFETs have been preferred over structures with single gate. Double-gate MOSFETs are more power efficient than single-gate MOSFETs because they reduce leakage current and are more effective for operation at lower supply voltages. Hence, it also provides an alternative for overcoming short channel effects.

Fins are etched into a silicon substrate and doped precisely during the complex semiconductor manufacturing processes used to fabricate FinFETs. Even though they are more difficult to manufacture, CNTFETs can sometimes be made using less complicated processes than FinFETs, depending on the specific CNT synthesis and integration methods used. Due to physical constraints of fin height and width, FinFETs also have scaling issues. Since CNTFETs are one-dimensional nanoscale devices, they may have a higher inherent scalability potential. FinFETs can be extensively used in microprocessors and other high-performance computing

components due to their ability to deliver high-speed operation and efficient power management. FinFET technology plays a pivotal role in powering the digital revolution across various industries, driving advancements in computing, communication, automation, and entertainment technologies.

Heat dissipation becomes a significant issue as MOSFETs are smaller and more densely packed on single chip. Because they utilize low power and produce less heat, CNTFETs have the potential to be efficient for high-performance devices. Modern electronic devices' increased power consumption is caused by MOSFET's subthreshold leakage current. Because of their unique electrical properties, CNTFETs have the ability to decrease this leakage.

Out of these device designs, CNTFETs act as a promising alternative to replace silicon MOSFETs because of its unique properties over the silicon. Limitations such as leakage current in scaled devices can be reduced by modifying material of channel by single CNT in traditional MOSFETs. CNT based FETs has outperform the silicon based MOSFETs in many ways [17].

1.5. PROPERTIES OF CARBON NANOTUBES

Due to its excellent properties, a promising candidate has emerged in form of carbon nanotubes for several applications. Some of its properties include high tensile strength, better electronic properties and high conductivity [17,189,191]. The light weight, greater flexibility, thermal conductivity and higher electrical properties of these material has the potential to make them effective thermal conductors and absorbent materials.

CNT's mechanical and electrical properties in comparison with silicon as channel material are represented in table 1.4 and 1.5.

Table 1.4. Comparison of CNT's mechanical properties with other materials [18].

Materials	**Thermal Conductivity (*W/mK*)**	**Young's Modulus (*TPa*)**	**Tensile Strength (*GPa*)**
Silicon	149	0.185	7
SWCNT	3,500-6,600	1-5	13-53
MWCNT	3000	0.27-0.95	11-150

From table 1.4, it is clear that young's modulus of SWCNT and MWCNT is more than the silicon so it's more flexible than the silicon. Additionally, they are capable of withstanding mechanical strain and stress without suffering serious distortion or harm. Strain engineering is frequently utilized in conventional silicon-based FETs to improve device performance. However, strain can result in unfavourable side effects as increased heat production and

leakage current. CNTs' extraordinary tensile strength, is greater than silicon, is well recognized from above table. They are particularly resistant to mechanical stress and bending which can be helpful in flexible electronic applications. CNT-based FETs are more efficient and reliable because they are capable of providing mechanical stability without the need for external strain engineering. Compared to silicon, CNTs offer higher thermal conductivity, which may be beneficial in dissipating heat produced during device operation more effectively. For CNT-based FETs, this property can result in fewer thermal issues and greater overall device performance.

Table 1.5. Comparison of semiconducting CNT's electrical properties with other materials [18].

Parameter	**GaAs**	**Semiconducting SWCNT**	**Ge**	**Silicon**
Electron Phonon Mean Free Path (*Å*)	58	˜700	105	76
Bandgap (*eV*)	1.424	0.9/diameter	0.66	1.12
Electron Mobility(cm^2/Vs)	8,500	20,000	3,900	1,500

Table 1.5. demonstrates that silicon has a lower electron mobility than semiconducting SWCNT. Silicon is a bulk semiconductor with a diamond crystal structure and due to lattice imperfections impurities, and phonon scattering, it inherently restricts the mobility of charge carriers (electrons or holes). CNTs, on the other hand, have a seamless hexagonal lattice and a one-dimensional crystal structure, which leads to fewer defects and less charge carrier scattering. Higher mobility results from the greater ease of movement of electrons across CNTs and can be used as FET device. The semiconducting property of CNT can be used in implementing FETs. CNTFETs will be main focus of this work.

1.6. CARBON NANOTUBES

Allotropes of an element is defined as the property by which chemical element exists in two or more different forms, in same physical state [19,200]. Four types of allotropes of carbon namely diamond, graphite, buckyball and carbon nanotubes. CNT has appeared as one of the favourable nanomaterials in semiconductor industry. A carbon nanotube was invented by a Japanese physicist, Sumio Lizima, in 1991. A hollow tube which is made up of carbon with a diameter of nanoscale is known as carbon nanotube [20,189]. It is also known as buckytubes.

Rolling up of two-dimensional graphite into a cylindrical shape structure forms a nanotube having a diameter of one to three nanometres. A two-dimensional graphene sheet is rolled up

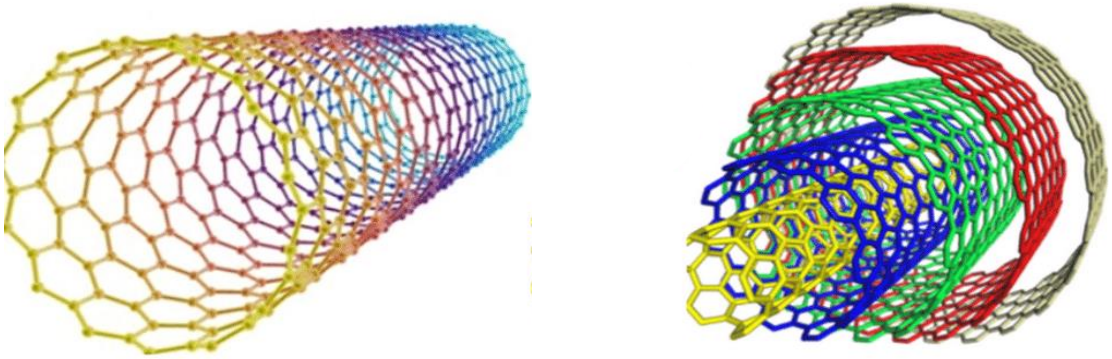
into a shape resembling a cylindrical tube to make a CNT. Classification of carbon nanotubes is as follows:

1.6.1. Classification of carbon nanotube

Carbon nanotubes have been categorized based on their structures, chirality and conductivity.

1.6.1.1.Classification based on their structures

Single walled carbon nanotubes (SWCNT) and multi walled carbon nanotubes (MWCNT) are two different kinds of CNTs based on their structure [21,196,197]. These have been classified in accordance with the range of carbon nanotube diameter of both structures.



(a) (b)

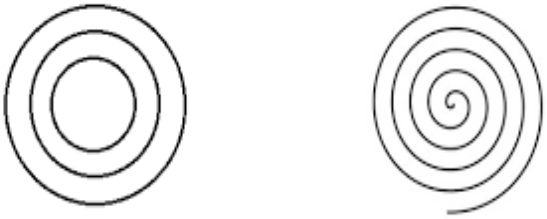
Figure. 1.13. (a) SWCNT (b) MWCNT structure [21].

a) Single-walled carbon nanotube (SWCNT)

As depicted in figure 1.13 (a), rolling up a graphene sheet results in formation of a hollow cylindrical tube-like structure to form a SWCNT [21, 193]. These nanotubes have diameter of around 0.4 to 4 nanometre and bandgap of 0 to 2 eV. The designs of SWCNT depend on the way in which graphene is wrapped into cylinders.

b) Multi-walled carbon nanotube (MWCNT)

MWCNT consists of several layers of rolled concentric tubes of graphene as described in figure 1.13 (b) [21]. MWCNTs have diameter of few *nm* to several tens of *nm*. It has several numbers of shells and each MWCNT shell has a different diameter and number of conducting channels.



(a) (b)

Figure 1.14. (a) Russian doll model (b) Parchment model [22].

Further, MWCNTs can be classified into two types namely Russian doll model and Parchment model as described in figure 1.14. (a) and (b).

- *Russian doll model*

Graphene sheets in Russian doll model are arranged in large-walled nanotubes as concentric cylinders. One carbon nanotube is present inside another carbon nanotube in the Russian doll model. Inner nanotube has a smaller diameter than outer nanotube.

- *Parchment model*

In parchment model, MWCNT is created by repeatedly rolling one sheet of graphene around itself, much like a scroll of paper.

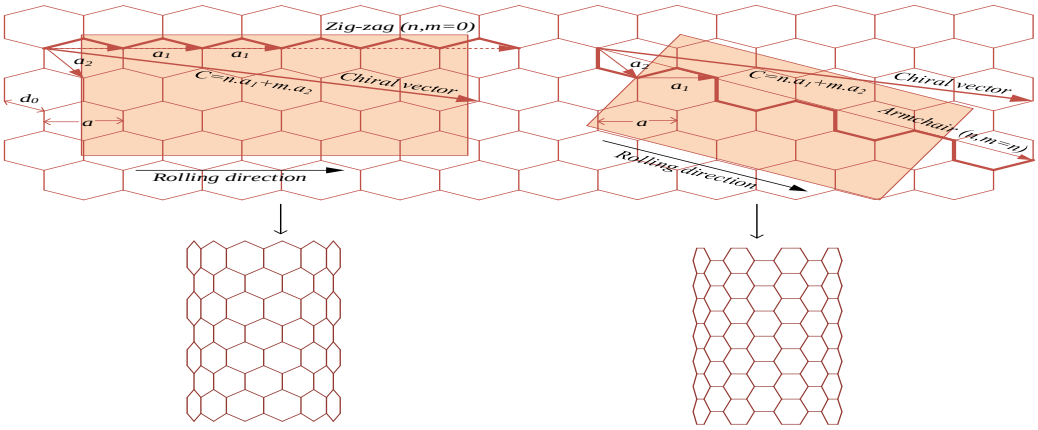
1.6.1.2. Classification of carbon nanotube based on chirality and conductivity

Orientation of graphene sheet while rolling, which is determined by chiral vector, determines the chirality of the CNTs. A carbon nanotube's chiral vector can be defined as [23]

$$\overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \tag{1.1}$$

where chiral vector is C_h , n and m are integers & basis vectors as a_1 and a_2. CNT can also be written as an expression of n and m.

Structure of CNT is specified using chiral vector (n, m). The different designs in which carbon nanotube are formed on the basis of chirality involves – zigzag and armchair structures. Based on the integer pair's (n, m) values and conducting nature of SWCNT, SWCNT has been described as Armchair (n, n) and Zig-zag (n, 0) CNTs as described in figure 1.15.



(a) (b)

Figure 1.15. Configurations of CNT (a) Zig-zag (semiconducting) (b) armchair (metallic) [24].

Carbon nanotube is said to be armchair if *m=n*, which occurs when both chiral indices are equal. If any of chiral indices, *n* or *m*, is zero, carbon nanotube is said to be zig-zag CNT as shown in figure 1.15. (a).

Conductivity of CNT depends on direction of CNT in which it is being rolled up. Armchair structures of CNT are metallic if *n-m=3i*, in which *i* represents the integer whereas zig-zag carbon nanotube structures are metallic or semiconducting depending upon integer values of chiral vector. In contrast to metallic CNTs, semiconductor CNTs have an energy bandgap. Semiconducting CNTs are excellent for logic devices due to their ability to switch between conducting and non-conducting states because of presence of a bandgap. Metallic CNTs, on the other hand, act like metals, having no bandgap and a constant density of states, which makes them less appropriate for use in digital applications. Semiconducting CNTs are preferred for most digital and analog applications, metallic CNTs may still find use in specialized applications where their high conductivity and unique electronic properties are advantageous, such as in interconnects or certain sensor applications.

Semiconducting CNTs are the preferred choice due to their bandgap and superior electrical characteristics. Further, high carrier mobility of semiconducting CNTs than metallic CNTs leads to faster transistor operation, which are beneficial for high-speed electronic devices.

1.7. CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNTFET)

Prior to 22 *nm* technology node, (MOSFET) enabled us to develop everyday advanced systems like smartphones and laptops. Due to an increase in SCE namely DIBL, impact ionization, channel length modulation & velocity saturation at 22 *nm* technology node, it is now impossible

to further scale down MOSFETs. Because of this, most foundries developed a new kind of transistor called a Fin Field Effect Transistor (FinFET), with fewer SCEs and better control of channels. This transistor structure is also employed at 16 *nm* and 14 *nm* nodes. However, it has been discovered that serious issues with FinFET in the 14 *nm* node exist, which could adversely degrade the IC's performance [25, 201]. In FinFET, rectangular fins have corners that produce corner effects and degrade the performance. Source and drain capacitance as well as capacitance between the two regions of a FinFET are forms of parasitic capacitance, which have an adverse effect on performance and reliability.

In nanoscaled domain, MOSFET has reached its technological and, more importantly, its fundamental physical limitations. Additionally, it is predicted that for MOSFETs, at circuit and device level, there is a significantly higher defect and failure rate. So, it has become essential for industry to introduce technologies which enable ongoing device implementation with increased performance. CNTFET acts as one of most promising emerging technologies that has potential to replace silicon-based electronics. The advantages of using CNTFET over MOSFET are low consumption of power, better control over channel formation, reduction of gate leakage current and high electron mobility. CNTFETs have higher electron mobility which allows faster switching and hence there is less power dissipation [187, 206] in CNTFET as compared to MOSFETs. CNTs are thermally stable than MOSFETs and there is reduced heat generation in case of CNTFETs. Further, leakage current is less in CNTFETs in comparison with MOSFETs. Switching in MOSFETs occurs by altering resistivity of channel, while in CNTFETs, contact resistance of device is modulated.

For future nanoelectronics, carbon nanotube (CNT) technology is a viable replacement for current silicon technology due to its unique electrical properties. S. Ijiima invented carbon nanotubes, a new modification of carbon, in 1991 [26]. As seen in figure 1.16, a CNTFET is a transistor that, compared to traditional MOSFET construction, uses a single CNT as channel material.

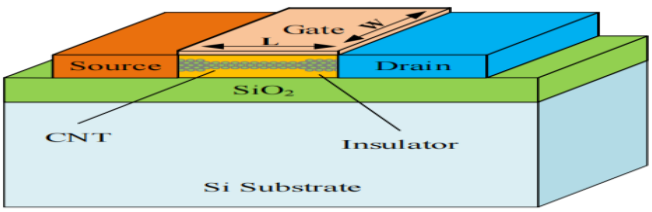


Figure 1.16. CNTFET structure [27].

CNTFET was first reported in year 1998. When compared to silicon, which is used as channel material in conventional MOSFETs, one CNT or a group of CNTs are used to form channel in CNTFET. CNTFET contains semiconducting nanotube as channel material. Both CNTFETs i.e., *n*-type and *p*-type are made using carbon nanotubes.

The various applications of CNTFETs include solar cells, used mainly in VLSI, faster computer chips and cancer treatment. Solar panel control circuits can employ CNTFETs for signal processing [204, 205]. They are used to process and amplify the electrical signals produced by photovoltaic cells inside solar cells. Thermal conductivity is quite good in CNTs. The heat in densely packed chips can be better controlled by this property [28, 202].

1.8. IMPORTANCE OF DOUBLE-GATE STRUCTURE OF CNTFET

With the scaling of VLSI device in nano-regime, various short channel effects have come into existence. These operational features consist in challenging scenarios for protective devices which must be considered in actual systems [186].

Different possible solutions to SCEs include multi gate devices, CNTFET and GNRFET [192]. This thesis presents multi gate structure of device namely double gate CNTFET to overcome short channel effects.

As the name suggests, DG-CNTFET consists of two type of gates namely top and bottom gate which is described in figure 1.17.

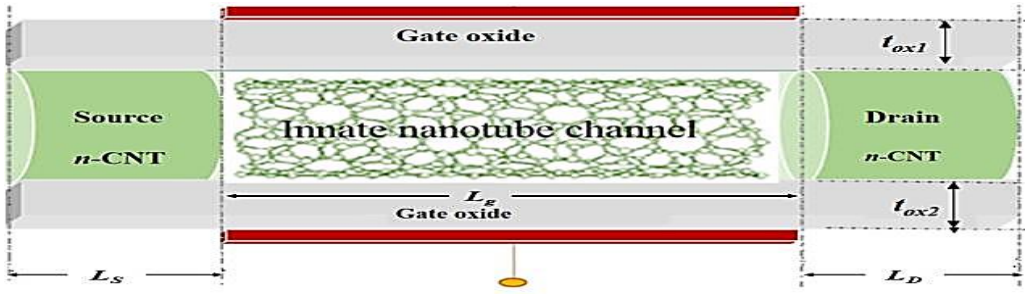


Figure 1.17. Double gate carbon nanotube field effect transistor structure [29].

Two gates provide better isolation of drain and gate &source and gate. It comprises of two single-gated CNTFET after each other, sharing a common terminal. The input applied at gate terminals controls output as well as functionality of carbon nanotubes [29]. Two gates allow for current flow in two channels that simultaneously control charge within the thin silicon layer of substrate. As gate controls conduction in the device, with two gates channel will be better controlled for the current flow.

Gate oxide layer between gate and channel is dielectric layer and metal used for gate is conductor and channel is also conductor, together, these three layers form a capacitor that decreases the device's overall gate capacitance.

There are numerous advantages of using double gate over single gate CNTFETs. Double gate enables higher drive current at lower threshold voltage and supply voltage. Leakage current at gate and channel of devices gets reduced which further reduces power consumption of device. Also, using two gates allow separate control of gate on voltage which also saves the chip area. DG-CNTFETs have been used in place of single gate because it removes short channel effects. This device is well suited for reducing SCEs namely threshold voltage variations, leakage current and DIBL [30].

1.9. MOTIVATION

With the advancement in VLSI industry, silicon transistors are further difficult to shrink after a particular feature size. The ability to advance MOSFET technology will start to decline, necessitating a rush to find a replacement. The feature size of the devices is reducing and their reduced size leads to the degradation of performance of device as it give rise to various SCEs namely threshold voltage variations, leakage current and DIBL. Due to a variety of SCEs, current study needs to investigate the possibility of replacing conventional MOSFETs. Various possible solutions to overcome short channel effects are high-k dielectric materials, strained silicon technology, multi-gate structures.

The researchers introduced carbon based nanostructures (carbon nanotubes and graphene nanoribbon) as new device materials for VLSI-ICs design at nano-scale. According to the literature, in nanoscale, these nanostructures act as an attractive alternative to MOSFETs. CNTFETs reduces the leakage current as there is rise in value of threshold voltage of device in comparison with MOSFETs. CNTFET have high electron mobility, high current density and low power consumption and enhances device performance by reducing the short channel effects [31-34,184].

Further, by using two gate geometry, the channel will be better controlled by the two gates for the current flow. DG-CNTFET has appeared as a promising candidate in various applications namely aeronautic engineering and automobile industry [35-37, 203]. Two gates are used to have better isolation between drain and gate &source and gate.

Developing the structure for performance analysis, modeling of CNTFET is crucial in the VLSI industry. Literature shows that although much work has been done on CNTFET modeling, a little work is reported related to temperature and the temperature impact on its ability to perform in thermal-aware environmental conditions has not yet been investigated. This thesis aims to model the DG-CNTFET's threshold voltage and drain current and evaluate its performance considering a variety of performance parameters. Also, while evaluating DG-CNTFET's performance, the impact of temperature has been taken into account. Further, this thesis involves SRAM cell performance using CNTFET at various technology nodes (10 *nm*, 22 *nm*, 32 *nm* and 45 *nm*).

1.10. THESIS CONTRIBUTIONS

This thesis presents the optimization of structure and performance analysis of DG-CNTFET. Device performance has been evaluated at thermal-aware environmental conditions so as to analyze the temperature effect on various performance parameters. Thesis contributions are as follows:

- The aim of first objective is to develop the optimized structure of double-gate carbon nanotube field effect transistor.

In this objective, different kinds of structure of DG-CNTFET have been taken into consideration to evaluate performance of all structures of DG-CNTFET. Further, the performance of device structures has been analysed at variable doping and considering process parameter variations to optimize structure of proposed DG-CNTFET. The proposed structure is conventional type DG-CNTFET due to its advantages over the other structures of DG-CNTFET and compared with existing structure of double-gate MOSFET. To evaluate performance of optimized DG-CNTFET structure and existing DG-MOSFET structure, current voltage characteristics of both structures have been obtained.

- The aim of second objective is to model the threshold voltage and drain current of double gate carbon nanotube field effect transistors (CNTFET).

Using optimized conventional DG-CNTFET structure, drain current and threshold voltage modeling has been carried out. Ballistic transport approach has been used for modeling current-voltage characteristics of single wall CNTFET. DG-CNTFET’s input and output characteristics have been obtained at room temperature. Analytical results achieved by writing codes using MATLAB have been compared with simulated results obtained in nano- TCAD ViDEs to

check accuracy of results. Further, CNT chirality and diameter effect on DG-CNTFET's threshold voltage presented as diameter is necessary parameter for calculating device's drain current and threshold voltage.

- The aim of third objective is to examine the impact of thermal aware environmental conditions on double-gate carbon nanotube field effect transistors.

In this objective, temperature effect on DG-CNTFET's drain current and threshold voltage has been evaluated to examine impact of variable temperature on device performance. Several performance parameters, including drain conductance, subthreshold swing, ON current and OFF current have been examined which are responsible for leakage current of the device. Further, temperature impact on DG-CNTFET's threshold voltage and performance of various channel parameters have also been studied. The results revealed that DG-CNTFET is thermally stable at variable temperature range.

- The aim of fourth objective is to analyze the performance of CNTFET SRAM cell using carbon nanotube field effect transistor.

SRAM cell performance based on CNTFET is evaluated considering read and write power dissipation, propagation delay and propagation delay product. Results obtained for CNTFET SRAM cell are compared with CMOS SRAM cell for evaluating the performance of device.

1.11. THESIS ORGANIZATION

Chapter 1 gives the brief introduction regarding scaling of devices and its impact, SCEs of VLSI devices and disadvantages of MOSFET. A brief description of carbon nanotubes and its properties are presented in this chapter. This chapter also includes classification of CNTs and basic concepts of CNTFET. Further, importance of double gate structure of DG-CNTFET is explained in this particular part of thesis. Finally, organization of thesis is described.

Chapter 2 provides an overview of literature containing a detailed content regarding the problems which have been studied in this thesis. Further, review related to the significance of present work is also described in this chapter. Literature including the beginning of transistor, its structures and SCEs which affects performance of VLSI device in nano-scale regime is also presented. The shortcoming of SCEs in MOSFETs and the necessity of carbon nanotubes to overcome shortcomings of MOSFET are also described. A review related to properties of carbon nanotube is highlighted for the study. Results shown in literature describes that there is

enhancement in the performance of the device as SCEs gets reduced in CNTFETs. Also, literature defines modeling of CNTFET under thermal environmental conditions. Review related to SRAM cell using CNTFET and CMOS technologies has been done for studying its performance. It's clear from the results presented in literature that CNTFET based SRAM cell can be utilized in applications where less power and higher speed devices are used. To study the comparison between CMOS SRAM cell and CNTFET SRAM Cell, literature review has been done. Research problems and gaps have been thoroughly identified in this chapter. On the basis of these research gaps, objectives of thesis have been formulated. To overcome these identified gaps, new methodologies/techniques have been proposed in the next chapters.

Chapter 3 presents the basic concepts and optimized structure of DG-CNTFET. This chapter includes study the basics of CNTs and their physical properties. Further, this chapter involves chirality concept that is used for studying physical and electronic properties of device. Also, detailed information regarding the design and optimization of structure of DG-CNTFET and its types have been presented in this chapter.

Chapter 4 defines temperature impact on various performance parameters of DG-CNTFET. An analytical model for DG-CNTFET that is temperature dependent has been proposed to analyse performance at variable temperature range. This developed model presented in chapter 3 is used to acquire current-voltage characteristics of DG-CNTFET. In order to investigate how temperature affects device performance, additional performance parameters, including drain conductance, subthreshold swing, ON and OFF current and output characteristics for a variety of temperatures have been evaluated.

In Chapter 5, threshold voltage performance analysis and effects of channel parameters on DG-CNTFET's threshold voltage at various temperatures. Temperature impact has been considered while assessing a device's performance in thermal environments.

Chapter 6 presents the application part of CNTFET. There are various applications of CNTFET which are used in VLSI industry. Out of these applications, SRAM cell is most popularly used in devices with less power and high speed. The brief introduction and scaling issues related to SRAM cell have been presented in this chapter. Further, the basic cell operations and design parameters have also been described. This proposed SRAM cell using CNTFET has been designed to evaluate performance of device. A comparative analysis of SRAM cell using CNTFET and CMOS technologies has been done to investigate performance of these SRAM devices considering power dissipation, propagation delay investigation and

power delay product (PDP) at several technology nodes such as 10 *nm*, 22 *nm*, 32 *nm* and 45 *nm*. Results reveal that CNTFET 6T SRAM cell outperforms CMOS based SRAM cell due to its low power dissipation and propagation delay which can further be utilized in applications requiring both fast speed and low power. Finally, **Chapter 7** describes conclusion of the thesis and future scope of research work in this area.

CHAPTER 2

LITERATURE REVIEW

This chapter involves a thorough analysis of existing literatures to give background knowledge on topics under consideration for the thesis and to emphasise the importance of ongoing research. This chapter presents the review related to the limitations and challenges occurred by scaling of silicon-based devices. Further, it also describes the review related to short channel effects which occur as a result of device scaling, methods to overcome the limitations and need of CNT as VLSI devices. Further, a temperature dependent modeling of CNTFET and its applications in the VLSI industry has been discussed in this chapter. Although there haven't been many studies related to temperature dependence on DG-CNTFET cited in the literature, there is still a lot of scope for investigation of temperature for design and optimization of high performance CNTFET based devices. This chapter gives the brief outline of CNTFET technology-based devices.

2.1. INTRODUCTION

The performance of various devices used in VLSI industry gets affected by silicon device scaling. Due to transistor scaling, feature size of device has reduced from micrometres to nanometres at nanoscale regime. At nanoscale, MOSFET has reached its technological and physical limits. Also, rate of failure and defects are higher at this device level. At this feature size, charge distribution gets affected as electric fields on source and drain sides are high. The driving current in the channel region increases when MOSFET’s channel length and source to drain spacing decreases which causes SCEs such as DIBL, subthreshold leakage current, bulk punch-through, fluctuations in threshold voltage, impact –ionization, hot electrons and surface scattering in device. To overcome these short channel effects (SCE), different techniques have been applied to develop new structures, technologies and device designs that can control SCEs at extremely small dimensions. Oxide thickness scaling using high-k/metal gate material to improve electrostatic control over the channel, multi-gate structures for higher drive current and using different channel materials to improve carrier mobility are some of the ways to reduce SCEs that have been discussed in the literature. Further, the review related to new device designs which include the usage of multi-gate structures of MOSFETs, strained silicon technology, high-k dielectric materials, FinFETs, CNTFETs and GNRFETs has been covered. Out of these device designs, CNTFETs act as a promising replacement for silicon MOSFETs because of its unique properties. Limitations such as leakage current in scaled devices can be

reduced by replacing channel material with single CNT in traditional MOSFETs. The literature shows that FETs based on CNTs have outperform silicon based MOSFETs in several ways. Different works have been presented in literature to understand the performance of CNTFET which makes it more convenient to use in VLSI industry in nano-regime. To analyze the performance of device, different temperatures are to be included in nano-regime to study accurate device behaviour. The modeling of DG-CNTFET's drain current (I_{ds}) and threshold voltage (V_{th}) and its performance parameters have been discussed in literature. Further, the review related to application of CNTFET i.e., SRAM, has been discussed in this chapter. The majority of the work discussed in the literature focuses on the CNTFET and how temperature affects different performance parameters.

2.2. CHALLENGES RELATED TO SCALING

The semiconductor industry depends greatly on transistor scaling. Reducing the feature size of device has an impact on its performance. Review related to the scaling of device has been studied and presented in the literature.

M.T. Bohr et al. [38], presented that the scaling of transistors and considering Moore's law has led to development of cheaper, denser ICs and consumes lower power. The CMOS scaling trends, various new device options and technology have also been discussed. The scaling of MOSFETs led to leakage current when the gate oxide thickness gets scaled and gave rise to electron tunneling. Various techniques namely high-k metal gate and strained silicon transistors are introduced to enhance performance of device and decrease leakage current. The next innovation is use of FinFET transistor which uses the 3D structure. The improvement of electrostatic control by the steeper subthreshold slope, lower off state and lower threshold voltage has also been presented in this paper.

M. Bohr [39], studied that beyond 65 *nm* generation, scaling transistors will undoubtedly provide additional challenges. Further, it is widely acknowledged that the straightforward scaling rules are no longer an adequate approach for addressing the performance, power and transistor density requirements in future. To continue scaling, there have been advancements in strained silicon, multiple-gate devices, metal gates, and high-k dielectrics.

M. Leog et al. [40], in this paper, shows that reducing the size of transistor allows for the integration of more devices into an area as well as reducing source and drain distance. In addition, electric carriers of channel are no longer under the control of gate terminal, as source and drain distance is reduced. Furthermore, they suggested that using metal electrodes and

high-k dielectric will improve gate control and decrease tunnelling gate leakage current. As it decreases SCE and removes the leakage route, transistor structures like ultra-thin Silicon-on Insulator are a different choice for device scaling. Also, they investigated utilizing more complicated 'double-gate' FETs improve electrostatic gate control and furthermore reduces leakage. In this paper, strain and orientation effects as well as other mobility-enhancing approaches are explored.

Paul. A. Packan et al. [41], studied that the charge concentrations in source, drain and channel need to increase for MOS transistor to scale. They adopted the use of channel profile engineering that isolates source and drain regions. To improve performance, halo-channel profile engineering was also applied.

K.J. Kuhn [42], discussed the considerations for CMOS scaling. In this paper, various transistor architectures including thin silicon-on-insulator, FinFET and nanowire architectures have been compared and discussed. This work has examined some of the technology issues including those related to improved gate stacks, mobility, resistance and capacitance. It was discussed in this paper that device parasitic resistance decreases drive current and increases delay which has an impact on circuit's performance. Further, due to scattering from various surfaces, metals and semiconductors resistivity rises with reducing size. Also, it was studied that parasitic capacitances affects the circuit performance by increasing capacitive load and increasing delay. In this paper, it was further discussed that for improving electrostatic implementing architecture which reduce S/D interaction and decrease the effective electrical gate dielectric thickness, is necessary. Improving the short channel properties requires reducing the interaction between the source and drain.

2.3. LIMITATIONS OF MOSFET AS A DEVICE AND ITS SOLUTION

The need for smaller, faster and less expensive devices led to the development of basic concept behind FETs in 1930 to replace the vacuum tubes of large size.

P. M. Zeitzoff et al. [43], studied that due to deep submicron dimensions of MOSFETs and some important device and material limits that are being approached, IC industry is encountering growing difficulties in maintaining the traditional pace of scaling. It is predicted that strained silicon channels will be used to create MOSFETs with improved mobility. It is predicted that strained silicon channels will be used to create MOSFETs with improved mobility. Further, scaling causes polysilicon depletion in the gate electrode and metal-gate electrodes are the most suitable solution.

R.K. Ratnesh et al. [44], described that to improve the efficiency of transistors and their large integration, most of the researchers are working on scalability of transistors. Further, there is a need of nanoscaled transistors that use low-cost and low-power designs. The MOSFET scaling in nanometre scale induces different tunneling and short channel effects causing degradation and various challenges in fabrication process. Various techniques are developed to resolve the SCEs using nanowire and nano-FET. This paper further deals with the most recent developments in MOSFET technology. Scaling of MOS technology has been described yearwise in this paper and is shown in table 2.1.

Table 2.1. MOS technology scaling yearwise [44].

Sr. No.	**Production Year**	**MOSFET Technology (Length of gate)**
1	1971	10μm, 10000 *nm* (2-D technology)
2	1974	6 μm, 6000 *nm*
3	1977	3 μm, 3000 *nm*
4	1981	1.5 μm, 1500 *nm*
5	1987	800 *nm*
6	1990	600 *nm*
7	1993	350 *nm*
8	1996	250 *nm*
9	1999	180 *nm*
10	2001	130 *nm*
11	2003	90 *nm*
12	2005	65 *nm*
13	2007	45 *nm*
14	2009	32 *nm*
15	2012	22 *nm* (3-D Technology)
16	2014	14 *nm*
17	2016	10 *nm*
18	2018	7 *nm*
19	˜ 2020	5 *nm*
Future trends		
20	˜ 2021	3 *nm*
21	˜ 2024	2 *nm*

It was also described that scaling of transistors must follow Moore's law which is defined as the number of transistors in a dense IC must double every two years. Scaling down technologies allowed for the manufacturing of more transistors from one individual silicon wafer. This

reduces cost, increases the compactness of circuit and also improves speed and performance. Making a device with a lot of transistors is a difficult task. Because of the transistor's reduced dimensions, short channel effects arise. To diminish SCEs, various techniques have been presented in this paper. Different types of multi-gate structures including DG-MOSFET, FinFET, gate-all-around FET (GAAFET) and surrounding-gate MOSFET are discussed. These devices reduce leakage current that enhances device's performance. Scaling limits and mechanisms have been discussed in this chapter. Furthermore, a variety of nanoFETs have been presented.

Z.X. Yan et al. [45], studied that when there is increase in substrate bias, DIBL first raises threshold voltage shift; when channel length is further decreased then threshold voltage reduces further. It was also presented that transition from surface to subsurface level, DIBL effect and appearance of punch through effect can be used to explain changes in DIBL with substrate bias for devices with changing length. Further, in this paper, various temperature characteristics and characteristics associated with channel doping with respect to DIBL were simulated and implemented. There was an improvement in DIBL.

M.J. Deen et al. [46], in this research, studied the tunnelling of carriers across a forbidden energy barrier to produce gate current in MOS devices. Particular characteristics of tunnelling that occur in modern MOS transistors include phenomena like direct tunnelling, depletion of polysilicon, hole tunnelling, valence band tunnelling and gate current partitioning, are examined together with the physical principles of tunnelling in a MOS device. Several compact MOS models' gate current modelling approaches are described and contrasted. It is also explained that when designing circuits with MOSFETs that have ultra-thin oxides, certain factors and additional effects must be taken into account.

T. Tsuchiya et al. [47], presented that hot carriers are the serious problem in short channel devices which is responsible for the device degradation. As electrons with high energy flow through oxide layer, they become stuck and accumulated oxide charge increases. This alters device's threshold voltage which controls how gate controls drain current. By determining where impact of the hot carriers is most significant on channel SiO_2, it was possible to investigate the relation between *p* and *n*-channel MOSFET degradation and hot electrons/holes. In p-MOSFETs, hot-electron trapped in saturation region is a major contributor to negative-charge generation and hole injection in linear region contributes to transconductance degradation. It is also described in this paper that hot electrons injection into region of SiO_2

above channel and close to the drain in *n* MOSFETs is what causes interface-state generation that results in degradation of transconductance in saturation region. Hot holes do not affect transconductance, degradation in *n* MOSFETs since they are injected into SiO_2 located above drain depletion layer in drain region.

A. Chaudhry et al. [48], discussed the various methods and techniques for controlling SCEs. To satisfy increasing need for fast speed and high performing ULSI applications, work explores unfavourable SCE that cause a MOS device based on silicon-on-insulator (SOI) that degrade performance of device. A brief analysis of each attempt's strengths and weaknesses is provided. According to scaling law, MOSFET dimensions have continued to decrease to enable higher-speed and denser packed MOS integrated circuits. Due to their extremely large integration, current VLSI's have a rather significant increase in power consumption. This strength should definitely be decreased. It works well to select a lower power supply voltage. However, it causes the MOSFET current driving capacity to degrade. As a result, scaling MOS dimensions is crucial for enhancing drivability and producing VLSI ICs that are more efficient and useful. Further, the main performance issues with SCE include lack of pinchoff, threshold voltage change with decreased channel length, DIBL and the hot-carrier effect at rising drain voltage. Additionally, SCE reduces gate voltage's capacity to be controlled in relation to drain current which degrades subthreshold slope and there is rise in drain OFF-current. (DMG) has been emphasised in thin-film SOI MOSFETs for SCE suppression. This article reviews recent proposals for SOI MOSFET SCE reduction. It is also described how suppressing SCEs like hot-carrier effects, DIBL and CLM affects reliability of scaled MOSFETs and are evaluated for a novel device structure known as dual-material gate SOI MOSFET. In order to avoid unwanted SCE in SOI devices, a number of new device structures are presented in literature. Physical mechanisms determining SCE are discussed in this work and evaluated to overcome SCE. Effectiveness of a new device structure known as dual-material gate (DMG) in reducing SCE in thin-film SOI MOSFETs is focussed through the use of analytical model that accounts for effect of various device parameters.

T. Sekigawa et al. [49], first reported double-gate concept and has been fabricated by various researchers. They discussed that a MOS transistor's threshold voltage begins to reduce quickly as its channel length decreases below a particular value. It was also presented that threshold voltage gets affected with the fluctuations caused by the fabrication processes which limits the use of short channel devices. These issues can be resolved when a bottom gate is added to MOS transistor structure because it protects channel area from electrical interference caused by

wirings or other active components below. It is also mentioned that this device can be used with a modified scaling rule. When all dimensions and doping level of channel are scaled, a scaled device achieves almost same threshold voltage.

K. Suzuki et al. [50], discussed that device performance is degraded by high doping concentration because of increased junction capacitance and lower mobility. It is suggested to get over the bulk MOSFET's scaling restrictions by using a DG-SOI MOSFET, in which potential control is provided by both gates. Research has been done on this device's characteristics, which include its high transconductance, SCE immunity, and ideal subthreshold factor. In this study, they developed a scaling theory and demonstrated how it can be used to design devices with appropriate S-factors. For double-gate SOI MOSFETs, they calculated a length that was applicable to scaling theory and outlined the process for creating t_{si} with an appropriate S-factor for a particular length of gate. Theoretically, despite L_G being $< 0.1\ pm$, almost ideal S-factor value can be expected. The thinnest t_{si} that can be manufactured is the biggest factor of shortest gate length device that can be designed.

2.4. INTRODUCTION TO CARBON NANOTUBES

Since the invention of CNT by Iijima in 1991, nanotubes have drawn attention because of their great potential for use as metallic nanowires and active semiconductor devices in coming integrated circuits (ICs). Understanding the basic electrical characteristics and developing numerous uses for carbon nanotubes have advanced tremendously (CNTs).

P. L. McEuen et al. [51], reviewed that SWCNTs have evolved into a highly promising material option for electronics. They have examined the manufacturing and electrical characteristics of devices based on single-wheat nanotubes. It is discovered that the electrical characteristics of metallic and semiconducting SWNTs are comparable to the best electronic materials available in market. This paper described the various techniques for nanotube growth and device fabrication. The chemical vapour deposition (CVD) has been mentioned in this paper which is used to fabricate SWNT. Various electrical properties of semiconducting tubes have been also been discussed. Semiconductor tubes have mobilities and transconductances comparable to or exceed best semiconductors and metallic tubes have current densities and conductivities that are on equal level or better than the best metals.

M.S. Fuhrer et al. [52], fabricated transistors made of semiconducting carbon nanotubes that have channels longer than 300 microns. It is stated that channel resistance gets dominated over diffusive carrier transport in long transistors. Field-effect mobility and intrinsic mobility at

room temperature are calculated using the transport characteristics. These values are calculated for semiconductors and can be used in high-speed transistors and biochemical sensors.

R. Srivastava et al. [53], presents the review articles that deal with detailed introduction, categorization, manufacturing processes, and optical uses for carbon nanotubes. MWNTs and SWNTs have been manufactured using a variety of techniques. Several properties and application as light emitting diodes have been presented. Chemical vapour deposition, laser vaporization and electric arc discharge are well-established methods for producing a variety of CNTs. This paper describes these methods. In addition, CNTs' optical properties, which are strongly related to their physical and electrical properties are also explored. The chiral vector of a CNT defines how carbon-atom honeycomb is organised considering CNT axis. CNTs may act as metal or a direct band-gap semiconductor entirely based on this characteristic. CNT's electrical characteristics are determined by its chiral vector. This vector depicts rolling of graphene sheet to create nanotube. It is also discussed that CNT film diode is probably the most promising form of device from the perspective of applications. The averaging effects that result from using many tubes produce performance that is consistent, strong and constant. The advantages of single-tube and film diodes enable efficient near-infrared light sources at nanoscale which are valuable in a variety of technological applications. This contributed significantly to the development of science and technology of fascinating material.

H. Daraee et al. [54], discussed carbon nanotube applications in drug delivery fields and medical areas. Also, production of carbon nanotubes, their functionality and doping have been discussed. They stated that SWCNT and MWCNTs can be distinguished based on number of layers in graphene sheet. Various methods for synthesis of carbon nanotube have been discussed which include carbon-arc discharge, laser ablation methods and CVD. Number of methods related to purification and drug delivery by carbon nanotube have been discussed.

R. Marani et al. [55], reviewed the literature on carbon nanotubes. They discussed types of CNTs, diameter of CNT and energy bandgap. Also, the basic of CNTFETs and various types of CNTFETs have been discussed. I-V characteristics and subthreshold band diagrams of schottky barrier CNTFETs have been discussed. Partial gated CNTFETs are those devices which consist of uniformly intrinsic doping that may be of *n* or *p*-type. The MOS-like CNTFETs consist of source and drain that are heavily doped. These devices give best results considering 'ON/OFF' current ratio and subthreshold swing. They described modeling of CNTFETs which include I-V model and subthreshold characteristics. In I-V model it has been

studied that when voltage at drain to source terminal is greater than zero, there is a flow of current at the beginning of channel along the carbon nanotube. Applying positive voltage at gate to source terminal, conduction band of channel decreased by qV_{CNT}. They also concluded that tunneling current of holes and electrons constitute total current through the carbon nanotube.

C. S. Lee et al. [56], proposed a model which described current-voltage characteristics of carbon nanotube which include carrier velocity having gate length below 15*nm*. Also, carrier mobility and velocity have been calculated which depends on carbon nanotube diameter. Various SCEs parameters like subthreshold slope, threshold voltage variations and DIBL have been described by authors. ON current for each carbon nanotube has been described. It has been estimated that ON current i.e. $I_{ON}=I_d$, for 2-*nm* diameter carbon nanotube is 27% higher than that of carbon nanotube with 1 *nm* diameter. The intrinsic delay which can be expressed as $t_{in} = (L_g C_{inv} V_{dd}) / I_{ON}$ has 21% lower value of t_{in} in case of 1-*nm* diameter carbon nanotube. Using Verilog-A, model of CNTFET has been implemented and output current has been analyzed with no numerical iterations.

2.5. CNTFET AND IMPACT OF THERMAL VARIATIONS

CNTFET is device having three terminals that contains a semiconducting nanotube between the two contacts (source and drain) and acts as a carrier channel that is controlled and turned ON or OFF electrostatically by third terminal (gate). A number of groups are working to create these devices in different variations, with growing success in enhancing performance. As CNTFETs have made significant progress from their initial conception in 1998 in terms of manufacturing simplicity, there is still much work to be done before large-scale integration and commercial use which are cost effective.

P. Arul et al. [57], have shown that excessive scaling affects MOSFET devices in nanometre regime (10 *nm*) due to SCEs. SCEs include subthreshold swing (SS), DIBL and threshold voltage roll-off (V_{th}) have a significant impact on CMOS devices performance. CNTFETs may be designed to provide good control over leakage current and consumption of power at nanometre scale. Effects of DIBL, I_{ON}/I_{OFF} ratio, and subthreshold swing are compared for C-MOSFET, DG-MOSFET, and CNTFET devices.

S. K. Sinha et al. [58], analyzed the advantage of CNTFET and oxide thickness's effect on quantum capacitance. Temperature effect and chiral vector variations on threshold voltage has

been studied. The comparison of MOSFET and CNTFET in terms of quantum capacitance has been discussed. In MOSFET, quantum capacitance increases as oxide thickness decreases which increases gate capacitance and increase propagation delay where as in CNTFET, quantum capacitance, gate capacitance and propagation delay decreased with reduction in oxide thickness. The chirality effect on threshold voltage has been studied. For smaller chiral vector, threshold voltage increased and threshold voltage decreased with large chiral vector. Also, it has been analyzed that to reduce the leakage power, threshold voltage should be more and chiral vector is small. The threshold voltage has negligible effect with rise in temperature. There is 4.6% threshold voltage deviation as temperature rises from 27 degrees to 227 degrees and deviation of 3.5% is observed when temperature reduces from -10 degrees to -60 degrees.

A. Singh et al. [59], described that nanoscale devices are replacing complementary metal oxide semiconductor technology. They compared the performance of CNTFET and nanowire transistor taking into account the parameters such as operation, structure, characteristics and challenges in design of device. Various parameters such as I_{ON}/I_{OFF} ratio, inverse subthreshold slope and transconductance have been compared for both the devices. I-V characteristics of both CNTFET and nanowire transistor have been discussed. The carbon nanotube has high I_{ON}/I_{OFF} ratio, higher transconductance and steep inverse subthreshold slope over the nanowire transistor.

S. Rani et al. [60], in this paper, studied that on the basis of operation, properties and structure, a comparison of different types of CNTFET is presented. Nano TCAD ViDES has been used to simulate the double gate planar geometry and three-dimensional structures of these three devices. Based on performance parameters including ON current (I_{ON}), I_{OFF}, and I_{ON}/I_{OFF}, the results are presented. The analysis of effective performance which include variable drain to source voltage (V_{ds}), channel length (L_g), diameter (d), and oxide thickness (t_{ox}), while maintaining other parameters constant. In comparison to conventional, schottky barrier transistors, it has been found from the simulated results that T-CNTFET offers the best performance.

B. Raj et al. [61], presented a model that was compatible for electrostatic schottky barrier CNTFET. In electrostatic SB-CNTFETs, polarity gates are being added to create electrostatic doping. By doping, fermi level for source and drain region shifts and bias of polarity gate. The characteristics of SB-CNTFETs have been studied using nano TCAD ViDES. Various models for schottky barrier and electrostatic schottky barrier CNTFET have been described by authors.

To simulate the properties of CNTFETs, current equations, surface potential models, and quantum capacitance models have been presented. They compared the outcomes with a semi-classical model that employed tedious look-up table method. Therefore, new circuit model made the simulations faster and easier. The work done by authors showed that electrostatic schottky barrier CNTFET has better voltage transfer characteristics as compared to SB-CNTFET.

M. Khosla et al. [62], described a conduction band minima and surface potential based model. Current voltage characteristics for CNT have been investigated by determining relation between gate voltage and surface potential. Quantum capacitance model for carbon nanotube has been studied.

G. Gelao et al. [63], proposed a compact model of CNTFET that was developed on basis on analytical approximations. To check the accuracy, results have been compared with numerical model. This model has been applicable to design both analog and digital circuits.

V. Ramola et al. [64], described that with increase in scaling of devices the power consumption has been increased. So to overcome the problem of power consumption, single metal gate has been replaced by double metal gate. These three-dimensional structures are helpful for reducing SCEs. They compared output characteristics of DG- CNTFET and conventional CNTFET. It has been concluded that I_{ON} and I_{OFF} for double metal gate is smaller than single metal CNTFET. The I_{ON} /I_{OFF} is higher than conventional CNTFET. Also, rise in transconductance has been observed in case of double metal gate CNTFET.

A. Diabi et al. [65], presented a compact model for schottky barrier CNTFET. Physical, geometrical parameters and their effect on dynamic performance were being discussed. Also, effect of V_{ds} on I-V characteristics has been discussed. Various parameters like height of barrier, oxide thickness and nanotube diameter has been investigated by measuring static and dynamic performance. ON current to OFF current ratio is raised by oxide thickness reduction. The OFF current is increased with increase in diameter of carbon nanotube in schottky barrier CNTFETs. It has been shown by the authors that with increase in height of schottky barrier, transition frequency decreases which further decreases the transconductance of device. As the transition frequency increases and ON to OFF current ratio decreases, there is a need to have thin oxide in device so that there is improvement in static and dynamic performance.

J. K. Saha et al. [66], studied the SCEs in DG-MOSFET and CNTFET. Various SCEs namely threshold voltage variations, subthreshold swing (SS) and I_{ON}/I_{OFF} ratio have been calculated

for both devices. It is shown that CNTFET has low leakage power consumption, high ON-current in comparison to double –gate MOSFETs that is utilized in applications with high speed and minimum power.

S. K. Sinha et al. [67], mentioned impact of channel length, work function of metal, chiral vector and high-k value of dielectric on CNTFET's threshold voltage. They studied how capacitance of gate gets affected by oxide thickness and provided justification for the superiority of CNTFETs over MOSFETs in the nanoscale range. High value of threshold voltage can be reached in CNTFETs at low chiral vectors, according to simulation using the HSPICE tool. Additionally, it has been found that temperature has very little impact on threshold voltage of CNTFET.

N. Kalam et al. [68], proposed a model compatible with CNTFETs for non-ballistic regime. Performance of CNTFETs with various gate dielectric constant considering temperature is studied. The drain current has been investigated by varying gate dielectric constant with different gate voltages. ON and OFF current and their ratios decreased with increase in temperature and dielectric constants. Also, effect of temperature on quantum capacitance and DIBL has been studied. Increasing the value of dielectric material slightly vary the drain induced barrier lowering.

S. M. Noorbakhsh et al. [69], developed 2D simulations for CNTFET. Effect of variable temperature ranging from 250K to 500K on several parameters including transconductance and subthreshold swing has been investigated. The authors obtained low ON/OFF current ratio value and high subthreshold swing with temperature rise. DIBL increased linearly with increase in temperature.

R. Marani et al. [70], studied that specifically considering the output resistance, transconductance, cut-off frequency and trans-characteristics, they analysed temperature fluctuations effects on design parameters of CNTFETs. According to analysis of CNTFET I-V characteristics, there are only slight variations with temperature changes, with the exception of the transition regions.

N. V. Karimi et al. [71], studied the parameter variations on characteristics of tunnel CNTFET. The effect of channel parameter has been discussed. Higher drain to source voltage values cause drain current to saturate, turning the device ON. On increasing drain to source voltage, tunneling at drain-channel side occurs. The higher value of OFF current and ON current exists because of ambipolarity. Ambipolarity means conduction in channel is due to two type of

carriers i.e., electrons and holes. It has been investigated that for constant diameter and length, there is increase in tunneling current and ON current with reduction of oxide thickness. Gate – source fringing decreases with thinner gate-oxide. It has also been studied how altering the channel parameters affects the tunnel CNTFET's properties.

S. A. Khan et al. [72], carried a thorough investigation of drain control coefficient effect on CNTFET performance. In this work, device performance was evaluated using an analytical model of CNTFET developed in MATLAB. It has been discovered that higher drain control coefficients improve the device's performance by increasing the drain current, drain conductance and transconductance. However, DIBL also rises with drain control coefficient, which degrades the device's functionality. Additionally, subthreshold swing deviates from the ideal value as drain control coefficient increases, which is also undesirable for scaled-down FETs' low threshold voltage and low-power operation.

X. **Yang et al. [73],** described a model for double-gate CNTFET. The double gate CNTFET helped to reduce ambipolar conduction. The primary and polarity gates were the two gates employed in the construction. Polarity gate is used to operate device in either mode i.e., *p*-type or *n*-type, while first gate is utilised to switch the device ON or OFF. The large values of I_{ON} / I_{OFF} have been investigated to reduce ambipolar effects by including polarity gates. Also effect of schottky barrier height and gate dielectric thickness has been studied on I_{ON}, I_{OFF} and I_{ON}/I_{OFF} ratio.

S. Fregonese et al. [74], presented a compact model for DG-CNTFET. This model described parameters such as charge, electrostatic modeling and quasi ballistic transport. Ten identical devices have been employed to simulate the ring oscillator circuit. Additionally, they investigated how the structure and related equations of DG CNTFET model are scalable and may be applied to simulate various 1-D ballistic DG FET types, including those based on graphene nanoribbons.

N. V. Karimi et al. [75], analyzed the performance of asymmetric graded double-halo tunnel CNTFET. It has been discussed that source-side doping reduces DIBL and drain-side halo doping lowers drain energy barrier and BTBT rise was observed. Also, subthreshold swing increases using this profile.

A. Naderi et al. [76], described CNTFET for reducing band to band tunneling. The maximum doping was done at source and doping at drain was minimum. There is an improvement in power delay and delay versus ON-OFF current.

N. Sardana et al. [77], discussed that short channel effects come into existence with decrease in channel length of device. CNTFET has been described as the important contender as compared to MOSFET to overcome these effects. Also, logic gates have been studied using CNTFETs.

R. Marani et al. [78], studied that in order to determine which CNTFET model is simplest to implement in simulation software, various CNTFET models were compared through the SRAM cell design. Here, main focus was on Stanford virtual source model (VS-CNTFET) and on already proposed model. Comparison of performance, power dissipation and stability is highlighted in simulation results while analysing SRAM cell with CNTFET technology.

A. Dutta et al. [79], analyzed the comparison between CNTFET and MOSFET SRAM cells. It was determined that SRAM cell based on CNTFET can be used for storing memory. SRAM cell based on CNTFET has less scattering, less power supply, better sensitivity and PDP. Furthermore, various types of ternary logic gates considering power dissipation have been discussed in this paper.

K. S. Sandha et al. [149], investigated the temperature-dependent PDP MWCNT interconnect bundle at three different technological nodes, namely 32 *nm*, 22 *nm*, and 16 *nm*, considering a variety of temperature range (200 K to 450 K). A comparative analysis was done on copper interconnects and MWCNT bundle interconnects. When compared to copper interconnects at three technology nodes, temperature-dependent MWCNT bundle interconnect performs better considering delay, power and PDP.

2.6. CNTFET MODELS

Electrodes that act as source and drain were imprinted on top of carbon nanotubes that were already laid down to enhance electrical properties of first manufactured CNTFET. Further, to improve metal and nanotube contact, Titanium (Ti) and Cobalt (Co) electrodes were considered in addition to gold (Au) using thermal annealing step for reducing the contact resistance. Likewise, *n*-type CNTFET was fabricated by doping and thermal annealing of alkali gas into vacuum. This process involves the charge transfer with in carbon nanotube. Thus, *n*-type CNTFET was also fabricated.

Based on fundamental physics, such as doping profiles of devices, modeling of semiconductor device develops models for behaviour of electrical devices. The development of compact models that make an attempt to depict how these devices behave electrically but

typically do not derive it from the underlying physics, may also be included. Examples include the well-known SPICE transistor models. Typically, it begins with the results of a simulation of the semiconductor process. MOS and bipolar transistor modeling are dominant in physics and modeling devices in ICs. Other crucial devices, such memory devices, on the other hand, have very different modeling requirements. Of course, reliability engineering issues exist as well, such as those involving electro-static discharge (ESD) protection circuits and devices, where the role of the substrate and parasitic devices is important.

C. S. Lee et al. [80], presented a data-calibrated compact model of virtual-source (VS)-based CNTFETs which describes inherent I-V and charge-voltage properties. Following characteristics of model have been included: (i) carrier versus velocity obtained using experimental devices having gate lengths as short as 15 *nm*; (ii) carrier velocity and effective mobility based on CNT diameter; (iii) depending on device dimensions, SCEs can include DIBL and inverse subthreshold slope degradation.; and (iv) decrease in gate capacitance can be attributed to small-signal capacitances, such as CNT quantum capacitance effect. For technology benchmarking and performance projection at sub-10 *nm* technology nodes, CNTFET model was appropriate because it reflected the effects of dimensional scaling.

C. S. Lee et al. [81], described a data-calibrated model of band-to-band tunnelling currents, direct source-to-drain currents, and contact resistance for CNTFETs. Drive current and leakage current trade-offs for CNTFETs were investigated using this model in the context of selecting CNT density, diameter and length of gate for a target contacted gate pitch. The model included decreased performance by parasitic effects and the impacts of dimensional scaling. With the help of physical knowledge, they described an analysis of CNTFET device parameters conducted close to the scaling limit. They also predicted the performance of CNTFETs with expected contacted gate pitch of 31 *nm* at 5-*nm* technology node. The research, which takes into consideration parasitic resistance, capacitance and tunnelling leakage current, indicated that 180 *CNTs/m* of CNT density would enable CNTFET technology to fulfil drive current target of 1.33 *mA/m*, that was within range of present experimental capabilities.

A. Singh et al. [82], provided a model of CNTFET to be used in circuits. Model was explicitly linked chirality to the transport mechanism. Additionally, it does not take into account self-consistent equations and was utilised in the creation of compatible model in HSPICE. Model was used to simulate top gate CNTFET in MATLAB, and the outcomes were compared to simulations of a similar structure that were applied using NanoTCAD ViDES, in order to

validate model. SRAM and an inverter circuit were created using HSPICE to show how well the model fits into the circuit. In the end, device simulations from NanoTCAD ViDES were compared to SRAM performance measurements.

B. Raj et al. [83], proposed a conduction band minima and compact model for CNTFET based on surface potential. Proposed model relates chirality within the quantum capacitance limit to I-V characteristics. For several capacitance models that were utilised to establish the connection between gate voltage and CNT surface potential, C-V characteristics were properly modeled. Proposed model of circuit strictly complies with quantum capacitance limit after discussing role of various capacitances. Given that it forbids self-consistent numerical simulation, the suggested model was effectively built for circuit simulations. Additionally, the results of experiments were contrasted with this compact model. Model has been employed for simulating an inverter in HSPICE.

J. Luo et al. [84], presented a virtual-source model, a semi-analytical model of CNTFETs with experimental data for gate length of 9 *nm* has been calibrated. The main performance limitation for CNTFETs was found to be contact resistance, and source-to-drain tunnelling that causes a large amount of leakage since carbon nanotubes have a low effective mass, which inhibits further gate length downscaling. By optimization of gate length, contact and extension regions, At 11*nm* and 7*nm* technology nodes, improvement in gate delay by more than 10% was observed and OFF-state leakage current remained below $0.5 \mu A/\mu m$.

A. Tijjani et al. [85], studied that on the basis of simulation analysis, goal was to examine impact of temperature variation in CNTFET. It was investigated how variations in temperature affect the use of CNTFETs for channel materials and TiO_2 as dielectric materials and gate control parameter 0.88 using nano device simulator FETtoy. The range of temperatures covered by this research study was from 273 K to 375 K, along with several parameters including fixed transport effective mass, drain control, and CNT (carbon nanotube) diameter. I_{ds} vs gate voltage, quantum capacitor versus gate voltage, DIBL, subthreshold swing (S), ON current, OFF current, transconductance (g_m), output conductance (g_d), and carrier injection velocity (v_{ij}) were some of the output parameters that were examined. It was clear from the results that TiO_2 when used as channel material for carbon nanotube suppresses the subthreshold effects in nanodevices.

2.7. APPLICATIONS OF CNTFETs

Since SRAM is being examined primarily for reducing frequency gap between CPU and main memory, its importance is increasing with technology. In modern designs, SRAM consumes up a large area of chip. From this viewpoint, SRAM has significant effects on computer systems' performance, reliability and consumption of energy. The reduced device dimensions of today's technology require SRAM design to be as small, energy-efficient and high-performing as possible. Maintaining its functionality through process and environmental variations, however, is difficult at nanoscale nodes. The technology scaling also reveals challenges for conventional bulk CMOS transistors below the 20 *nm* technology node.

SRAM reliability is adversely affected by the scaling process. At each emerging technology node, the number of possible faults increases significantly because of high device failure rates and low yield. Multigate devices, utilising CNTFET technology, have emerged as a viable solution for continued scaling, providing high current control in a compact area.

There are various applications of CNTFETs in different fields of electronic industry at nanoscale regime. One of the most prominent applications of CNTFET is Static Random Access Memory. The literature review related to SRAM cell based on CNTFET has been discussed in this section.

S. Ahmad et al. [86], stated that a successful technique often employed to fulfill ultra-low power demands of modern digital systems was voltage scaling. However, voltage scaling has a significant effect on SRAM cell stability in ultra-scaled technologies. This paper offered a thorough analysis of numerous designs and methods for resolving problems with SRAM cell stability. One method for solving the read stability problem is to decouple read operation. To improve read stability, literature has also employed loop-cutting, additional discharge path-based techniques, and modified schmitt-trigger based cell cores. However, most of these techniques have reduced the half-selected (HS) cells' write-ability and stability. The majority of write-ability enhancement strategies either decrease the current required to store data or strengthen access transistors to improve write current. It contains cells that are multi-V_{th} write assist based, feedback cutting, or V_{DD}/V_{SS} cut off. They examined alternate bitcells and a number of peripheral read/write assist mechanisms in addition to the bitcells themselves. Effective read-assist methods include dynamic WLUD and WL underdrive (WLUD). The peripheral strategies for improving write ability include VDD floating/lowering, transitory VDD collapse, WL boost, WL delayed boost, VSS raised, dual split control-VSS increased,

and negative BL (NBL). Additionally, a number of methods for resolving the HS cell problems were described, including write-back, bit-interleaving array design modification and column decoupled local wordlines.

C. Madhu et al. [87], studied that everyday demands for efficiency and speed are constantly increasing. Integral density of chip rises as technologies continues to be downscaled. The dependability and stability of memory device including SRAM and DRAM in various environments is an important concern. Evaluation of 6T SRAM cell based on CMOS at different technological nodes were done in paper. Using predictive technology model (PTM) file, primary goal was to simulate a 6T SRAM and assess its performance at several technology nodes. Consistency of SRAM bit cell considering static noise margin (SNM) was examined using the butterfly curve approach in HSPICE tool. Outcomes obtained in the paper clearly demonstrate that when we move to scaled technology nodes, delay decreased and stability increased, as evidenced by the increase in RSNM and WSNM for 6T SRAM cell, respectively, of 7.72% and 5.94%. The study's reduction in delay made 6T SRAM cells at 45 *nm* is suitable in high-speed applications, such as those for aircrafts and satellites.

S. Bala et al. [88], presented that a 6T SRAM cell on the basis of an electrostatically doped (ED) tunnel (CNTFET) was constructed and simulated in HSPICE. Based on power dissipation, read/write noise margin and read/write delay, ED tunnel CNTFET based 6T SRAM cell performance was examined. Simulation results are presented in comparison with conventional CNTFET based 6T SRAM cell indicate improved FOMs without affecting stability. For 0.9 V and 0.5 V values of V_{dd}, read noise margin was enhanced by 9.2% and 7.5%, but write noise margin was improved by 16% and 14%, respectively. Power dissipation was decreased by value of 9 pW at 0.9 V V_{dd} and by value of 4 pW at V_{dd} of 0.5 V. Results demonstrated that it can be applied for applications where low power is required.

M. Khapekar et al. [89], focused on dynamic power dissipations for operations (read and write) of 12T SRAM at different temperatures. Leakage current was reduced, so the virtual V_{dd} concept was used in the proposed 12T construction. Therefore, a decrease in leakage current resulted in a decrease in dynamic power. SRAM cell power dissipation was calculated and contrasted with few other memory cells already in use. It was a short channel BSIM4 model that was proposed for cell. Power consumption of a 12T SRAM was measured to be 44.7nW for read operation at 40 nW and 38.79 nW for write operation. Less power was lost while using the suggested SRAM cell. Tanner-13 EDA tool was used for simulation for 50 *nm* in this paper.

G. S. Kumar et al. [90], studied a 6T SRAM cell on basis of GAA-CNTFET architecture that was very stable and power-efficient. CNTFET and GAA-CNTFET are both used in 6-T SRAM cell design and analysis for several performance parameters including SNM, read SNM, write SNM, latency & leakage power. Impact on leakage current by changing supply voltage is further discussed. It was discovered that at higher supply voltages, the GAA-CNTFET is responsible for less power loss. Dual flat band voltage approach is applied to analyse the 6-T SRAM cell under various *p*-type CNTFET flat band conditions while holding the *n*-type flat band constant.

R. S. Prasad et al. [91], presented that the electronic industry, SRAM that serves as cache for system-on-chip is crucial. In recent years, CNTFETs have been employed as an alternative to silicon in circuit designs that require high performance, high stability and low power. For low-power cache memory, it is essential to design SRAM cells on the basis of CNTFET. Bit-lines in cells consumed the most power due to the higher power dissipation required to supply power to longer bit-lines with high capacitance. Due to bit-full line's voltage swing, the cache write used a significant amount of power. The innovative 7T SRAM cell described in this paper is based on a CNTFET that would reduce write power consumption by just performing a write operation on one of bit lines.

H. Kumar et al. [92], used Cadence Virtuoso Tool 180 *nm* technology, for the performance evaluation of 6T, 7T conventional CMOS planar SRAM cell based on a CNTFET architecture. The Stanford Compact Model's Verilog-A code was applied for CNTFET, and cadence Virtuoso Tool was used to generate symbol. The chiral vector (19,0) for CNTFET having physical channel length (L_{CH}) of 32.0 *nm* & contained a single carbon nanotube. Results demonstrated that CNTFET-based SRAM cells perform significantly better than traditional SRAM cells. For 6T CNTFET based SRAM, the current study found to have reduced power consumption by 66%, improved write delay by 24% for "0" and improved write delay by 34% for "1."

N. S. Bhat et al. [93], stated that CNTFET describes a field-effect transistor that, in contrast to the conventional MOSFET structure, use one carbon nanotube or a group of them to serve as channel material. It was also investigated that there have been significant advancements made in CNTFETs since their initial demonstration in 1998, and they now hold great promise as a possible substitute for silicon in electronic devices in future. Carbon nanotubes act as a promising material for nano-scale electron devices, such as quantum-effect devices and

nanotube FETs for novel intelligent circuits and ultra-high-density ICs, which are anticipated to lead to a breakthrough in current silicon technology. It was also studied that the purpose of a SRAM was to meet two requirements: i) SRAM acts as cache memory for CPU and DRAM. ii) Since SRAM requires no refreshing of current compared to DRAM, the driving force behind low power applications is SRAM technology. On the basis of the knowledge gained, various SRAMs designed for CNTFETs have been presented in this paper. The Stanford CNTFET model used in HSPICE simulations of this circuit revealed a significant improvement in power savings.

N. K. Shukla et al. [94], studied that a new class of energy-constrained systems made the necessity of power even more prominent as a result of growing need for portable semiconductor applications that run on batteries and ongoing growth of devices using CMOS. Also, operating CMOS circuits operating at power supply voltage less than transistor threshold is of recent interest in low-power VLSI design. Applications relating to wireless devices, healthcare applications, spacecraft applications, and other fields are all relevant to sub-threshold functioning because subthreshold circuits enable the fabrication of low power designs on contemporary CMOS technology. One of the options the designers have when creating low power SRAM circuits is lowering the supply voltage. SRAM with low power was greatly complicated by intra-die fluctuations and leakage - power in technologies beyond 130 *nm.* Leakage reduction for SRAM cells has been accomplished using high threshold (HVT) transistors and low supply voltages. They evaluated a typical SRAM cell and examined cell's leakage and standby- currents impact considering a range of V_{dd} and operating at deep sub-micron technology such as 90 *nm* and 65 *nm* for variable temperatures. Here, it has also been noted that temperature affects leakage currents at different supply voltages. It was noted that leakage increases to 90% for 90*nm* and 89% for 65*nm* at 1V and 0.5V of V_{dd}, respectively, when temperature increases from 400^0C to 1000^0C.

S. Joshi et al. [95], studied that SRAM is one of most widely used memory components used in most digital devices because of its incredible capability to hold data. Because of rapid advancement in technology, design of SRAM faces significant issues considering delay, stability and noise margin. This work compares various topologies' performance based on CNTFET SRAM cell including 6T, 7T, 8T, 9T, and 10T cells, considering consumption of power, read delay and write margin (WM), and static noise margin (SNM). To account CNTFET's nonidealities, tube diameter variations and metallic tubes effects are considered for

different topologies considering performance parameters including SNM, WM, delay during read operation and consumption of power.

G. B. Raja et al. [96], presented that instead of using CMOS, other method suitable for specific design must be investigated. Due to its unique features concerning power consumption, leakage power and delay etc., majority of recent designs are based on carbon nanotube FETs or FinFETs. This paper's main objective was to construct 6 T SRAM cells for CMOS, CNTFET, and FinFET, and then was compared considering the parameters including average power, delay and leakage. Simulated results were obtained for a 6T SRAM cell employing CMOS, FinFET and CNTFET at 32 *nm* technology node. Using the HSPICE tool, the designs were simulated and parameters like average power, leakage power and average delay were calculated for three various designs and compared. It is evident from results that in comparison with CMOS-based design, FinFET and CNTFET exhibit better performance in all aspects.

C. Venkataiah et al. [181], described that SRAM cell is better than DRAM as it does not require periodic refreshment of data. Capacitor is used to store data in DRAM cell. This paper analysed the performance of SRAM cells considering different types of FETs for its design. A variety of parameters like read/ write power consumption, delay and PDP have been evaluated for SRAM cell based on CNTFET. This cell is compared to SRAM cell based on CMOS. It was found that delays during write and read operations are improved by 85.8% and 94.3% respectively. Simulations were done in HSPICE tool.

S. Lin et al. [183], proposed a SRAM cell considering CNTFET which is designed for low power applications. Different threshold voltages have been applied and these can be adjusted by varying CNT diameter. While proposing SRAM cell structure, same type of CNTFETs have same chirality and *n*-type and *p*-type transistors possess variable chiralities. Various parameters like power dissipation and write time were used to evaluate SRAM cell. Simulations have been done to investigate the CNTFET SRAM cell's power and delay due to its process variations. SRAM cell based on CNTFET counterpart SRAM cell using CMOS when it is applied to process variations such as diameter, temperature and supply voltage.

2.8. GAPS IN PRESENT STUDY

According to literature review, it has been analyzed that as feature size of MOSFET is decreasing, short channel effects come into existence with the scaled dimensions of device.

Because of higher thermal conductivity, carrier mobility and low leakage current, CNTs have the potential to replace them.

The performance of MOSFETs is restricted due to presence of various SCEs including leakage current, threshold voltage fluctuations and DIBL. CNTFETs have presented good results in terms of leakage current, less fluctuations in threshold voltage as compared to MOSFETs. CNTFETs have higher electron mobility which allows faster switching and hence there is less power dissipation in CNTFET as compared to MOSFETs. CNTs are thermally stable than MOSFETs and there is reduced heat generation in case of CNTFETs.

Various studies have shown that CNTFET is a leading contender in overcoming the short channel effects as seen in MOSFETs at nanoscale. Double-gate structure of CNTFET is proposed due to its various advantages over single-gate CNTFET. There is increase in drive current at low values of threshold voltage and supply voltage. Power consumption also reduced using the double-gate as there is decrease in leakage current at the gate and channel of the device. Further, the chip area gets reduced as two gates allow separate control of gate on voltage.

When source and drain are closer to each other, leakage current flows in the device that needs to be investigated for CNTFETs. As the thickness of silicon dioxide becomes thin, tunnel current increases significantly and there are fluctuations in threshold voltage and transconductance. Thus, high k value of dielectric materials are needed so as to reduce tunneling current. The fabrication of CNTFETs remains a big challenge. Some new techniques need to be proposed and issues related to it need to be taken off. The effect of process variations and carbon nanotube diameter needs to be investigated.

Further, the effect of temperature and bandgap on single gate CNTFET considering a variety of parameters including ON current, OFF current and ON/OFF current ratio, DIBL and subthreshold slope have been investigated. Few work have been examined in the literature to analyse temperature effect on CNTFETs' performance. Therefore, temperature dependent work needs to be extended considering double gate CNTFET so as to outperform the MOSFET based devices in terms of various performance parameters.

Further, it has been concluded from literature that CNTFETs can be used in combinational circuits for designing logic gates, multiplexer, adder, subtractor and decoder. In present era, with the advancement in semiconductor industry, the size of different handheld and portable electronic devices gets reduced day by day. As maximum area is used up by memories so there

is a need for longer battery backup and high performance of the device which has become main target for research work. With the scaling of devices, power has become major challenge for semiconductor industry. Therefore, less power and high-speed memory design are necessary. For evaluating performance of CNTFET-based SRAM cell for designing devices with low power at different technology nodes, a number of performance parameters considering delay, power delay product (PDP) & power dissipation, can be explored in this work which be used to design both high-speed and low-power devices.

2.9. OBJECTIVES OF PROPOSED WORK

The following objectives have been proposed and included in the research. These objectives are based on earlier research, provided literature review, and existing knowledge:

1. To develop the optimized structure of double gate carbon nanotube field effect transistor (CNTFET).
2. To model the threshold voltage and drain current of double gate carbon nanotube field effect transistors (CNTFET).
3. To examine the impact of thermal aware environmental conditions on double gate carbon nanotube field effect transistors.
4. To analyze the performance of CNTFET SRAM cell using carbon nanotube field effect transistors.

2.10. RESEARCH METHODOLOGY

The following aspects will be included in work to be done for methodology for suggested proposal.

Various short channel effects have been studied. The possible alternatives to overcome SCEs have been analysed taking into account the scaling of device. Carbon nanotubes and its types-SWCNTs and MWCNTs are studied in detail. Their physical structures are analysed thoroughly. The properties and history of carbon nanotubes have been discussed. Also, the various advantages of CNTFET over MOSFET have been studied. The different type of structures of DG-CNTFET have been selected on the basis of variable doping and device dimensions. Out of these structures, the optimized structure of DG-CNTFET has been obtained and compared with existing structure of DG-MOSFET.

Drain current modeling equation of DG-CNTFET is derived to compare the result with DG-MOSFET. Various parameters are calculated to compare the results to minimize SCEs. Device's input and output characteristics have been taken into consideration when evaluating

its performance. The effect of thermal aware environmental conditions on DG-CNTFET has been investigated to obtain performance analysis of device at variable temperature range. The simulated results in NanoTCAD ViDES have been compared with drain current developed through an analytical model in MATLAB to check accuracy of results obtained. Further, the performance analysis of DG-CNTFET's threshold voltage is done and results is obtained in nanoHUB tools.

Performance of SRAM cell based on CNTFET at various technology nodes is evaluated considering power dissipation, propagation delay, and power delay product by analysing and evaluating SRAM cell in HSPICE. Further, CNTFET 6T SRAM cell was compared with CMOS based 6T SRAM cell to analyse performance of cells at different technology nodes. Thus, obtained results in terms of power dissipation, delay and PDP helps to compare and conclude performance of 6T SRAM cell using CNTFET and CMOS technologies at different technologies in this work. SRAM cell using CNTFET have a great potential as VLSI interconnect material for upcoming generations.

CHAPTER 3

CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET) - An Overview

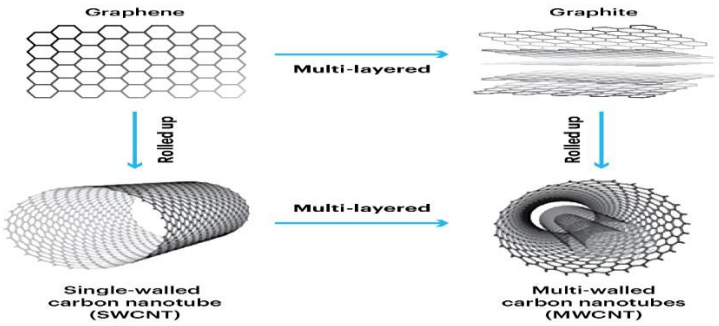
The main aim of chapter is to study basics of carbon nanotubes and their physical properties. This chapter starts with chirality concept which is used to study physical and electrical properties of device. This chapter discussed the detailed information regarding the CNTFET and its classification, DG-CNTFET and advantages of DG-CNTFET over the single gate CNTFET. The chapter concludes with structure optimization of DG-CNTFET.

3.1. CARBON NANOTUBES

Although, material 'carbon' was discovered many years ago, but its crystalline forms have been introduced and experimentally used in last few decades. Its crystalline forms contain buckyballs, carbon nanotube and graphene. Graphite and diamond were the older forms of carbon and have been replaced by newer forms such as carbon nanotube and graphene that describes significant properties like extremely high electron mobility and thermal conductivity. The new forms of carbon are also known as reduced- dimensional nanomaterial as both carbon nanotube and graphene occupy much less space as compared to graphite and diamond [97]. CNTs have a high intrinsic mobility that is greater that of many semiconductors due to their ballistic transport along tube direction. Their thermal conductivity is better than diamond and their mechanical tensile strength is much higher than steel.

Carbon nanotube is a rolled hollow cylinder of graphene sheet that contains carbon atoms appear in a hexagonal pattern. The diameter of carbon nanotube varies from few nanometres to 100 nanometres and its thickness is around 0.1 nanometres [97]. Depending on various kind of carbon nanotubes, these exhibit several electrical, thermal and structural properties [98]. Carbon nanotube has good electrical conductance and mechanical properties which makes it a promising candidate in VLSI industry.

Ballistic transport occurs in carbon nanotube so electrons can travel through large distances without scattering due to which it has low electrical resistance. As the resistance of carbon nanotube is less, so it can dissipate less energy. Therefore, carbon nanotube can be employed in applications with less power to solve power consumption problems [99].



(a) (b)

Figure 3.1. (a) SWCNT (b) MWCNT structure [100].

Two categories of CNTs exist namely single walled carbon nanotubes (SWCNT) and multi walled carbon nanotubes (MWCNT) as described in figure 3.1. (a) and (b) respectively.

SWCNT have carbon atoms that are arranged in hollow cylindrical structure with a diameter of 0.5 to 5 nanometres [101]. Multi-walled carbon nanotube structure is somewhat similar to that of SWCNT but the difference is that MWCNT consist of concentric cylindrical walls of carbon nanotubes [102]. Diameter of both internal nanotube and external most nanotube can vary from few nanometres to hundreds of nanometres.

3.2. IMPORTANCE OF CHIRALITY ON CARBON NANOTUBE

Chirality is one of most important concepts for describing the different configurations, electrical properties and characteristics of carbon nanotubes. Chirality is obtained from a Greek word that is used for hand. Chirality is used for representing reflection symmetry of an object and its mirror image [103].

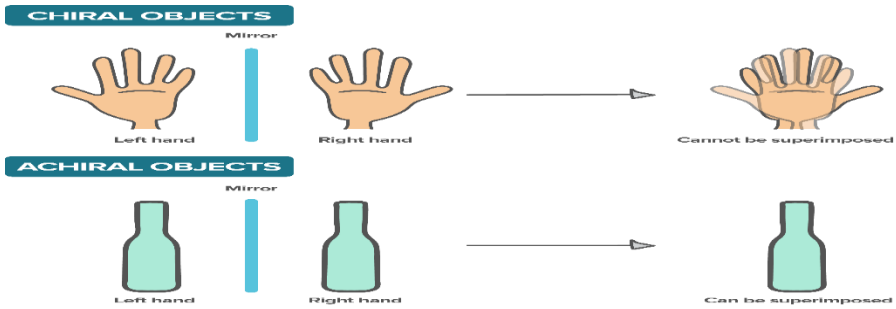


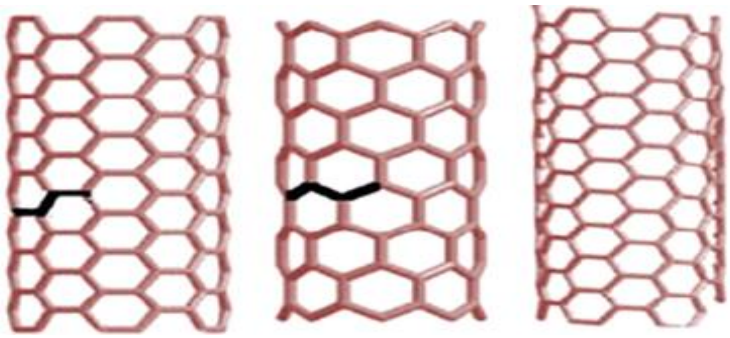
Figure 3.2. Chiral and achiral objects [104].

Chiral objects are difficult to superimpose on their mirror images, but achiral objects are susceptible to superimposing on its mirror image. This can be illustrated by considering the example of a human hand, the mirror image of left hand is right hand and it never superimposes on right hand. So, we can say that human hand is chiral object as shown in figure 3.2. On the

other side, consider the example of a circle, the mirror image of circle is also a circle so it can be superimposed on top of original image.

Chiral CNTs cannot be superimposed on mirror images whereas CNTs superimposed on their mirror images are known as achiral CNTs. There are three kinds of SWCNTs depending on geometry of cross-section of carbon nanotubes.

Armchair CNTs, zig-zag CNTs and chiral CNTs are three different kinds of SWCNTs based on the chirality and their geometry is described in figure 3.3.



(a) (b) (c)

Figure 3.3. CNT configuration with chiral vector C_h and its basis vectors (a) Armchair (b) Zig-zag (c) Chiral [105].

3.3. PARAMETERS DECIDING PERFORMANCE OF A DEVICE

Transistor is a type of semiconductor device applied to enhance power and the strength of signals in electrical systems. This is one of fundamental building blocks in modern electronics [106]. It is made of semiconductor material and consists of three terminals that connect to a circuit in an electronic device. Three most significant characteristics of any transistor are speed, power consumption and scalability [107]. These features decide the performance of any transistor. To replace the existing technology of silicon based MOSFET, CNTFET can outperform MOSFET in terms of these characteristics in order to give better performance of device.

CNTFETs act as a promising candidate to MOSFETs. The main drawbacks of MOSFET are short channel effects which have been reduced by using CNTFETs [108]. Device performance is measured considering speed and power which has been mentioned in this section of the chapter.

3.3.1. Speed

Speed plays an essential role in analysing device performance, whether it's a computer, smartphone, or any other electronic gadget. The importance of speed in evaluating the

performance of device can vary depending on the specific device applications and its usage, and impacts the performance of the device in several ways. A faster device can handle multiple tasks simultaneously with ease, ensuring that users can switch between applications or processes without noticeable lag or slowdowns. Faster processing allows for quicker completion of tasks which can save valuable time. In CNTFET, due to ballistic transport mechanism, mean free path (MFP) is larger than path of carriers. So, there is less collision of charge carriers which reduces resistance in the CNTFET [108-109]. Thus, it is easy to achieve high speed in terahertz for processors in today's scenario.

3.3.2. Power

Speed also affects the power efficiency of device. In some cases, faster processors may be more energy-efficient because they can complete tasks more quickly, allowing the device to enter a low-power state sooner. But extremely fast processors may consume more power under heavy workloads. Therefore, power is another factor which affects the performance of device in any system. Power consumption gets reduced when device is OFF because, in the 'OFF' state, the device typically consumes very less or no power at all. Turning 'OFF' a device often disconnects from its power supply, cutting off the source of electricity. This ensures that even if there are residual leakage currents, they are too small to show significant effect on overall consumption of power. But, at scaled down technology nodes, leakage current increases which become an important factor that need to be studied for high performance of the device. As compared to MOSFET design, power consumption of CNTFET is less [110]. Carbon nanotubes have high carrier mobility as compared to MOSFETs, allowing for faster switching speeds. Faster switching can lead to shorter ON-times and OFF-times, which, in turn, can reduce dynamic power consumption. Further, CNTFETs allows for better control over channel length and reduction in leakage current, which is a significant source of power consumption in MOSFETs as they scale down to nanometre level. So, transistor made of CNTFET can be turned ON and OFF more effectively, reducing standby power consumption. Inspite of large gate length and thickness of oxide, CNTFET replaces MOSFET technology.

3.3.3. Scalability

Carbon nanotubes possess high mobility property, which measures how quickly electrons can move through a material. The high value of carrier mobility in CNTs results in faster switching speeds and better overall transistor performance when compared to traditional MOSFETs. This advantage of higher mobility becomes more prominent as feature sizes decrease because the distances that electrons need to travel become shorter [111]. CNTFETs exhibit lower leakage current compared to MOSFETs, especially as feature sizes shrink [111]. The reduced leakage

current in CNTFET contributes to lower power consumption and improved energy efficiency. CNTFETs can operate at higher frequencies and power levels without overheating, further improving their performance in certain applications. Therefore, the devices made with CNTFET gets improved with the reduction of feature size. CNTFET shows better results when compared to MOSFETs for various applications.

3.4. HISTORY OF CARBON NANOTUBE FIELD EFFECT TRANSISTORS

In 1998, first CNTFET was invented, named as back gate CNTFET. Early structure of CNTFET was *p*-type in nature. It was initially unclear whether this was because of contact doping or doping using atmospheric oxygen adsorption. Doping by an alkali (electron donor) gas and thermally annealing in vacuum, *n*-type conduction was achieved [112]. Charge transfer occurs within nanotube bulk when doped by exposure to an alkali gas, which is similar to doping in traditional semiconductor materials. The first carbon nanotube CMOS circuits both utilizes *p*-type and *n*-type CNTFETs [112].

Some of the drawbacks of back-gate CNTFET were low value of transconductance and high ON-resistance of around megaohms (MΩ) [112]. Therefore, this device required high gate voltage to turn 'ON' the device. To overcome these drawbacks, this structure was modified to top gate CNTFET which resulted in improvement of electrical characteristics of CNTFET [113].

To get better performance and remove the shortcomings of back-gate CNTFET, first top gate CNTFET was developed in 2003 [113]. The full advantage of gate dielectric was offered by CNT, which was completely embedded in gate insulator. *n*-type and *p*-type devices both can be made using CNTFET's top gate topology. Another advantage is that it can be easily modified to make it suitable for high-frequency operation, that back-gated devices are unable to achieve because of large overlap capacitance between drain, gate and source. With these properties, devices with top gate become technologically significant CNTFETs manufactured so far which are comparable to MOSFETs.

3.5. CARBON NANOTUBE FIELD EFFECT TRANSISTOR (CNTFET)

The promising candidate at nano-scale regime in VLSI industry is CNTFET. CNTFET shows higher performance, less power consumption, high power density and high speed. Studies have described that CNTs have very high thermal conductivity value and this property of CNTs can be applied in FET devices [105, 108].

A nanoscale device known as a CNTFET is capable of providing high-performance, high-power density integrated circuits at low power consumption. Higher current carrier mobility of CNTFETs, enable CNTFETs to provide a superior driving current density [108].

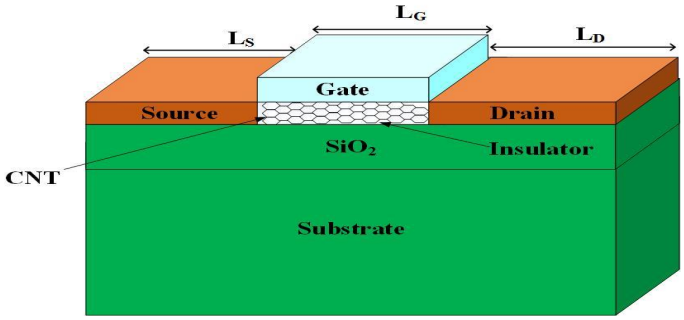


Figure 3.4. CNTFET structure [27].

A device that uses CNT as the channel is CNTFET. The ability of CNTFET to carry high current and because of its metallic and semiconductor properties, these can be widely used in many applications. Smaller dimensions, low consumption of power and high speed performance are necessary with advancement of new technology [107]. There are some disadvantages like shorter channel effect which are overcome by CNTFET.

A CNTFET is formed by replacing bulk silicon with a single CNT or multiple CNTs as channel just as in MOSFET which is described in figure 3.4. [27]. CNTFET also includes three terminals such as source, drain and gate. CNTFETs operate on basis of field-effect principle. An electric field is produced when a voltage at gate electrode is applied that modulates flow of charge carriers—electrons or holes—through carbon nanotube channel. Current between source and drain in device is controlled by gate of device. This modulation of current allows CNTFETs to function as switches or amplifiers.

3.5.1. Types of CNTFET

CNTFETs have been divided into number of types depending on the design and fabrication of device. On the basis of design and fabrication of the device, CNTFET has been classified into four types which are as follows:

- Back-gate CNTFET
- Top-gate CNTFET
- Wrap-around CNTFET
- Suspended CNTFET

3.5.1.1. Back gate CNTFET

The early methods for fabricating CNTFETs comprised of pre-patterning the parallel metal strips over a silicon dioxide substrate, followed by random deposition of CNTs (which is semiconducting in nature) on top [114].

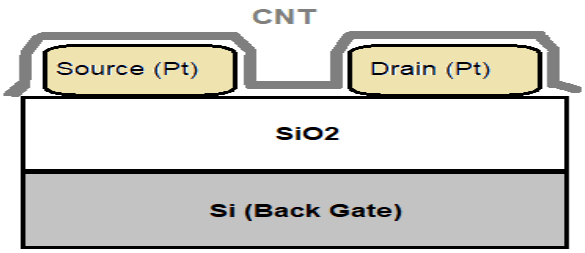


Figure 3.5. Back-gate CNTFET structure [114].

'Source' and 'drain' contacts are made up of a metal strip. The silicon oxide substrate can be utilized as gate oxide and metal contact on back makes semiconducting CNT gateable as shown in figure 3.5. The semiconducting nature of CNT, increases the contact resistance because there is a formation of schottky barrier at metal–semiconductor interface. These types of CNTFET have low transconductance which resulted from the high contact resistance. Reason for high contact resistance is devices' weak van der Waals coupling to their noble metal electrodes. The SiO_2 film is dispersed with a thin layer of SWCNT, which is used to make source and drain electrodes composed of transition metals that are compatible with silicon technology, namely titanium (*Ti)* or cobalt (*Co).* At high temperature, contact resistance decreases forming a low resistance *Co* contacts and *TiC* contacts. The disadvantages of this type of CNTFET is that it has high contact resistance and low transconductance [114].

3.5.1.2. Top gate CNTFET

The advantage of this method is that drain current is raised from nano amperes to micro amperes, transconductance is also increased. So this method is preferred over the previous type of CNTFET though the fabrication process is complex.

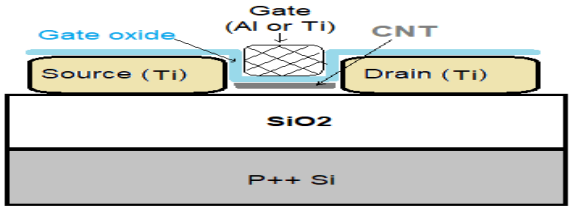


Figure 3.6. Top-gate CNTFET structure [114].

On a silicon oxide substrate, single-walled carbon nanotubes are solution deposited (process of settling of particles from a solution or suspension on to a pre-existing surface). Then, scanning electron microscope is applied to locate individual CNTs. After isolating a single tube, high-resolution electron beam lithography is applied to define and prepattern source and drain contacts [114]. By strengthening the bond between contacts and CNT, reduction of contact resistance takes place when an annealing step at a high temperature is performed. Then, either through evaporation or atomic layer deposition, a thin top-gated dielectric is deposited on top of CNT as shown in structure described in figure 3.6. Operation is completed when top gate contact is applied to gate dielectric. As gate dielectric is thin in nature, so large value of electric field can be generated by lower gate voltage.

3.5.1.3. Wrap-around CNTFET

These CNTFETs are also called gate-all-around CNTFETs and are improved structure in comparison with top-gate CNTFET as described in figure 3.7. In this, entire CNT circumference is gated rather than only portion that is close to metal gate contact. Ideally, this should enhance CNTFET's performance by reducing leakage current and increasing ON/OFF current ratio of device. Wrap-around gate CNTFETs have a more effective coupling between gate and channel since gate is in close proximity to channel from all sides. This design allows for improved gate efficiency and better control over current flow and reduced leakage.

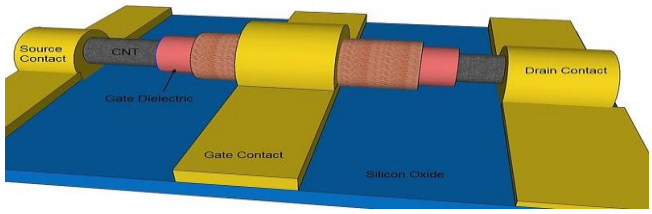


Figure 3.7. Wrap-around CNTFET structure [115].

The first step in fabrication of a device is use atomic layer deposition for wrapping CNTs in a gate dielectric and gate contact [115]. The ends of the wrapped nanotubes, where their wrappings etched off are exposed when they are solution-deposited on an insulating substrate. On CNTs ends and metallic outer wrapping, source, drain and gate are then deposited.

3.5.1.4. Suspended CNTFET

Reduced scattering at CNT-substrate interface is an advantage of this technique that enhances the performance of the device. The reduced scattering at CNT-substrate contact in suspended

gate CNTFETs is primarily due to the physical gap between the CNT and the substrate, which minimizes direct interactions and interference. In contrast, top gate and wrap gate CNTFETs have a closer interaction between the CNT and the gate, which can lead to increased scattering effects arising from gate material properties and geometric variations.

To minimize contact with substrate and gate oxide, CNTFET device design comprises of suspending the nanotube above a trench as depicted from figure 3.8.

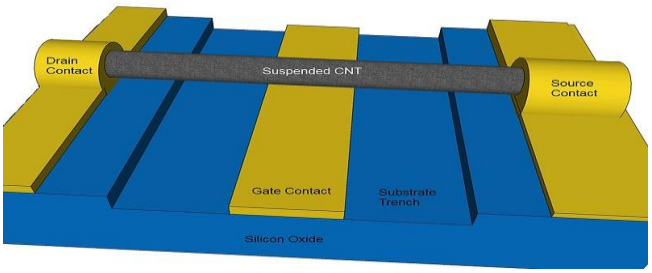


Figure 3.8. Suspended CNTFET structure [116].

The fabrication of suspended CNTFETs can be done in several ways, including growing them over trenches using catalyst particles, moving them to a substrate and then under-etching dielectric beneath and transfer-printing onto a trenched substrate [116].

Disadvantage of suspended CNTFET is that material used as a gate dielectric is air or vacuum. This is only applicable to the short nanotubes and not for longer nanotubes. These suspended CNTFETs are only used for studying the intrinsic properties and cannot be commercially used.

Single-gate CNTFETs are more susceptible to SCEs, including threshold voltage variations and DIBL. These effects can lead to reduced control over the transistor's behaviour and limit its performance at smaller feature sizes. Single-gate CNTFETs suffer from higher gate leakage compared to double-gate CNTFETs. This leakage can result in increased power consumption and reduced energy efficiency. Further, the single-gate structures of CNTFET exhibit a lower ON/OFF current ratio compared to double-gate CNTFETs. So, it’s difficult to turn OFF the single-gate CNTFET completely, leading to increased standby power consumption. These disadvantages of single-gate CNTFET are reduced by using the double-gate structure of CNTFET.

3.6. DG-CNTFET STRUCTURES

DG-CNTFETs have gained significant attention in field of nanoelectronics because of their unique properties and possible advantages over the single gate CNTFET. DG-CNTFETs offer better control over flow of electrons when compared to traditional single-gate CNTFET. This

is because they have two gates (one on top and one on the bottom), allowing for precise modulation of the channel current. Double-gate CNTFET consists of two gates namely top gate and bottom gate for better isolation of drain & gate and source& gate.

The different types of structure of DG-CNTFET have been taken into consideration for performance analysis of DG-CNTFET's structures. Based on doping, various kinds of CNTFETs are

- Schottky-Barrier (SB)DG-CNTFET
- Partially gated (PG) DG-CNTFET
- MOSFET-like (Conventional) DG-CNTFET
- Tunnel DG-CNTFET

3.6.1. Schottky Barrier (SB) DG-CNTFET

Schottky barrier DG-CNTFET is designed by introducing a schottky-barrier at every contact between metal and semiconductor. Source and drain terminals consist of metal and schottky barrier exists between metal and nanotube contact terminals. Therefore, this device is known as schottky barrier DG-CNTFET. Schottky barrier DG-CNTFET involves metal contacts at drain and source side with channel consisting of intrinsic carbon nanotube as shown in figure 3.9.

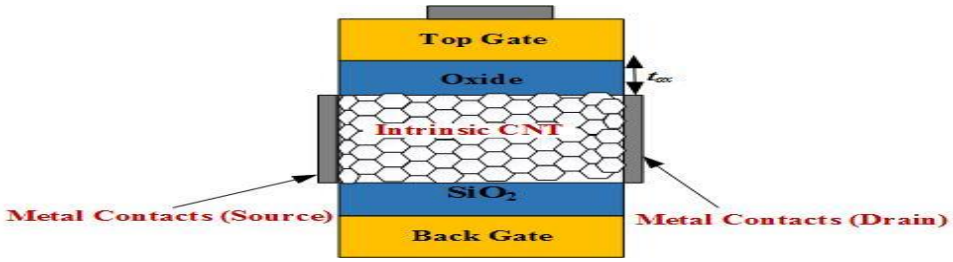


Figure 3.9. Schottky-Barrier DG-CNTFET structure [117].

The working operation of SB-CNTFET involves direct tunneling of electrons and holes at source and channel junction [117]. At the junctions of source and drain, potential barrier occurs and tunneling of electrons as well as from holes contribute to current in device. Voltage at gate terminal controls barrier width and transconductance in device. When gate voltage is less, barrier is large and it limits current from flowing in the channel of device. Further, when gate voltage is increased, height of barrier is decreased which allows flow of current in channel.

As there is no doping in the channel i.e. intrinsic, so there exists ambipolarity in device. Ambipolarity means the current is due to holes and electrons in the device. When positive or higher gate voltage is applied, there is tunneling of electrons from source inducing schottky barrier at source side in conduction band. On applying negative or low gate voltage, tunneling

of holes occur from drain side which induces schottky barrier in valence band [117]. When oxide thickness is decreased and schottky-barrier is zero, ambipolar conduction takes place which increases leakage current in device. Ambipolar conduction reduces SB-CNTFET's performance which can be enhanced by increasing thickness of oxide. Various techniques have been applied to suppress the ambipolarity in schottky barrier CNTFETs. Double gate can be used instead of single gate to overcome the problem of ambipolarity in the CNTFETs.

3.6.2. Partially gated (PG) DG-CNTFET

It consists of uniformly doped channel with ohmic contacts at ends of nanotube as shown in figure 3.10. Device operates in depletion mode when channel is uniformly doped.

Figure 3.10. Partially-gated DG-CNTFET structure [117].

These devices can be *n*-type or *p*-type based on doping material. Applying positive (negative) voltage at the gate electrode, depletes the carriers and turns the device OFF in case of *p*-type (*n*- type) partially gated DG- CNTFET.

3.6.3. MOSFET-like (Conventional) DG-CNTFET

The next kind of CNTFET is MOSFET-like double-gate CNTFET which is also known as conventional DG-CNTFET as it resembles the structure of conventional DG-MOSFET [117]. Structure of conventional DG-CNTFET is given in figure 3.11. The construction of this device consists of silicon that forms substrate of device. Silicon dioxide layer is grown over silicon substrate. A conventional DG-CNTFET is formed by one or more semiconducting CNTs which are well-positioned under gate is intrinsic and source and drain extension regions are *n*-type/*p*-type depending upon type of DG-CNTFET. MOSFET-like DG-CNTFET involves source and drain terminals which are doped heavily instead of metal that were used in SB-DG-CNTFET [117].This type of DG-CNTFET uses highly doped *n*-type or *p*-type drain and source region.

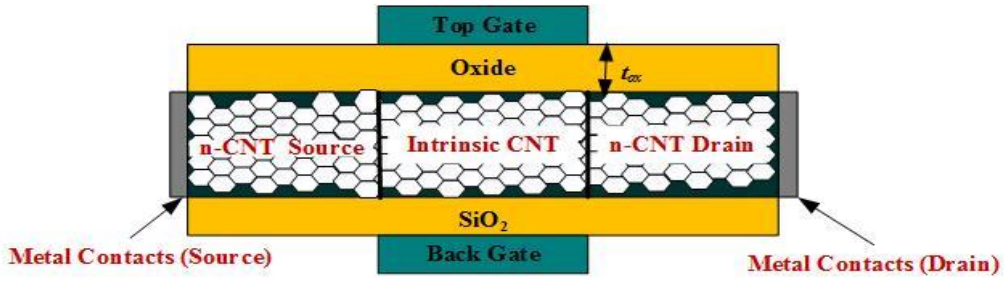


Figure 3.11. MOSFET-like (Conventional) DG-CNTFET structure [117].

As source and drain regions are *n*-type doped and channel is intrinsic, potential barrier occurs for charge carriers to flow from source to drain. This is OFF state. Carriers do not see any barrier in ON state. Gate electrostatics controls the top of the barrier similar to the conventional MOSFET.

Applying positive voltage at gate, barrier decreases and when this applied voltage at gate terminal is greater than threshold voltage, there is a formation of channel between source and drain. At the beginning of channel formation, current flows due to ballistic transport.

3.6.4. Tunnel DG-CNTFET

In a tunnel DG-CNTFET, source and channel's potential barrier is so wide because of band-to-band tunnelling (BTBT) phenomenon that there is reduction in possibility of a carrier to tunnel from source to drain region in an OFF state.

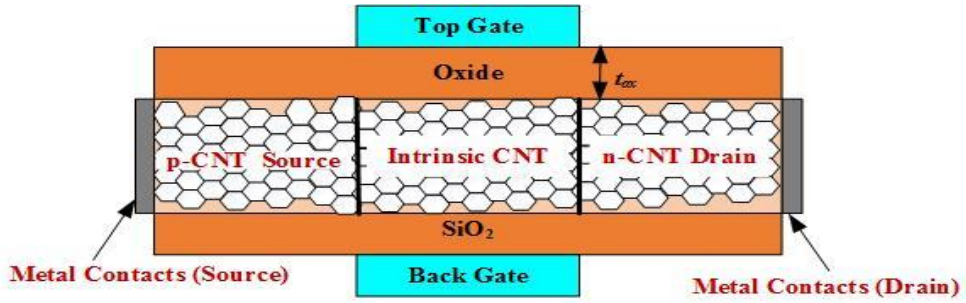


Figure 3.12. Tunnel DG-CNTFET structure [117].

Tunnel DG-CNTFET fabrication is a challenging task as it requires very high thermal budgets. This is due to the fact that one carbon atom removed from tube and replaced using a dopant atom degrades the properties of carbon nanotubes (CNTs). Introducing *n-i-p* or *p-i-n* doping at CNT channel give rise to tunnel DG-CNTFET as shown in figure 3.12. It is based on tunneling behaviour of CNTFET.

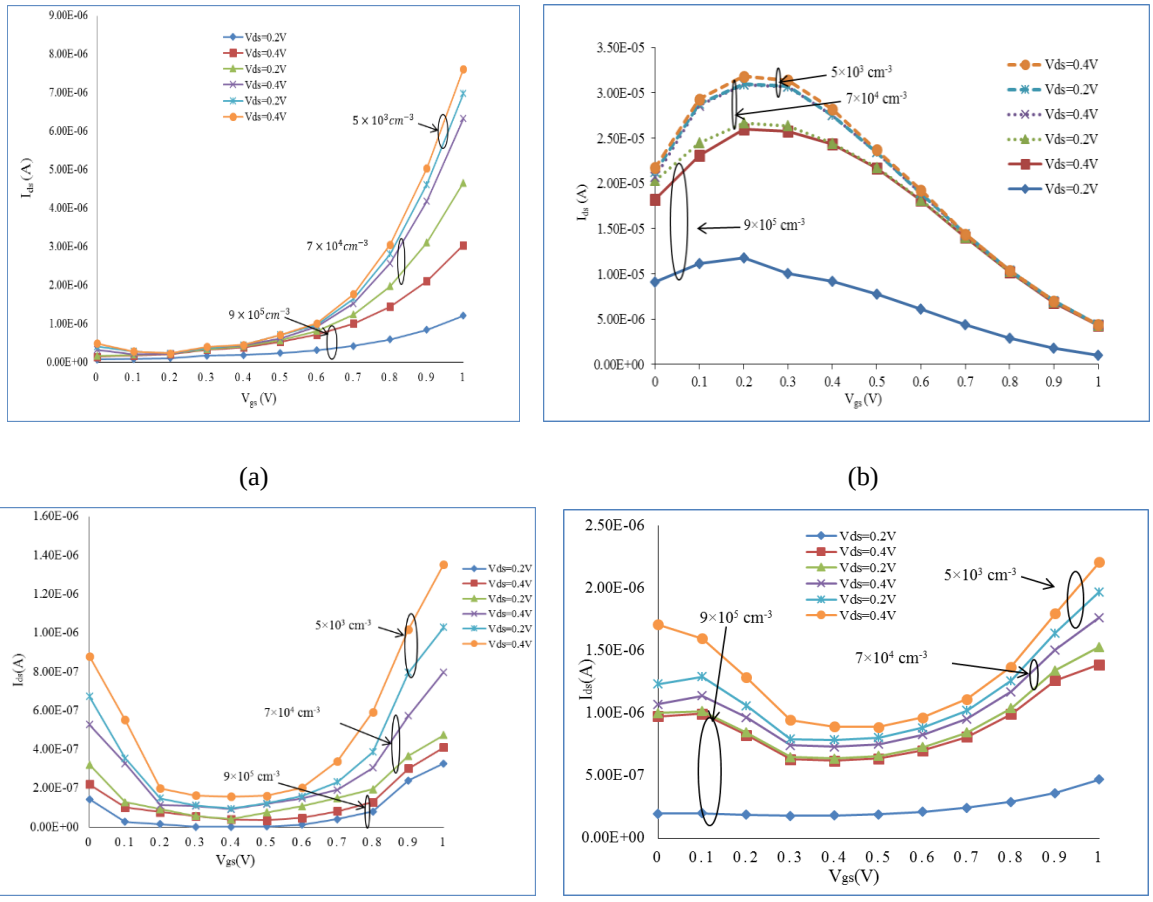
3.7. DEVICE OPTIMIZATION

This section focuses on device optimization using variable doping and process parameter variations of DG-CNTFET. Structure of DG-CNTFET has been optimized with respect to parameters, which are: (1) considering the variable doping and 2) process parameter variations of DG-CNTFET.

Performance of DG-CNTFET structures mentioned in previous section have been analysed for variable doping values and process parameter variation to propose the optimized structure of DG-CNTFET. While optimizing DG-CNTFET structure, the main target is to lower the leakage current i.e., OFF current and to have high value of ON current to get high value of I_{ON}/I_{OFF} ratio by considering device dimensions according to the ITRS 2015.

3.7.1. Optimization based on variable doping in DG-CNTFET

To analyze the impact of doping for the structure optimization, different doping values have been taken and its performance evaluation has been done. The current- voltage curves of DG-CNTFETs at various doping values of 5×10^3, 7×10^4 and 9×10^5 as a molar fraction are shown in figure 3.13. Ratio of doping atoms to total atoms is known as molar fraction [118]. To choose optimum value of doping, variable doping values have been considered so as to optimize the structure of DG-CNTFET. Current voltage characteristics have been simulated for doping values of 5×10^3, 7×10^4 and 9×10^5 at various values of drain to source voltage (V_{ds}) for all four structures of DG-CNTFET using NanoTCAD ViDES tool to analyze the performance of these devices at variable doping values. NanoTCAD ViDES is a device simulator used to compute transport in nanoscale devices. This tool solves self-consistently the 3D Poisson and quantum transport equation within the NEGF formalism. It is found that with doped source/drain regions, leakage current improves as doping fraction decreases from 10^5 to 10^3. Rising doping fraction value increases ON current, which enhances device's ON current to OFF current ratio.



(a) (b)

(c) (d)

Figure 3.13. Doping effect on current –voltage characteristics of (a) Conventional DG-CNTFET (b) Partially-gated DG-CNTFET (c) Schottky-barrier DG-CNTFET (d) Tunnl DG-CNTFET.

Figure 3.13. (a) to (d) shows the doping effect on current voltage (I-V) characteristics of various DG-CNTFET's structures. Current-voltage characteristics for all four structures i.e., Conventional DG-CNTFET, Partially-gated DG-CNTFET, Schottky-barrier DG-CNTFET and Tunnel DG-CNTFET considering variable doping have been plotted.

In CNTFET, increasing the doping level has several effects on its current-voltage (I-V) characteristics such as decrease in leakage current. The doping value to consider in a CNTFET are source and drain doping levels, which can influence behaviour of device.

Figure 3.13. shows that increasing source and drain doping levels for DG-CNTFET can significantly impact drain current by modifying the electrical properties of transistor. Current voltage characteristics of all four structures of DG-CNTFET considering different doping values have been plotted for variable drain to source voltage. Effect of variable doping on conventional DG-CNTFET's I-V characteristics considering different drain to source voltage has been described in figure. 3.13. (a). It is observed that at variable drain to source voltage (V_{ds}), there is an effect of variable doping on current voltage characteristics of conventional DG-CNTFET. Higher doping value of 5×10^3 improve device's current carrying capability leading to higher drain current when gate to source voltage increases at variable V_{ds}. There is an enhancement in the conductivity due to increased charge carriers in channel, allowing for better current flow between source and drain terminals of conventional DG-CNTFET. Current voltage characteristics of partially gated DG-CNTFET considering the variable doping has been shown in figure. 3.13. (b). In figure 3.13. (c), it is shown that I-V characteristics of schottky barrier DG-CNTFET gets affected by variable doping. In schottky barrier DG-CNTFET, doping affects schottky barrier height at metal - CNT interface. Device's height of barrier gets reduced with the increased doping, making the charge carriers to tunnel through the barrier more easily which enhances the current flow in the device. The effect on current voltage characteristics of tunnel DG-CNTFET considering the variable doping and drain to source voltage has been discussed in figure 3.13. (d). The current voltage characteristics of tunnel DG-CNTFET gets affected by variable doping. The characteristics of tunnel DG-CNTFET becomes steeper on increasing doping values and higher current levels are obtained due to enhanced tunneling.

From figure 3.13, it is clear that for decrease in doping value from 9×10^5 to 5×10^3, rise in drain current of device is observed. When doping levels in source and drain for all structures are decreased from 9×10^5 to 5×10^3, the concentration of charge carriers also increases which are available at these terminals and improves the efficiency of carrier injection into the carbon nanotube channel which further increases drain current when transistor in ON state.

Further, reason for increase in drain current in these structures of DG-CNTFET with increase in doping value is that doping reduces contact resistance at interface between source and drain regions and CNT channel. Lower contact resistance allows for more efficient transfer of charge carriers between heavily doped regions and channel which further contributes to increase in drain current in device [119].

Increasing doping in source and drain regions of a CNTFET leads to higher drain current by improving carrier injection and reducing contact resistance in the device [119]. So, higher doping value is required which can acts as optimum value of doping in the DG-CNTFET.

Now, to select the optimum value of doping and the best structure of DG-CNTFET, the ON current for all the four structures at different doping values has been calculated in table 3.1.

Table 3.1. ON current of different structures of DG-CNTFET at variable doping values.

Doping value(cm^{-3}) →	**V_{ds}= 0.2V**	**V_{ds}=0.4V**	**V_{ds}=0.2V**	**V_{ds}=0.4V**	**V_{ds}=0.2**	**V_{ds}=0.4V**
	9×10^5		**7×10^4**		**5×10^3**	
Conventional DG-CNTFET	6.42E-07	6.48E-07	1.21E-06	3.83E-06	1.62E-06	1.67E-06
Partially-gated DG-CNTFET	9.48E-10	1.07E-09	1.05E-06	3.26E-06	2.64E-08	2.62E-08
Schottky-barrier DG-CNTFET	2.30E-07	3.25E-07	3.28E-07	8.37E-08	6.28E-08	3.25E-07
Tunnel DG-CNTFET	3.65E-07	2.87E-07	1.02E-06	2.34E-06	1.58E-08	2.34E-07

Comparison of ON current for four several structures of DG-CNTFET at variable doping in source and drain regions of device at different drain to source voltage values is shown in table 3.1. It can be seen that conventional DG-CNTFET has greater ON current value in comparison to other structures of DG-CNTFET. Further, it is observed that doping level of 5×10^3 gives better performance considering ON current and its value for conventional DG-CNTFET is the highest followed by other three structures of the DG-CNTFET.

Doping in DG-CNTFET lowers the resistance, a higher current can flow through the material for a given voltage. Further, it also modifies the energy barriers that charge carriers must overcome to move through the material. Lowering these barriers makes it easier for charge carriers to move, resulting in increased drain current.

In conventional DG- CNTFETs, gate electrode has more channel control, leading to efficient modulation of the channel's conductivity. In partially gated DG- CNTFETs, only a portion of the nanotube is gated, which can result in less effective control over the entire channel. In tunnel DG-CNTFETs, the operation is based on quantum tunneling, which limits the ON

current. Schottky barrier DG- CNTFETs have a built-in schottky barrier that can hinder the flow of current.

When doping levels are relatively high, performance of DG-CNTFET degrades. The reason, why device performance, degrades with relatively doping with high values of order of 10^2 is that barrier height and conduction band tunnel barrier length have been significantly reduced. Direct source-to-drain (intraband) tunnelling is dominated for leakage current [120]. As a result, ON current to OFF current ratio is drastically decreased. Considering entire gate voltage range, for high doping values, electron current dominates leakage current.

When doping of 7×10^4 is decreased to 5×10^3 in source and drain regions, intraband tunneling component of leakage current is increased by a small modulation of tunnel barrier width. However, current's interband tunneling component is simultaneously decreased. Overall leakage current is reduced and ON current to OFF current ratio increases. IBM experimental group and Bockrath [120] demonstrated that optimal doping level is 10^{-3} dopants per carbon atom.

So, optimum doping value of 5×10^3 and conventional DG-CNTFET has been selected for proposed optimized structure which is named as conventional *n*-type DG-CNTFET on the basis of doping by plotting I-V characteristics of DG-CNTFET structures to analyze device performance.

3.7.2. Optimization based on diameter and process parameter variations of DG-CNTFET

Now, next part is to optimize device based on diameter and process parameter variations for proposed structure of DG-CNTFET. For this, different device dimensions (diameter and channel length variations) have been taken into considerations and best results are achieved in terms of device performance. DG-CNTFET's current voltage characteristics for four kinds of structures are achieved using nano-TCAD ViDES.

Diameter of carbon nanotube that is used as CNTFET channel is one of most significant parameters. Diameter of carbon nanotubes used in CNTFETs can significantly impact their electronic properties. Diameter of CNT in CNTFET is similar to silicon thickness as in case of conventional MOSFETs. Bandgap in case of carbon nanotube varies inversely with CNT diameter whereas the bandgap is constant in silicon used as the channel in MOSFET. So, OFF current and ON current are directly affected by diameter of carbon nanotube. Generally, for the optimization of CNTFETs, the diameter of carbon nanotubes fall within the range of few nanometres to tens of nanometres [121]. The diameter of semiconducting SWCNTs is 1 *nm* –

2 *nm* [122]. Therefore, proper selection of diameter of carbon nanotube ensures proper OFF state and ON current to OFF current ratio. Extensive simulations at various diameters were performed to make the selection and three sets of diameters, i.e., 1 *nm*, 1.25 *nm* and 1.5 *nm*, have been selected which ensures best OFF state of the DG-CNTFET for all the four structures. Channel length and diameter variation impact on I_{ds}-V_{gs} characteristics of all four structures of DG-CNTFET have been discussed in figure 3.14.

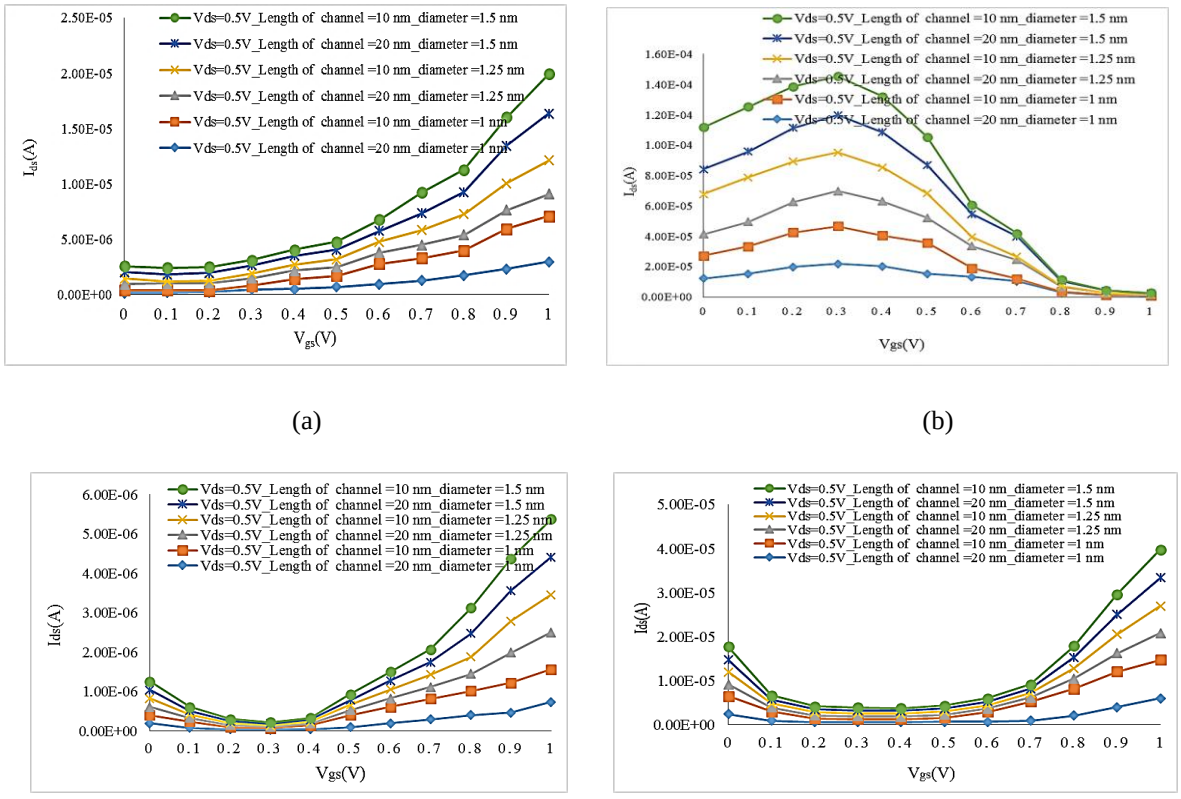


Figure. 3.14. The effect of diameter variation and process parameter variation on I_{ds}-V_{gs} characteristics of (a) proposed conventional *n*-type DG-CNTFET (b) Partially-gated DG-CNTFET(c) Schottky-barrier DG-CNTFET (d) Tunnel DG-CNTFET.

Current-voltage characteristics of (a) proposed conventional *n*-type DG-CNTFET (b) Partially-gated DG-CNTFET(c) Schottky-barrier DG-CNTFET (d) Tunnel DG-CNTFET by variation in diameters of carbon nanotube and channel length have been shown in figure 3.14. The diameter of carbon nanotube directly impacts various aspects of DG-CNTFET's I-V characteristics at various channel length.

It is shown from the figure 3.14. (a) that CNT diameter and process parameter variation i.e., channel length, affects current voltage characteristics of proposed conventional *n*-type DG-CNTFET. Increasing the diameter from 1 *nm* to 1.5 *nm*, allows for more current carrying

capacity as there is more space for charge carriers to flow, which leads to high value for drain current at a given V_{ds}. Longer channel length i.e., 20 *nm*, of device, results in higher resistance in carbon nanotube channel which reduces drain current of proposed conventional *n*-type DG-CNTFET. Figure 3.14. (b) shows effect of variable diameter and length of channel on I_{ds}-V_{gs} characteristics of partially gated DG-CNTFET. Increase in diameter and reducing the channel length of schottky-barrier DG-CNTFET leads to improvement in current voltage characteristics of schottky barrier DG-CNTFET as described in figure. 3.14 (c). The larger diameter of carbon nanotube enhances current carrying capacity, while shorter channel length improves the current density and switching speed of schottky barrier DG-CNTFET. Figure 3.14 (d) shows the effect of variable diameter and channel length on I-V characteristics of tunnel DG-CNTFET. Smaller diameter of carbon nanotubes (1 *nm*) tends to have a larger bandgap which require higher threshold voltage for conduction. Higher diameter of carbon nanotube (1.5 *nm*), with a smaller bandgap, require a lower threshold voltage for DG-CNTFET [123]. Therefore, the choice of CNT diameter directly influences DG-CNTFET's threshold voltage which affects ON current, OFF current and ON current to OFF current ratio.

It is clear from results that scaling channel length i.e., 10 *nm* affects the current-voltage characteristics of all DG-CNTFET structures. It is shown from figure that as channel length of DG-CNTFET decreases, there is rise in drain current with increase in applied gate to source voltage. When channel length of device is decreased, it allows for faster carrier transport across channel, resulting in a higher drain current. Further, decreasing channel length of device from 20 *nm* to 10 *nm*, channel between source and drain terminals becomes shorter that decreases resistance of channel in the device. Also, in CNTFETs, quantum mechanical effects become significant. These effects can enhance electron transport and result in an increase in drain current.

Table 3.2. Comparison of ON current for different structures at V_{ds} =0.5V at variable diameter and channel length of DG-CNTFET.

Type of DG-CNTFET	**ON current at channel Length=20nm**			**ON current at channel length =10nm**		
	d=1*nm*	**d=1.25*nm***	**d=1.5*nm***	**d=1*nm***	**d=1.25*nm***	**d=1.5*nm***
Proposed Conventional *n*-type DG-CNTFET	1.91E-05	2.50E-05	2.92E-05	1.95E-05	2.97E-05	3.12E-05
Partially-gated DG-CNTFET	1.47E-06	4.58E-06	4.69E-06	1.45E-05	4.87E-05	5.74E-05
Schottky-barrier DG-CNTFET	2.04E-05	2.68E-06	3.78E-06	2.09E-05	2.98E-05	3.08E-06
Tunnel DG-CNTFET	8.94E-06	9.33E-06	9.83E-06	9.08E-05	1.25E-05	2.47E-05

Table 3.2. describes the comparison of ON current for different structures of DG-CNTFET at V_{ds} =0.5V considering the variable diameter and process parameter variation. The diameter =1.5 *nm* and channel length =10 *nm* of proposed conventional *n*-type DG-CNTFET contribute to increased ON current by enhancing the conductivity of the CNT channel and improving the overall performance as compared to other structures of DG-CNTFET. The reason for this is that channel length = 10 *nm* results in faster transit times for the carriers, allowing the transistor to switch ON and OFF more quickly than the channel length of 20*nm*. This rapid switching capability is desirable for high-speed electronic devices. Also, the channel length =10 *nm* allows for better electrostatic channel control by gate electrode. CNTs with diameter=1.5 *nm* provides more conductive pathway for electrons to flow. As diameter rises from 1 *nm* to 1.5 *nm*, there is more surface area for carrier to move, leading to a higher ON current [123].

In proposed conventional *n*-type DG-CNTFET, ON current is affected by efficient gate control which increases the ON current as compared to other structures when diameter rises from 1 *nm* to 1.5 *nm*. Schottky barrier height affects the electron injection efficiency in schottky barrier DG-CNTFET so ON current is less as compared to conventional DG-CNTFET. Also, the partially gated DG-CNTFET has less ON current than the tunnel DG-CNTFET and conventional DG-CNTFET. Considering channel lengths, i.e. 20 *nm* and 10 *nm*, the ON current for all the four structures of DG-CNTFET is more at 10 *nm* channel length as compared to ON current at channel length of 20 *nm*. ON current at diameter = 1.5 *nm* for all structures of DG-CNTFET is more in comparison to ON current at diameter = 1 *nm.* To get I_{ON}/I_{OFF} ratio, study of OFF current is necessary for all four structures of DG-CNTFET as the main target while optimizing the device is to get high value of ON to OFF current ratio and lower leakage current i.e., OFF current.

Table 3.3. Comparison of OFF current for different structures at V_{ds} =0.5*V* at variable diameter and channel length of DG-CNTFET.

Type of DG-CNTFET	**OFF current at channel length=20*nm***			**OFF current at channel length=10*nm***		
	d=1*nm*	**d=1.25*nm***	**d=1.5*nm***	**d=1*nm***	**d=1.25*nm***	**d=1.5*nm***
Proposed Conventional *n*-type DG-CNTFET	1.28E-10	2.42E-08	2.87E-07	2.15E-11	4.21E-09	5.78E-08
Partially-gated DG-CNTFET	9.85E-08	1.25E-07	3.64E-07	9.56E-08	5.24E-08	6.25E-07
Schottky-barrier DG-CNTFET	5.78E-08	6.24E-08	6.42E-08	8.75E-08	6.54E-08	7.98E-07
Tunnel DG-CNTFET	9.76E-07	4.78E-08	5.84E-08	1.00E-08	5.21E-09	8.52E-08

The comparison of OFF current for different structures of DG-CNTFET at V_{ds} =0.5V considering the different channel lengths and diameters has been shown in table 3.3. It is clear from results that scaling of channel length directly affects I_{OFF} considering channel length =10 *nm*. Reason for decrease in OFF current of proposed conventional *n*-type DG-CNTFET at channel length 10 *nm* is that it corresponds to a shorter path for charge carriers to travel between source and drain those results in lower resistance in channel, allowing charge carriers to move more easily, thereby decreasing the OFF current than the other four structures of the DG-CNTFET. The proposed conventional *n*-type DG-CNTFET structure with channel length=10 *nm* leads to improved electrostatic control, reduced leakage paths, and decreased tunneling probabilities, all of which contribute to a decrease in the OFF current. The gate can more effectively modulate the flow of charge carriers at shorter channel length, reducing the OFF current. At diameter=1 *nm* of carbon nanotube often have a larger bandgap, that makes carriers more difficult to move across the nanotube [123]. This increased bandgap in smaller diameter of carbon nanotube (d=1 *nm*) can reduce the OFF current. The enhanced electrostatic control provided by gates in proposed conventional n-type DG-CNTFET helps in reducing OFF current by suppressing leakage paths. While other three structures come with specific challenges such as schottky barrier imperfections and tunneling processes, which can lead to comparatively higher OFF current values in partially gated, schottky barrier and tunneling DG-CNTFET.

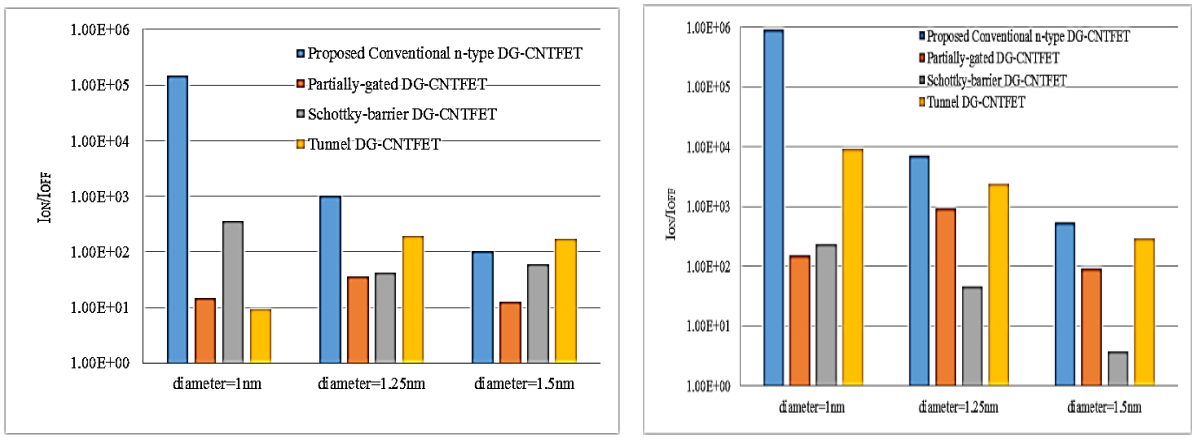
Table 3.4. ON current to OFF current ratio comparison for different structures at V_{ds} =0.5*V* at variable diameter and channel length of DG-CNTFET.

Type of DG-CNTFET	**ON current to OFF current ratio at channel length=20nm**			**ON current to OFF current ratio at channel length=10nm**		
	d=1*nm*	**d=1.25*nm***	**d=1.5*nm***	**d=1*nm***	**d=1.25*nm***	**d=1.5*nm***
Proposed Conventional *n*-type DG-CNTFET	1.49E+05	1.03E+03	1.02E+02	9.07E+05	7.05E+03	5.40E+02
Partially-gated DG-CNTFET	1.49E+01	3.66E+01	1.29E+01	1.52E+02	9.29E+02	9.18E+01
Schottky-barrier DG-CNTFET	3.53E+02	4.29E+01	5.89E+01	2.39E+02	4.56E+01	3.86E+00
Tunnel DG-CNTFET	9.16E+00	1.96E+02	1.68E+02	9.08E+03	2.40E+03	2.90E+02

ON current to OFF current ratio comparison for different structures of DG-CNTFET at V_{ds} = 0.5V considering variable channel lengths and diameters is described in table 3.4. It is clear from table that proposed conventional *n*-type DG-CNTFET has greater ON current to OFF

current ratio as compared to other three structures of the DG-CNTFET at channel length =10 *nm*. For smaller diameter (1 *nm*) CNTs, quantum confinement effects become more significant. When the diameter is small (1 *nm*), the electronic states in the CNT become quantized, leading to discrete energy levels. This quantization can enhance the control over the flow of current, resulting in better ON-OFF switching behaviour. Large diameter (1.5 *nm*) CNTs generally exhibit higher OFF current. OFF current is current that flows through transistor when it is in OFF state. Due to quantum confinement effects and the wider bandgap associated with larger diameter (1.5 *nm*) CNTs, the OFF current increases, leading to low ON current to OFF current ratio [123].

Proposed conventional *n*-type DG-CNTFETs have a large value of ON current to OFF current ratio due to symmetric gate, allowing for effective control of current flow between source and drain at channel length=10 *nm* as compared to ON current to OFF current ratio at channel length =20 *nm*. The partially gated DG-CNTFETs have lower ON current to OFF current ratio value as compared to proposed conventional *n*-type DG-CNTFETs due to partial gate leading to variation in device performance. The schottky barrier DG-CNTFETs have low ON current to OFF current ratio as compared to conventional and tunnel DG-CNTFETs because of energy barriers at metal semiconductor junction, which cause rise in leakage current when device is in OFF state.



(a) (b)

Figure. 3.15. Diameter variations on ON current to OFF current ratio at (a) channel length =20*nm* and (b) channel length =10*nm* of different structures of DG-CNTFET.

ON current to OFF current ratio of different structures of DG-CNTFET considering the different channel length and variable diameter is shown in figure 3.15. Figure. 3.15. (a) describes that for diameter=1 *nm*, ON current to OFF current ratio of proposed conventional *n*-type DG-CNTFET at channel length 20 *nm* is more as compared to I_{ON}/I_{OFF} ratio at diameter

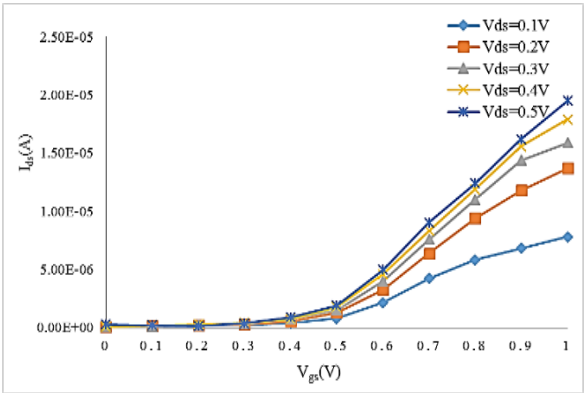
value of 1.25 *nm* and 1.5 *nm*. The I_{ON}/I_{OFF} ratio of schottky-barrier DG-CNTFET is more followed by partially-gated DG-CNTFET and tunnel DG-CNTFET at diameter =1 *nm*. Figure. 3.15. (b) shows the I_{ON}/I_{OFF} ratio of all four structures of DG-CNTFET at channel length =10 *nm*. It is described from figure that at channel length of 10*nm*, proposed conventional *n*-type DG-CNTFET shows higher I_{ON}/I_{OFF} ratio as compared to other three structures of DG-CNTFET. At shorter channel length of 10 *nm*, quantum mechanical effects become more significant as compared to channel length of 20 *nm*. These effects can lead to improved confinement of charge carriers within channel that results in better control of current flow and a high value of ON current to OFF current ratio at lesser channel length of 10 *nm* is obtained. Further, as diameter of carbon nanotube increases from 1 *nm* to 1.5 *nm*, the ON current to OFF current ratio decreases for proposed conventional *n*-type DG-CNTFET. The bandgap of a CNT decreases as its diameter increases from 1 *nm* to 1.5 *nm*. A smaller bandgap means that electrons require less energy to move from valence band to conduction band, making it easier for electrons to flow even when transistor is in OFF state. This increased current in OFF state reduces ON current to OFF current ratio when diameter rises from 1 *nm* to 1.5 *nm*. Differences in ON current to OFF current ratios among these different types of DG-CNTFET can be attributed to presence of additional barriers which include schottky barriers in schottky barrier DG-CNTFET and tunneling barriers in tunnel DG-CNTFET and non-uniform gating configurations in partially gated DG-CNTFET, which impact the control of current flow through the carbon nanotube channel.

Based on performance analysis, optimized conventional *n*-type DG-CNTFET designs for diameter=1 *nm* (13, 0), diameter=1.25 *nm* (16, 0) and diameter=1.5 *nm* (19, 0) for channel length =10 *nm* is proposed for low power applications. It was observed that for diameter = 1*nm*, for chirality (13, 0), the I_{OFF} is small due to high bandgap. Compared to diameter=1 *nm*, carbon nanotube with diameter=1.25 *nm* has large value of OFF current and higher value of ON current. Carbon nanotube with diameter=1.5 *nm* has much higher OFF current and higher ON current but has less value of ON current to OFF current ratio when compared to diameter =1 *nm* and 1.25 *nm*. As diameter of carbon nanotube increases from 1 *nm* to 1.5 *nm*, both ON current and OFF current rise but OFF current rises more rapidly as compared to ON current. There is an increase of 4.35% and 3.34% in ON current and OFF current as diameter of carbon nanotube rises from 1*nm* to 1.5*nm* on decreasing channel length value from 20 *nm* to 10 *nm*. Further, there is a decrease of 2.46% in ON current to OFF current ratio as diameter of carbon nanotube increases from 1*nm* to 1.5*nm* and length of channel changes from 20 *nm* to 10 *nm*.

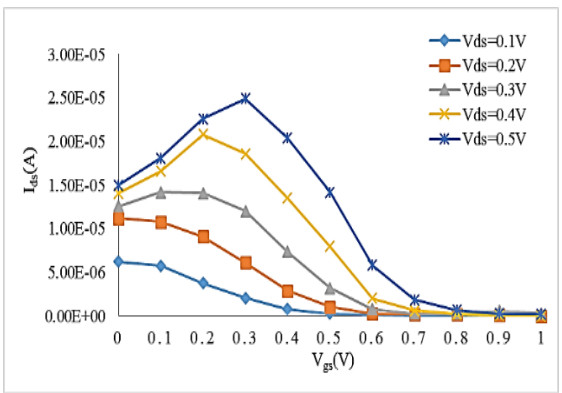
Diameter selection for semiconducting SWCNTs below 1 *nm* is less suitable as it involves complex fabrication processes [124]. Also, decreasing the channel length also improves the switching speed of the CNTFET. This means that the transistor can switch between it's ON and OFF states more quickly, which is essential for high-speed electronic devices. When length of channel becomes smaller, particularly below 10 *nm*, various challenges and limitations arise, making it less recommended for practical fabrication [124]. The fabrication process for CNTFETs, especially at extremely small scales, can lead to a high degree of variability in the device properties. Variability between individual devices of CNTFET can make it difficult to maintain consistent and reliable performance, which is crucial for practical applications [124]. Selection of channel length below 5 *nm* is not suitable for optimization as fringing fields from gate occurs and device can still be turned ON. Also, device performance degrades below channel length of 5 *nm* [124]. Drain current is only reduced when overall length is below a critical value. So, optimum value of channel length and diameter are 10 *nm* and 1 *nm* respectively. Hence, it is concluded from results that proposed parameters may be used in conventional *n*-type DG-CNTFET device applications for better overall performance.

3.7.3. Analysis of DG-CNTFET at variable drain to source voltage

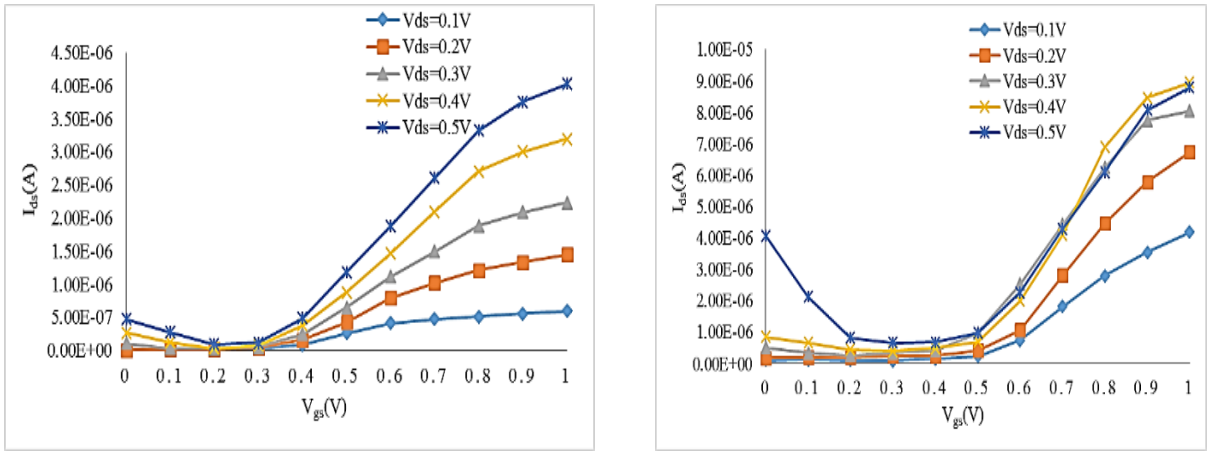
To analyze effect of variable drain to source voltage, all four structures of DG-CNTFET are simulated for (13, 0) CNT with t_{ox} = 1 *nm*, $L_G = L_S = L_D$ = 10 *nm*, diameter =1 *nm* and channel length =10 *nm*. These dimensions are in accordance with the ITRS 2015. The length of gate, source and drain used are L_G=L_S=L_D to keep the symmetry of the device maintained. These dimensions were used to obtain current voltage characteristics for channel length of 10 *nm* at variable drain to source voltage V_{ds}. For both *p*-type and *n*-type regions, doping values of 5×10^3 as a molar fraction [118] were utilised. The semiconducting zigzag CNTs with (*n*,0) have been used for double gate planar geometry. Current voltage characteristics for all four DG-CNTFET structures have been obtained using the NanoTCAD ViDES.



(a)



(b)



(c) (d)

Figure 3.16. Current-voltage characteristics for different structures of (a) proposed conventional *n*-type DG-CNTFET (b) Partially-gated DG-CNTFET (c) Schottky-barrier DG-CNTFET (d) Tunnel DG-CNTFET for channel length=10*nm* at diameter=1*nm* at variable V_{ds}.

The current-voltage characteristics of different structures of DG-CNTFETs at channel length=10 *nm* and diameter=1 *nm* for variable V_{ds} have been described in figure. 3.16. The simulated results of proposed conventional *n*-type DG-CNTFET in figure 3.16 (a) show that the characteristics are significantly enhanced when doping is added to CNT source and drain sides on increasing drain to source voltage. As charge develops inside the channel, gate bias has a direct impact on how gate controls the current flow.

The I_{ds} vs V_{gs} characteristics for a partially- gated CNTFET with a uniformly doped (*p*-type) CNT channel is shown in figure 3.16. (b). Because CNT has been uniformly doped throughout channel, this device operates in depletion mode. Because of ohmic contacts, device's properties are better than those of an intrinsic channel. For negative gate bias, holes will repel from channel, turning OFF the *p*-type device. This occurs very late than the expected values as carbon nanotubes are generally *p*-type devices [117]. Varying V_{ds} from 0.1V to 0.5V, in a partially gated DG-CNTFET can impact drain current to voltage characteristics by affecting the transition between saturation and linear regions, introducing output conductance effects and modulating the threshold voltage of DG-CNTFET.

Due to schottky-barrier in schottky barrier DG-CNTFET, drain to source voltage has a significant effect on current voltage characteristics of device and CNT in this case shows ambipolar effect. Figure 3.16. (c) describes that devices that operate in subthreshold range (V_{ds}= 0.1*V*) operate *n*-type when gate voltage is increased. But as it operates in a saturation region, threshold voltage is significantly larger than subthreshold region, and it is continuously varying as V_{ds} rises. Figure 3.16. (d) describes the current- voltage characteristics of tunnel DG-CNTFET in which there is band to band tunneling that occurs in device. Due to different device

physics involved in all four structures of DG-CNTFET, I-V characteristics are different from the proposed conventional *n*-type DG-CNTFET.

As we see from the figure 3.16. that on increasing gate voltage, there is rise in drain current of device at variable drain to source voltage for all four structures of DG-CNTFET. Increasing V_{ds} from 0.1V to 0.5V, enhances the switching speed of DG-CNTFET by reducing the transition times between the ON and OFF states. This effect can be advantageous in digital applications where fast switching is necessary. Further, increasing the V_{ds} from 0.1V to 0.5V, affects the ability of transistor to control the current flow which can impact device performance in certain applications.

Further, to analyze the four structures of DG-CNTFET at variable V_{ds}, various performance parameters namely ON current, OFF current and ON current to OFF current ratio are analysed to choose the best structure out of the four structures available for DG-CNTFETs.

The performance of all structures of DG-CNTFET considering ON current, OFF current and ON current to OFF current ratio is presented in table 3.5., 3.6. and 3.7. for channel length =10 *nm* and diameter = 1 *nm* at variable $V_{ds.}$

Table 3.5. ON current of different structures of DG-CNTFET at different values of $V_{ds.}$for channel length=10*nm* at diameter= 1*nm*.

V_{ds} (V)	**Proposed Conventional *n*-type DG-CNTFET I_{ON} (A)**	**Partially-gated DG-CNTFET I_{ON} (A)**	**Schottky-barrier DG-CNTFET I_{ON} (A)**	**Tunnel DG-CNTFET I_{ON} (A)**
0.1	1.31E-05	1.09E-06	3.49E-06	1.10E-06
0.2	1.39E-05	2.04E-06	6.56E-06	1.76E-06
0.3	1.59E-05	2.14E-06	9.90E-06	5.08E-06
0.4	1.79E-05	3.98E-05	1.57E-05	8.54E-06
0.5	1.95E-05	1.45E-05	2.09E-05	9.08E-06

Table 3.5. describes the ON current for different DG-CNTFET's structures. It is seen from table that proposed conventional *n*-type DG-CNTFET has higher ON current than the other structures of DG-CNTFET at channel length=10 *nm* and diameter=1 *nm*. As the V_{ds} increases from 0.1V to 0.5V, the energy barrier reduces so that the charge carriers can overcome barrier to move from source to drain. Also, increasing V_{ds} from 0.1V to 0.5V leads to decrease in channel resistance which allows for easier flow of charge carriers, resulting in higher ON current.

The I_{ON} of proposed conventional *n*-type DG-CNTFET is high because of doping concentration at source and drain sides. For conventional DG-CNTFET, entire carbon nanotube serves as the conducting channel. This design allows for a more charge carriers to flow through channel, further increasing ON current compared to other designs where only a portion of the nanotube

may be used. The ON current in proposed conventional *n*-type DG-CNTFETs is relatively high as compared to other four structures because there are no additional barriers or interfaces between source/drain and channel, allowing for efficient charge carrier transport.

The schottky barrier DG-CNTFETs have a metal-semiconductor junction at the source or drain, which forms a schottky barrier. This barrier can hinder the flow of charge carriers, reducing the ON current compared to proposed conventional *n*-type DG-CNTFET. The schottky barrier introduces an energy barrier that carriers must overcome, leading to a decrease in ON current in schottky barrier DG-CNTFET.

In partially gated DG-CNTFET, partial gating can limit the effective channel length, reducing the overall current flow which decreases the ON current as compared to proposed conventional n-type DG-CNTFETs. The efficiency of gate plays a crucial role in calculating ON current in partially gated DG-CNTFETs [117].

The tunnel DG-CNTFET utilizes quantum tunneling phenomena for charge transport. These transistors have an ultrathin gate dielectric, allowing electrons to tunnel through barrier between source and drain. Tunneling barrier in tunnel DG-CNTFET also limits the ON current.

Table 3.6. OFF current of different structures of DG-CNTFET at different values of V_{ds} for channel length=10*nm* at diameter=1*nm*.

V_{ds} (V)	**Proposed Conventional *n*-type DG-CNTFET I_{OFF}(A)**	**Partially-gated DG-CNTFET I_{OFF}(A)**	**Schottky-barrier DG-CNTFET I_{OFF}(A)**	**Tunnel DG-CNTFET I_{OFF}(A)**
0.1	1.75E-10	9.98E-08	7.79E-09	9.15E-08
0.2	3.02E-11	9.83E-08	8.46E-09	5.90E-09
0.3	1.10E-11	3.26E-08	6.56E-09	9.71E-08
0.4	2.40E-11	8.59E-08	8.19E-09	9.94E-08
0.5	2.15E-11	9.56E-08	8.75E-08	1.00E-08

Table 3.6. describes the OFF current for different structures of DG-CNTFET for channel length=10 *nm* at diameter=1 *nm*. The OFF current in a CNTFET is desired to be as low as possible to ensure efficient switching and minimize consumption of power. It is clear from table that proposed conventional *n*-type DG-CNTFET has much less OFF current than the other structures of DG-CNTFET. OFF current of device describes leakage current of device. Low OFF current in DG-CNTFET determines low leakage current that flows from source to drain when transistor is OFF. Due to device's enhancement mode in proposed conventional n-type DG-CNTFET, I_{OFF} is significantly lower than others.

Further, in schottky barrier DG-CNTFETs, schottky barrier arises at source and CNT interface that introduces a barrier to the flow of carriers. When the schottky barrier is formed, it can

result in a higher value of OFF current in comparison with a proposed conventional *n*-type DG-CNTFET. This is because there is a current flow through schottky barrier even when gate voltage is not applied [117].

Although, tunnel DG-CNTFETs offer very steep switching characteristics, they have higher OFF currents due to inherent tunneling process. Electrons can tunnel through barrier even when gate voltage is OFF which increases leakage current in device.

The OFF current of proposed conventional *n*-type DG-CNTFET is less for all the values of V_{ds} that varies from 0.1V to 0.5V as compared to the other structures of DG-CNTFET. The OFF current in these different DG-CNTFET structures varies due to the specific mechanisms, such as electrostatic control, schottky barriers, partially-gated regions and quantum tunneling. The proposed conventional *n*-type DG-CNTFET offers better control over the channel, leading to lower OFF currents compared to schottky barrier, partially-gated, and tunnel DG-CNTFETs [117].

Table 3.7. ON current to OFF current ratio of different structures of DG-CNTFET at different V_{ds} for channel length=10*nm* at diameter=1*nm*.

V_{ds} (V)	Proposed Conventional *n*-type DG-CNTFET I_{ON}/I_{OFF}	Partially-gated DG-CNTFET I_{ON}/I_{OFF}	Schottky-barrier DG-CNTFET I_{ON}/I_{OFF}	Tunnel DG-CNTFET I_{ON}/I_{OFF}
0.1	7.49E+04	1.09E+01	4.49E+02	1.20E+02
0.2	4.60E+05	2.08E+01	7.75E+02	2.98E+02
0.3	1.45E+05	6.56E+01	1.51E+03	5.23E+01
0.4	7.46E+05	4.63E+02	1.92E+03	8.59E+01
0.5	9.07E+05	1.52E+02	2.39E+02	9.08E+03

From table 3.7. it is clear that proposed conventional *n*-type DG-CNTFET has greater value of ON current to OFF current ratio than other structures of DG-CNTFET. High value of ON current to OFF current ratio of DG-CNTFET can be utilized in digital applications.

High value of ON current to OFF current ratio results in greater value of transconductance of the proposed conventional *n*-type DG-CNTFET. The transconductance of a CNTFET measures how effectively the gate voltage controls the current flow, can also increase with a shorter channel length which can be used for amplification and signal processing applications. I_{ON}/I_{OFF} is figure of merit for having better performance (more I_{ON}) and low leakage current (less I_{OFF}) for DG-CNTFET. Better gate control in proposed conventional *n*-type DG-CNTFET leads to more I_{ON}/I_{OFF}. The higher I_{ON}/I_{OFF} ratio in proposed conventional *n*-type DG-CNTFET compared to schottky barrier, partially gated, and tunnel DG-CNTFETs is primarily due to

their symmetric gating, absence of significant energy barriers and reduced leakage currents in the OFF state. These factors collectively contribute to more effective switching characteristics and high value of ON current to OFF current ratio.

So, proposed conventional *n*-type DG-CNTFET gives best performance considering ON current, OFF current and ON current to OFF current at channel length = 10 *nm* in comparison with partially-gated DG-CNTFET, schottky-barrier DG-CNTFET and tunnel DG-CNTFET. Hence, conventional *n*-type DG-CNTFET is proposed structure for this work.

3.8. COMPARISON OF OPTIMIZED STRUCTURE WITH EXISITING LITERATURE

To compare the performance of proposed optimized DG-CNTFET with conventional DG-CNTFET available in the literature, a comparative analysis is performed.

Table 3.8. Comparison of different structures of DG-CNTFET at V_{ds} =0.5V with the existing literature.

Type of DG-CNTFET	I_{ON}(A)	I_{OFF}(A)	I_{ON}/ I_{OFF}
Proposed Conventional *n*-type DG-CNTFET	1.95E-05	2.15E-11	9.07E+05
Conventional DG-CNTFET [117]	1.41E-05	4.06E-10	3.4E+04
Schottky-barrier DG-CNTFET [117]	3.26E-06	2.31E-08	1.41E+02

The comparison of different structures of DG-CNTFET at V_{ds} =0.5V with the existing paper in literature is shown in table 3.8. It is shown in results that results follow a similar trend with existing results in literature. ON current of proposed conventional *n*-type DG-CNTFET is high as compared to existing structures of conventional DG-CNTFET and schottky barrier DG-CNTFET in literature. The OFF current of proposed conventional *n*-type DG-CNTFET is less in comparison with other DG-CNTFET structures available in literature. Further, ON current to OFF current ratio is more for proposed *n*-type conventional DG-CNTFET.

Due to higher OFF (leakage) current of schottky-barrier and conventional structure available in literature, conventional *n*-type DG-CNTFET is proposed as our concern is to reduce the SCEs namely leakage current and threshold voltage fluctuations. Proposed conventional *n*-type DG-CNTFET gives better performance in comparison to other structures of DG-CNTFET in all aspects available in existing literature. Due to ambipolarity issue in case of schottky barrier DG-CNTFET, we are proposing conventional *n*-type DG-CNTFET for this work.

The doping is introduced in device at source and drain regions and intrinsic CNT is used as a channel in proposed conventional *n*-type DG-CNTFET which is analyzed for applications that consumes low power. Also, evaluation is done for a variety of parameters i.e., variable doping, diameter and process parameter variations such as channel length length to propose the optimized low power conventional *n*-type DG-CNTFET design. The performance analysis

shows that CNT diameter and channel length affects OFF current directly and variable doping affects ON current, resulting in high ON current to OFF current ratio value. Further, proposed conventional *n*-type DG-CNTFET has been compared with the existing structures in literature. Proposed conventional *n*-type DG-CNTFET has shown better results over other four device structures considering ON current, OFF current and ON current to OFF current ratio. Simulation results show that proposed conventional *n*-type DG-CNTFETs with diameter=1 *nm*, channel length =10 *nm* and doping value=5×10^3 as molar fraction are best candidates for low power applications. Various simulations for different process parameter variations such as channel length examined that proposed conventional *n*-type DG-CNTFETs are more immune to process variations.

3.9. COMPARISON OF PROPOSED CONVENTIONAL N-TYPE DG-CNTFET WITH DG-MOSFET

The optimized structure of conventional *n*-type DG-CNTFET has been proposed due to its various advantages over the SB- DG-CNTFET, PG- DG-CNTFET and tunnel DG-CNTFET. Further, proposed structure of conventional *n*-type DG-CNTFET has been compared with the DG-MOSFET which is existing structure in literature.

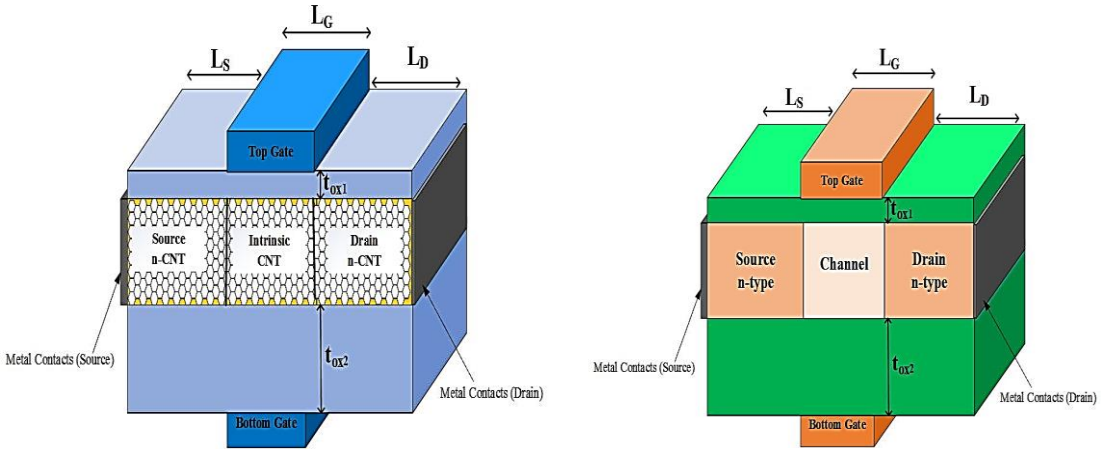


Figure 3.17. (a) Optimized structure of proposed conventional *n*-type DG-CNTFET (b) Structure of DG-MOSFET.

The proposed structure for this thesis is conventional *n*-type DG-CNTFET as depicted by figure 3.17 (a) over the existing structure of DG-MOSFET, where L_S, L_D and L_G are lengths of source, drain and gate respectively. t_{ox1} and t_{ox2} defines thickness of oxide layers of top and bottom gates. DG-MOSFET structure is described in figure 3.17. (b).

Table 3.9. describes the device parameters of optimized structure of conventional DG-CNTFET considered for evaluating the performance of device. These parameters have been used to evaluate the conventional *n*-type DG-CNTFET and compared with the DG-MOSFET.

Table 3.9. Device parameters of optimized structure of conventional *n*-type DG-CNTFET.

Parameters	**Values**
Thickness of oxide	1*nm*
Diameter (d)	1.093*nm*
Silicon Film thickness	5*nm*
Oxide material	SiO_2 (ξ_r =3.9)
Nanotube Length	30*nm*
Source Length	10*nm*
Gate Length	10*nm*
Drain Length	10*nm*
Doping	$5\times10^{3}cm^{-3}$

Current- voltage characteristics for conventional *n*-type DG-CNTFET is further compared with DG-MOSFET to analyze device performance considering ON current, OFF current and ON current to OFF current ratio.

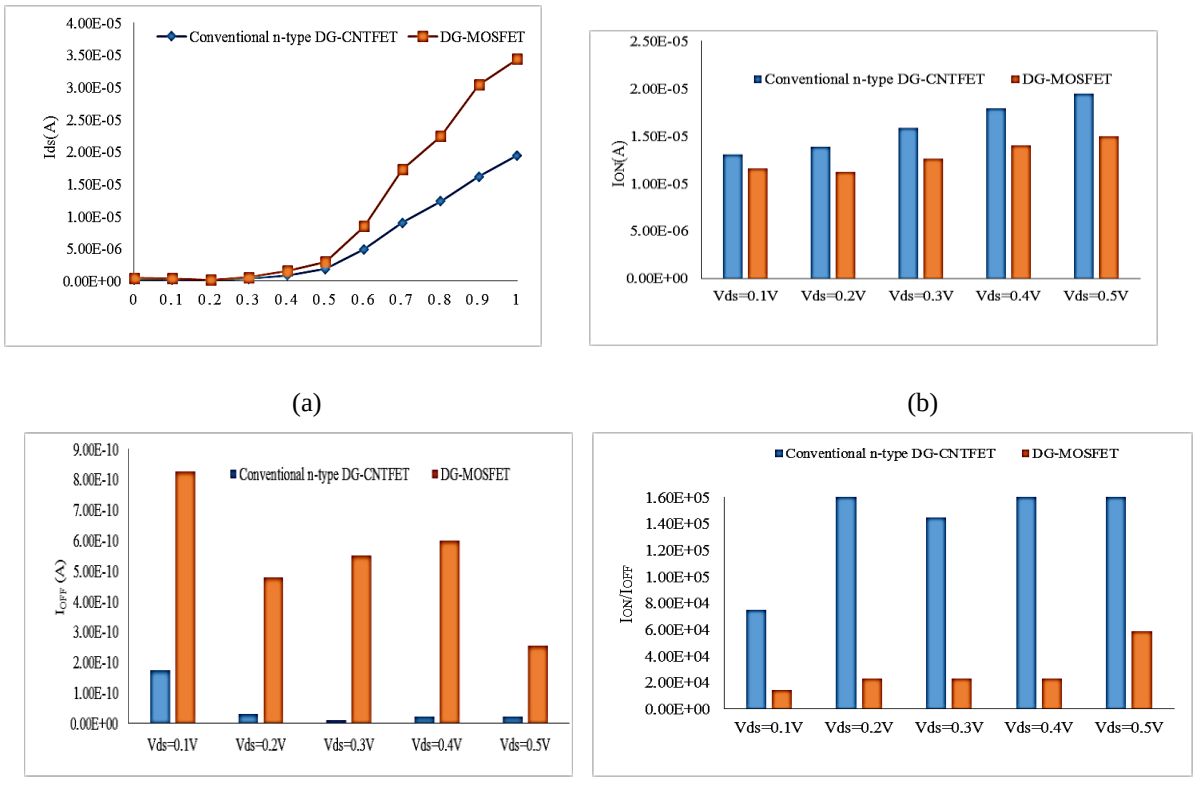


Figure 3.18. DG-MOSFET and conventional *n*-type DG-CNTFET's (a) current-voltage characteristics (b) ON current (c) OFF current and (d) ON current to OFF current Ratio.

Figure 3.18. (a) describes the (a) current voltage characteristics (b) ON current (c) OFF current and (d) ON current to OFF current ratio of DG-MOSFET and optimized structure of conventional *n*-type DG-CNTFET. The drain current of conventional *n*-type DG-CNTFET is more in comparison with DG-MOSFET as shown from figure 3.18. (a). Conventional *n*-type DG-CNTFET exhibit ballistic transport, which means electrons travel through the carbon nanotube channel without scattering. This results in less resistance and higher electron mobility, leading to higher drain current compared to DG-MOSFETs where scattering due to lattice imperfections and phonon scattering occur. The ON current of conventional *n*-type DG-CNTFET is high when compared with DG-MOSFET as described from figure 3.18 (b).

Figure 3.18. (c) shows that OFF current is less in conventional *n*-type DG-CNTFET when compared with DG-MOSFET so leakage current is less in conventional *n*-type DG-CNTFET. Conventional *n*-type DG-CNTFETs often use semiconducting carbon nanotubes, which have a relatively larger bandgap compared to the materials used in DG-MOSFETs (typically silicon). A larger bandgap means that there is a greater energy barrier for electrons to move in off state that results in low OFF-state leakage current in conventional *n*-type DG-CNTFETs. ON current to OFF current ratio describes ability to switch devices, which is more in conventional *n*-type DG-CNTFET when compared with DG-MOSFET as depicted in figure 3.18 (d). Therefore, optimized conventional *n*-type DG-CNTFET structure is best in performance when compared with DG-MOSFET. Optimized conventional *n*-type DG-CNTFET structure is proposed structure for this work.

3.10. SUMMARY AND CONTRIBUTION OF CHAPTER

This chapter explored the basic concepts of chirality, carbon nanotube and history of CNTFETs. Structure of CNTFET has been discussed in detail. Types of single- gate CNTFET such as back-gate CNTFET, top-gate CNTFET, wrap-around CNTFET and suspended CNTFET have been discussed. Further, to understand the concept of DG-CNTFET, various types of CNTFET on the basis of doping have been discussed in this chapter. DG-CNTFET has been used with the aim of reducing the SCEs like leakage current and threshold voltage fluctuations. On the basis of doping in the device, CNTFET has been classified into four kinds namely SB-DG-CNTFET, PG-DG-CNTFET, MOSFET- like (Conventional type) DG-CNTFET and tunnel DG-CNTFET. The optimized structure of conventional n-type DG-CNTFET has been proposed according to the ITRS 2015 on the basis of doping and variable diameter & process parameter variations. The performance of all four structures of DG-CNTFET have been evaluated on the basis of performance parameters with the aim of reducing

leakage current and high ON current. Simulation results showed that proposed conventional n-type DG-CNTFETs with diameter=1 *nm*, channel length =10 *nm* and doping value=5×10^3 as molar fraction are the best alternatives for applications that require less power. Several process variations including variable diameter of CNT and channel length are simulated. It is analysed that proposed conventional *n*-type DG-CNTFETs are more immune to process variations. The conventional *n*-type DG-CNTFET has been obtained as optimized device which is a proposed structure for the thesis due to its best performance out of all four structures in all aspects.

Few studies related to conventional *n*-type DG-CNTFET has been cited in the literature. But a little work has been done considering temperature impact on performance of conventional DG-CNTFET. So, it is necessary to evaluate DG-CNTFET performance at different temperature to analyze the impact of thermal environmental conditions for conventional *n*-type DG-CNTFET. Temperature dependent drain current modeling and performance analysis of conventional *n*-type DG-CNTFET is presented in the chapter 4 considering the optimized device parameters of the DG-CNTFET described in this chapter.

PUBLISHED WORK RELATED TO THIS CHAPTER:

[1] Aakanksha Lakhanpal and Karmjit Singh Sandha, "Impact of Thermal-Aware Enviromental Conditions on Double- Gate Carbon Nanotube FET." *Microelectronics Journal*, vol. 114, p. 105146, 2021. (**SCI indexed- Impact Factor - 2.2**)

[2] Aakanksha Lakhanpal and Karmjit Singh Sandha, "Performance Analysis of Double-gate Carbon-nanotube FET and MOSFET for High Speed Integrated Circuits Design.", *International Journal of Engineering and Advanced Technology (IJEAT),* vol. 9, 2019. (**Scopus indexed**)

CHAPTER 4

TEMPERATURE DEPENDENT DRAIN CURRENT MODELING & PERFORMANCE ANALYSIS OF DG-CNTFET

Temperature-dependent drain current modeling and performance analysis of DG-CNTFET are presented in this chapter to estimate device performance at nano-scaled technology nodes under variable environmental conditions. To develop model for drain current of DG-CNTFET, the optimized structure presented in previous chapter has been used. In this chapter, current-voltage characteristics of DG-CNTFET are calculated by writing codes in MATLAB using developed analytical model described in derived equations for drain current and analytical results for drain current obtained in MATLAB are also compared with simulation results achieved by nano TCAD ViDES simulation tool at variable temperature to analyze thermally-aware environmental conditions effect on DG-CNTFET. DG-CNTFET's developed analytical model is utilized to estimate various performance parameters for variable temperature range.

4.1. INTRODUCTION

As the technology nodes have been scaled down, various SCEs of MOSFET namely leakage current, DIBL and mobility degradation have become prominent which degrade the overall performance of chip at nano-scaled technology nodes. As a result, there is need for innovative solutions to overcome these shortcomings so that the advantages of scaled down technology nodes can be achieved. As per the recent studies, carbon nanotubes have a potential to act as a leading material to overcome these issues at advanced technology nodes. Considering its excellent thermal conductivity and better electrical properties, CNTs seem to be a very good way out for semiconductor industry. Simulation studies based on thermal characteristics showed that CNTs had a very high thermal conductivity and can provide the stable conduction at variable thermal environment condition [125]. Traditional MOSFETs use bulk silicon as channel material whereas CNTFETs use one/more CNTs as channel material [125].

High performance, faster speed and small size are the necessities of today's semiconductor industry. Various problems such as changing thermal conditions and high current densities lowers IC's reliability. For VLSI industry and high packing densities of ICs, temperature variations play a crucial role and must be taken into account. Thermal conditions can basically affect device operations and are the main cause for the failure of integrated circuits because of the large fluctuations in the device parameters in nano-regime. Therefore, devices that depend on temperature and have to work under variable temperature need be thoroughly analysed. For

every device to work properly, it is very necessary to understand how temperature variations affect device performance and ICs.

CNTFET can be stable at high temperatures, but their properties can change under extreme conditions. High temperatures might lead to the deformation or breakage of nanotubes, affecting the performance and reliability of transistor. On other hand, at very low temperatures, mobility of charge carriers can be limited leading to slow switching speeds and decreased conductivity affecting overall device performance. For temperature range of 250 K to 400 K, VLSI devices have great inconsistency to operate under variable temperatures in nano-regime. The performance of device for various performance parameters namely drain conductance, subthreshold swing, ON and OFF currents and output characteristics are largely affected by the temperature variations. As a result, it is possible to evaluate device performance by analysing the various temperature dependent parameters and their effect on device performance.

This chapter includes temperature dependent drain current modeling using the optimized structure of DG-CNTFET developed in last chapter. DG-CNTFET's current-voltage characteristics have been evaluated at room temperature. Further, to evaluate DG-CNTFET's performance in a thermal variable environment, an analytical model of DG-CNTFET that is temperature dependent is developed. DG-CNTFET's I-V characteristics are determined in nano-TCAD ViDES (nano-Technology Computer Aided Design ViDES) simulator using developed model. Results obtained for DG-CNTFET's I-V characteristics by writing codes in MATLAB are compared with the current voltage characteristics obtained in nano-TCAD ViDES simulator at various temperatures of 250 K to 400 K to analyze variable temperature effect on DG-CNTFET. Also, results for a temperature range of 250 K to 400 K that affects output characteristics, drain conductance, subthreshold swing, ON current and OFF current under thermal environmental conditions have been obtained.

4.2. DOUBLE-GATE CARBON NANOTUBE FIELD EFFECT TRANSISTOR

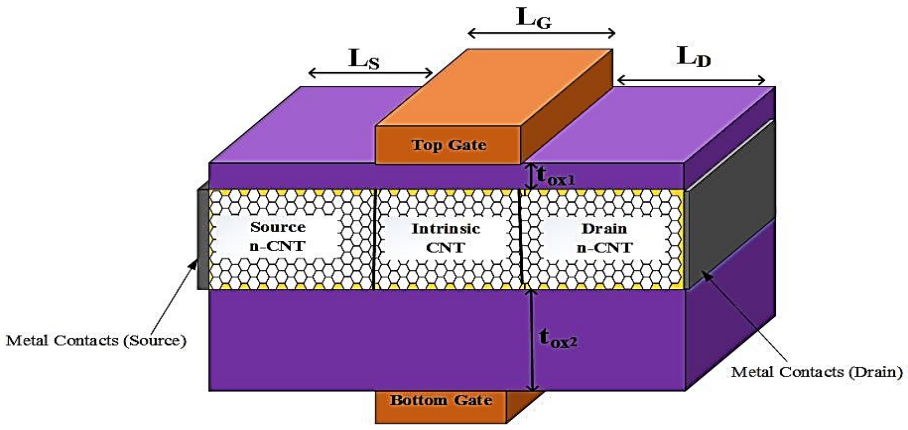


Figure 4.1. Conventional DG-CNTFET structure [121].

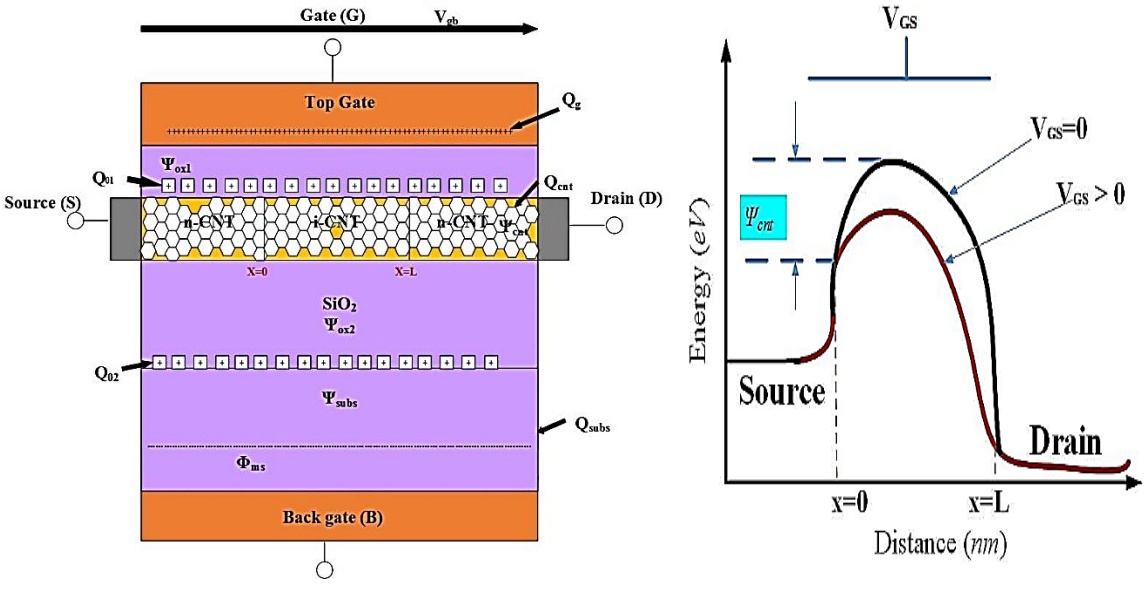
DG-CNTFET consist of two gates namely top gate and bottom gate as described in figure 4.1. L_S, L_D and L_G are lengths of source, drain and gate respectively. t_{ox1} and t_{ox2} define thickness of oxide layers. In DG-CNTFET, two gates are used to have better isolation between drain and gate &source and gate. The functionality of device is controlled by gate of device. Source and drain regions are doped with *n* type CNT and channel is made intrinsic. By introducing *n*-type dopants in CNT, the fermi level of CNT shifts which affects the electronic properties of CNTs. There are numerous advantages of using double gate over single gate CNTFET. Using double gate enables higher drive current at lower threshold voltage and supply voltage. Leakage current at gate and channel of DG-CNTFET gets reduced which further reduces power consumption of device. DG-CNTFET have been used in place of single gate CNTFET because it reduces short channel effects. This device is well suited for reducing SCEs namely leakage current and DIBL.

4.3. TEMPERATURE DEPENDENT DRAIN CURRENT MODELING OF CONVENTIONAL DG-CNTFET

Using the optimized structure of conventional DG-CNTFET obtained in previous chapter, the temperature dependent modeling of drain current for DG-CNTFET has been carried out.

Some of the approaches like Non equilibrium green function (NEGF) are complex in nature and are more time consuming [126]. So, there is need for mechanism named as ballistic transport approach [126] which is best for modeling current-voltage characteristics of single wall CNTFET. Charge of CNT is calculated using the transport mechanism in this approach. The CNT charge causes current flow in channel. To study how temperature affects the current-voltage characteristics of DG-CNTFET, a temperature dependent model is developed. The model, on basis of chirality, is only applicable to semiconducting property of carbon nanotubes.

Due to ballistic transport that takes place in CNTFET, Current transport is not dependent on length of CNTs [127]. 10 *nm* -15 *nm* is mean free path reported for SWCNT [128]. Therefore, in current calculations, length of channel is not a major consideration. Chirality/diameter of CNT is dominant factor for current calculations. Diameter, bandgap, doping and threshold voltage are the factors that affect current calculations. Further, the oxide layer's capacitance, which is calculated by oxide thickness and dielectric constant, is important while calculating current [126]. Figure 4.2. (a) describes a charge sheet model of DG-CNTFET. Current transport equation of DG-CNTFET is achieved by calculation of charge inside the carbon nanotube and relating terminal voltages to carbon nanotube potential which are described by the charge sheet model of DG-CNTFET. The basic charge distributions inside DG-CNTFET are given by charge sheet model [129]. The distribution of charges is explained as follows: Q_g is charge on gate, Q_{01} and Q_{02} are charges inside oxide layers, charge inside CNT is Q_{cnt} and Q_{subs} is charge in substrate. Potential drop across oxides is ψ_{ox1} and ψ_{ox2} and voltage between gate and substrate (back gate) is V_{gb}, potential across CNT is ψ_{cnt} and work function difference between gate and substrate materials is ϕ_{ms}. Surface potential in substrate with respect to back gate is ψ_{subs}.



(a) (b)

Figure 4.2. (a) DG-CNTFET's charge and potential distribution (b) Shift in band with gate bias at high drain voltage.

The shift in bandgap of CNT with gate bias for high drain voltage is described in figure 4.2. (b). When voltage at gate is not applied across CNT, energy band gap is more at distance x=0. When voltage at gate terminal is applied across a CNT, potential that is induced between the

CNT and oxide interface rises, affecting the band diagram to shift downward at distance x=L, because of raised surface potential of carbon nanotube (CNT). The band gap shifts downward when positive gate bias is applied as depicted in figure 4.2. (b)Charge carriers in CNT, affects electronic properties and shifts the band gap when distance changes from x=0 to the length of channel.

Doping value in DG-CNTFETs has effect on OFF current (I_{OFF}) and charge produced in channel has effect on ON current (I_{ON}). Model is used for the conventional devices because conduction occurs due to doping and shift in source and drain's fermi levels. Doping value considered for this work is 5×10^3 as molar fraction which is described as number of doped atoms per unit total number of atoms and is optimized doping value as discussed in previous chapter. Chiral numbers (n, m) describe properties of CNT. Calculation of diameter of CNT for DG-CNTFET is necessary because it directly affects device's electrical characteristics, including drain current. The CNT diameter affects its density of states and electronic band structure. These factors influence how electrons move within the nanotube, affecting carrier transport properties. The first step for calculating drain current is calculation of CNT diameter used as channel material in DG-CNTFET. Diameter (d) and band gap (E_g) are calculated using these chiral numbers (n, m).

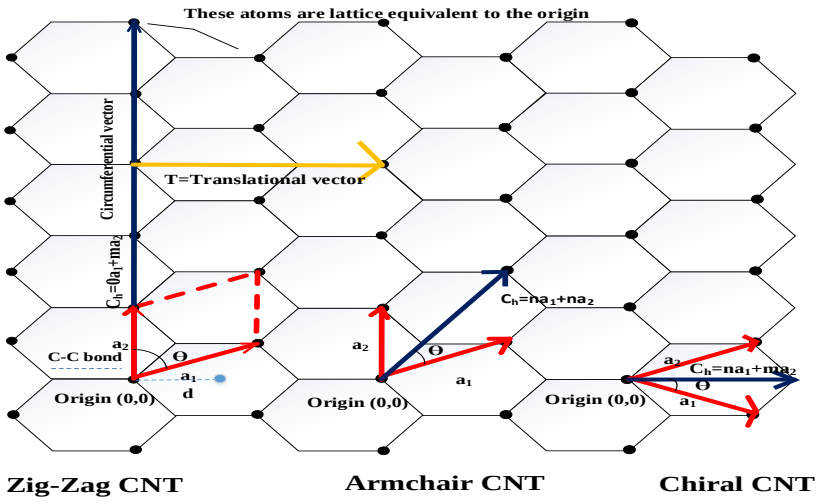


Figure 4.3. CNT configurations with chiral vector C_h and basis vectors a_1 and a_2.

Figure 4.3. depicts configuration of various kinds of CNT based on chirality with basis vectors as a_1 and a_2 and chiral vector C_h. Chiral vector, denoted by C_h, forms an angle θ with a_1. n and m can be used to describe diameter and chiral angle θ of a carbon nanotube (CNT).

Considering CNT diameter, circumferential vector is expressed as

$C=\pi d$ (4.1)

$$\overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \quad (4.2)$$

Cartesian coordinates are used to represent a_1 and a_2 as

$$a_1 = (\frac{3}{2}\ a_{cc}\ ,\ \frac{\sqrt{3}}{2}\ a_{cc})\ \ \&\ a_2 = (\frac{3}{2}\ a_{cc}\ ,\ -\frac{\sqrt{3}}{2}\ a_{cc}) \quad (4.3)$$

$$a_1 = \frac{3}{2}\ a_{cc}\ \hat{i} + \frac{\sqrt{3}}{2}\ a_{cc}\ j\ \ \&\ a_2 = \frac{3}{2}\ a_{cc}\ \hat{i} - \frac{\sqrt{3}}{2}\ a_{cc}\ j \quad (4.4)$$

Magnitude of a_1 and a_2 is denoted as

$$|a_1| = \sqrt{(\frac{3}{2}acc - 0)^2 + (\frac{\sqrt{3}}{2}acc - 0)^2} \quad (4.5)$$

$$|a_2| = \sqrt{(\frac{3}{2}acc - 0)^2 + (-\frac{\sqrt{3}}{2}acc - 0)^2} \quad (4.6)$$

As chiral vector's magnitude is equal to tube's circumference and it can be denoted as

$$|\overrightarrow{C}| = n|\overrightarrow{a_1}| + m|\overrightarrow{a_2}|$$

$$|\overrightarrow{a_1}| + |\overrightarrow{a_2}| = \sqrt{a_1^2 + a_2^2 + 2a_1a_2\cos\theta} \quad (4.7)$$

$$|\overrightarrow{C}| = \sqrt{3a_{cc}{}^2(n^2 + m^2 + nm)} \quad (4.8)$$

Now we need to determine CNT diameter,

Magnitude of chiral vector = Circumference = πd

First step is to determine diameter (d) value, which is provided by [130]. Therefore, diameter of carbon nanotube can be written as

$$d = \frac{\sqrt{3}a_{cc}\sqrt{(n+m)^2 - nm)}}{\pi} \quad (4.9)$$

where chiral numbers are n, m and a_{cc} value = 0.142 nm and it indicates inter- atomic distance of carbon atoms [130]. CNT diameter is closely related to its bandgap energy. Smaller diameter

of carbon nanotubes tends to have larger bandgaps, which can influence the drain current of device. The second step involves using the bandgap to derive conduction band minima. Bandgap with half value at zero gate voltage is conduction band minima. Diameter of CNT is related to bandgap as given by [131]

$$E_{Gap} = \frac{2aV_{pp\pi}}{d\sqrt{3}} \tag{4.10}$$

where $V_{pp\pi}$ is carbon π-π bond's energy which is $3.033eV$ [130], d is CNT diameter, a represents carbon atoms' inter-atomic distance. Number of carriers depend on the bandgap of material. A large bandgap will make it more difficult for a carrier to be thermally excited across the bandgap. Increasing the bandgap energy decreases the carrier concentration as the bandgap energy increases, exciting electrons from valence band to conduction band is difficult, resulting in few electrons and holes in channel. Concentration of intrinsic charge carriers (n_{cnt}) of nanotube is defined as [132]

$$n_{cnt} = \int_{E_C}^{\infty} D(E)\, f(E) dE \tag{4.11}$$

where $f(E)$ represents Fermi-Dirac distribution and $D(E)$ stands for density of states. Fermi dirac distribution can be given as

$$f(E) = \frac{N(E)}{g(E)} = \frac{1}{1+\exp\left(\frac{E-E_F}{kT}\right)} \tag{4.12}$$

where particles number per unit volume per unit energy is $f(E)$. In addition, $N(E)$ stands for particles number & $g(E)$ is volume per unit energy, k is defined as Boltzmann constant, T stands for temperature and E_F for CNT fermi level.

For calculating density of states $D(E)$ of CNT, we need to know carbon nanotube's energy dispersion relation.

$g(E)$ which is density of states per unit length at energy E, gives total number of states per unit length between E and $E+dE$.

Between E_1 and E_2, total number of states per unit length is indicated by

$$\int_{E_1}^{E_2} g(E)dE \tag{4.13}$$

Following is the free electron's energy dispersion

$$E = \frac{k^2 h^2}{2m} + E_o \tag{4.14}$$

where *m* is particle's effective mass, *k* is Boltzmann constant, and Planck constant is *h.*

To find number of states between *E* and *E+dE*, differential wave vector *dk* is normalised according to length of one state.

$$g(E)dE = \frac{1}{\pi}\frac{dk}{dl} \tag{4.15}$$

Eq. 4.14 further implies

$$E - E_o = \frac{h^2 k^2}{2m} \tag{4.16}$$

Determining *k* from Eq. 4.16, is represented as

$$k = \frac{1}{h}\sqrt{2m(E - E_o)} \tag{4.17}$$

Eq. 4.17 when differentiated with respect to *E* results in $\frac{dk}{dE}$ as

$$\frac{dk}{dE} = \frac{1}{h}\sqrt{\frac{2m}{E - E_o}} \tag{4.18}$$

Overall density of states (DOS) is represented as

$$g_{tot}(E) = \sum_{j=1}^{N} g(E, j) = \frac{1}{\pi}\left|\frac{dk}{dE}\right| \tag{4.19}$$

where *N* is CNT structure's number of subbands.

So, CNT's energy dispersion relation must be known in order to determine DOS. In this work, zig-zag carbon nanotube has been used for which *E-k* dispersion relation of CNT which is zig-zag in nature is represented as

$$E_{zz}(k,q) = \pm \mathrm{V}_{pp\pi}\sqrt{1+4\cos(\frac{\sqrt{3}}{2}\mathrm{ka})\cos(\frac{\pi j}{n})+4\cos^2(\frac{\pi j}{n})} \tag{4.20}$$

where j is integer index (1 to $2n$) of subband, the value of $V_{pp\pi}$ is 3.1eV & k is expressed as

$$k = \pm\frac{2}{a\sqrt{3}}\cos^{-1}\{\frac{1}{4}\sec(\frac{\pi j}{n})[\frac{E^2}{V_{pp\pi}}-2\cos(\frac{2\pi j}{n})-3]\} \tag{4.21}$$

Differentiating k value with respect to E and substituting in eq. (4.19), we obtain,

$$g_{zz}(E,j) = \frac{8}{a\pi V_{pp\pi}\sqrt{3}}\frac{\mathrm{E}}{\sqrt{E^2-{E_c}^2}}dE \tag{4.22}$$

Therefore, density of states $D(E)$ is denoted as

$$D(E)dE = 2\sum_1^{AllBands}\frac{4}{\pi a V_{pp\pi}\sqrt{3}}\frac{E}{\sqrt{E^2-E_c^2}} \tag{4.23}$$

where a is interatomic distance between carbon atoms, which is approximately 0.142 nm, $D(E)$ is density of states and E_c is minimum conduction band energy.

Now, by putting $D(E)$'s value in Eq. (4.11), we get,

$$n_{cnt} = 2\sum_1^{AllBands}\frac{4}{\pi a V_{pp\pi}\sqrt{3}}\int_{E_c}^{\infty}\frac{E}{\sqrt{E^2-E_c^2}}(1+e^{\frac{(E-E_F)}{kT}})^{-1}dE \tag{4.24}$$

$$n_{cnt} = N_c I\exp(-E_c/kT) \tag{4.25}$$

where E_c is energy of conduction band, N_c is effective density of states at conduction band edges which is denoted by eq. (4. 26). Also, value of I is computed in eq. (4. 27),

$$N_C = \frac{8kT}{\pi V_{pp\pi}a\sqrt{3}} \tag{4.26}$$

Integral (I) is determined as [129]

$$I = \frac{1}{\sqrt{kT}}\int_0^{6\frac{E_C}{kT}}\frac{(kTx+E_C)}{x^{1/2}\sqrt{(kTx+2E_c)}}\mathrm{e}^{-x}dx \tag{4.27}$$

where k stands for Boltzmann constant, T is operating temperature, x is a number between 0 and $6\frac{E_C}{kT}$, and E_C is conduction band energy.

Fermi levels are zero at source and drain sides for intrinsic CNT. Doping affects current in the device. The fermi level which is shown by ΔE_F, shifts with doping. The ΔE_F value is as follows [132]

$$\Delta E_F = kT \ln\left(1+\frac{N}{n_{cnt,i}}\right) \tag{4.28}$$

where N stands for doping value in DG-CNTFET. ΔE_F can have a positive or negative value based on the doping. *For n*-type doping, ΔE_F is positive, whereas for *p*-type doping, it is negative. Drain current calculations for DG-CNTFET depends mainly on temperature (T), effective density of states (N_c) & conduction band energy (E_c). From eq. (4. 29), it is depicted that DG-CNTFET drain current gets affected in a thermal environment with varying temperatures.

Drain current (I_{DS}) is represented by [133]

$$I_{ds} = \frac{qkT}{\pi h}\left\{\ln\left[1+e^{\frac{\Delta E_F+q(\varphi_{cnt}(0)-V_{SS}-\Phi_0)-E_c}{kT}}\right]-\ln\left[1+e^{\frac{\Delta E_F+q(\varphi_{cnt}(L)-Vds-\Phi_0)-E_c}{kT}}\right]\right\} \tag{4.29}$$

where Ψ_{cnt} stands for front gate surface potential, Φ_0 for back gate surface potential, h is Planck's constant, q is charge on electron. Value of Ψ_{cnt} at source and drain side can be computed as [129]

$$\varphi_{cnt}(0) = V_{gs} - V_{th} \tag{4.30}$$

$$\varphi_{cnt}(L) = \frac{V_{gs} - \delta I e^{-1} - V_{fb} + \delta m\left(V_{cb} + \Phi_0 + \frac{E_c - \Delta E_F - kT}{q}\right)}{1+\delta m} \tag{4.31}$$

where V_{fb} stands for flat band voltage, V_{gs} for gate to source voltage and V_{cb} for potential induced by voltages of source and drain between CNT and substrate. For L as length of channel, m and δ values are denoted by [129]

$$m = \frac{\sqrt{\frac{2E_C}{kT}+1}-Ie^{-1}}{\frac{2kT}{q}} \tag{4.32}$$

$$\delta = \frac{qLN_c}{C} \tag{4.33}$$

4.3.1. Quantum Capacitance Model

The conventional DG-CNTFET's quantum capacitance model for one-dimensional transport is shown in figure 4.4. For quantum capacitance model. Variation in electrical charge (q_{cnt}) in channel in relation to CNT surface potential (Ψ_{cnt}) is defined as DG-CNTFET channel's quantum capacitance (C_q). Quantum capacitance model is considered to calculate the total capacitance in DG-CNTFET.

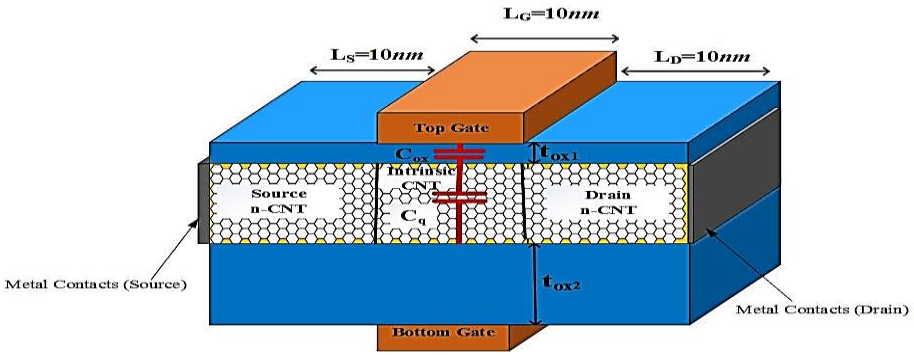


Figure 4.4. DG-CNTFET's model of quantum capacitance.

In quantum capacitance model, total capacitance C is the sum of following two capacitances, oxide capacitance (C_{ox}) and quantum capacitance (C_q):

$$C = \frac{C_{ox} C_q}{C_{ox} + C_q} \tag{4.34}$$

Capacitance (C_{ox}) of oxide layer and quantum capacitance (C_q) are represented by [134]

$$C_{ox} = \frac{2\pi\xi_o L}{\ln \frac{t_{ox} + r + \sqrt{t_{ox}^2 + 2t_{ox} r}}{r}} \tag{4.35}$$

where t_{ox} is oxide layer's thickness, r is CNT radius and oxide material's dielectric constant is ξ_o. Quantum capacitance is represented as [135]

$$Cq = \frac{\partial q_{cnt}}{\partial \varphi_{cnt}} \tag{4.36}$$

where q_{cnt} is CNT channel's charge when V_{gs} is applied and represented by [136]

$$q_{cnt} = \frac{q}{2} n_{cnt} \exp\left(\frac{\varphi_{cnt}}{kT}\right)\left[1+\exp\left(\frac{-V_{ds}}{kT}\right)\right] \tag{4.37}$$

The representation of first conduction band minima is 0.45*/d.*

4.4. PERFORMANCE ANALYSIS OF DRAIN CURRENT IN DG-CNTFET

Device's I-V characteristics curve shows relationship between voltage across the terminals of proposed DG-CNTFET structure and current flowing through device.

In DG-CNTFET, I-V characteristics provide valuable information about the behaviour and performance of device. Analysing these current-voltage characteristics of DG-CNTFET can yield several important parameters. ON current, OFF current and subthreshold swing are determined through DG-CNTFET's I-V characteristics. Plotting drain current versus drain to source voltage in presence of constant V_{gs} is DG-CNTFET's output characteristics. The parameters such as the drain conductance of the DG-CNTFET are extracted using output characteristics.

Current flowing through DG-CNTFET when it's in ON state is the ON current. It is important for understanding the ability of device to carry current. The current flowing through the DG-CNTFET when it is in OFF state is OFF current. It is essential for determining leakage current and power consumption in device. Subthreshold swing measures the steepness of subthreshold region of I-V curve and is important for low power design of device. Analyzing I-V characteristics and output characteristics and then extracting these parameters can help in optimizing the DG-CNTFET for various applications, including digital logic circuits, analog circuits and high-frequency devices.

Table 4.1. describes device parameters of DG-CNTFET used in the calculations and simulations.

Table 4.1. Device parameters of conventional DG-CNTFET.

Parameters	Values
Oxide material	SiO_2 (ξ_r =3.9)
Diameter (*d*)	1.093*nm*
Silicon Film Thickness	5*nm*
Nanotube Length	30*nm*
Thickness of oxide	1*nm*
Source Length	10*nm*
Gate Length	10*nm*
Drain Length	10*nm*
Doping	$5\times10^{3} cm^{-3}$

This section evaluates proposed DG-CNTFET structure's I-V characteristics at room temperature in nano-TCAD ViDES and MATLAB simulation tools.

Further, in order determine how proposed DG-CNTFET structure performs in a variable temperature range of 250K to 400K, various performance parameters considering output characteristics, ON current, OFF current, subthreshold swing and drain conductance have been evaluated.

Proposed conventional DG-CNTFET structure's I-V characteristics is calculated using its analytical model and its equations as mentioned in section 4.3. Current-voltage characteristics for proposed model of DG-CNTFET are calculated by writing codes in MATLAB using analytical model described in previous section (using eq. 4.1-4.37) and analytical results achieved in MATLAB are compared with simulation results obtained at room temperature using nano-TCAD ViDES simulation tool, as illustrated in figure 4.5.

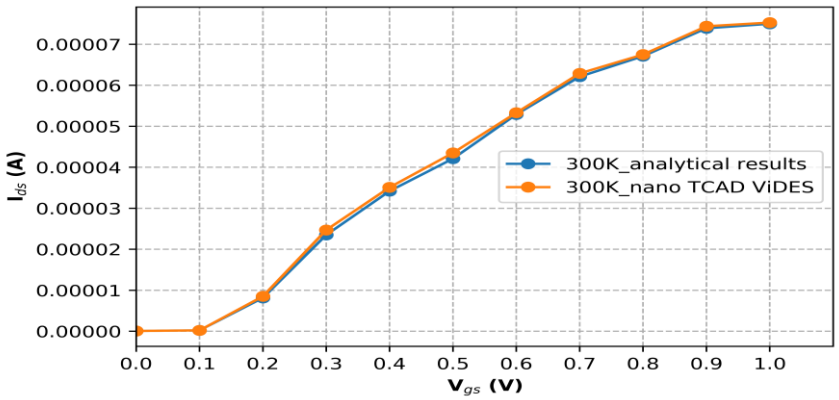


Figure 4.5. Current- voltage (I-V) characteristics of DG-CNTFET at V_{ds}= 0.4V.

DG-CNTFET's current-voltage characteristics is obtained in nano TCAD ViDES simulator and compared with the analytical results obtained using MATLAB at room temperature. Figure shows that analytical results and simulated results obtained using nano-TCAD ViDES simulator follow a similar trend. When gate to source terminal is given a positive voltage (V_{gs}), an electric field is created in channel region of DG-CNTFET. This electric field influences the behaviour of charge carriers in carbon nanotube channel. Applying a positive voltage to gate, more charge carriers are introduced in the channel, enhancing current flow between drain and source terminals of DG-CNTFET. As a result, when the DG-CNTFET's gate to source voltage rises, it also increases drain current.

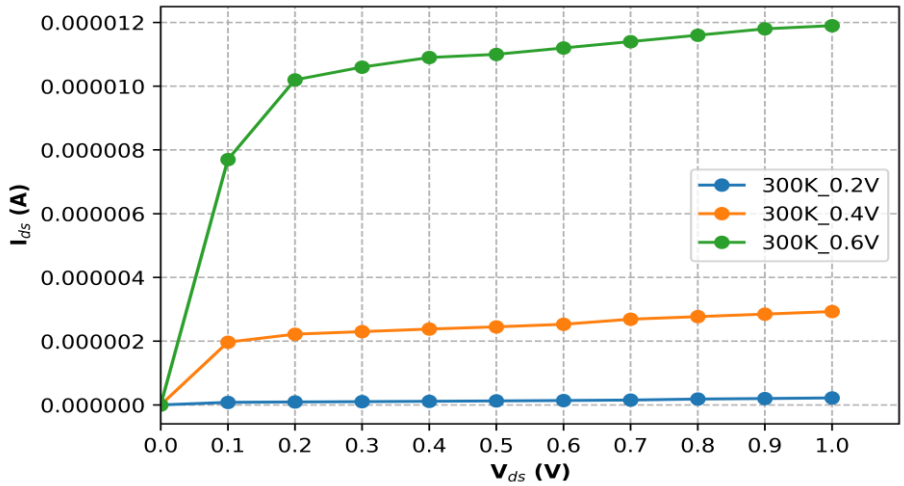
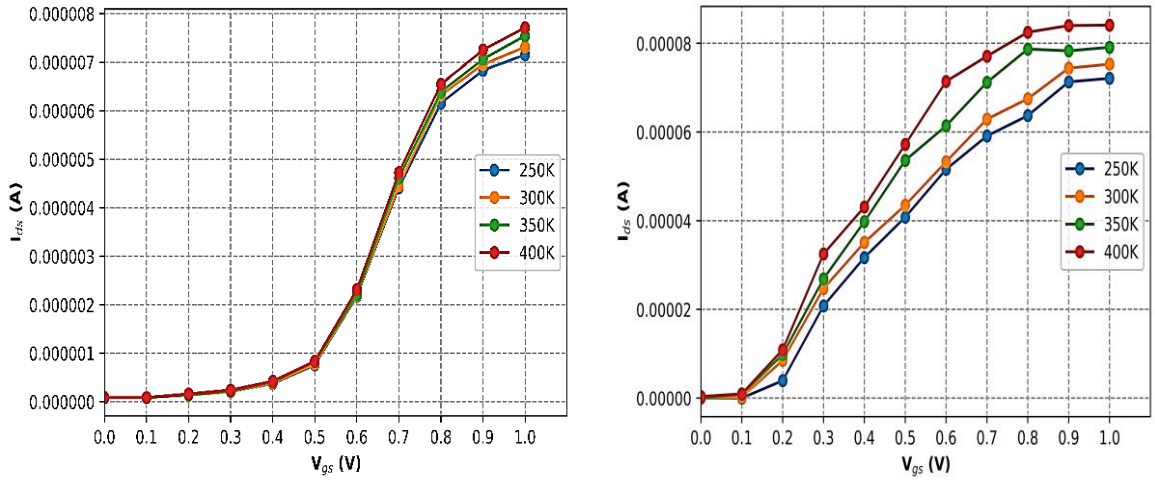


Figure 4.6. DG-CNTFET's output characteristics at variable V_{gs} values at room temperature.

DG-CNTFET's output characteristics has been obtained in figure 4.6. There is rise in drain current at low values of V_{ds} values. Increasing gate to source voltage (V_{gs}) from 0.2V to 0.6V in DG-CNTFET leads to significant rise in drain current (I_{ds}) for a given V_{ds}. In the plot of output characteristics of DG-CNTFET, increasing the V_{gs} from 0.2V to 0.6V causes I_{ds}-V_{ds} curve to shift upwards. For a given V_{ds} value, corresponding drain current will be higher when V_{gs} is increased from 0.2V to 0.6V. This shift in DG-CNTFET's output characteristics signifies enhanced conductivity of DG-CNTFET for higher gate to source voltage, indicating the improved performance and better transistor behaviour for electronic applications. With increase in V_{ds}, drain current of DG-CNTFET gets saturated as conduction channel saturates between source and drain and there is constant flow of current in the device.

DG-CNTFETs with higher output characteristics can switch ON and OFF quickly and can be used in applications where high-speed operation is required. Further, improved output characteristics of DG-CNTFET operate efficiently at low power and can be used for battery-powered devices, leading to longer battery life and reduced energy consumption in various devices.

To estimate the impact of variable temperatures, DG-CNTFET's I-V characteristics for variable temperatures (250K to 400K) are evaluated on the basis of temperature dependent analytical equations (4.1- 4.37) using MATLAB and described in figure 4.7. (a) and figure 4.7. (b) for constant drain to source voltages (V_{ds}) of 0.1V and 0.4V respectively.



(a) (b)

Figure 4.7. (a) DG-CNTFET's I-V characteristics for variable temperatures at V_{ds} = 0.1V (b) DG-CNTFET's I-V characteristics for variable temperatures at V_{ds} = 0.4V.

Temperature (250K to 400K) impact on drain current for various V_{gs} at drain to source voltage V_{ds} = 0.1V & V_{ds}=0.4V is shown in figure 4.7. (a) & (b). Because same number of electrons and holes contribute to DG-CNTFET's drain current, it's value of lower at temperature T=250K for V_{gs} < 0.5V than drain current at temperature T=400K. Also, at low V_{ds} ie. 0.1V, the impact of temperature induced changes in carrier concentration might be relatively consistent, leading to more stable I_{ds}-V_{gs} curve of DG-CNTFET. At low V_{ds}, these effects have a comparatively smaller influence resulting in more stable I_{ds}-V_{gs} curve. Further, the band bending near drain region can affect the carrier transport. At low V_{ds}, the band bending has a smaller impact on the carrier movement compared to high V_{ds}, leading to more consistent I_{ds} with respect to V_{gs}.

Further, for V_{gs} > 0.5V, because carrier mobility in CNTFETs is proportional to carrier velocity, rise in carrier mobility results in increase in carrier velocity. At higher V_{ds} i.e., 0.4V, transistor's threshold voltage can shift due to various SCEs including DIBL and channel length modulation. These shifts can affect relationship between I_{ds}, V_{ds} and V_{gs}.

The comparison of current-voltage characteristics has been evaluated using MATLAB considering the developed model of DG-CNTFET and simulated results are carried out in nano TCAD ViDES for a V_{ds} of 0.4V at variable temperature range as depicted in figure 4.8, taking into account the parameters of device given in table 4.1.

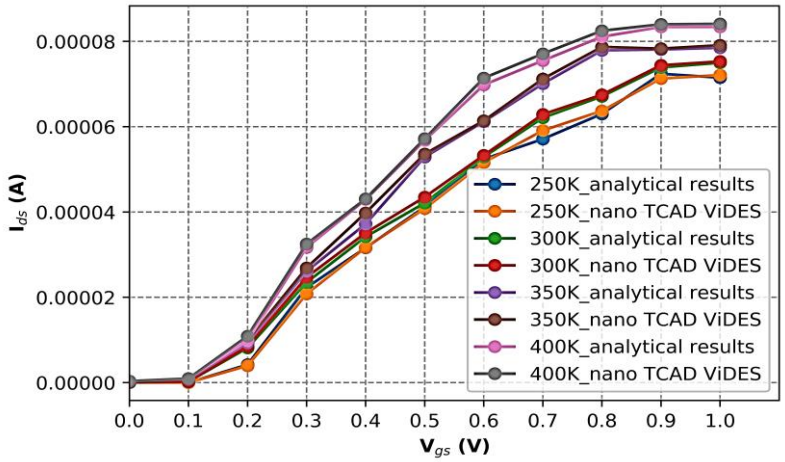


Figure 4.8. Simulated and analytical DG-CNTFET's I-V characteristics at variable temperatures.

Drain current (I_{ds}) of DG-CNTFET is calculated by putting different V_{ds} values in eq. (4. 29). Drain current (I_{ds}) for various V_{gs} values is then plotted [137]. It has been seen that results achieved by analytical model in MATLAB which is temperature dependent follow a similar trend for I-V characteristics obtained by nano-TCAD ViDES simulator. There is small variation in results since MATLAB and nano-TCAD ViDES use different modeling approaches. The charge sheet-based model, which is used for calculating the CNT potential and band shift using MATLAB is highly affected by source and drain regions' parasitic resistances. However, in another approach (nano-TCAD ViDES), transport for nanoscale devices is performed and computed using NEGF formalism [136].

DG-CNTFET's extracted drain current (I_{ds}) values at various temperatures such as 250K, 300K, 350K and 400K are shown in table 4.2. In MATLAB, DG-CNTFET structure's analytical model is used to calculate drain current (I_{ds}), and nano-TCAD ViDES investigates the simulated drain current values for various V_{gs}.

Table 4.2. Parameter I_{ds} for variable temperatures using nano-TCAD ViDES simulator and analytical model.

	Simulator Results				**Analytical Model Results**			
V_{gs}	I_{ds} **at** V_{ds}**=0.4V**				I_{ds} **at** V_{ds}**=0.4V**			
	250K	**300K**	**350K**	**400K**	**250K**	**300K**	**350K**	**400K**
0	9.19nA	0.070 µA	0.079 µA	0.342 µA	9.43nA	0.072 µA	0.077 µA	0.335µA
0.1	10.2nA	0.212 µA	0.812 µA	0.954 µA	9.20nA	0.221 µA	0.754 µA	0.947 µA
0.2	3.94 µA	8.52 µA	9.85 µA	10.9 µA	4.21µA	8.52 µA	9.35 µA	9.85 µA
0.3	20.8 µA	24.7 µA	26.9 µA	32.5 µA	22.3 µA	24.7 µA	26.1 µA	31.7 µA
0.4	31.7 µA	35.1 µA	39.8 µA	43.1 µA	31.6 µA	35.1 µA	37.2 µA	42.9 µA
0.5	40.8 µA	43.5 µA	53.6 µA	57.2 µA	41.2 µA	43.5 µA	52.9 µA	56.8 µA
0.6	51.6 µA	53.3 µA	61.4 µA	71.4 µA	52.4 µA	53.3 µA	61.2 µA	69.8 µA
0.7	59.1 µA	62.9 µA	71.2 µA	77.1 µA	57.1 µA	62.9 µA	70.1 µA	75.5 µA
0.8	63.7 µA	67.5 µA	78.7 µA	82.5 µA	63 µA	67.5 µA	77.9 µA	81.1 µA
0.9	71.3 µA	74.4 µA	78.3 µA	84 µA	72.4 µA	74.4 µA	78.1 µA	83.4 µA
1	72.1 µA	75.3 µA	79.1 µA	84.1 µA	7.15 µA	75.3 µA	78.5 µA	83.4 µA

Results achieved from analytical model used in MATLAB follow a similar trend as I_{ds} obtained in nano-TCAD ViDES for varying temperatures (250 K-400 K) at various values of V_{gs} and constant V_{ds} of 0.4V. Further, the results also show that for different V_{gs}, drain current (I_{ds}) increases as temperature increases from 250K to 400K. Temperature increase from 250K to 400K, increases thermal energy that allow the electrons to overcome energy barrier at interface between nanotube and source/drain, leading to higher carrier mobility and high drain current in DG-CNTFET. Therefore, in order to study actual device performance, impact of temperature cannot be ignored as it affects the drain current (I_{ds}). Further, in order to establish accuracy between simulated results achieved in nano-TCAD ViDES and analytical model obtained in MATLAB, percentage error in drain current (%age error in I_{ds}) was also determined at temperatures that varies from 250 K to 400 K, as depicted in table 4.3.

Table 4.3. Percentage error in I_{ds} for variable temperatures considering analytical model and nano-TCAD ViDES simulator.

V_{gs}	I_{ds} %age error in analytical and simulated results at variable temperature			
	250K	**300K**	**350K**	**400K**
0	2.61	2.85	2.53	2.04
0.1	9.80	4.24	7.14	0.73
0.2	6.85	4.46	5.07	9.63
0.3	7.21	4.85	2.97	2.46
0.4	0.31	2.56	6.53	0.46
0.5	0.98	3.21	1.3	0.69
0.6	1.55	0.75	0.32	2.24
0.7	3.38	1.27	1.54	2.07
0.8	1.09	0.59	1.01	1.69
0.9	1.54	0.67	0.25	0.71
1	0.83	0.39	0.75	0.83

The results show that drain current is rising almost in same ratio on increasing V_{gs}, for the analytical and simulation results. A small variation of less than 10% in error occurs in I_{ds} as determined by both simulated and analytical models. However, table 4.3. reveals that as temperature rises from 250 K to 400 K, %age error in I_{ds} decreases. At higher temperature (400 K), the thermal energy enables electrons to overcome scattering caused by impurities, defects or phonons in the DG-CNTFET. Reduced scattering leads to more predictable electron transport resulting in decrease in percentage error of drain current in DG-CNTFET. Also, the thermal energy of electrons increases at 400 K, allowing them to move more freely through the CNT channel. This enhanced mobility results in a smoother and more stable current flow reducing fluctuations and errors in drain current of DG-CNTFET. Thermal energy can help electrons to overcome potential energy barriers at the interfaces and within the DG-CNTFET

structure. As a result, the transistor operates more consistently, leading to decrease in percentage error of drain current in DG-CNTFET.

Further, using nano-TCAD ViDES, investigations have been done regarding the temperature impact on a variety of other parameters including drain conductance, subthreshold swing, ON current, OFF currents and output characteristics.

After plotting DG-CNTFET's input characteristics, I_{ds} vs V_{ds} plot representing the DG-CNTFET's output characteristics has been obtained. DG-CNTFET's output characteristics are used to determine gain and operating point which calculates power dissipation of device.

DG-CNTFET's output characteristics at different temperatures considering various gate voltages are described in figure 4.9.

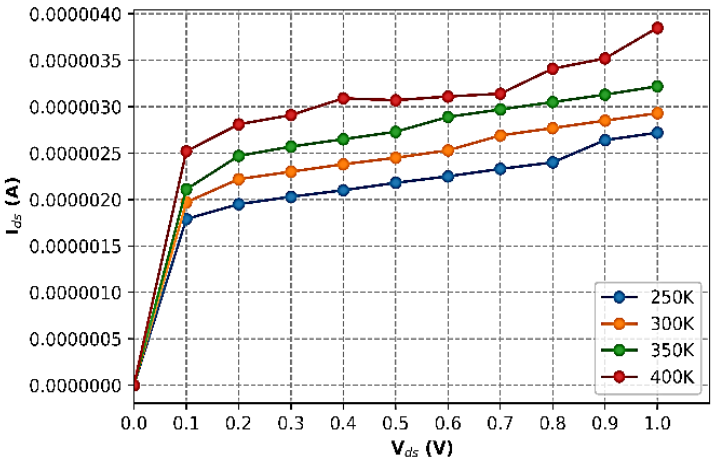


Figure 4.9. DG-CNTFET's output characteristics for different temperatures at V_{gs}=0.4V.

It is described from figure. 4.9. that when temperature (400 K) is raised, drain current rises at low value of V_{gs}. Also, for low values of V_{ds}, drain current is more at higher temperatures (400 K) than it is at lower temperatures (250 K). It is shown that at saturation region, drain current differences at high and low temperatures decreases. In saturation region, I_{ds} is approximately equal at 300 K and 350 K. This is because the conductive channel saturates in the saturation region and no longer connects source and drain regions. As a result, charge carriers are unrestricted in their movement and region of high resistance proportional to drain source voltage (V_{ds}) are present, consequently, this region's resistance will also be proportional to same voltage. The dependence will cancel out as current is defined as voltage per unit resistance, resulting in 'constant' drain current irrespective of temperature variations [138,182].

For various temperature ranges (250 K to 400 K), ON current and OFF current are shown in figure 4.10. Device gets ON when applied voltage (V_{gs}) exceeds threshold voltage (V_{th}) for proposed DG-CNTFET is called DG-CNTFET's ON current.

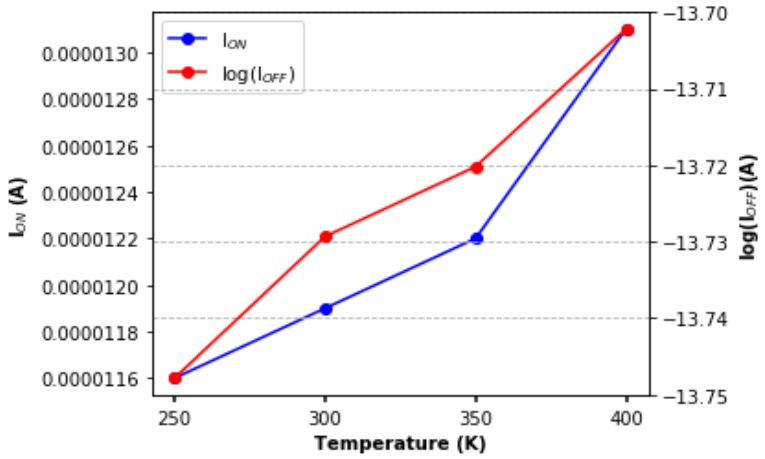
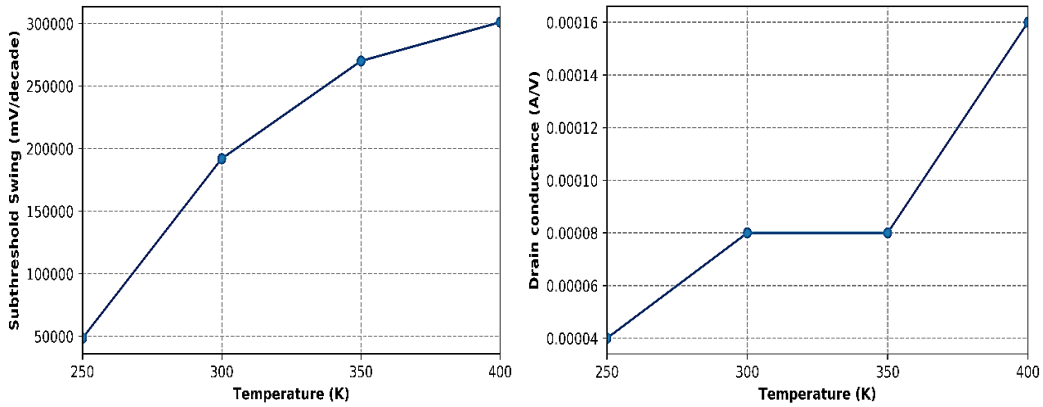


Figure 4.10. ON current at V_{gs} = 0.8 V and V_{ds} = 0.8V & OFF current at V_{gs} = 0V and V_{ds} = 0.8V for variable temperatures of DG-CNTFET.

On increasing temperature from 250 K to 400K, ON current rises. This rise has a constant slope. At V_{gs}=0V and V_{ds}=0.8V, DG-CNTFET's OFF current is also determined at various temperature. Figure 4.10. shows that the OFF current is higher at T=400 K than it is at T=250 K. At 400 K, the OFF current is 1.05 times greater than it is at 250 K. OFF-state charge increases, which causes the OFF current in DG-CNTFET to rise. Temperature rise causes an increase in ON current, but increase in OFF current degrades device performance. Also, when temperature rises, gate control on channel gets declined and therefore decrease in current capability is observed [139]. From Figure 4.10., it can be concluded that a rise in temperature causes a rise in both ON-state current and OFF-state leakage current.

Subthreshold swing and drain conductance are next parameters which need to be examined to determine how temperature affects proposed DG-CNTFET structure's performance. Subthreshold swing variation for DG-CNTFET's variable temperature range is shown in figure 4.11. (a). Change in V_{gs} required to generate one decade increase in I_{ds} known as DG-CNTFET's subthreshold swing [140]. It is a crucial parameter indicating how effectively the transistor can turn ON and OFF. Subthreshold swing is an important parameter used for low voltage and high gain in analog applications.



(a) (b)

Figure 4.11. (a) DG-CNTFET's subthreshold swing (b) Drain conductance at different temperature.

It is clear from figure 4.11. (a) that subthreshold swing increases when temperature increases. Increasing temperature leads to increase in DG-CNTFET's subthreshold swing. For high temperatures (400K), thermal energy increases which cause more electron-hole pairs generation resulting in high value of OFF current and subthreshold swing in device.

Drain conductance represents rate of change of drain current with respect to drain-source voltage when gate-source voltage is held constant. Drain conductance is described as temperature function in figure 4.11. (b). Drain current in ON-state affects drain conductance (g_d). Therefore, increase in ON-current causes a rise in drain conductance. Figure 4.11. (b) clearly shows for different temperatures ranging from 250 K to 400 K, drain conductance rises by 4 times. At high temperature (400K), various thermal effects come into play, such as phonon scattering, which impact the electrical conductance of DG-CNTFET. A higher drain conductance implies a larger variation in drain current for given change in drain-source voltage, which is crucial for amplifying weak signals in electronic circuits under thermal aware environmental conditions.

Nano-TCAD ViDES is used to evaluate effect of temperature on several parameters. The MATLAB results and I-V characteristics obtained in nano-TCAD ViDES simulator exhibit a similar trend. The analytical and simulated model's drain current has a slight variation of less than 10% error. Results illustrate how variations in temperature affect DG-CNTFET's I-V characteristics, ON current, output characteristics, subthreshold swing, OFF current and drain conductance.

4.5. SUMMARY AND CONTRIBUTION OF CHAPTER

In order to examine DG-CNTFET's performance under a variable thermal environmental condition, this chapter focussed on modeling of drain current in DG-CNTFET that is temperature dependent. Using the nano-TCAD ViDES simulator, DG-CNTFET's I-V characteristics have been analysed. The analytical results obtained by writing codes in MATLAB have been compared to simulated results in nano-TCAD ViDES and it has been observed that analytical and simulated results follow similar trend with each other. The analytical and simulated model's drain current has a slight variation of less than 10% error.

It was also studied that how temperature affected other performance parameters of DG-CNTFET such as subthreshold swing, drain conductance, ON current, OFF current and output characteristics. It is concluded in this chapter that drain current rises with rise in temperature for different V_{ds} values. ON current increases with temperature rise which means device has high transconductance and can be used in amplifying circuits. OFF current also increases with the temperature which declines device reliability due to increase in leakage current. Subthreshold swing increases with temperature rise as energy of carriers increase and number of carriers injected into channel are more, leading to high leakage (OFF) current. Four times increase in drain conductance is observed as temperature rises from 250 K to 400 K. As drain conductance depends on drain current in ON state, higher temperatures cause drain conductance to rise. These results can be effectively applied to these devices' design considerations. Device performance under thermal environmental conditions, considering temperature impact on DG-CNTFET's threshold voltage has been evaluated in the next chapter.

PUBLISHED WORK RELATED TO THIS CHAPTER:

[1] Aakanksha Lakhanpal and Karmjit Singh Sandha,"Impact of Thermal-Aware Enviromental Conditions on Double- Gate Carbon Nanotube FET." *Microelectronics Journal*, vol. 114, p. 105146, 2021. (**SCI indexed- Impact Factor - 2.2**)

CHAPTER-5

TEMPERATURE DEPENDENT THRESHOLD VOLTAGE PERFORMANCE ANALYSIS OF DG-CNTFET

This chapter contains a detailed description of performance analysis of DG-CNTFET performance considering temperature-dependent threshold voltage. To evaluate device performance for variable temperatures, temperature impact on DG-CNTFET's threshold voltage has been taken into consideration. Also, several parameters related to channel namely chirality, CNT diameter, dielectric materials with high-k values and thickness of oxide layer have been investigated at variable range of temperature to understand device performance at variety of temperatures.

5.1. INTRODUCTION

One of most essential semiconductor components used in VLSI chips is MOSFET. Integrated circuits (ICs) are made using MOSFETs that provide benefits of compact size, fast speed and low consumption of power. Before end of 2017, size of basic MOS transistor is expected to reduce from several nanometres to less than 10 *nm* [141]. As channel length of semiconductor devices is being decreased to nanoscale, a variety of SCEs including leakage current, band-to-band tunnelling, mobility degradation, threshold voltage fluctuations and DIBL are appearing and becoming more prevalent in semiconductor devices. Because of these limitations, it is not possible to further scale down MOSFET devices to nanoscale. Consumption of power, leakage current and device reliability all get increase as device's gate oxide layer thickness decreases below 1.5 *nm* [141]. Ability to scale down the size of semiconductor devices has been limited and is experienced by silicon-based technology [142]. The semiconductor industry must therefore discover several devices and materials which can eventually be merged with current technologies that are based on silicon. Several devices including FinFETs, Silicon-on-Insulator MOSFETs and nanowire FETs have been developed to reduce SCEs and scaling issues, which have significantly enhanced the device performance [143].

One suitable material for these emerging nanoscale devices is carbon nanotubes (CNTs). Several efforts have been done to enhance device performance and understand the physics of CNTFETs [144-147]. CNTFETs have replaced silicon-based MOSFETs to reduce all

shortcomings and drawbacks, including large leakage currents and threshold voltage roll-off [130, 148-150]. In recent years, significant achievement are obtained in order to overcome scaling challenges to outperform silicon-based MOSFET devices.

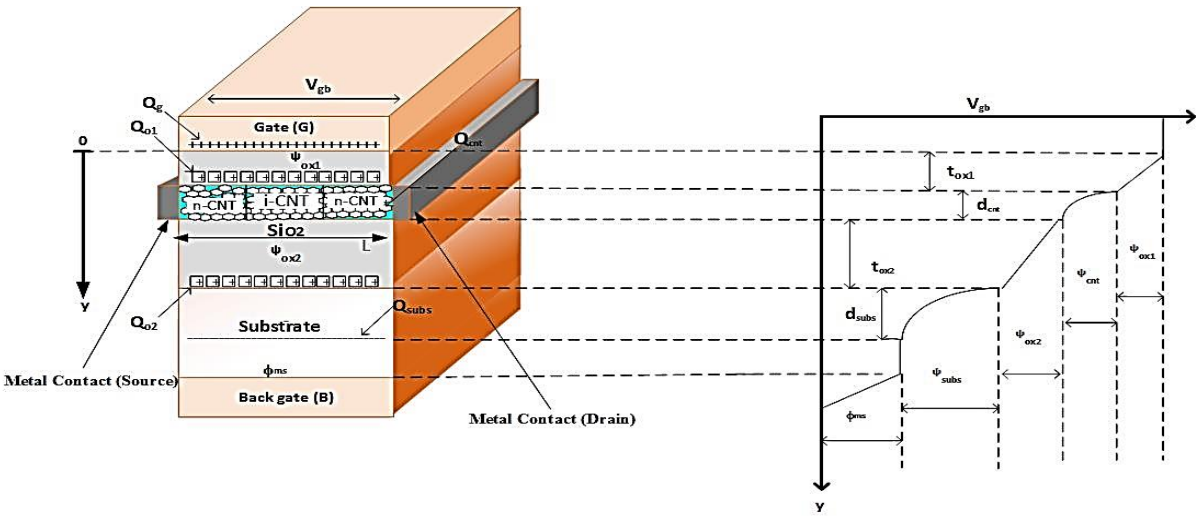
Various low-voltage gadgets, like computers, laptops, cameras, and smartphones, use ultra-low threshold voltages while large supply and threshold voltages are used for devices that must operate at fast speeds. Temperature dependence considering threshold voltage and investigation of various parameters related to channel on threshold voltage are significant from an application aspect in electronic systems and aeronautical applications. Furthermore, to examine DG-CNTFET performance in thermally aware environmental conditions, it is necessary to consider temperature impact on threshold voltage.

5.2. TEMPERATURE DEPENDENT THRESHOLD VOLTAGE OF DG-CNTFET

Minimum voltage needed to turn on device at gate terminal of a FET is known as threshold voltage (V_{th}) [151]. Material's properties, applied voltage, and device's geometry all affect the threshold voltage. In today's semiconductor industry, scaled devices are expected to have low threshold voltages so that they can turn the device ON rapidly. Dissipation due to leakage power increases within these devices. Devices considering high value of threshold voltage are needed for scaled semiconductor industry to avoid leakage current at large scale. A strong contender with a high threshold voltage that may be used to scaled devices for reducing higher leakage mechanisms is the DG-CNTFET.

Considering charge and potential distribution between gate and substrate for DG-CNTFET, this section presents model equations as presented in figures. 5.1. (a) and (b).

Charge distributions of DG-CNTFET are shown in figure 5.1. (a). Q_g stands for gate charge, Q_{cnt} for CNT charge, Q_{01} and Q_{02} for the charge on oxide layers and Q_{subs} for the charge on substrate. Figure 5.1. (b) displays various potential distributions between gate and substrate in DG-CNTFET. Thickness of oxides at gate and substrate are t_{ox1} and t_{ox2} respectively. d_{cnt} and d_{subs} are CNT diameter and substrate diameter respectively for DG-CNTFET.



(a) (b)

Figure 5.1. (a) DG-CNTFET charge distributions (b) DG-CNTFET potential distribution.

Using condition for charge neutrality, charge per unit area is represented by,

$$Q_g + Q_{cnt} + Q_{subs} + \sum_{i=1}^{2} Q_{oi} = 0 \tag{5.1}$$

Charges on oxide layers are represented by Q_{01} and Q_{02}, whereas Q_g stands for gate charge, Q_{cnt} for CNT charge and Q_{subs} for the charge on substrate.

Considering potential balancing condition and Kirchhoff's law, voltage at gate substrate (back gate), V_{gb} is expressed as

$$V_{gb} = \phi_{ms} + \psi_{cnt} + \psi_{subs} + \sum_{i=1}^{2} \psi_{oxi} \tag{5.2}$$

where ψ_{ox1} and ψ_{ox2} represent the potential across oxides, ψ_{cnt} represents the potential across CNT. ϕ_{ms} is work function considering gate to substrate and ψ_{subs} is DG-CNTFET's substrate to back gate surface potential. Work function considering gate to substrate ϕ_{ms} is given as

$$\phi_{ms} = \phi_{mc} + \phi_{cs} \tag{5.3}$$

ϕ_{mc} is work functions difference of metal gate and CNT & ϕ_{cs} is work functions difference between CNT and substrate respectively. Taking into account the back gate, $\psi_{cnt,s}$ denotes

potential at interface between gate oxide and CNT, which is combination of various potentials such as ψ_{cnt}, ψ_{ox2}, ϕ_{cs} and ψ_{subs}. Therefore, eq. (5.2) can also be represented as

$$V_{gb} = \phi_{mc} + \psi_{ox1} + \psi_{cnt,s} \tag{5.4}$$

where potential at interface between CNT and gate oxide while taking into account the back gate is given by $\psi_{cnt,s}$.

Third equation of Maxwell, is used to describe the relationship between electric field and distribution of charge which is given below as [129]

$$\nabla.(\varepsilon E) = \rho_v \tag{5.5}$$

where ε is the material's permittivity, charge per unit volume is ρ_v and E is electric field. For the DG-CNTFET, we apply Maxwell's third equation, taking into account the constant electric field at bottom edge of CNT and along gate oxide region. Eq. (5.5) may be expressed as follows

$$\varepsilon_{cnt} E_{cnt} - \varepsilon_{ox1} E_{ox1} = Q_{01} + Q_{cnt} \tag{5.6}$$

where E_{cnt} and E_{ox1} denotes the electric field between gate oxide and CNT.

Let charge in CNT given at gate terminal is neutralized and can be represented by

$$\Delta Q_g = \Delta Q_{cnt} \tag{5.7}$$

V_{fb} indicates flat band voltage that is applied to compensate band bending at interface of CNT and gate oxide. In this flat band condition, E_{cnt} can be neglected & substituted by a potential gradient. By applying this value to eq. (5.6), we get

$$\varepsilon_{ox1} \frac{d\psi_{ox1}(y)}{dy} = Q_{01} + Q_{cnt} \tag{5.8}$$

After integration of eq. (5.8), substitute the value in eq. (5.4) for gate oxide potential we obtain

$$V_{gb} = \psi_{cnt,s} - \frac{Q_{cnt}}{C_{ox1}} + \phi_{mc} - \frac{Q_{01}}{C_{ox1}} \tag{5.9}$$

where potential considering back gate at interface between CNT and gate oxide is $\psi_{cnt,s}$, ϕ_{mc} is work function difference between metal gate and CNT. C_{ox1}, capacitance between gate and

CNT, assuming that the CNT is a line charge and gate is a planar conducting plate, can be determined as follows [129]

$$C_{ox1} = \frac{2\pi\xi_{ox1}L}{\ln\frac{t_{ox1}+r+\sqrt{t_{ox1}^2+2t_{ox1}r}}{r}} \tag{5.10}$$

Also, C_{ox2} is oxide layer's capacitance between substrate's surface and CNT and is expressed by [129]

$$C_{ox2} = \frac{2\pi\xi_{ox2}L}{\ln\frac{t_{ox2}+r+\sqrt{t_{ox2}^2+2t_{ox2}r}}{r}} \tag{5.11}$$

V_{fb} represents flat band voltage, that is shown as

$$V_{fb} = \phi_{mc} - \frac{Q_{01}}{C_{ox1}} \tag{5.12}$$

When eq. (5.9) & eq. (5.12) are combined, voltage at gate to substrate (V_{gb}) is calculated, which is defined as

$$V_{gb} = \psi_{cnt,s} - \frac{Q_{cnt}}{C_{ox1}} + V_{fb} \tag{5.13}$$

Considering the back gate, $\psi_{cnt,s}$ indicates potential at gate oxide and CNT interface. V_{fb} represents voltage across the flat band. In a carbon nanotube, Q_{cnt} stands for charge carrier concentration.

Concentration of charge carriers in carbon nanotubes has recently been calculated [152] using formula $|Q_{cnt}| = qnc_{nt}L$, where η_{cnt} is carrier concentration & CNT length given by L. Q_{cnt}, i.e., charge on CNT is denoted by

$$|Qcnt| = qLNc\frac{\sqrt{E_F^2 - E_C^2}}{kT} \tag{5.14}$$

where q is electron charge, L is length of CNT, effective density of states is N_c, energy of conduction band (E_c), T stands for the operating temperature, E_F for fermi energy, and k for the Boltzmann constant.

N_c defines density of states of conduction band as

$$N_C = \frac{8kT}{\pi V_{pp\pi} a\sqrt{3}} \tag{5.15}$$

where $V_{pp\pi}$ is energy of carbon-carbon bond, which is 3.033 *eV*, *a* denotes carbon atoms interatomic distance which is 0.142 *nm*, *k* denotes Boltzmann constant & operating temperature is *T*.

Taking into account neutrality conditions of potential and charge for FETs, stated in eq. (5.1) and eq. (5.2), gate to substrate voltage (V_{gb}) of FETs is achieved.

CNT potentials ($\Psi_{cnt,s}$) of source and drain regions mentioned in eq. (5.13) can be represented as [129]

$$\varphi_{cnt,s}(0) = V_{gb} - V_{fb} \tag{5.16}$$

$$\varphi_{cnt,s}(L) = \frac{V_{gb} - \delta I e^{-1} - V_{fb} + \delta m\left(V_{cb} + \Phi_0 + \dfrac{E_c - \Delta E_F - kT}{q}\right)}{1 + \delta m} \tag{5.17}$$

where V_{cb} is potential that is developed between CNT and substrate by terminal voltages at source and drain, V_{fb} is flat band voltage. For channel of length *L*, *m* and δ are represented [129] by

$$m = \frac{\sqrt{\dfrac{2E_C}{kT} + 1} - Ie^{-1}}{\dfrac{2kT}{q}} \tag{5.18}$$

$$\delta = \frac{qLN_c}{C_{ox1}} \tag{5.19}$$

When V_{gb} is given by V_{fb} and ψ_{cnt} is 0, carbon nanotube's surface potential, $\Psi_{cnt,s}$,is determined by ϕ_0 as follows

$$\phi_0 = \phi_{cs} - \frac{Q_{02}}{C_{ox2}} \tag{5.20}$$

and

$$\Delta E_F = kT \ln\left(1 + \frac{N}{n_{cnt,i}}\right) \tag{5.21}$$

The expression given in eq. (5.21) represents the shift in fermi level given by ΔE_F. This shift in fermi level is due to the doping in DG-CNTFET. *N* stands for doping concentration which is taken as molar fraction for DG-CNTFET.

$n_{cnt,i}$ is intrinsic charge carrier concentration which is denoted as

$$n_{cnt} = N_c I \exp(-E_c / kT) \tag{5.22}$$

where N_c stands for effective conduction band density of states and E_c stands for conduction band energy.

Q_{cnt} is the charge on carbon nanotube and can be expressed as

$$Q_{cnt} = - C_{ox1} (V_{gb} - \Psi_{cnt,s} - V_{fb}) \tag{5.23}$$

The value of $\Psi_{cnt,s}$ from eq. (5. 17) is substituted in eq. (5. 23)

$$Q_{cnt} = - C_{ox1} \left(\frac{\delta I e^{-1} + \delta m \left(V_{gb} - V_{fb} - V_{cb} - \Phi_0 - \frac{E_c + \Delta E_F + kT}{q} \right)}{1 + \delta m} \right) \tag{5.24}$$

While calculating DG-CNTFET's threshold voltage considering eq. (5.23) and eq. (5.24), Q_{cnt} is assumed to have a value of 0 at V_{th}. When we put $Q_{cnt} = 0$ in eq. (5.24) we obtain,

$$V_{th} = V_{fb} + \phi_0 - \frac{\Delta E_F}{q} + \frac{E_c}{q} - \frac{kT}{q} - \frac{Ie^{-1}}{m} \tag{5.25}$$

5.3. RELATION OF CNT DIAMETER TO THRESHOLD VOLTAGE

DG-CNTFET's threshold voltage is calculated by controlling CNT diameter. First, we determine the circumferential vector, which is equivalent to diameter of CNT as

$$\overrightarrow{C_h} = n\overrightarrow{a_1} + m\overrightarrow{a_2} \tag{5.26}$$

where *n*, *m* are integers and a_1 and a_2 represents lattice's basis vector.

In DG-CNTFET, CNT diameter is expressed as

$$d = \frac{\sqrt{3} a_{cc} \sqrt{(n+m)^2 - nm)}}{\pi} \tag{5.27}$$

where chiral numbers are given by *n* and *m*, a_{cc} = 0.142 *nm* that describes carbon atoms inter-atomic distance. Threshold voltage (V_{th}) is expressed considering CNT diameter which is defined by

$$V_{th} = \frac{a(V_\pi)}{qd\sqrt{3}} \tag{5.28}$$

where charge on electron is *q*, lattice constant is given by *a* and V_π describes energy between carbon π - π bond =*3.033eV* [129] and *d* is diameter in nanometres.

5.4. QUANTUM CAPACITANCE

(C_q) is one of material's properties of channel. It is necessary to calculate both threshold voltage and gate capacitance.

For CNTFET devices, a detailed investigation has been done [153] to understand how the oxide layer thickness affects capacitance of gate. Fermi level should rise above conduction band edge as quantum well charge increases because semiconductor quantum well's density of state is finite. Quantum capacitance corresponds to the energy needed for fermi level's movement. As stated in [154], quantum capacitance (C_q) decreases as oxide thickness increases.

The inverse and logarithmic relationship between DG-CNTFET's capacitance (C_G) and oxide thickness (t_{ox}) is given below

$$C_G = \frac{2\pi k_{ox}\varepsilon_o}{\ln(2t_{ox}/r)} \tag{5.29}$$

While calculating quantum capacitance, semiconductor CNTs strongly depend on the density of states. Also, the contribution from both electrons and holes is used to determine C_q of semiconducting CNTs and is given by

$$Cq = \frac{4q^2 N_o}{k_B T} e^{-E_g/2k_B T} \cosh[\frac{\mu}{k_B T}] \tag{5.30}$$

where *q* is electron's charge, k_B is Boltzmann constant value, *T* denotes temperature, E_g denotes energy of bandgap, and N_o is fermi level density of states.

5.5. THRESHOLD VOLTAGE PERFORMANCE ANALYSIS IN DG-CNTFET

This section of chapter uses nanoHUB simulation tools to describe simulation results and performance analysis of DG-CNTFET's threshold voltage. An open-access tool named

as nanoHUB has MATLAB scripts for simulating different devices at the deep nanometre regime.

This section describes chirality and CNT diameter effect on DG-CNTFET's threshold voltage. The chirality specifies the particular arrangement of carbon atoms in carbon nanotube's structure. It also affects the electronic properties of CNT, classifying CNT as metallic or semiconducting on basis of structure. Threshold voltage of CNT based FET is influenced by chirality as it affects the electronic band structure. Metallic CNTs tend to have a lower threshold voltage compared to semiconducting CNTs because of their higher conductivity and lower bandgap. Chiral vector (*n*, *m*), determines CNT diameter.

CNT diameter is a significant factor for determining threshold voltage for the following reasons. Energy levels of a CNT depend on diameter and chirality. A smaller diameter CNT may have different energy levels compared to a larger diameter, resulting in variations in threshold voltage. This is important in semiconducting CNTFETs where threshold voltage depends on alignment of energy levels of CNT with source and drain electrodes. Capacitance of gate dielectric and CNT channel play an essential role in calculating DG-CNTFET's threshold voltage. CNT diameter affects its physical dimensions and consequently its capacitance. The gate capacitance determines the amount of charge required to change potential of channel that in turn affects threshold voltage.

Further, this section is categorized into several subsections and using nanoHUB simulation tools, various channel parameters' effect, such as chirality, CNT diameter, and various high-k dielectrics used as gate oxides, on the DG-CNTFET's threshold voltage at temperatures ranging between 225 and 400 K has been investigated. Also, oxide layer thickness's effect on threshold voltage under varied temperatures is studied. These subsections provide an explanation of the obtained outcomes.

5.5.1. Temperature impact on threshold voltage

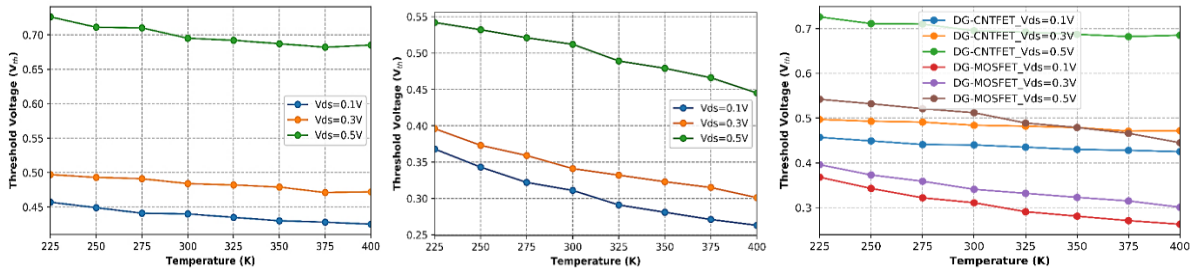
One of most essential parameters for studying the behaviour of semiconductor devices is temperature. It has been established that when temperature increases, threshold voltage of silicon-based MOSFETs decreases, quickly turning ON the device. With rise in temperature for such devices, leakage current increases even more. This is one of most significant phenomenon that arises when silicon-based devices operate at a higher temperatures. But in DG-CNTFET, this isn't the case. The transfer of more charge carriers can be made possible by

CNTs' strong covalent bonds between carbon atoms and they are chemically inert, which enhances drain current and threshold voltage fluctuations in DG-CNTFET [155].

Table 5.1. Effect on threshold voltage at variable temperature for various V_{ds} values.

	DG-MOSFET			***DG-CNTFET***		
Temperature (*K*)	**V_{th} at V_{ds}= 0.1 V**	**V_{th} at V_{ds}=0.3V**	**V_{th} at V_{ds}=0.5V**	**V_{th} at V_{ds}= 0.1 V**	**V_{th} at V_{ds}=0.3V**	**V_{th} at V_{ds}=0.5V**
225	0.368	0.396	0.542	0.457	0.497	0.726
250	0.343	0.373	0.532	0.455	0.493	0.71
275	0.322	0.359	0.521	0.449	0.491	0.711
300	0.311	0.341	0.512	0.443	0.484	0.695
325	0.291	0.332	0.489	0.441	0.482	0.692
350	0.281	0.323	0.479	0.439	0.479	0.687
375	0.271	0.315	0.466	0.435	0.471	0.682
400	0.263	0.301	0.445	0.433	0.472	0.685

As temperature rises from 225 K to 400 K, DG-CNTFET's threshold voltage only varies by 5.25 percent, while that of a DG-MOSFET changes by 28%. Under thermal environmental conditions, DG-MOSFET exhibit more variations than DG-CNTFET. This is due to the reason that because of their unique electronic properties, CNTs are less susceptible to temperature-induced variations in threshold voltage. CNTs have one-dimensional structure with high density of electronic states, which results in a relatively constant bandgap over a wide temperature range. This inherent property helps to maintain a stable threshold voltage in case of DG-CNTFET. In DG-CNTFETs, due to their one-dimensional structure, there is less opportunity for phonon scattering to affect carrier mobility, leading to more stable device characteristics over temperature variations than the DG-MOSFETs. DG-CNTFET performs better in applications where it is necessary to design the device taking into account the thermal environment.



(a) (b) (c)

Figure 5.2. Variation in threshold voltage for (a) DG-CNTFET (b) DG-MOSFET and (c) combined results for different V_{ds}, taking into account different temperatures.

Threshold voltage variations in DG-CNTFET, DG-MOSFET, and the overall result of figure 5.2. (a) and figure 5.2. (b) at varying temperatures from 225 K to 400 K for V_{ds} = 0.1V, 0.3V, and 0.5V, respectively, are described in figures 5.2. (a), (b), and (c). As seen in figure 5.2 (a), there has been a little decrease in V_{th} on rising temperature from 225 K to 400 K because of the presence of several DG-CNTFET's heat dissipation mechanisms. This is because heating is reduced. The heat distribution of DG-CNTFET devices is non-uniform, resulting in reduced heat production inside channel and maximum heat near source and drain sides of channel. Reduced heating effect also lowers leakage current, which reduces power loss in device. Therefore, DG-CNTFET's threshold voltage is less affected by temperature increase. According to figure 5.2. (b), threshold voltage of DG-MOSFET is much lower than DG-CNTFET at higher temperatures, which has a greater impact on device parameters and characteristics. Figure 5.2 (c) displays overall results of both DG-CNTFET and DG-MOSFET. Temperature impact on DG-CNTFET's and DG-MOSFET's threshold voltage is shown in table 5.1. Transport mechanisms of carriers in CNTs and silicon are different. CNTs support ballistic transport for shorter channel lengths, meaning that carriers can move without scattering. The ballistic transport can lead to less sensitivity of threshold voltage to temperature changes than diffusive transport, which is more common in silicon-based devices. Due to minor reduction in V_{th} with increasing temperature and when compared to DG-MOSFET, DG-CNTFET has excellent thermal stability. [156-158]. Table 5.2. shows a comparison for threshold voltage at different temperature with the available results in literature.

Table 5.2. DG-CNTFET's threshold voltage comparison for variable temperatures with results available in literature at V_{ds}=0.5V.

Temperature (K)	**Threshold voltage (V)**	**Threshold voltage (V) [159]**
225	0.726	0.62
250	0.711	0.55
275	0.71	0.54
300	0.695	0.52
325	0.692	0.48
350	0.687	0.43
375	0.682	0.42
400	0.685	0.41

From table 5.2. it is described that when temperature increases from 225 K to 400 K, threshold voltage of DG-CNTFET decreases. The similar trend for obtained threshold voltage is seen when we compare obtained results with threshold voltage as available in existing literature. As the temperature rises, electrons in valence band acquire enough thermal energy to transfer into conduction band. Conduction band electron density increases along with conductivity and resistivity decreases.

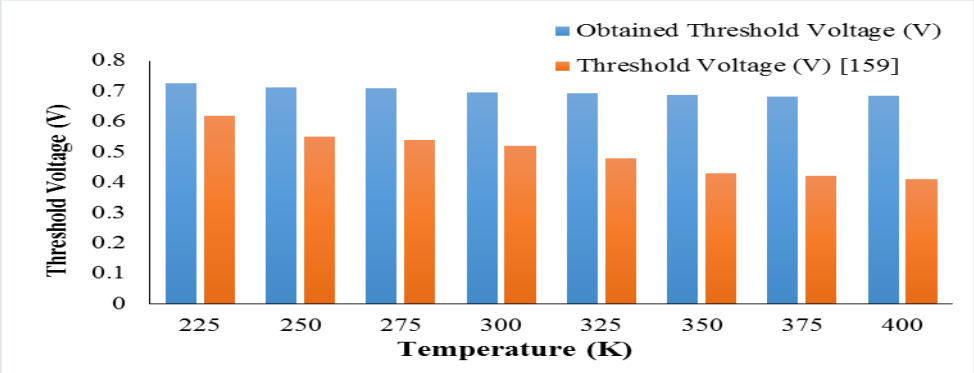


Figure. 5.3. Comparison of obtained DG-CNTFET's threshold voltage with results available in literature.

The results obtained for DG-CNTFET's threshold voltage are shown in figure. 5.3 along with a comparison to results that are currently available in the literature. The figure makes it clear that the obtained threshold voltage is slightly higher than threshold voltage available in existing literature. The OFF-state leakage current (I_{OFF}) is decreased by utilising a high threshold voltage in CNTFETs. In OFF state (gate-source voltage below threshold value) of transistor, I_{OFF} stands for the current that travels from source to drain. I_{OFF} can be considerably reduced by utilising a high threshold voltage which reduces power consumption in digital circuits. This is important in applications that use low power or energy.

The choice of threshold voltage should align with the specific application and performance requirements. Low-threshold voltage CNTFETs may be more suitable in certain situations, particularly for high-speed digital circuits where fast switching is required. While selecting the proper threshold voltage for CNTFET-based designs, designers need to balance a number of parameters including power consumption, speed and compatibility.

5.5.2. CNT chirality's impact on threshold voltage

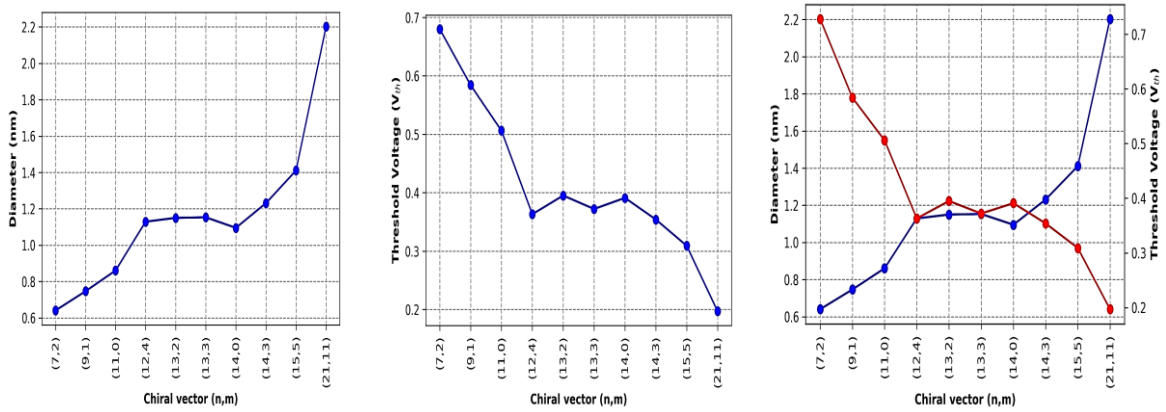
The property of carbon nanotubes called chirality determines whether a CNTFET is metallic or semiconducting in nature. It is based on how atoms are arranged in nanotube of CNTFET.

(n,m) integer pair represents the chirality. To examine the CNT diameter and chirality impact on DG-CNTFET's threshold voltage, eq. (5.28) describes the relation between diameter of CNT and DG-CNTFET's threshold voltage. This equation makes it clear that CNT diameter and threshold voltage are inversely related. DG-CNTFET's threshold voltage can be controlled by varying chiral vector and CNT diameter [160]. Table 5.3 shows a variety of chiral vector combinations.

Table 5.3. DG-CNTFET's threshold voltage for different chiral vectors.

Chiral vector(*n,m*)	***nm value***	***(m+n)^2 value***	***Diameter (d)***	**Threshold voltage (*V*)**
(7,2)	14	81	0.6403	0.680
(9,1)	9	100	0.7463	0.584
(11,0)	0	121	0.8605	0.506
(12,4)	48	256	1.129	0.363
(13,2)	26	225	1.15	0.395
(13,3)	39	256	1.153	0.372
(14,0)	0	196	1.095	0.391
(14,3)	42	289	1.231	0.354
(15,5)	75	400	1.4104	0.309
(21,11)	231	1024	2.203	0.197

Different sets of chiral vectors for DG-CNTFET are described in table 5.3. The sum $(n+m)^2$ and product (nm) of a specific set of integer pairs of chiral vector are also taken in order to analyze threshold voltage trend considering chirality.



(a) (b) (c)

Figure 5.4. Chiral vector (*n,m*) effect on DG-CNTFET's (a) diameter (b) threshold voltage and (c) overall results when both are taken into account.

DG-CNTFET device's threshold voltage and CNT diameter variation considering various sets of integers in chiral vector is defined in figure 5.4. (a) and 5.4. (b). Figure 5.4 (c) shows chirality effect on DG-CNTFET's threshold voltage and CNT diameter. Figure 5.4. (c) shows that the threshold voltage in DG-CNTFETs for various sets of integer chiral vectors decreases as the CNT diameter increases. Since DG-CNTFET's threshold voltage is inversely proportional to (n, m) pair of chiral vectors, it is shown in eq. (5.28) that the value of threshold voltage has decreased. Also, table 5.3 illustrates how the diameter of the carbon nanotube rises in accordance with an increase in sum of product of integer pair of chiral vector, or $(n+m)^2$, which in turn enhances DG-CNTFET's thermal conductivity and consequently decreases device's threshold voltage. In DG-CNTFET, a large value of chiral angle results in much larger thermal conductivity than a smaller chiral angle [161].

5.5.3. Diameter's impact on threshold voltage at variable temperatures

Eq. (5.28) can be used to determine the CNT diameter's effect on DG-CNTFET's threshold voltage. Also, CNT diameter variation effect on DG-CNTFET's threshold voltage at varying temperatures is described in eq. (5.25).

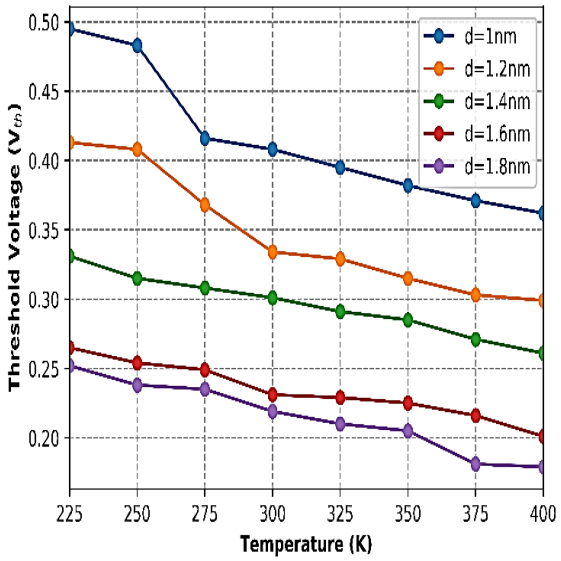


Figure 5.5. Diameter effect on DG-CNTFET's threshold voltage at different temperature range.

The effect of varying the CNT diameter on DG-CNTFET's threshold voltage for variable temperatures is shown in figure 5.5. When temperature is increased, it has been found that threshold voltage decreases as nanotube diameter increases. Table 5.3. also shows that the square of $(n+m)$ increases.

Further, DG-CNTFET's threshold voltage is inversely related to CNT diameter. Therefore, variations in CNT diameter have an impact on van der Waals interactions that raises thermal transport near contact. Size of nanotube gets deformed when van der Waals forces and carbon atoms energy change, which has an impact on device's thermal conductivity. Depending on CNT diameter, different gate voltages can be used to turn ON the DG-CNTFET.

Bandgap energy of a CNT in DG-CNTFET is inversely proportional to CNT diameter. Larger-diameter CNTs have smaller bandgap, which means they require less energy (lower voltage) to transition from valence band to conduction band. As temperature increases, thermal energy in the system allows more electrons to access the conduction band, effectively reducing threshold voltage that is needed to turn ON the DG- CNTFET.

5.5.4. Oxide thickness's impact on threshold voltage at variable temperatures

One important property for channel material is quantum capacitance (C_Q). To calculate the gate capacitance and threshold voltage knowledge of quantum capacitance is necessary.

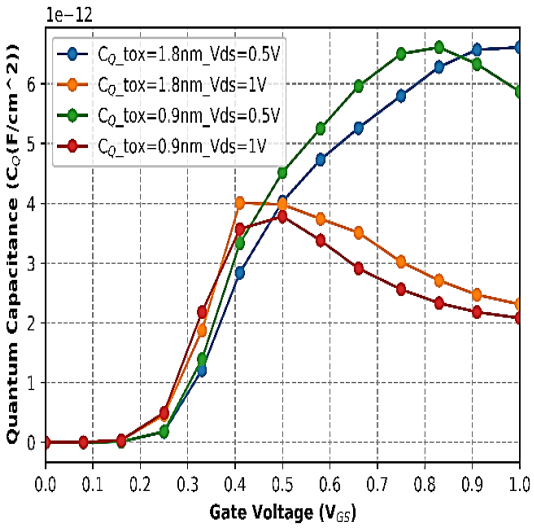


Figure 5.6. DG-CNTFET's quantum capacitance at variable oxide thickness for different drain voltage.

The variation in DG-CNTFET's quantum capacitance at t_{ox} =0.9 *nm* and 1.8 *nm* for different V_{ds} values is depicted in figure 5.6. Figure makes it clear that DG-CNTFET's quantum capacitance decreases with reduction in oxide thickness that lowers leakage current & enhances DG-CNTFET gate control, improving the device performance. Lower value of quantum capacitance enhances propagation delay & decreases leakage current, which enhance device performance. As a result, as shown in figure, a decreased capacitance of gate is observed with

oxide thickness reduction, which also impacts threshold voltage as described in eq. (5.10) and eq. (5.25).

As the oxide thickness decreases in DG-CNTFET, electrostatic coupling between gate electrode and CNT channel becomes stronger. This increased coupling leads to stronger quantum confinement effects in the carbon nanotube of DG-CNTFET. Quantum confinement results in discrete energy levels for electrons in CNT. As oxide layer becomes thinner in DG-CNTFET, these discrete energy levels become more pronounced, leading to an increase in quantum capacitance in device.

A thinner layer of oxide reduces dielectric screening effect between gate electrode and CNT channel in DG-CNTFET. This means that electric field of gate electrode penetrates more effectively into CNT, affecting the quantum capacitance. With a thinner oxide layer, gate voltage has a stronger influence on charge distribution within CNT, leading to an increase in quantum capacitance.

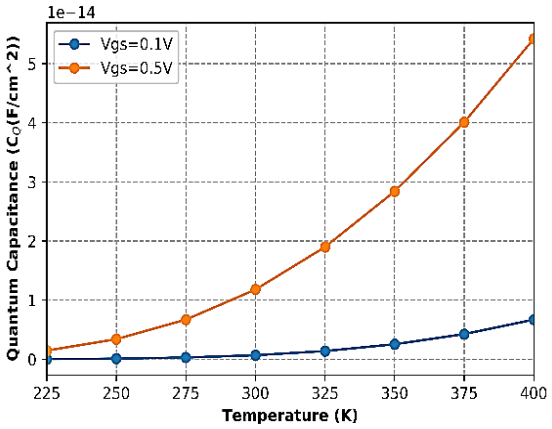


Figure 5.7. DG-CNTFET's quantum capacitance at variable temperature for different values of V_{gs}.

Quantum capacitance can lead to threshold voltage shift in DG-CNTFET. This shift is due to the discrete energy levels in CNT, which affect the way electrons respond to variations in gate voltage. This can make the transistor turn ON or OFF at slightly different gate voltages. Quantum capacitance is temperature-dependent, as it is closely associated with electronic density of states. Changes in temperature can influence electrons' energy distribution in CNT, affecting the quantum capacitance and consequently DG-CNTFET's threshold voltage. DG-CNTFET's quantum capacitance varies with temperature variations as shown in figure 5.7. According to figure 5.7., the quantum capacitance of DG-CNTFET increases as temperature rises. The reason for this increase is that when temperature rises, electron

concentration improves, ultimately leading to an increase in quantum capacitance. As a result, in DG-CNTFET, temperature rises lead to an increase in quantum capacitance. Moreover, it rises ratio of quantum to insulator capacitance. It ultimately enhances device's performance by affecting leakage current.

5.5.5. Threshold voltage effect of high-k dielectric material at different temperatures

Due to electrical and thermal stability between *Si* and SiO_2, silicon dioxide (SiO_2) has been used as gate dielectric in MOSFET devices. SiO_2 thickness and length of gate have been scaled in such devices to reduce area of chip and achieve fast speed in ICs. When the gate dielectric is thin, tunneling takes place, increasing gate leakage and device power dissipation.

High-k values of dielectric materials are used to overcome tunneling. By substituting a high-k value of dielectric material for silicon dioxide as gate dielectric, leakage effects are reduced which increases gate capacitance and is understood from eq. (5.29).

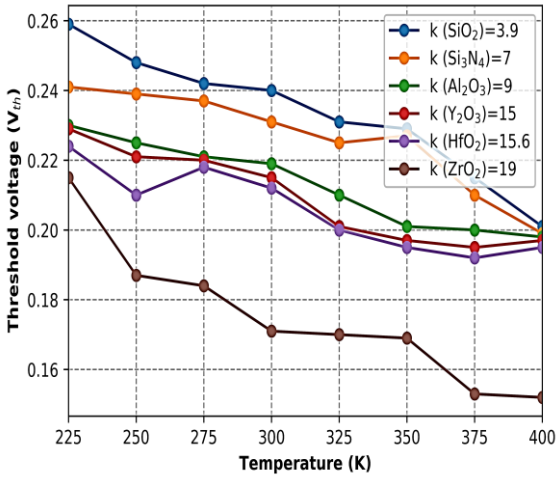


Figure 5.8. DG-CNTFET's threshold voltage for different high-k value materials at variable temperature.

Threshold voltage effects for different high-k values of dielectric materials used in DG-CNTFETs operating at temperatures between 225 K and 400 K is shown in figure 5.8. Threshold voltage effect for several high-k values of dielectric materials used in DG-CNTFETs operating at temperatures between 225 K and 400 K is described. As illustrated in figure, threshold voltage with high value is achieved for lower-k oxide materials namely SiO_2 and Al_2O_3. Eq. (5.10) and eq. (5.11) show clearly why DG-CNTFET's threshold voltage increased in this manner. Gate capacitance of DG-CNTFET increases as oxide material's dielectric (k) value increases, which further decrease the threshold voltage and enabling faster switching and also lowering device's heat dissipation.

5.6. SUMMARY AND CONTRIBUTION OF CHAPTER

This chapter examined the impact of various channel parameters at a variable range of temperature on DG-CNTFET's threshold voltage. Using nanoHUB simulation tools, the impact of different temperatures (225 K to 400 K) on variable parameters related to channel, including chirality, CNT diameter, quantum capacitance and high-k dielectric, has been investigated. This has been extended to DG-CNTFET's threshold voltage.

Also, it was determined in performance analysis section of this chapter that threshold voltage of DG-CNTFETs changes with variations in CNT chirality and diameter which has an impact on DG-CNTFET's thermal conductivity. Further, it was examined that decrease in DG-CNTFET's quantum capacitance would enhance device's propagation delay. Faster switching rates and less dissipation of power are made possible by oxide material in DG-CNTFETs through the use of higher k-dielectric materials, according to results shown in this chapter.

Further, this chapter included a study of DG-CNTFET and DG-MOSFET threshold voltages at different temperatures. A small decrease in DG-CNTFET's threshold voltage at different temperatures was achieved, making it more appropriate for applications where thermal environmental conditions must be taken into account for design purposes because of unique property of thermal stability found in CNTs in comparison with DG-MOSFET.

PUBLISHED WORK RELATED TO THIS CHAPTER:

[1] Aakanksha Lakhanpal and Karmjit Singh Sandha, "Impact of channel parameters on threshold voltage at variable temperatures of Double gate CNTFET." *Micro and Nanostructures*, vol. 164, p. 105146, 2022. (**SCI indexed- Impact Factor – 3.1**)

CHAPTER 6

STATIC RANDOM ACCESS MEMORY (SRAM)

In this chapter, developed optimized CNTFET structure has been used as an application in VLSI area to design and evaluate 6T SRAM cell performance in HSPICE tool for various technology nodes. This chapter also presents a comparative analysis of 6T SRAM cell using CNTFET and CMOS technologies to analyse SRAM cells performance considering performance parameters namely power dissipation, propagation delay and power delay product at various technology nodes. Also, to study temperature impact, CNTFET-based 6T SRAM cell performance for designing devices with low power has been evaluated for a number of performance parameters, including read and write power dissipation, propagation delay and power delay product (PDP) at variable technology nodes. Further, introduction of Static Random Access Memory (SRAM) cell, brief overview of memory and its types are presented in this chapter. This chapter further includes the memory hierarchy, types of SRAM cell and working of SRAM. Limitations of MOSFET-based SRAM cell is also explored in this chapter.

6.1. INTRODUCTION

From past few years, various advancements are still going with a faster pace. Prior to the inventions of computers, computing used to be the hardest task. When the computing task was made easy, several issues such as delay, speed of device and power consumption came into existence which are also increasing now a days. Earlier, the focus of semiconductor industry was only on the optimized speed.

The advancement of technology, in various applications namely mobile industry, biomedical devices and many more, demands a circuit and device which consumes minimum power and are also energy efficient. SRAM comprises of transistors which are highly useful now a days in various applications due to its efficient computing ability.

Earlier, the VLSI industry focused on optimizing the speed in various fields which include video graphics and video compression. This solved the purpose of entertainment with high-speed devices. But for various portable devices such as smart-phones and tablet computers, limitation for power dissipation occurs. As the various wireless devices are emerging in semiconductor consumer market, the limitation of power consumption must be solved so as to make the devices energy-efficient.

So, it is very important to minimize the total consumption of power and optimizing device's speed keeping in mind the minimum reduction in size and battery life of device. Therefore, low- power and high-speed design is the most important factor for the system – on –chip design in portable devices.

SRAM cells with six transistors are one of most commonly used circuit components in modern system- on-chip (SoC) solutions. It is the most often used alternative in on-chip memory solutions because of its fast speed and ability to integrate with CMOS digital circuitry.

6.2. MEMORY

In many different fields including science, entertainment, engineering, business as well as in education, computers are required to carry out a number of tasks. They are capable of performing a predetermined set of activities without the need for human interaction, working at fast speeds and handling huge volumes of data with excellent accuracy. Data processing is handled by the CPU, which then uses output devices to display the results. Memory is needed by the CPU to process the data, store the output and hold subsequent results.

Memory can be defined as the device which is used to store data and instructions so that computer can access these quickly. These devices can be used to write, hold and read the data. The information can be either temporarily or permanently stored in the device. Memory is described as the most important component of computer. Computer performance is mainly determined by memory and CPU.

6.3. MEMORY HIERARCHY

A computer not only uses a single memory but various types of memories. Memory hierarchy divides memory into a set of levels based on the response time. An embedded system must be both fast and affordable. The choice and amount of a variety of memory types are important in such situations. As we already know, different memories operate at varying speeds, cost and penalty for die area. As high-speed memory has a high price, they are only used for a small number of high priority tasks. The slower and less expensive memories are typically used in large quantities for general-purpose applications.

There are four levels of memory hierarchy which are as follows and shown in figure 6.1.

1. Internal Processor Memory
2. Primary Memory

3. Secondary Memory
4. Tertiary Memory

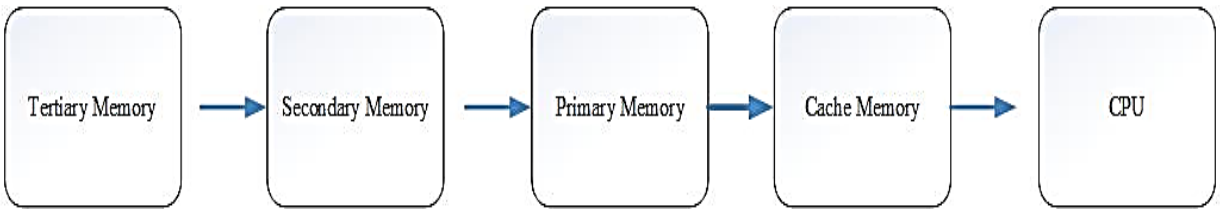


Figure 6.1. Memory Hierarchy [171].

Either CPU (processor) or a special fast bus are used to connect to internal processor memory. Cache memory and special registers are two common types of internal memory that CPU can access directly. This memory is used to temporarily store information and commands that CPU is currently processing. Although processor memory is fastest of all memories, it is also priciest. As a result, only a very small portion of internal processor memory of computer system is used. It aims to close speed limitations between processor and main memory.

Suppose, it is necessary to process a set of instructions that are kept on a hard disk. The instructions are already on the third level of hierarchy and are saved on a hard drive. From here, the second stage, which is the main memory, loads the operating system of computer system (let's say Windows). As soon as processor is prepared to handle the instructions, they remain there. Once instructions are ready, a selected number of set of instructions are relocated to the cache memory. There may be various levels of cache memories, depending on the application and system cost. The instructions are then divided into a number of units that are transferred to the processor registers for immediate processing. The output will return to the hard drive in the same hierarchy.

6.4. MEMORY CATEGORIZATION

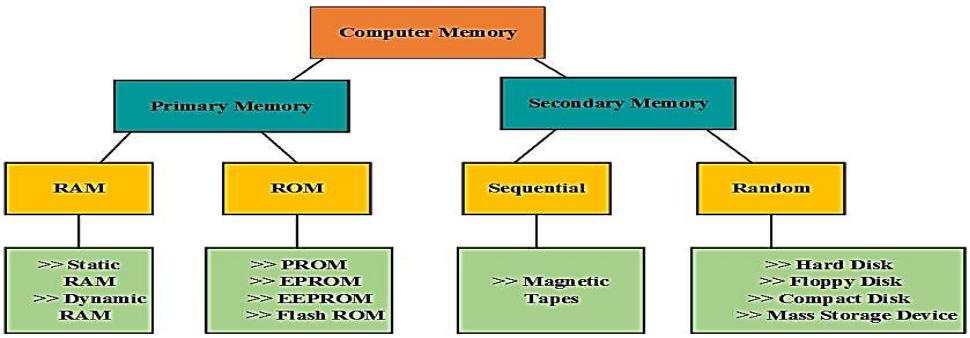


Figure 6.2. Memory Categorization [162].

Computer memory is space within computer's storage where instructions needed for processing data are kept and data to be processed is stored. As seen in figure 6.2, there are two basic categories of computer memory namely primary memory and secondary memory [162].

6.4.1. Secondary/ Non-volatile memory

Non-volatile memory is another term used for secondary memory. Data can be stored in device permanently. They are typically the slowest type of computer memory with high storage density and are typically cheaper to manufacture. These are further categorized based on how data is stored and accessed from memory as follows [162].

6.4.1.1. Sequential

In sequential type of secondary memory, data is accessed or written in a sequential manner. Every block of data is accessed, i.e., written or read from memory locations which are sequential in nature. One of the examples of sequential secondary memory is magnetic tape.

a) Magnetic Tapes

Magnetic tape resembles the tape as seen on music cassettes in appearance [163]. It is a magnetically coated plastic tape. On the surface of material, small portions that are magnetised and demagnetized contain the data. Surface's demagnetized portion corresponds to bit value '0' whereas magnetized portion corresponds to bit value '1'. Although magnetic tapes come in a variety of sizes, main differences among magnetic tape units are speeds at which tape is moved by read/write head and density of recording on tape. The recording density of the tape refers to how much information and number of binary digits that can be accommodated on an inch of linear tape.

6.4.1.2. Random or Direct

When a computer has direct or random access, it can go directly to location where the user's required data is stored. Magnetic disks and optical disks are the two types of direct access storage that are used most frequently. The information is kept in these devices as a numbered sequence of blocks. Computer-based directory assistance operations and airline reservation systems applications are perfect examples for the direct access method. There is no set pattern for the data requests in these situations.

Some of the examples of random memories are Compact Disks, Mass Storage Devices, Hard Disk Drives, and Floppy Disk Drives.

a) Hard Disk Drives

Main computer storage device is hard disk. It comprises of a stack of disc platters coated with protective layers and a magnetic coating made of glass or an aluminium alloy substrate [164]. They are firmed sealed to stop dust particles from entering the platters that cause head crashes. A hard disk can store a lot of data that can be internal or external (removable or fixed). The storage capacity has grown significantly since the day the hard disks were first released. Access time is used to measure the speed of hard disks. A hard disk drive that has a lower access time is faster than the one that has a higher access time.

b) Floppy Disk Drives

A flat, spherical sheet of Mylar plastic covered in ferric oxide is called a floppy disk. This contains minute particles that can hold magnetic field and enclosed in plastic cover for protection. Using floppy disk drive (FDD), data may be read from and written to a computer on rotating this removable disk. FDD handles all fundamental operations of a disk [165]. The magnetic orientation of the particles is changed by the read/write head of disk drive. Particle orientation in one direction indicates '1' whereas particle orientation in other indicates '0'.

In past, personal computers used floppy disks for transmitting data between machines, distributing software and creating small backups. Floppy diskettes are compact, affordable, widely accessible and simple to store. These have long shelf life when stored in proper manner. Further, these have a write-protect capability that let users to prevent writing to a diskette. The user must slide a lever towards the edge of disks, exposing a hole to write-protect a diskette. The portability of floppy disks is its main benefit.

c) Compact Disks

Most common and least priced kind of optical disk is compact disk which was created exclusively to store music in early days. A CD is a metal disk which is silver coloured, shiny and 12 *cm* in diameter. Three layers typically constitute an optical disk namely a polycarbonate base layer that allows light to propagate, an aluminium layer and an acrylic protective layer on top. CD pits are typically 0.15 microns in depth, 0.83 to 3 microns in length, and 0.15 microns in width. One track on a CD spiral outward from the middle to the edge. The track would extend for three and a half miles if 12 *cm* CD was considered. Each sector on single track is of equal length and same density [166]. These unique contiguous sectors are used for storing and keeping files.

d) Mass Storage Devices

Large amount of data is stored on the system using mass storage devices. These digital data storage memories operate at very high speeds. Some of its examples include solid state drives and SD cards.

6.4.2. Primary Memory/Volatile Memory

Volatile memory is another name for primary memory because data cannot be permanently stored in the device. To store data in memory, user can choose any section of primary memory but the data cannot be retained there permanently. The other name of primary memory is volatile memory. The data gets lost when power supply from primary memory is removed or disconnected.

6.4.2.1. Read Only Memory (ROM)

As the main memory of computer is blank and volatile in nature so it needs some special instructions for the start-up operations. For performing start-up operations and transferring control to the operating system, a particular special chip must contain some instructions (special boot programmes). The start-up instructions are stored on a special chip known as ROM.

Its non-volatile nature suggests that when power is switched off, its contents are retained. ROM is more secure and safer than RAM because one can only read and use instructions and data stored within and these cannot be altered. Data and instructions can only be written into ROM once. A ROM chip cannot be rewritten or reprogrammed once it has been set up. The ROM chips, which are found in the most of small electronic devices are extremely reliable which can utilize very little power and contains all programming required for device operation. Types of Read- Only-Memory (ROM) are as follows:

a) Programmable Read –Only Memory (PROM)

It is very difficult, time consuming and expensive process to produce a ROM chip from the scratch. So, PROM has been created that can be programmed. Blank chips of PROM can be purchased at a low cost and users can programme these using a special device known as a PROM-programmer. On other hand, once a PROM is programmed, its data cannot be altered. Similarly, to other ROMs, PROM is non-volatile memory.

b) Erasable Programmable ROM (EPROM)

An EPROM can be repeatedly erased and reprogrammed, just like a PROM. It can be erased by simply exposing device to a strong UV light source for a certain period of time. The EPROM eraser will completely erase the EPROM and it is not selective. Despite being more expensive than PROM, EPROM is more helpful because it can be reprogrammed.

c) Electrically Erasable Programmable ROM (EEPROM)

This form of ROM is written using slightly higher voltage after being erased with an electrical charge. In contrast to erasing the entire chip using ultraviolet light, EEPROM may be erased one byte at a time. Reprogramming is hence slow but complex. Further, no additional specialized equipment is needed while altering the contents. These chips are frequently used for keeping programmable instructions in printers and other devices because they can be altered without opening a casing.

d) Flash Read Only Memory (ROM)

Also referred to as flash memory or flash BIOS, flash ROMs are a kind of constantly powered non-volatile memory that allow for block-based programming and erase/reprogramming operations. A form of EEPROM that, unlike flash memory, can be erased completely and then rewritten completely at byte level. The BIOS and other control codes of a personal computer are usually retained in flash memory. Rather than writing data in bytes, flash memory can be written in blocks when BIOS needs to be altered or rewritten that makes the update operation simpler. Digital mobile phones, digital cameras and other devices all use flash memory.

6.4.2.2. Random Access Memory (RAM)

Because memory locations are selected at random, primary storage is known as random access memory (RAM). It uses memory to execute both read and write operations. Information stored in primary memory is permanently lost as power is switched off [168].

Therefore, RAM is volatile in nature. RAM is categorised into two kinds namely dynamic random access memory (DRAM) and static random access memory (SRAM)

a) Dynamic Random – Access Memory (DRAM)

As long as there is power, data continues flowing in and out of memory. DRAM needs to be refreshed often to keep data, unlike SRAM. To do this, memory is placed on a refresh circuit that rewrites data many hundred times per second. As DRAM is portable and inexpensive, so,

this can be used for system memory. A DRAM cell consists of one transistor, capacitor, address line, bit line and ground as shown in figure 6.3. DRAM needs expensive, complex sensing and refresh circuitry [168-169]. The data bits of DRAM are stored using a capacitive arrangement. Data corruption caused by capacitor charge leakage is therefore a major issue.

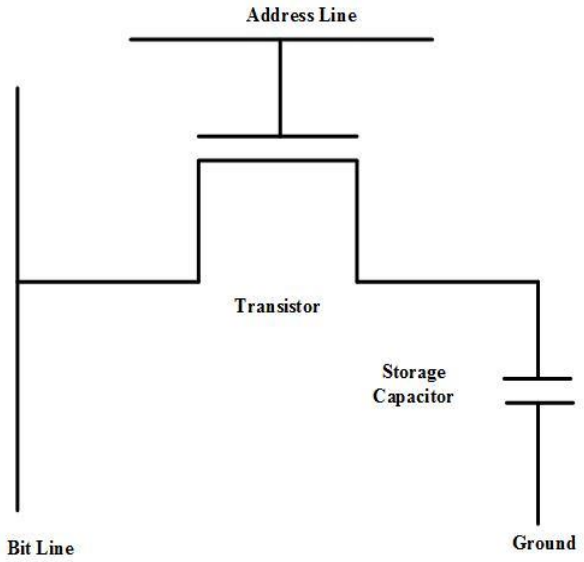


Figure. 6.3. DRAM structure [170].

DRAM memories use a lot of power when they are inactive due to the inherent problems with charge leakage and continuous refreshing, making them unsuitable for embedded system applications that must operate under low power conditions. The capacitors also have a significant charging and discharging period that restricts the performance of DRAM memory, making it generally slower than SRAMs.

b) *Static Random Access Memory (SRAM)*

Term ‘static’ defines that memory contents are retained as long as power is supplied. However, the data is lost as soon as the power turns off. As opposed to read-only memory, SRAM is now a volatile memory. SRAM does not require periodic ‘refreshing’ (pulsing electricity through every memory cell). Although significantly more expensive than DRAM, it is highly fast. As SRAM has fast speed, it is commonly used as cache memory. The next sections of this chapter provide a detailed description of SRAM cell.

6.5. STATIC RANDOM ACCESS MEMORY (SRAM)

A RAM which stores each memory bit considering a flip-flop circuitry is SRAM as shown in figure 6.4. Loss of data occurs whenever power is disconnected, so SRAM is volatile in nature.

In the presence of power, the data gets retained permanently in SRAM, while in DRAM, the data gets destroyed in seconds so the data must be periodically refreshed. SRAM is used more often for the cache and internal registers of a CPU as compared to DRAM, which is often used as a computer's main memory. Compared to DRAM, SRAM is faster but it costs more in terms of silicon area and cost [172].

SRAM cell removes the drawback of DRAM as it does not involve the use of capacitors and there is no need for the refreshing circuit in SRAM. A SRAM cell consist of six transistors. Out of these six transistors, two are access transistors and other four transistor makes the circuit for SRAM cell. This reduces the memory density and is expensive to use. It consumes less power and is reliable to use.

Therefore, based on the applications, SRAM cell is used in various devices. It is used between DRAM and CPU clocks in today's modern computers.

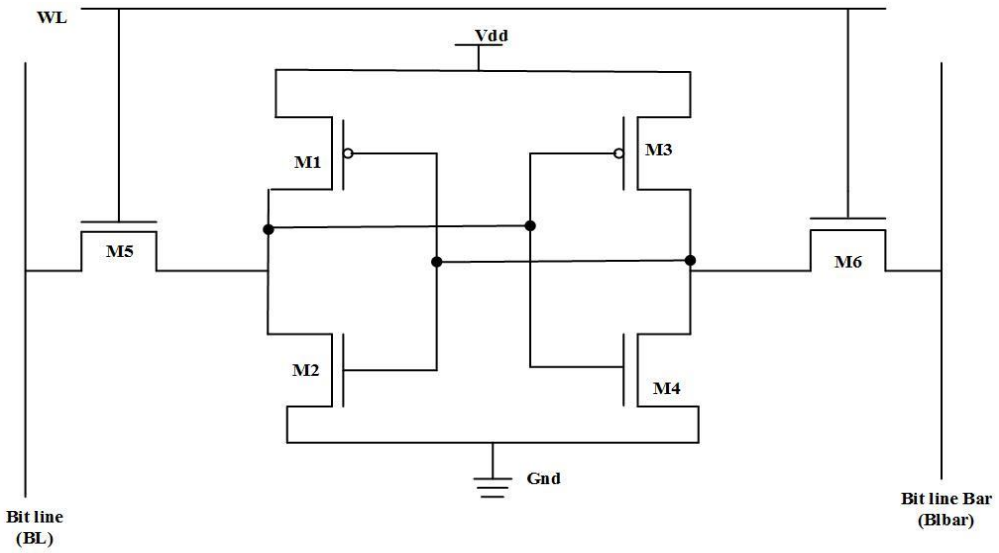


Figure 6.4. Structure of basic 6T SRAM cell

6.6. TYPES OF SRAM

SRAM has been divided into three types on the basis of functionality, data retention and number of memory cells used.

6.6.1. On basis of functionality

On basis of functionality, SRAM has been classified into two types namely Asynchronous and Synchronous SRAM [173].

6.6.1.1.Synchronous SRAM

Synchronous SRAMs are those devices that get sync with a clock signal from outside the system. Only specific clock states will cause the device to read and write information into memory. Clock's switching point, or when it moves from LOW to HIGH (‘rising edge’) or HIGH to LOW (‘falling edge’), is particular condition of interest. Synchronous SRAM uses a clock signal to coordinate read and write operations, making them suitable for high-speed data processing in synchronous systems.

6.6.1.2.Asynchronous SRAM

The asynchronous SRAM is not dependent on the state of a clock. These SRAM devices operate asynchronously, meaning they don't rely on a clock signal for read and write operations. As soon as it receives the command to do so, it will start reading information from or writing information into the memory. They are commonly used in cache memory and other applications where access speed is crucial.

6.6.2. On basis of retaining the data

On the basis of data retention, SRAM has been classified into two types namely volatile SRAM and non-volatile SRAM.

6.6.2.1. Volatile SRAM

Volatile SRAM is one in which data losses, when power is switched off. Volatile SRAM is often used for storing data that needs to be accessed quickly by the CPU, such as cache memory in processors or registers in microcontrollers. It is not suitable for long-term data storage.

6.6.2.2.Non-Volatile SRAM

Non-Volatile SRAM is one that is used to perform all the work assigned to basic SRAM in addition to data retaining ability of SRAM. This type of SRAM is used in aerospace applications where retaining of data is necessary. Non-volatile memory retains data even as power is switched off, making it suitable for long-term storage.

6.6.3. On basis of number of cells

SRAM has been classified into three kinds based on number of cells in SRAM cell design which are as follows

6.6.3.1. Four (4T) transistors SRAM

Components of 4T SRAM are two poly-load resistors and four NMOS as shown in figure 6.5. The PMOS transistors have been replaced out with extremely high polysilicon resistors to reduce number of transistors and total amount of space that 6T cell occupies [174]. In comparison with 6T cell, this cell has less transistors and occupies less space. Due to extremely high resistances applied in design, this cell is sensitive to soft error and noise.

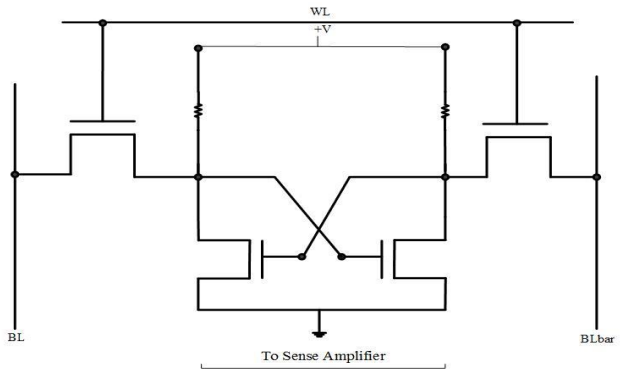


Figure 6.5. 4T SRAM cell structure [174].

6.6.3.2. Six (6T) transistor SRAM

In 6T SRAM cell, a PMOS transistor is used in this case to replace the resistors. Six transistors comprise the SRAM cell: one NMOS and one PMOS transistor for each inverter and two NMOS transistors connected to row line as described in figure 6.6. In terms of speed, noise immunity and standby current, this cell outperforms a 4T structure. Large size of this cell is mainly a drawback.

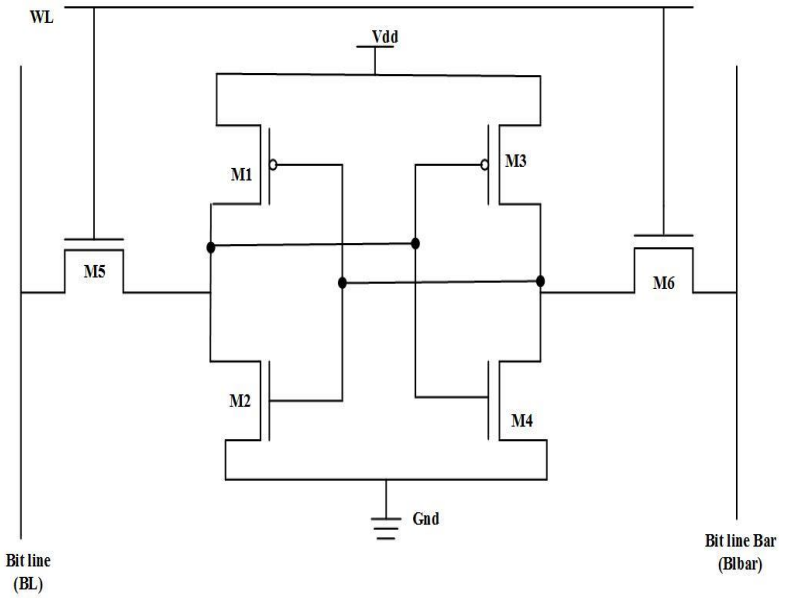


Figure 6.6. 6T SRAM cell structure [175].

6.6.3.3.Thin film (TF) transistor SRAM

Manufacturers have made an effort to lower the current passing through the load resistor of 4T cell. As a result, experts created a mechanism that allows them to alter the electrical properties of the resistor load by changing channel of transistor.

Thin film transistor (TFT) is the name given to this resistor which is established as a PMOS transistor. It is developed by depositing the silicon surface with many layers of polysilicon. The polysilicon load forms source, channel and drain as described in figure 6.7. As in 6T cell architecture, the polysilicon gate of this TFT is connected to the gate of the opposite inverter. To ensure the functionality of transistor, oxide layer between this control gate and TFT polysilicon channel needs to be as thin as possible. This cell is superior to 4T SRAM cell but its performance is not that much efficient when compared to 6T SRAM cell.

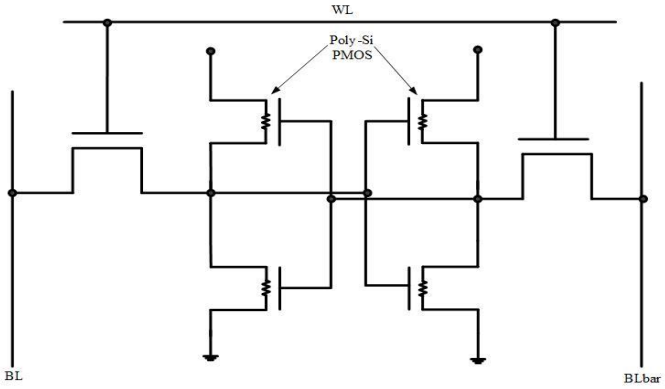


Figure 6.7. Thin film transistor SRAM cell structure [176].

6.7. LIMITATIONS OF MOSFET BASED SRAM CELLS

The short channel effects occur in MOSFET which degrades the mobility of charge carrier and leakage occurs at nano-scale regime. Further, the fluctuations in threshold voltage of MOSFET creates problem of stability where low power design of device is required [29].

Research has shown that the ultra-thin body DG- MOSFET devices are more appropriate for application in sub-50 *nm* technologies as these devices overcome SCE. They also have improved ON current and scalability when compared with single gate devices. Further, they are lightly doped, which eliminates variations in threshold voltage occurred by random fluctuations in dopant.

6.8. DESIGN STRUCTURE OF 6T SRAM CELL BASED ON CMOS TECHNOLOGY

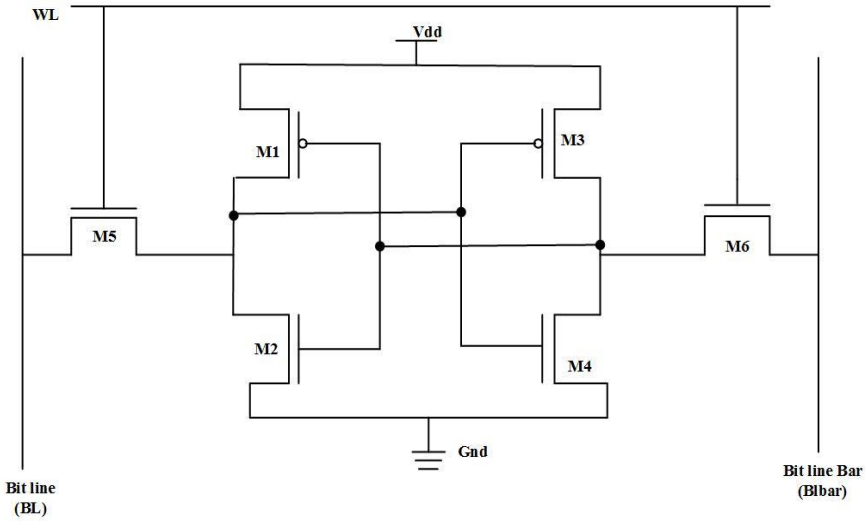


Figure 6.8. Structure of 6T SRAM cell based on CMOS technology.

A single memory bit is stored in CMOS-based 6T SRAM cell. Two-bit lines (*BL and BLbar*) that are used to access memory cells through the use of two access transistors (*M5 and M6*) that get controlled by Word line (*WL*) as depicted in figure 6.8. CMOS 6T SRAM cell operates similarly to its SRAM cell based on CNTFET.

6.9. SRAM CELL BASED ON CNTFET TECHNOLOGY

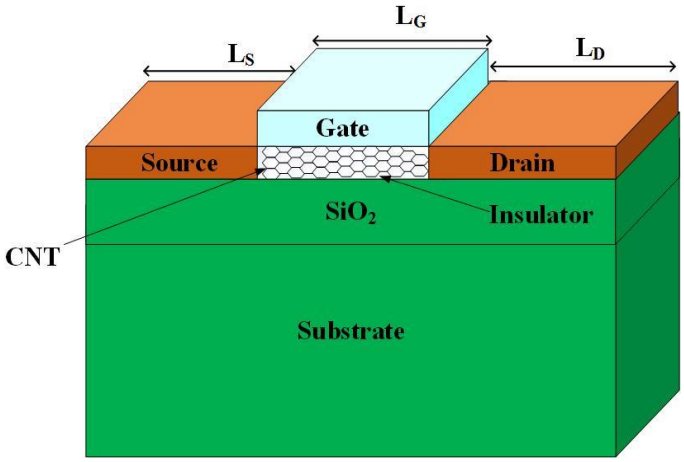


Figure 6.9. CNTFET structure [27].

According to figure 6.9., a CNTFET transistor has 4 terminals: gate, source, drain and substrate. The dielectric film is used to cover and undoped the semiconductor CNTs. Carbon nanotubes to experience less resistance during the ON state and for the device to turn ON and OFF using the electrostatic property when gate voltage increases, strongly doped CNTs are positioned in the middle of gate and source/drain.

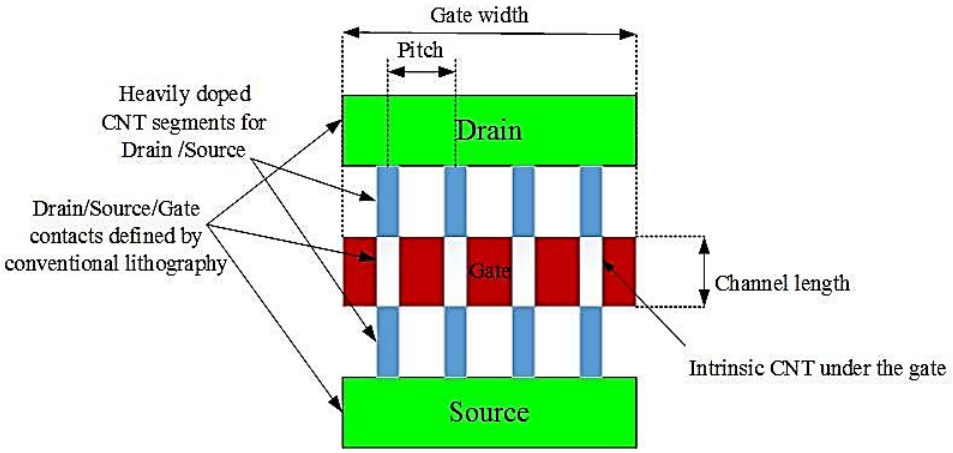


Figure 6.10. Layout of CNTFET [177].

Figure 6.10. shows the CNTFET layout diagram using Stanford CNFET model [177]. Multiple semiconducting CNTs should ideally grow in an exact parallel and straight pattern on quartz or a silicon substrate. Gate-covered portions are intrinsic CNT areas where gate controls conductivity. By heavily doping the CNT segments that make up source and drain, two types of transistors can be created namely *p*-type or *n*-type. Metal drain, gate, source and interconnect contacts defines the conventional lithography. Carbon nanotubes (CNTs) are synthesised in a self-assembled manner to determine pitch size and the inter-carbon nanotube (CNT) distance using CNT synthesis process.

Device scaling leads to various design challenges in nano regime. Memory cell with minimum size increases leakage current which reduces battery backup time. For such memory cells there is need for good optimization with low power and high speed of device.

Various techniques have been proposed for power reduction and to increase speed of memory cell. Due to its higher integration, low power and best performance, carbon nanotube has emerged as an alternative material for next-generation SRAM design in recent years. So, new devices such as CNTFET can be used for designing SRAM cells due to its unique properties.

Two cross-coupled inverters contain four transistors which stores each bit in a SRAM. The two stable states represented by ‘0’ and ‘1’are stored in each storage cell. Access transistors are required to access cross - coupled inverters when operations (read and write) are being carried out. Storing one memory bit requires six transistors.

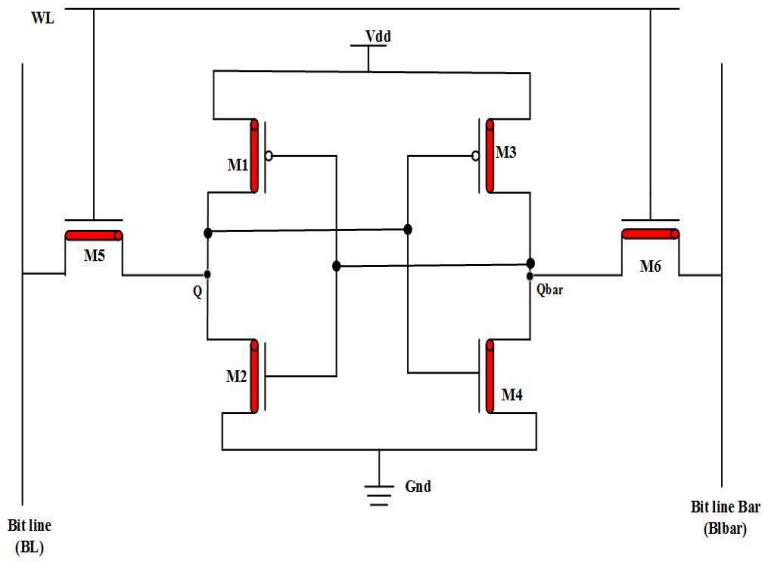


Figure 6.11. 6T SRAM cell structure based on CNTFET technology [178].

Figure 6.11. describes design of 6T SRAM cell structure based on CNTFET technology. The *M5* and *M6* access transistors, which enable *BL* and *BLbar* bit lines of the memory cell that word line (*WL*) controls. Transfer of data during operations (read and write) is done by these bitlines. There is minor difference in device orientation in CNTFET based memories rather than in CMOS based memories [178]. Source and drain are not interchangeable in case of CNTFET as in case of CMOS devices.

6.10. WORKING OF SRAM

The three SRAM cell operation modes are Read, Write and Hold. This section describes the hold, read and write operations.

1) Hold operation
2) Read Operation
3) Write Operation

The transistors *M6* and *M5* are turned off when the computer is in hold operation, which separates memory cell from bit lines by setting word line to '0' (*WL* = '0'). As long as the supply V_{dd} is connected to transistors *M1* through *M4*, which constitute two inverters coupled in a feedback loop, data is kept in latch until supply is turned ON.

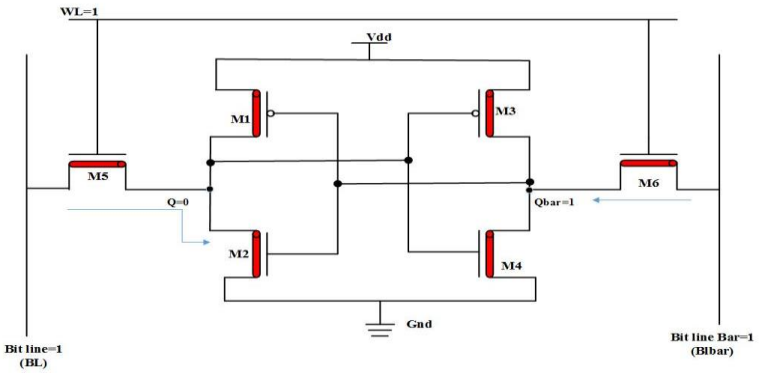


Figure 6.12. CNTFET-based 6T SRAM cell with read operation [178].

Figure 6.12. describes read operation of SRAM cell. Access transistors (*M5* and *M6*) are turned ON during a read operation by applying voltage to word line. Upon turning these access transistors ON, the voltage at point *Q* will be given to the bit line (*BL*). Similarly, voltage present at *Qbar* is given to *BLbar*. Let *Q* is at logic '1'. Therefore, *BL* will have logic '1' and logic '0' will be present at *BLbar*. Using sense amplifier, voltage can be read. The purpose of two bit lines is to enhance speed of SRAM cell. To enhance speed of SRAM cells, bit lines are precharged with some finite values. Let these precharged values be 2V for logic '1' and 0V for logic '0'. Therefore, the bit lines are precharged with a voltage of 1V. Let us make an assumption that the voltage being read through SRAM is a logical '1'. So, voltage at Q will be 2V and voltage at *Qbar* will be 0V. As access transistor *M5* gets turned ON, the voltage of value 2V is reflected at the bit line. But transistor takes some time to reach from 1V to 2V at Q and 1V to 0V at *Qbar*, rather than waiting for voltage to rise from 1V to 2V and falling from 1V to 0V. The speed of read cycle can be increased by analyzing trend of changing voltage. The difference of *BL* and *BLbar* bit lines voltages is taken and amplification of these voltages is done and sensed using sense amplifier.

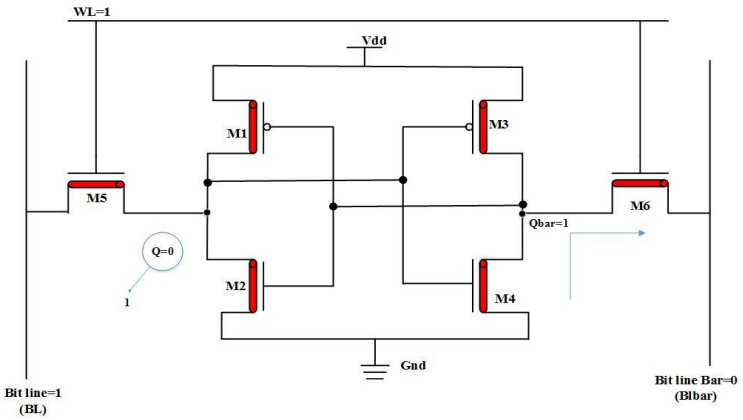


Figure 6.13. CNTFET-based 6T SRAM cell with write operation [178].

Figure 6.13. describes write operation of 6T SRAM Cell. While writing data in the SRAM cell, voltage which is to be written on inverter pair that must be applied to bit line. Let logic '1' is applied at bit line and initial voltage stored in inverter pair is logic '0'. Therefore, logic '0' is applied at *Qbar* and *BLbar*. When *M5* is turned ON, voltage at bit line is given to first inverter and second inverter tries to decrease the voltage of *BL* to logic '0'. Similarly, logic '0' is given to input of second inverter, output will be set to logic '1'. And logic '1' will cause output of first inverter to change to logic '0'. Therefore, logic '1' is latched between the inverters.

6.11. PERFORMANCE PARAMETERS OF CNTFET SRAM CELL

SRAM cells are essential building blocks in modern integrated circuits, commonly used for high-speed, low-power and volatile storage of data. Various performance parameters characterize SRAM cells and these parameters can vary depending on the specific design and technology node of SRAM cell. Some of the performance parameters of SRAM cells are as follows

6.11.1. Propagation Delay

Time difference between applied input and produced output is referred to as propagation delay [179]. It is important to reduce delay and enhance speed of system while designing any system. SRAM cell speed is determined by reading and writing access times. Propagation delay is described as difference between 50% of input rise and 50% of output fall [179].

6.11.2. Power Delay Product (PDP)

Power delay product (PDP) can be expressed as multiplication of propagation delay and average power which is consumed. PDP estimates the energy used in a switching event (0 to 1 or 1 to 0 transition) and is also known as switching energy. Performance of device is measured by power delay product. A circuit design is energy efficient if it gives low PDP.

Power delay product (Ws) = Propagation Delay(s) × Power Dissipation (W)

6.11.3. Power Dissipation

Power consumption of device is divided into two categories: dynamic power also called as switching power and static power also defined as leakage power [180]. Leakage power is now the most common power consumer in smaller geometries, while switching power is the most common contributor in larger geometries. Both types of power can be reduced with power reduction strategies. SRAM uses less energy while writing and reading than it does when the

system is sleep mode because it uses less energy when it is operating in a dynamic manner [184].

6.12. DEVICE PARAMETERS

Table 6.1. shows device parameters for simulating a 6T SRAM cell based on CNTFET.

Table 6.1. Device parameters for 6T SRAM cell based on CNTFET.

Sr. No.	Device Parameters	Values
1.	Length of channel (L_{ch})	Depends on the technology node
2.	Dielectric material thickness(t_{ox})	1nm
3.	Chirality (n,m)	(13,0)
4.	Power Supply	0.9V
5.	Work function	4.5eV
6.	Fermi Level	0.6eV
7.	Source/Drain work function with metal contact	4.6eV

Device parameters considered for the simulation of 6T SRAM cell based on CNTFET technology are mentioned in table 6.1. The length of channel of SRAM cell depends on the selection of particular technology node. The chirality taken for the carbon nanotube is (13, 0) and thickness of oxide layer is 1 *nm* which is considered for CNTFET SRAM cell simulation.

6.13. PERFORMANCE ANALYSIS OF SRAM CELL BASED ON CNTFET AND CMOS TECHNOLOGY

This section explains how the 6T SRAM cells are developed using two different types of technologies, CNTFET and CMOS. Using the 32 *nm* model files known as Stanford CNTFET model and PTM model at various technology nodes, both the 6T SRAM cells on basis of CMOS and CNTFET technology have been evaluated and analysed in HSPICE tool.

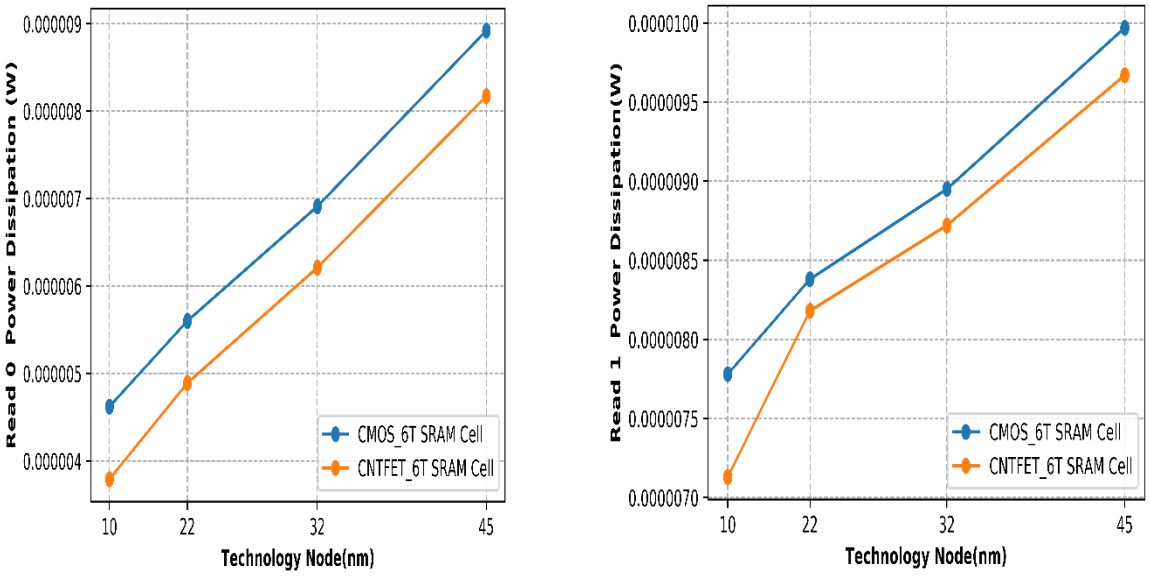
This section of the chapter explains how the technology node affects propagation delay, power dissipation and power delay product (PDP) for 6T SRAM cells based on CNTFET and conventional type technologies. The performance of device is further evaluated by comparing both 6T SRAM cells based on CNTFET and CMOS technologies, taking into account propagation delay, power dissipation and power delay product at different technology nodes.

6.13.1. Read and Write Power Dissipation

Read and write power dissipation is amount of energy consumed during write and read operations. Power consumed during read and write operations is often expressed in units of

watts (W) or micro watts (μW). These measurements provide an understanding of how much electrical energy is used during memory access operations. Total current and voltage consumption of source can be used to describe the power consumption. Mobile device design requires low consumption of power. Read and write power dissipation goes down as the technology node decreases.

6.13.1.1. Power dissipation during read operation



(a) (b)

Figure 6.14. Power dissipation of CNTFET and CMOS-based 6T SRAM cells during operations (a) Read 0 (b) Read 1 at different technology nodes.

The power dissipation of CNTFET and CMOS-based 6T SRAM cells for read operations is described in figure 6.14. (a) and (b) at various technology nodes, including 10*nm*, 22*nm*, 32*nm* and 45*nm*. Figure 6.14. shows that when technology nodes are scaled down, read power dissipation for a 6T SRAM cell based on CNTFET technology reduces in comparison to 6T SRAM cell based on CMOS technology. This drop is result of operating current decreasing with the scaled technology node under constant power supply voltage and variable environmental conditions. The power dissipation gap between CMOS and CNTFET based 6T SRAM cell decreases as the technology nodes increases from 10 *nm* to 45 *nm*. Therefore, with scaled technology nodes, read power dissipation decreases.

The figure also shows that the percentage increase in read power dissipation for scaled down technology nodes during read '0' operation increases from 8.46% to 18% as the technology

node scaled down from 45*nm* to 10*nm*. In order to design CNTFET-based devices, lower technology nodes are preferred.

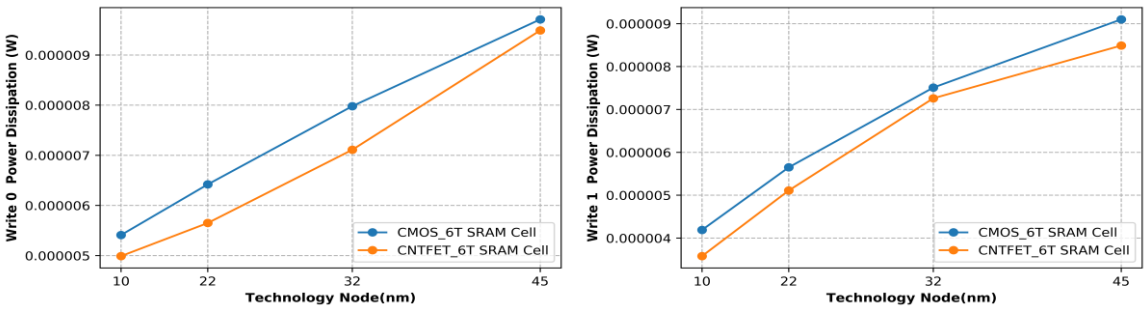
Table 6.2. Percentage change in power dissipation for read operations of CNTFET- 6T SRAM cell in comparison to SRAM cell using CMOS technology at variable technology nodes.

Technology node (*nm*)	**Power Dissipation (*W*) Read '0' Operation**		**%age Change**	**Power Dissipation (*W*) Read '1' Operation**		**%age Change**
	6T CMOS SRAM Cell	**6T CNTFET SRAM Cell**		**6T CMOS SRAM Cell**	**6T CNTFET SRAM Cell**	
10*nm*	4.62E-06	3.79E-06	18.0	7.78E-06	7.13E-06	8.43
22*nm*	5.60E-06	4.89E-06	12.8	8.38E-06	8.18E-06	2.38
32*nm*	6.91E-06	6.21E-06	10.2	8.95E-06	8.72E-06	2.54
45*nm*	8.92E-06	8.17E-06	8.46	9.97E-06	9.67E-06	3.03

Based on CNTFET and CMOS technologies, table 6.2. shows the percentage change in read power dissipation of 6T SRAM cells for various technological nodes. The table shows that read power dissipation for SRAM cells employing CNTFETs is significantly lower than in SRAM cells made with CMOS technology for technology nodes 10 *nm*, 22 *nm*, 32 *nm* and 45 *nm.*

When compared to 6T SRAM cell with CMOS technology at various technology nodes for read '0' operation, there is a reduction in the read power dissipation of CNTFET-based SRAM cells of 18% for 10*nm*, 12.8% for 22*nm*, 10.2% for 32*nm*, and 8.46% for 45*nm.* Applications where lower power dissipation is necessary, CNTFET based SRAM cell designs can be used.

6.13.1.2. Power dissipation during write operation



(a) (b)

Figure 6.15. Power dissipation for 6T SRAM cells using CNTFET and CMOS technologies during operations (a) Write 0 (b) Write 1 at diferent technology nodes.

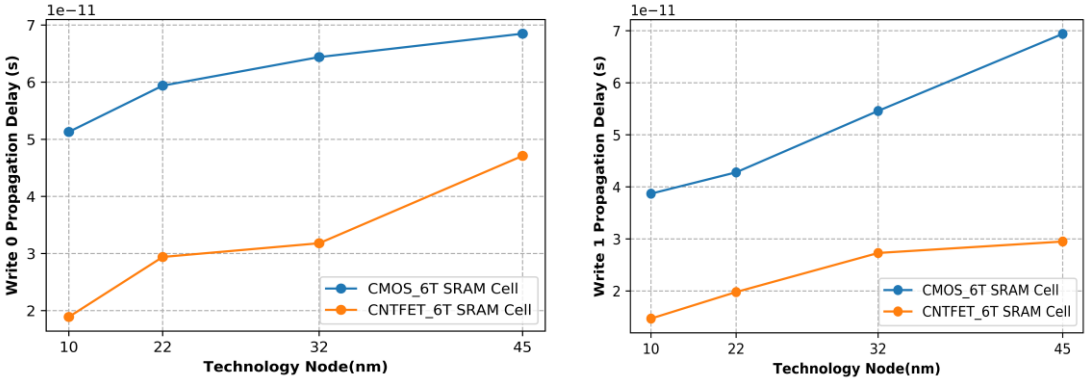
Power dissipation of a 6T SRAM cell using both CMOS and CNTFET during write operations at various technology nodes is described in figure 6.15. (a) and (b). Figure shows that for CNTFET SRAM cells, write power dissipation decreases with scaled down technology nodes. This decrease is a result of inverter losses that occurs when pull-up and pull-down transistors change states at lower technology nodes. Two transistors turn ON during the transition period, creating a path for current to flow from power supply VDD rail to the ground. At lower technological nodes, write power dissipation will decrease because transistor ON resistance increases. Smaller technology nodes can also enable lower operating voltages, which can contribute to reduce the power dissipation in CNTFETs. Further, CNTFET based 6T SRAM cell uses carbon nanotubes having high electron mobility which can contribute to faster switching speeds and consequently lowering consumption of power for read and write operations.

Table 6.3. Percentage change in power dissipation for write operation of CNTFET based 6T SRAM cell in comparison to CMOS based SRAM cell at variable technology nodes.

Technology node (*nm*)	**Power Dissipation (*W*) Write '0' Operation**		**%age Change**	**Power Dissipation (*W*) Write '1' Operation**		**%age Change**
	6T CMOS SRAM Cell	**6T CNTFET SRAM Cell**		**6T CMOS SRAM Cell**	**6T CNTFET SRAM Cell**	
10*nm*	5.41E-06	4.99E-06	7.77	4.19E-06	3.58E-06	14.46
22*nm*	6.42E-06	5.65E-06	11.97	5.65E-06	5.11E-06	9.55
32*nm*	7.98E-06	7.11E-06	10.90	7.51E-06	7.26E-06	3.26
45*nm*	9.71E-06	9.49E-06	2.27	9.10E-06	8.49E-06	6.68

While using CNTFET and CMOS technologies, table 6.3. shows the power dissipation for write '0' and write '1' operations of 6T SRAM cell at various technology nodes. Table shows that, at technology node of 10*nm*, percentage change in write power dissipation between SRAM cells using CNTFET and CMOS technology is 14.4%. CNTFET based 6T SRAM cell can therefore be used in low power designs

6.13.2. Propagation Delay



(a) (b)

Figure 6.16. Propagation delay of CNTFET and CMOS technology based 6T SRAM cell during operations (a) Write 0 (b) Write 1 at different technology nodes.

It is obvious from figure 6.16. (a) and (b) that scaling down the technology nodes reduces the propagation delay of 6T SRAM cell using CNTFET technology. The decrease in threshold voltage in lower technology nodes causes an increase in overdrive voltage and drain current, which causes the propagation delay to decrease. As technology nodes advance, there is often a trend toward lower supply voltages to reduce power consumption. Lower supply voltages can lead to slower switching speeds in CNTFETs, which in turn can result in longer propagation delays.

Also, the propagation delay of 6T SRAM cell based on CMOS increases with increase in technology nodes. Further, CNTFET - based 6T SRAM cell describes less propagation delay as compared to CMOS - based 6T SRAM cell for various technology nodes i.e., 10*nm*, 22*nm*, 32*nm* and 45*nm*. Further, CNTFET based 6T SRAM cell uses CNTFET that exhibit ballistic transport of charge carriers in which electrons can travel through the channel with minimal scattering, reducing time it takes for signals to propagate through transistors and contributing to lower propagation delays in comparison with CMOS based 6T SRAM cell.

Therefore, it is seen from simulated results that for all four technologies considered for this work, 6T SRAM cell based on CNTFET performs better than CMOS-based 6T SRAM cell. Thus, CNTFET based SRAM cell increases memory cell speed which enhances device performance.

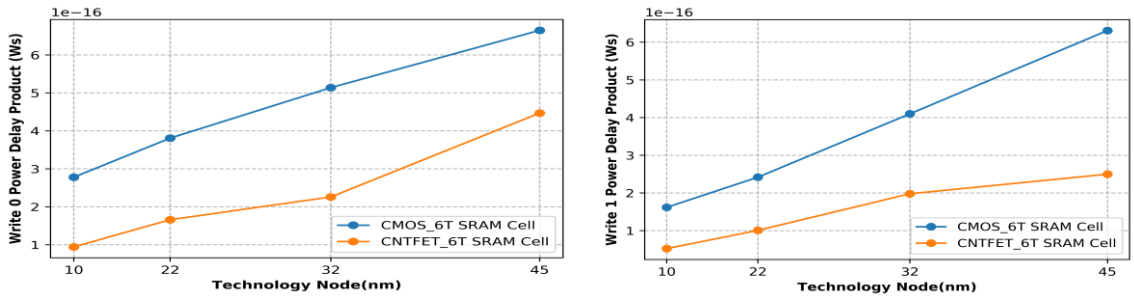
Table 6.4. Percentage change in propagation delay for write operation of 6T SRAM cell using CNTFET in comparison with CMOS based 6T SRAM cell at variable technology nodes.

Technology node (*nm*)	**Propagation Delay (*s*) Write '0' Operation**		**%age Change**	**Propagation Delay (*s*) Write '1' Operation**		**%age Change**
	6T CMOS SRAM Cell	**6T CNTFET SRAM Cell**		**6T CMOS SRAM Cell**	**6T CNTFET SRAM Cell**	
10*nm*	5.13E-11	1.89E-11	63.2	3.87E-11	1.47E-11	62
22*nm*	5.94E-11	2.94E-11	50.5	4.28E-11	1.98E-11	53.7
32*nm*	6.44E-11	3.18E-11	41	5.46E-11	2.73E-11	50
45*nm*	6.85E-11	4.71E-11	31.2	6.94E-11	2.95E-11	57.5

Table 6.4. compares the propagation delay for write operations of 6T SRAM cell based on CNTFET with a CMOS based SRAM cell for various technology nodes. Threshold voltage variability is a challenge in CMOS technology and can lead to increased propagation delay due to variations in transistor characteristics whereas CNTFETs are expected to have reduced threshold voltage variability which result in more predictable and consistent circuit performance, thereby reducing delays. As a result, SRAM cells produced from CNTFET are better than SRAM cells made from CMOS because propagation delay of SRAM cell using CNTFET is decreased by 63.2% at 10*nm* technology as compared to CMOS based SRAM cell.

6.13.3. Power Delay Product (PDP)

Power delay product is an essential component in manufacture of ICs. As a result, performance of device is determined as product of propagation delay and power dissipation. It is related to energy efficiency of the device.



(a) (b)

Figure 6.17. Power delay product (PDP) in case of 6T SRAM cell using CNTFET and CMOS technologies during operations (a) Write 0 (b) Write 1 at different technology nodes.

Power delay product of a 6T SRAM cell using CNTFET and CMOS technologies during write 0 and write 1 operations at various technology nodes has been described in figure 6.17. (a) and (b). Figure illustrates that as technology nodes decreases, power delay product of a 6T SRAM cell using CNTFET technology gets reduced. Further study describes that SRAM cell based on CNTFET shows lower power delay product than SRAM cell using CMOS at a variety of technology nodes. In comparison with 6T SRAM cell made using CMOS technology, CNTFET SRAM cell has lower value of power delay product (PDP), which indicates that they are more energy efficient.

Table 6.5. Percentage change in power delay product for write operations of CNTFET 6T SRAM cell in comparison with CMOS based SRAM cell at variable technology nodes.

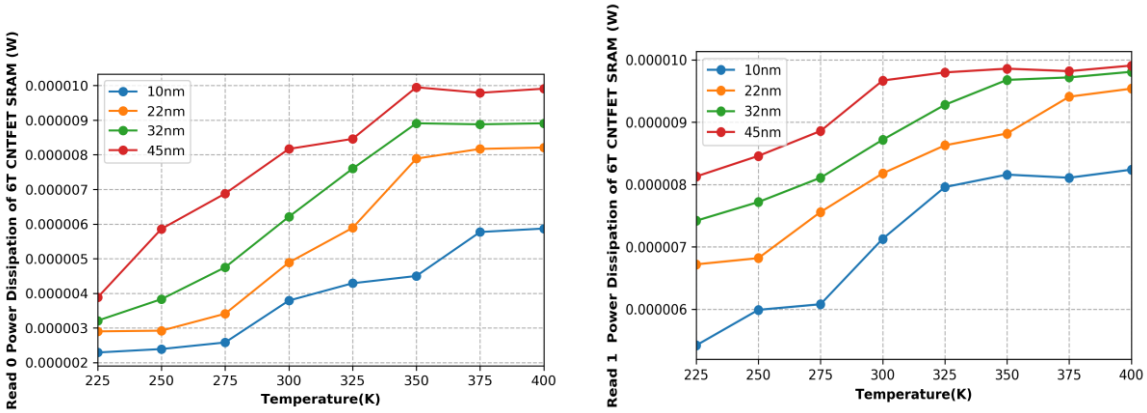
Technology node (*nm*)	**Power Delay Product(*Ws*) Write '0' Operation**		**%age Change**	**Power Delay Product (*Ws*) Write '1' Operation**		**%age Change**
	6T CMOS SRAM Cell	**6T CNTFET SRAM Cell**		**6T CMOS SRAM Cell**	**6T CNTFET SRAM Cell**	
10*nm*	2.78E-16	9.43E-17	66	1.62E-16	5.26E-17	67.5
22*nm*	3.81E-16	1.66E-16	56.4	2.42E-16	1.01E-16	58.2
32*nm*	5.14E-16	2.26E-16	47.4	4.10E-16	1.98E-16	51.6
45*nm*	6.65E-16	4.47E-16	32.8	6.31E-16	2.50E-16	60.3

Table 6.5. describes the percentage change in power delay product while performing write operation of CNTFET-based 6T SRAM cell in comparison with 6T SRAM cell of CMOS technology at variable technology nodes. It is also clear from the table that as we move from higher technology nodes (45 *nm*) to scaled technology nodes (10 *nm*), ratio of power delay product of CNTFET based 6T SRAM cell to CMOS based 6T SRAM cell is increasing so at scaled technology nodes, CNTFET based 6T SRAM cell is more energy efficient than CMOS based 6T SRAM cell. Advancements in CNTFET technology may lead to improved energy efficiency and higher speed in smaller nodes in the future than the CMOS based SRAM cell. Hence, SRAM cell using CNTFET technology is more suitable candidate for nanometer technologies to replace SRAM cell based on CMOS. Thus, for devices with high-speed and low-power, CNTFET can be used as alternative option to replace CMOS based devices.

6.14. IMPACT OF TEMPERATUE ON PERFORMANCE PARAMETERS

Temperature impact on power dissipation during read and write operations, propagation delay, and power delay product (PDP) of a 6T SRAM cell based on CNTFET have been described in this part of chapter. Influence of varying temperatures between 225K and 400K has been taken into consideration in order to evaluate performance of SRAM cells under thermal environmental conditions.

Figure 6. 18. (a) and (b) describes power dissipation for 6T SRAM cells based on CNTFET technology during operations (a) Read 0 (b) Read 1 at variable temperature for different technology nodes.

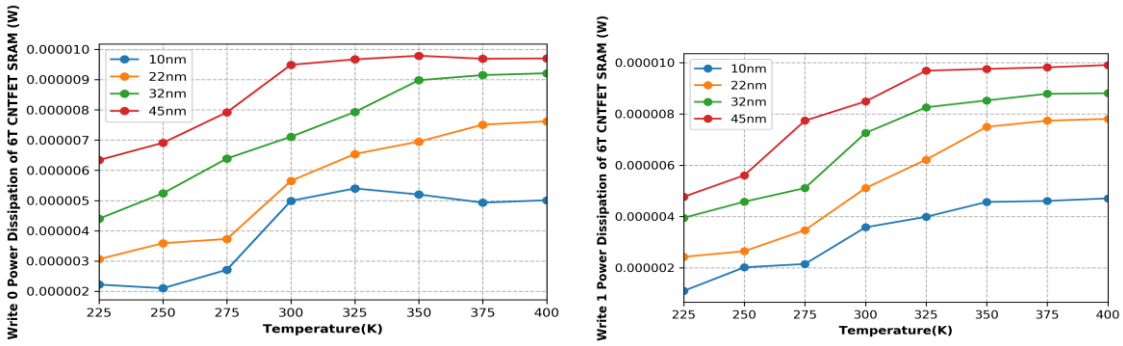


(a) (b)

Figure 6. 18. Power dissipation of 6T SRAM cells based on CNTFET technology during operations (a) Read 0 (b) Read 1 at variable temperature for different technology nodes.

It is shown from figure 6. 18. (a) and (b) that read power dissipation increases with increase in temperature at different technology nodes. At low temperatures, read power dissipation increases with rise in temperature and technology nodes i.e., from 10 *nm* to 45 *nm*. Reason is that faster switching speeds increase power dissipation for read and write operations in CNTFET SRAM cells. Increasing temperatures increases thermal generation of charge carriers within the device that can contribute to increased leakage currents and, consequently, higher power dissipation. Also, as temperature rises from 300 K to 350K i.e. at moderate high temperatures, power dissipation increases but increase is less as compared to power dissipation at low temperatures because at moderate higher temperatures, mobility of charge carriers in carbon nanotubes may increase. However, there is a limit to this increase, and beyond a certain temperature, further increments may not significantly affect mobility. As a result, electrical

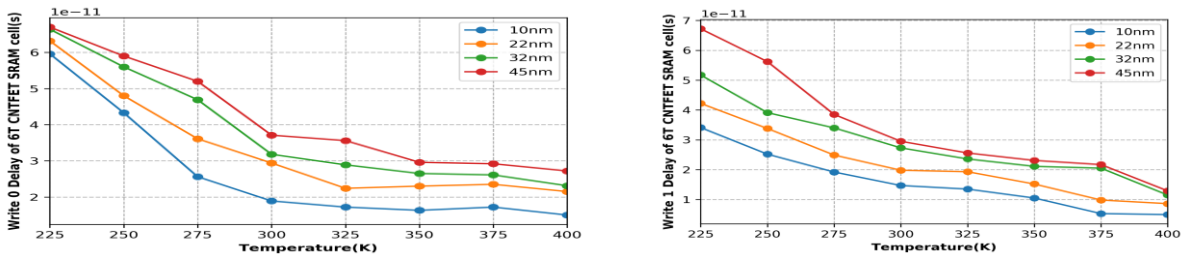
characteristics of CNTFET may become relatively constant, leading to a stabilization of power dissipation. At high temperature of 350 K to 400K, rate of read power dissipation increase is nearly constant because higher temperature means the greater is consumption of power as well as heat dissipation. Any device that dissipates more heat or power has a greater possibility of degradation. Because of this, there is a lower possibility of a CNTFET-based SRAM cell degrading at higher temperatures [182]. As technology nodes decreases from 45 *nm* to 10 *nm*, CNTFET SRAM cells benefit from reduced parasitic capacitance and improved performance. Smaller feature sizes contribute to lower power dissipation, as well as faster access times and reduced area.



(a) (b)

Figure 6. 19. Power dissipation of 6T SRAM cells based on CNTFET technology during operations (a) Write 0 (b)Write 1 at variable temperature for different technology nodes.

Power dissipation of 6T SRAM cells based on CNTFET technology during operations (a) Write 0 (b) Write 1 at variable temperature for various technology nodes as described in figure 6. 19. (a) and (b). It is observed from figure that when temperature increases from 225K to 400K, write power dissipation increases in case of 6T SRAM cell based on CNTFET for various technology nodes.

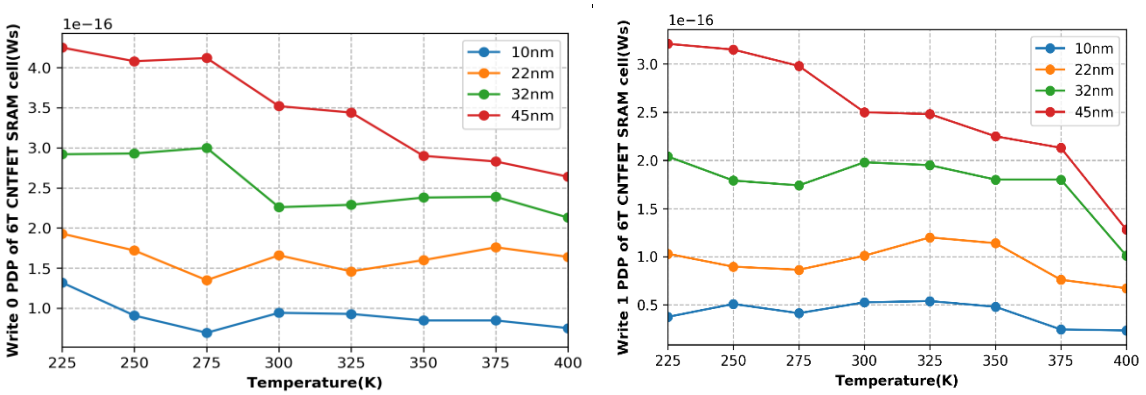


(a) (b)

Figure 6.20. Propagation delay of 6T SRAM cell using CNTFET technology during operations (a) Write 0 (b) Write 1 at variable temperature for different technology nodes.

Figure 6.20. (a) and (b) describes propagation delay of CNTFET based 6T SRAM cell during operations (a) Write 0 (b) Write 1 at variable temperature for different technology nodes. Charge carriers' mobility in 6T SRAM cell based on CNTFET gets influenced by temperature variation (225K-400K). At higher temperature, i.e., 400K, the increased thermal energy enhances carrier mobility which leads to faster charge transport within the transistor channel reducing the propagation delay of CNTFET based 6T SRAM cell. Further, threshold voltage of CNTFETs exhibit some dependence on temperature as explained in chapter 5. At higher temperature of 400K, there is a reduction in threshold voltage of CNTFETs, which ultimately impact overall performance of CNTFET based SRAM cell. If threshold voltage decreases as temperature increases from 225K to 400K, it contributes to faster switching and reduction in propagation delay of 6T SRAM cell based on CNTFET. Decreasing technology nodes from 45 *nm* to 10 *nm* lead to reduced parasitic capacitance and improved transistor performance. Smaller transistors can switch faster which contribute to lower propagation delays in 6T SRAM cell using CNTFET.

PDP of 6T SRAM cell using CNTFET technology during operations (a) Write 0 (b) Write 1 at variable temperature for different technology nodes is described in figure 6. 21. (a) and (b).



(a) (b)

Figure 6.21. Power delay product of 6T SRAM cell using CNTFET technology during operations (a) Write 0 (b) Write 1 at variable temperature for different technology nodes.

It is shown from the figure 6. 21. (a) and (b) that power delay product of 6T SRAM cell using CNTFET technology during operations (a) Write 0 (b) Write 1 decreases as temperature rises from 225 K to 400 K at different technology nodes. The reason is that higher temperatures leads to improved electron mobility, which in turn enhances speed of CNTFET based 6T SRAM cell. Faster operation results in a low delay contributing to a reduction in power-delay product. Higher temperature i.e., (400K) also lead to higher leakage currents, which may offset

benefits of improved mobility. The overall impact on power-delay product will depend on specific characteristics of CNTFET technology being used in SRAM cell. Scaled technology nodes have lower intrinsic capacitance leading to decreased power consumption in SRAM cell. Further, as technology node decreases from 45 *nm* to 10 *nm* there is reduction in capacitance, shorter interconnect lengths and smaller transistor sizes, all of which contribute to lower power consumption and reduced delay in 6T SRAM cell using CNTFET technology.

6.15. COMPARISON OF 6T SRAM CELL WITH EXISTING LITERATURE

To compare performance of proposed CNTFET based 6T SRAM cell with CMOS 6T SRAM cell available in literature, a comparative analysis is performed.

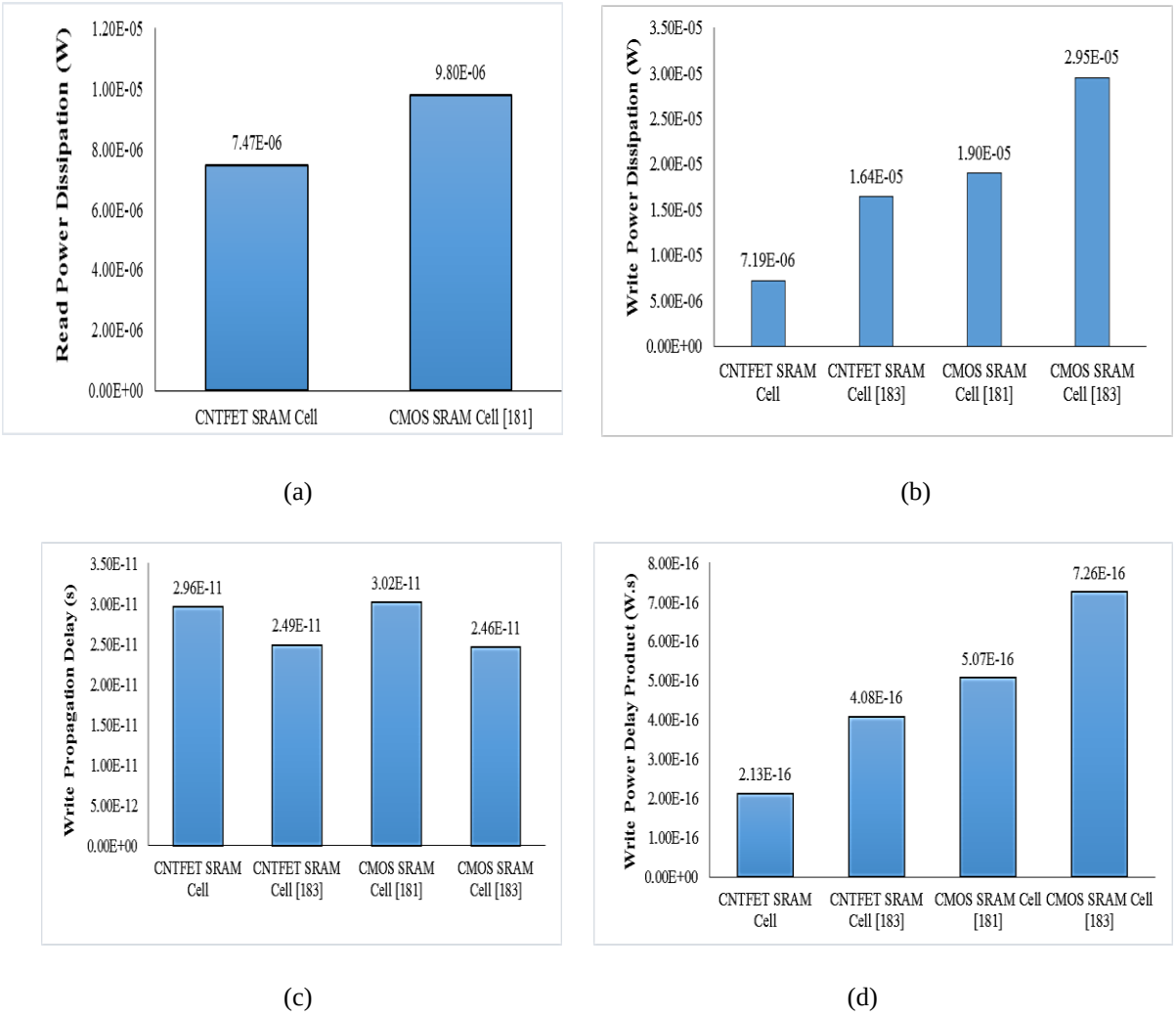


Figure 6.22. Comparison of (a) Read power dissipation (b) Write power dissipation (c) Write propagation delay (d) Write power delay product of 6T SRAM cell using CNTFET and CMOS technologies.

Figure 6.22. shows comparison of dissipation of power during read and write operations, write propagation delay and write power delay product of 6T SRAM cell using CNTFET and CMOS

technologies. Read and write power dissipation of CNTFET based SRAM cell is less in comparison with 6T SRAM cells existing in literature which is described in figure 6.22. (a) and (b). This is because CNTFETs exhibit superior electrical properties and have lower OFF current when compared to CMOS transistors which is a significant source of reduced power dissipation in CNTFET based 6T SRAM cell. Figure 6.22. (c) describes that write propagation delay for 6T SRAM cell considering CNTFET is less than results available in literature for CMOS based 6T SRAM cell in [181] where as it is nearly equal to write delay as observed in SRAM cells available in [183]. High carrier mobility of CNTFET allows for faster charge carrier movement through channel resulting in quicker switching speeds and consequently lowering propagation delays in comparison to 6T SRAM cell based on CMOS. The combination of lower power consumption and faster switching speeds in CNTFET based 6T SRAM cell contributes to overall improved energy efficiency resulting in a lower power-delay product in comparison with 6T SRAM cell available in literature as given in figure 6.22. (d).

6.16. SUMMARY AND CONTRIBUTION OF CHAPTER

The memory and its types, its hierarchy have been discussed in detail in this chapter. A brief introduction related to SRAM cell has been described. The various types of SRAM cell based on their functionality, data holding ability and number of cells have been explored. Further, SRAM cell working and SRAM cell using CNTFET technology have been elaborated. Based on performance parameters of CNTFET SRAM cell, a comparative analysis between CNTFET and CMOS based SRAM cell is done to study performance of CNTFET based SRAM cell. Investigation of a CNTFET based 6T SRAM cell for performance parameters including read and write power dissipation, propagation delay and power delay product (PDP) for various technology nodes including 10*nm*, 22*nm*, 32*nm* and 45*nm* was main focus of this chapter. Performance of both SRAM devices using CNTFET and CMOS has been investigated by a comparison of both SRAM cells at various technology nodes, including 10*nm*, 22*nm*, 32*nm* and 45*nm*, while accounting for read and write power dissipation, propagation delay and power delay product (PDP). It was analyzed from results that 6T SRAM cell based on CNTFET outperforms CMOS based 6T SRAM cell considering read and write power dissipation, propagation delay and power delay product. Combination of lower power consumption and faster switching speeds in CNTFET based 6T SRAM cell contributes to overall improved energy efficiency resulting in lower power-delay product in comparison to CMOS based 6T SRAM cell.

PUBLISHED WORK RELATED TO THIS CHAPTER:

[1] Aakanksha Lakhanpal and Karmjit Singh Sandha,"Impact of variable temperature on the performance analysis of CNTFET and CMOS-based SRAM Cells," in International Conference, *Recent Advancements in Communication, Computing and Artificial Intelligence (RACCAI)*, 2023. (**Scopus indexed – Accepted**)

[2] Aakanksha Lakhanpal and Karmjit Singh Sandha,"CNTFET and CMOS-based SRAM Cells: A Comparative Analysis for Low-Power Design," *Analog Integrated Circuits and Signal Processing*, 2023. (**SCI indexed- Under Review)**

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

A set of conclusions have been drawn using the analytical and simulated results obtained in thesis. The following sections of this chapter contain the conclusion and future work scope.

7.1. CONCLUSION

The research work included in this thesis, presented the optimized structure of double gate carbon nanotube field effect transistor. In the initial phase of this work, a thorough study related to the limitations in scaled devices and challenges occurred by silicon device scaling has been done. Further, review related to short channel effects, methods to overcome these limitations has been discussed so that need of CNT, CNT based devices and temperature dependent modeling of DG-CNTFET and its application in the VLSI industry could be established. Although there haven't been many studies cited in the literature, there is still a lot of scope for investigation in design and optimization of high performance of CNTFET based devices. Brief outline of CNTFET technology-based devices has been presented in the literature.

The effect of temperature and bandgap on single gate CNTFET considering several parameters namely ON current, OFF current, ON to OFF current ratio, DIBL and subthreshold slope has been investigated in various studies. Further, in literature, a few research have been done on temperature effect on performance analysis of double gate CNTFETs. Therefore, temperature dependent work needs to be extended considering double gate CNTFET so as to outperform the MOSFET based devices in terms of various performance parameters.

The modeling of drain current of the proposed structure of DG-CNTFET is carried out. Further, temperature impact on several performance parameters of DG-CNTFET has been established. To evaluate DG-CNTFET performance, an analytical model that is temperature dependent has been proposed at variable temperature range. This developed model presented in this work is used to achieve I-V characteristics of DG-CNTFET. To examine the temperature impact on device performance, other performance parameters including drain conductance, subthreshold swing, ON and OFF current and output characteristics have also been investigated at various temperatures. Using nano-TCAD ViDES simulator, device's I-V characteristics have been modeled. It was also studied that how temperature affected performance parameters namely drain conductance, subthreshold swing, ON current, OFF current, output characteristics and I-V and output characteristics. It was analyzed from results that drain current increases with rise

in temperature at different V_{ds} values. Further, at varying temperatures, drain conductance and ON current were raised. In addition, leakage current increased by varying temperature and affects the reliability of the device. On rising temperature from 250 K to 400 K, drain conductance rises by a factor of 4 and subthreshold swing increases with temperature. These results can be effectively applied to design considerations in devices.

Furthermore, this work describes the threshold voltage modeling and channel parameters effect on DG-CNTFET's threshold voltage at various temperatures. Using nanoHUB simulations tools, the impact of varying temperature range on several channel parameters, namely chirality, CNT diameter, quantum capacitance and high-k dielectric, has been studied. This has been extended to DG-CNTFET's threshold voltage.

It was discovered that the threshold voltage of DG-CNTFETs changes with variations in CNT chirality and diameter, which has an impact on DG-CNTFET's thermal conductivity. It was further examined that reduction in DG-quantum CNTFET's capacitance would enhance the device's propagation delay. Higher k value of dielectric oxide materials in DG-CNTFETs provide much faster switching rates and reduced consumption, according to results shown in this chapter.

Threshold voltage analysis for DG-CNTFET and DG-MOSFET at varying temperatures was also performed in this work. It was observed that DG-CNTFET's threshold voltage decreases slightly with temperature that makes it suitable for applications where thermally aware environmental conditions need to be considered for design purposes.

Last part of this work included the application part of CNTFET. The basic cell operations and design parameters have also been described. The SRAM cell using CNTFET has been designed to evaluate device performance.

In addition to this, a comparative analysis of SRAM cell considering CNTFET and CMOS technologies has been done to investigate SRAM cell performance considering power dissipation, propagation delay and power delay product (PDP) at variable technology nodes such as 10 *nm*, 22 *nm*, 32 *nm* and 45 *nm*. Results showed that 6T SRAM cell based on CNTFET outperforms SRAM cell based on CMOS due to lesser power dissipation and propagation delay which can further be used for less power and high-speed applications.

At last, it is concluded that:

CNTFETs are better contender to replace the traditional MOSFETs at nanoscale in VLSI industry as it overcomes various SCEs. To evaluate CNTFET device performance, considering various parameters, effect of temperature is necessary to study the device for high performance applications under thermal environment conditions.

7.2. FUTURE SCOPE OF WORK

The work presented in this thesis described various short channel effects and shortcomings of traditional MOSFETs and DG-CNTFETs have been proposed as alternative to replace the MOSFET based devices at nanoscale. Further, in order to evaluate DG-CNTFET's performance under variable temperature range, modeling of threshold voltage and drain current has been presented. Exploring the various fields of proposed area, the performance of the device can be improved further. Therefore, there are some points and ideas that can be explored in near future in the field of CNTFETs and are as follows:

- In nanoscale regime, it is necessary to remove various short channel effects of scaled devices. Therefore, to overcome these effects various high-k values of dielectric materials such as HfO_2 can also be used as gate oxide material to overcome the drawbacks of traditional silicon dioxide (SiO_2) gate dielectric. Further, to evaluate device performance, effect of temperature considering the HfO_2 as gate oxide material need to be analyzed.
- In future, most desirable work using CNTFETs with enhanced performances, lower costs of production, or higher reliability. By including external effects to inner CNT transistor such as several CNTs at a single gate, channel fringe capacitances, parasitic source/drain resistance and series resistance caused by scattering effects, device's performance can be further enhanced.
- In overall circuit level designs, the power analysis is very important. Therefore, adding a power component to the optimization framework will be very helpful for circuit designers in the early design stage, along with performance and an area for more in-depth research.
- The manufacturing of CNTFETs are the major challenges as these involve complex growth processes and should be taken care of in future work.

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