

DECLARATION

I hereby declare that the work which is being presented in the thesis entitled, “**Analysis, Verification and FPGA Implementation of Vedic Multiplier with BIST Capability**” in partial fulfillment of the requirement for the award of degree of M.Tech (VLSI Design & CAD) at electronics and Communication Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Mr. Arun Kumar Chatterjee**, Lecturer, ECED.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of my degree.

Date: 15/07/2009



Vinay Kumar

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.



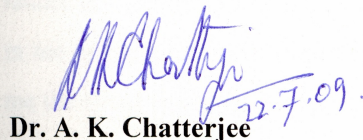
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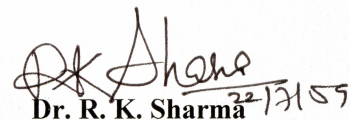
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