

PERFORMANCE ANALYSIS OF VARIOUS MULTI-LEVEL VOLTAGE SOURCE CONVERTER TOPOLOGIES

A Dissertation submitted in fulfillment of the requirements for the Degree
of

MASTER OF ENGINEERING *in* **Power Systems**

Submitted by

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DECLARATION

I hereby certify that the work which is presented in dissertation entitled, "PERFORMANCE ANALYSIS OF VARIOUS MULTI-LEVEL VOLTAGE SOURCE CONVERTER TOPOLOGIES", in partial fulfillment of the requirements for the award of the degree of Master of Engineering in Power Systems, submitted to Electrical & Instrumentation Engineering Department of Thapar University, Patiala is as authentic record of my own work carried under the supervision of **Dr. PARAG NIJHAWAN**. It refers others researcher's work which are duly listed in the reference section. The matter contained in this dissertation has not been submitted, neither in part nor in full to any other degree to any other university or institute except as reported in text and references.

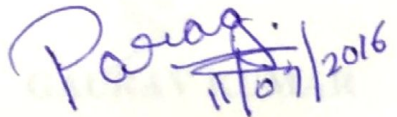
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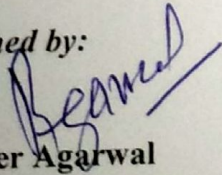

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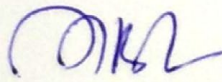
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ABSTRACT

Multi-Level Inverter is a boon to power industries in the present scenario as power industries require high voltage and good quality sinusoidal voltage waveform. Both these requirements can be fulfilled by Multi-Level Inverter. But the proper selection of inverter for different industrial application is necessary. Here the selection of Voltage Source Multi-Level Inverter for STATCOM (Static Compensator) is carried out by performing simulation based performance analysis. STATCOM is a FACTS (flexible alternating current transmission system) device which is used to maintain flat voltage profile while providing reactive power support and damp power oscillations. STATCOM is connected to the transmission line and it works on high voltage ranging from 132kV to 765kV. Hence, conventional two -level inverter is not a good choice as it has to operate in PWM mode and there is a requirement of large transformers. In high power and high voltage application PWM causes high switching losses, therefore, soft switching at the fundamental frequency is desired. The STATCOM discussed here is having constant dc-link voltage which is not found in conventional STATCOM operation. Maintaining constant dc-link voltage helps in utilizing converter efficiently. The STATCOM performance is analyzed by switching inductive and capacitive load for a particular duration in MATLAB/SimPowerSystem Toolbox.

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LIST OF ABBREVIATIONS

ACRONYMS	FULL-FORMs
FACTS	Flexible Alternating Current Transmission Systems
GTO	Gate Turn-Off Thyristor
IGBT	Integrated Gate Bipolar Transistor
MTO	MOS turn-Off Thyristors
MLI	Multi-Level Inverter
PWM	Pulse Width Modulation
SPWM	Single Pulse width Modulation
MPWM	Multi-pulse width Modulation
VSC	Voltage Source Converter
STATCOM	Static Synchronous Compensator
DCMLI	Diode-Clamped Multi-level inverter
FCMLI	Flying Capacitor Multi-level inverter
CHBMLI	Cascaded H-Bridge Multi-level inverter
THD	Total Harmonic Distortion
PCC	Point of Common Coupling
RTDS	Real Time Digital Simulator
EAF	Electrical Arc Furnaces
ES	Energy Source

RMS	Fast Fourier Transform
SDCSs	Separate Dc Source
PV	Photo Voltaic
PI	Proportional Integral

LIST OF SYMBOLS

Symbols	Meaning
σ	Conduction Angle
β	Dead Angle
δ	Load Angle
v_{a_0}	Phase-a Output Voltage
V_s or v_{dc}	dc Source Voltage
v_{a_01}	Fundamental RMS Component of Phase-a Voltage.
E	EMF
X	Inductive Reactance
V	Terminal Voltage
I	Current
S	Complex Power
P	Active Power
Q	Reactive Power
v_{c1}	Fundamental Component of Converter Voltage
v_p	Active Component of Voltage
v_r	Reactive Component of voltage
i_p	Active Current Component
i_r	Reactive Current Component

v_{dc}^*	Reference dc-Link Voltage
i_d^*	d-axis Reference Current Component
i_d	d-axis Current Component
i_q^*	q-axis Reference Current Component
v_{td}, v_{tq} and v_{t0}	Terminal Voltage dq0 Components
i_{td}, i_{tq} and i_{t0}	Terminal Current dq0 Components
$Kp_d, Kp_q,$ $KI_d,$ and KI_q	Proportional Integral Constant of d-Axis And q-Axis

CHAPTER-1

OVERVIEW

1.1 Introduction

FACTS is new technology in power industries. The main function of this technology is to control and improve the power flow capability of the transmission line. FACTS depend on an assembly of ac/dc and/or dc/ac converters and/or high power ac switches. The converters are an assembly of different power semiconductor devices such as GTO, IGBT, MTO, and IGCT that perform the above-mentioned tasks. The main among them is dc/ac conversion and this operation is popularly known as an inverter. The inverter is a device which converts dc voltage into symmetrical ac voltage with desired magnitude and frequency.

Conventional voltage source inverter is a two- level inverter. Three phase two level inverter works in two modes i.e. 180° or 120° conduction mode. In order to eliminate harmonic frequencies, different modulation techniques are used for example SPWM, MPWM, Sinusoidal PWM, the third harmonic injected PWM, and space vector PWM. Increasing the switching frequency leads to the improvement of the voltage waveform. However these PWM techniques have drawbacks, switching at PWM will cause high switching losses in high power and high voltage converter circuits. Sinusoidal voltage can be achieved in two ways either by PWM technique or from several levels of voltage. The prior technique is used in two-level inverter and second is the approach towards MLI. Thus, MLI is an inverter where different voltage levels are used to obtain a sinusoidal voltage.

There is a vast scope in the application of voltage source MLI in high power application for example in utility system to control active and reactive power. STATCOM (STATIC synchronous COMPensator) is one of the FACTS devices which perform the above-mentioned task. A Static Synchronous compensator is a device which can control capacitive or inductive output current without affecting the ac system voltage. STATCOM uses a storage device such as a superconducting coil or capacitors. Sudden change in reactive power demand leads to voltage instability, underutilization of transmission line and power oscillations. The Large reactive current in the transmission system is one of the most prevalent problems, which increases

transmission losses and lowers the stability of a power system. The above-mentioned problems can be mitigated by the use of STATCOM. About 80% of the loads in power systems are inductive in nature. When these loads are switched on, huge reactive power demands occur. This demand is to be satisfied from the nearby reactive power source. If there is no nearby reactive power source the load will drag this power from the far end, this will increase current in the transmission line. The increase in the current of transmission line increases power loss, therefore, efficiency reduces. This increase in current also causes voltage regulation problem.

1.2 Literature Review

Multi-level Inverter is burning topic of the era and its implementation in FACTS devices is on the top of IEEE spectrum.

The concept of MLI came into existence in the year 1975. Nabae was the first person who introduces the concept of the multi-level inverter. This was developed while he was trying to improve the two-level inverter. He had used a neutral point of dc to construct three levels. This inverter was first presented as neutral point clamped three-level inverter. [1], [2], [3]. A lot of work is going on in the field of increasing efficiency and reducing Harmonic distortions.

The main topologies are DCMLI, FCMLI and CHBMLI and these topologies are reliable [1, 7]. Multi-level inverters reduce the harmonic content in the output ac voltage waveform and thereby reduce the size of filters [4]. As per IEEE 519 latest updates:

Table 1.1 Voltage Distortion Limits [9]

S.No.	Bus Voltage V at PCC (Point of common coupling)	Individual Harmonic (%)	Total Harmonic distortion (THD)(%)
1	$V \leq 1.0 \text{ kV}$	5.0	8.0
2	$1 \text{ kV} < V < 69 \text{ kV}$	3.0	5.0
3	$69 \text{ kV} < V < 161 \text{ kV}$	1.5	2.5
4	$161 \text{ kV} < V$	1.0	1.5

The THD for voltage ranging from 69kV to 161kV should be 2.5% as per IEEE 519 standard [9]. Along with optimal filter sizing High voltage; High power capability is possible while sacrificing the switching losses switching losses can be reduced by soft switching [6]. In [5] the NPC inverter has been modeled and effects of redundant switching states have been analyzed mathematically on dc capacitors voltages. With the increase in a number of levels if numbers of the pulse are increased the capacitor requirement reduces but this will increase magnetics[7]. The advantage of using multi-level inverter are their low voltage stress on switching devices, low rate of change of voltage in voltage source, more capacity, less interference [1]. In [3] carrier based closed loop control technique is developed for reducing switching losses by introducing dead time between switching period of each half cycle hence increasing the converter efficiency.

As per IEEE Facts (Flexible AC Transmission system) is defined as “a power electronics based system and other static equipment that provide control of one or more AC transmission system parameters to enhance the controllability and increase power capability”.

These Facts devices are classified as

1. Series compensator
2. Shunt compensator
3. Combined series compensators
4. Combined shunt compensators

Table1.2 Comparison of Various FACTS Devices [22]

S.No.	FACTS Device	Connection Type	Switching Device used	Application
1	STATCOM	Shunt	GTO	Voltage Control
2	SVC	Shunt	Thyristor	Voltage Control
3	SSSC	Series	GTO	Power Flow Control
4	TCSC	Series	Thyristor	Power flow control
5	UPFC	Shunt and Series	GTO	Voltage and Power flow control
6	TCPAR	Series and shunt	Thyristor	Power flow control

Multi-level inverters have lots of applications such as in FACTS (Flexible AC Transmission System) as active filters D-STATCOM (Distribution- STATic synchronous COMPensator), T-STATCOM (Transmission-STATic synchronous COMPensator), UPFC (Unified Power Flow Controller) and UPQC (Unified Power Quality Conditioning). Beyond FACTS as in conventional applications such as solar energy conditioning and Electrical drives where VFD control is required.

IEEE definition of STATCOM is a subset of the broad-based shunt connected controller which includes the possibility of an active power source or storage on the dc side so that the injected current may include active power [10]. In the year 1976 Gyugyi proposed the concept of STATCOM. In the case of D-STATCOM (Distribution synchronous STATic COMPensator) two-level bridge converter of low capacity can be used at much higher switching frequency [11]. These converters are connected at medium voltage bus using a step-up transformer. In the case of T-STATCOM as capacity is high the static switches must be triggered at low frequencies. So in T-STATCOM system three-level neutral point clamped inverter is used [11], [12], [13], [14]. In [15] author presents the analysis of dead-time how it effect the harmonics of three-level. NPC inverter. Hybrid-STATCOM with low voltage on dc side reduces the cost of the system [16]. Lots of theory are proposed for controlling STSTCOM such as p-q theory [19], [20], [21] and d-q theory [17], [3], [14], [18]. In [23] fixed modulation index based STATCOM is presented with variable dc capacitor voltage this STATCOM is used to compensate voltage fluctuations.

To minimize the voltage and current harmonics analysis of STATCOM based on Bessel's functions of the first kind is discussed in [24] in order to reduce the THD of STATCOM while considering MI (modulation index) fix. To damp out the low-frequency oscillation in power system STATCOM based damping stabilizers are designed and implemented in [25] stabilizer based on STATCOM is implemented to (RTDS) Real-Time digital simulator. In [26] STATCOM of 60 MVA is described which is implemented to Japanese bullet Train power station in order to reduce the negative sequence power, this is achieved by using two sets of 12 single phase inverter connected in a multi-stage fashion. This STATCOM has been in use since 2003 in central Japan Railways Company.

The novel design of STATCOM for suppressing the subsynchronous resonance caused due to series capacitors is discussed in [27]. Solar farms can also be used to increase the power transfer capability of transmission line in by reducing the reactive current flowing from generating

station this is discussed in [28]. Faults on the grid are random these faults causes instability in wind farms stability of induction generator is of prime importance their stability can be improved by using STATCOM. The controller for STATCOM of such situations is discussed in [29]. When STATCOM is working under transient condition prime importance is to increase the reactive power to its maximum until the voltage reaches to its nominal value this concept is implemented to post-fault conditions on induction machines connected to grid [30].

In [31] STATCOM for 40-MVA EAF in Tennessee, USA is implemented based on Cascaded H-Bridge inverter. This STATCOM is proposed for EAF (Electric Arc Furnace) analysis is based upon transient network analysis(TNA). Various artificial intelligence techniques are implemented for STATCOM controllers such as an artificial neural network (ANN), Fuzzy Logic controller and their combinations one such research is available for transient stability improvement using neural-fuzzy controller design [32]. Reactive power compensation is not the only issue that is to be tackled through the use of STATCOM, power oscillation is another problem this can be suppressed if the same STATCOM is connected to the system with ES (Energy Source). This ES is connected to the dc link of the converter and provide a small amount of active power during power oscillations. The ES can be capacitors, batteries or superconductors [33]. This literature suggests potential cost saving and comparison of different types of ES. In [34] the 48 pulse GTO based STATCOM and SSC is described in detail for reactive power compensation and voltage stabilization. In [35] the author discussed how they designs of 6.6kV transformerless 5-level STATCOM with pulse width modulation in Simulink and verified its waveform with the experimental setup. STATCOM is also very much useful in pf (Power Factor) correction of grid connected PCC (point of common coupling). In [36] about 300 publications are summarized and concluded that STATCOM is compensator that behaves dynamically it used for controlling dynamics of the system, the FACTS device can be used in four P-Q coordinate system. The various case study of different STATCOM installed in the world is mentioned in this review paper. In [37] the three cascaded legs are connected in star configuration and can work in unbalanced condition for achieving the target the value of active power in each phase is adjusted by adjusting the dc-link voltage. In [38] 48-pulse GTO converter is improved by switching the GTOs at fundamental frequency using angle control for a specific dead angle for controlling the reactive power by varying the RMS voltage of STATCOM. Comparison of STATCOM based on different converter topologies is done in [39] where true-48, quasi-48 pulse STATCOM and

cascaded H-Bridge comparison is done on the bases of THD number of switching devices and converter losses. One of the research works is on hardware implementation of NPC (neutral point clamped) multi-level inverter where low cost gate driver circuit is implemented using IRF 2110 IC [40].

1.3 Scope of Work

As there is vast scope in this topic one can go for converter topology, controller design and hardware implementation. Comparison of Multi-level Converters and selection of converter on THD bases, number of components, and switching losses is done while considering the challenges. Study of different converter topologies is done first thereafter analysis on Simulink model is done. Out of the different topologies one of the topologies is used in STATCOM. There after a topology is hardware implemented.

1.4 Aim and Objectives of Thesis

The three main objectives of this work are

- Simulation based analysis of different types of Multi-Level Inverters.
- Simulation based analysis of STATCOM using best suited Multilevel Inverter.
- A prototype of one H-bridge and one diode clamped inverter on hardware.

1.5 Organization of Thesis

This thesis is subdivided into 6 chapters:-

Chapter 1 comprises of introduction and recent developments. This chapter also comprises of the scope of work, aim and objective of thesis and organization of thesis.

Chapter 2 is on multi-level voltage source converter this chapter comprises of introduction about multi-level inverter in which requirement of MLI (multi-Level inverter) is discussed. After discussing introduction, classification of MLI is put forward here different topologies are discussed with their operating principle, mathematical analysis, features and applications. The different topologies comprise of DCMLI, FCMLI and CHBMLI.

Chapter 3 is on STATCOM. This chapter deals with an introduction to STATCOM its requirement, basic principle, Features and operation control. Basic principle discusses the

analogy between Electrical generator that is a synchronous machine and Electronic generator that is the inverter. Operation control discusses the type of control possible.

Chapter 4 is focusing on a simulation that is MATLAB Simulink based performance analysis. The very first topic of this chapter is simulation based analysis of different MLI topology. Here results of different topology for 48 pulses Three-Level inverter are discussed and compared on the basis of FFT analysis. Later on in this chapter Performance analysis of 48 pulse three-level based STATCOM is discussed. This will include Control algorithm and performance analysis.

Chapter 5 is on hardware implementation of single-phase H-bridge CMOS inverter and diode clamped three-Level three phase inverter. Here the waveform for inverters is matched with the simulation.

Chapter-6 Is about the conclusion, future scope, appendix and references.

CHAPTER-2

MULTI-LEVEL VOLTAGE SOURCE CONVERTERS

2.1 Introduction

Conventional VSI is referred to as two-level inverters. Increasing the switching frequency leads to better output voltage waveform. Various PWM switching strategies can be used to control harmonics. It is very difficult to operate VSI in high power and high voltage applications due to increased switching losses and constraints of device rating. Along with above-mentioned constraints there is a problem in series and parallel combinations of devices. Multi-level inverter started becoming the solution for high voltage, high power and reduced harmonic voltage waveform. The primary structure of multi-level inverter to obtain a sinusoidal voltage waveform is to assemble various levels of voltages, obtained from various capacitor voltage sources. Multi-level starts from three-level the two-level inverters are not considered as a MLI. The unique architecture of MLI helps in forming high voltage with lower harmonics with optimized magnetics sometimes even without the use of transformers or series switches.

2.2 Classification of MLI

Nahe introduces the first multilevel inverter that was the neutral clamped inverter. Several new topologies were developed after that but among them following three are superior.

- Diode-clamped or neutral clamped Multi-level inverter DCMLI.
- Capacitor clamped or Flying capacitor Multi-level inverter FCMLI.
- Cascaded H-Bridge Multi-level inverter CHBMLI.

2.2.1 DCMLI

As discussed earlier to get the ac sinusoidal voltage waveform different voltage levels are assembled together. This can be achieved by multilevel inverters. Multi-level inverter starts with a three-level inverter. One of the methods to achieve three-level is DCMLI is presented here. The desired magnitude of ac voltage can be achieved without a change in dc-link voltage.

Operation

The Logic diagram for the single phase three-level inverter is shown in Fig-2.1. One leg of three-level inverter behaves as single pole triple throw (SPTT) switch. The ac voltage V_{AN} when the pole is connected to upper throw (T1) is $V_{AN}=+V_s/2$, if it is connected to middle throw (T2) $V_{AN}=0$ and if it is connected to bottom (T3) $V_{AN}=-V_s/2$. Therefore it is possible to achieve three levels. As the load connected is inductive or capacitive the current could be in either direction it can flow out of the pole or into the pole. Voltages achieved are $+V_{dc}/2$ or 0 or $-V_{dc}/2$ and these voltages are independent of current as it is a voltage source converter or an inverter.

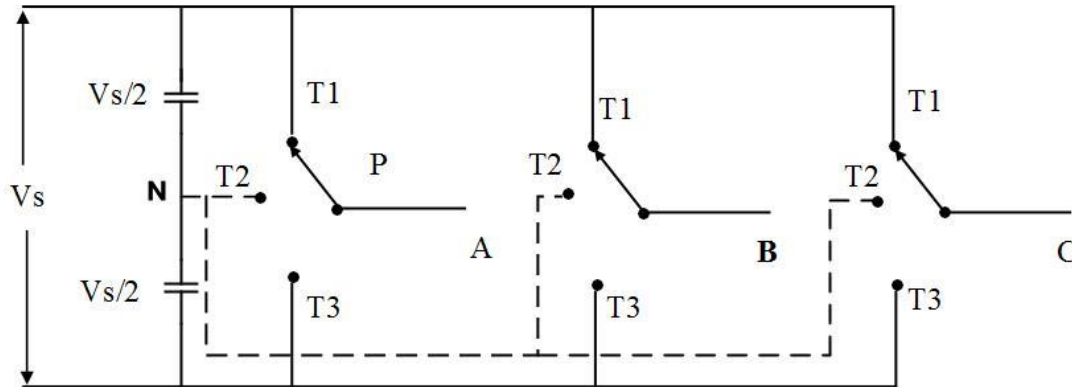


Fig- 2.1 Schematic Diagram for NPC Three-Level Inverter

Next challenge is what kind of switch which is required to synthesize this single pole triple throw (SPTT) switch. Every leg is an SPTT switch. Realization of SPTT switch is shown in Fig-2.2. Any of the static switches with off control can be used in the fabrication of SPTT switch as for example GTO (Gate Turn-Off Thyristor), IGBT (insulated-gate bipolar transistor), IGCT (Integrated Gate commutated Thyristor), and MTO (MOS Turn-Off Thyristor). These devices along with diode in anti-parallel are the perfect switching device for multilevel inverters realization. Let (Sa1, Sa2, Sa3 and Sa4) are switches of phase A and similarly for phase B and C as shown in Fig-2.3. The configuration of switch realized should be

- it must have Bidirectional current,
- Unipolar voltage ,and
- the voltage rating of the device should be V_{dc} .

The switching table is given in Table2.1.

Table 2.1 Switching Logic Table DCMLI

S.No	Voltage level	S1	S2	S3	S4
1	$+\frac{V_s}{2}$	On	On	Off	Off
2	0	Off	On	On	Off
3	$-\frac{V_s}{2}$	Off	Off	On	On

From the above table when S1 / S2 are on and S3 / S4 are off $+\frac{V_s}{2}$ volt is available at the pole with respect to neutral point for “ σ ” duration where “ $\sigma=180^\circ-2\beta$ ” conduction angle, when S2/S3 are on S1/S4 are off 0 volts is available at the pole with respect to neutral for “ 2β ” dead angle , and when S3/S4 are on and S1/S2 are off $-\frac{V_s}{2}$ volt is available at the pole with respect to neutral for “ σ ” where “ $\sigma=180^\circ-2\beta$ ”.

Hardware requirement per phase for n-level inverter is:

Table 2.2 Component List DCMLI

S.No	Component	Quantity
1	GTO (Gate turn-off thyristors)	(n+1)
2	Diodes	(n-1)*(n-2)
3	Capacitores	(n-1)

For three level n=3 GTO=4, Diodes=2 for clamping, Capacitores=2.

FEATURES of DIODE-CLAMPED

- High voltage rating required for blocking diodes.
- Unequal device rating.
- Sa1 conducts only when $V_o=V_s$ whereas Sa2 conducts over entire cycle for both $V_o=0$ and $V_o=V_s$.
- Unequal conduction duty requires different current rating device.
- Capacitor voltage unbalance.

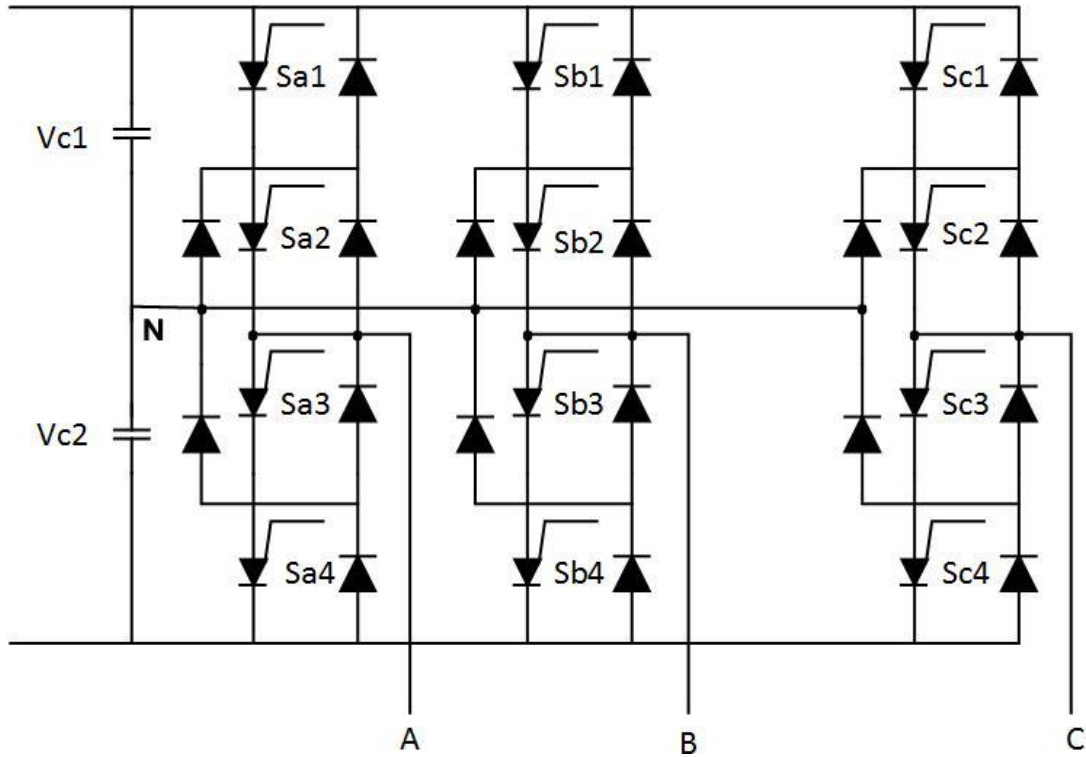


Fig-2.2 Realization of Three-Level DCMLI Using Power Semiconductor Devices

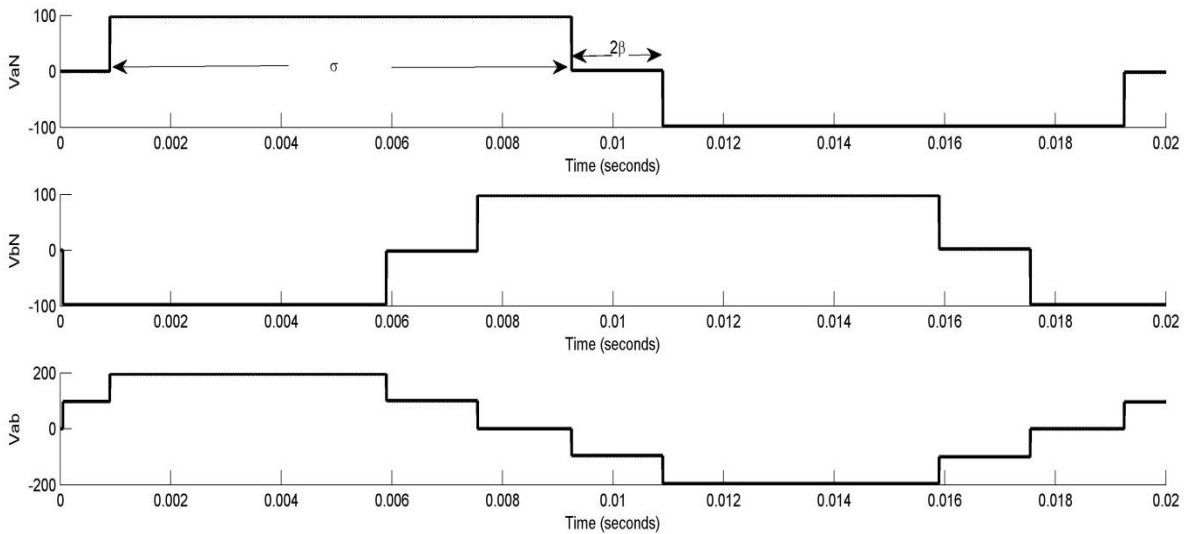


Fig-2.3 Waveform of DCMLI Three-Level Inverter

Mathematical Analysis

In above mentioned three phase three level VSC inverter at any instant Turn-Off device can handle any instantaneous inverter action whereas the anti-parallel diodes can handle rectification

action at any instant of time. Using Fourier series analysis of above phase voltage Van (phase to neutral voltage is defined as)

$$v_{a_0} = \frac{4}{\pi} \left(\frac{V_s}{2} \right) \left[\sin \frac{\sigma}{2} * \sin \left(\omega t + \frac{\sigma}{2} \right) - \frac{1}{3} \sin \frac{3\sigma}{2} * \sin 3 \left(\omega t + \frac{\sigma}{2} \right) + \frac{1}{5} \dots \right] \quad \dots(2.2.a.1)$$

For nth harmonics

$$v_{a_0} = \frac{4}{\pi} \left(\frac{V_s}{2} \right) \left[\frac{1}{n} \sin \frac{n\sigma}{2} * \sin n \left(\omega t + \frac{\sigma}{2} \right) \right] \quad \dots(2.2.a.2)$$

RMS of nth harmonics

$$v_{a_0} = \frac{2\sqrt{2}}{\pi} \left(\frac{V_s}{2} \right) \frac{1}{2} \sin \frac{n\sigma}{2} \quad \dots(2.2.a.3)$$

RMS of fundamental voltage component

$$v_{a_01} = \frac{2\sqrt{2}}{\pi} \left(\frac{V_s}{2} \right) \sin \frac{\sigma}{2} \quad \dots(2.2.a.4)$$

Generalized form of fundamental voltage component

$$v_{a_01} = \frac{2\sqrt{2}}{\pi} \left(\frac{V_s}{2} \right) \sin \frac{180^\circ - 2\beta}{2} \quad \dots(2.2.a.5)$$

Where, “ σ ” is conduction angle and “ β ” is the dead angle. By varying “ β ” the RMS value of ac voltage is controlled and thus power can be controlled.

Advantages

- Reduction in filter requirement.
- Enhancement in efficiency as switching occurs at the fundamental frequency.
- Controlling is easy.

Disadvantages

- With the increase in levels diode requirement increases.

2.2.2 FCMLI

As, in case of DCMLI three level inverter the different voltage levels of $+\frac{V_s}{2}$, 0, and $-\frac{V_s}{2}$ are possible there is one another topology through which these three levels have achieved this topology is known as the flying capacitor. The schematic diagram for FCMLI is shown in Fig-2.4. When switch S1/S2 are on together $+\frac{V_s}{2}$ volts level is possible when S2/S3 are on the 0-volt level is possible when S3/S4 are on $-\frac{V_s}{2}$ volts is possible. The circuit diagram for a realization of this topology is shown in Fig-2.5. Waveform for Output voltage of FCMLI topology is shown in Fig-2.6

Table2.3 Switching Logic Table FCMLI

S.No	Voltage level	S1	S2	S3	S4
1	$+\frac{V_s}{2}$	On	On	Off	Off
2	0	Off	Off	On	On
3	$-\frac{V_s}{2}$	Off	Off	On	On

Components requirement for n-level inverter per phase bases.

Table2.4 Component List FCMLI

S.No	Components	Quantity
1	GTO (Gate Turn-Off thyristors)	(n+1)
2	Capacitors requirement for dc-link	(n-1)
3	Capacitors	$N_c = \sum_{k=1}^{k=(n-1)} (n - k)$
4	Diode	0 for clamping purpose 1 diode per switch as feedback diode

Features of FCMLI

- Provides switch combination redundancy for balancing different voltage levels.
- Both real and reactive power flow can be controlled.

- Inverter control is complex.

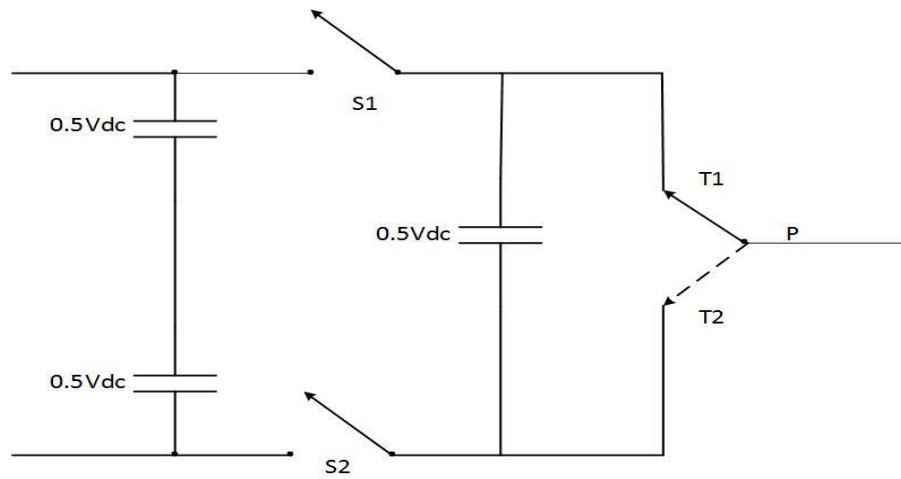


Fig- 2.4 Schematic Diagram for FCMLI Three-Level Inverter

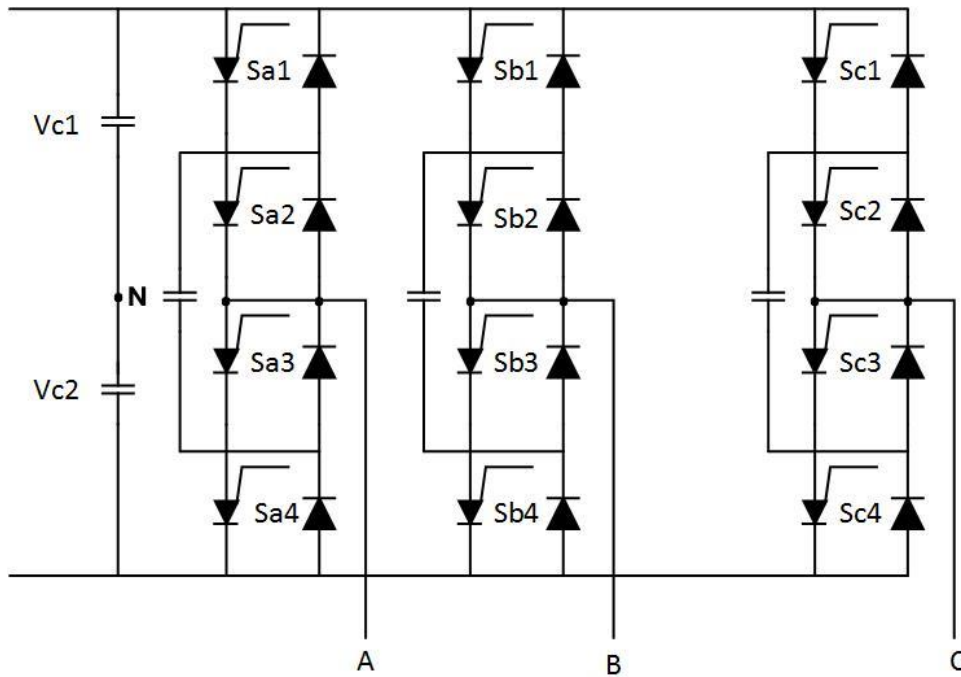


Fig-2.5 Realization of FCMLI Three-Level Inverter Using Power Semiconductor Devices

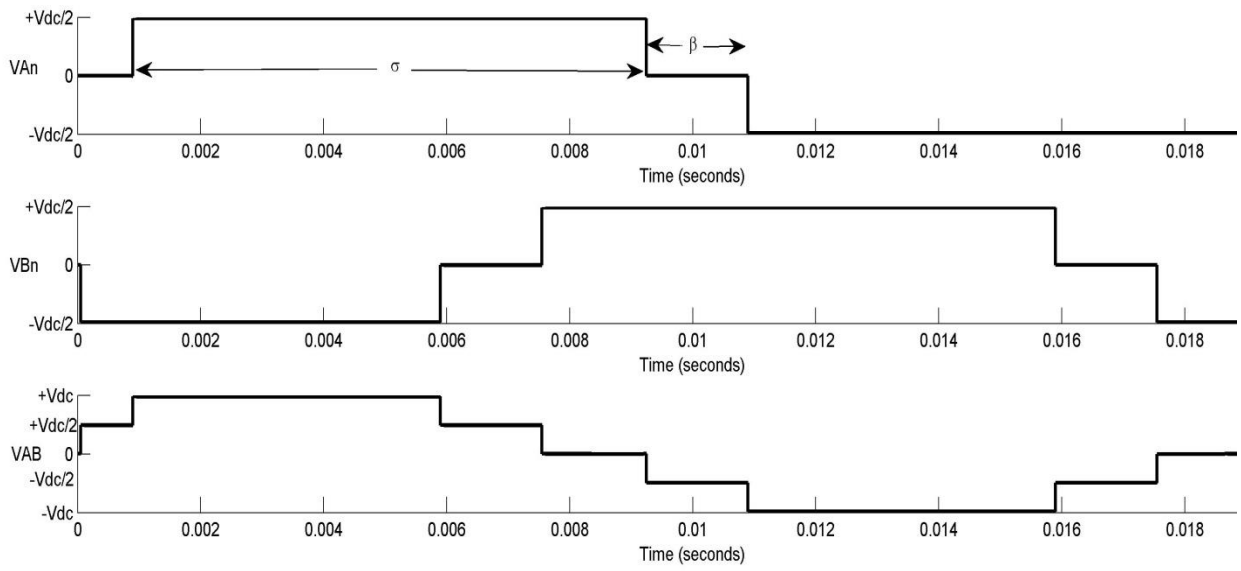


Fig.-2.6 Waveform of FCMLI Three-Level Inverter

By controlling the switching time output voltage RMS value of voltage can be controlled.

2.2.3 CHBMLI

The very basic inverter configuration that is full wave H-bridge inverter can be used as a multi-level inverter by connecting a number of H-bridge in series different levels can be achieved. The main purpose of this topology is to connect individual dc voltage supply to construct desired sinusoidal voltage wave shape. These individual dc sources are also known as several separate dc sources (SDCSs) consider for example solar PV panels. The basic difference in CHBMLI versus DCMLI and FCMLI is there is no requirement of the diode for clamping and capacitors for voltage-balancing.

Operation

Consider basic three-level CHBMLI topology Fig-2.7 shows this topology with three separate dc sources per phase. The phase voltage of the inverter is a summation of three individual ac voltages generated from individual H-bridge.

$$v_{An} = v_{A1} + v_{A2} + v_{A3} \quad \dots(2.2.c.1)$$

Each of the H-bridge modules of this topology is excited with the equal level of dc voltages. These are triggered by a square wave of different pulse width but of the same frequency. The modules are cascaded to give the final output voltage waveform as shown

in the Fig-2.8 The output voltage can be extended to nearly sinusoidal ac voltage waveform with an increase in a number of levels or pulses. by increasing the pulse or number of levels the THD can also be reduced to the prescribed limit as mentioned in IEEE Recommendations IEEE Standard 519 2014. The switching is carried out at the fundamental frequency.

Features

- Cascaded H-bridge multi-level inverter can be used as AC to Dc and DC to AC conversions. The separate dc source is very much suitable for renewable energy systems such as PV solar panels.
- Connecting single dc source to all the H-bridge module makes this topology faulty as there may come a situation where the particular switches of two or more modules may remain on simultaneously resulting in short circuit.

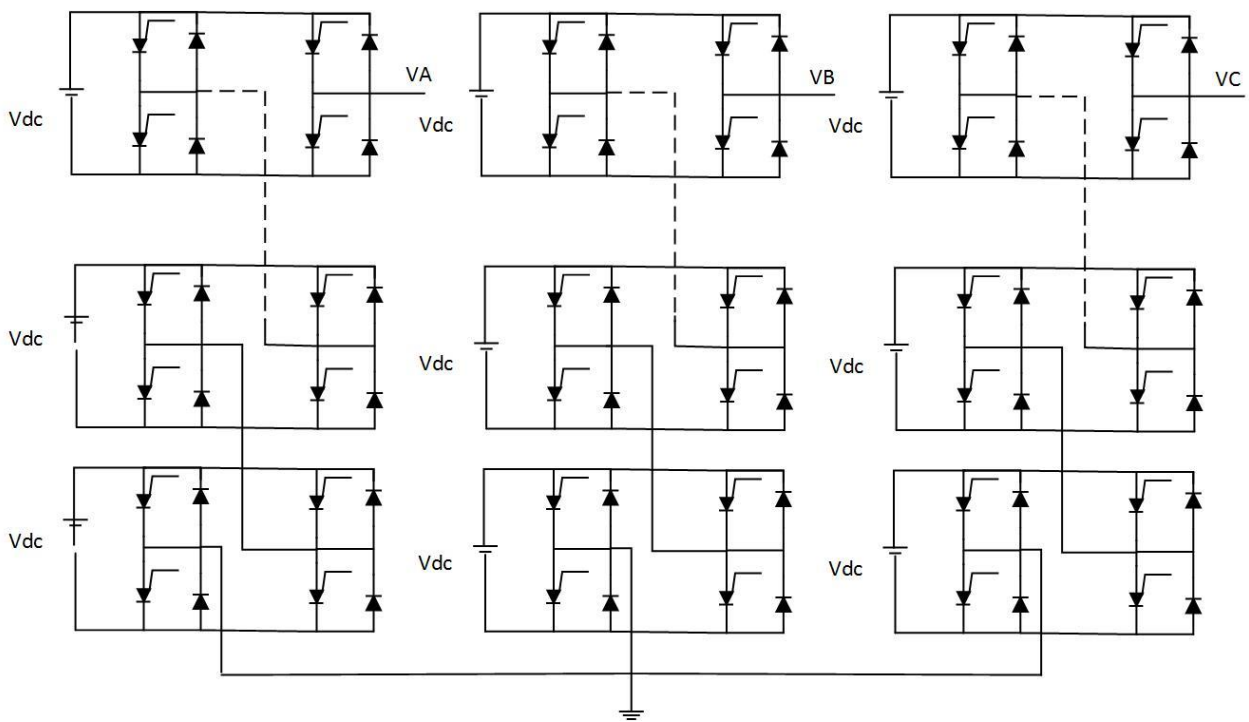


Fig-2.7 Realization of CHBMLI

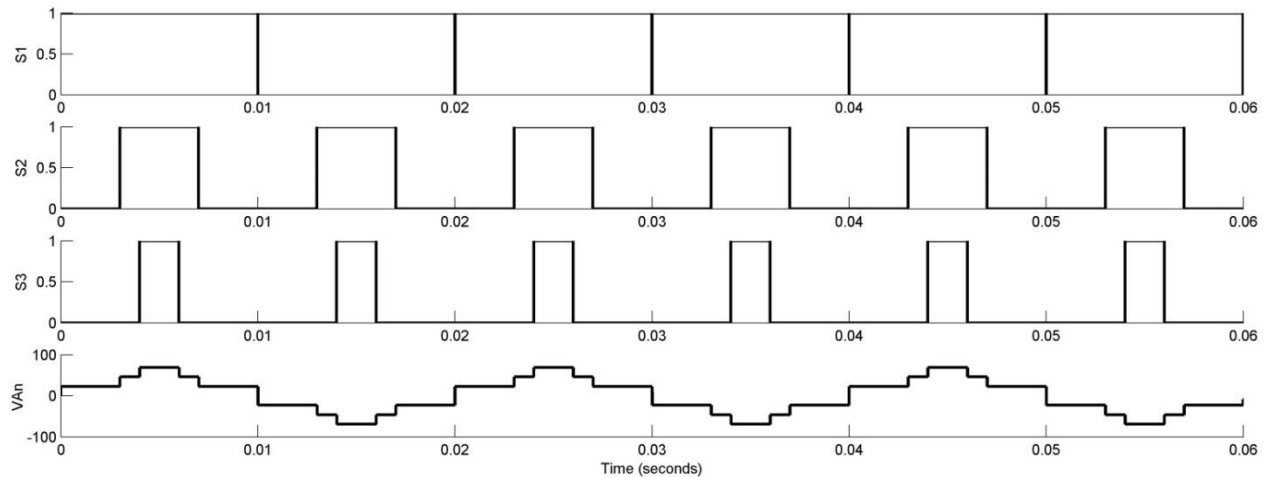


Fig-2.8 Waveform of CHBMLI

Advantages

- A number of components required are optimized as compared to DCMLI and FCMLI.
- To reduce the voltage stress on switches soft switching is possible in H-bridge connection.

Disadvantages

- Capacitor voltage balancing become complex as the number of controllers (mainly PI) increases with the number of capacitors acting as a separate voltage source.
- It requires separate dc source for each module so this limits its application to real power transfer at high voltage.

2.3 Applications

Power industry requires high voltage and high power in various applications. Some of the applications are mentioned below

- In renewable system solar PV panel generating dc power and MLI convert this to three phase ac for grid connection.

- Active and reactive power compensation for transmission network using FACTS technology in shunt compensators (STATCOM) and series compensators (SSSC) and their combination as UPFC (unified power flow control).
- Used in active filters as shunt (D-STATCOM), series filter (DVR) and combination UPQC (Unified Power Quality Control) for filtering voltage and current in nonlinear load network such as controlled rectifiers.
- Back to back intertie for asynchronous links.
- Using MLI in induction and synchronous motor speed control by VFD methodology.

CHAPTER-3

STATCOM (STATIC SYNCHRONOUS COMPENSATOR)

3.1 Introduction

Before the era of power electronics the reactive power demand by various industries was fulfilled by reactive power compensator that is a synchronous condenser. A synchronous condenser is an overexcited synchronous machine running on no-load. Sometimes, these machines are also known as phase modifiers, as they can adjust the phase by adjusting the dc excitation to the machines. The basic idea behind the development of STATCOM comes from synchronous condensers. A synchronous condenser is a machine that runs at no load so there is no active power required. The only active power required by this machine is to meet frictional losses. Various researchers in 90's mainly Dr. Lazlo Gyugyi and N.Hingorani were working in the same field. They come with the suggestion that instead of using the rotatory machine one can create a static machine which will produce reactive power in an efficient manner. This machine that is electronic generator is called STATCOM.

3.2 Basic Principle

Power system deals with various ups and downs in active and reactive powers. The conventional device used to suppress reactive power problem on the transmission line is a synchronous condenser. It is a synchronous motor with no load attached to the shaft. Consider the single line diagram for synchronous machine acting as a motor connected to the transmission line as shown in the Fig-3.1.

- V System bus voltage.
- X Machine synchronous reactance plus transformer reactance.
- E Internal EMF due to excitation.

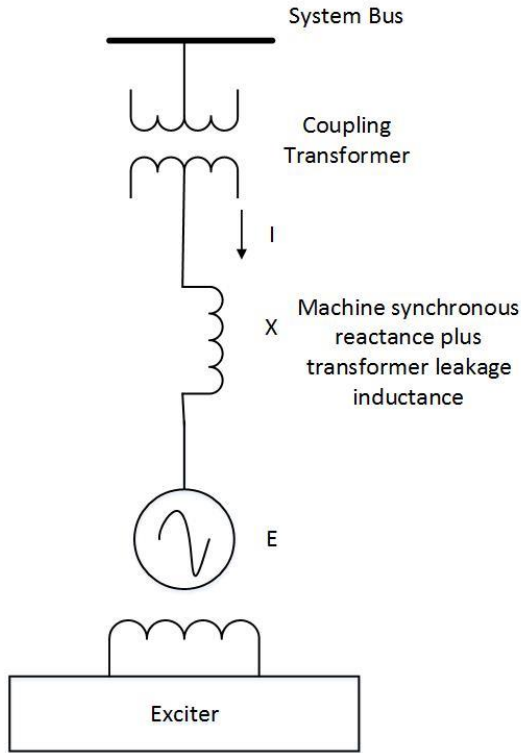


Fig-3.1 Synchronous Motor on No-load

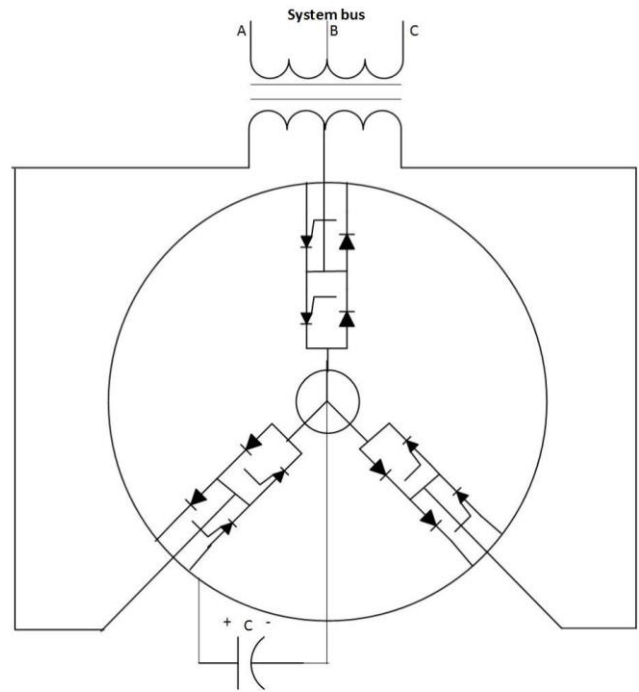


Fig-3.2 Electronic Generator

From Fig-3.1

$$I = \frac{V-E}{X} \quad \dots(3.2.1)$$

$$S = VI^* \quad \dots(3.2.2)$$

$$S = P + jQ \quad \dots(3.2.3)$$

$$Q = \frac{1-E}{X} V^2 \quad \dots(3.2.4)$$

To control the reactive power Excitation is to be controlled hence the magnitude of emf E of its internal voltage is to be varied. When there is a requirement of leading reactive power excitation is increased which in turns increases E Such that E is greater than V. During lagging reactive power demand excitation is reduced such that E is less than V.As there is no requirement of active power to generate reactive power the synchronous machine at no load is not an efficient method as it consumes active power to fulfill the mechanical losses.

STATCOM (STATIC synchronous COMPensator) previously called as STATCON (STATIC synchronous CONDensers) is originated from the same basic concept of the synchronous motor running at no-load here the excitation is replaced by capacitor C, and the output three phase voltage of fundamental frequency is produced by converter circuit. The output voltage on PCC of grid and converter are in phase. With variation in converters voltage reactive power is controlled. When converter voltage is more than system voltage current flows from the converter to a system and thus provides leading (capacitive) reactive power. Similarly when converter voltage is less than system voltage it will draw lagging (inductive) reactive power. If the magnitude of converter output voltage is equal to system voltage reactive power is zero. The ac voltage generated by dc to ac converter (electronic generator) uses a capacitor as a storage device. Till today lots of VSC (voltage source converters) used for STATCOM design such as DCMLI, FCMLI and CHBMLI as discussed above.

Features of STATCOM

- Provide leading reactive power even at low voltage this accounts for the wide operating range.
- If storage device for example superconducting coil or capacitor is replaced by battery both active as well as reactive power can be compensated.

3.3 Operation and Control

There are two control methodologies for controlling STATCOM

a) Type 1

In this control methodology two converters are connected in series the magnitude can be varied by varying different values of “ α ” for two converters. The control angles of vsc1 and vsc2.

$$v_{lead} = V\angle -\delta + \alpha \quad \dots(3.3.a.1)$$

$$v_{lag} = V\angle -\delta - \alpha \quad \dots(3.3.a.2)$$

Where, “ 2α ” is the angle between two voltage source converters and it is controlled for variation in total ac voltage. “ δ ” is load angle.

$$v_{c1} = 2n \left(\frac{p\sqrt{6}}{6\pi} \right) \cos \left(\frac{\pi}{48} \right) v_{dc} \cos \alpha \quad \dots(3.3.a.3)$$

Cos α is modulation index.

$$v_p = kV_{dc} \cos \delta \quad \dots(3.3.a.4)$$

$$v_r = -kV_{dc} \sin \delta \quad \dots(3.3.a.5)$$

From equation

$$\frac{d}{dt} \begin{bmatrix} i_p \\ i_r \end{bmatrix} = \begin{bmatrix} -\frac{R\omega_B}{X} & 0 \\ 0 & -\frac{R\omega_B}{X} \end{bmatrix} \begin{bmatrix} i_p \\ i_r \end{bmatrix} + \begin{bmatrix} u_p \\ u_r \end{bmatrix} \quad \dots(3.3.a.6)$$

$$u_p = G_{ci}(s)(i_p^* - i_p) \quad \dots(3.3.a.7)$$

$$u_r = G_{ci}(s)(i_r^* - i_r) \quad \dots(3.3.a.8)$$

Where $G_{ci}(s)$ is

$$G_{ci}(s) = \frac{K_{ci}(1+sT_{ci})}{sT_{ci}} \quad \dots(3.3.a.9)$$

$$e_p = -\frac{\omega X}{\omega_B} i_r + \frac{X}{\omega_B} u_p \quad \dots(3.3.a.10)$$

$$e_r = \frac{\omega X}{\omega_B} i_p - \frac{X}{\omega_B} u_r \quad \dots(3.3.a.11)$$

$$k = \alpha = \frac{\sqrt{e_p^2 + e_r^2}}{V_{dc}} \quad \dots(3.3.a.12)$$

$$\delta = -\tan^{-1} \frac{e_r}{e_p} \quad \dots(3.3.a.13)$$

$$T_{ci} = \frac{L}{R} \quad \dots(3.3.a.14)$$

$$K_{ci} = \frac{L}{T_r} \quad \dots(3.3.a.15)$$

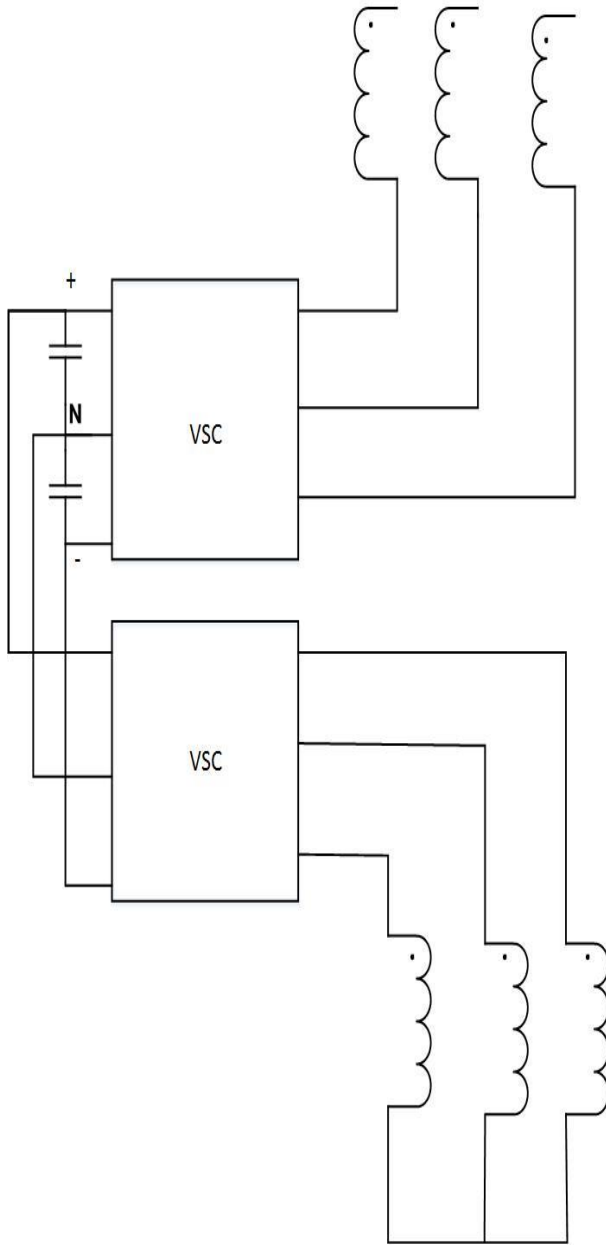


Fig-3.3 Realization of Type 1 STATCOM

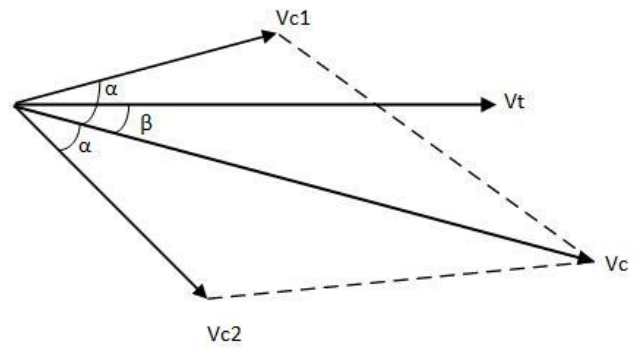
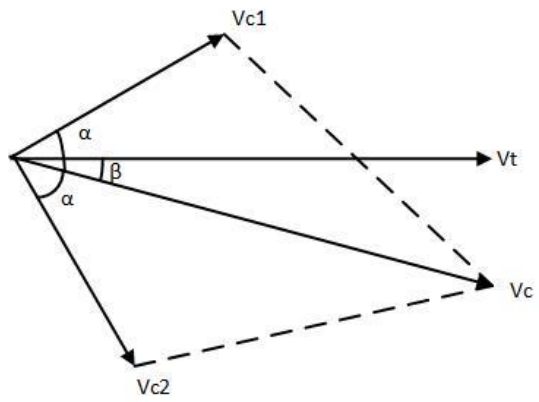
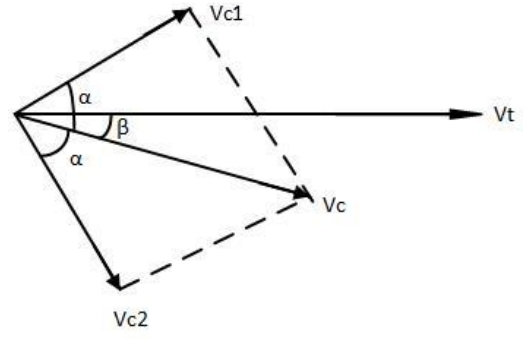


Fig-3.4 Phasor Diagram for STATCOM

$$i_p = \frac{1}{1+sT_r} i_p^* \quad \dots(3.3.a.16)$$

$$i_r = \frac{1}{1+sT_r} i_r^* \quad \dots(3.3.a.17)$$

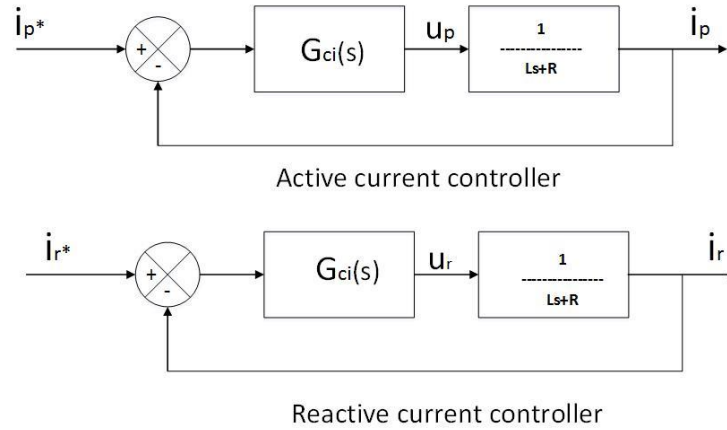


Fig-3.5 Current Controller for Active and Reactive Current

b) Type 2

$$i_Q + ji_D = (i_p - ji_r)e^{j\theta} \quad \dots(3.3.b.1)$$

$$L \frac{d\hat{I}'}{dt} + j\theta \cdot L\hat{I}' + (R + j\omega_0 L) = V_s + j0 - kv_{dc}e^{j\delta} \quad \dots(3.3.b.2)$$

$$\hat{I}' = i_p - ji_r \quad \dots(3.3.b.3)$$

$$L \frac{di_p}{dt} + Ri_p + \omega Li_r = V_s - kv_{dc} \cos\delta \quad \dots(3.3.b.4)$$

$$L \frac{di_r}{dt} + Ri_r - \omega Li_p = kv_{dc} \sin\delta \quad \dots(3.3.b.5)$$

$$\frac{cdv_{dc}}{dt} + Gv_{dc} = k(i_p \cos\delta - i_r \sin\delta) \quad \dots(3.3.b.6)$$

Where $\omega = \omega_0 + \frac{d\theta}{dt}$

v_{dc} , i_p , and i_r are constant if v_s and δ are constants.

$$v_{dc_0} = \frac{k}{G} (i_{p_0} \cos\delta_0 - i_{r_0} \sin\delta_0) \quad \dots(3.3.b.7)$$

$$i_{p^0} = \frac{(R + \frac{k^2}{G} \sin^2 \delta)}{(\omega L + \frac{k^2}{2G} \sin 2\alpha)} i_{r_0} \quad \dots(3.3.b.8)$$

$$i_{r_0} = \frac{V_{s0} \left(\omega L + \frac{k^2}{2G} \sin 2\delta_0 \right)}{R^2 + \frac{k^2 R}{G} + \omega^2 L^2} \quad \dots(3.3.b.9)$$

$$X_{ST} = \frac{R^2 + \frac{k^2 R}{G} + \omega^2 L^2}{\omega L - \frac{k^2}{2G}} \quad \dots(3.3.b.10)$$

$$\alpha_0 = -45^\circ \quad G = 0$$

$$X_{ST} = -2R$$

$$V_{dc0} = \frac{k}{G} \frac{(R \cos \alpha_0 - \omega L \sin \alpha_0) V_{s0}}{(R^2 + \frac{k^2 R}{G} + \omega^2 L^2)} \quad \dots(3.3.b.11)$$

$$E_s = k V_{dc}, \quad k = \frac{p}{6} \cdot \frac{\sqrt{6}}{\pi}$$

Using above approach STATCOM is developed in MATLAB Simulink environment and same is discussed in Next chapter about MATLAB Simulink Performance analysis.

CHAPTER-4

SIMULINK BASED PERFORMANCE ANALYSIS of MLIs

4.1.Simulation of Multilevel Inverters

Behavior and challenges of various converter topologies are put forward by developing the discrete component model on MatlabSimPowerSystemsToolbox.

4.1.1 DCMLI Three Level 48-Pulse VSC.

The block diagram for 48-pulse three-level converters is shown in the Fig-4.1 given below.

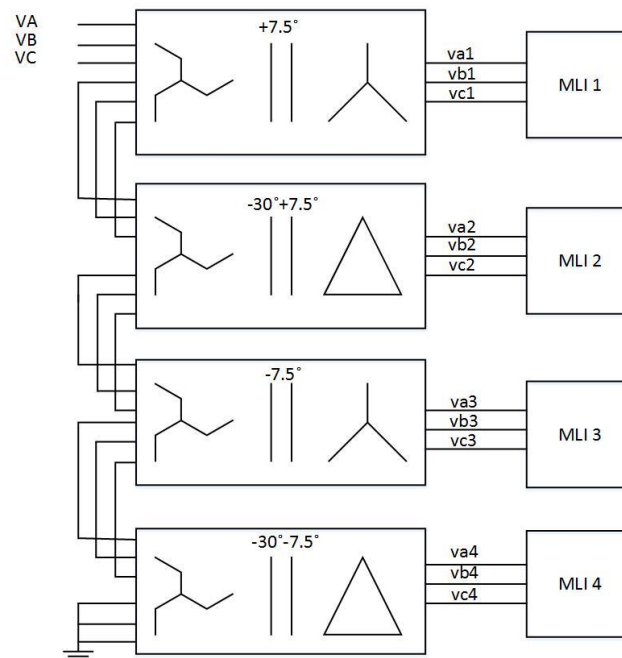


Fig-4.1 Realization of 48-Pulse Three-Level Inverter

The three-level inverter as discussed in section (2.2.1) is connected to the zig-zag transformers so that the voltages of different MLI can be connected in series with a phase lag of 7.5° . The proposed model consist of four three-level inverters along with four zig-zag transformers as shown in Fig-2(a) .The waveform for 48-pulse three-level inverter with and without transformer at the ac end is shown in Fig-4.2. The complete 48-pulse converter consists of two series star and two series delta transformers which are configured using a zig-zag transformer. Each three-level neutral clamped converter of Fig-2.2 is connected to LV (Low Voltage) side of transformers and

HV (High Voltage) side of the transformer is connected in series. On the dc side all converters are connected to common dc link center tapped at 'Vdc/2'. Firing angle to converter 1 and 2 are +7.5 ahead which gives phase angle of +7.5° to converter 1 and -22.5° to converter 2. Firing angle to converter 3 and 4 are delayed by a phase angle of -7.5° which gives phase angle of -7.5° to converter 3 and -37.5° to converter 4. Fig-4.3 and Fig-4.4 show the FFT (Fast Fourier Transform) analysis of this converter.

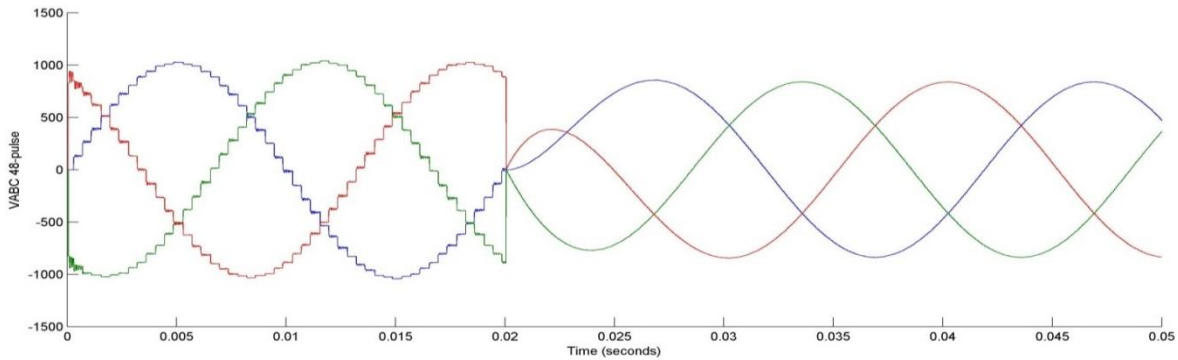


Fig-4.2 Waveform of 48-Pulse Three-Level DCMLI

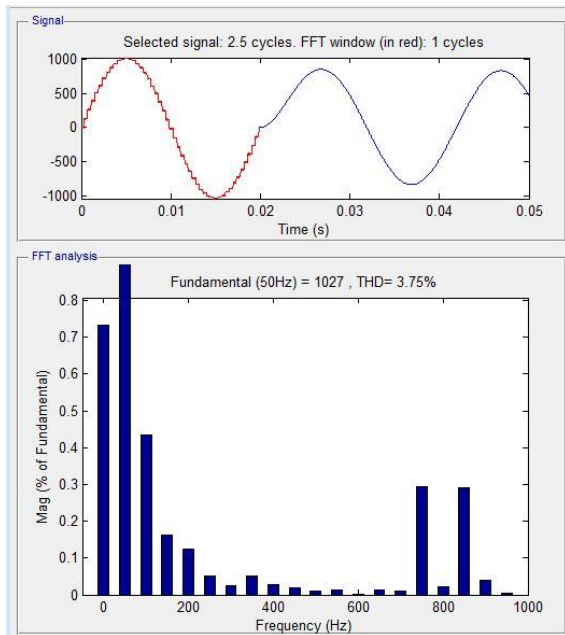


Fig-4.3 FFT (Fast Fourier Transform) Analysis of 48-Pulse DCMLI without Transformer

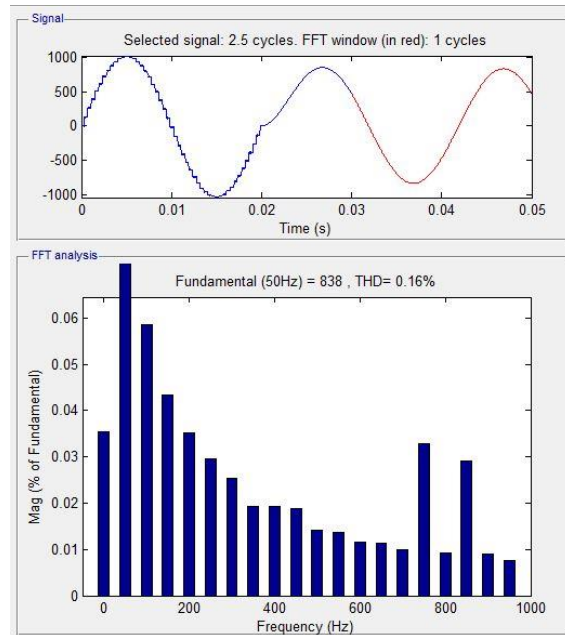


Fig-4.4 FFT (Fast Fourier Transform) Analysis of 48-Pulse DCMLI with Transformer

4.1.2 FCMLI Three Level 48-Pulse Voltage Source Converters.

The flying capacitor based three-level 48 pulse MLI similar to Diode-clamped MLI. The only difference is that the individual Diode-clamped MLI are replaced by flying capacitor MLI. The waveform for three phase 48 pulse ac output voltage using flying capacitor arrangement with and without transformer is shown in Fig-4.5. Fig-4.6 and Fig-4.7 show the FFT (Fast Fourier Transform) analysis of this topology.

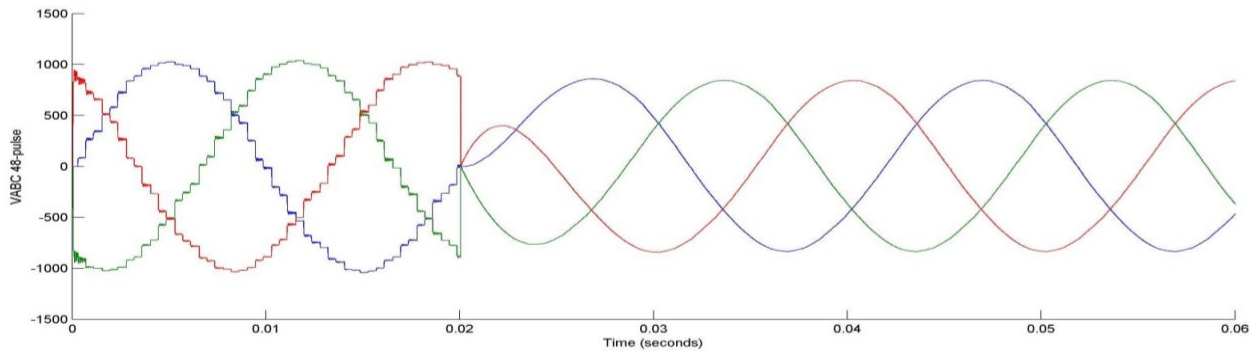


Fig-4.5 Waveform of 48-Pulse Three-Level FCMLI

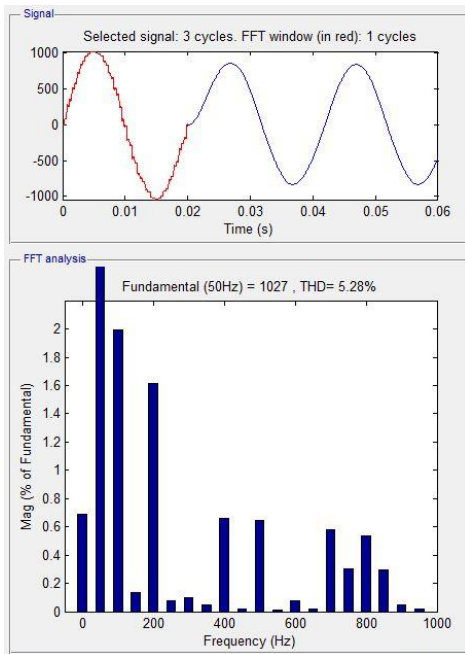


Fig-4.6 FFT Analysis of 48-Pulse Flying Capacitor Inverter without Transformer

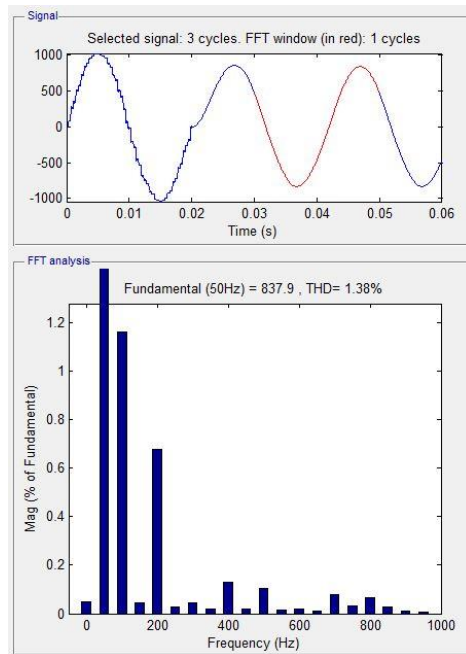


Fig-4.7 FFT Analysis of 48-Pulse Flying Capacitor Clamped Inverter with Transformer

4.1.3 20-Level CHBMLI

Here the realization of 20-level cascaded H-bridge inverter is carried out. Each H-bridge produces certain level rectangular wave for a certain duration. The model for 20 level cascaded H-bridge converters is designed in a similar way as discussed in Fig-2.6 using Matlab/SimPowersystem toolbox.

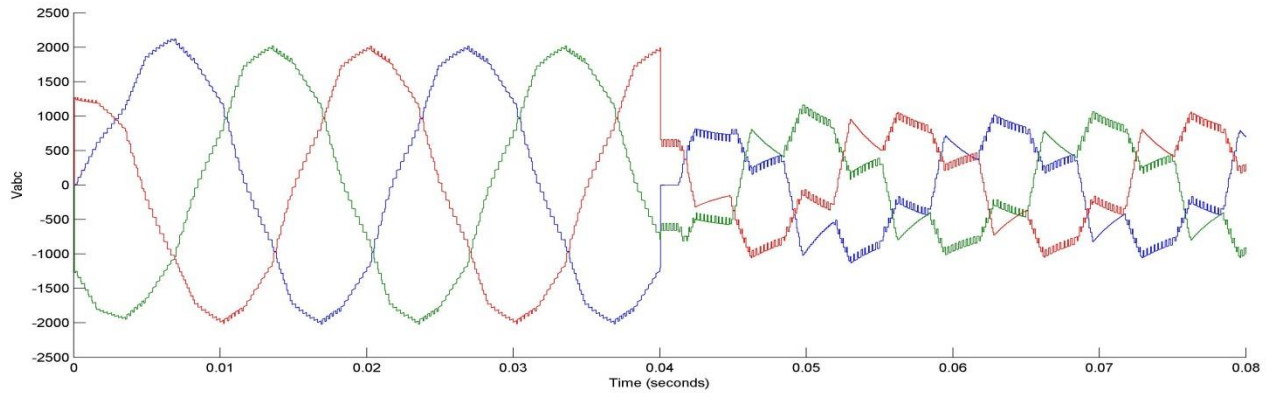


Fig-4.8 Waveform of 20-Level Cascaded H-Bridge Inverter

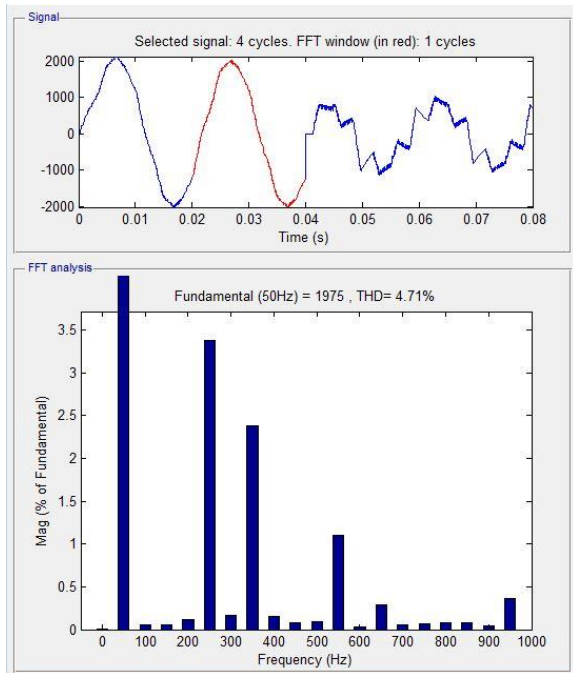


Fig-4.9 FFT Analysis of 20 Level Cascaded H-Bridge Inverter without a Transformer.

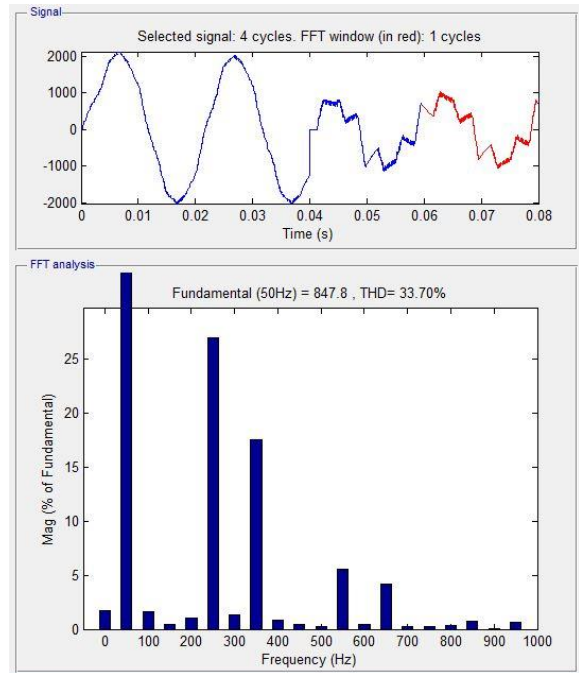


Fig-4.10 FFT Analysis of 20 Level Cascaded H-Bridge Inverter with a Transformer.

Maintaining constant voltage of each source to an equal level is a difficult task as it requires as many numbers of PI controllers as many capacitors acting as a voltage source. Fig.4.8, Fig.4.9 and Fig.4.10 shows the output ac voltage waveform, FFT analysis of converter with and without transformer respectively. The THD level is not so good but is within the prescribed limit.

Table4.1 Comparison Table of Different Topologies

S.No	Topology	THD (%)	Challenges
1	Diode-clamped three-Level 48-pulse converter	Without Transformer=3.75 With Transformer=0.16	Less number of capacitors fewer difficulties
2	Flying capacitors three-level 48 pulse converter	Without Transformer=5.28 With Transformer=1.38	As compared to diode clamped a number of capacitors are more so more PI controller required selection of controller constant become difficult.
3	Cascaded H-bridge 20 level converter	With Transformer=4.71 With Transformer=33.70	Individual supply for each bridge required a maximum number of the voltage source. To maintain their voltage levels number of PI controller increases.

4.2. Simulation of STATCOM

After analyzing the three converters topology mentioned above and looking into their results and advantages and disadvantages it is concluded that the best waveform with lower THD is possible in diode-clamped. This topology also requires minimum PI controllers to maintain the capacitor voltage to a fixed value. The model under consideration is shown in Fig- 4.11

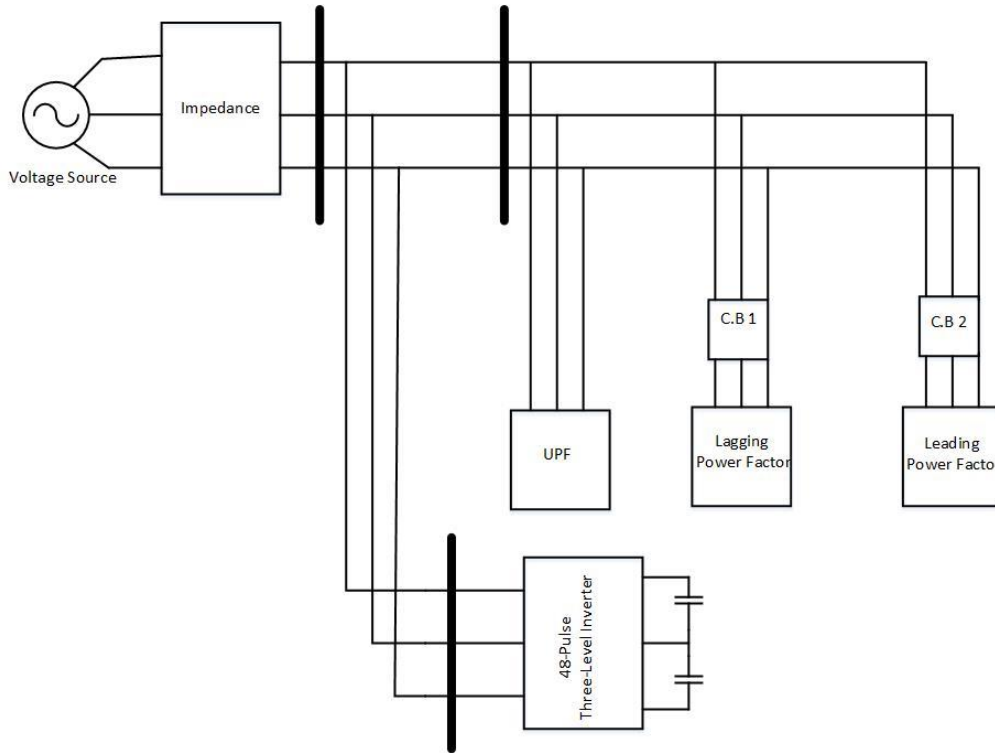


Fig-4.11 Model under Consideration

The control strategy used here is Type 2 current controller. The configuration for the STATCOM is same as for three-level DCMLI 48 pulse converters.

4.2.1. Control Algorithm

a) The Dc-Link Voltage Controller

Capacitors are connected on the dc side of the converter these capacitors holds dc voltage. For dc link voltage to be flat “ v_{dc} ” is compared with “ v_{dc}^* ” the reference dc voltage. The error signal so generated is controlled through PI (proportional Integral) controller this controller estimates the value of “ i_d^* ”. This “ i_d^* ” is fed to decoupled current controller. When dc link voltage is less than “ v_{dc}^* ” “ i_d^* ” increases and share a small amount of active power with a capacitor to charge the capacitor and thereby maintaining the dc link voltage to reference dc voltage “ v_{dc}^* ”.controller is shown in Fig-4.12 and its mathematical equation is

$$i_d^* = kp_{dc}(v_{dc}^* - v_{dc}) + kI_{dc} \int (v_{dc}^* - v_{dc}) dt \quad \dots(4.2.1.a)$$

b) AC Voltage Controller

One of the applications of STATCOM is constant ac terminal voltage. In order to obtain ac terminal voltage ' v_t ' constant PI controller is used to drag this voltage to its reference ac ' v_t^* '. PI controller compare the actual value with the reference value and generate signal ' i_q^* '. It is injected to the decoupled current controller.

$$i_q^* = kp_{ac}(v_t^* - v_t) + kI_{ac} \int (v_t^* - v_t) dt \quad \dots(4.2.1.b)$$

Block diagram for ac voltage controller is shown in Fig-4.12.

c) Decoupled Current Controller

' v_{td} ', ' v_{tq} ' and ' v_{t0} ' voltages and ' i_{td} ', ' i_{tq} ' and ' i_{t0} ' are calculated using park's transformation from terminal voltage v_{tabc} and terminal current i_{tabc} .

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - 120) & \sin(\theta + 120) \\ \cos\theta & \cos(\theta - 120) & \cos(\theta + 120) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad \dots(4.2.1.c.1)$$

$$\begin{bmatrix} i_{td} \\ i_{tq} \\ i_{t0} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin(\theta - 120) & \sin(\theta + 120) \\ \cos\theta & \cos(\theta - 120) & \cos(\theta + 120) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad \dots(4.2.1.c.2)$$

PLL (Phase lock loop) is used to obtain $\sin\theta$ and $\cos\theta$ it is used for synchronization purpose.

The instantaneous active and reactive powers for the system under consideration is given as

$$P = v_{td} i_d + v_{tq} i_q \quad \dots(4.2.1.c.3)$$

$$Q = v_{td} i_q - v_{tq} i_d \quad \dots(4.2.1.c.4)$$

The dq0 voltage and current are calculated using above mentioned park's transformation.

As frame of terminal voltage is aligned to d-axis ' v_{tq} ' is zero. Equation for reference voltage is

$$v_d^* = v_{td} - Ri_d - \omega Li_q - Kp_d (i_d^* - i_d) - KI_d \int (i_d^* - i_d) dt \quad \dots(4.2.1.c.5)$$

$$v_q^* = v_{tq} - Ri_q + \omega Li_d - Kp_q (i_q^* - i_q) - KI_q \int (i_q^* - i_q) dt \quad \dots(4.2.1.c.6)$$

' Kp_d ', ' Kp_q ', ' KI_d ', and ' KI_q ' constant for proportional controller and integral time constant of PI (proportional integral) controller. Block for decoupled controller in given Fig .4.12.

d) Phase Angle Calculation

For constant dc link voltage converter is fired at angle ' δ^* '. ' δ^* ' is given as

$$\delta^* = \tan^{-1} \left(\frac{v_d^*}{v_q^*} \right) \quad \dots(4.2.1.d.1)$$

From equation 5

$$v_{c1} = \frac{2\sqrt{2}}{\pi} \left(\frac{V_s}{2} \right) \sin \frac{180^\circ - 2\beta}{2} \quad \dots(4.2.1.d.2)$$

Reactive power is controlled by controlling dead angle ' σ ' as it controls the RMS value three phase MLI VSC output voltage. ' n ' is transformer's ratio and ' p ' is a number of the pulse. Controller for this is given in Fig-4.12.

e) DC Link Capacitor Voltage Balancer

Power loss in positive and negative connected switch should for the efficient converter. This is achieved by capacitor voltage balance this will also reduce voltage stress on the converter. The voltage across two of the capacitors is compared and an error signal is derived from PI controller. This will give ' $\Delta\delta^*$ ' and added to ' δ^* '. Controller block diagram for dc link capacitor voltage balance is given in Fig-4.12.

f) Pulse Generator

To maintain the conduction angle ' $\sigma=180-2\beta$ ' converter is triggered at ' $-\delta+\Delta\delta$ '. The block diagram is shown in Fig -4.12.

4.2.2. Performance Analysis

To investigate the behavior of STATCOM for different loading situations model is developed in MATLAB/SimPowerSystemsToolbox. Ratings and specifications for STATCOM design are given in appendix Table6.1. Unity power factor load is continuous, 0.707 power factor lagging load for 0.2 sec from 0.4 to 0.6 sec, and 0.707 leading load for 0.2 sec from 0.8 to 1 sec. The loads are switched on and off using circuit breakers with internally defined timing. From very basics Q (reactive power) is positive for lagging loads and Q (reactive power) is negative for leading loads. During 0.4 to 0.6 sec lagging load is switched on and it is obvious that there is a fall in terminal voltage. This voltage instability during the switching of the lagging load is mitigated by providing the reactive power. During this situation STATCOM behaves as leading load as can be depicted from the waveforms in Fig-4.13. During 0.6 to 0.8 sec only UPF load is acting and voltage is stable in this regime. During 0.8 to 1 sec leading load is switched on and there is a rise in voltage. This type of voltage instability is compensated by absorbing the reactive power. During this period STATCOM is behaving as lagging load.

Table4.2 THD Comparison for Different Loading.

Sno	Type of load	Timing	THD
1	UPF (Unity power factor) load	(0-0.4 sec) (0.6-0.8sec)	2.03%
2	Lagging power factor	0.4-0.6 sec	2.20%
3	Leading power factor	0.8-1 sec	1.08%

It is clearly visible from the waveform pattern that reactive current is injected by STSTCOM into the system during lagging load period. And during the leading load period reactive current is taken out from the system and absorbed by converter capacitor.

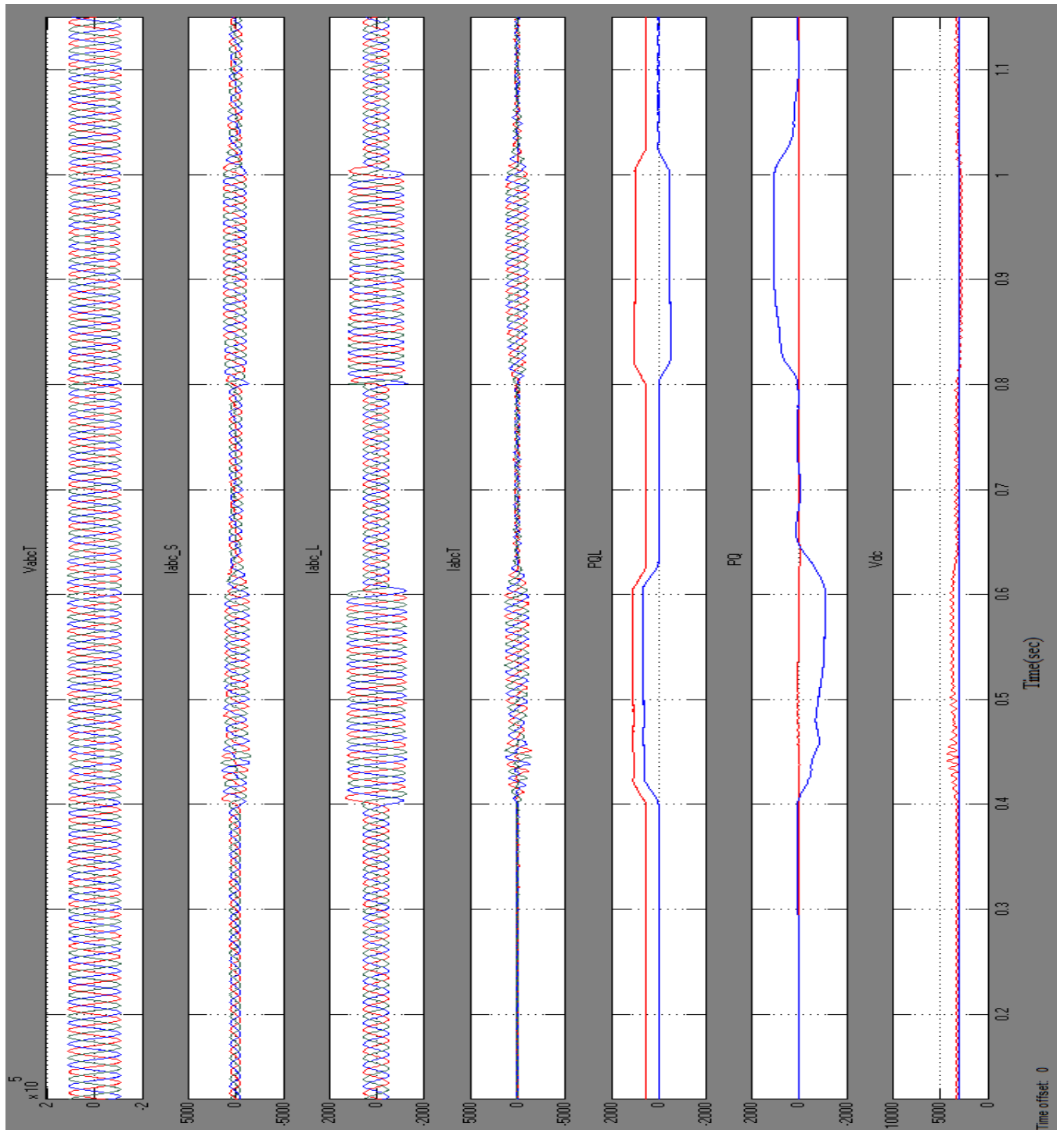


Fig-4.13 Waveform of STATCOM Performance Analysis

CHAPTER-5

HARDWARE IMPLEMENTATION

5.1. Introduction

The prototype H-bridge inverter and three level DCMLI is developed on zero PCB using Arduino mega 2560. These are implemented while considering the Simulation model into account.

5.2. Single Phase CMOS H-Bridge Inverter

CMOS (Complementary MOS) is a combination of P channel and N channel MOSFETs. P channel and N channel MOSFETs are connected in series in two of the leg. The value of different components and their specifications are mentioned in appendix table.

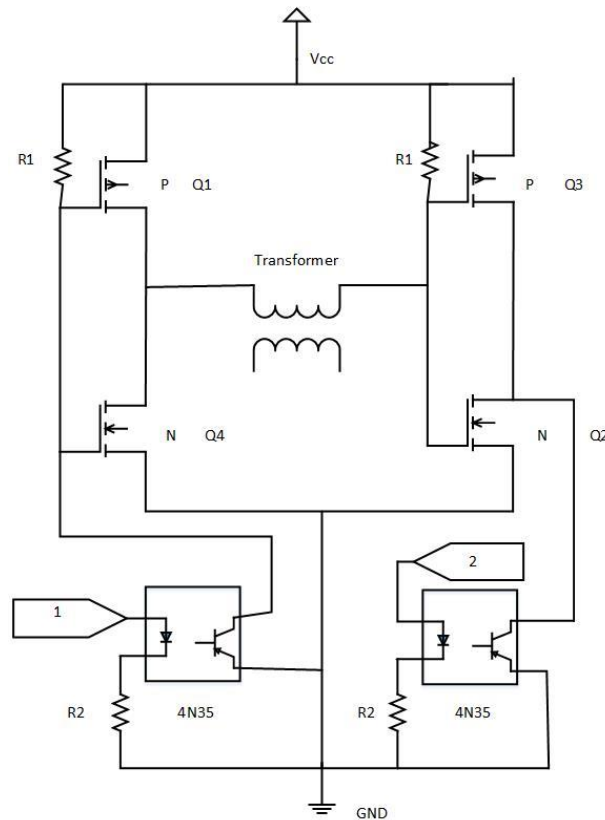


Fig-5.1 Circuit Diagram of Single Phase CMOS H-bridge Inverter

Switching pulses are generated by Arduino by interfacing it with the MATLAB Simulink model. Two pulses of 20msec time period and 50% duty cycle with 180° phase shift are produced in Simulink. Later on this Simulink model is deployed to Arduino mega 2560. Pin number 8 and 9 is selected for the output pulse terminals. These pulses are then isolated from the power module using Opto-coupler IC 4N35. The biasing resistance value is given Appendix. A 24 volt 3 ampere 220volt transformer is used to step up the voltage. When pulse 1 is high Q4 and Q3 are on whereas when pulse 2 is high Q1 and Q2 are on. This will generate AC voltage of square waveform. AN ac load that is an incandescent lamp of 15watt is connected across the transformer high voltage terminals. Simulation waveform of H-Bridge inverter is shown in Fig-5.2.

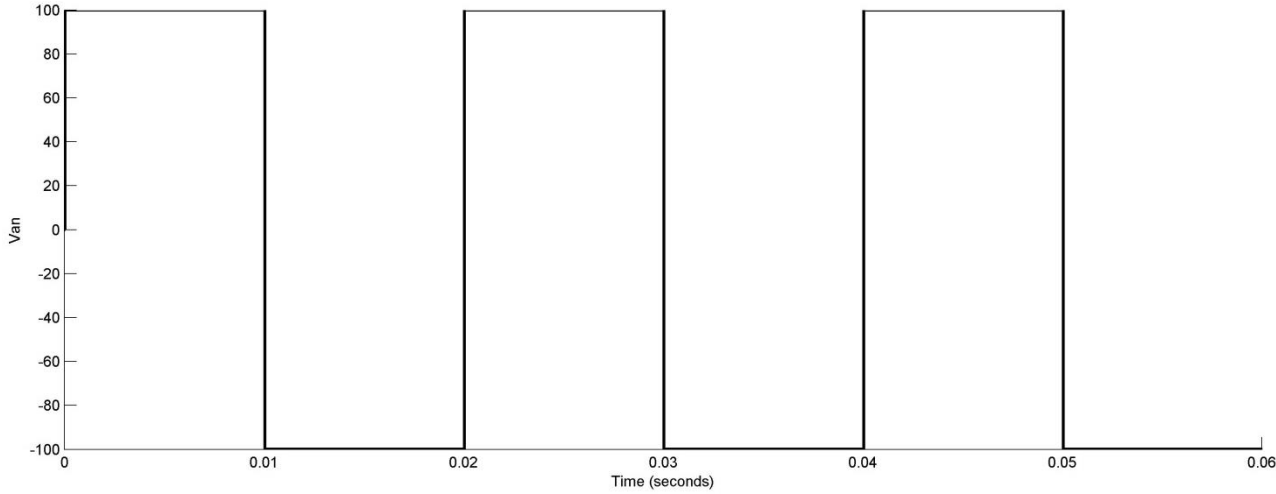


Fig-5.2 Simulation Waveform of H-Bridge Inverter

The waveform of Single phase square wave inverter is shown in Fig-5.3.

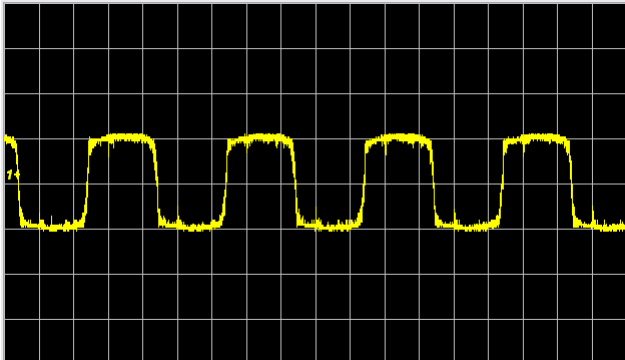


Fig-5.3 Waveform of Single Phase CMOS Based Inverter

Similar three H-bridge inverter are to be connected in series to form three level single phase and total of nine such converters to form three level three phase.

5.3. Three Phase Three-Level DCMLI

Circuit diagram for three level diode clamped inverter is shown in the Fig-5.4. The model is first simulated in MATLAB Simulink environment. Sinusoidal PWM is used while implementing the DCMLI with carrier frequency 2 kHz and modulating signal 50 Hz with 0.7 modulation index. The waveform for simulation is shown in Fig-5.5. The rating of different components is specified in the appendix. The hardware model is N-channel based with a diode in anti-parallel behaving as feedback diode. Two diodes in each leg are also connected to clamp the neutral. The waveform for both line and phase voltages are shown in Fig-5.6 and Fig-5.7 respectively.

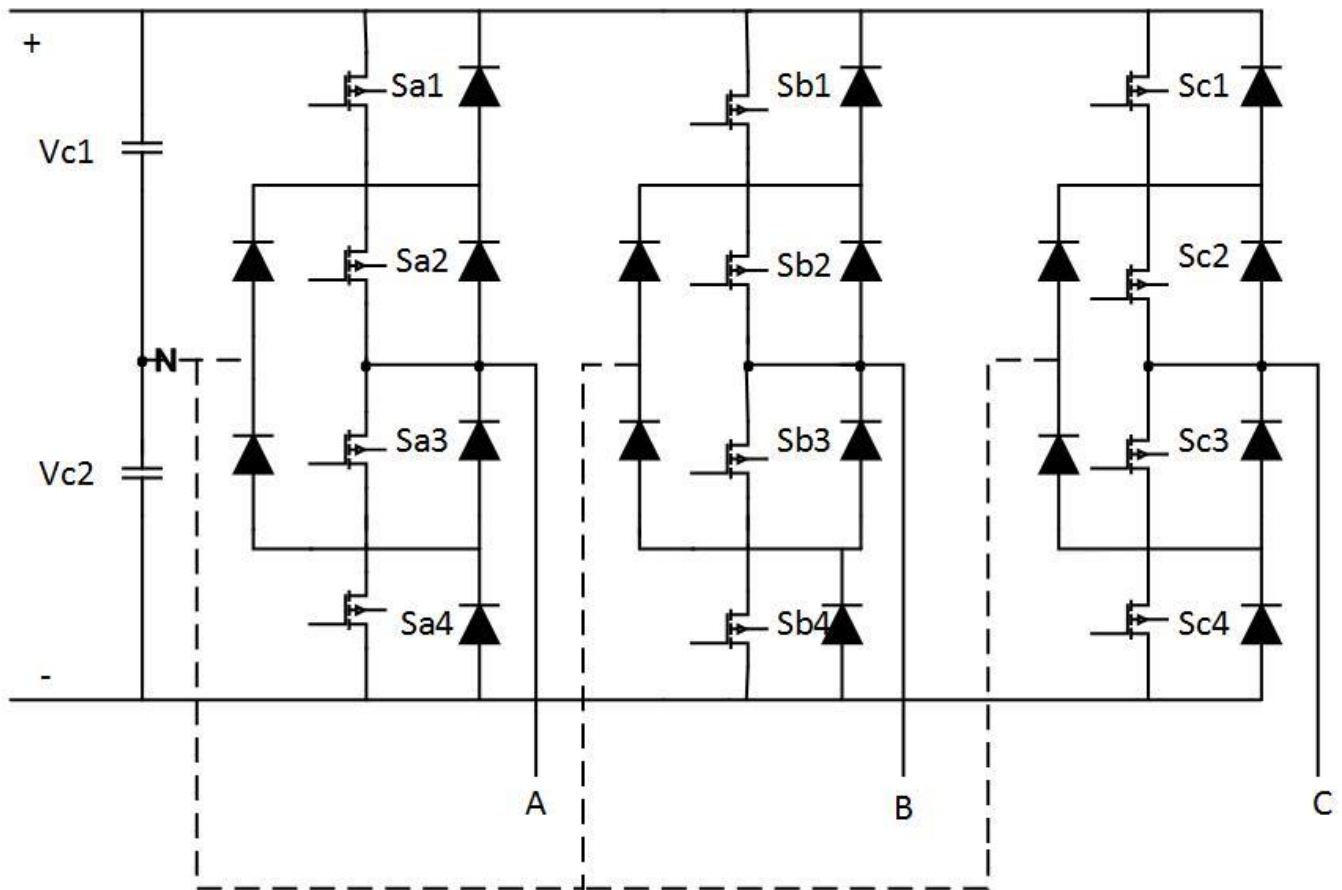


Fig-5.4 Circuit Diagram of Three Level Diode Clamped MOSFET Based Inverter

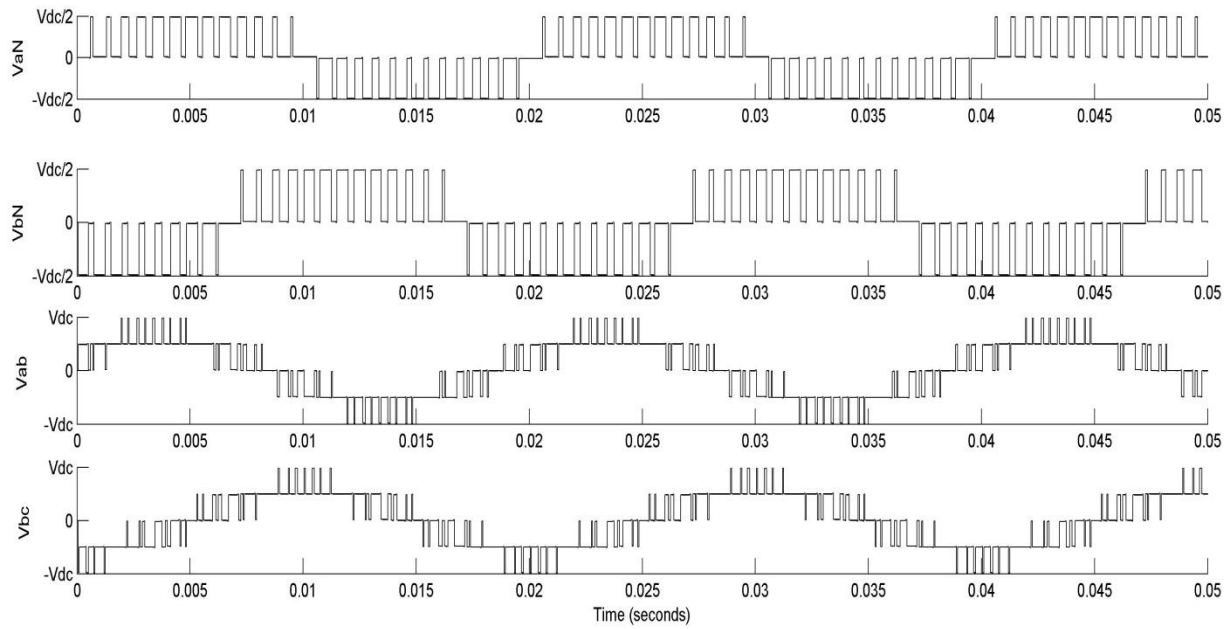


Fig-5.5 Simulation Waveform of Three-level DCMLI

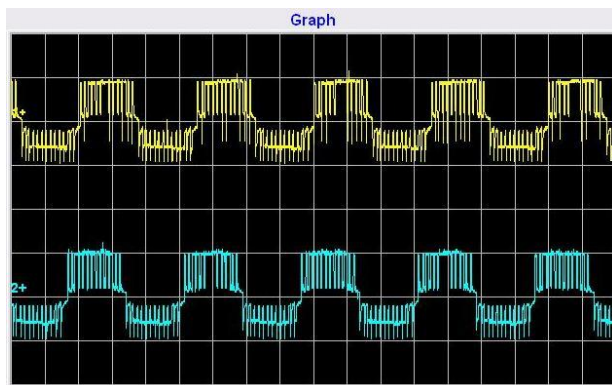


Fig-5.6 Pole Voltage Waveform of a-Phase and b-Phase V_{aN} and V_{bN} .

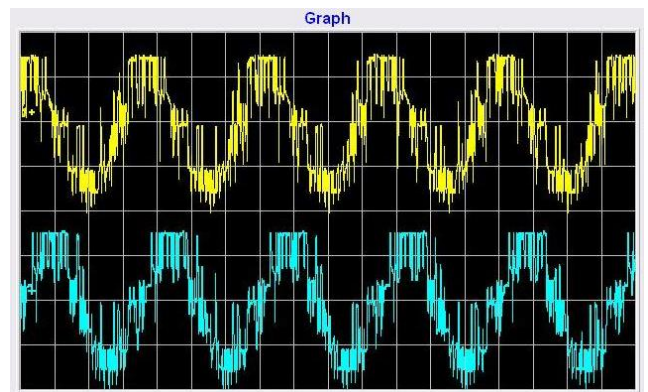


Fig-5.7 Line Voltage Waveform of V_{ab} and V_{bc} .

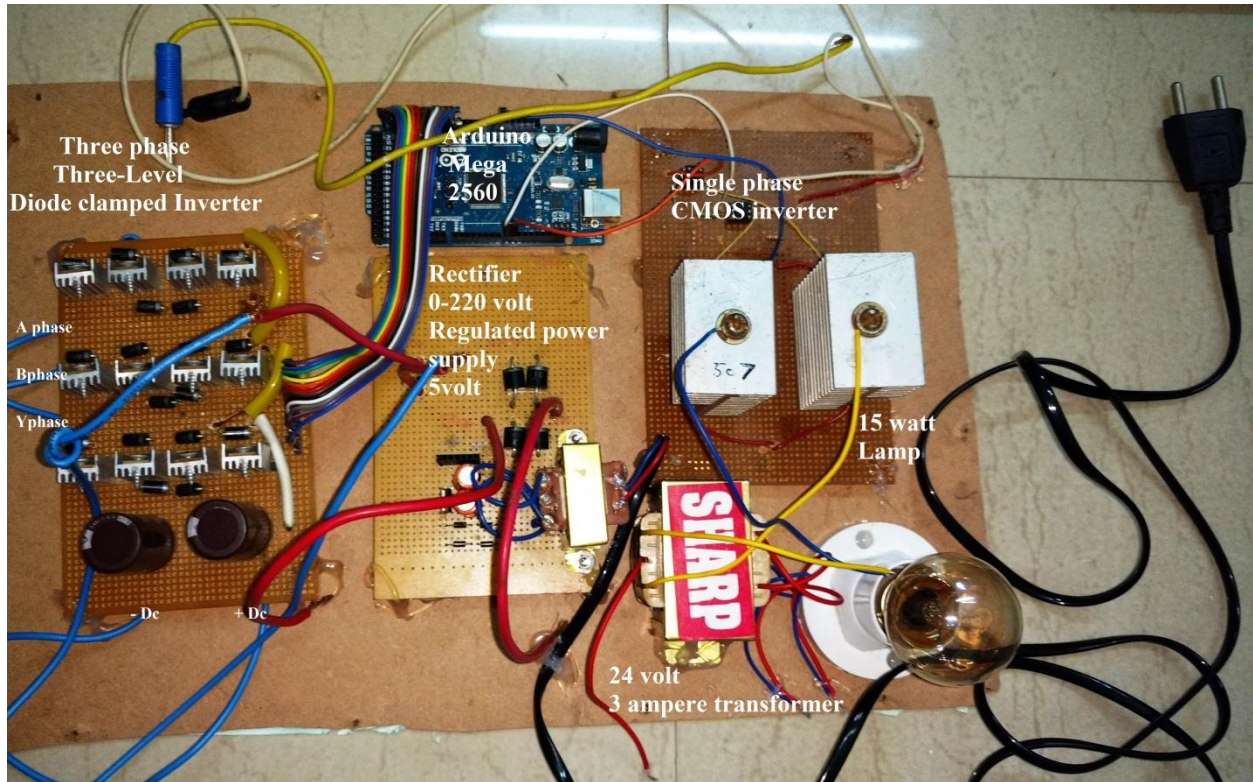


Fig-5.8 Single Phase CMOS Inverter and Three-Phase Three-Level DCMLI

5.4 Challenges

While implementing the Single phase H-bridge CMOS inverter and three phase three-level inverter following difficulties are faced:-

- Adding the add-ons of Arduino to MATLAB/Simulink.
- Implementing on breadboard causing loose connections.
- While implementing SPWM technique to the CMOS inverter the width change was propagating to the entire waveform creating one pulse in each cycle with carrier frequency instead of modulating frequency.
- Using driver IC IRF 2110 leads to a problem in a transient situation so not opted this IC.
- Tried for continuous switching implementation in three-level diode clamped inverter but error due to a large matrix size of pulse generator it was unable to deploy in Arduino mega 2560.

Chapter-6

CONCLUSION and FUTURE SCOPE

6.1 Conclusion

The performance of different three-level voltage source converters based on GTOs is compared for selection of inverter. Challenges and demerits are associated with different topologies of converters and are taken into account for selection. The FFT analysis of different topologies has been performed for THD level. From the observation it can be concluded that Diode-clamped inverter has a much lesser value of THD as compared to the other topologies. Therefore DCMLI output ac voltage waveform is very much closer to conventional synchronous generator output voltage waveform. So the selection of diode-clamped three-level inverter is done.

This topology of three-level inverter along with multi-pulse configuration is used for STATCOM. The STATCOM design is of constant dc-link voltage with capacitor voltage balanced. The advantage of this control scheme is less voltage stress on switches and less switching losses therefore highly efficient model is achieved. The model is capable of compensating both active and reactive current and hence maintains the terminal voltage at a constant value with very good quality waveform below 2.5% THD in all the three loading cases.

Implementation on hardware is a bit difficult but I have implemented H-bridge single phase inverter where the voltage waveform is very much similar to the simulation waveform. The model is tested on resistive load (incandescent lamp).The next is the prototype of diode-clamped three-level inverter where I have matched the waveform pattern of simulation with hardware.

6.2 Future Scope

Some of the recommendations for future research in this area are

1. Using Artificial Intelligence technique such as ANN(Artificial Neural Network)and Fuzzy Logic controller instead of the conventional controllers such as PI and PID controllers as it is a bit difficult to find controller constants for a discrete system such as an inverter.

2. Implement Flying capacitor and read voltage through Arduino and compare it with a reference value in PC (personal computer) and apply PI controller to control capacitor voltage thereafter deploying the simulation to the Arduino Mega 2560.
3. One can also go for cascaded H-bridge inverter using D-space and DSP as a number of switching increases.

Appendix

Table6.1:- Components and their specification used in STATCOM

S.No	Elements	Parameters
1	GTO based VSC	4
2	Zig-Zag Transformer (as series transformers)	4 each of 25MVA.17.5kV(primary),2,21kV(secondary),15%(X)
3	Pulse Number	48
4	Nominal ac source voltage	132kV
5	Nominal dc link voltage	3kV
6	GTO switching frequency	50Hz
7	DC capacitor	125mf
8	DC voltage controller	$Kp_{dc} = 4,$ $KI_{dc} = 250$
9	Decoupled current controller	$Kp_d = 30,$ $Kp_q = 60$
10	AC voltage controller	$Kp_t = 0.12,$ $KI_t = 5$
11	DC Link capacitor voltage balancer	$Kp = 0.001,$ $KI = 0.0001$
12	Short circuit level	132kV,50Hz,3%Zn,1000MVA

Table6.2:- Specification of electronics components used in Hardware design of Single phase full wave inverter

S.No	Component	Quantity	Specification
1	IRF540	2	<p><i>N-channel MOSFET</i></p> <p>$V_{DS} = 100\text{volt}$</p> <p>$R_{DS(on)} = 0.077\Omega$</p> <p>$V_{GS} = 10\text{volt}$</p> <p><i>Continuous $I_D = 28\text{ amp at } 25^\circ\text{C}$</i></p> <p><i>Continuous $I_D = 20\text{ amp at } 100^\circ\text{C}$</i></p>

2	IRF9540	2	<p><i>P-channel MOSFET</i></p> <p>$V_{DS} = -100\text{volt}$</p> <p>$R_{DS(on)} = 02\Omega$</p> <p>$V_{GS} = -10\text{volt}$</p> <p><i>Continous $I_D = -19\text{ amp at } 25^\circ\text{C}$</i></p> <p><i>Continous $I_D = -13\text{ amp at } 100^\circ\text{C}$</i></p>
3	4N35	2	<p><i>Optocoupler</i></p> <p><i>INPUT</i></p> <p><i>Reverse voltage $V_R = 6\text{volt}$</i></p> <p><i>Fotward current $I_F = 50\text{m}$</i></p> <p><i>Power dissipation = 70mA</i></p> <p><i>OUTPUT</i></p> <p>$V_{CEO} = 70\text{ volt}$</p> <p>$V_{EBO} = 7\text{ volt}$</p> <p>$I_C = 50\text{mA}$</p> <p><i>Isolation Test Voltage</i></p> <p>$V_{iso} = 5000\text{volt VRMS}$</p>
4	Resistances color code	4	<p>$R_1 = 10k$</p> <p>$R_2 = 330\Omega$</p>
5	Jumper wires	3	<i>Multi-color Spacing: 2.54mm; length: 20cm</i>
6	Heat sink	2	<i>Two MOSFET mounted</i>
7	Transformer	1	<i>12-0-12 / 230 volt 3 ampere</i>
8	Bulb	1	<i>15watt 230 volt</i>
9	Holder	1	<i>Bulb holder</i>
10	PCB	1	<i>Zero PCB 15 x 30cm</i>
11	Arduino	1	<i>Arduino mega 2560</i>
12	DSO	1	<i>Dual channel</i>
13	Regulated DC supply	1	<i>DC-30volt -2ampere</i>
14	Connecting wire	-	<i>Single strand</i>

Table6.3:- Specification of Electronics Components used in Hardware Design of Three Level Diode Clamped Inverter

S.No	Component	Quantity	Specification
1	Diode	12+6=18	<i>IN5008</i>
2	IRF 540	12	<i>N-channel MOSFET</i> $V_{DS} = 100\text{volt}$ $R_{DS(on)} = 0.077\Omega$ $V_{GS} = 10\text{volt}$ <i>Continuous $I_D = 28\text{ amp at } 25^\circ\text{C}$</i> <i>Continuous $I_D = 20\text{ amp at } 100^\circ\text{C}$</i>
3	Capacitor	2	<i>Electrolytic 200volt 470uF</i>
4	Heat Sink	12	<i>Single MOSFET mounted</i>
5	Comb	15	<i>Male connector</i>
6	Jumper wire	15	<i>Multi-color Spacing: 2.54mm; length: 20cm</i>
7	PCB	1	<i>Zero PCB 15 x 30cm</i>
9	Arduino	1	<i>Arduino mega 2560</i>
10	DSO	1	<i>Dual channel</i>
11	Rectifier	1	<i>230volt- 8 ampere</i>
12	Auto transformer	1	<i>0-230 volt -10 ampere</i>

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