LOW-VOLTAGE CMOS CURRENT MIRRORS

Thesis submitted towards the partial fulfillment of the requirements for the award of the degree of

Master of Technology

In

(VLSI Design & CAD)

Submitted by

Manish Tikyani

Roll. No. 600961010

Under the supervision of

Mr. Rishikesh Pandey

Assistant Professor, ECED

Thapar University, Patiala

Department of Electronics & Communication Engineering

Thapar University, Patiala – 147004,

INDIA

July 2011

CERTIFICATE

I hereby declare that the work, which is being presented in the thesis, entitled "LOW-VOLTAGE CMOS CURRENT MIRRORS" in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Mr. Rishikesh Pandey, Assistant Professor, ECED.

Manish Tikyani

Date: 14/7/2011

This is to certify that the above statement made by the candidate is correct and true to best of my knowledge.

Rishikesh Pandey

Date: 14/07/2011

Rishikesh Pandey
Assistant Professor
ECED, Thapar University
Patiala-147004

Dr A. K. Chatterjee
Head of Department
ECED, Thapar University
Patiala-147004

20.7.11

Dr S. K. Mohapatra
Dean of Academic Affairs
Thapar University
Patiala-147004

ACKNOWLEDGMENTS

First of all, I would like to express my gratitude to *Mr. Rishikesh Pandey*, Assistant Professor, Electronics and Communication Engineering Department, Thapar University, Patiala for his patient guidance and support throughout this thesis work. I am truly very fortunate to have the opportunity to work with him.

I am thankful to the Head of Department, *Professor* (*Dr.*) *A. K. Chatterjee* and PG coordinator, Associate Professor (*Dr.*) *Alpana Agarwal* of Electronics and Communication Engineering Department to support me towards successful completion of this work.

I am also thankful to the entire faculty and staff of Electronics and Communication Engineering Department.

Next, I would like to thank *Mr. B. K. Hemant* (Project faculty) for all the good times at the lab. I specially thank to *Pankaj sir, Anand sir, Anil sir*, *Vivek sir*, *Manjeet*, *Sunil*, *Mohan*, *Ajay*, *Wazir*, and *Sunny* for their help and suggestions which makes everyday a pleasant one. Thanks so much to all of you for the fun and great memories here at Thapar University.

Finally, and above everyone else, I would like to thank *My Family* for standing by me through all the joys and sorrows that life had to offer. My heartfelt thanks and life-long gratitude go to my *dearest mother*, *loving father* and *my brother* for all the love and affection that they have showered upon me.

Manish Tikyani

Roll no: 600961010

ABSTRACT

Current mirror is the main building block of analog circuit designing which is used to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The responsibilities of Current Mirror circuit are current amplification and to provide proper biasing to analog circuits.

In this thesis low-voltage current mirror circuit operating at the supply voltage of +1.3 volt is proposed. The proposed circuit is developed by using four p-type and five n-type transistors. The bandwidth of the proposed circuit has been enhanced using resistive compensation technique. The ac analysis of the proposed circuit has also been presented.

The proposed circuit has been simulated using Cadence Design Environment in UMC 0.18 μm CMOS technology. The layout of the proposed circuit has been designed using Virtuoso editor. The post-layout simulation using Spectre has also been presented.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF SYMBOLS

V_{DD}	Supply Voltage
C_{gs}	Gate to Source Capacitance
C_{gd}	Gate to Drain Capacitance
C_{db}	Drain to Substrate capacitance
g_{mi}	Transconductance of MOSFET
r_{oi}	Output Resistance
g_{oi}	Output Conductance
i_o	Output Current
i_{in}	Input Current
v_o	Output Voltage
v_{in}	Input Voltage
z_o	Output Impedance
z_{in}	Input Impedance
ω_p	Pole Frequency
ω_{in}	Input Pole Frequency
ω_o	Output Pole Frequency
C_{in}	Input Capacitance
W	Width of MOSFET
L	Length of MOSFET
s	Complex Frequency

CHAPTER 1 INTRODUCTION

1.1 INTRODUCTION

Since the introduction of integrated circuits, the current mirror circuit has served as the basic building block in analog circuit design. Current mirror circuit plays a huge role to decide overall circuit characteristics. Integrated circuit industry concentrating on low-voltage operation, low-power consumption, wide bandwidth and minimum area requirements, therefore, there is a growing need for new, low-voltage analog circuit designs.

As its name implies it copy the current. In other words, a two terminal circuit whose output current is independent of the output terminal voltage and depends only on the input current is called current mirror. Figure 1.1 shows the symbols of current mirror circuits in which arrow is used to designate the direction of the current flow on the input side. The ratio 1: K represents the current gain of the mirror circuit [18].

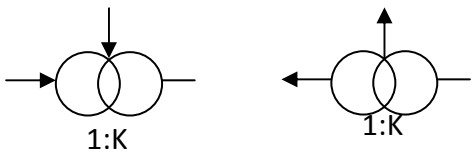

Figure 1.1 Current Mirror symbols (a) NMOS current mirror (b) PMOS current mirror

Current mirror circuits are used to perform current amplification in multiple of reference current, level shifting, biasing and loading [10].

1.2 CURRENT MIRROR CHARACTERISTICS

In this section different characteristics of an ideal current mirror circuit have been discussed.

1.2.1 INPUT-OUTPUT RESISTANCE

Ideal CM has zero input and infinite output resistance, which implies that the input voltage does vary with the input currents and the output currents are independent of applied output voltage. However practical CMs have nonzero input and finite output resistances and they do not truly copy the currents at the output port and a designer should aim to achieve lowest possible input (R_{in}) and highest possible output resistances(R_{out}). Due to these nonidealities, the error in the current transfer ($\Delta i = I_{in} - I_{out}$) equals $I_{in}(r_{in}/r_{out})$

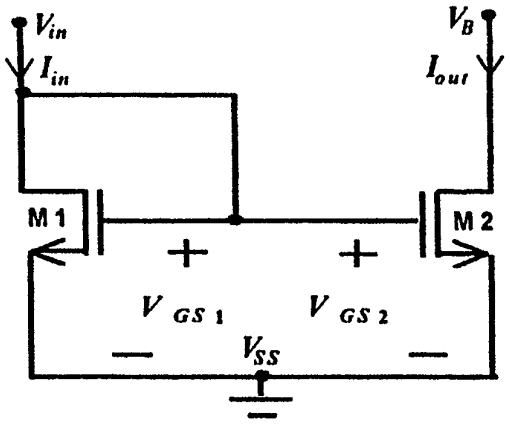

Figure 1.2 Basic Current Mirror [CM] structure [6]

1.2.2 INPUT LINEAR RANGE

For the accurate reproduction of the current at the CM output, the total input current must be in the range where both the devices M_1 and M_2 operate in saturations.

1.2.3 OUTPUT VOLTAGE SWING

An ideal CM produces an accurate output current regardless of the voltage present at the output. In reality a CM require a minimum voltage at the output to ensure that the devices operate in saturation. This voltage is called the output compliance voltage.

1.2.4 DC BALANCE

The drain source voltage of the mirror transistors M_1 and M_2 [6] (Figure 1.2) affects the accuracy of the output current. The error due to mismatch in drain to source voltages equal $\lambda\,(V_{DS2} - V_{DS1})$. This indicates that if the drain source voltages of the mirroring transistors are not balanced then there will be an offset current.

1.2.5 FINITE BANDWIDTH

The current amplification in CMC is typically is less than a factor of 100 and due to the constant gain bandwidth product high frequency operation of the circuit is possible. CMCs provide wide bandwidth operation at low gains. However, the voltage mode circuits with similar closed loop gains produce comparable bandwidths.

1.2.6 DYNAMIC RANGE

The dynamic range of a circuit is the ratio of maximum signal level to the minimum detectable signal level. The maximum input signal is determined by the input determines the minimum detectable signal.

1.2.7 DEVICE MATCHING

Accurate mirroring of the signal current requires perfect matching of the mirroring M_1 and M_2. However imperfections in the CMOS processes lead to random and systematic errors in devices.

In summary, CM the desirable characteristics are:

(a) Current Transfer Ratio (CTR) must be precisely set by the (W/L) ratio and it should be independent of temperature.

(b) Very high output impedance (high R_{out} and low C_{out}). As a result the output current is independent of output voltages.

(c) Low input resistance (R_{in}).

(d) Low input and output compliance voltages.

Several current mirror circuits have been reported in literature. Rajput and Jamuar [3] have suggested level shifted high output impedance current mirror circuit to operate on low power supply voltage. Kaur *et al.* [8] have proposed self cascode current mirror circuit to achieve high output impedance. Sharma et *al.* [7] have presented FGMOS based wide range low-voltage current mirror circuit. Minch [14] has proposed current mirror circuits that function well at all current levels, ranging from weak inversion to strong inversion. These circuits are operated at the supply voltage of +5 volt. Rajput and Jamuar [2,3] have suggested high performance current mirror for low-voltage designs operated at the supply voltages of ±1 volt and +1.5 volt. Baghtash and Azhari [10] have proposed low input impedance current mirror circuits operated at the supply voltage of +1.5 volt.

In this thesis, a novel current mirror circuit is presented which is operated at the supply voltage of + 1.3 volt. Also its bandwidth is enhanced using resistive compensation technique. The proposed circuit is developed by using four p-type and five n-type transistors.. The proposed circuit is operated at the supply voltage of +1.3 volt. The proposed circuit has been simulated using Cadence Design Environment in the UMC 0.18 μm CMOS technology. The simulation results and AC analysis have been presented to demonstrate the feasibility of the proposed current mirror circuit. The bandwidth of this circuit has also been enhanced using resistive compensation technique.

1.3 ORGANIZATION OF THE THESIS

The thesis is organized as follows:

CHAPTER 1: INTRODUCTION. This chapter presents an overview of current mirror circuits, the specifications of the design and its applications.

CHAPTER 2: BASIC CURRENT MIRROR DESCRIPTION. This chapter discusses the mathematical analysis of different current mirror circuits.

CHAPTER 3: LITERATURE REVIEW. This chapter explains the comparative study of the different current mirror circuits available in literature in terms of input and output impedance, DC characteristics, supply voltage requirement and bandwidth response.

CHAPTER 4: HIGH OUTPUT IMPEDANCE LOW-VOLTAGE CURRENT MIRROR. In this chapter, low-voltage current mirror circuit with high output impedance is discussed.

CHAPTER 5: LOW-VOLTAGE CURRENT MIRROR STRUCTURE. This chapter presents a novel current mirror circuit operated at the supply voltage of +1.3 volt. The bandwidth enhancement of the proposed circuit by using resistive compensation technique is also suggested.

CHAPTER 6: SIMULATION RESULTS. In this chapter, the pre-layout and post-layout simulation results of the proposed current mirror circuit have been presented which confirm the theoretical analysis of the proposed circuit.

CHAPTER 7: CONCLUSIONS AND FURTHER DEVLOPMENT. A brief conclusion and possible improvements have been discussed in this chapter.

CHAPTER 2

BASIC DESCRIPTION OF CURRENT MIRROR

2.1 INTRODUCTION

This chapter demonstrates the basic description of the current mirror through mathematical analysis. This chapter is organized as follows: The simple current mirror is discussed in section 2.2. In section 2.3, cascode current mirror is presented.

2.2 SIMPLE CURRENT MIRROR

A simple current mirror circuit is like a resistive divider circuit as shown in the Figure 2.1. The transistor M_1 is biased in saturation region. The output current I_{out} is obtained as

$$I_{OUT} = \frac{1}{2}\mu_n C_{ox} \frac{W}{L} \left[V_{DD} \frac{R_2}{R_1+R_2} - V_{th}\right]^2 \quad (2.1)$$

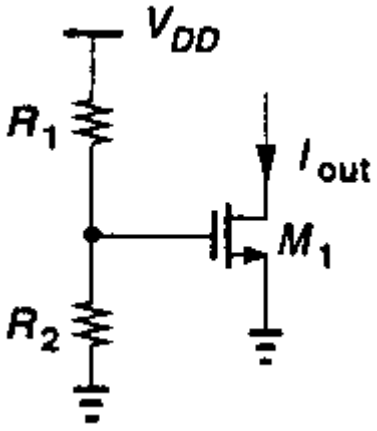

Figure 2.1 current mirror represented by resistive divider [1]

The relation (2.1) reveals various dependencies of output current (I_{OUT}) upon the supply, process, and temperature. The overdrive voltage (V_{DS}) is a function of supply voltage (V_{DD}) and threshold voltage (V_{th}). The threshold voltage may vary by 100mv from wafer to wafer, also mobility (μ_n) and V_{th} exhibit temperature dependence. Thus I_{OUT} is poorly defined. The issue becomes more severe as the device is biased with a smaller overdrive voltage to consume less headroom.

It is important to note that the above process and temperature dependencies exist even if the gate voltage is not a function of the supply voltage means if the gate-source voltage of a MOSFET is precisely defined then its drain current is not. So, must seek other methods of biasing MOS current sources.

The design of current sources in analog circuits is based on "copying" currents from a reference, with the assumption that one precisely defined current source is already available. While this method may appear to entail an endless cycle, it is carried out as illustrated in Figure 2.2.

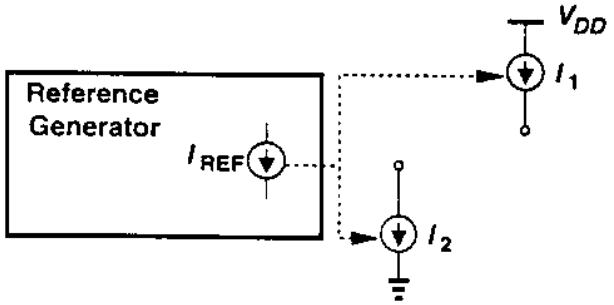

Figure 2.2 Use of reference to generate various currents [1]

A relative complex circuit sometimes requiring external adjustments is used to generate a stable reference current, I_{REF} which is then copied to many current sources in the system as shown in Figure 2.3.

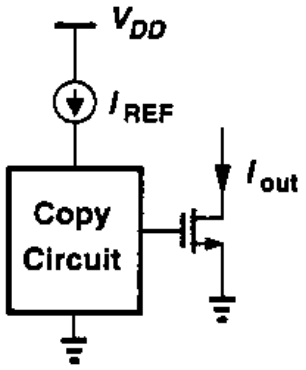

Figure 2.3 Conceptual means of copying currents.[1]

In Figure 2.3, If

$$I_{REF} = f(V_{gs}) \tag{2.2}$$

Where f( ) denotes the functionality of I_D versus V_{gs}.

Equation (2.2) can be written as

$$V_{gs} = f^{-1}(I_{REF}) \tag{2.3}$$

From equation (2.3), it is observed that if a transistor is biased at $I_{REF,}$ then it produces $V_{gs} = f^{-1}(I_{REF})$. Thus if this voltage is applied to the gate and source terminals of a second MOSFET, the resulting current is $I_{out} = f\,f^{-1}(I_{REF}) = I_{REF}$ as shown in Figure 2.4(b). From another point of view, two identical MOS devices that have equal gate-source voltages and operate in saturation carry equal currents (if λ=0).

The structure consisting of M_1 & M_2 in Figure 2.4(b) is called a "Current Mirror". In the general case, the device need not be identical. Neglecting channel-length modulation, the currents relations can be expressed as

$$I_{REF} = \left(\frac{1}{2}\right) \mu_n C_{ox} (W/L)_1 (V_{gs} - Vth)^2 \tag{2.4}$$

$$I_{OUT} = \left(\frac{1}{2}\right) \mu_n C_{ox} (W/L)_2 (V_{gs} - Vth)^2 \tag{2.5}$$

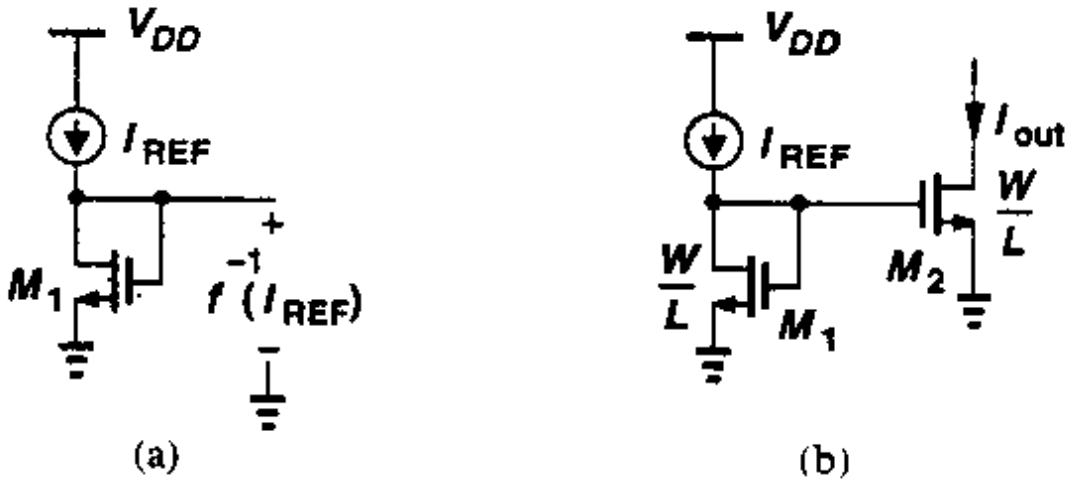

Figure 2.4 (a) Diode connected device providing inverse function (b) Basic current mirror

Dividing eqn. (2.5) by eqn. (2.4), the relation between I_{OUT} and I_{REF} is obtained as

$$I_{OUT} = I_{REF}\left[\frac{(W/L)_2}{(W/L)_1}\right] \quad (2.6)$$

The key property of this topology is that it allows precise copying of the current with no dependence on process and temperature. The ratio of I_{out} and I_{REF} is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy [1].

To calculate I_{out} and I_{REF} relationship of the following circuit (Figure 2.5)

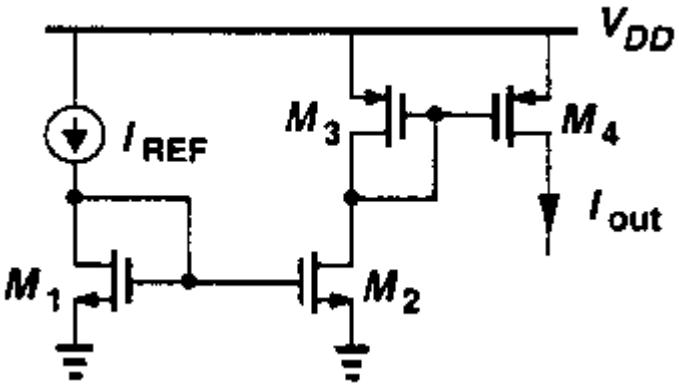

Figure 2.5 Two stage Current Mirror [1]

Different current equations can be expressed as follows

$$I_{D2} = I_{REF}\left[\frac{(W/L)_2}{(W/L)_1}\right] \quad (2.7)$$

$$|I_{D3}| = |I_{D2}| \quad (2.8)$$

$$I_{D4} = I_{D3}\left[\frac{(W/L)_4}{(W/L)_3}\right] \quad (2.9)$$

Thus $$I_{D4} = I_{D3}\,\alpha\,\beta\,I_{REF} \quad (2.10)$$

where $$\alpha = \left[\frac{(W/L)_2}{(W/L)_1}\right] \qquad \beta = \left[\frac{(W/L)_4}{(W/L)_3}\right] \quad (2.11)$$

Proper choice of α and β can establish large or small ratios between I_{D4} and I_{REF}. For example α= β=5 yields a magnification factor of 25. Similarly α=β=0.2 can be utilized to generate a small, well defined current.

2.3 CASCODE CURRENT MIRROR

In the discussion, channel length modulation is neglected. Channel length modulation effect results in significant error in copying currents, especially if minimum length transistors are used so as to minimize the width and hence the output capacitance of the current source. For the simple mirror of Figure 2.4(b), the drain current

$$I_{D1} = \left(\frac{1}{2}\right)\mu_n C_{ox}\,(W/L)_1\,(V_{gs} - V_{th})^2\,(1 + \lambda V_{DS1}) \quad (2.12)$$

$$I_{D2} = \left(\frac{1}{2}\right)\mu_n C_{ox}\,(W/L)_2\,(V_{gs} - V_{th})^2\,(1 + \lambda V_{DS2}) \quad (2.13)$$

and hence

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1}\;\frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} \quad (2.14)$$

While $V_{DS1} = V_{GS1} = V_{DS2}$, V_{DS2} may not equal V_{GS2} because of the circuitry fed by M_2.

In order to suppress the effect of channel length modulation, a cascade current source can be used. In Figure 2.6(a) if V_b is chosen such that $V_Y = V_X$, then I_{out} closely tracks I_{REF}. This is because the cascade devices shield the bottom transistor from variations in V_P.

$$\Delta V_Y \approx \Delta V_P / [(g_{m3} + g_{mb3})\, r_{03}] \quad (2.15)$$

Thus the voltage V_Y remains close to V_X and hence $I_{D1} \approx I_{D2}$ with high accuracy. Such accuracy is obtained at the cost of the voltage headroom consumed by M_3, while L_1 must be equal to L_2. The length of M_3 need not be equal to L_1 and L_2.

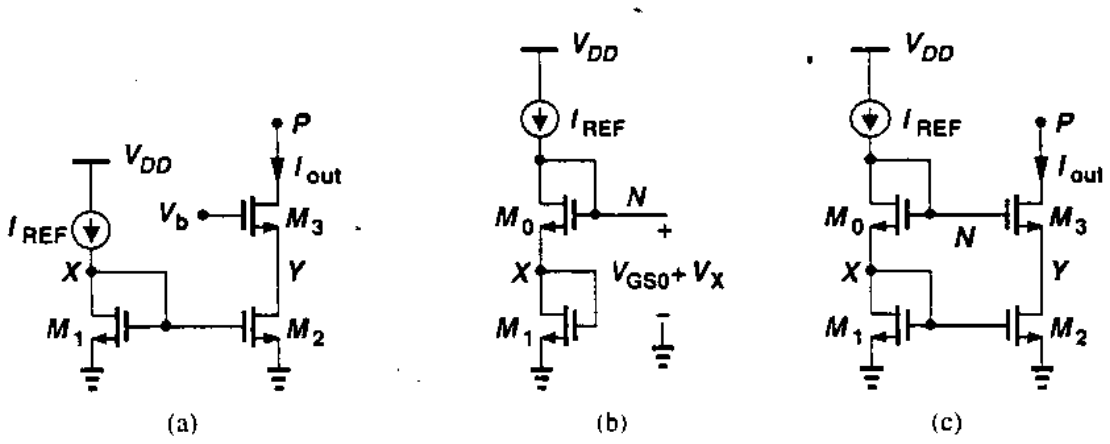

Figure 2.6 Different structures

(a) Cascode current source

(b) Modification of mirror circuit to generate the cascode bias voltage

(c) Cascode current mirror [1]

Since the objective is to ensure $V_Y = V_X$, it must be ensure that $V_b - V_{GS3} = V_X$ or $V_b = V_X + V_{GS3}$. This result suggests that if a gate-source voltage is added to V_X, the required value of V_b can be obtained. As shown in Figure 2.6(b), the idea is to place another diode connected device M_0 in series with M_1, thereby generating a voltage $V_N = V_{GS0} + V_X$. Proper choice of the dimensions of M_0 with respect to those of M_3 yields $V_{GS0} = V_{GS3}$. Connecting node N to the gate of M_3 as shown in Figure 2.6(c), it can be written that $V_{GS0} + V_X = V_{GS3} + V_Y$. Thus if $[(W/L)_3/(W/L)_0] = [(W/L)_2/(W/L)_1]$, then $V_{GS3} = V_{GS0}$ and $V_Y = V_X$. This result holds even if M_0 and M_3 suffer from body effect.

While operating as a current source with high output impedance and accurate value, the topology of Figure 2.6(c) nonetheless consumes substantial voltage headroom. For simplicity, let us neglect the body effect and assume all the transistors are identical. Then the minimum allowable voltage at node P is equal to

$$V_N - V_{TH} = V_{GS0} + V_{GS1} - V_{TH} = (V_{GS0} - V_{TH1}) + (V_{GS1} - V_{TH1}) + V_{TH} \quad (2.16)$$

two overdrive voltages plus one threshold voltage. Thus the cascade mirror of Figure 2.6(c) wastes one threshold voltage in the headroom. This is because $V_{DS2} = V_{GS2}$, whereas V_{DS2} could be as low as $V_{GS2} - V_{TH}$ while maintaining M_2 in saturation.

Figure 2.7 is describing the method to compensate the effect of channel length modulation. In Figure 2.7(a) V_b is chosen to allow the lowest possible value of V_P but the output current does not accurately track I_{REF} because M_1 and M_2 sustain unequal drain-source voltages. In Figure 2.7(b) higher accuracy is achieved but the minimum level at node P is higher by one threshold voltage.

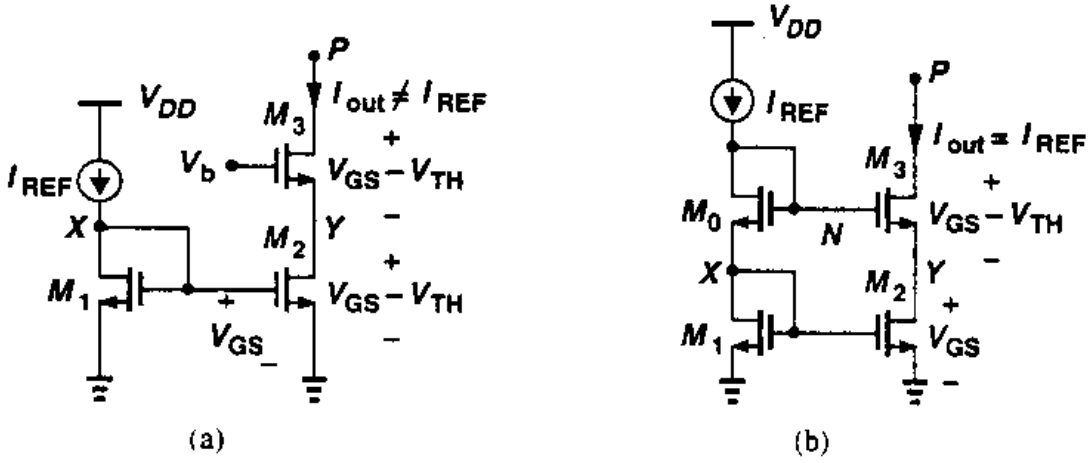

Figure 2.7 (a) Cascode current mirror with minimum headroom voltage

(b) Headroom consumed by cascade mirror [1].

In order to eliminate the accuracy headroom trade off described above, Figure 2.8(a) has the cascade topology with its output shorted to its input. It must be ensure that $V_b - V_{TH2} \leq V_X (= V_{GS1})$ for M_2 to be saturated and $V_{GS1} - V_{TH1} \leq V_A (= V_b - V_{GS2})$ for M_1 to be saturated. Thus

$$V_{GS2} + (V_{GS1} - V_{TH1}) \leq V_b \leq V_{GS1} + V_{TH2} \quad (2.17)$$

A solution exists if $V_{GS2} + (V_{GS1} - V_{TH1}) \leq V_{GS1} + V_{TH2}$, that is if $V_{GS2} - V_{TH2} \leq V_{TH1}$. It must be ensure that the size of transistor M_2 must be such that its overdrive voltage remains less than one threshold voltage.

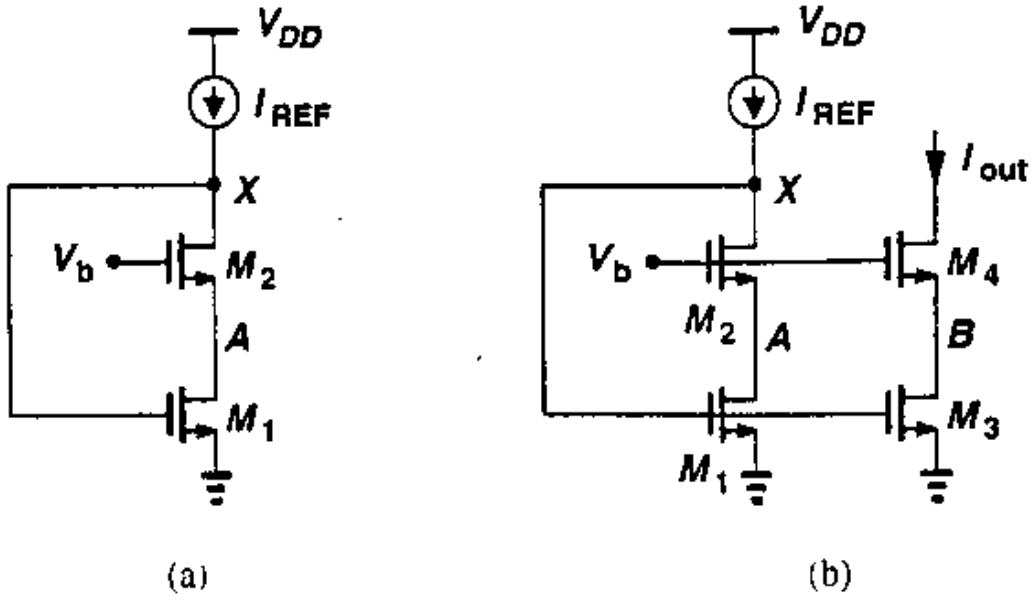

Figure 2.8 Modification of cascode mirror for low voltage operation [1].

In Figure 2.8(b), where all of the transistors are in saturation and proper rationing ensures that $V_{GS2} = V_{GS4}$. If $V_b = V_{GS2} + (V_{GS1} - V_{TH1}) = V_{GS4} + (V_{GS3} - V_{TH3})$, then the cascode current source M_3 and M_4 consumes minimum headroom (the overdrive of M_3 plus that of M_4) while M_1 and M_3 sustain equal drain source voltages, allowing copying of IREF. It is a "Low voltage cascode" current mirror circuit.

CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

In this chapter different topologies and current mirror circuits are discussed to achieve the target of low-voltage power supply, low input impedance and high output impedance. This chapter is organized as follows: different topologies of current mirror circuit are discussed in section 3.2. In section 3.3, simple low-voltage current mirror circuit is presented. Section 3.4, discusses the adaptive biasing low-voltage current mirror circuit. FGMOS based wide range low-voltage current mirror circuit is discussed in section 3.5. In section 3.6, self cascode current mirror circuit is given and very low input impedance, low power current mirror circuit is presented in section 3.7.

3.2 DIFFERENT TOPOLOGIES OF LOW-VOLTAGE CURRENT MIRROR

In this section different topologies of Low-Voltage Current Mirror (LVCM) circuit are discussed.

3.2.1 LEVEL SHIFTING STAGE

A level shifted CM structure is shown in Figure 3.1. The transistor M_3 is used to shift the voltage level at the drain of M_1. V_{in} is a characteristics parameter of a LVCM and decides the range of input voltage swing in such circuits.

The bias current (I_{bias}) decides the operational region of M_3 and the input current (I_{in}) and the externally applied voltage at the drain terminal of M_2 decides operational mode for M_2. Similarly I_{bais1} and I_{in} decide the operation region of M_1. For example, how value of I_{bias1} forces M_3 to operate in subthreshold region, while I_{bias1} ensures M_3 to operate in saturation region. When I_{in} is high enough and drain voltage V_{DS2} is low, M_2 operates in saturation region. For low input currents and high I_{bias1}, the gate voltage for M_1 is high (input current is also high)

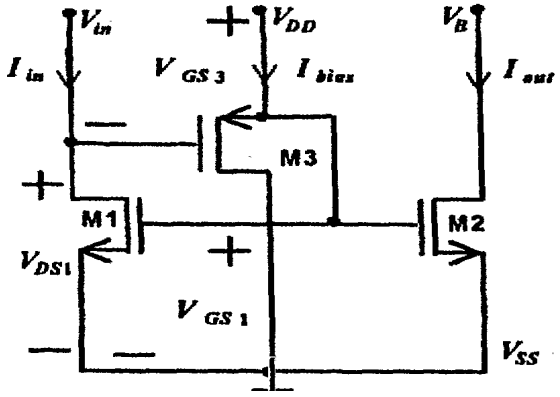

Figure 3.1 Level Shifted Current Mirror [3,7].

Thus V_{in} can be calculated by applying KVL

$$V_{in} = V_{gs1} - V_{gs3} \tag{3.1}$$

By applying KVL in other loop,

$$V_{DD} - V_{GS1} = 0 \qquad V_{GS1} = V_{DD} \tag{3.2}$$

Since $V_{TP} > V_{TN}$, there is a difficulty to keep the condition $V_{GS1} - V_{GS3} > 0$ valid in a level shifter based circuits over a wide range of I_{in} [3,7]. One of the solutions is to use a p-n-p transistor for level shifting and now $V_{in} = V_{GS1} - V_{BE}$. Generally V_{BE} approximates as 0.7V and V_{GS1} is always more than 0.8V (If is assumed that V_T=0.8V). As the device sizes are reducing and V_T is also reducing and there will be a situation where $V_{GS1} - V_{BE} > 0$ will not be valid and hence it would not be able to use a p-n-p transistor. Thus there is need to have an alternate choice of PMOS transistor as shown above in Figure 3.1.

3.2.2 CASCODE CM STAGE

Cascode term is the combination of Common source (CS) and Common Gate (CG) as shown in Figure 3.2. MOSFET M_2 is in CS mode while M_3 is in CG mode.

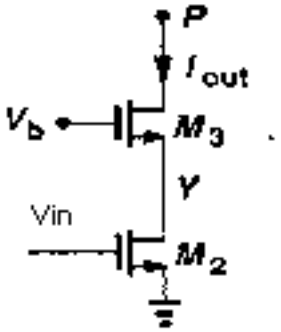

Figure 3.2 Cascode stage [1,8]

Voltage V_b is used to provide biasing for M_3 while input voltage is gives to M_2. This cascode input signals may be come from the last stage. Main motive of cascode structure is to provide high gain with high output impedance for LV application.

3.2.3 SELF CASCODE CM STAGE

As the MOSFET size is shrinking the output impedance of the MOSFET is also reducing due to the channel length modulation. To get high gain, it needs high output impedance of the devices and short channel MOSFET cannot do it, to get it cascading is the obvious technique. Cascading MOSFET increases the gain but it decreases the output signal swing as well. So cascode structure cannot use in LV systems. If the circuit used is modified in such a way that the biasing of the transistor M_2 does not affect the output voltage swing, the output impedance of the structure can be increased to have high gain structure at LV levels. One of the technique is to use the self cascode (SC) structure which does not require high compliance voltage at output nodes and provide high output impedance to give high output gain. This approach has potential applications in low voltage design [5,8]. A self cascode is a 2-transistor structure [11] (Figure 3.3(a)), which can easily be treated as a single composed transistor (Figure 3.3(b)). The composite structure has much larger effective channel length and the effective output conductance is much low.

The lower transistor M_1 is equivalent to a resistor, where value is input dependent.

The composite structure has both the gates of M_1 & M_2 driven by the input signal and shares a single bias source. In this case composite cascode works like a common-source stage, but with higher voltage gain. In self cascode for optimal operation, the W/L ratio of M_2 is larger than that of M_1, i.e. m>>1. The effective g_m for the composite transistor is approximated as

$$g_{m(effective)} = \frac{g_{m2}}{m} = g_{m1} \tag{3.3}$$

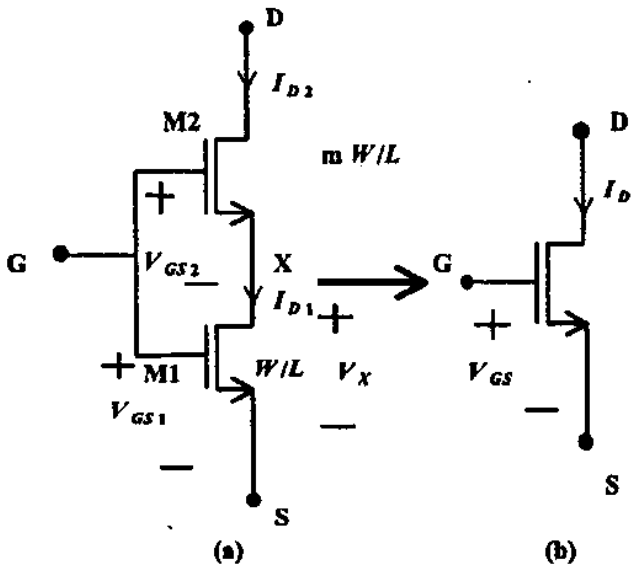

Figure 3.3 (a) Self Cascode structure (b) Composite structure [5,8]

For composite transistor to be in saturation region M_2 have to be in saturation region and M_1 in linear region [11,13]. For these transistors, the current I_{D1} and I_{D2} are given as

$$I_{D1} = \beta_1 \left(Vin - V_{TN} - \left(\frac{V_X}{2}\right)\right) V_X \qquad \text{(Linear region)} \tag{3.4}$$

$$I_{D2} = \beta_2 (Vin - V_{TN} - V_X)^2 \qquad \text{(Saturation region)} \tag{3.5}$$

By solving the above expressions

$$I_{D2} = \left[\frac{\beta_1 \beta_2}{2(\beta_1 + \beta_2)}\right](Vin - V_{TN})^2 \quad (3.6)$$

$$\beta_{effective} = \frac{\beta_1 \beta_2}{(\beta_1 + \beta_2)} \quad (3.7)$$

For $\beta_2 = m\beta_1$

$$\beta_{effective} = \left[\frac{m}{(m+1)}\right]\beta_1 = \left[\frac{1}{(m+1)}\right]\beta_2 \quad (3.8)$$

And for m>>1

$$\beta_{effective} \approx \beta_1 \quad (3.9)$$

Thus in a self cascode structure M_1 operates in linear region, while M_2 operates in saturation region. Hence, voltage between source and drain of M_1 is small. There is no appreciable difference between V_{Dsat} of composite and simple transistor and a self cascode can be used in LV operation [8].

For a self cascode

$$V_{Dsat} = V_{Dsat} - M_2 + V_{DS} - M_1 \quad (3.10)$$

$$V_{Dsat} = V_{Dsat} - M_1 + I_{D2}R_{M1} \quad (3.11)$$

where $$R_{M1} = \frac{1}{\mu_n C_{OX}(V_{in} - V_{TN})\left(\frac{W}{L}\right)} \quad (3.12)$$

The operating voltage of regular cascode is much higher than that of SC and hence a SC structure is suitable for LV design. The advantage offered by SC structure is that it offers high input impedance similar to a regular cascode structure while output voltage requirement are similar to that of single transistor [12].

3.2.4 MULTI INPUT FLOATING GATE MOSFET CM STAGE

The usage of low voltage circuits in portable and mobile equipment is well established now. In non-mobile equipment, the applications of low voltage low power circuits are increasing because it reduces the equipment weight and power consumption. The current mirrors (CMs) are used as basic element for the design of low voltage circuit structures and many low voltage current mirror structures have been developed. Most of these structures have low compliance voltage at output node but many of them have high compliance voltage at the input node. There are few circuits, which have low input and output compliance voltages. However they have high offset current, thus limiting the operating range. To increase their operating range, adaptation of multiple inputs floating gate (MIFG) technology (a promising technique in low voltage design), needs to be examined.

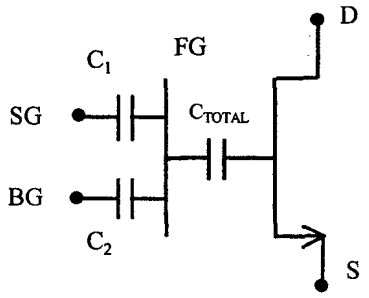

Figure 3.4 MIFG Transistor structure [4]

In a multiple inputs floating gate transistor the gate is floating. The first polysilicon layer forms the floating gate (FG) over the n-channel while the second polysilicon layer forms the multiple input gates (MIG). The FG is capacitively coupled to the MIG.

A two-input MIFG MOSFET is shown in Figure 3.4 where a dc voltage is applied at one of the gates called bias gate (BG) while the signal is applied at second gate termed as signal gate (SG). For a two-input FGMOS with $V_s = V_B = 0$ and C_1, $C_2 >> C_D$, the expression for floating gate voltage, V_{FG} is

$$V_{FG} \approx K_1 V_1 + K_2 V_2 \tag{3.13}$$

$$K_1 = \frac{C_1}{C_{total}} \qquad K_2 = \frac{C_2}{C_{total}} \tag{3.14}$$

$$C_{total} = C_1 + C_2 + C_s + C_D + C_B \tag{3.15}$$

Similarly, C_1 and C_2 represent the capacitances between FG and SGs respectively. C_{total} is the sum of all the capacitances between SGs and FG, capacitance between FG to drain, capacitance between FG to source and capacitance between FG to bulk. Now the drain current (I_D) in saturation region is given by

$$I_D = \frac{\beta}{2}\ (V_{FG} - V_T)^2 = \frac{\beta}{2}\ [(K_1V_1 + K_2V_2) - V_T]^2 \tag{3.16}$$

where β and V_T are the transconductance parameter and threshold voltage, respectively. It may be written as

$$I_D = \beta K_1^2\ [V_1 - V_T(\text{eff})]^2 \tag{3.17}$$

$$V_T(\text{eff}) = \frac{(V_T - V_2K_2)}{K_1} \tag{3.18}$$

As the value of $V_T(\text{eff})$ depends on K_1, K_2 and V_2, it is possible to program the value of the effective threshold voltage of the MOSFET as per the requirement [4, 7].

3.3 LOW-VOLTAGE SIMPLE CURRENT MIRROR STRUCTURE

In a conventional CM figure M_1 is used in diode connected configuration and V_{in} is required to pump I_{in} into the input port. Here V_{in} depends solely on the biasing conditions of M_I, which operates in saturation mode. Its trans-conductance (g_{m1}) decides the input impedance (R_{in}). For this structure (V_{in}) is given by

$$V_{in} \approx V_{tn} + \sqrt{\left[\frac{(2\ I_{in})}{\beta_1}\right]} \tag{3.19}$$

Lower limit of V_{in} is restricted to V_{tn}.

The LVCM (Figure 3.5) uses M_1 and M_2 as a conventional CM**.** The level shifter M_4 is operated in sub threshold region by selecting low bias current I_{bias1}. Second level shifter M_5 provides suitable bias to M_3**,** which is used to enhance the output impedance (R_{OUT}). I_{in} flowing through M_1 is transferred to M_2. V_{in} is given by

$$V_{in} = \sqrt{\left[\frac{(2\ I_{in})}{\beta_1}\right]} + \Delta Vth - |V_X| \qquad (3.20)$$

where $$V_X = \eta V_T \ln[\frac{(L_4\ I_{bias1})}{(W_4\ I_{Do4})}] \qquad 3.21)$$

The minimum output voltage of the LVCM is

$$V_{OUT} = V_{DS2(sat)} + V_{DS3(sat)} \qquad (3.22)$$

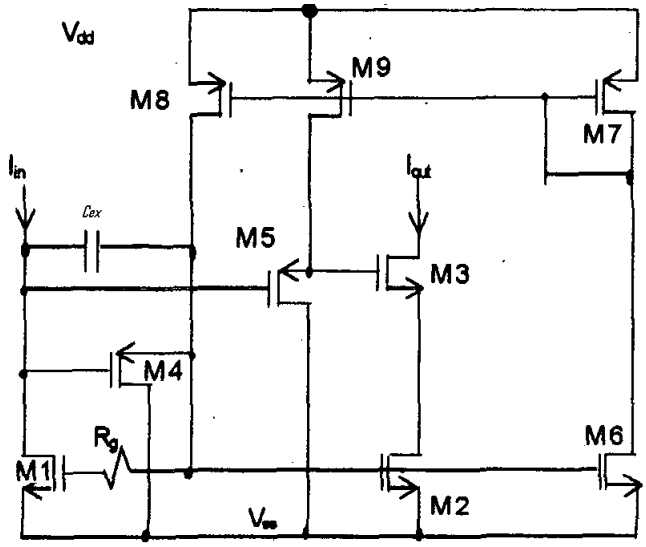

Figure 3.5 Low Voltage Current Mirror [2]

I_{offset} is the most critical factor in LVCMs and sets the lower limit for I_{in} . Due M4, the gates of M_1 and M_2 are not at reference potential even when I_{in} is zero. The gate of M2 is at elevated voltage and its drain voltage depends on externally applied voltage (the drain

voltage of M_1 is decided by I_{in}). Hence a sub threshold current will flow in M_2 when I_{in} equals zero. This current is known as offset current, and is given by

$$I_{offset} = \frac{W_2}{L_2}\frac{L_4}{W_4}\frac{I_{D02}}{I_{D04}} I_{bias1} \exp(\Delta V_t/\eta V_T) \quad (3.23)$$

It indicates that I_{offset} can be tailored according to the designers need through the appropriate selection of W and L. Threshold voltage mismatch $\Delta V_{th} \approx (V_{tp} - V_{tn})$ depends on particular CMOS technology [2]. Even if the threshold voltages of PMOS and NMOS are matched I_{offset} cannot be reduced to zero. The lower limit of $I_{offsett}$ is

$$I_{offset} = \frac{W_2}{L_2}\frac{L_4}{W_4}\frac{I_{D02}}{I_{D04}} I_{bias1} \quad (3.24)$$

Appropriate values for W/L of M_2 and M_4 and Low I_{bias1} ensure lower I_{offset}.

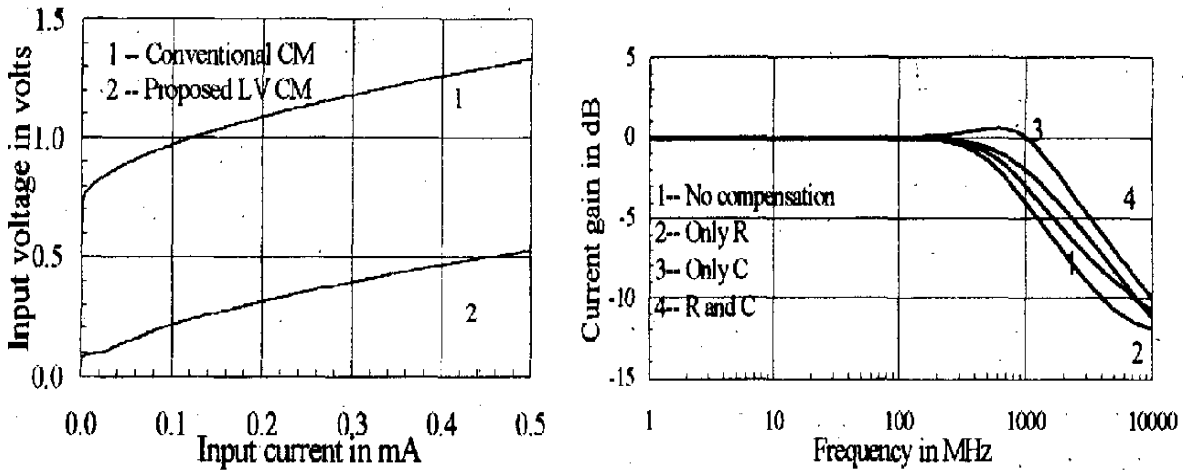

Figure 3.6 (a) Input voltage characteristics

(b) Effect of compensation on Bandwidth [2]

3.4 ADAPTIVE BIASING LOW-VOLTAGE CURRENT MIRROR

In this section adaptive biasing low-voltage current mirror circuit structure and result is discussed.

3.4.1 SIMPLE LVCM STRUCTURE

The conventional CM structures do not have high output resistance. The LVCM structure shown in Figure 3.7 is based on the triode transconductor structure, and is expected to increase the output resistance. The input current I_{in} is pumped into the drain of M_1. The bias current of M_4 is kept small so that M_4 operates in the subthreshold region and M_1 is in the saturation region. The transconductance (g_{m1}) and channel conductance (g_{d1}) of M_1 decide the input impedance (R_{in})**.** Here, M_4 provides the requisite gate bias for M_1 and M_2 while M_5 provides suitable bias for M_3. V_{in} is given by

$$V_{in} = \sqrt{\left[\frac{(2\ I_{in})}{\beta_1}\right]} + \Delta Vth - |\eta V_T \ln\left(\frac{L_4}{W_4}\ \frac{I_{bias1}}{I_{D04}}\right)| \qquad (3.25)$$

where $\Delta V_{th} \approx (V_{tp} - V_{tn})$ is the mismatch between the threshold voltages of M_1 and M_4 and β_1 represents the transconductance parameter for M_1

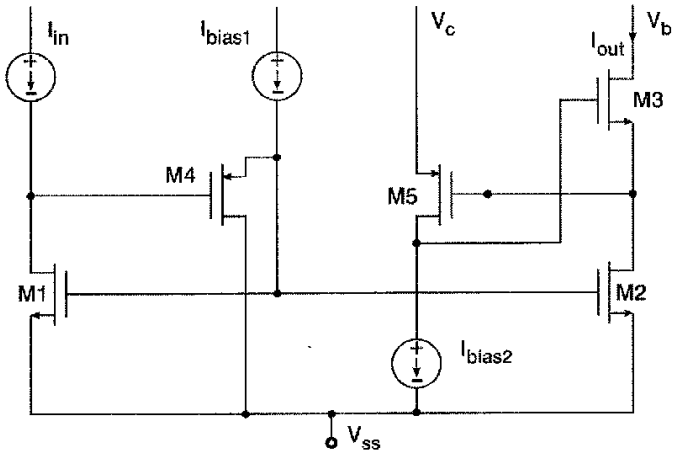

Figure 3.7 High output impedance LVCM [3]

V_{gs1} and V_{gs2} are equal, but V_{ds2} depends on the applied bias voltage (V_b), output current (I_{out}) and the bias current of M_5 (I_{bias2}). The current I_{bias2} is biased to be 10uA, which ensures that M_5 operates in the linear region for entire range of V_b because the drain gate voltage of M_5 equals V_{gs3}. For a current flow through M_3 and M_2, lower V_b implies lower V_{ds2}. This causes higher V_{gs5} than that required for I_{bias2} to flow. V_{ds5} depends on the gate bias of M_3 and is at least equal to $V_{ds2} + V_{tn}$. These conditions ensure that M_5 operates in the linear region. Also V_{ds2} increases as V_b is increased and M_3 has to pump I_{out} but drain source voltage of M_3 is small and inadequate for the purpose. Hence, it requires higher gate source bias, which equals the difference of applied voltage at source of M_5 (V_C) and the drain voltage of $M_2 = (V_C - V_{ds5})$. V_C is normally taken as V_{DD} itself. Now V_{DD} divides between V_{ds2} and V_{ds3} as:

$$\frac{V_{ds2}}{V_{ds3}} = \frac{\beta_3 (V_c - V_{ds2} - V_{tn})}{\beta_2 (V_{ds1} + V_{gs4} - V_{tp})} \tag{3.26}$$

When V_b is small, the above ratio is high and V_{ds2} equals V_b. With the increase in V_b, V_{ds2} rises as M_5 enters into the saturation from the linear region. When V_{ds2} increases further, V_{gs3} decreases to a minimum value where further decrease in V_{gs3} will not allow I_{out} to flow. Now the increase in V_{ds2} stops and remains fairly independent and V_{ds3} starts rising. M_3 enters into saturation, resulting M_5 to be always in the linear region [3].

The input impedance (R_{in}) and the output impedance (R_{out}) are given by

$$R_{in} \approx \frac{1}{g_{m1}} \qquad R_{out} \approx \frac{g_{m3}}{(g_{d2}\ g_{d3})} \tag{3.27}$$

where g_{d2} and g_{d3} represent the output conductance of M_2 and M_3, while g_{m1} and g_{m3} represent transconductance for M_1 and M_3, respectively. Similarly, the minimum output voltage necessary for CM operation is equal to:

$$V_{out(min)} = V_{ds2(min)} + V_{ds3(min)} \tag{3.28}$$

3.4.2 ADAPTIVE BIASING TECHNIQUE

For the LVCM of Figure 3.7, a minimum I_{bias1} is required and V_{in} is dependent of both I_{in} and I_{bias1}. If I_{in} is increased, then V_{in} also increases. But this increase can be reduced to a smaller value by increasing Ibias1. It is possible to increase I_{bias1} proportional to I_{in} by using the CMs obtained using M_6, M_7 and M_8 (Figure 3.8). The current through M_8 is proportional to I_{in} and is I_{bias}. The gate source voltage for M_2 (V_{gs2}) is given by

$$V_{gs2} = V_{ds1} + |\Delta V_{tp4}| - |\eta V_T \ln\left(\frac{L_4}{W_4}\ \frac{I_{bias1}}{I_{D04}}\right)| \qquad (3.29)$$

where ΔV_{tp4} is the threshold voltage of M_4.

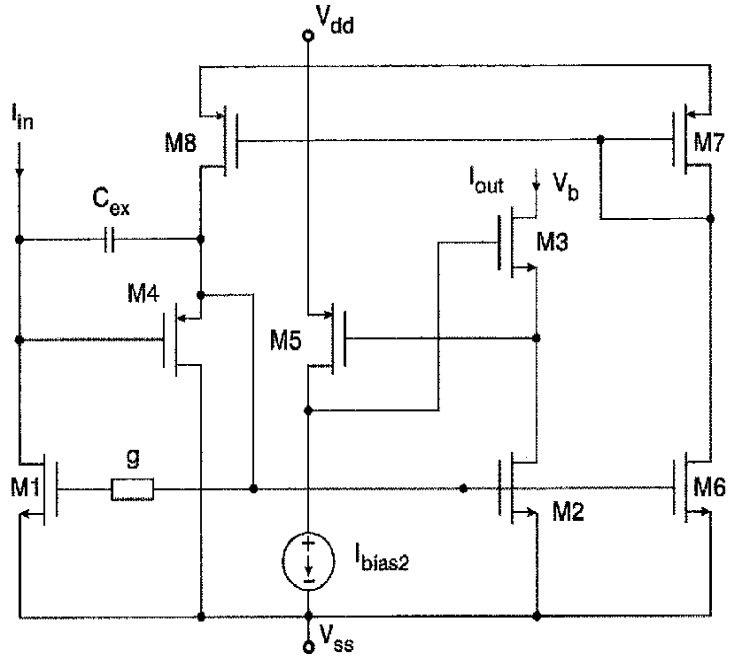

Figure 3.8 ABLVCM structure [3]

It is find that V_{gs2} depends on V_{ds1} and I_{bias1}. For low input current ($I_{in} \leq 10\mu A$), V_{ds2} is nearly equal to zero volts and I_{bias1} solely decides V_{gs2}. I_{bias1} drives V_{gs2} to be near V_{in} even Tor zero I_{in}**.** V_{in} will also be zero, but V_{ds2} increases independently with V_b. Under this condition, a current flows through M_2 (even though I_{in} is zero), because decides the gate bias for M_2 and V_{ds2}, increases independently with Vb.

This condition drives M_2 into the subthreshold region and a small current, known as the offset current (I_{offset}) flows through M_2. As I_{bias1} increases, the gate source bias of M_2 increases, although V_{in} is still negligible (= 0.0V for $I_{in} < 1\mu A$). This causes I_{offset} to increase. Thus, I_{offset} restricts the increase in I_{bias1}.

Thus two contradictory requirements emerge (i.e. that I_{bias1} should be increased to keep V_{in} low and at the same time Ibias1 should be decreased to keep I_{offset} low). In the design of an adaptively biased LVCM (ABLVCM), I_{bias1} is kept low, when I_{in} is low and is increased for higher I_{in}. Higher I_{bias1} imparts low V_{in}, at higher I_{in} and lower I_{bias} is necessary at low I_{in} to have low I_{offset}. Table 3.1 gives the values of offset current under different operating conditions [3].

It is found that I_{offset} can also be minimized by matching the threshold voltages of the PMOS and NMOS transistors, but cannot be made zero. As shown in Table 3.1, operation of the PMOS transistor in the sub-threshold region reduces I_{offset} by a factor of 3. This concept has been used in the ABLVCM structure.

Table 3.1 I_{offset} under different operating condition

Parameter	Operating conditions	
	M1, M2, and M4 (in sub-threshold)	M1 and M2 (in sub-threshold) and M4 (in saturation)
I_{offset}	$\frac{W_2}{L_2}\frac{L_4}{W_4}\frac{I_{DO2}}{I_{DO4}} I_{bias1} \exp\left(\frac{\Delta V_{th}}{\eta V_T}\right)$	$\frac{\beta_2}{2}\left\{\sqrt{\frac{2I_{bias1}}{\beta_4}} + \Delta V_{th}\right\}^2$
I_{offset} (Minimum)	$\frac{W_2}{L_2}\frac{L_4}{W_4} I_{bias1}$	$\frac{K_2}{K_4}\frac{W_2}{L_2}\frac{L_4}{W_4} I_{bias1}$

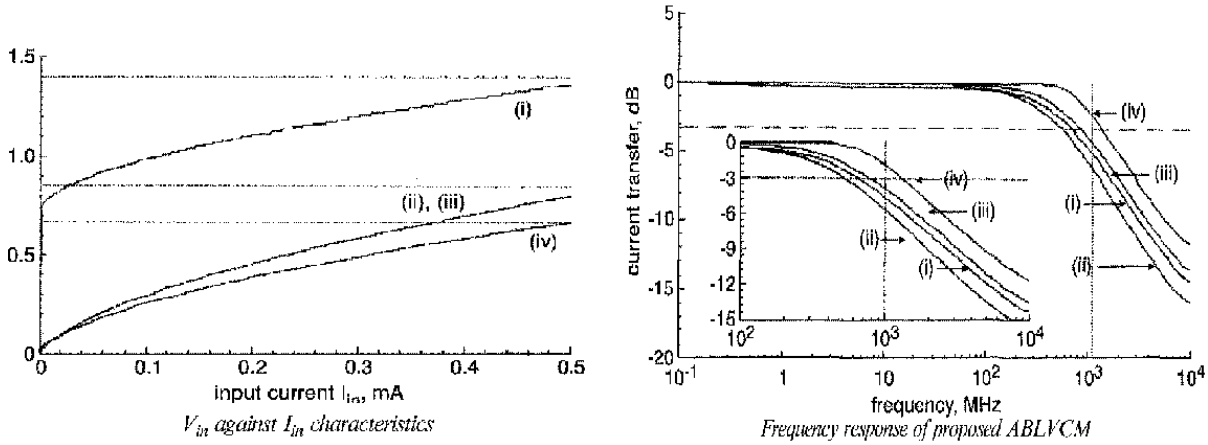

Figure 3.9 (a) (I) Conventional CM (II) simple CM (III) LVCM (IV) ABLVCM
Figure 3.9(b) (I) without compensation (II) with resistive compensation (III) with capacitive compensation (IV) with resistive capacitive compensation [3]

The I_{in} against V_{in}, characteristics for ABLVCM, it looks that V_{in} is 0.65V for I_{in} of 500µA, whereas it was 0.8V and 1.36V for the LVCM and the conventional CM, respectively. The frequency response of ABLVCM is similar to that of the LVCM and the bandwidth is dependent on the type of compensation used.

3.5 FGMOS BASED WIDE RANGE LOW-VOLTAGE CURRENT MIRROR

A conventional CM structure is shown in Figure 3.10 (a), which requires input voltage (V_{in}) of at least one V_{th}. This CM has high compliance voltage at input end and is unsuitable for low voltage applications. The equivalent of this circuit in MIFG technology is shown in Figure 3.10 (b).

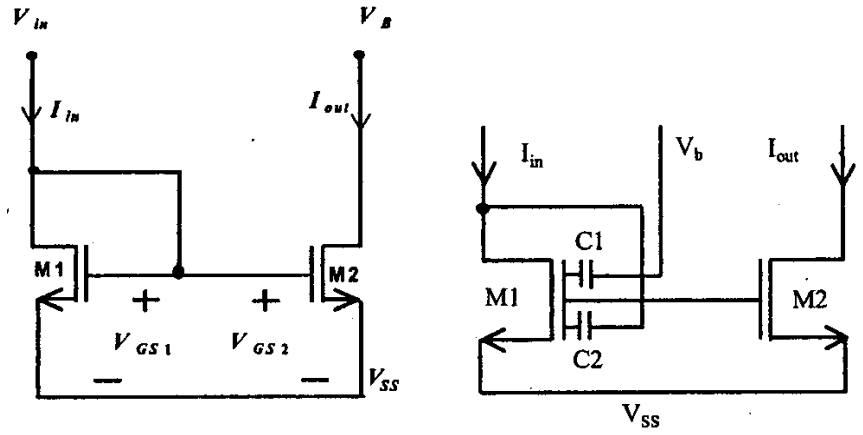

Figure 3.10 (a) Conventional CM (b) CM based on MIFG MOSFETs [4,7]

In this circuit, one of the gate input terminals has been used to program the threshold voltage of the MOSFET. It is found that the use of dc bias voltage (V_b) has decreased the threshold voltage but the V-I characteristic is similar to conventional CM. This circuit has low compliance voltage at low currents but is not suitable for high input currents.

However in this circuit the threshold voltage can be made programmable if the input voltage V_b can be made to change proportional to I_{in}. This is achieved by feeding back I_{in} to produce a voltage proportional to the $I_{in.}$ This voltage is obtained by passing it through a resistance. The voltage drop across the resistance will be high at high I_{in} while it will be low at low $I_{in.}$ A circuit, which implements this behavior, is shown in Figure 3.11(a), where I_{in} is fed back through current mirror formed by M_4 and M_5.

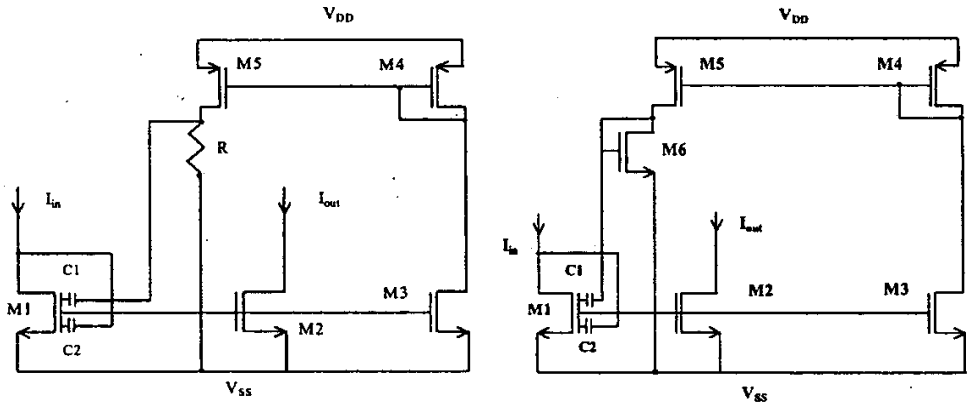

Figure 3.11 (a) CM using MIFG with resistor (b) CM using MIFG MOSFET [4]

To represent complete CMOS implementation, a MOSFET M_6 as shown in Figure 3.11 (b) has replaced the resistance. The use of M_6 reduces the threshold sufficiently at high I_{in}. However, at low I_{in} almost negligible current flows through M_6, which provide very low bias voltage (V_b)**.** In this mode, the input voltage is almost similar to a simple CM. To decrease this voltage further, a constant current flow has to be maintained through the MOSFET M_6. The output impedance of this structure is low. Using MOSFET M_7 as shown in Figure 3.12 increases the output impedance. To bias M_7, transistors M_8 and M_9 are used.

The Figure 3.12 obtains a further improvement over the structure shown in Figure. 3.11(b). In that sense, MOSFETS M_7 and M_8 are added and the output is taken from the drain of M_7. This structure is similar to the one given in. The use of M_7 and M_8 has given added advantage of low output compliance voltage high output impedance. M_5. This circuit uses feedback currents at two places. One for programming the threshold voltage, which is higher at higher input currents thereby reducing the input compliance voltage at high input currents. Secondly the current is fed back to bias the transistor M_8, which increases the output impedance of the resultant current mirror [4].

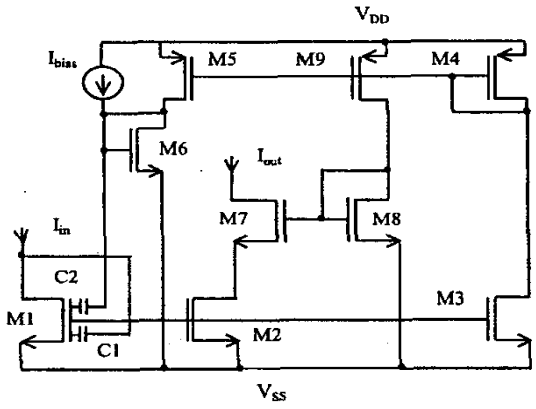

Figure 3.12 Final structure for MIFG mirror [4]

The CM circuits have been simulating for 0.5µm technology with supply voltages of ±0.75V. W/L ratios for various MOSFETs are chosen as 200µm/1µm for M_1 and M_2, 50µm/1µm for M_3, 100µm/0.5µm for M_4 and M_5, 35µm/1µm for M6, 200µm/0.5µm for M_7, 1.5µm/1µm for M_8 and 50µm/0.5µm for M_9. The input port characteristics of the various CMs are shown in Figure 3.13(a). By observation of this plot it is found that the LVCM in Figure 3.12 has the best performance and the power consumption is 1.26 mW.

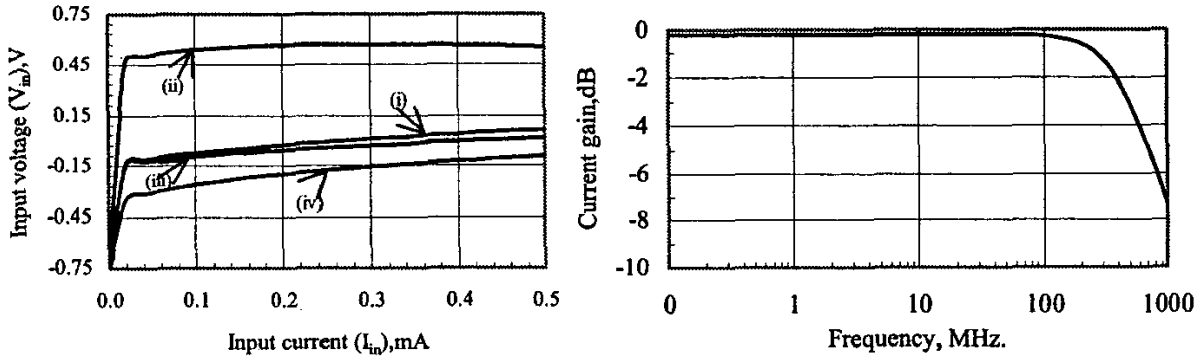

Figure 3.13 (a) comparative V_{in}-I_{in} curves for various CMs (i) Conventional CM (ii) CM with resistor (iii) CM with MOSFET (iv) LVCM. Figure 3.13 (b) Frequency response of the propose CM [4]

The offset current is found to be 58nA and current transfer ratio is almost equal to unity with error less than ±0.1%. The frequency response of CM is shown in Figure.3.13 (b) and the bandwidth is found as 500 MHz

3.6 SELF CASCODE CURRENT MIRROR

The Self Cascode Current Mirror (SCCM) is shown in Figure 3.14. Here, the output stage of a conventional CM structure is replaced by the Self Cascode (SC) structure. M_4 serves the purpose of the level shifter. The circuit is simulated for 0.13 µm technology with level 7 parameters. I_{bias} of 5 µA is injected into it. The circuit operations are simulated for supply voltage of ±0.5 V.

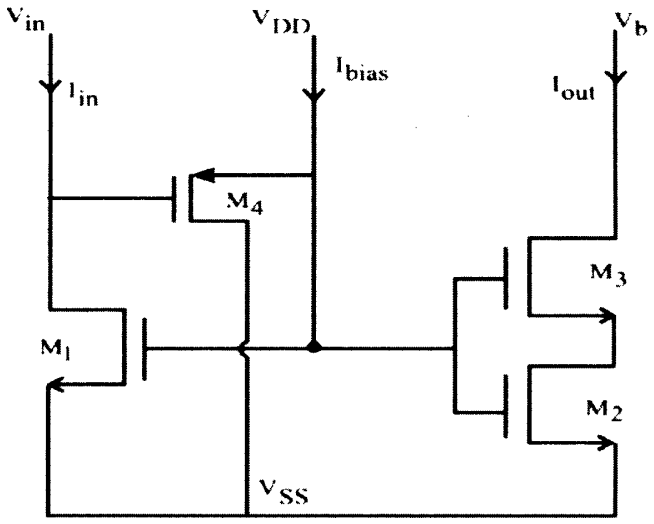

Figure 3.14 Self Cascode Current Mirror (SCCM) [8]

The input compliance voltage of 290 mV and the output compliance voltage of 300 mV are obtained for 90% of input current i.e. 100 µA. The output characteristic for low currents is shown in Figure 3.15. An offset current of 360 occurs at I_{in}= 0A.

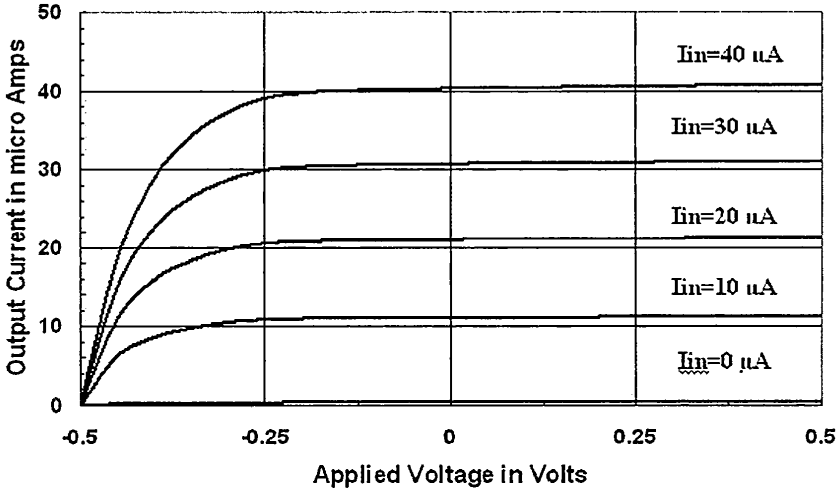

Figure 3.15 I-V Characteristics of SCCM at low currents [8]

For I_{in} of 100 µA the 3db bandwidth comes out to be 2.1 GHz. The influence of gate resistances at M_l, M_2, M_3 of SCCM over the bandwidth are shown in Figure 3.16(a). The gate resistance at M_1 (3 KΩ) increases the bandwidth to 2.2 GHz and for 5KΩ to 2.3 GHz. The capacitance in between the drain and gate of M_1 increases the bandwidth to 4.2 GHz. The bandwidth improves by threefold when both resistance and capacitor are included at M_l, it comes out to be 6.1 GHz (for R_g = 3 KΩ and C = 10 nF). The effect of resistive and capacitive compensation at M_1 of SCCM is shown in Figure 3.16(b).

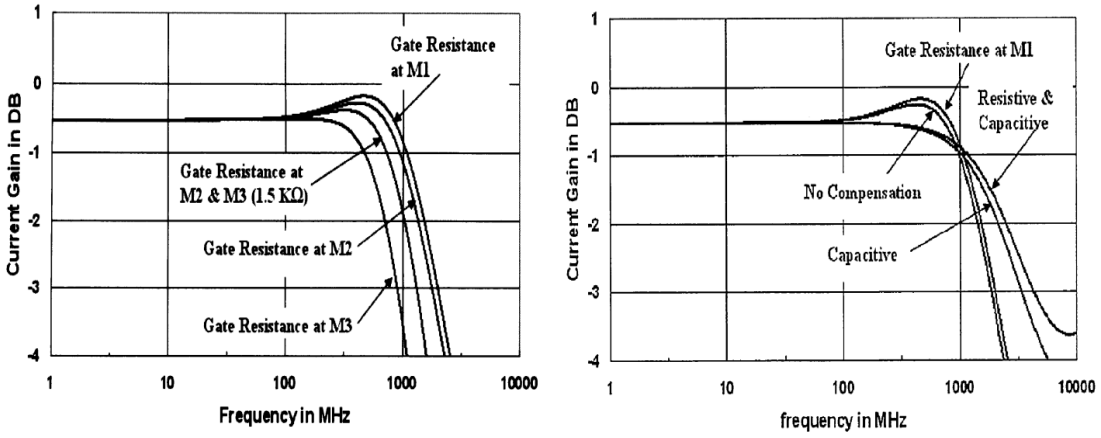

Figure 3.16 (a) Effect of Gate resistances at M_1, M_2, and M_3 on bandwidth of SCCM.

Figure 3.16 (b) Influence of various compensation techniques at M_1 on the bandwidth of SCCM [8]

3.7 VERY LOW INPUT IMPEDANCE LOW POWER CURRENT MIRROR

To get low input impedance, the main idea is to incorporate transistor M_3 in series with the input terminal of the basic circuit of the current mirror and use a gain amplifier of '−A' gain to control the gate voltage of M_3. In Figure 3.17 is shown a simple current mirror (a) and the conceptual schematic of the current mirror (b). Any increment in source voltage of M_3 (as the result of injected input current) causes its gate voltage to decrease '−A' times, hence causing stronger sink of input current which results in input impedance decrement by 'A'. Figure 3.18 shows transistor level implementations of this idea. As shown in Fig 3.18 (a) the amplifier can be implemented by only two transistors which act as a simple inverter for which input voltage is obtained as:

$$V_{in} = V_{gs3} + V_{ds4} \tag{3.30}$$

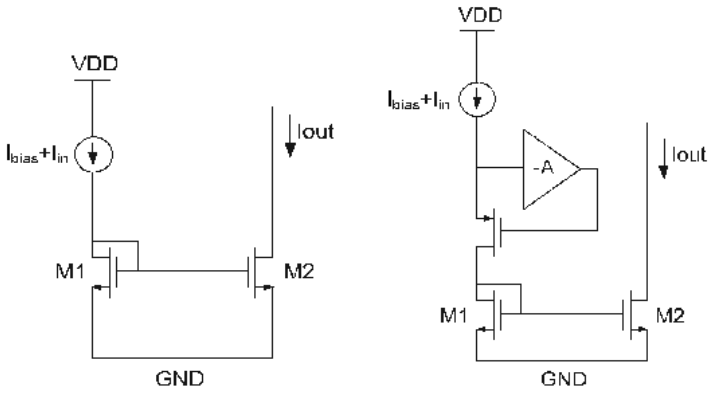

Figure 3.17 (a) A simple current mirror

(b) A conceptual schematic of the current mirror [10]

For the amplifier to have the significant gain required for perfect operation of the circuit, transistors M_4 and M_5 should operate in saturation region. If either of M_4 or M_5 leaves saturation condition, amplifier's gain reduces leading to increase of input impedance [10].

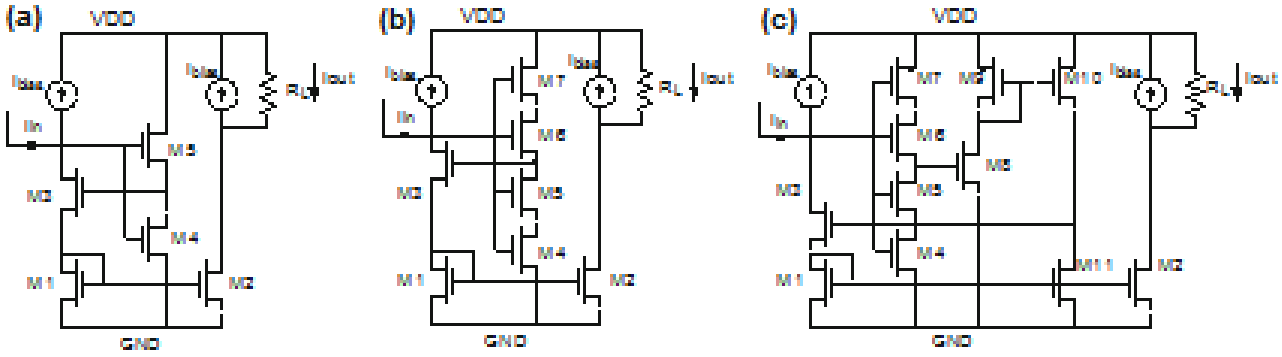

Figure 3.18 Transistor implementation of the low input impedance current mirror [9]

Figure 3.18(b) shows another implementation of the added amplifier using self cascode scheme. By using self cascode schematic, effective length of transistors can be increased causing two advantages: (1) the gain of the amplifier increases due to increase of its output resistance hence leads to lower input resistance; (2) amplifiers' current is decreased which saves power consumption. The gain of amplifier can be increased by adding two extra cascode transistors. But this method has two limits; (1) supply voltage limits due to increasing of cascode transistors; (2) input impedance bandwidth degradation due to existing of a very high impedance node in feedback loop. Another scheme to achieve a higher gain is cascading of gain stages. Figure 3.18(c) shows a current mirror in which amplifier of "A" is implemented by cascading of a self cascode inverter of "−A1" gain and a positive gain stage of "+A2" building by transistors M_8-M_{11}. So the amplifiers gain of "A" obtained as:

$$A = A1 * A2 \tag{3.31}$$

The advantage is that A can be increased without increase of power supply voltage.

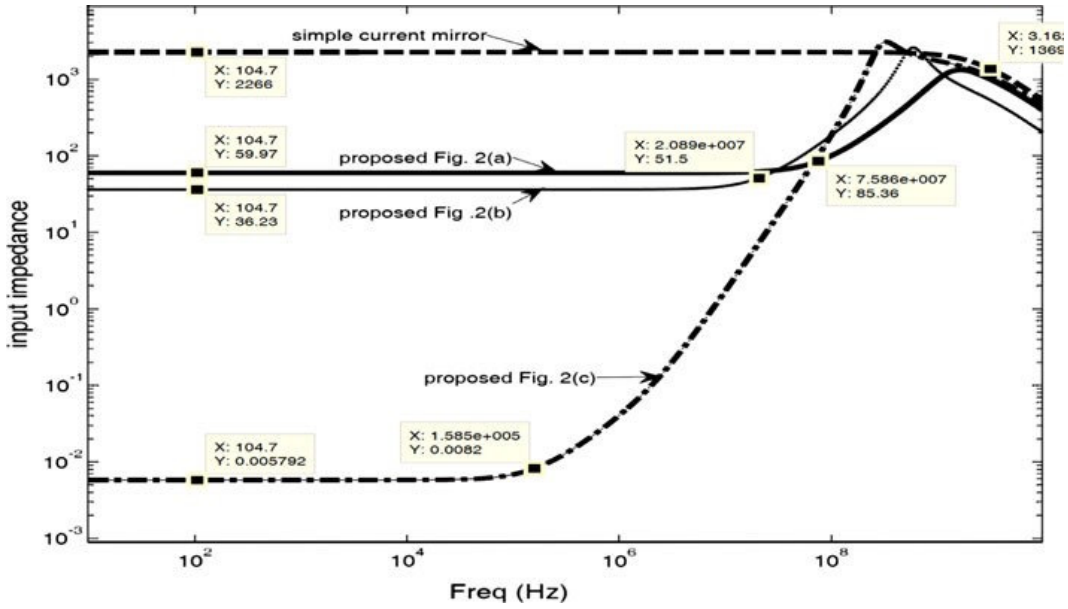

Figure 3.19 Comparison of input impedance of different circuits shown in Figure 19

Figure 3.19 shows that circuit of 3.18 (c) has minimum input impedance 5.8mΩ, which is 4×10^5 times smaller than input impedance of simple current mirror in same conditions and it has high frequency bandwidth of 577 MHz. It consumes only 161 µW power.

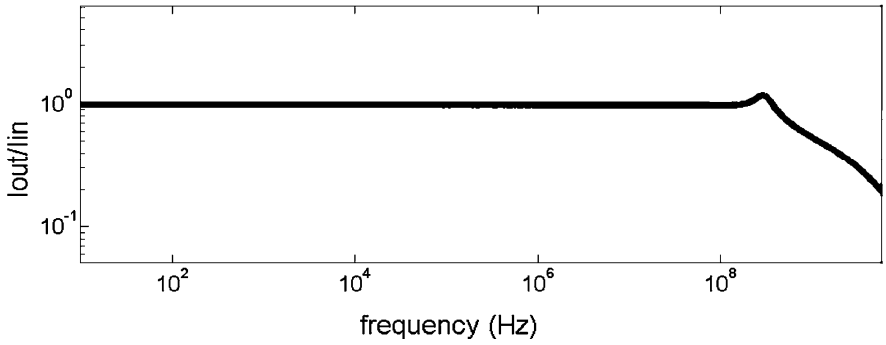

Figure 3.20 Frequency response of circuit figure 3.18 (c) [10]

3.8 COMPARISON OF DIFFERENT CURRENT MIRROR CIRCUITS

In this section different current mirror circuits discussed above are compared in tabular form. These all current mirror circuits are compared in terms of current mirror characteristics parameters. Table 3.2 comparing the different current mirror circuits

Table 3.2 Comparison of different current mirror circuits.

Circuit Name	Simulation Technology	Input Current Range (I_{in})	Supply Voltage	Input impedance (R_{in})	Output Impedance (R_{out})	Bandwidth (BW)
Simple LVCM	0.8 µm	1-500µA	± 1.0 V	650Ω	850 KΩ	2 GHz
ABLVCM	1.2 µm	1-500µA	± 1.0 V	1.8KΩ	1 MΩ	1.2 GHz
FGMOS LVCM	0.5 µm	100nA-500µA	± 0.75 V	200 Ω	1.35 MΩ	500 MHz
SC LVCM	0.13 µm	1-100 µA	± 0.5 V	1 KΩ	0.62 MΩ	6.1 GHz
Low input imp, Low power CM	0.18 µm	1-100 µA	1.5 V	5.8 mΩ	407 KΩ	577MHz

CHAPTER 4

HIGH OUTPUT IMPEDANCE LOW-VOLTAGE CURRENT MIRROR

4.1 INTRODUCTION

In this chapter a high output impedance low-voltage current mirror circuit is discussed. The chapter is organized as follows: The high output impedance low-voltage current mirror circuit is discussed in section 4.2. In section 4.3, the AC analysis of the circuit is presented. Section 4.4 discusses the simulation results.

4.2 CIRCUIT DESCRIPTION

The high output impedance Current Mirror (CM) is shown in Figure 4.1 [18]. The main idea is to increase the loop gain by a factor $g_m r_o$ by cascoding transistor M_1while maintaining the drain symmetry of the current mirror formed by M_2 and M_4. In the circuit bias-loop circuit is formed by transistors M_1 to M_4. In the circuit bias current and input current is denoted by I_{in} and I_B. With the output transistor M_5 disconnected out from the loop and with no input current applied at the drain of transistor M_2 ($I_{in} = 0$) the steady-state drain voltage of M_1, $V_{D,M1}$, is equal to that of M_3, and is thus equal to their gate bias voltage V_B. Furthermore, mirror transistors M_2 and M_4 are at the same saturation level I_F/I_R (the ratio of their forward current component to their reverse current component [17]). As a consequence, their drain voltages are identical: $V_{D,M2} = V_{D,M4}$.

In the circuit, when output transistor M_5 closes the feedback loop and a current I_{in} is forced in the drain of transistor M_2. Since M_2 is biased with a gate voltage V_B to sink a current I_B, the current applied at its drain will disturb this steady state and result in an increase of its drain voltage. As a consequence, the gate-source voltage of transistor M_1 will be reduced, resulting in a rapid increase of its drain voltage to allow current I_B to keep flowing. This voltage being applied to the gate of the output transistorM_5, the output current will increase and so will the bias voltage V_B, which is determined by the sum of the drain voltage of M_4 and the gate-source voltage of M_3: $V_B = V_{D,M4} + V_{GS,M3.}$ The steady state will be reached when the current through M_4 is equal to $I_{in} + I_B$, such that the current forced out of the source of M_1 is equal to $I_{D,M2} - I_{in} = I_B$. At that point, the saturation level of transistors M_2 and M_4 is exactly equal to $\frac{I_F}{I_R} = 2 + \frac{I_{in}}{I_B}$ and their drain-source saturation voltage $V_{DS,SAT}$ is identical as well. Therefore, the drain symmetry of the current mirror formed by M_2 and M_4 is maintained and there is no current offset between the output and input currents; the output current I_{out} is exactly equal to I_{in}.

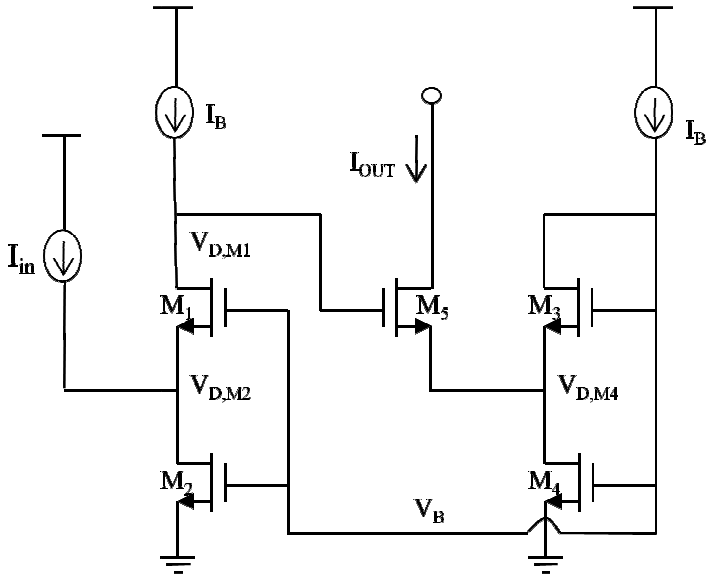

Figure 4.1 High output impedance low-voltage CM schematic circuit [18].

4.3 AC ANALYSIS

In this section the AC analysis of the high output impedance low-voltage CM circuit has been performed. The AC equivalent model of this circuit is shown in Figure 4.2

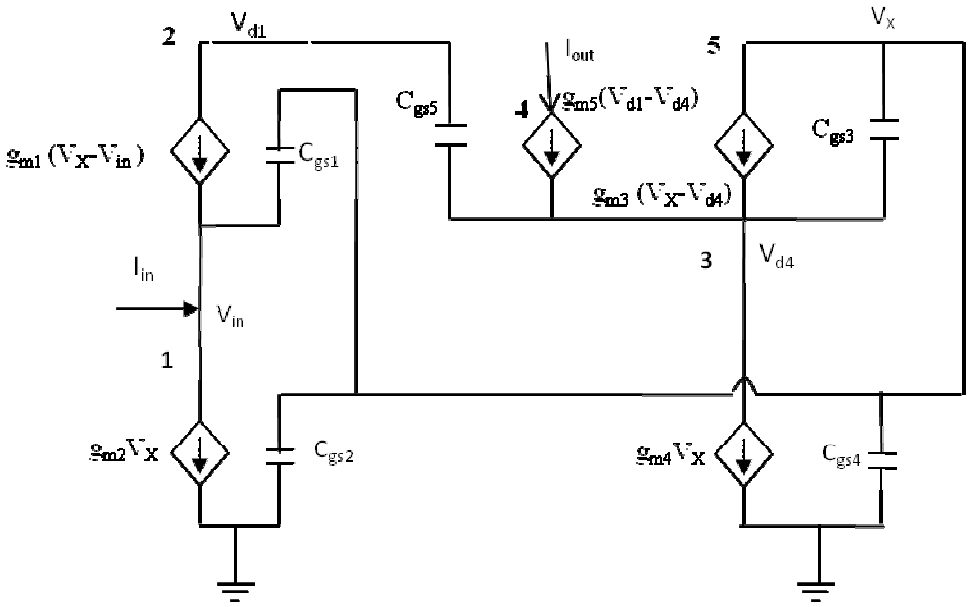

Figure 4.2 AC model of the high output impedance low-voltage CM circuit (Figure 4.1)

where g_{mi} (i = 0 to 5) and C_{gsi}(i = 0 to 5) is the transconductance and gate-to-source capacitance of the i^{th} transistor, respectively. Similarly $V_{in,}V_{d1,}V_{d4}$ is the input voltage, drain voltage of the transistor $M_{1,}$ drain voltage of the transistor $M_{4,}$ respectively. V_X is the gate voltage of the transistors $M_{1,}M_{2,}M_{3,}M_{4.}$

As per schematic circuit

$$g_{m1} = g_{m3}; g_{m2} = g_{m4} \tag{4.1}$$

The given AC equivalent model (Figure 4.2) can be modified as Figure 4.3.

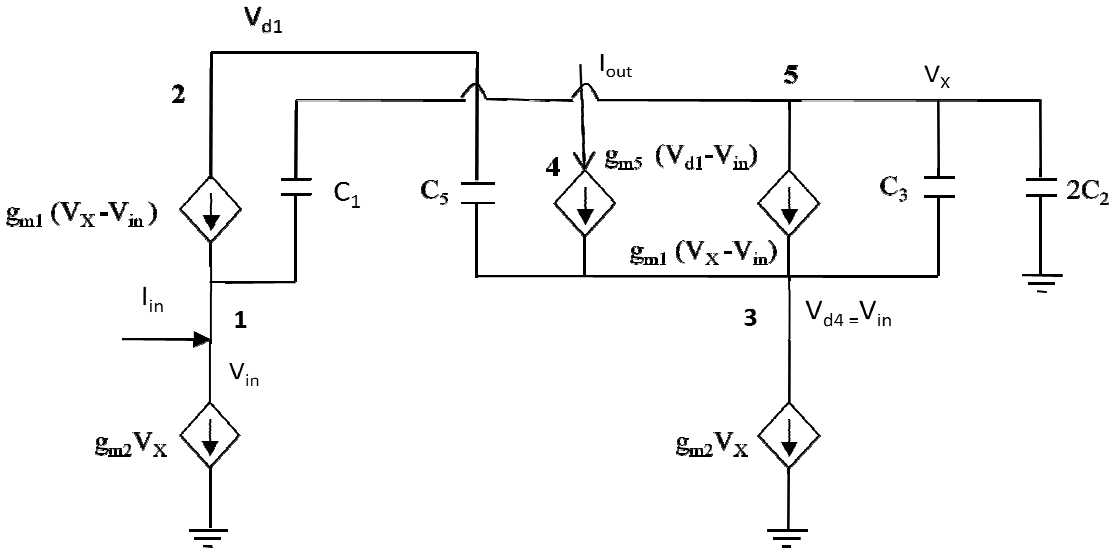

Figure 4.3 Simplified AC equivalent model of the Figure 4.2

In the AC equivalent model, it is assumed that

$$C_1 = C_{gs1}; C_2 = C_{gs2} = C_{gs4}; C_3 = C_{gs3}; C_5 = C_{gs5} \tag{4.2}$$

Applying KCL at node 4, the output current I_{out} is

$$I_{out} = g_{m5}(V_{d1} - V_{in}) \tag{4.3}$$

Applying KCL at node 1, the relation can be expressed as

$$I_{in} + g_{m1}(V_X - V_{in}) = g_{m2}V_X + (V_{in} - V_X)\, sc_1 \tag{4.4}$$

Equation (4.4) can be written as

$$I_{in} = V_X(g_{m2} - g_{m1} - sc_1) + V_{in}\,(sc_1 + g_{m1}) \tag{4.5}$$

Applying KCL at node 2, relation is

$$g_{m1}(V_X - V_{in}) + (V_{d1} - V_{in})sc_5 = 0 \tag{4.6}$$

After simplification (4.6), reduces to

$$V_X = \left[\frac{V_{in}(sc_5+g_{m1})-V_{d1}sc_5}{g_{m1}}\right] \tag{4.7}$$

Applying KCL at node 3, the expression is

$$g_{m2}V_X + (V_{in} - V_{d1})sc_5 + (V_{in} - V_X)sc_3 = g_{m5}(V_{d1} - V_{in}) + g_{m1}(V_X - V_{in}) \tag{4.8}$$

After simplification (4.8), can be written as

$$V_X(g_{m2} - sc_3 - g_{m1}) = V_{d1}(sc_5 + g_{m5}) - V_{in}(sc_3 + sc_5 + g_{m1} + g_{m5}) \tag{4.9}$$

Using (4.7) in (4.9), it can be expressed as

$$\left[\frac{V_{in}(g_{m1}+sc_5)-V_{d1}sc_5}{g_{m1}}\right](g_{m2} - sc_3 - g_{m1}) = V_{d1}(sc_5 + g_{m5}) - V_{in}(sc_3 + sc_5 + g_{m1} + g_{m5}) \tag{4.10}$$

By simplifying (4.10), the voltage V_{d1} is

$$V_{d1} = V_{in}\left[\frac{(sc_5+g_{m1})(g_{m2}-g_{m1}-sc_3)+g_{m1}(sc_3+sc_5+g_{m1}+g_{m5})}{g_{m1}(sc_5+g_{m5})+sc_5(g_{m2}-sc_3-g_{m1})}\right] \tag{4.11}$$

Using (4.11) in (4.3), the output current I_{out} is

$$I_{out} = g_{m5}V_{in}\left[\frac{(sc_5+g_{m1})(g_{m2}-g_{m1}-sc_3)+g_{m1}(sc_3+sc_5+g_{m1}+g_{m5})}{g_{m1}(sc_5+g_{m5})+sc_5(g_{m2}-sc_3-g_{m1})} - 1\right] \tag{4.12}$$

By simplifying (4.12), the output current I_{out}

$$I_{out} = V_{in}\left[\frac{g_{m1}g_{m2}g_{m5}}{g_{m1}(sc_5+g_{m5})+sc_5(g_{m2}-sc_3-g_{m1})}\right] \tag{4.13}$$

Using (4.7) in (4.5), input current I_{in} is

$$I_{in} = \left[\frac{V_{in}(sc_5+g_{m1})-V_{d1}sc_5}{g_{m1}}\right]\ (g_{m2} - g_{m1} - sc_1) + V_{in}\,(sc_1 + g_{m1}) \tag{4.14}$$

After simplification (4.14) can be written as

$$I_{in} = \left[\frac{V_{in}[(sc_5+g_{m1})(g_{m2}-g_{m1}-sc_1)+g_{m1}(sc_1+g_{m1})]-V_{d1}sc_5(g_{m2}-g_{m1}-sc_1)}{g_{m1}}\right] \tag{4.15}$$

Dividing (4.13) by (4.15), the current gain can be written as

$$\frac{I_{out}}{I_{in}} = \frac{g_{m1}^2 g_{m2}g_{m5}}{c_1c_3c_5^2(s^4+s^3X_1+s^2X_2+sX_3+X_4)} \tag{4.16}$$

where $$X_1 = \frac{(C_3 g_{m1} - C_3 g_{m2} - C_1 g_{m1})}{C_1 C_3} \quad (4.17)$$

$$X_2 = \frac{(C_5 g_{m1}^2 - C_1 g_{m1} g_{m5} - C_5 g_{m1} g_{m2} + C_5 g_{m1}^2 - C_3 - C_3 g_{m1} g_{m2})}{C_1 C_3 C_5} \quad (4.18)$$

$$X_3 = \frac{(g_{m1} g_{m2} g_{m5} - g_{m1}^2 g_{m5} - g_{m2} + g_{m1} g_{m2}^2)}{C_1 C_3 C_5} \quad (4.19)$$

$$X_4 = \frac{(g_{m1}^2 g_{m2} g_{m5} - g_{m1} g_{m2} - g_{m1} g_{m5})}{C_1 C_3 C_5} \quad (4.20)$$

As from relation (4.16), this circuit current gain has four poles and as per mathematical calculation these are complex conjugate poles.

4.4 SIMULATION RESULTS

In this section DC and AC characteristics of the high output impedance low-voltage CM schematic circuit have been discussed.

4.4.1 DC CHARACTERISTICS

Current transfer characteristics of the high output impedance low-voltage CM circuit is shown in Figure 4.4, it plots the output current versus input current. The input current is varied from 0 to 100 μA. From the plot of Figure 4.4, it can be seen that the output current follows the input current.

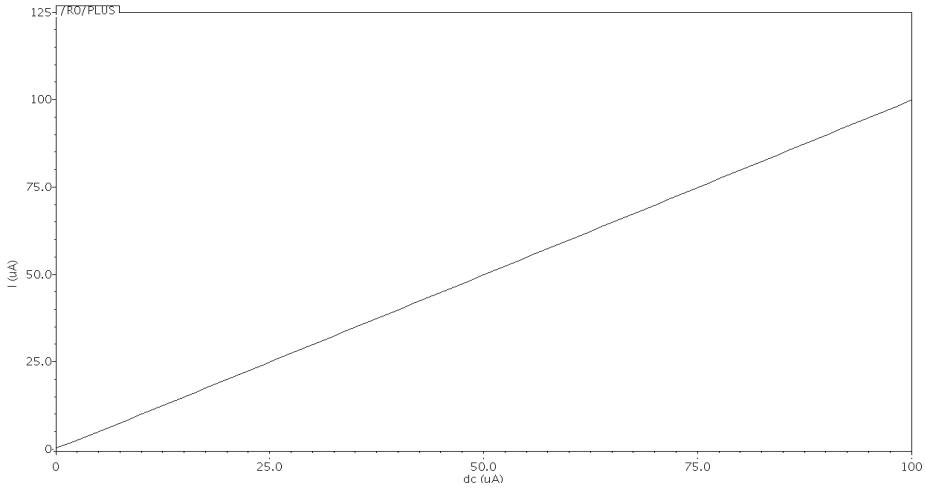

Figure 4.4 Current transfer characteristics of the high output impedance low-voltage CM circuit.

4.4.2 AC CHARACTERISTICS

The frequency response of the high output impedance low-voltage CM circuit is shown in Figure 4.5. In this response, current gain and frequency is taken at vertical and horizontal axis, respectively. In the beginning current gain is constant with the frequency and then overshoot occurs. This overshoot occurs due to complex conjugate poles in the circuit transfer function. The bandwidth of this circuit is 220 MHz.

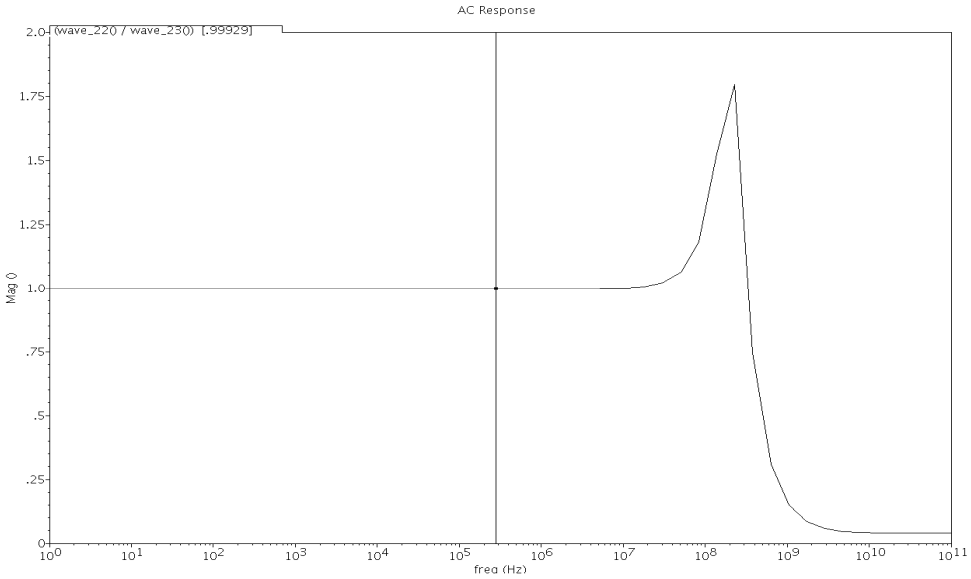

Figure 4.5 Frequency response of the high output impedance low-voltage CM circuit.

CHAPTER 5

PROPOSED LOW-VOLTAGE CURRENT MIRROR CIRCUIT

5.1 INTRODUCTION

In this chapter, low-voltage current mirror circuit structure operating at the supply voltage of + 1.3 volt is proposed. The bandwidth of the proposed circuit has been increased using resistive compensation technique. This chapter is organized as follows: the proposed current mirror circuit is discussed in section 5.2. In section 5.3, the proposed current mirror circuit AC analysis is presented. Section 5.4 discusses the AC analysis of the proposed current mirror circuit with enhanced bandwidth.

5.2 CIRCUIT DESCRIPTION

Figure 5.1 shows the proposed low-voltage current mirror circuit. In the proposed circuit the transistors M_4 and M_5 are generating the bias current. At node 1, two currents namely input current (I_{in}) and bias current (I_b) are injecting in which the input current is transferred to the output terminal (node 4). As per KCL, the value of W/L of transistor M_0 is chosen in such a manner that the current ($I_{in} + I_b$) will flow through it. The gate-to-source voltages (V_{gs}) of transistors M_0 and M_1 are equal therefore, the same current ($I_{in} + I_b$) will flow through the transistors. The remaining transistors are used to copy the currents and transfer to the appropriate nodes. Finally, the output current (I_{out}) through transistor M_8 is same as the input current (I_{in}).

The aspect ratios of the transistors M_0-M_7 are chosen as

$$\left(\frac{W}{L}\right)_{M0} = \left(\frac{W}{L}\right)_{M1};\ \left(\frac{W}{L}\right)_{M2} = \left(\frac{W}{L}\right)_{M3};$$

$$\left(\frac{W}{L}\right)_{M4} = \left(\frac{W}{L}\right)_{M5};\ \left(\frac{W}{L}\right)_{M6} = \left(\frac{W}{L}\right)_{M7} \tag{5.1}$$

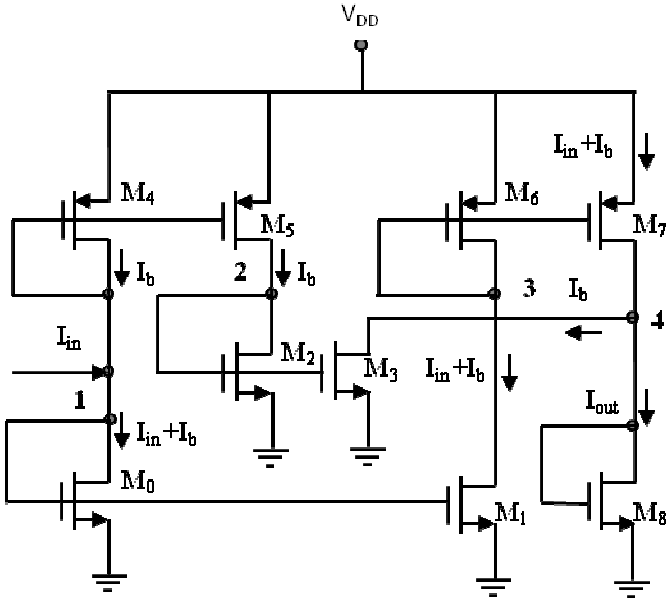

Figure 5.1 Proposed low-voltage current mirror circuit

Using KCL at node 4, the current expression can be written as

$$I_{out} + I_b = I_{in} + I_b \tag{5.2}$$

Now (5.2), reduces to

$$I_{out} = I_{in} \tag{5.3}$$

Relation (5.3) proves the current mirror behavior. The transconductance parameters and parasitic capacitances of the transistors are chosen as

$$g_{m0} = g_{m1};\ g_{m2} = g_{m3};\ g_{m4} = g_{m5};\ g_{m6} = g_{m7}$$

$$C_{gs0} = C_{gs1};\ C_{gs2} = C_{gs3};\ C_{gs4} = C_{gs5};\ C_{gs6} = C_{gs7} \tag{5.4}$$

5.3 AC ANALYSIS OF THE PROPOSED CIRCUIT

In this section the AC analysis of the proposed current mirror circuit is presented. The AC equivalent model of this circuit is shown in Figure 5.2

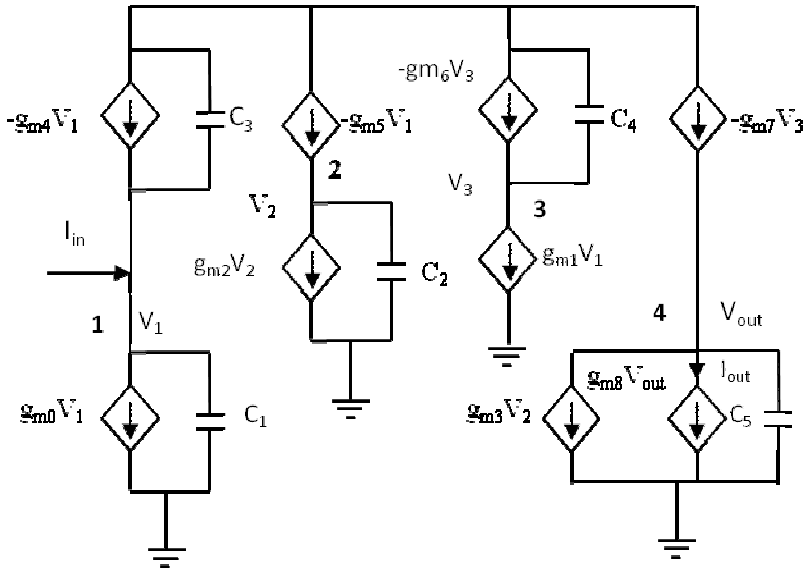

Figure 5.2 AC equivalent model of proposed low-voltage current mirror (Figure 5.1)

In this model, it is assumed that

$$C_1 = Cgs_0 + Cgs_1;\ C_2 = Cgs_2 + Cgs_3;\ \ C_3 = Cgs_4 + Cgs_5;$$

$$C_4 = Cgs_6 + Cgs_7;\ \ C_5 = Cgs_8 \tag{5.5}$$

where Cgsi (i = 0 to 8) is the gate to source capacitance of the i^{th} transistor.

From Figure 5.2, the output current I_{out} is

$$I_{out} = g_{m8}V_{out} \tag{5.6}$$

where g_{m8} is the transconductance of the transistor M_8 and V_{out} is the output voltage.

Using KCL at nodes 1, 2, 3 and 4, different expressions can be written as follows

$$I_{in} - g_{m4}V_1 = g_{m0}V_1 + sc_3V_1 + sc_1V_1 \tag{5.7}$$

$$-g_{m5}V_1 = g_{m2}V_2 + sc_2V_2 \tag{5.8}$$

$$-g_{m6}V_3 = g_{m1}V_1 + sc_4V_3 \tag{5.9}$$

$$-g_{m7}V_3 = g_{m8}V_{out} + g_{m3}V_2 + sc_5V_{out} \tag{5.10}$$

where g_{mi} (i = 0 to 8) is the transconductance of the i^{th} transistor and V_1, V2, and V_3 are the voltages at nodes 1, 2 and 3, respectively.

After simplification (5.7), (5.8), (5.9) and (5.10) reduces to (5.11), (5.12), (5.13) and (5.14), respectively as:

$$I_{in} = V_1[g_{m0} + sc_1 + sc_3 + g_{m4}] \tag{5.11}$$

$$V_2 = \frac{-g_{m5}V_1}{(sc_2+g_{m2})} \tag{5.12}$$

$$V_3 = \frac{-g_{m1}V_1}{(sc_4+g_{m6})} \tag{5.13}$$

$$V_{out}(sc_5 + g_{m8}) = -(g_{m3}V_2 + g_{m7}V_3) \tag{5.14}$$

Substituting (5.12) and (5.13) in (5.14), the output voltage V_{out} is

$$V_{out} = \frac{1}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \tag{5.15}$$

Using (5.15) in (5.6), the output current I_{out} is

$$I_{out} = \frac{g_{m8}}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \tag{5.16}$$

Dividing (5.16) by (5.11), the current gain is

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\,[g_{m1}g_{m7}(sc_2+g_{m2})+g_{m3}g_{m5}(sc_4+g_{m6})]}{(sc_5+g_{m8})(sc_1+sc_3+g_{m0}+g_{m4})(sc_2+g_{m2})(sc_4+g_{m6})}$$

The above relation can be written as:

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m1}g_{m7}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m3}g_{m5}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{c_5(c_1+c_3)\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \tag{5.17}$$

The transconductance parameters and parasitic capacitances of the transistors are chosen as

$$g_{m0} = g_{m1};\ g_{m2} = g_{m3};\ g_{m4} = g_{m5};\ g_{m6} = g_{m7}$$

$$C_{gs0} = C_{gs1};\ C_{gs2} = C_{gs3};\ C_{gs4} = C_{gs5};\ C_{gs6} = C_{gs7} \tag{5.18}$$

Using (5.18) in (5.17), (5.17) becomes

$$\frac{I_{out}}{I_{in}} = \frac{g_{m8}\left[\frac{g_{m0}g_{m6}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m2}g_{m4}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{c_5(c_1+c_3)\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \tag{5.19}$$

From (4.19), it can be seen that the transfer function exhibits a dominant pole (at $s = \frac{-g_{m6}}{c_4}$) which decide the bandwidth of the proposed circuit.

5.4 LOW VOLTAGE CURRENT MIRROR CIRCUIT WITH ENHANCED BANDWIDTH

In this section low-voltage current mirror circuit with enhanced bandwidth is described. The AC analysis also has been discussed.

5.4.1 CIRCUIT DESCRIPTION

The bandwidth of the proposed circuit has been improved by modifying the circuit as shown in Figure 5.3. In this circuit, a resistance R is connected between drain and gate terminals of the transistor M_0 [16]. This circuit working is similar to first circuit. In this figure, the resistance(R) connected between drain and gate terminals of the transistors M_0 create the voltage difference between two terminals.

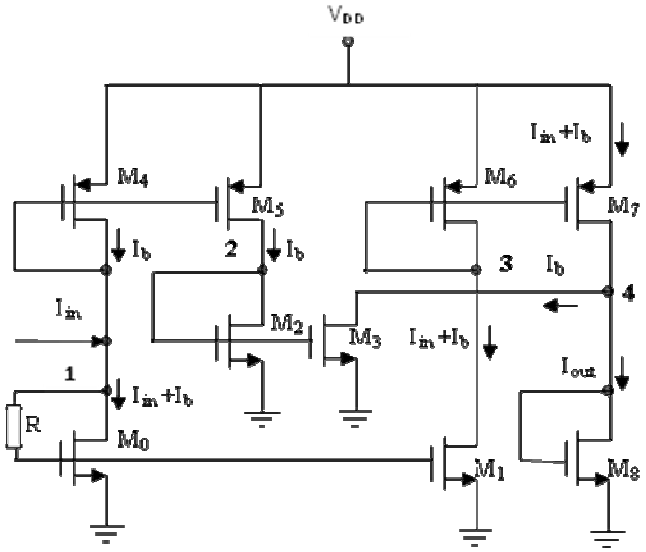

Figure 5.3 Proposed low-voltage current mirror circuit with enhanced bandwidth.

5.4.2 AC ANALYSIS OF THE PROPOSED CIRCUIT WITH ENHANCED BANDWIDTH

In this section the AC analysis of the bandwidth enhanced proposed circuit has been performed and the AC equivalent model of this circuit is shown in Figure 5.4

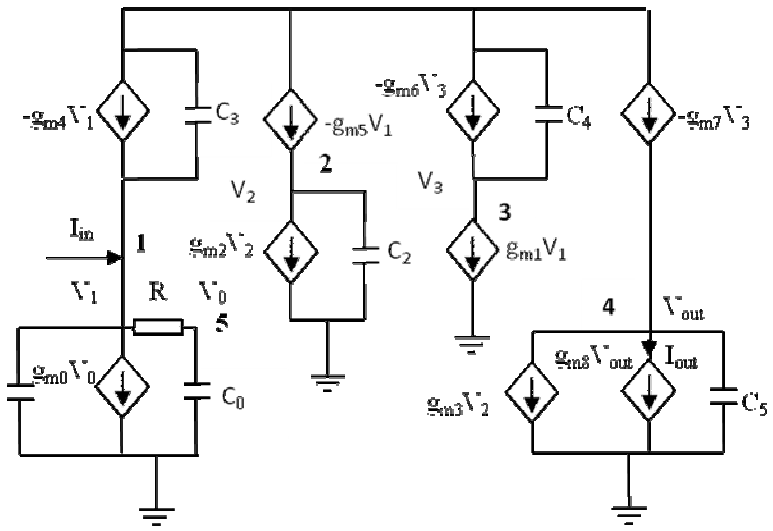

Figure 5.4 AC equivalent model of enhanced bandwidth current mirror circuit (Figure 5.3).

In this AC equivalent model, it is assumed that

$$C_0 = Cgs_0;\ C_1 = Cgs_1;\ \ C_2 = Cgs_2 + Cgs_3;$$

$$C_3 = Cgs_4 + Cgs_5;\ C_4 = Cgs_6 + Cgs_7;\ \ C_5 = Cgs_8 \qquad (5.20)$$

where Cgsi (i = 0 to 8) is the gate-to-source capacitance of the i^{th} transistor.

From Figure 5.4, the output current I_{out} is

$$I_{out} = g_{m8}V_{out} \qquad (5.21)$$

where g_{m8} is the transconductance of the transistor M_8 and V_{out} is the output voltage.

Using KCL at nodes 1, 2, 3, 4 and 5, different expression can be written as follows

$$I_{in} - g_{m4}V_1 = g_{m0}V_0 + sc_3V_1 + sc_1V_1 + \frac{V_1 - V_0}{R} \qquad (5.22)$$

$$-g_{m5}V_1 = g_{m2}V_2 + sc_2V_2 \qquad (5.23)$$

$$-g_{m6}V_3 = g_{m1}V_1 + sc_4V_3 \qquad (5.24)$$

$$-g_{m7}V_3 = g_{m8}V_{out} + g_{m3}V_2 + sc_5V_{out} \qquad (5.25)$$

$$\frac{V_0 - V_1}{R} + sc_0V_0 = 0 \qquad (5.26)$$

where g_{mi} (i = 0 to 8) is the transconductance of the i^{th} transistor. The V_0, V_1, V2, and V_3 are the voltages at nodes 0, 1, 2 and 3, respectively.

After simplification (5.22), (5.23), (5.24), (5.25) and (5.26) reduces to (5.27), (5.28), (5.29), (5.30) and (5.31), respectively as:

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + sc_1 + sc_3\right] + V_0 \left[g_{m0} - \frac{1}{R}\right] \tag{5.27}$$

$$V_2 = \frac{-g_{m5}V_1}{(sc_2+g_{m2})} \tag{5.28}$$

$$V_3 = \frac{-g_{m1}V_1}{(sc_4+g_{m6})} \tag{5.29}$$

$$V_0 = \frac{V_1}{1+Rsc_0} \tag{5.30}$$

Substituting (5.30) in (5.27), the input current I_{in} is

$$I_{in} = V_1 \left[g_{m4} + \frac{1}{R} + sc_1 + sc_3\right] + \frac{V_1}{1+Rsc_0}\left[g_{m0} - \frac{1}{R}\right] \tag{5.31}$$

With further calculation (5.31), may be written as

$$I_{in} = \frac{V_1[s^2Rc_0(c_1+c_3)+s(Rg_{m4}c_0+c_0+c_1+c_3)+g_{m0}+g_{m4}]}{(1+Rsc_0)} \tag{5.32}$$

Using (5.28) and (5.29) in (5.25), the output voltage V_{out} is

$$V_{out} = \frac{1}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \tag{5.33}$$

Substituting (5.33) in (5.21), the output current I_{out} is

$$I_{out} = \frac{g_{m8}}{(sc_5+g_{m8})}\left[\frac{g_{m3}g_{m5}V_1}{(sc_2+g_{m2})} + \frac{g_{m1}g_{m7}V_1}{(sc_4+g_{m6})}\right] \tag{5.34}$$

Divinding (5.34) by (5.32), the current gain is

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{m8}\,[g_{m1}g_{m7}(sc_2+g_{m2})+g_{m3}g_{m5}(sc_4+g_{m6})]}{(sc_5+g_{m8})(sc_2+g_{m2})(sc_4+g_{m6})} \times \frac{(Rsc_0+1)}{[s^2Rc_0(c_1+c_3)+s(Rg_{m4}c_0+c_0+c_1+c_3)+g_{m0}+g_{m4}]} \tag{5.35}$$

The above relation can be written as:

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{m8}\left[\frac{g_{m1}g_{m7}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m3}g_{m5}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \times \frac{\left(s+\frac{1}{Rc_0}\right)}{(c_1+c_3)\left[s^2+s\frac{c_0(1+g_{m4}R)+c_1+c_3}{(c_1+c_3)}+\frac{g_{m0}+g_{m4}}{(c_1+c_3)}\right]} \quad (5.36)$$

The transconductance parameters and parasitic capacitances of the transistors are chosen as

$$g_{m0} = g_{m1};\ g_{m2} = g_{m3};\ g_{m4} = g_{m5};\ g_{m6} = g_{m7}$$

$$C_{gs0} = C_{gs1};\ C_{gs2} = C_{gs3};\ C_{gs4} = C_{gs5};\ C_{gs6} = C_{gs7} \quad (5.37)$$

Using (5.37) in (5.36), (5.36) becomes

$$\frac{I_{OUT}}{I_{IN}} = \frac{g_{m8}\left[\frac{g_{m0}g_{m6}}{c_4}\left(s+\frac{g_{m2}}{c_2}\right)+\frac{g_{m2}g_{m4}}{c_2}\left(s+\frac{g_{m6}}{c_4}\right)\right]}{\left(s+\frac{g_{m2}}{c_2}\right)\left(s+\frac{g_{m6}}{c_4}\right)\left(s+\frac{g_{m8}}{c_5}\right)\left(s+\frac{g_{m0}+g_{m4}}{c_1+c_3}\right)} \times \frac{\left(s+\frac{1}{Rc_0}\right)}{(c_1+c_3)\left[s^2+s\frac{c_0(1+g_{m4}R)+c_1+c_3}{(c_1+c_3)}+\frac{g_{m0}+g_{m4}}{(c_1+c_3)}\right]} \quad (5.38)$$

From (5.38), it can be seen that the transfer function has two zeros and five poles. In (5.19), the transfer function has one zero and four poles. Therefore, it is evident that the resistance R connected between drain and gate of the transistor M_0 introduces a zero and a pole in the transfer function of Figure 5.3. This introduced zero cancels the dominant pole and therefore, the bandwidth of the proposed circuit (Figure 5.1) is now enhanced. . The MOSFETs sizes in term of channel width to length ratio are listed in Table 5.1.

In back end layout diagram these all MOSFET are drawn with multiple number of fingers to reduce parasitic to get accurate post-layout simulation results.

Table 5.1 MOSFET Sizes

MOSFET	W/L RATIO (μm)
M_0	44.8/2.0
M_1	44.8/2.0
M_2	1.8/0.9
M_3	1.8/0.9
M_4	5.3/0.9
M_5	5.3/0.9
M_6	93.6/1.44
M_7	93.6/1.44
M_8	16.38/0.9

CHAPTER 6

SIMULATION RESULTS AND LAYOUT

6.1 INTRODUCTION

The proposed circuit has been simulated using CADENCE design environment in UMC 0.18 µm CMOS process technology. This chapter is organized as follows: The simulation results of the proposed current mirror circuits are discussed in section 6.2. Section 6.3 presents the layout designing of proposed circuit. In section 6.4, post-layout simulation results are discussed.

6.2 SIMULATION RESULTS

In this section simulation results of the proposed low-voltage current mirror circuit without and with bandwidth enhancement resistance have been discussed.

6.2.1 DC CHARACTERISTICS

Figure 6.1 shows the current transfer characteristic of the proposed current mirror circuit and plots the output current versus input current. In Figure 6.1, input and output current is taken at horizontal and vertical axis, respectively. The input current is varied from 0 to 100μA. From the plot of Figure 6.1, it can be seen that the output current I_{OUT} varies linearly as input current I_{IN}. This type of response validates the effectiveness of the proposed circuit.

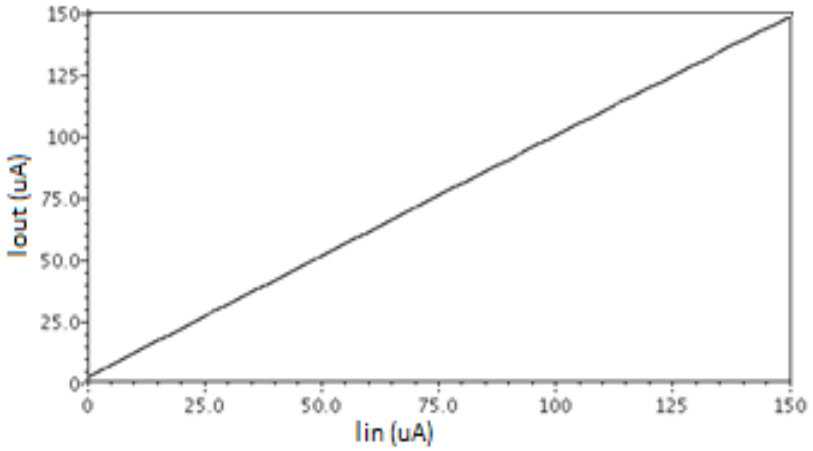

Figure 6.1 Current transfer characteristics of the proposed current mirror circuit

6.2.2 AC CHARCTERISTICS

Figure 6.2 shows the frequency response of the proposed circuits. In this figure current gain and frequency is taken at vertical and horizontal axis, respectively. In the same figure, frequency response of the proposed circuit with bandwidth enhancement resistance ($R_1 = 3.7K\Omega$) is also drawn. The bandwidths of the proposed circuits without and with enhancement resistance are 60 MHz and 163 MHz, respectively.

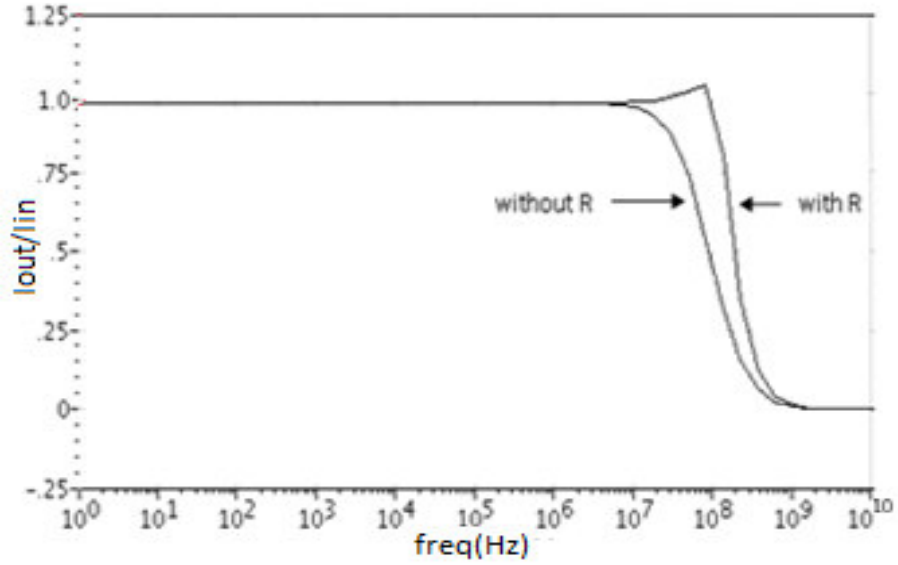

Figure 6.2 Frequency response of the proposed current mirror circuits.

6.3 LAYOUT DESIGNING

In this section layout designing of the proposed low-voltage current mirror circuit have been discussed.

The physical layout design of proposed current mirror circuit has been done in standard UMC 0.18 µm CMOS process technology. The Virtuoso layout editor tool by Cadence was used for the design of physical layout structure. The extracted layout views of low-voltage current mirror circuits without and with enhanced bandwidth are shown in the Figure 6.3 and 6.4, respectively. During post-layout simulation extracted layout views are need to be attached with schematic circuits. Basic design rules are summarized below:

Metal 1 to metal 1 spacing	0.24 um
Minimum contact size	0.24 um*0.24 um
Poly to poly spacing	0.24 um
Poly to metal spacing	0.28/0.00 um
Contact overlap to p+ diffusion	0.10 um
Metal 1 width	0.24 um
Poly extension beyond active	0.22 um
Minimum contact spacing	0.26 um
N well overlap p+ diffusion	0.43 um
Diffusion contact to poly spacing	0.15 um
Minimum p+ implant overlap p+ diffusion	0.22 um
Poly width	0.18 um
Minimum poly extension on to field region	0.22 um
Minimum poly gate to field edge spacing	0.28 um

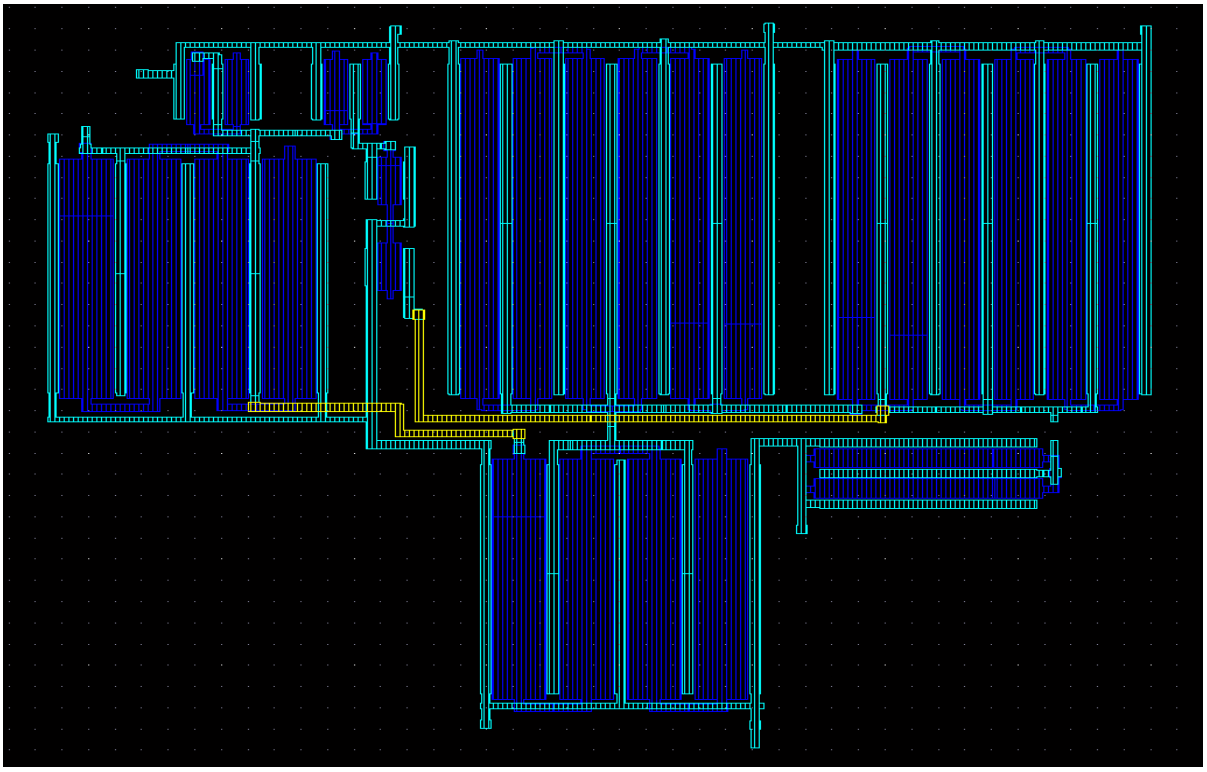

Figure 6.3 Extracted layout view of the proposed current mirror circuit.

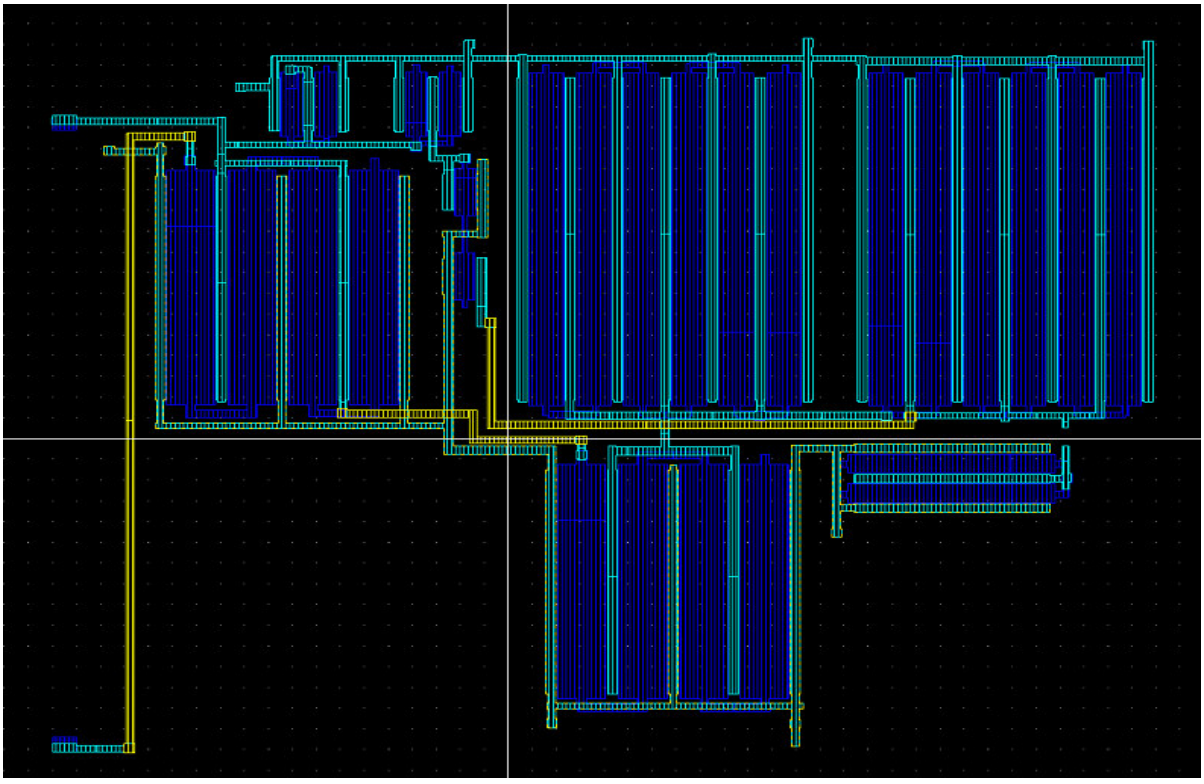

Figure 6.4 Extracted layout view of the proposed current mirror circuit with bandwidth enhancement resistance

6.4 POST-LAYOUT SIMULATION RESULTS

In this section post-layout simulation results of the proposed low-voltage current mirror circuit have been discussed.

6.4.1 DC CHARCTERISTICS

The post-layout current transfer characteristic of the proposed current mirror circuit is shown in Figure 6.5. Output current (I_{out}) is varying linearly as input current I_{in}. Pre-layout and post-layout current transfer responses of the proposed current mirror circuits are same. This type of response approves the effectiveness of proposed current mirror circuits.

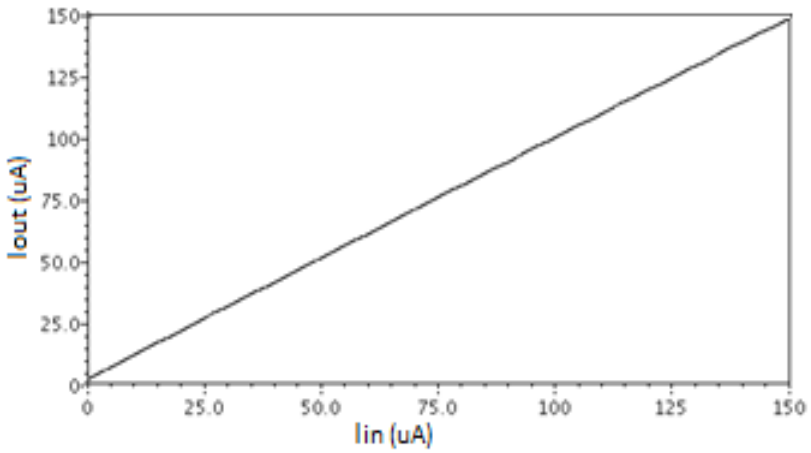

Figure 6.5 Post-layout current transfer characteristics of the proposed current mirror circuit.

6.4.2 AC CHARCTERISTICS

The post-layout AC response of the proposed current mirror circuit is shown in Figure 6.6. The bandwidths of the proposed circuits without and with enhancement resistance ($R_1 = 3.7K\Omega$) are 60 MHz and 160 MHz, respectively. The percentage gain error ($I_{out}\backslash I_{in}$) in simulation results and post-layout simulation results of the proposed circuit is 0.25%.

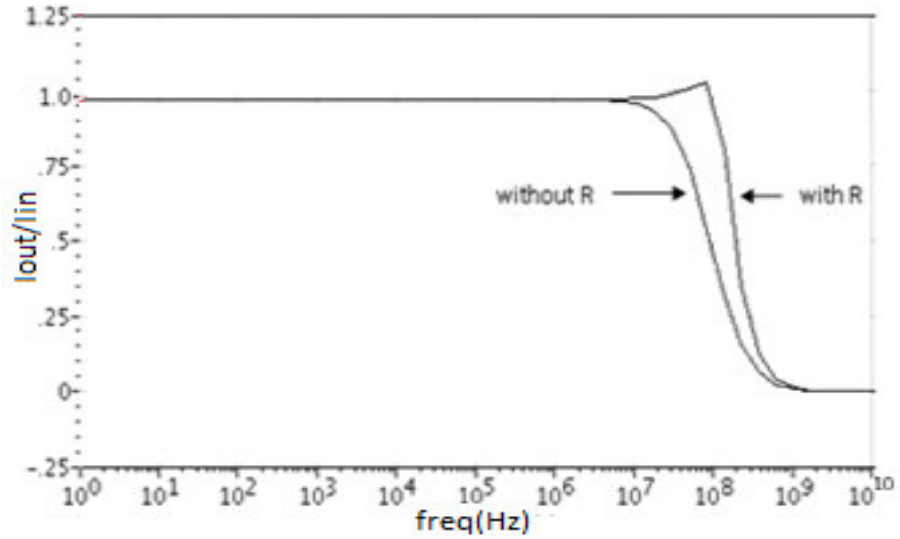

Figure 6.6 Post-layout frequency responses of the proposed current mirror circuits

Table 6.1 shows the comparison of the proposed low-voltage current mirror circuit with other current mirror circuits proposed in literature [2], [3] and [10]. It can be seen that proposed low-voltage current mirror circuit has lower power supply voltage requirement as compared to the current mirror circuits reported in [2], [3] and [10].

Table 6.1 Comparison of proposed low-voltage current mirror circuit with different current mirror structure reported in [2], [3] an [10].

Circuit Name	Simulation Technology	Input Current Range (I_{in})	Supply Voltage	Input Impedance (R_{in})	Output Impedance (R_{out})	Bandwidth (BW)
Simple LVCM[2]	0.8 µm	1-500µA	± 1.0 V	650Ω	850 KΩ	2 GHz
ABLVCM [3]	1.2 µm	1-500µA	± 1.0 V	1.8KΩ	1 MΩ	1.2 GHz
Low input impedance, Low power CM[10]	0.18 µm	1-100 µA	1.5 V	5.8 mΩ	407 KΩ	577MHz
Proposed Low voltage current mirror	0.18 µm	1-100 µA	1.3 V	NA	NA	163MHz

CHAPTER 7

CONCLUSION AND FURTHER DEVELOPMENT

7.1 CONCLUSION

In this thesis, a new low-voltage current mirror circuit operating at a supply voltage of +1.3V is presented. The bandwidth of this circuit has been enhanced using resistive compensation technique. The mathematical analysis of the frequency response has also been presented. The simulation and layout results have been presented to demonstrate the feasibility of the proposed current mirror circuit.

7.2 SUGGESTION FOR FURTHER DEVELOPMENT

The input impedance of the proposed circuit can be reduced by applying amplifier at the gate terminal of the input transistor as described in section 3.7.

The output impedance of the proposed circuit can be improved by applying cascode, self cascode stage at the output terminals. The output impedance also can be improved by adding differential amplifier stage at the gate terminal of the output transistor with one reference voltage source.

REFERENCES

1. Behzad Razavi, Design of analog Integrated Circuits, McGraw Hill, 2001.
2. S. S. Rajput and S. S Jamuar, "A high performance current mirror for low voltage designs," *Asia-Pacific Conference on Circuits and Systems*, pp. 170-173, Dec 2000.
3. S. S. Rajput and S. S Jamuar, "Low voltage, low power, high performance current mirror for portable analogue and mixed mode applications," *IEEE Proc.- Circuits, Devices and systems*, Vol. 148, No. 5, pp. 273-278, Oct 2001.
4. Susheel Sharma, S. S. Rajput, L. K. Magotra and S. S Jamuar, "FGMOS based wide range low voltage current mirror and its applications," *Asia-Pacific Conference on Circuits and Systems*, Vol. 2, pp. 331 - 334, Oct 2002.
5. S. S. Rajput and S. S Jamuar, "Ultra low voltage Current Mirror OP AMP and its applications," *Asia-Pacific Conference on Circuits and Systems*, Vol.1, pp.145 - 148, 2002.
6. S. S. Rajput and S. S Jamuar, "Advanced current mirrors for Low Voltage Analog Designs," *International Conference on Semiconductor Electronics*, Vol. 2, pp. 331 - 334, Dec 2004.
7. Rohan Sehgal, "A 0.8V operational amplifier using Floating Gate MOS technology," *International Conference on Semiconductor Electronics*, pp.795 – 799, Dec 2006.
8. Jasdeep Kaur, Nupur prakash and S. S. Rajput, "Low voltage high performance Self cascode CCII," *IEEE Proc.- INMIC*, pp. 7 – 11, Dec 2008.
9. S.S. Rajput, Prateek Vajpayee and G.K. Sharma, "1V high performance current mirror for low voltage analog and Mixed signal applications in submicron regime," *IEEE Proc.-TENCON*, pp. 1 – 4, Jan 2009.
10. Hassan Faraji Baghtash and Seyed Javad Azhari, "Very low input impedance low power current mirror," *Analog Integrated Circuits and Signal Processing*, Vol.

66, No. 1, pp. 9-18, 2010.

11. DJ. Comer and D.T. Comer, Fundamentals of Electronic Circuit Design. New York: John Wiley & sons Inc. 2003.
12. A. Zeki, H. Kuntman, "Accurate and high output impedance current mirrors suitable for CMOS current output stages," *Electronics Letters*, Vol. 33, pp. 1042 1043, Jun 1997.
13. J. Mulder, A. C. Woerd, W. A. Serdijn, and A. H. M Roermund., "High swing cascode MOS current mirror," *Electronics letters*, Vol. 32, pp. 1251-1252, Jul 1996.
14. B. A. Minch, "Low-Voltage Wilson Current Mirrors in CMOS," *Asia-Pacific Conference on Circuits and Systems*, pp. 170-173, Dec 2007.
15. David A Johns and Ken Martin, Analog Integrated Circuit Design, Wiley, 1996.
16. T. Voo and C. Toumazau, "High speed current mirror resistive compensation technique," *Electronic Letters*, Vol. 31, pp. 248-250, Feb 1995.
17. Louis-François Tanguay, Mohamad Sawan and Yvon Savaria, "A very high output impedance current mirror for very-low biomedical analog circuits," *Asia-Pacific Conference on Circuits and Systems,* pp. 642-645. Nov 2008.
18. B. Minch, "A Low-Voltage MOS Cascode Bias Circuit for All Current Levels," *International Symposium on Circuits and Systems*, Vol. 3, pp. 619-622, Aug 2002.

APPENDIX A

(A) MODEL PARAMETERS FOR PMOS TRANSISTOR

- model p_18_mm bsim3v3 type=p
- + mobmod=3.0000e+00 version=3.2000e+00 capmod=2.0000e+00
- + binunit=1.0000e+00 nqsmod=0.0000e+00
- + tox=4.2000e-09 + dtox_p_18_mm toxm=4.2000e-09
- + xj=1.0000e-07 nch=6.1310e+17 ngate=1.0000e+23
- + vth0= - 4.5550e-01 + dvth0_p_18_mm k1=5.7040e-01
- + k2=6.9730e-03 k3=-2.8330e+00 k3b=1.3260e+00
- + w0=-1.9430e-07 nlx=2.5300e-07 dvt0=4.8850e-01
- + dvt1=7.5780e-02 dvt2=1.2870e-01 dvt0w=-1.2610e-01
- + dvt1w=2.4790e+04 dvt2w=6.9150e-01 lint=-1.0410e-08
- + wint=-1.5250e-07 dwg=-1.1510e-07 dwb=-1.0390e-07
- + u0=1.1450e+02 + du0_p_18_mm ua=1.5400e-09
- + ub=2.6460e-19 uc=-9.5870e-02 vsat=5.3400e+04
- + a0=1.3500e+00 ags=3.8180e-01 b0=-3.0880e-07
- + b1=0.0000e+00 keta=1.0440e-02 a1=0.0000e+00
- + a2=1.0000e+00 voff=-1.0730e-01 nfactor=1.5350e-00
- + cit=-1.0670e-03 cdsc=7.5780e-04 cdscd=-2.8830e-05
- + cdscb=1.0000e-04 eta0=1.0710e+00 etab=-9.2910e-01
- + dsub=1.9191e+00 pclm=2.6530e+00 pdiblc1=0.0000e+00
- + pdiblc2=5.0000e-06 pdiblcb=0.0000e+00 drout=1.4570e+00
- + pscbe1=4.8660e+08 pscbe2=2.8000e-07 pvag=1.1620e+00
- + rdsw=7.9210e+02 prwg=0.0000e+00 prwb=0.0000e+00
- + alpha0=0.0000e+00 alpha1=0.0000e+00 beta0=3.0000e+01
- + cgdo=2.0540e-10 + dcgdo_p_18_mm cgbo=0.0000e+00
- + cgso=2.0540e-10 + dcgso_p_18_mm xpart=1.0000e+00
- + cf=1.5330e-10 dlc=5.6000e-08 cgsl=0.0000e+00
- + cgdl=0.0000e+00 ckappa=6.0000e-01 clc=1.0000e-07
- + cle=6.0000e-01 dwc=0.0000e+00 vfbcv=-1.0000e+00
- + noff=1.0000e+00 voffcv=0.0000e+00 acde=1.0000e+00
- + moin=1.5000e+01 lmin=1.8000e-07 lmax=5.0000e-05
- + wmin=2.4000e-07 wmax=1.0000e-04
- + xl= - 2.0000e-09 + dxl_p_18_mm
- + xw=0.0000e+00 + dxw_p_18_mm js=3.0000e-06
- + jsw=4.1200e-11 cj=1.1400e-03 + dcj_p_18_mm

- + mj=3.9500e-01 pb=7.6200e-01
- + cjsw=1.7400e-10 + dcjsw_p_18_mm mjsw=3.2400e-01
- + tnom=2.5000e+01 ute=-4.4840e-01 kt1=-2.1940e-01
  - + kt1l=-8.2040e-09 kt2=-9.4870e-03 ua1=4.5710e-09
  - + ub1=-6.0260e-18 uc1=-9.8500e-02 at=1.2030e+04
  - + prt=0.0000e+00 xti=3.0000e+00 ww=1.2360e-14
  - + lw=-2.8730e-16 ll=6.6350e-15 wl=0.0000e+00
  - +wln=1.0000e+00 wwn=1.0000e+00 wwl=0.0000e+00
  - + lln=1.0000e+00 lwn=1.0000e+00 lwl=0.0000e+00
  - + llc=-7.4500e-15 lwc=0.0000e+00 lwlc=0.0000e+00
  - + wlc=0.0000e+00 wwc=0.0000e+00 wwlc=0.0000e+00
  - + lvth0=4.4000e-03 + dlvth0_p_18_mm
  - + wvth0= - 1.4800e-02 + dwvth0_p_18_mm
  - + pvth0=3.2000e-03 + dpvth0_p_18_mm lnlx=-1.5840e-08
  - + wrdsw=1.0070e+01 weta0=0.0000e+00 wetab=0.0000e+00
  - + wpclm=0.0000e+00 wua=2.6300e-09 lua=-8.1530e-11
  - + pua=5.8550e-11 wub=0.0000e+00 lub=0.0000e+00
  - + pub=0.0000e+00 wuc=0.0000e+00 luc=0.0000e+00
  - + puc=0.0000e+00 wvoff=-9.8160e-03 lvoff=-9.8710e-04
  - + pvoff=-9.8330e-05 wa0=-4.8070e-02 la0=-2.8100e-01
  - + pa0=8.6610e-02 wags=-4.1770e-02 lags=4.4540e-02
  - + pags=-4.0760e-02 wketa=0.0000e+00 lketa=-1.2000e-02
  - + pketa=0.0000e+00 wute=-2.6820e-01 lute=0.0000e+00
  - + pute=0.0000e+00 wvsat=-1.4200e+04 lvsat=0.0000e+00
  - + pvsat= - 4.3400e+02 + dpvsat_p_18_mm lpdiblc2=3.0120e-03
  - + cjswg=4.200e-10 + dcjgate_p_18_mm wat=-6.4050e+03
  - + wprt=2.1660e+02 n=1.0000e+00 pbsw=6.6500e-01
  - + cta=1.0000e-03 ctp=7.5300e-04 pta=1.5500e-03
  - + ptp=1.2400e-03 ldif=8.0000e-08 rsh=8.0000e+00
  - + rd=0.0000e+00 rsc=0.0000e+00 rdc=0.0000e+00
  - + hdif=2.6000e-07 rs=0.0000e+00
  - + noimod=2 noia=3.57456993317604E+18 noib=2500
  - + noic=2.61260020285845E-11 ef=1.1388
  - + em=41000000

(B) MODEL PARAMETERS OF NMOS TRANSISTOR

- model n_18_mm bsim3v3 type=n
- + version=3.2000e+00 binunit=1.0000e+00 mobmod=1.0000e+00
- + capmod=2.0000e+00 nqsmod=0.0000e+00
- + tox=4.2000e-09 + dtox_n_18_mm toxm=4.2000e-09
- + xj=1.6000e-07 nch=3.7446e+17 rsh=8.0000e+00
- + ngate=1.0000e+23 vth0=3.0750e-01 + dvth0_n_18_mm
- + k1=4.5780e-01 k2=-2.6380e-02 k3=-1.0880e+01
- + k3b=2.3790e-01 w0=-8.8130e-08 nlx=4.2790e-07
- + dvt0=4.0420e-01 dvt1=3.2370e-01 dvt2=-8.6020e-01
- + dvt0w=3.8300e-01 dvt1w=6.0000e+05 dvt2w=-2.5000e-02
- + lint=1.5870e-08 wint=1.0220e-08 dwg=-3.3960e-09
- + dwb=1.3460e-09 u0=3.1410e+02 + du0_n_18_mm
- + ua=-9.2010e-10 ub=1.9070e-18 uc=4.3550e-11
- + vsat=7.1580e+04 a0=1.9300e+00 ags=5.0720e-01
- + b0=1.4860e-06 b1=9.0640e-06 keta=1.7520e-02
- + a1=0.0000e+00 a2=1.0000e+00 voff=-1.0880e-01
- + nfactor=1.0380e+00 cit=-1.5110e-03 cdsc=2.1750e-03
- + cdscd=-5.0000e-04 cdscb=8.2410e-04 eta0=1.0040e-03
- + etab=-1.4590e-03 dsub=1.5920e-03 pclm=1.0910e+00
- + pdiblc1=3.0610e-03 pdiblc2=1.0000e-06 pdiblcb=0.0000e+00
- + drout=1.5920e-03 pscbe1=4.8660e+08 pscbe2=2.8000e-07
- + pvag=-2.9580e-01 rdsw=4.9050e+00 prwg=0.0000e+00
- + prwb=0.0000e+00 wr=1.0000e+00 alpha0=0.0000e+00
- + alpha1=0.0000e+00 beta0=3.0000e+01 xpart=1.0000e+00
- + cgso=2.3500e-10 + dcgso_n_18_mm
- + cgdo=2.3500e-10 + dcgdo_n_18_mm cgbo=0.0000e+00
- + cgsl=0.0000e+00 cgdl=0.0000e+00 ckappa=6.0000e-01
- + cf=1.5330e-10 clc=1.0000e-07 cle=6.0000e-01
- + dlc=2.9000e-08 dwc=0.0000e+00 vfbcv=-1.0000e+00
- + noff=1.0000e+00 voffcv=0.0000e+00 acde=1.0000e+00
- + moin=1.5000e+01 lmin=1.8000e-07 lmax=5.0000e-05
- + wmin=2.4000e-07 wmax=1.0000e-04
- + xl= - 1.0500e-08 + dxl_n_18_mm
- + xw=0.0000e-00 + dxw_n_18_mm js=1.0000e-06
- + jsw=7.0000e-11 cj=1.0300e-03 + dcj_n_18_mm
- + mj=4.4300e-01 pb=8.1300e-01
- + cjsw=1.3400e-10 + dcjsw_n_18_mm mjsw=3.3000e-01
- + tnom=2.5000e+01 ute=-1.2860e+00 kt1=-2.2550e-01
- + kt1l=-4.1750e-09 kt2=-2.5270e-02 ua1=2.1530e-09
- + ub1=-2.6730e-18 uc1=-3.8320e-11 at=1.4490e+04

- + prt=-1.0180e+01 xti=3.0000e+00 wl=0.0000e+00
- + wln=1.0000e+00 ww=7.2620e-16 wwn=1.0000e+00
- + wwl=0.0000e+00 ll=-1.0620e-15 lln=1.0000e+00
  - + lw=2.9960e-15 lwn=1.0000e+00 lwl=0.0000e+00
  - + llc=-2.1400e-15 lwc=0.0000e+00 lwlc=0.0000e+00
  - + wlc=0.0000e+00 wwc=0.0000e+00 wwlc=0.0000e+00
  - + lvth0= - 1.0000e-03 + dlvth0_n_18_mm
  - + wvth0=6.027e-02 + dwvth0_n_18_mm pvth0=0 + dpvth0_n_18_mm
  - + lnlx=-2.8540e-08 wnlx=0.0000e+00 pnlx=0.0000e+00
  - + wua=-1.8800e-11 wu0=5.4000e-01 + dwu0_n_18_mm
  - + pub=3.8000e-20 pw0=1.3000e-09 wrdsw=0.0000e+00
  - + weta0=0.0000e+00 wetab=0.0000e+00 leta0=1.5740e-03
  - + letab=0.0000e+00 peta0=0.0000e+00 petab=0.0000e+00
  - + wpclm=0.0000e+00 wvoff=-4.0780e-04 lvoff=-4.2080e-03
  - + pvoff=-3.7880e-04 wa0=-4.7310e-02 la0=-4.6670e-01
  - + pa0=-2.6490e-02 wags=4.2420e-03 lags=3.0280e-01
  - + pags=0.0000e+00 wketa=0.0000e+00 lketa=-1.9420e-02
  - + pketa=0.0000e+00 wute=6.3730e-02 lute=0.0000e+00
  - + pute=0.0000e+00 wvsat=5.0660e+03 lvsat=0.0000e+00
  - + pvsat=0.0000e+00 + dpvsat_n_18_mm lpdiblc2=-4.7520e-03
  - + wat=7.0670e+03 wprt=0.0000e+00 ldif=8.0000e-08
  - + hdif=2.6000e-07 n=1.0000e+00 pbsw=8.8000e-01
  - + cjswg=5.0000e-10 + dcjgate_n_18_mm ctp=9.1400e-04
  - + ptp=9.2400e-04 cta=9.1900e-04 pta=1.5800e-03
  - + elm=5.0000e+00 tlevc=1.0000e+00
  - + noimod=2 noia=1.3182567385564E+19 noib=144543.977074592
  - + noic=-1.24515794572817E-12 ef=0.92
  - + em=41000000