Low-Voltage Wide Linear Range Tunable Operational Transconductance Amplifier

A dissertation submitted in partial fulfillment of the requirement for the award of degree of

Master of Technology

in

VLSI Design

Submitted by

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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **"Low-Voltage Wide Linear Range Operational Transconductance Amplifier"** in partial fulfilment of the requirement for the award of degree of Master of Engineering in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Dr. Rishikesh Pandey, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ABSTRACT

The design of tunable operational transconductance amplifier (OTA) with wide linear range has become increasingly challenging with the scaling in the power supply voltage. Tunability of OTA provides flexibility to change the range of filters as well as gain in automatic gain controllers. In recent years the use of voltage as a control parameter for tuning has become more difficult with the reduced supply voltage environment, which has result in lower noise margins and narrower linear range.

In this dissertation, bias current approach is used along with floating-gate MOSFET to develop the low-voltage tunable OTAs namely, floating-gate MOSFET tunable grounded resistor based OTA and FGMOS based wide linear range (FGWLR) OTA. The proposed circuits are simulated using TSMC 0.18μm CMOS technology process parameters and their simulation results are presented. The applications of these circuits such as grounded resistor, low-pass filter and high-pass filter are developed and the simulation results of these circuits are also discussed. The layout of the proposed FGWLR OTA is designed using Cadence® Virtuoso XL Design Environment tool.

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LIST OF SYMBOLS

g_m	Transconductance
I	Current
V	Voltage
R	Resistance
μ	Carrier Mobility
C_{oX}	Oxide Capacitance
W	Channel Width
L	Channel Length
V_T	Threshold Voltage
K	Transconductance Parameter
V_{GS}	Gate Source Voltage
V_{FG}	Floating Gate MOSFET Voltage
A_d	Differential Gain
C	Capacitance

ABBREVIATIONS

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
FGMOS	Floating-Gate MOSFET
OTA	Operational transconductance Amplifier
Op-Amp	Operational Amplifier
KCL	Kirchhoff Current Law
CMRR	Common Mode Rejection Ratio
PSRR	Power Supply Rejection Ratio
THD	Total Harmonic Distortion
LPF	Low Pass Filter
HPF	High Pass Filter
EOTA	Electronically Current-Tunable CMOS OTA
FGTGR	Floating Gate Tunable Grounded Resistor
FGWLR	Floating Gate Wide Linear Range

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With the reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage-mode circuits has greatly affected which results in a reduced dynamic range, an increased propagation delay and reduced low noise margins. However, scaling of supply voltage has lesser effect on performance of current mode circuits because their design emphasis is on branch currents rather than nodal voltages. Current mode circuits also offer advantages such as increased bandwidth, higher dynamic range, simple circuitry and lower power consumption over their voltage mode counterparts. Operational transconductance amplifier (OTA) is one such important current-mode analog building block [1]

Operational Transconductance Amplifier (OTA) is a device that translates voltage inputs to current output. It is basically a voltage controlled current source. OTA are widely used to develop floating and grounded resistors, balanced output integrators, adders, subtractors, multipliers, g_m-C active filters, automatic gain control circuits [2-4, 15-16, 25], etc. When the transconductance (g_m) of the OTA is varied then it is known as tunable OTA.

1.2 MOTIVATION

Tunable OTA is a versatile building block for continuous time analog signal processing. Tuning of transconductance (g_m) is an important requirement in many applications such as g_m-C active filters, tunable grounded resistors, automatic gain control circuits, etc. Transconductance tuning is required not only to compensate for fabrication tolerances but also to achieve programmability of relevant parameters [5]. Tuning in operational

transconductance amplifier (OTA) is achieved by either varying transconductance as function of control voltage or bias current. With recent scaling in CMOS technologies use of voltage as control parameter for tuning is becoming increasingly difficult and thus for low voltage OTA applications, tuning is often achieved using bias current as it shows better linear range at low voltages. Use of floating-gate MOSFETs (FGMOS) instead of conventional MOSFETs in tunable OTA circuits has shown better linear range and performance even at low voltages [6]. For two input floating-gate MOSFET threshold voltage is given as [7]

$$V_{Teff} = V_T - \frac{k_1}{k_2} V_b \quad (1.1)$$

where V_T is the threshold voltage, V_b is the biasing voltage, k_1 equals to C_{G1}/ C_{TOTAL} and k_2 equals to C_{G2}/ C_{TOTAL} are the capacitances between the floating-gate and control gates and C_T is the total capacitance.

From equation (1.1), it is observed that by proper selection of capacitance, threshold voltage can be reduced. Thus FGMOS can operate at power supply voltage levels that are well lower than the intended operational limits for a particular technology and consume less power [8].

The **floating-gate MOSFET** (**FGMOS**) is a type of field-effect transistor having construction similar to that of conventional MOSFET except that its gate is completely surrounded by silicon dioxide, a high quality insulator. The insulator creates a high resistance potential barrier due to which the charge contained in it remains unchanged for long periods of time. The main advantage of floating-gate MOSFET is the electrical isolation provided by the AC coupling capacitors. Floating-gate MOSFET have the ability to store an initial charge on the floating-gate, which allows fabrication imperfections to be corrected for devices that are required to be precisely matched, such as the input transistors of a differential pair or a current mirror. Floating-gate MOSFETS provides flexibility to implement both linear and non-linear functions, controllability over the threshold voltage of every single transistor and multiple inputs to achieve tunability [8]. Fig.1 shows the I-V characteristics comparison of the conventional MOSFET and FGMOS. From the Fig.1 it is clear that the Floating-gate MOSFET can operate at low voltage levels. Due to their many advantages at low voltage levels, in this work floating gate MOSFET are chosen to develop the wide linear range tunable OTAs.

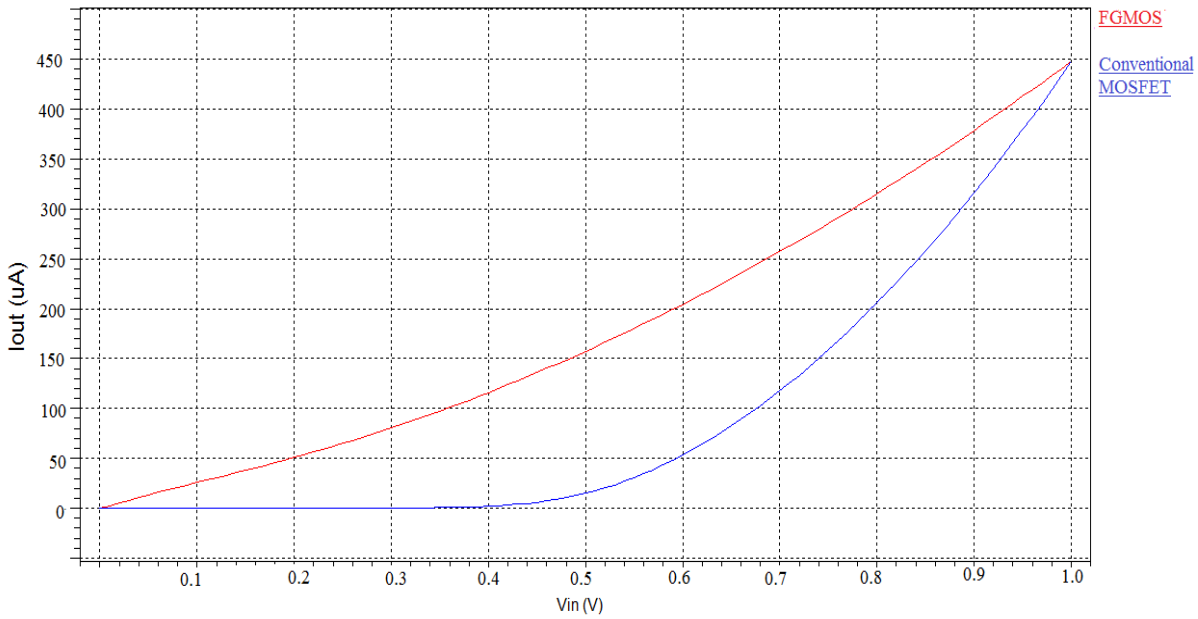

Fig.1: I-V characteristics comparison of FGMOS and conventional MOSFET

1.3 KEY CONTRIBUTIONS

The work in this dissertation can be summarized as follows.

1. Design and simulate a floating-gate MOSFET tunable grounded resistor (FGTGR) based OTA.
2. Application of FGTGR based OTA in the development of grounded resistor, low-pass filter and high-pass filter.
3. Design and simulate a FGMOS based wide linear range (FGWLR) OTA.
4. Investigating the applications of FGWLR as grounded resistor, low-pass filter and high-pass filter.

In this thesis, new tunable OTAs based on FGMOS have been proposed. These circuits find wide applications in the area of signal processing. The operational transconductance amplifiers proposed in this dissertation have been simulated using TSMC 0.18µm CMOS technology process parameters and the simulation results are presented. The performance parameters of these circuits have also been compared with the existing circuits available in literature and the comparison shows that the proposed FGWLR OTA has lower supply voltage requirement and higher linearity whereas FGTGR based OTA has higher transconductance range.

1.4 ORGANIZATION OF THE DISSERTATION

The dissertation is organized as follows

CHAPTER 1 addresses the motivation of the work and the organization of the dissertation.

CHAPTER 2 discusses the operational transconductance amplifier and its various configurations. Small signal analysis and large signal analysis of CMOS OTA are also discussed. The applications of OTA such as multiplier, grounded resistors and low-pass filter are also addressed in this chapter.

CHAPTER 3 focuses on various techniques to design tunable OTA available in the literature.

CHAPTER 4 proposes the FGTGR based OTA and FGMOS based wide linear range OTA. The applications of the proposed OTAs such as grounded resistor, low-pass filter and high-pass filter are also discussed.

CHAPTER 5 discusses the simulation results for FGTGR based OTA and FGMOS based wide linear range OTA. This chapter also presents layout design of proposed circuits.

CHAPTER 6 summarizes the dissertation and suggests future scope of the work.

CHAPTER 2

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

2.1 INTRODUCTION

This chapter gives the description of operational transconductance amplifier (OTA) and its applications. In section 2.2, OTA is discussed. Section 2.3 explains tunable OTA. Various configurations of OTA are discussed in section 2.4. Section 2.5 introduces the CMOS OTA with its large signal and small signal analysis. In section 2.6, various characteristics of OTA are discussed. Section 2.7 gives the comparison between OTA and OP-AMP. In section 2.8, applications of OTA such as grounded resistors and low-pass filter are discussed. The chapter is concluded in section 2.9.

2.2 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

Operational transconductance amplifier (OTA) is a voltage controlled current source device that translates input voltage to output current. The symbol of OTA is shown in Fig. 2.1. An ideal OTA has two voltage inputs with infinite impedance (i.e. there is no input current). The common mode input range is also infinite, while the differential signal between these two inputs is used to control an ideal current source. Therefore, an OTA is known as voltage control current source. The ideal transfer characteristic of OTA is defined as

$$I_{OUT} = g_m (V_+ - V_-) \quad (2.1)$$

or

$$I_{OUT} = g_m V_{in} \quad (2.2)$$

where g_m is the transconductance parameter and is defined as the ratio of change in output current with change in input voltage.

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \quad (2.3)$$

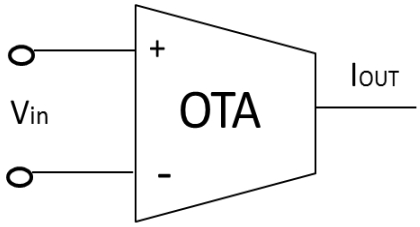

Fig. 2.1: Ideal model of OTA [1]

2.3 TUNABLE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The transconductance of the OTA can also be made to vary. If it is possible to vary the transconductance of OTA then the circuit is known as tunable OTA. Tunability provides flexibility to change the range of filters as well as gain in automatic gain controllers. Tunability in OTA can be achieved by using MOSFET operating in saturation or linear regions. The transconductance can be varied either by changing the control voltage or by changing the bias current.

The circuits which use voltage as control parameter to change the transconductance of OTA have limited range of operation at low voltage because of linearity restrictions. The transconductance of OTA can also be made to vary with bias current. The circuits which use this approach have shown better linear range and are thus preferred.

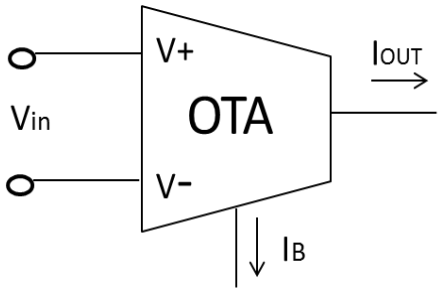

Fig. 2.2: Tunable model of OTA [1]

The tunable OTA is modelled as three input and one output terminals device as shown in Fig. 2.2. The three inputs V_+, V_- and I_B are known as input voltages applied at non-inverting terminal, inverting terminal and bias current, respectively. For linear filter applications, it is highly desirable that the transconductance (g_m) should be linearly dependent on the bias current.

2.4 VARIOUS CONFIGURATIONS OF OTA

The performance of analog circuits is often limited by second order effects that can build up and limit the circuit performance. Parasitic associated with analog circuits provide numerous paths for unwanted disturbances to couple into the signal path. The design configurations for analog circuits must be chosen in such a way that the effects of these parasitics can be limited [1]. Any analog circuit developed by using OTA can have any of the following three configurations:-

- Single ended output configuration
- Differential output configuration
- Balanced differential output configuration

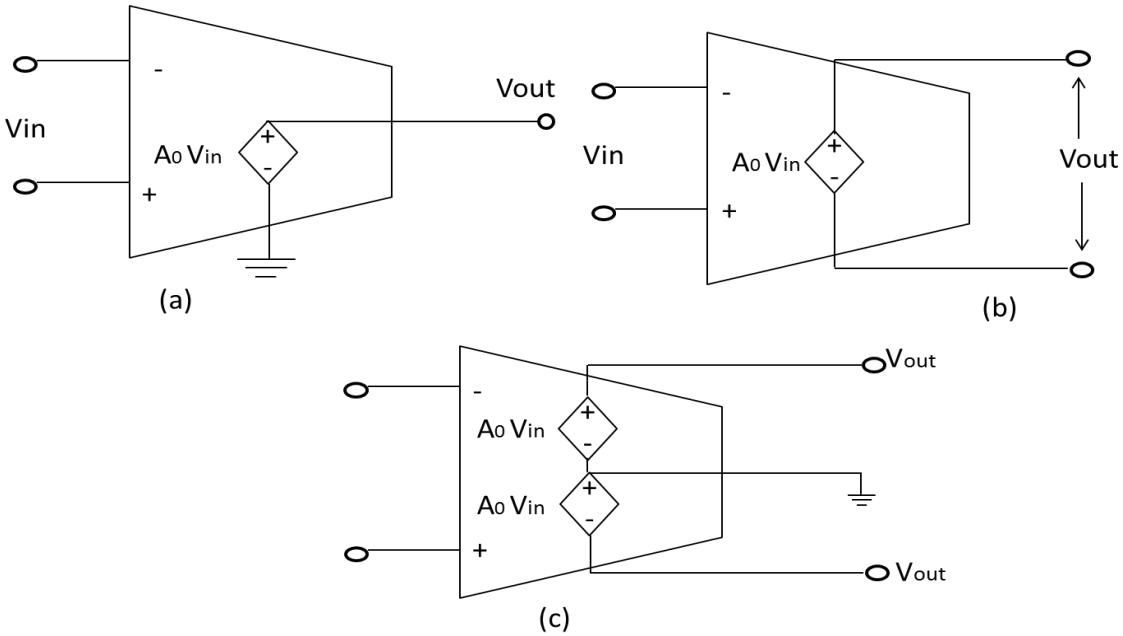

Fig. 2.3: Various configurations of OTA (a) Single ended output (b) Differential output (c) Balanced differential output [1]

Fig. 2.3 shows the various configurations of OTA. Single ended output configuration is shown in Fig. 2.3(a), in which the output is taken with respect to ground. Fig. 2.3(b) shows the differential configuration of OTA. In differential configuration, the output is defined as the difference between the two output terminal voltages. To reduce the impact of parasitic couplings, circuits are often realize as differential structures rather than single ended

schemes. Yet even further improvement is obtained if the analog circuit is not only differential but also balanced as shown in Fig. 2.3(c), in which individual differential outputs are accurately balanced and defined with respect to ground. The balanced configuration is realized with both inverting and non-inverting signal paths, which have fully symmetrical configurations such that all parasitic injection couple equally distributes on both signal paths as common-mode signals. The differential nature of these circuits causes the common mode disturbances to cancel such that their impact is reduced significantly.

2.5 CMOS OTA

The differential pair transconductor is used as basic building block to develop operational transconductance amplifier. The differential pair offers a true differential input and can achieve both positive and negative transconductance values. The inherent symmetry of the differential amplifier tends to reduce offset and drift. It also offers excellent high performance and low noise. Common mode feedback can be used for the implementation of fully balanced configuration, thus improving the dynamic range and CMRR.

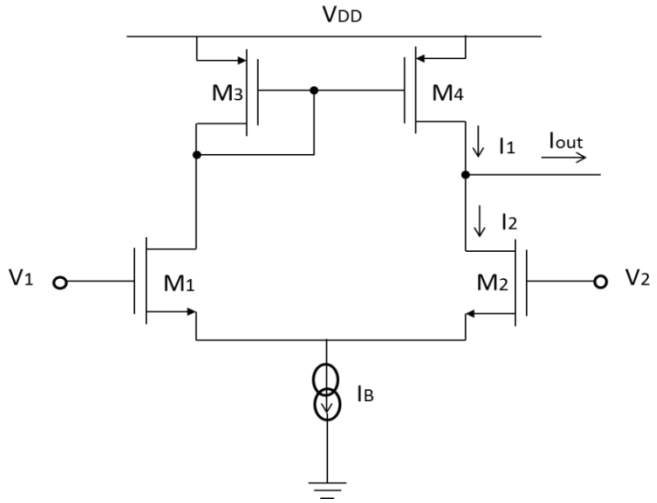

Fig. 2.4: CMOS OTA [1]

A CMOS OTA which consists of self-biasing differential pair stage with active load is shown in Fig. 2.4. M_1 and M_2 are matched NMOS pair and M_3 and M_4 are matched PMOS pair. All the current level in the circuit are determined by current source I_B, half of which flows through M_1 and M_3, with the other half flowing through M_2 and M_4, respectively.

2.5.1 LARGE SIGNAL ANALYSIS

Fig. 2.4 shows a single-output CMOS OTA, which is formed by matched MOSFET pair M_1-M_2 and M_3-M_4. All the transistors are biased in the saturation region. Using KCL at the output node, the output current (I_{out}) is given as

$$I_{OUT} = I_1 - I_2 \tag{2.4}$$

where I_1 and I_2 are the drain currents of transistors M_1 and M_2, respectively and are given as

$$I_1 = \frac{\mu C_{ox} W_1}{2L_1}(V_{GS1} - V_T)^2 \tag{2.5}$$

$$I_2 = \frac{\mu C_{ox} W_2}{2L_2}(V_{GS2} - V_T)^2 \tag{2.6}$$

where V_T is the threshold voltage, μ is the carrier mobility, C_{ox} is the channel capacitance per unit area, W_1& W_2 are the channel width and L_1&L_2 are the channel length of transistors M_1 and M_2, respectively.

From Fig. 2.4, it can be seen that the bias current (I_B) is given as

$$I_B = I_1 + I_2 \tag{2.7}$$

The input voltage (V_{in}) of the differential pair is defined as

$$V_{in} = V_{GS1} - V_{GS2} \tag{2.8}$$

The input voltages V_1 and V_2 are obtained by using equations (2.5) and (2.6) as

$$V_{GS1} = \sqrt{\frac{2I_1}{K}} + V_T \tag{2.9}$$

$$V_{GS2} = \sqrt{\frac{2I_2}{K}} + V_T \tag{2.10}$$

Using equations (2.8), (2.9) and (2.10), input voltage (V_{in}) is obtained as

$$V_{in} = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2I_2}{K}} \tag{2.11}$$

or

$$V_{in}^2 = 2\left(\frac{I_1+I_2}{K}\right) - \frac{4}{K}\sqrt{I_1 I_2} \quad (2.12)$$

Using equations (2.7) and (2.12), the input voltage (V_{in}) is given as

$$V_{in}^2 = \frac{2}{K} I_B - \frac{4}{K}\sqrt{I_1 I_2} \quad (2.13)$$

Squaring both sides of equation (2.13) and using the relation $(I_1 + I_2)^2 - (I_1 - I_2)^2 = 4I_1I_2$ and equations (2.4) and (2.7), the output current (I_{OUT}) is modified as

$$I_{OUT} = \frac{K}{2} V_{in}\sqrt{\frac{4I_B}{K} - V_{in}^2} \quad (2.14)$$

The transconductance g_m is given as

$$g_m = \frac{\partial I_{out}}{\partial V_{in}} = \frac{K}{2}\left(\frac{\frac{4I_B}{K}}{\sqrt{\frac{4I_B}{K} - V_{in}^2}}\right) \quad (2.15)$$

If $V_{in}=0$ then the equation (2.15) reduces to

$$g_m = \frac{k}{2}\left(\frac{\frac{4I_B}{K}}{\sqrt{\frac{4I_B}{K}}}\right) = \sqrt{I_B K} \quad (2.16)$$

From equation (2.16), it is observed that the transconductance (g_m) depends on square root of bias current (I_B).

2.5.2 SMALL SIGNAL ANALYSIS

The small signal model of CMOS OTA is shown in Fig. 2.5. Gain of differential pair can easily be found using small signal analysis.

Using KCL at node 'a' gives

$$g_{m3}V_{g3} + \frac{V_{g3}}{r_{03}} + \frac{g_{m1}V_{id}}{2} + \frac{V_{g3}}{r_{01}} = 0 \quad (2.17)$$

or

$$V_{g3} = -\frac{g_{m1}V_{id}}{2}\left(\frac{1}{g_{m3}} \| r_{03} \| r_{01}\right) \quad (2.18)$$

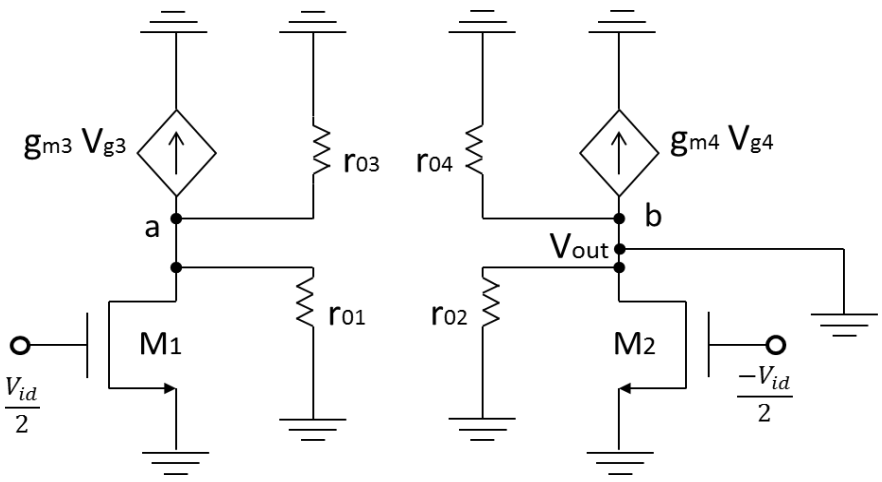

Fig. 2.5: Small signal model of CMOS OTA

If r_{01} , $r_{02} >> \frac{1}{g_{m3}}$ then equation (2.18) reduces to

$$V_{g3} \approx -\frac{g_{m1}v_{id}}{2}\left(\frac{1}{g_{m3}}\right) \tag{2.19}$$

Using KCL at node 'b' gives

$$g_{m4}\,V_{g3} + \frac{V_{out}}{r_{04}} + \frac{V_{out}}{r_{02}} - \frac{g_{m2}V_{id}}{2} = 0 \tag{2.20}$$

Using equation (2.19), equation (2.20) is modified as

$$-\frac{g_{m1}V_{id}}{2}\left(\frac{1}{g_{m3}}\right)g_{m4} + \frac{V_{out}}{r_{04}} + \frac{V_{out}}{r_{02}} - \frac{g_{m2}V_{id}}{2} = 0 \tag{2.21}$$

or

$$V_{out}\left(\frac{r_{02}+r_{04}}{r_{02}r_{04}}\right) = \frac{V_{id}}{2}\left(\frac{g_{m1}g_{m4}}{g_{m3}} + g_{m2}\right) \tag{2.22}$$

Since transistors M_3-M_4 and M_1-M_2 are perfectly matched so their transconductances are equal, the differential gain (A_d) is given as

$$A_d = \frac{V_{out}}{V_{id}} = g_m\left(\frac{r_{02}+r_{04}}{r_{02}r_{04}}\right) \tag{2.23}$$

If $r_{02} = r_{04} = r_0$, then the differential gain of CMOS OTA is given as

$$A_d = \frac{g_m}{2}r_0 \tag{2.24}$$

2.6 CHARACTERISTICS OF OTA

In this section, various parameters of OTA such as common-mode rejection ratio, total harmonic distortion, input common mode range and power supply rejection ratio are discussed.

2.6.1 INPUT COMMON MODE RANGE (V_{ICMR})

Input common mode voltage (V_{ICM}) is defined as the average voltage at the inverting and non- inverting input terminal of OTA and is described as

$$V_{ICM} = \frac{V_{in}^{+} + V_{in}^{-}}{2} \tag{2.25}$$

where V_{in}^{+} is defined as the input voltage at the non-inverting terminal of OTA and V_{in}^{-} is defined as input voltage at the inverting terminal of OTA.

The input common mode range (V_{ICMR}) defines a range of common mode input voltage that results in proper operation of the OTA and describes how close the input can get to either supply rail. If V_{ICMR} is violated than the normal linear operation of OTA is not appropriate.

2.6.2 COMMON MODE REJECTION RATIO (CMRR)

The common-mode rejection ratio (CMRR) is a measure of ability of OTA to reject the signals that appear on both input terminals. Ideally an OTA should amplify only the differential mode signal, but not any noise or common mode signal. The common-mode rejection ratio (CMRR) is defined as the ratio of the common-mode gain to differential-mode gain of an OTA. Ideally an OTA must have infinite CMRR.

$$CMRR = \left|\frac{Ad}{Acm}\right| \tag{2.26}$$

where A_d is defined as differential gain and A_{cm} is defined as common-mode gain of OTA.

2.6.3 LINEARITY

A large signal analysis of the circuit illustrates its signal handling limitation. The most common method of describing large signal performance of a circuit is by measuring its total

non- linearity. For OTA, non-linearity is defined as the percentage deviation from the ideal value of $g_m V_{id}$. Rearranging equation (2.18) gives

$$I_{OUT} = \sqrt{I_B K}\, V_{in}\sqrt{1 - \frac{kV_{in}^2}{4I_B}} \qquad \text{for } -\sqrt{\frac{I_B}{K}} \ll V_{in} \ll \sqrt{\frac{I_B}{K}} \tag{2.27}$$

From the equation (2.27), it is observed that as signal level increases, transfer function becomes non-linear and therefor harmonic distortion occurs.

2.6.4 POWER SUPPLY REJECTION RATIO (PSRR)

Power supply rejection ratio (PSRR) is defined as the ratio of change in the supply voltage to the equivalent change in the input voltage of OTA. An ideal OTA must have infinite PSRR.

$$\text{PSRR} = \frac{\Delta V_{supply}}{\Delta V_{input}} \tag{2.28}$$

where ΔV_{supply} defined as the change in supply voltage and ΔV_{input} is defined as the change in input voltage of OTA.

2.6.5 TOTAL HARMONIC DISTORTIONS (THD)

Total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

$$\text{THD} = \frac{P_2 + P_3 + P_4 + \ldots\ldots + P_\infty}{P_1} \tag{2.29}$$

where P_1 is the power of the fundamental harmonic and P_2, P_3, P_4 etc. are the power of higher harmonics.

2.7 COMPARISON BETWEEN OP-AMP AND OTA

Operational Amplifier (OP-AMP) is the fundamental building block in analog integrated circuit design. An OP-AMP is basically a three stage device. The first stage of OP-AMP is a differential amplifier. The first stage is followed by one more gain stage, such as a common source stage and finally by an output buffer. Operational transconductor amplifier is a subset of OP-AMP. The operational transconductor amplifier (OTA) is basically an OP-AMP without output buffer. An OP-AMP without output buffer can only drive capacitive load,

therefor operational transconductor amplifier are basically used to drive only capacitive load. Due to high output resistance of OTA it can be used as open-loop configuration as its high output resistance prevents the output from going into saturation even at high differential input voltages, whereas OP-AMP output enters the saturation if used as open loop configuration.

2.8 APPLICATIONS OF OTA

OTA is a versatile building block for continuous time analog signal processing. OTA are widely used to develop floating and grounded resistors, balanced output integrators, adders, subtractors, multipliers, g_m-C active filters, automatic gain controllers [2-4, 16, 27] etc. In this section, applications of OTA such as grounded resistor and low-pass filter are discussed.

2.8.1 GROUNDED RESISTOR

The grounded resistor can easily be implemented using OTA as shown in Fig. 2.6. The resistance of the grounded resistor depends on transconductance (g_m) of OTA.

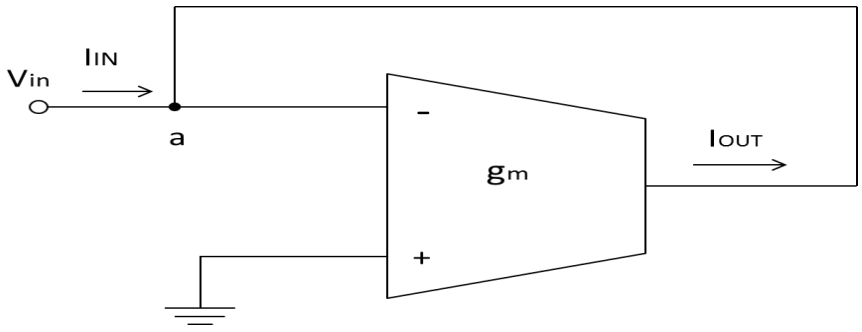

Fig. 2.6: Grounded resistor (R) [16]

Output current (I_{OUT}) is given as

$$I_{OUT} = -g_m V_{in} \tag{2.30}$$

Applying KCL at node 'a' gives

$$I_{IN} + I_{OUT} = 0 \tag{2.31}$$

$$I_{OUT} = -I_{IN} \tag{2.32}$$

Using equations (2.30) and (2.32), the resistance (R) is given as

$$R = \frac{1}{g_m} \tag{2.33}$$

From equation (2.33), it is observed that the circuit behaves like a resistor.

The same circuit of OTA can also be used to develop the negative resistor (-R) when input is applied at non-inverting terminal of OTA as shown in Fig. 2.7.

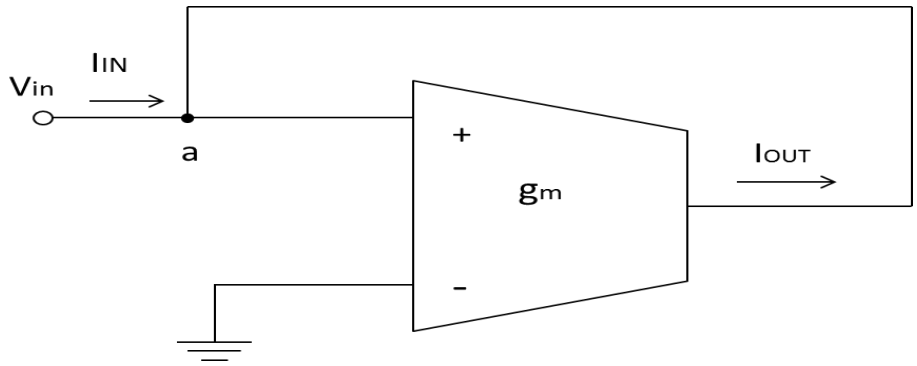

Fig. 2.7: Grounded resistor (-R) [16]

Output current (I_{OUT}) is given as

$$I_{OUT} = g_m V_{in} \tag{2.34}$$

Comparing equations (2.32) and (2.34) gives

$$R = -\frac{1}{g_m} \tag{2.35}$$

From the equation (2.35), it is observed that the circuit behaves like a negative grounded resistor.

2.8.2 LOW PASS FILTER

Low-pass filter is the main building block for most continuous-time filters. Low-pass filter developed using an OTA and a capacitor is shown in Fig. 2.8.

The output current (I_{OUT}) is given as

$$I_{OUT} = g_m V_{IN} \tag{2.36}$$

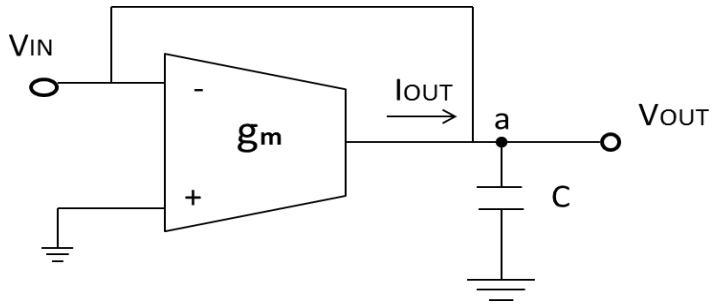

Fig. 2.8: OTA as low-pass filter

Using KCL at node 'a' gives

$$- I_{OUT} + V_{OUT}SC = 0 \tag{2.37}$$

Using equations (2.36) and (2.37), the output voltage (V_{OUT}) is given as

$$V_{OUT} = \frac{g_m V_{IN}}{SC} \tag{2.38}$$

From equation (2.38), it is observed that the circuit behaves as a low-pass filter.

2.9 CONCLUSIONS

Many analog circuits such as g_m-C filters, tunable resistors, automatic gain controllers etc., require the use of OTA whose transconductance is varied by some control parameter. Transconductance tuning is required not only to compensate for fabrication tolerances but also to achieve tunability [5]. In this chapter applications of OTA such as grounded resistor and low-pass filter have been discussed.

CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

This chapter discussed the various techniques to design tunable operational transconductance amplifiers (OTAs) available in literature. Section 3.2 explains basic concept of tuning in OTAs. In section 3.3, voltage-controlled tunable OTAs are discussed. Section 3.4 explains the current-controlled tunable OTAs. The chapter is concluded in section 3.5.

3.2 TUNING IN OTAs

Tunable OTA is a versatile building block for continuous time analog signal processing applications such as floating and grounded resistors, balanced output integrators, adders, subtractors, multipliers, g_m-C active filters, automatic gain controllers [2-4, 15-16], etc. Tunability is frequently accomplished by the use of MOSFETs functioning as source degeneration devices in the triode region [9-10], since their equivalent resistance can be freely adjusted. To improve their linearity active cascodes are used to limit the drain to source voltage difference of the input transistor. The several techniques to design linear tunable OTA based on MOSFET transistors operating in saturation region have been reported in [11, 13, 18-22]. However, most of them are operated in voltage mode and the controllable voltage range is rather limited. Another method of tuning of the transconductance (g_m) is by varying the bias current (I_{bias}) of the differential pair. In this approach the transconductance (g_m) is proportional to the square root of bias current which limits the allowable input swing. Various OTAs have been proposed in which the transconductance is linearly dependent on the bias current. With recent scaling in CMOS technologies, use of voltage as the control parameter for tuning is becoming increasingly difficult and thus for low voltage OTA, tuning is often achieved using bias current as it shows better linear range.

3.3 VOLTAGE-CONTROLLED OTA

Several researches have suggested voltage-controlled operational transconductance amplifiers [12-16]. In these circuits the MOSFETs are operated in either saturation region or triode region. The main advantage of voltage mode OTA circuits is that the operation of these circuits is quite simple.

3.3.1 LINEAR TUNABLE TRANSCONDUCTOR

S. Huang *et. al* [12] proposed tunable transconductor which is developed using a basic cell. The basic cell of the tunable transconductor is shown in Fig 3.1.

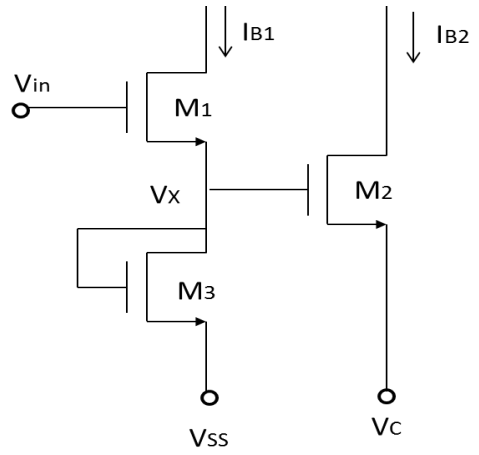

Fig. 3.1: Basic cell of the tunable transconductor

The transistors M_1, M_2 and M_3 are biased in the saturation region and are perfectly matched. The drain currents I_{B1} and I_{B2} shown in basic cell are given as

$$I_{B1} = \frac{\beta}{2}(V_{in} - V_X - V_T)^2 \tag{3.1}$$

$$I_{B2} = \frac{\beta}{2}(V_X - V_C - V_T)^2 \tag{3.2}$$

where I_{B1} & I_{B2} are the drain current of M_1 and M_2, V_T is the threshold voltage, β is the transconductance parameter, V_{in} is the input voltage of M_1, V_X is the input voltage of M_2 & M_3 and V_C is the control voltage applied to source of M_2.

Since, M_1 & M_3 are matched pair, so their gate-source voltage (V_{GS}) must be equal which gives

$$V_{in} - V_X = V_X - V_{SS} \tag{3.3}$$

or

$$2V_X = V_{in} + V_{SS} \tag{3.4}$$

Using equations (3.1), (3.2) and (3.4) the difference of drain currents I_{B1} and I_{B2} is given as

$$I_{B1} - I_{B2} = \frac{\beta}{2}(V_C - V_{SS})(V_{in} - V_C - 2V_T) \tag{3.5}$$

From the equation (3.5), it is observed that the differential current in basic cell has a linear relationship with the input voltage and control voltage. A linear transconductor can easily be implemented by cross coupling of basic cells as shown in Fig. 3.2

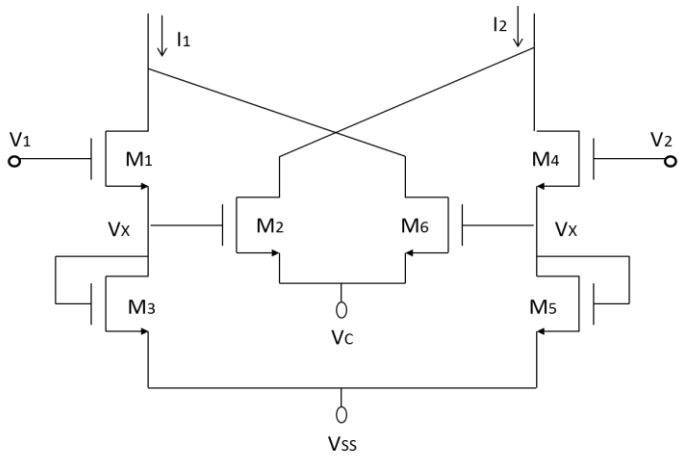

Fig. 3.2: Transconductor using two basic cell

Using equation (3.5), the differential currents (I_1-I_2) and (I_2-I_1) are given as

$$I_1 - I_2 = \frac{\beta}{2}(V_C - V_{SS})(V_1 - V_C - 2V_T) \tag{3.6}$$

$$I_2 - I_1 = \frac{\beta}{2}(V_C - V_{SS})(V_2 - V_C - 2V_T) \tag{3.7}$$

Using equations (3.6) and (3.7), the differential current (I_1-I_2) is obtained as

$$I_1 - I_2 = \frac{\beta}{4}(V_C - V_{SS})(V_1 - V_2) \tag{3.8}$$

From equation (3.8), the transconductance (g_m) is given as

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} = \frac{\beta}{4}(V_C - V_{SS}) \tag{3.9}$$

From the equation (3.9), it is observed that the transconductance (g_m) of the OTA is linearly controlled by the control voltage (V_C).

3.3.2 CROSS COUPLED TRANSCONDUCTOR

Z. Wang *et al.* [13] proposed bias offset technique to develop a tunable gain OTA. Two cross coupled differential pair biased in saturation region with unequal voltages are used to develop linear transconductor as shown in Fig.3.3. Current mirror is used to obtain single ended output.

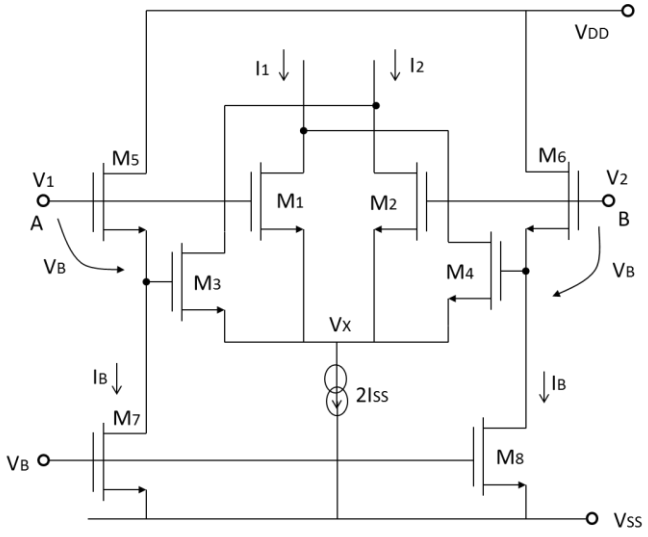

Fig. 3.3: Cross coupled transconductor

Transistors M_1, M_2, M_3 & M_4 are perfectly matched. Another set of matched transistors is formed by M_5, M_6, M_7 & M_8. M_7- M_8 are biased with control voltage V_B. Due to matching same voltage appears on transistors pair M_5-M_6 and act as a voltage shift from the inputs to the gate of M_3 and M_4. All the transistors are biased in saturation region and equation for currents I_1 and I_2 are given as

$$I_1 = I_{d1} + I_{d4} \tag{3.10}$$

$$I_2 = I_{d2} + I_{d3} \quad (3.11)$$

where I_{d1}, I_{d2}, I_{d3} and I_{d4} are drain currents of M_1, M_2, M_3 and M_4 respectively and are given as

$$I_{d1} = K(V_1 - V_X - V_T)^2 \quad (3.12)$$

$$I_{d2} = K(V_2 - V_X - V_T)^2 \quad (3.13)$$

$$I_{d3} = K(V_1 - V_B - V_X - V_T)^2 \quad (3.14)$$

$$I_{d4} = K(V_2 - V_B - V_X - V_T)^2 \quad (3.15)$$

where V_T is the threshold voltage, V_B is the control voltage, V_X is the source voltage of M_1, K is the transconductance parameter and is equal to $\frac{\mu}{2} C_{0x} \frac{W}{L}$, μ is the carrier mobility, C_{ox} is the channel capacitance per unit area, W is the channel width and L is the channel length respectively.

Using equations (3.12), (3.15) and (3.10), the current I_1 is given as

$$I_1 = K(V_1 - V_x - V_T)^2 + K(V_2 - V_B - V_x - V_T)^2 \quad (3.16)$$

Using equations (3.13), (3.14) and (3.11), the current I_2 is given as

$$I_2 = K(V_2 - V_x - V_T)^2 + K(V_1 - V_B - V_x - V_T)^2 \quad (3.17)$$

Output current (I_{OUT}) is obtained using current mirrors and is given as

$$I_{OUT} = I_1 - I_2 \quad (3.18)$$

Using equations (3.17), (3.18) and (3.19), the output current (I_{OUT}) is modified as

$$I_{OUT} = 2KV_B(V_1 - V_2) \quad (3.19)$$

From equation (3.19), the transconductance (g_m) is given as

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} = 2KV_B \quad (3.20)$$

From the equation (3.20), it is observed that the transconductance (g_m) of the OTA is linearly controlled by changing the control voltage (V_B).

3.3.3 BALANCED OUTPUT TRANSCONDUCTOR AMPLIFIER

The Balanced Transconductance Amplifier [BOTA] suggested by Mahmoud *et al.* [14] is shown in Fig. 3.4. The transistors M_1–M_8 are perfectly matched and their gate voltages are the input voltages. The remaining transistors M_9-M_{12} are used to transfer the currents to the output ports of the transconductor circuit. All the transistors M_1-M_{12} are biased in the saturation region with their sources connected to their substrate/bulk.

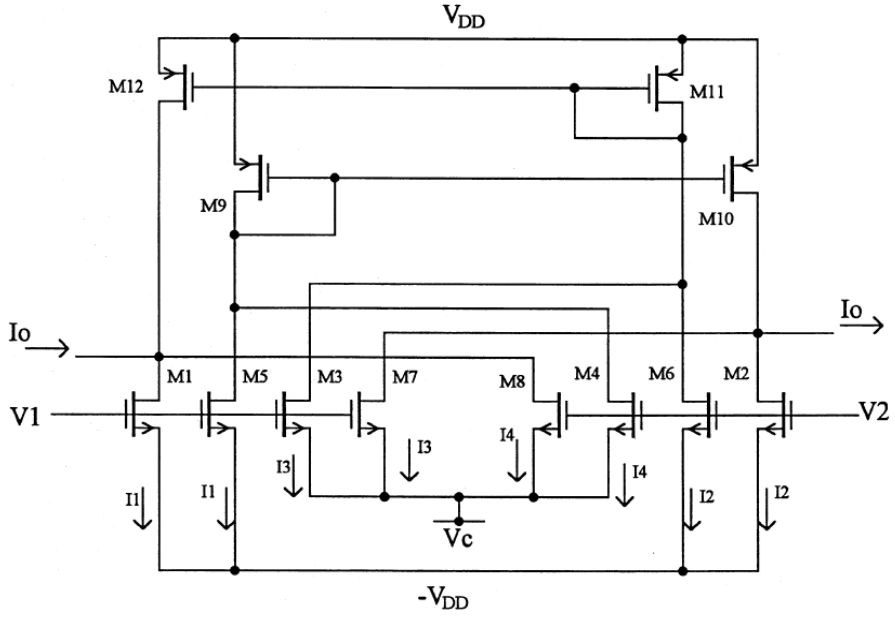

Fig. 3.4: Balanced output transconductor amplifier

From the Fig. 3.4, the output current (I_O) is given as

$$I_O = (I_1 + I_4) - (I_2 + I_3) \tag{3.21}$$

where I_1, I_2, I_3 and I_4 are the drain currents of transistors M_1-M_5, M_2-M_6, M_3-M_7 and M_8- M_4 respectively and are given as

$$I_1 = \frac{K}{2}(V_1 + V_{DD} - V_T)^2 \tag{3.22}$$

$$I_2 = \frac{K}{2}(V_2 + V_{DD} - V_T)^2 \tag{3.23}$$

$$I_3 = \frac{K}{2}(V_1 - V_C - V_T)^2 \tag{3.24}$$

$$I_4 = \frac{K}{2}(V_2 - V_C - V_T)^2 \quad (3.25)$$

where $K = \mu C_{0x} \frac{W}{L}$ is the transconductance parameter, V_T is the threshold voltage, μ is the mobility, C_{ox} is the channel capacitance per unit area, W is the channel width, L is the channel length, V_1 and V_2 are the gate voltages.

Using equations (3.22), (3.23), (3.24), (3.25) and (3.21), the output current (I_O) is modified as

$$I_O = K(V_C + V_{DD})(V_1 - V_2) \quad (3.26)$$

From equation (3.26), the transconductance (g_m) is given as

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} = K(V_C + V_{DD}) \quad (3.27)$$

From the equation (3.27), it is observed that the transconductance (g_m) of BOTA is controlled by the control voltage (V_C).

3.4 CURRENT-CONTROLLED OTA

The main disadvantage of voltage-controlled OTAs is their limited controllable voltage range. Use of DC bias current as a control parameter rather than control voltage provides tunable OTAs with wide linear range. Several researches have suggested current-controlled operational transconductance amplifiers [17-22].

3.4.1 ELECTRONICALLY CURRENT-TUNABLE CMOS OTA (EOTA)

The balanced CMOS OTA proposed by K. Kaewdang *et al.* [18] is shown in Fig. 3.5. The transistors M_1 and M_2 are perfectly matched. All the transistors M_1-M_8 are biased in the saturation region.

Using KCL at the output node, the output current (i_{out}) is given as

$$i_{out} = I_2 - I_1 \quad (3.28)$$

where I_1 and I_2 are drain currents of M_1 and M_2, respectively and are given as

$$I_1 = \frac{\mu C_{ox} W_1}{L_1}(V_{GS1-} V_T)^2 \quad (3.29)$$

$$I_2 = \frac{\mu C_{ox} W_2}{L_2}(V_{GS2-}V_T)^2 \qquad (3.30)$$

where V_T is the threshold voltage, μ is the carrier mobility, C_{ox} is the channel capacitance per unit area, W_1& W_2 are the channel width and L_1&L_2 are the channel length of M_1 and M_2, respectively.

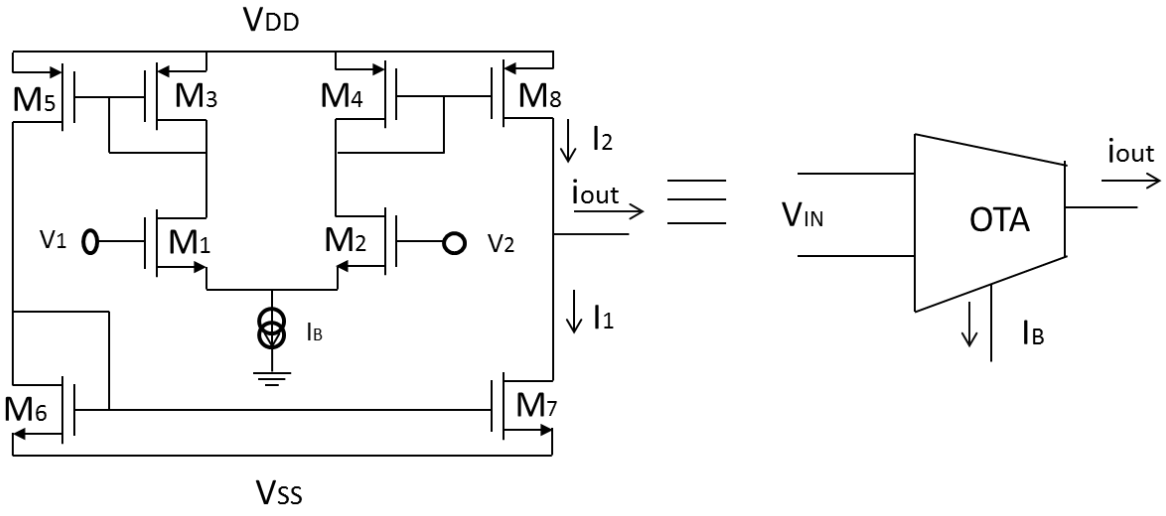

Fig. 3.5: Balanced CMOS OTA

Using equations (3.28), (3.29) and (3.30), the output current (i_{out}) is given as

$$i_{out} = \sqrt{2I_B K}\, V_{in}\sqrt{1-\frac{kV_{in}^2}{2I_B}} \qquad \text{for } -\sqrt{\frac{I_B}{K}} \ll V_{in} \ll \sqrt{\frac{I_B}{K}} \qquad (3.31)$$

From equation (3.31), the transconductance (g_m) is given as

$$g_m = \frac{\Delta I_{OUT}}{\Delta V_{IN}} = \sqrt{2I_B K} \qquad \text{for } -\sqrt{\frac{I_B}{K}} \ll V_{in} \ll \sqrt{\frac{I_B}{K}} \qquad (3.32)$$

Using equations (3.31) and (3.32), the output current (i_{out}) is given as

$$i_{out} = g_m V_{in} = \sqrt{2I_B K}\, V_{in} \qquad (3.33)$$

From equations (3.32) and (3.33), it is observed that the transconductance (g_m) and output current (i_{out}) depend on the square root of the bias current (I_B).

The balanced CMOS OTA is used as basic building block to develop the electronically current-tunable CMOS OTA (EOTA) which is shown in Fig. 3.6. In EOTA the

transconductance is directly proporttional to the bias current (I_B). The OTA_1 converts the differential input voltage into the current i_L, which flows into an active resistor R_L, developed by the OTA_2. The OTA_3 converts the voltage drop across OTA_2 into the output current (i_{out}).

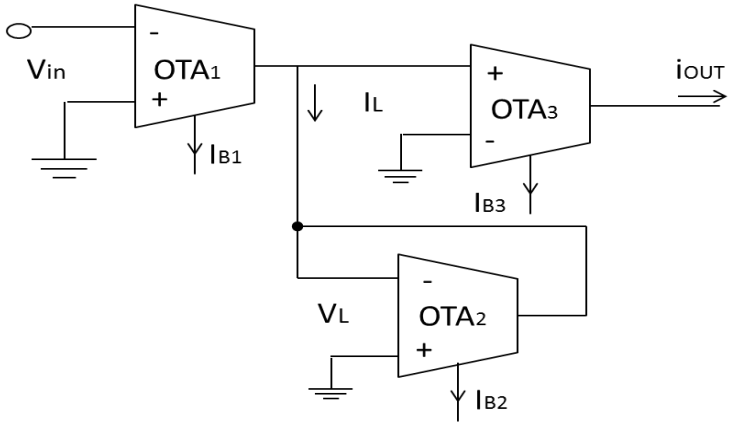

Fig. 3.6: Electronically current-tunable CMOS OTA

3.4.2 EOTA WITH ACTIVE RESISTOR

The proposed EOTA in [18] has various drawbacks and a complicated structure. The EOTA circuit is modified by replacing OTA_2 with active resistor [19] as shown in Fig. 3.7. The active resistor is formed by two NMOS and the value of resistance is equal to $\frac{1}{4}K(V_{DD} - V_T)$, where V_{DD} is the supply voltage, V_T is the threshold voltage and K is the transconductance parameter of N-MOSFET.

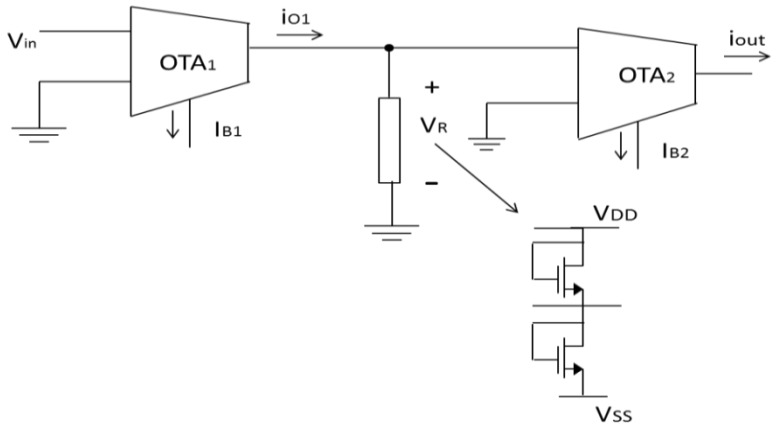

Fig. 3.7: EOTA with active resistor

3.4.3 WIDE LINEAR RANGE BALANCED CMOS OTA

K. Kaewdang *et al.* [21] suggested a balanced output transconductance amplifier shown in Fig. 3.8 accepts two input voltages and provides balanced output currents. In this circuit, the fixed gain differential transconductor is followed by variable current gain cell. The current gain cell is modified from a current-mode translinear circuit. Variable current gain cell basically consists of current mirror circuits. The current at port I_1 and I_2 are multiplied 'n' times by the current mirror arrangement to produce differential output currents i_{out}^{+} and i_{out}^{-} at the ports A1 and A2, respectively.

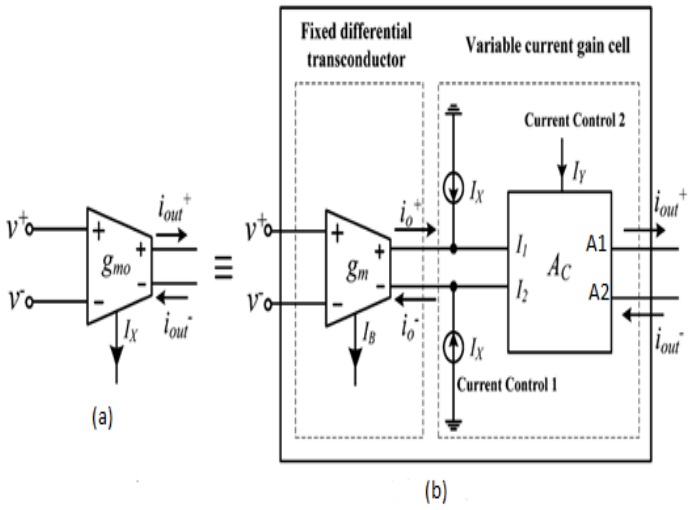

Fig.3.8: Balanced output transconductance amplifier (a) Symbol (b) Building block [21]

3.4.4 PSEUDO-DIFFERENTIAL OTA

J. Wei *et. al.* [22] presented the pseudo-differential configuration circuit for the V-I conversion. The main difference between the pseudo–differential and fully differential configuration is that the negative input is used as a reference only. Negative input is not intended to carry signal of interest. The circuit consists of the fully balanced pseudo-differential transconductor cascaded with the programmable gain current amplifier. Programmable gain cell basically consist of network of current mirrors.

3.4.5 DIGITALLY CONTROLLED OTA

Li *et al.* [23] have proposed digitally controlled OTA in which the gain of OTA is digitally as well as linearly controlled. The tunable OTA is realized using a class AB current mirror, a current division network and two fully balanced differential transconductors. The first differential transconductor is developed using P-MOSFET differential pair and the other by N-MOSFET differential pair. Biasing current is used to change the g_m of the OTA which is provided by the output of class AB current mirror.

3.5 CONCLUSIONS

In this chapter various methods to develop voltage controlled OTA and current controlled OTAs available in literature are discussed. With reduction in power supply-voltage the design of both current-controlled OTA and voltage-controlled OTA with wide linear range has become challenging. One solution of this problem is to design the circuit using low-voltage technique such as floating-gate MOSFETs instead of conventional MOSFETs. Use of floating-gate MOSFET increases the linear range of the OTAs as no part of the supply voltage is used in overcoming the threshold voltage as floating-gate MOSFET can turns on at almost zero voltage by appropriate selection of the input capacitances.

CHAPTER 4

WIDE LINEAR RANGE OTA USING FGMOS

4.1 INTRODUCTION

This chapter proposes new low-voltage tunable operational transconductance amplifiers namely floating-gate MOSFET tunable grounded resistor (FGTGR) based OTA and FGMOS based wide linear range OTA. In section 4.2, FGTGR based OTA is proposed. In section 4.3, applications of FGTGR based OTA such as grounded resistor, low-pass filter and high-pass filter are addressed. Section 4.4 presents FGMOS based wide linear range (FGWLR) OTA. In section 4.5, the applications of FGWLR OTA such as grounded resistor, low-pass filter and high-pass filter are presented. The chapter is cocluded in section 4.6.

4.2 PROPOSED FLOATING-GATE MOSFET TUNABLE GROUNDED RESISTOR BASED OTA

The proposed floating-gate MOSFET tunable grounded resistor (FGTGR) based OTA shown in Fig. 4.1 has been developed using balanced CMOS OTA [18] and a FGTGR [24]. The OTA_1 converts differential input voltage into a current i_{o1}, which flows into the FGTGR. The second OTA (OTA_2) converts the voltage drop (V_R) across FGTGR into the output current (i_{OUT}).

The transistors M_1-M_8 are biased in the saturation region. The transistors M_1 and M_2 are perfectly matched. Using KCL at the output node of OTA_1, the output current (i_{O1}) is given as

$$i_{O1} = I_2 - I_1 \tag{4.1}$$

where I_1 and I_2 are the drain currents of transistors M_1 and M_2, respectively and are given as

$$I_1 = \frac{\mu C_{ox} W_1}{2L_1}(V_{GS1-}V_T)^2 \quad (4.2)$$

$$I_2 = \frac{\mu C_{ox} W_2}{2L_2}(V_{GS2-}V_T)^2 \quad (4.3)$$

where V_T is the threshold voltage, μ is the carrier mobility, C_{ox} is the channel capacitance per unit area, W_1& W_2 are the channel width and L_1&L_2 are the channel length of M_1 and M_2 respectively.

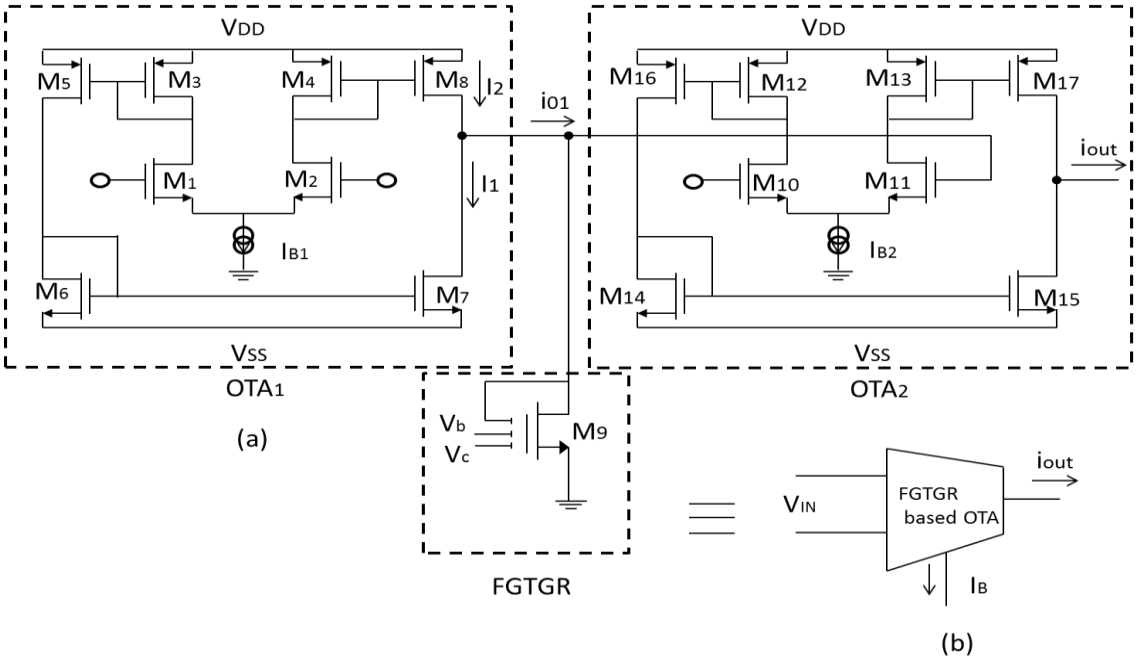

Fig. 4.1: FGTGR based OTA **(a)** Schematic diagram **(b)** Symbol

Using equations (4.1), (4.2) and (4.3), the output current (i_{O1}) of OTA_1 is given as

$$i_{O1} = \sqrt{2I_{B1}K}\, V_{in}\sqrt{1-\frac{kV_{in}^2}{2I_{B1}}} \qquad \text{for } -\sqrt{\frac{I_{B1}}{K}} \ll V_{in} \ll \sqrt{\frac{I_{B1}}{K}} \quad (4.4)$$

The transconductance (g_{m1}) of OTA_1 is given as

$$g_{m1} = \frac{dI_{out}}{dV_{in}} = \sqrt{2I_{B1}K} \qquad \text{for } -\sqrt{\frac{I_{B1}}{K}} \ll V_{in} \ll \sqrt{\frac{I_{B1}}{K}} \quad (4.5)$$

Using equations (4.4) and (4.5), the output current (i_{O1}) of OTA_1 is modified as

$$i_{O1} = g_{m1}V_{in} = \sqrt{2I_{B1}K}\, V_{in} \quad (4.6)$$

From equations (4.5) and (4.6), it is observed that the transconductance (g_{m1}) and output current (i_{O1}) of OTA_1 both depend on square root of the DC bias current (I_{B1}).

The FGTGR suggested in [24] has been developed using a FGMOS transistor M_9 biased in the triode region. The drain current of M_9 is given as

$$I_{D9} = K_n((V_{FG} - V_T)V_{DS} - \frac{V_{DS}^2}{2}) \tag{4.7}$$

Floating gate voltage V_{FG} is given as

$$V_{FG} = k_1V_C + k_2V_b + k_3V_{in} \tag{4.8}$$

where $k_1 = C_1/C_T$ and $k_2 = C_2/C_T$, $k_3 = C_3/C_T$ are the capacitive coupling ratios, C_1, C_2 and C_3 are the capacitances between floating-gate and control gate, C_T is the total capacitance ($C_T=C_1+C_2+C_3$), V_C is the control voltage, V_b is the bias voltage and V_{in} is the input voltage.

Using equation (4.8) and by proper selection of capacitive coupling ratio, the drain current of M_9 is modified as

$$I_{D9} = K_n(k_1V_C + k_2V_b - V_T)V_{DS} \tag{4.9}$$

From equation (4.9), the resistance of FGTGR is given as

$$R = \frac{V_{DS}}{I_{D9}} = \frac{1}{K_n(k_1V_C+k_2V_b-V_T)} \tag{4.10}$$

The voltage drop (V_R) across the FGTGR is given as

$$V_R = i_{o1}R \tag{4.11}$$

Using equations (4.6) and (4.11) the voltage drop (V_R) across FGTGR is modified as

$$V_R = g_{m1}V_{in}R \tag{4.12}$$

where $g_{m1} = \sqrt{2I_{B1}K}$ is the transconductance of OTA_1.

The OTA_2 convert the voltage drop V_R into output current (i_{out}) given as

$$i_{out} = g_{m2}V_R \tag{4.13}$$

Using equations (4.12) and (4.13), the output current (i_{out}) is given as

$$i_{out} = g_{mT} V_{in} \tag{4.14}$$

where $g_{mT} = g_{m1} g_{m2} R$ is the total transconductance of the circuit.

The proposed FGTGR based OTA has a advantage that its transconductance (g_m) is linearly tuned either by varying the bias current (I_B) or variable resistance of the FGTGR.

4.3 APPLICATIONS OF FGTGR BASED OTA

The applications of FGTGR based OTA such as grounded resistor, low-pass filter and high-pass filter are proposed in this section.

4.3.1 GROUNDED RESISTOR USING FGTGR BASED OTA

The proposed FGTGR based OTA is used to develop grounded resistor as shown in Fig 4.2. The resistance of the grounded resistor can be varied by changing the bias current (I_B).

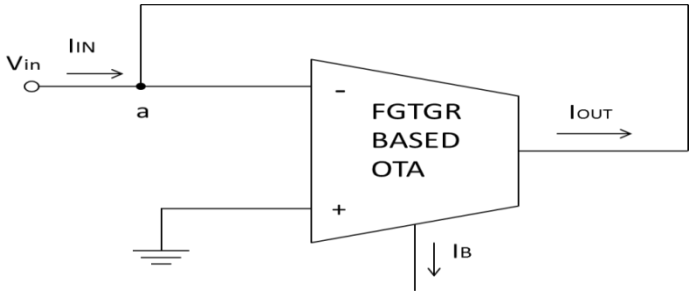

Fig. 4.2: Proposed grounded resistor (R) based on FGTGR based OTA

The FGTGR based OTA can also be used to develop the negative resistor (-R) when input is applied at non-inverting terminal of OTA as shown in Fig. 4.3.

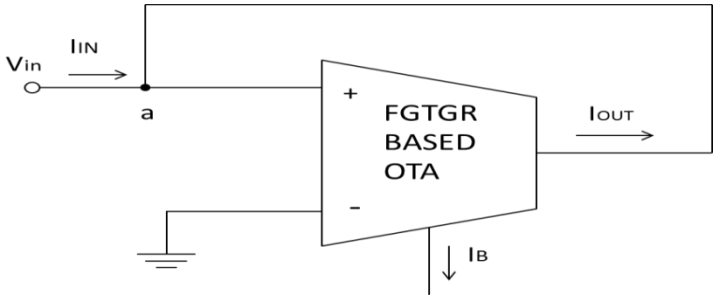

Fig. 4.3: Proposed grounded resistor (-R) based on FGTGR based OTA

4.3.2 FGTGR OTA BASED LOW-PASS FILTER

Low-pass filter (LPF) developed using the FGTGR based OTA is shown in Fig. 4.4. The cut-off frequencies of the low-pass filter can be varied either by changing the bias current (I_B) or variable resistance of the FGTGR.

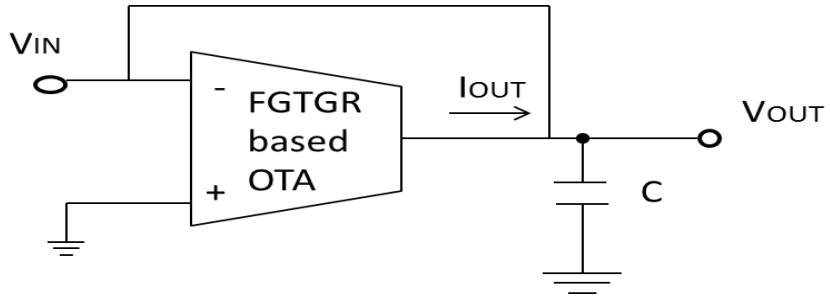

Fig. 4.4: Proposed low-pass filter based on FGTGR based OTA

4.3.3 HIGH PASS FILTER USING FGTGR BASED OTA

High-pass filter developed using the proposed FGTGR based OTA is shown in Fig. 4.5. The cut-off frequencies of the high-pass filter can be varied either by changing the bias current (I_B) or variable resistance of the FGTGR.

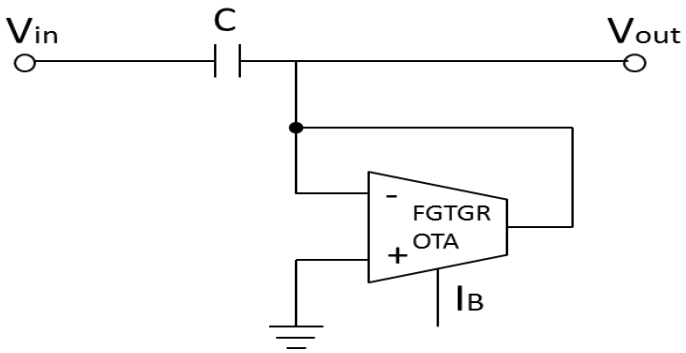

Fig. 4.5: Proposed high-pass filter based on FGTGR based OTA

4.4 PROPOSED FGMOS BASED WIDE LINEAR RANGE OTA

The FGTGR based OTA circuit proposed in Fig. 4.1 has a drawback that its linear range is limited. The linear range can be improved by using floating-gate MOSFET instead of conventional MOSFET in differential pair of balanced CMOS OTA. The schematic diagram

of the proposed FGMOS based wide linear range (FGWLR) OTA is shown in Fig. 4.6. The circuit has been developed using two FGMOS based balanced OTAs and one FGTGR.

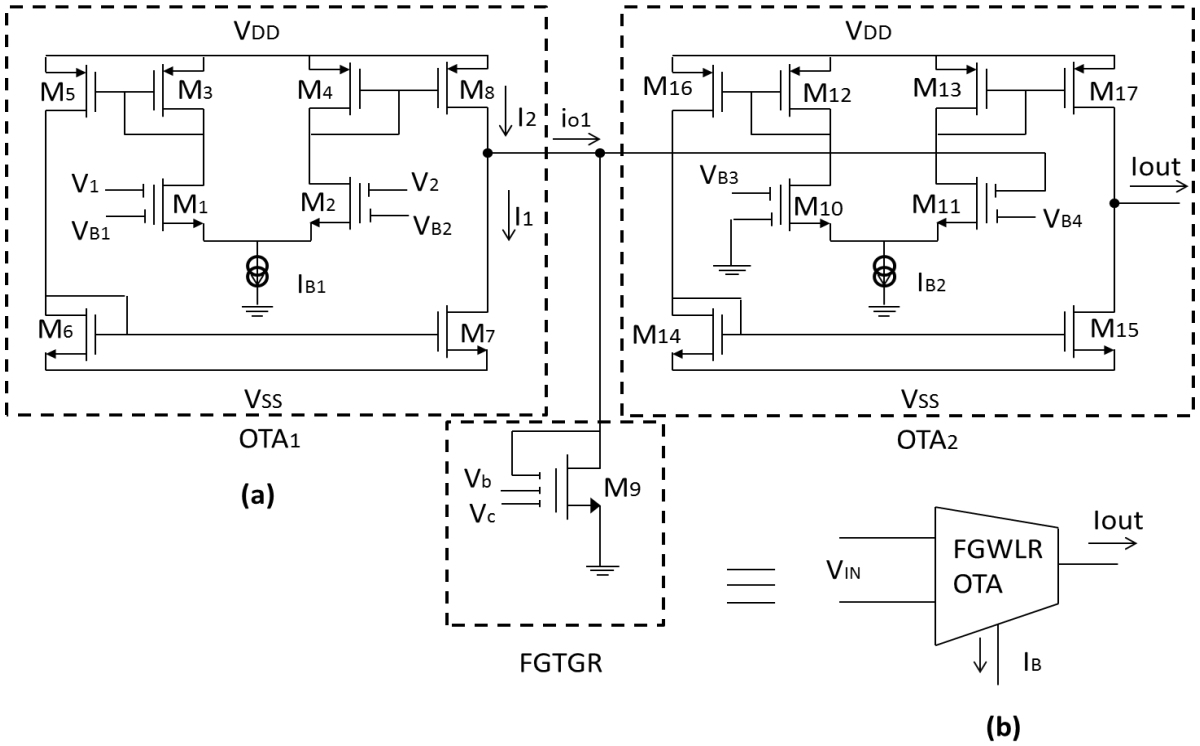

Fig. 4.6: FGMOS based wide linear range OTA **(a)** Schematic diagram **(b)** Symbol

The FGMOS based balanced OTA is shown in Fig. 4.7. The transistors M_1-M_2 of FGMOS based balanced OTA are two-input terminal floating-gate MOSFET. One input terminal is used to apply input signal voltage (V_1 or V_2) and other is used for applying biasing voltage (V_{B1} or V_{B2}) to reduce the threshold voltage.

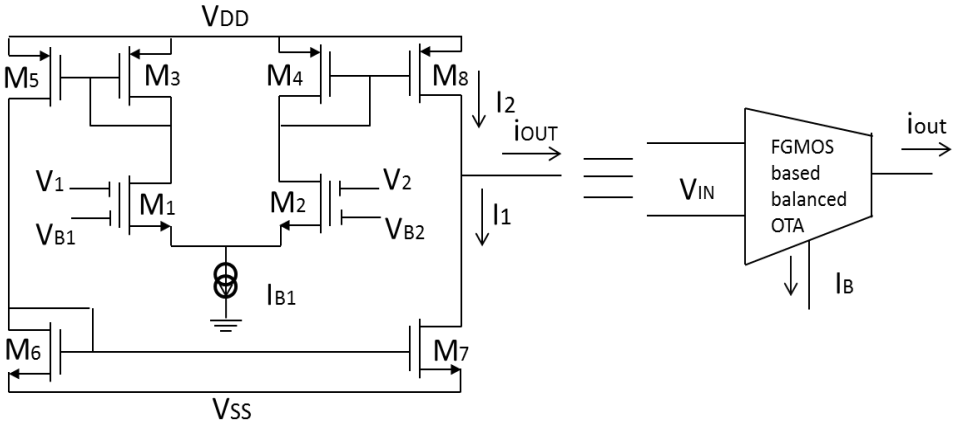

Fig. 4.7: FGMOS based balanced OTA

All the transistors M_1-M_8 are biased in the saturation region. The transistors M_1 and M_2 are perfectly matched. Using KCL at the output node, the output current (i_{out}) is given as

$$i_{out} = I_2 - I_1 \tag{4.15}$$

where I_1 and I_2 are the drain currents of floating-gate transistors M_1 and M_2, respectively and are given as

$$I_1 = \frac{\mu C_{ox} W_1}{2L_1}(V_{FG} - V_{SS} - V_T)^2 \tag{4.16}$$

$$I_2 = \frac{\mu C_{ox} W_2}{2L_2}(V_{FG} - V_{SS} - V_T)^2 \tag{4.17}$$

where V_{FG} is the floating gate voltage (V_{FG}), V_T is the threshold voltage, μ is the carrier mobility, C_{ox} is the channel capacitance per unit area, W_1& W_2 are the channel width and L_1&L_2 are the channel length of M_1 and M_2, respectively.

The floating gate voltage (V_{FG}) is expressed as

$$V_{FG} = (\sum_{i=1}^{N} C_i V_i + C_{fd} V_{DS} + C_{fs} V_{SS} + C_{fb} V_{BS} + Q_{FG}) / C_T \tag{4.18}$$

where $\sum_{i=1}^{N} C_i$ is the sum of N-input capacitances, C_{fd} is the overlap capacitance between floating-gate and drain, C_{fs} is the overlap capacitance between floating-gate and source, C_{fb} is the parasitic capacitance between floating gate and substrate, V_i is the applied input voltage at ith input gate, V_{DS} is the drain-to-source voltage, V_{BS} is the substrate-to-source voltage, and Q_{FG} is the residual charge

Ignoring the overlap capacitances and Q_{FG}, floating-gate voltage (V_{FG}) reduces to

$$V_{FG} = (\sum_{i=1}^{N} C_i V_i) / C_T \tag{4.19}$$

Using equations (4.15), (4.16) and (4.17), the output current (i_{out}) is given as

$$i_{out} = \sqrt{2 I_B K}\ V_{in}\sqrt{1 - \frac{k V_{in}^2}{2 I_B}} \qquad \text{for } -\sqrt{\frac{I_B}{K}} \ll V_{in} \ll \sqrt{\frac{I_B}{K}} \tag{4.20}$$

where V_{in} is equal to (V_{FG1}- V_{FG2}) and V_{FG1} & V_{FG2} are the input voltages at the gate of M_1-M_2, respectively.

The transconductance (g_m) is given as

$$g_m = \frac{dI_{out}}{dV_{in}} = \sqrt{2I_{B1}K} \qquad \text{for} \quad -\sqrt{\frac{I_{B1}}{K}} \ll V_{in} \ll \sqrt{\frac{I_{B1}}{K}} \tag{4.21}$$

Using equations (4.20) and (4.21), the output current is obtained as

$$i_{out} = g_m V_{in} = \sqrt{2I_B K}\, V_{in} \tag{4.21}$$

From equations (4.20) and (4.21), it is observed that transconductance (g_m) and output current (i_{out}) depend on square root of the bias current (I_B).

The OTA_1 (FGMOS based balanced OTA) converts the differential input voltage into the current i_{O1}, which flows into the FGTGR. The OTA_2 (FGMOS based balanced OTA) converts the voltage drop (V_R) across FGTGR into the output current (i_{OUT}).

From equation (4.14), the output current (i_{out}) of FGWLR OTA is given as

$$i_{out} = g_{mT} V_{in} \tag{4.22}$$

where $g_{mT} = g_{m1} g_{m2} R$ is the total transconductance of the circuit.

The proposed FGMOS based wide linear range OTA has a advantage that its transconductance (g_m) is tuned either by varying the bias current (I_B) or variable resistance of the FGTGR.

4.5 APPLICATIONS OF FGMOS BASED WIDE LINEAR RANGE OTA

In this section applications of FGMOS based wide linear range (FGWLR) OTA such as grounded resistor, low-pass filter and high-pass filter are proposed.

4.5.1 FGWLR OTA BASED GROUNDED RESISTOR

The proposed FGMOS based wide linear range OTA is used to develop grounded resistor as shown in Fig 4.8. The resistance of the grounded resistor can be varied by changing the bias current (I_B).

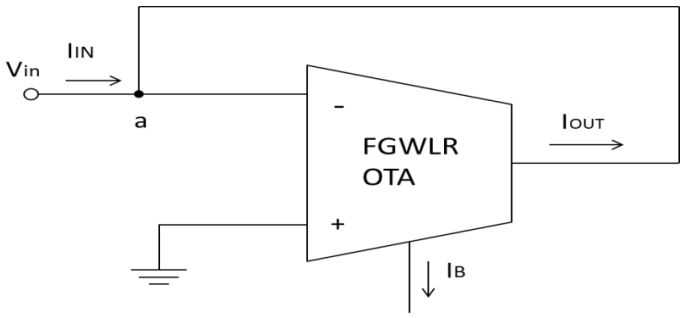

Fig. 4.8: Proposed FGWLR OTA based grounded resistor (R)

The FGWLR based OTA can also be used to develop the negative resistor (-R) when input is applied at non-inverting terminal of OTA as shown in Fig. 4.9.

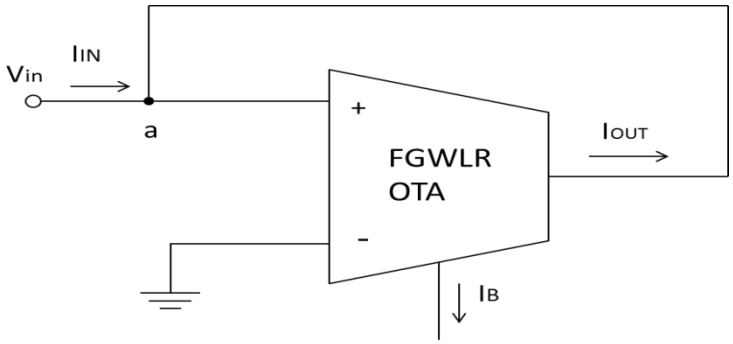

Fig. 4.9: Proposed FGWLR OTA based grounded resistor (-R)

4.5.2 LOW PASS FILTER USING FGWLR OTA

Low-pass filter (LPF) developed using FGWLR OTA is shown in Fig. 4.10. The cut-off frequencies of the low-pass filter can be varied either by changing the DC bias current(I_B) or variable resistance of the FGTGR.

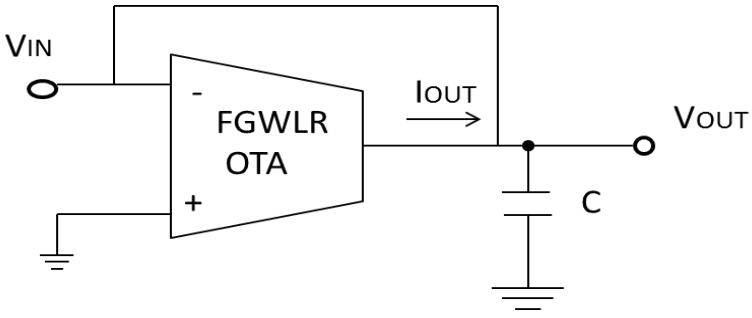

Fig. 4.10: Proposed FGWLR OTA based low-pass filter

4.5.3 HIGH PASS FILTER USING FGWLR OTA

High-pass filter developed using FGMOS based wide linear range OTA is shown in Fig. 4.11. The cut-off frequencies of the high-pass filter can be varied either by changing the DC bias current(I_B) or variable resistance of the FGTGR.

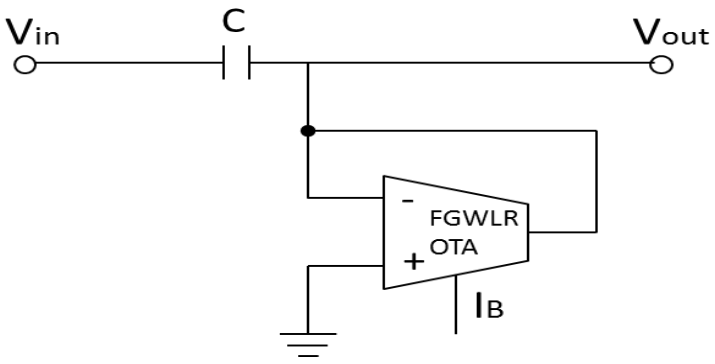

Fig. 4.11: Proposed FGWLR OTA based high-pass filter

4.6 CONCLUSIONS

In this chapter FGTGR based OTA and wide linear range FGMOS based OTA are proposed. The proposed OTA circuits are also used to develop grounded resistor, low-pass filter and high-pass filter.

CHAPTER 5

SIMULATION RESULTS & LAYOUT

5.1 INTRODUCTION

The proposed circuits, FGTGR based OTA and FGMOS based wide linear range OTA have been simulated using TSMC 0.18μm CMOS technology process parameters. The chapter is organized as follows. Section 5.2 presents the simulation results of FGTGR based OTA and its applications such as grounded resistor, low-pass filter and high-pass filter. In section 5.3, the simulation results of wide linear range FGMOS based OTA and its applications such as grounded resistor, low-pass filter and high-pass filter are discussed. Section 5.4 addresses the layout of FGMOS based wide linear range OTA designed using UMC 0.18μm CMOS process technology. The chapter is concluded in section 5.5

5.2 SIMULATION RESULTS OF FGTGR BASED OTA

The FGTGR based OTA shown in Fig. 4.1 has been simulated using TSMC 0.18 μm CMOS technology. The circuit is operated at the supply voltages of ± 0.5V. The dimension of the transistors of proposed circuit is listed in table I.

Table I: Transistors sizing of FGTGR based OTA

MOSFETS	W(μm)	L(μm)
M_1-M_2, M_{10}-M_{11}	2.5	0.5
M_3-M_8, M_{12}-M_{17}	22	0.5
M_9	20.84	0.5

The DC characteristics of the proposed FGTGR based OTA is shown in Fig. 5.1. The plot is drawn between output current (I_{OUT}) and the input voltage (V_{in}) for the different DC bias currents (I_B), which show that the proposed FGTGR based OTA converts input voltage into

output current. From the Fig. 5.1 it can be seen that the FGTGR based OTA shows linear range from -150mV to 150mV.

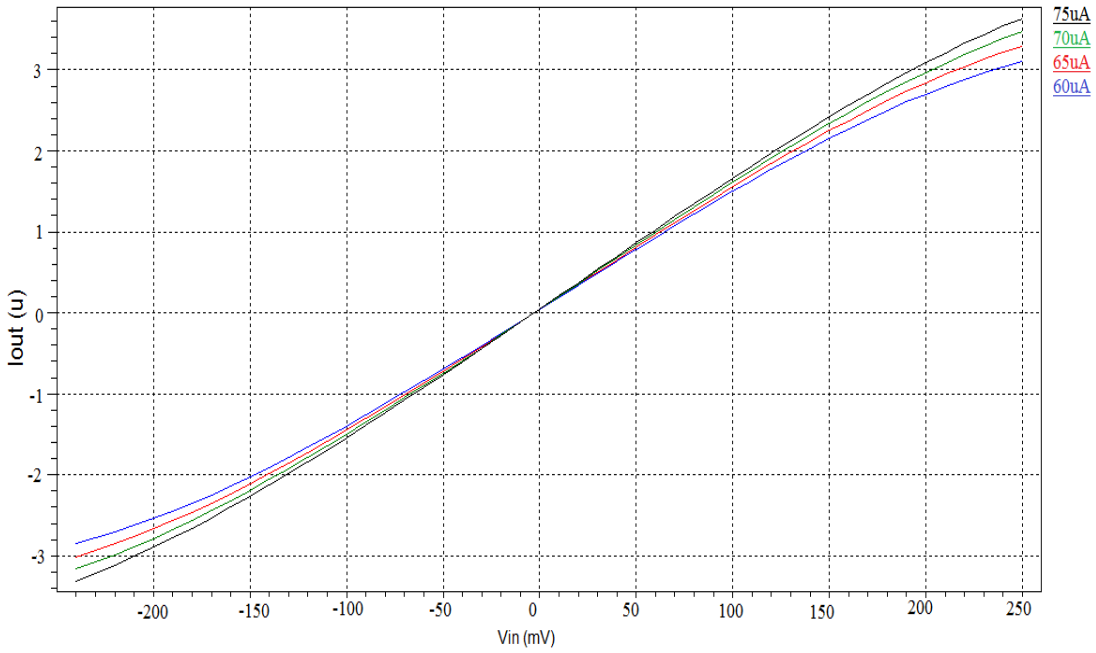

Fig. 5.1: DC Characteristics of the FGTGR based OTA

The variation of output current (I_{OUT}) of FGTGR based OTA with the bias currents (I_B) is listed in table II. From the table II, it is observed that the output current (I_{OUT}) is directly proportional to the DC bias current (I_B).

Table II: Variation of output current (I_{OUT}) with DC bias current (I_B)

I_{OUT}				
Vin(V)	I_B=60 µA	I_B=65 µA	I_B=70 µA	I_B=75 µA
-0.25	-2.96×10^{-6}	-3.08×10^{-6}	-3.39×10^{-6}	-3.39×10^{-6}
-0.15	-2.02×10^{-6}	-2.10×10^{-6}	-2.19×10^{-6}	-2.26×10^{-6}
-0.05	-6.97×10^{-7}	-7.21×10^{-7}	-7.43×10^{-7}	-7.64×10^{-7}
0.05	7.79×10^{-7}	8.09×10^{-7}	8.37×10^{-7}	8.63×10^{-7}
0.15	2.15×10^{-6}	2.24×10^{-6}	2.33×10^{-6}	2.41×10^{-6}
0.25	3.10×10^{-6}	3.29×10^{-6}	3.46×10^{-6}	3.63×10^{-6}

The frequency response of the proposed FGTGR based OTA is shown in Fig. 5.2. From the Fig. 5.2, it is observed that -3dB frequency of the circuit is 120 MHz.

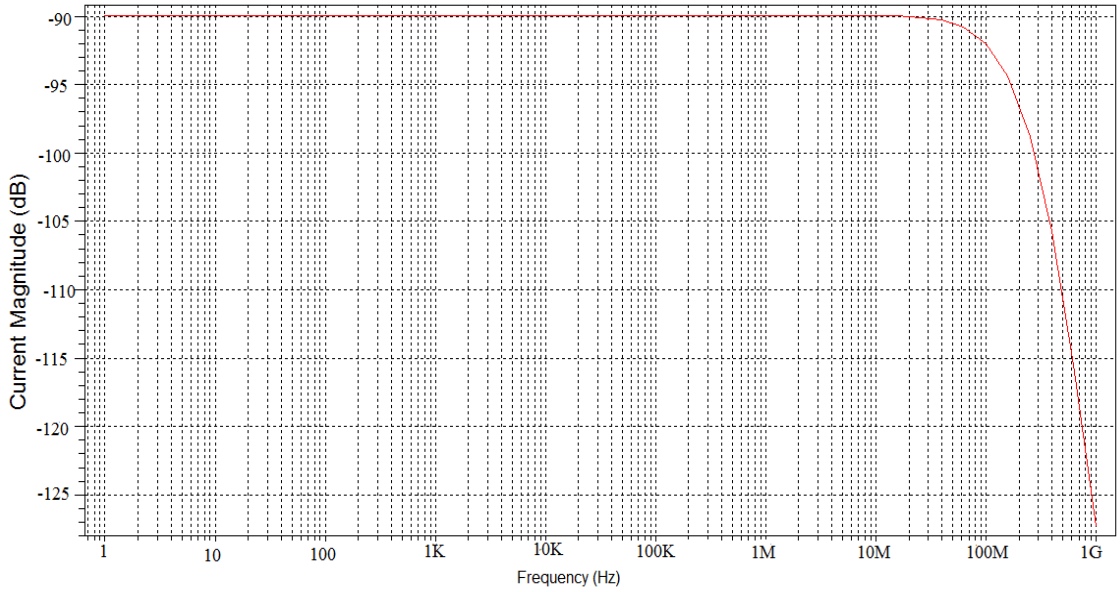

Fig. 5.2: Frequency response of the FGTGR based OTA

The variation of transconductance (g_m) of the FGTGR based OTA with the DC bias current (I_B) is shown in Fig. 5.3. The plot is obtained by varying the DC bias current (I_B) from 40 µA to 140 µA.

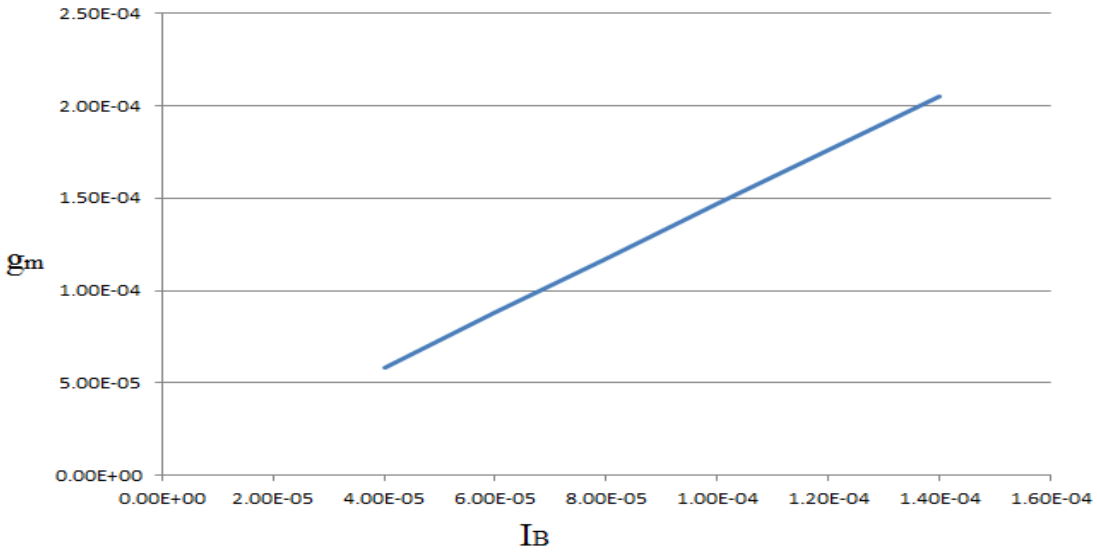

Fig. 5.3: Variation of transconductance (g_m) with DC bias current (I_B)

Table III compares the proposed FGTGR based OTA with different OTAs available in the literature [16, 18, 19, 20, 22, 25]. From the table III, it can be seen that the proposed FGTGR based OTA has lower supply voltage requirement and higher transconductance range.

Table III: Comparison of FGTGR based OTA with previous circuits

	FGTGR based OTA	[16]	[18]	[19]	[20]	[22]	[25]
CMOS Tech.	0.18 µm	0.18 µm	1 µm	1 µm	0.5 µm	0.18 µm	0.35 µm
V_{DD}(V)	1	1.5	5	5	3.3	1.8	1.8
Tunability	Current-Voltage	voltage	Current	Current	Current	Current	Voltage
g_m(µA/V)	73-733	120-287	0-539	102.4	50-200	3.36-452	45-406
Basic Cell	Balanced CMOS OTA	Cross coupled pair	Balanced CMOS OTA	Balanced CMOS OTA	Flipped voltage follower	Pseudo differential pair	Self-Cascode pair
Operating Region	Saturation Region	Saturation Region	Saturation Region	Saturation Region	Triode Region	Saturation Region	Triode Region
-3 dB BW	120 MHz	50 MHz	120 MHz	47 MHz	NA	680 MHz	78 MHz
Linear range	30% of V_{in}	NA	25% of V_{in}	44% of V_{in}	NA	22% of V_{in}	NA

5.2.1 SIMULATION RESULTS OF FGTGR BASED OTA GROUNDED RESISTOR

Fig. 5.4 shows the I-V characteristics of the grounded resistor (R) developed using proposed FGTGR based OTA shown in Fig. 4.2. From the Fig. 5.4 it can be seen that the grounded resistor shows linear range from -250mV to 250mV.

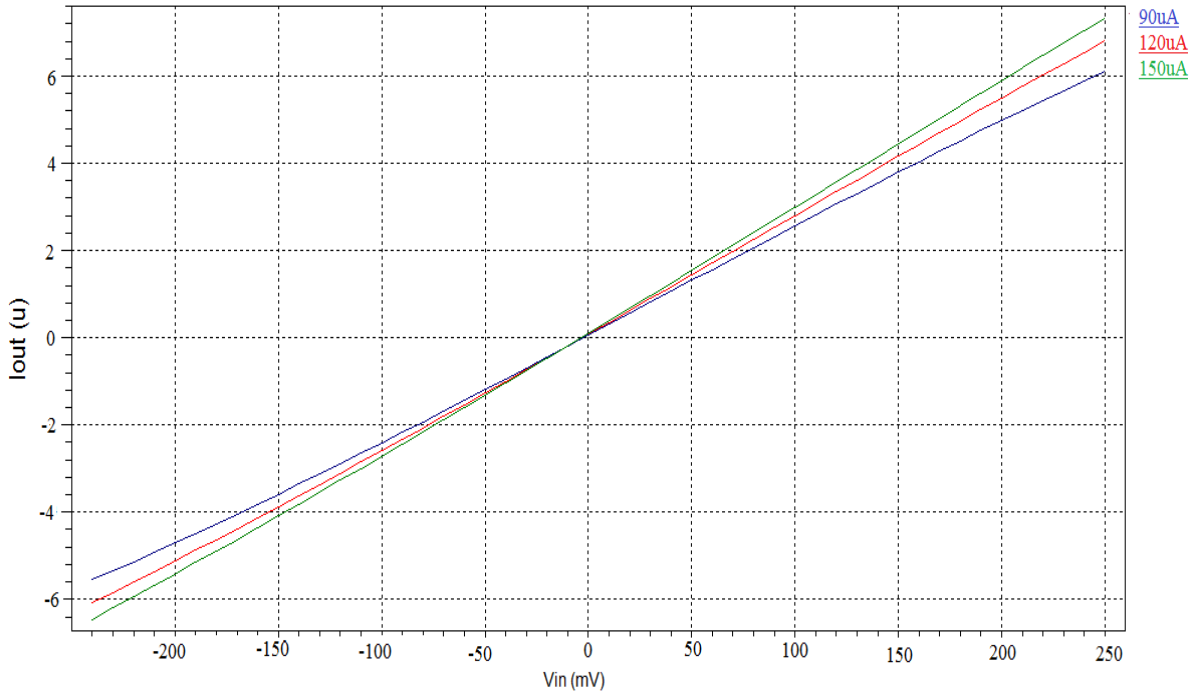

Fig. 5.4: I-V characteristics of the grounded resistor (R)

Table IV shows the variation of the resistance of the grounded resistor for different values of DC bias current (I_B). From the table IV, it is observed that the resistance of grounded resitor changes from 120 KΩ to 24.5 KΩ for the DC bias current 25µA-125µA with the increment of 20µA.

Table IV: Variation of resistance with the bias current (I_B)

DC bias Current (I_B)	Resistance
25 µA	120 KΩ
50 µA	54 KΩ
75 µA	37.2 KΩ
100 µA	29.2 KΩ
125 µA	24.5 KΩ

The I-V characteristics of the grounded resistor (-R) is shown in Fig. 5.5. From the Fig. 5.5 it can be seen that the grounded resistor (-R) shows the linear range from -250mV to 250mV.

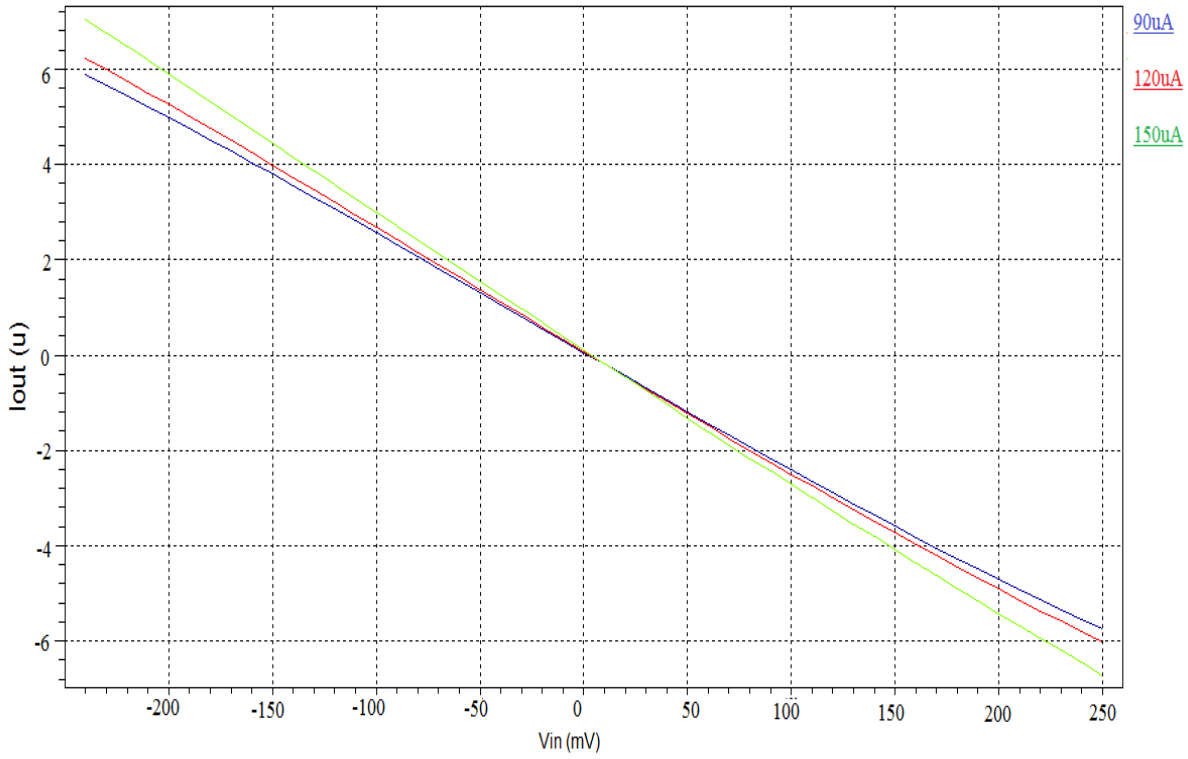

Fig. 5.5: I-V characteristics of the grounded resistor (-R)

5.2.2 SIMULATION RESULTS OF LPF BASED ON FGTGR BASED OTA

The cut-off frequencies of low-pass filter (LPF) based on FGTGR based OTA (Fig. 4.4) for different values of DC bias current (I_B) are listed in table V. From the table V, it is observed that the cut-off frequencies of the low-pass filter changes from 18 KHz to 28.7 KHz for the DC bias current 90 µA to 150 µA with the increment of 20 µA.

Table V: Cut-off frequencies of LPF for different values of DC bias current (I_B).

DC Bias Current	Cut-Off Frequencies
90 µA	18 KHz
110 µA	20 KHz
130 µA	24.5 KHz
150 µA	28.7 KHz

5.2.3 SIMULATION RESULTS OF HPF BASED ON FGTGR BASED OTA

The cut-off frequencies of high-pass filter (HPF) based on FGTGR based OTA (Fig. 4.5) for different values of DC bias current (I_B) are listed in table VI. From the table VI, it is observed that the cut-off frequencies of the high-pass filter changes from 413.65 KHz to 1.03 MHz for the DC bias current 50 µA to 150 µA with the increment of 25 µA.

Table VI: Cut-off frequencies of HPF for different values of DC bias current (I_B).

DC Bias Current	Cut-Off Frequencies
50 µA	413.65 KHz
75 µA	603 KHz
100 µA	788 KHz
125 µA	915 KHz
150 µA	1.03 MHz

5.3 SIMULATION RESULTS OF FGMOS BASED WIDE LINEAR RANGE OTA

The FGMOS based wide linear range (FGWLR) OTA shown in Fig. 4.7 has been simulated using TSMC 0.18 µm CMOS technology. The circuit is operated at the supply voltages of $\pm$0.5V. The dimension of transistors of proposed circuit is listed in table VII.

Table VII: Transistors sizing of FGMOS based wide linear range OTA

MOSFETS	W(µm)	L(µm)
M_1-M_2	5	0.5
M_7-M_8	25	0.5
M_3-M_6, M_{10}-M_{17}	22	0.5
M_9	20.84	0.5

The DC characteristics of the proposed FGMOS based wide linear range OTA is shown in Fig. 5.6. The plot is drawn between output current (I_{OUT}) and the input voltage (V_{in}) for the

different DC bias currents (I_B). From the Fig. 5.6 it can be seen that the FGWLR OTA shows linear range from -350mV to 350mV.

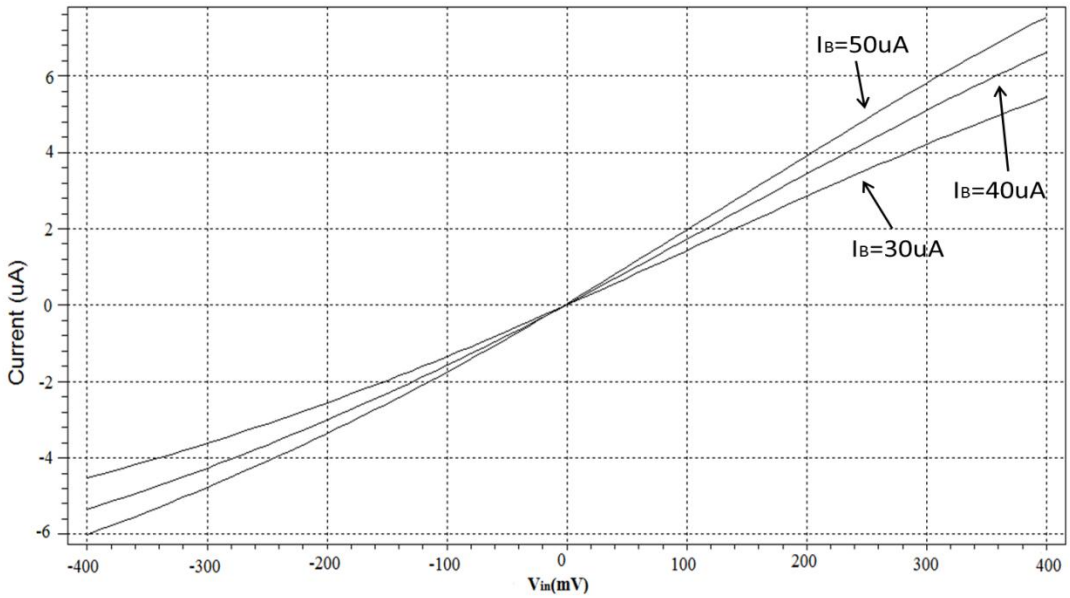

Fig. 5.6: DC Characteristics of the FGWLR OTA

The variation of output current (I_{OUT}) of FGWLR OTA with the bias currents (I_B) is listed in table VIII. From the table VIII, it is observed that the output current (I_{OUT}) is directly proportional to the DC bias current (I_B).

Table VIII: Variation of output current (I_{OUT}) with DC bias current (I_B)

I_{OUT}			
Vin(V)	I_B=30 µA	I_B=40 µA	I_B=50 µA
-0.4	-4.51×10^{-6}	-5.34×10^{-6}	-6.00×10^{-6}
-0.3	-3.61×10^{-6}	-4.26×10^{-6}	-4.77×10^{-6}
-0.2	-2.55×10^{-6}	-3.00×10^{-6}	-3.35×10^{-6}
-0.1	-1.34×10^{-6}	-1.57×10^{-6}	-1.75×10^{-6}
0.1	1.42×10^{-6}	1.55×10^{-6}	1.96×10^{-6}
0.2	2.8×10^{-6}	3.43×10^{-6}	3.91×10^{-6}
0.3	4.2×10^{-6}	5.09×10^{-6}	5.81×10^{-6}
0.4	5.44×10^{-6}	6.60×10^{-6}	7.54×10^{-6}

The linearity error for the proposed FGMOS based wide linear range OTA is shown in Fig. 5.7. The proposed FGMOS based OTA converts the input voltage into output current with nonlinearity of less than 4% for the input voltage (V_{in}) in the ranges of -250mV to 250mV.

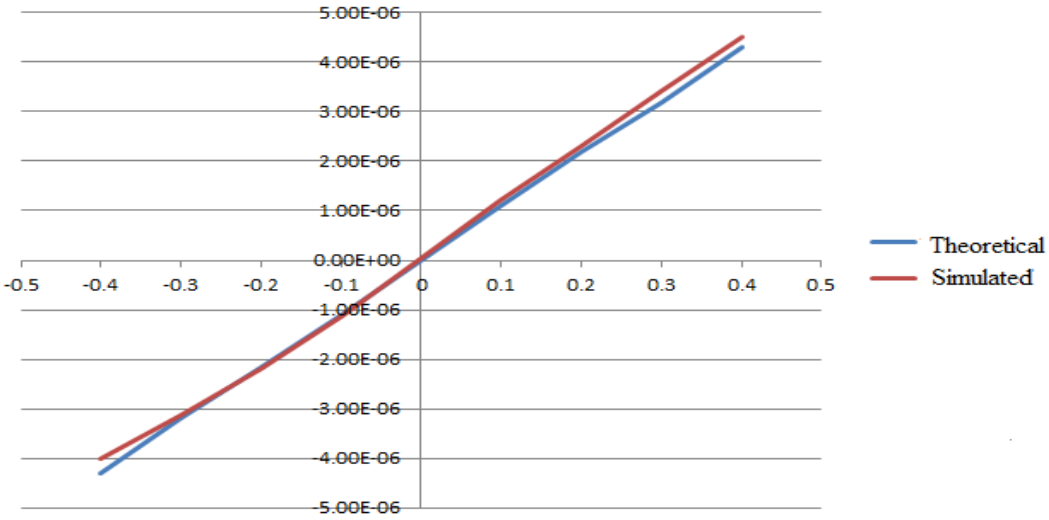

Fig. 5.7: Linearity error for the FGWLR OTA

The frequency response of the FGMOS based wide linear range OTA is shown in Fig. 5.8. From the Fig. 5.8, it is observed that -3dB frequency of the circuit is 17MHz.

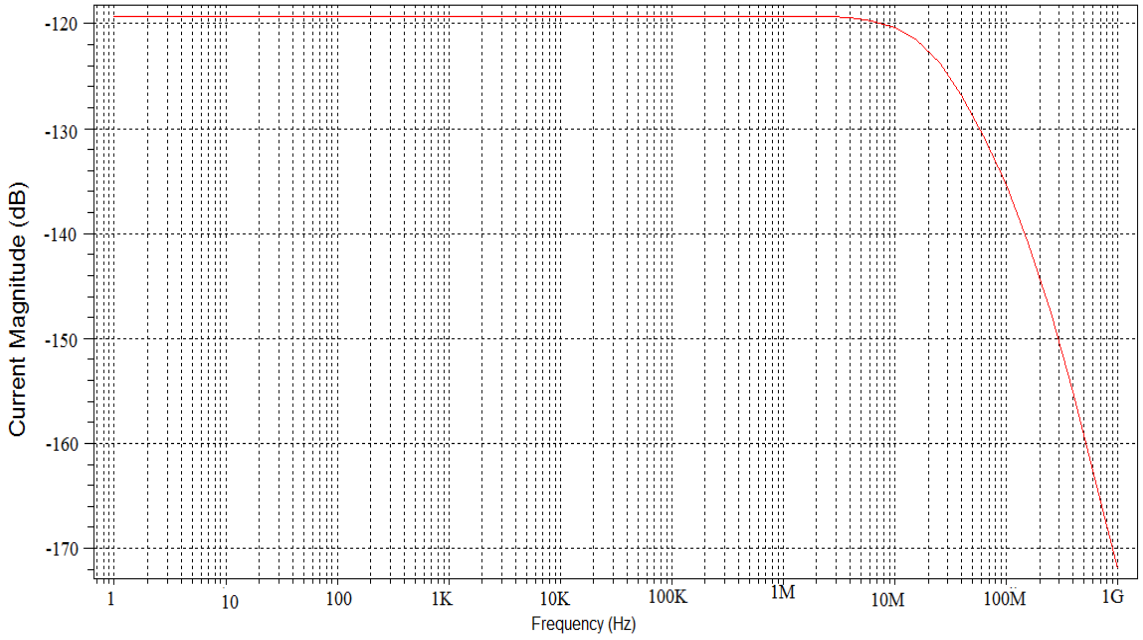

Fig. 5.8: Frequency response of the FGWLR OTA

The variation of transconductance (g_m) of the FGMOS based wide linear range OTA with the the bias current (I_B) is shown in Fig. 5.9. The plot is obtained by varying the DC bias current (I_B) from 40 μA to 140 μA.

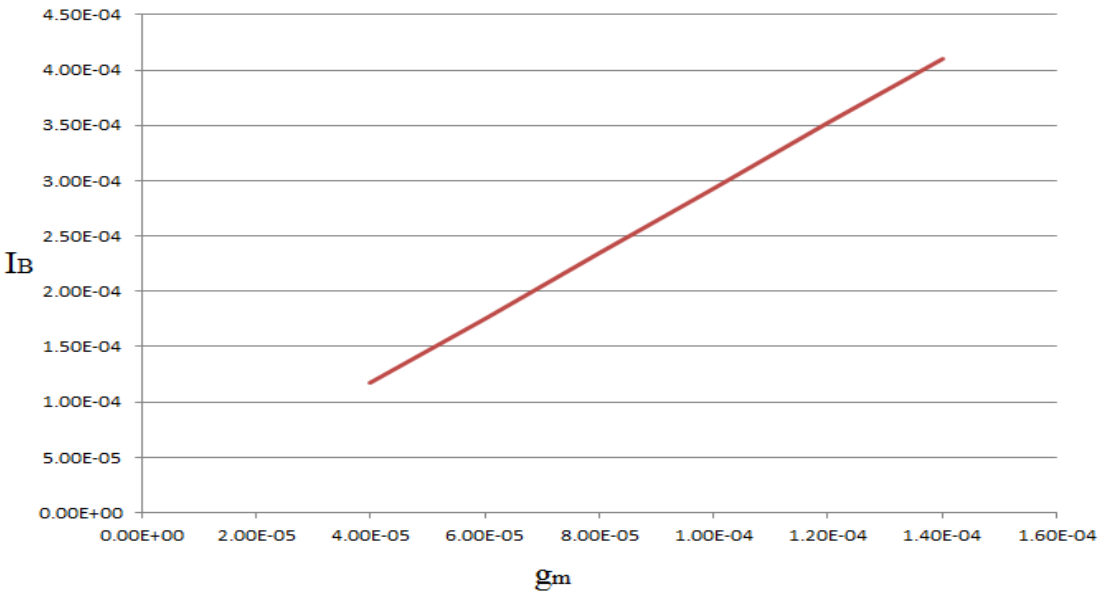

Fig. 5.9: Variation of transconductance (g_m) with DC bias current (I_B)

Table IX compares the proposed FGWLR OTA with different OTAs available in literature [16, 18, 19, 20, 22, 25]. From the table IX, it can be seen that the proposed FGWLR OTA has lower supply voltage requirement and higher linear range.

Table IX: Comparison of FGWLR OTA with previous circuits

	FGWLR OTA	[16]	[18]	[19]	[20]	[22]	[25]
CMOS Tech.	0.18 µm	0.18 µm	1 µm	1 µm	0.5 µm	0.18 µm	0.35 µm
V_{DD}(V)	1	1.5	5	5	3.3	1.8	1.8
Tunability	Current-Voltage	voltage	Current	Current	Current	Current	Voltage
g_m(µA/V)	73-439	120-287	0-539	102.4	50-200	3.36-452	45-406
Basic Cell	Balanced CMOS OTA	Cross coupled pair	Balanced CMOS OTA	Balanced CMOS OTA	Flipped voltage follower	Pseudo differential pair	Self-Cascode pair
-3 dB BW	17 MHz	50 MHz	120 MHz	47 MHz	NA	680 MHz	78 MHz
Linear range	70% of V_{in}	NA	25% of V_{in}	44% of V_{in}	NA	22% of V_{in}	NA
Operating Region	Saturation Region	Saturation Region	Saturation Region	Saturation Region	Triode Region	Saturation Region	Triode Region

5.3.1 SIMULATION RESULTS OF FGWLR OTA BASED GROUNDED RESISTOR

Fig. 5.10 shows the I-V characteristics of the grounded resistor (R), developed using FGWLR OTA shown in Fig. 4.8. From the Fig. 5.10 it can be seen that the grounded resistor shows linear range from -250mV to 250mV.

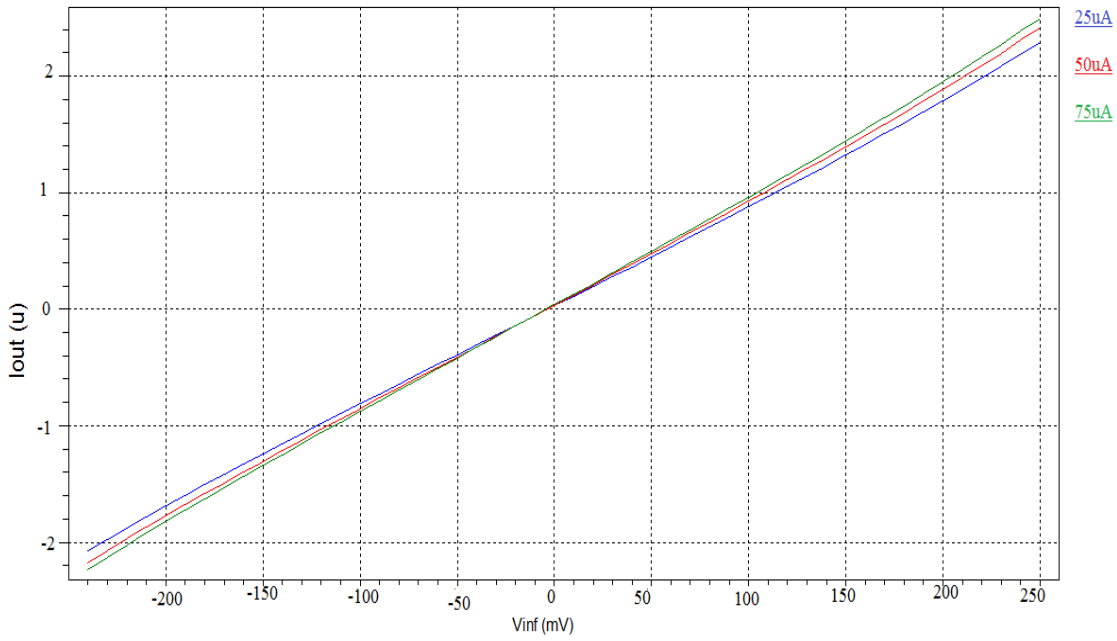

Fig. 5.10: I-V characteristics of the grounded resistor (R)

Table X shows the variation of the resistance of the tunable grounded resistor for different values of DC bias current (I_B). From the table X, it is observed that the resistance of grounded resistor changes from 187 KΩ to 91 KΩ for the DC bias current 25µA-65µA with the increment of 20µA.

Table X: Variation of resistance with the bias current (I_B)

DC bias current (I_B)	Resistance
25 µA	187 KΩ
35 µA	148 KΩ
45 µA	120 KΩ
55 µA	103 KΩ
65 µA	91 KΩ

The I-V characteristics of the grounded resistor (-R) is shown in Fig. 5.11. From the Fig. 5.11 it can be seen that the grounded resistor shows linear range from -250mV to 250mV.

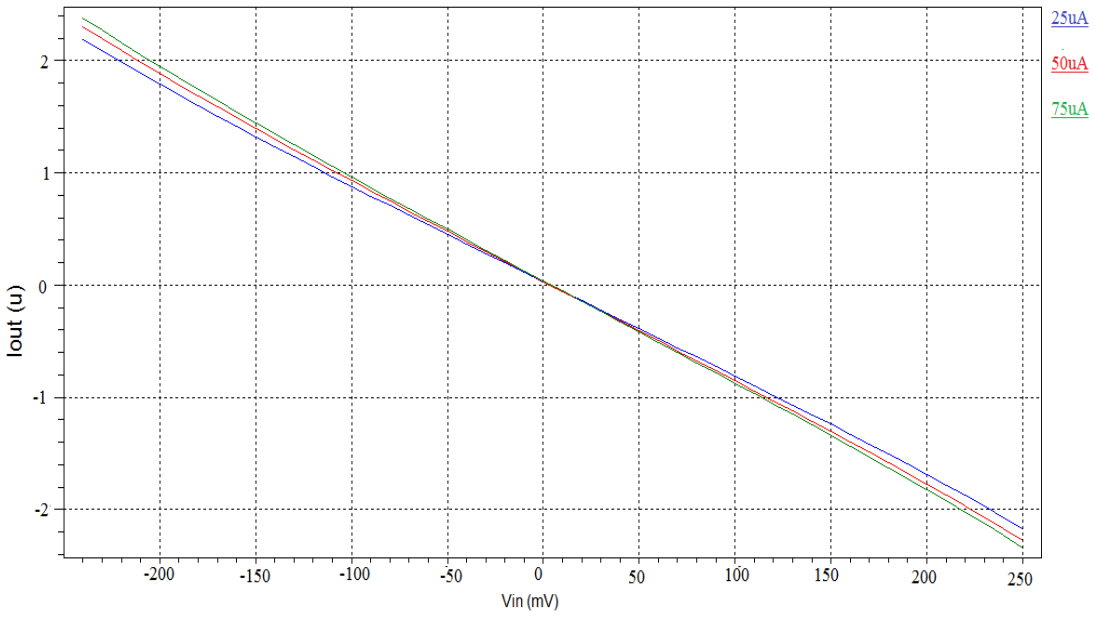

Fig. 5.11: I-V characteristics of the grounded resistor (-R)

5.3.2 SIMULATION RESULTS OF FGWLR OTA BASED LPF

The cut-off frequencies of low-pass filter (LPF) based on FGWLR OTA (Fig. 4.10) for different values of DC bias current (I_B) are listed in table XI. From the table XI, it is observed that the cut-off frequencies of the LPF changes from 42 KHz to 81 KHz for the DC bias current 25 µA-50 µA with the increment of 5 µA.

Table XI: Cut-off frequencies of LPF for different values of DC bias current (I_B).

DC bias Current (I_B)	Cut-Off Frequencies
25 µA	42 KHz
30 µA	50.2 KHz
35 µA	58 KHz
40 µA	66 KHz
45 µA	74 KHz
50 µA	81 KHz

5.3.3 SIMULATION RESULTS OF FGWLR OTA BASED HPF

The cut-off frequencies of high-pass filter (HPF) based on FGWLR OTA (Fig. 4.11) for different values of DC bias current (I_B) are listed in table XII. From the table XII, it is observed that the cut-off frequencies of the high-pass filter changes from 5.25 KHz to 31.62 KHz for the DC bias current 25 µA-150 µA with the increment of 25 µA.

Table XII: Cut-off frequencies of HPF for different values of DC bias current (I_B).

DC bias Current (I_B)	Cut-Off Frequencies
25 µA	5.25 KHz
50 µA	11.39 KHz
75 µA	17.93 KHz
100 µA	20 KHz
125 µA	25 KHz
150 µA	31.62 KHz

5.4 LAYOUT OF PROPOSED CIRCUITS

The physical layout of FGMOS based balanced OTA and FGMOS based wide linear range OTA have been designed using UMC 0.18µm CMOS process technology in cadence virtuoso layout editor. Design Rule Check (DRC) is performed in order to verify that layout fulfils all electrical and geometric rules provided by foundry. The basic design rules are:

Metal 1 to metal 1 spacing	0.24 µm
Minimum contact size	0.24 µm*0.24 µm
Poly to poly spacing	0.24 µm
Poly to metal spacing	0.28/0.00 µm
Contact overlap to p+ diffusion	0.1 µm
Metal 1 width	0.24 µm
Poly extension beyond active	0.22 µm
Minimum contact spacing	0.26 µm
N well overlap p+ diffusion	0.43 µm
Diffusion contact to poly spacing	0.15 µm

Minimum p+ implant overlap p+ diffusion	0.22 µm
Poly width	0.18 µm
Minimum poly extension on to field region	0.22 µm
Poly contact to diffusion edge spacing	0.18 µm
Minimum poly overlap contact	0.1 µm
Minimum metal area	0.1764 µm*µm
Minimum metal2 width	0.28 µm
Metal1 and metal2 overlap over via	0.08 µm
Minimum non equal potential 1.8 V N well spacing	2µm

5.4.1 LAYOUT OF FGMOS BASED BALANCED OTA

The layout of the FGMOS based balanced OTA of Fig. 4.7 is designed using UMC 0.18µm CMOS process technology in cadence virtuoso layout editor and is shown in Fig. 5.12.

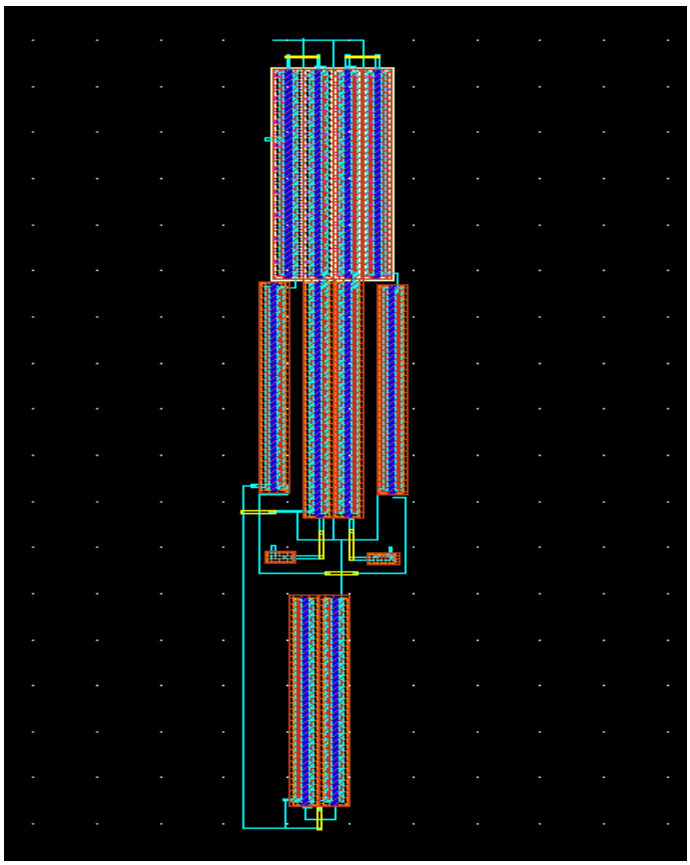

Fig. 5.12: Layout of FGMOS based balanced OTA

5.4.2 LAYOUT OF FGMOS BASED WIDE LINEAR RANGE OTA

The layout of the FGMOS based wide linear range OTA of Fig. 4.6 is designed using UMC 0.18µm CMOS process technology in cadence virtuoso layout editor and is shown in Fig. 5.13.

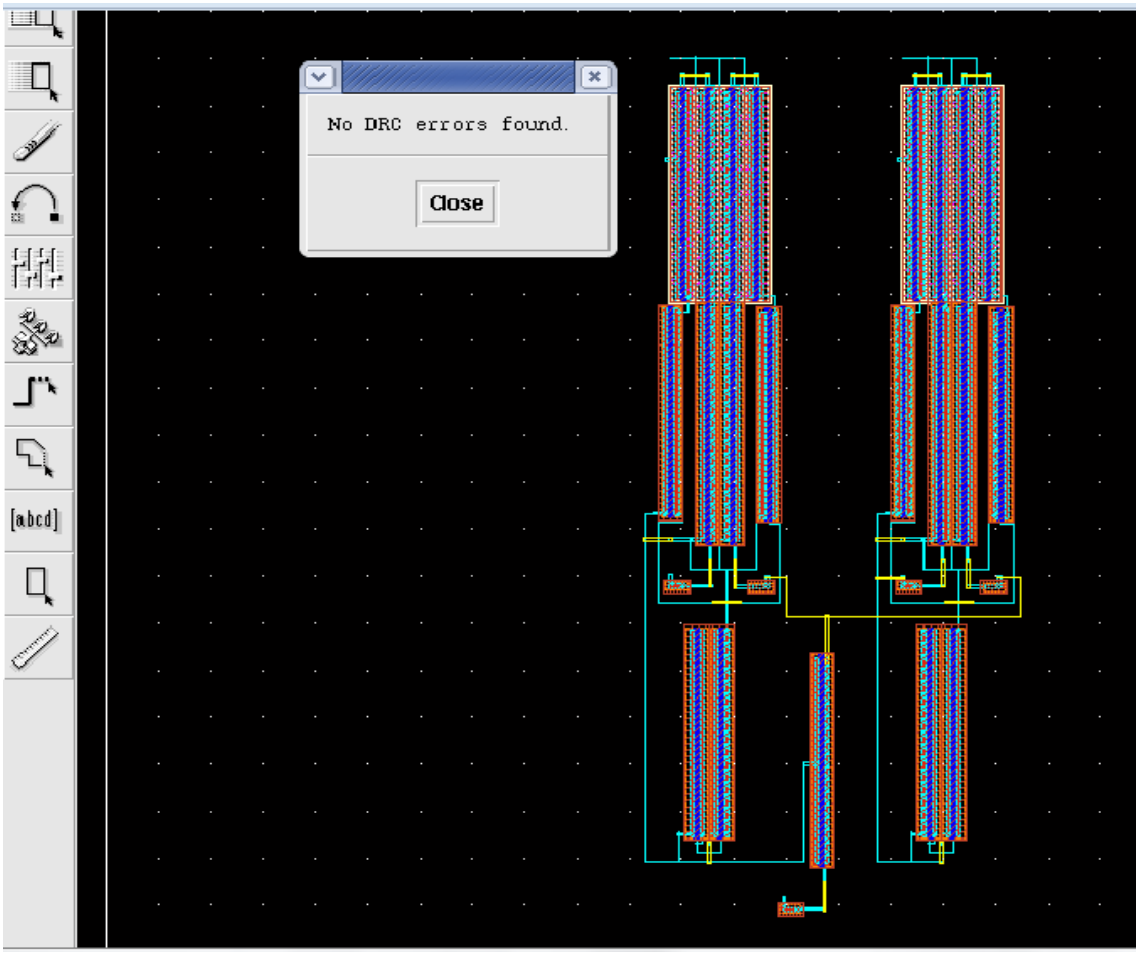

Fig. 5.13: Layout of FGMOS based wide linear range OTA

5.5 CONCLUSIONS

In this chapter, the simulation results of FGTGR based OTA and FGWLR OTA are presented. The FGTGR based OTA shows linear range from -150mV to 150mV and FGWLR OTA shows linear range from -350mV to 350mV at supply voltage of $\pm$0.5V. Thus FGWLR OTA shows better linear range and is preferred.

CHAPTER 6

CONCLUSIONS AND FUTURE SCOPE

6.1 CONCLUSIONS

Operational transconductance amplifier is an important building block of analog signal processing applications. With reduction in supply voltage, as the current mode signal processing is becoming more attractive because of its numerous advantages, the role of Operational transconductance amplifier has become even more important. OTA has very good high frequency response which makes it suitable for high frequency applications. Tunability of OTA provides flexibility to change the range of filters as well as gain in automatic gain controllers.

In this work low voltage wide linear range operational transconductance amplifier has been developed by using floating-gate MOSFETs. The FGTGR based OTA and FGMOS based wide linear range (FGWLR) OTA has been proposed. The proposed circuits have been simulated using TSMC 0.18μm CM OS technology process parameters and their simulation results have been presented. The transconductance of the proposed circuits can be varied either by changing the bias current (I_B) or variable resistnace of the FGTGR. The proposed circuits have been compared with the existing circuits available in the literature and it is observed that the proposed FGWLR OTA has lower supply voltage requirement and higher linearity whereas FGTGR based OTA has higher transconductance range. The proposed circuits are also used to develop grounded resistor, low-pass filter and high-pass filter and simulation results of these circuits have been presented. The physical layout of FGMOS based wide linear range OTA is designed using standard UMC 0.18μm CMOS process technology.

6.2 FUTURE SCOPE

Some suggestions and ideas for future work:

- The bandwidth of the proposed FGMOS based wide linear range OTA can be improved by using quasi floating-gate MOSFETs.
- The linear range of the proposed circuits can be further extended by using additional transistor in parallel with the input transistors to overcome common mode range constraints.

LIST OF PUBLICATIONS

- **Sumit Verma** and Rishikesh Pandey, "Design of Electronic Tunable CMOS OTA: A Comparative study," *International Journal of Electronics Communication and Computer Engineering*, pp. 478-481, Mar. 2013.
- **Sumit Verma** and Rishikesh Pandey, "Novel operational transconductance amplifier based on floating-gate MOSFET tunable grounded resistor," *International Conference on Advances in Electronics, Electrical and Computer Engineering*, Dehradun, June 22-23, 2013.

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