LOW-VOLTAGE ANALOG CIRCUITS BASED ON FLIPPED VOLTAGE FOLLOWER CELL

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in

VLSI Design & CAD

Submitted by

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This thesis is dedicated to my parents
for their love, endless support
and encouragement.

CERTIFICATE

I hereby declare that the work, which is being presented in the thesis, entitled "**LOW-VOLTAGE ANALOG CIRCUITS BASED ON FLIPPED VOLTAGE FOLLOWER CELL**" in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI Design & CAD at Department of Electronics and Communication Engineering, Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Mr. Rishikesh Pandey, Assistant Professor, Department of Electronics and Communication Engineering (ECED).

The matter presented in the thesis has not been submitted in any other University/Institute for the award of any degree.

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ABSTRACT

In this thesis, a basic cell known as “Flipped Voltage Follower” for low-power/low-voltage operation is explained. It is evidenced how different versions of this cell, coined as “Flipped Voltage Follower (FVF)” have been used in the past for many applications. The detailed classification of basic topologies derived from the FVF cell is presented. In addition, a comprehensive list of recently proposed low-voltage/low-power CMOS circuits based on the Flipped Voltage Follower is explained. Some applications of the FVF cell such as current mirror and four-quadrant analog multiplier are also discussed which show the potential of FVF cell for the design of high-performance low-power/low-voltage analog and mixed-signal circuits.

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V_{DD}	Supply Voltage	λ	Channel length modulation
V_o	Output Voltage	μ	Mobility
V_{in}	Input Voltage	g_{mi}	Transconductance of MOSFET
V_A	Early Voltage	C_{in}	Input Capacitance
V_{GS}	Gate to Source Voltage	C_{gs}	Gate to Source Capacitance
V_{DS}	Drain to Source Voltage	C_{gd}	Gate to Drain Capacitance
V_{BS}	Body to Source Voltage	C_{db}	Drain to Substrate Capacitance
R_s	Source Resistance	C_{ox}	Oxide Capacitance
R_L	Load Resistance	V_T	Thermal Voltage
r_{oi}	Output Resistance	i_o	Output Current
I_{in}	Input Current	W	Width of MOSFET
z_{in}	Input Impedance	L	Length of MOSFET
z_o	Output Impedance	V_{TH}	Threshold Voltage
ω_p	Pole Frequency	C_L	Load Capacitance
ω_{in}	Input Pole Frequency	I_D	Drain Current
ω_o	Output Pole Frequency	γ	Body effect coefficient

CHAPTER

1

INTRODUCTION

1.1 Background

Downscaling of CMOS processes has forced analog circuits to operate with continuously decreasing supply voltages. This trend has been mainly driven by the need to reduce power consumption of the digital circuitry in mixed-mode very large-scale integration (VLSI) systems and to prevent oxide breakdown with decreasing gate-oxide thickness. In addition, low power consumption and low supply voltages are requirements of the portable electronic equipment market. Several techniques have been proposed to reduce supply voltage requirements in analog and mixed-signals circuits, among them: Folding cascode, Triode-mode and Subthreshold operation of MOS transistors, Floating-gate MOSFET, Level shifter, Bulk driven circuit and Current-mode processing [1].

1.2 Motivation

Out surrounding world is analog in nature. Digital systems require analog to digital conversion at the front of the system and digital to analog conversion at its end. Analog computation and signal processing makes it simpler and faster [2]. Analog signal processing represents the signals as physical quantities like e.g. charge, current, voltage or frequency. These signals are continuous in value and continuous in time. Analog signal processing is most effective when precision is not the major criteria and when massive parallel collective processing of large number of signals that are continuous in time and amplitude is required [3]. In this thesis, we discuss the low voltage analog circuit design. The new smaller size process technologies offer opportunities to operate at higher frequencies consuming less power. For analog circuits, this fact partially applies since it is often the case that additional current is needed to keep the same performance when the power supply voltage is decreased. Furthermore, for sub-micron technology it would not

be possible to use voltage doublers to enhance the circuit performance due to low breakdown voltage of the transistors [4].

Driven by low-power and low-voltage requirements for integrated mixed-signal portable applications, analog signal processing circuits such as four-quadrant analog multipliers are becoming more compact and operate with lower supply voltages. Concentrating on circuit topologies, a circuit cell called "flipped voltage follower" (FVF) has been popularly used for low-voltage design since it needs only a supply voltage of $V_{TH} + V_{eff}$, where V_{TH} is the threshold voltage and $V_{eff} (= V_{GS} - V_{TH})$ is the effective gate voltage. Further detail about flipped voltage follower (FVF) cell is discussed in Chapter 2.

1.3 Applications

The FVF cell has been used in the past for different application such as current mirror [5], current conveyor [6], and multiplier [7] etc. In this thesis, some application of the flipped voltage follower (FVF) cell such as current mirror and multiplier have been presented.

1.4 Thesis organization

This thesis is organized such that first it provides an insight into different analog circuits based on FVF cell and then discusses specifics of different design methods, simulation results and layout considerations.

Chapter 2 concentrates on flipped voltage follower (FVF) cell implementation. The simulation and Layout design of FVF cell has been presented.

Chapter 3 concentrates on low-voltage current mirrors based on FVF cell. The simulation and layout design of low-voltage current mirrors based on FVF cell has been presented

Chapter 4 concentrates on low-voltage CMOS four-quadrant analog multiplier based on FVF cell. The simulation and layout design of low-voltage CMOS four-quadrant analog multiplier based on FVF cell has been presented.

Finally, conclusions about my thesis are presented in **Chapter 5**.

CHAPTER

2

THE FLIPPED VOLTAGE FOLLOWER

2.1 Source follower

The source follower (common-drain configuration) is shown in Figure 2.1(a). The input signal is applied to the gate and the output is taken from the source. From a large-signal standpoint, the output voltage is equal to the input voltage minus the gate-source voltage. The gate-source voltage consists of two parts: the threshold voltage and the overdrive voltage. If both parts are constant, the resulting output voltage is simply offset from the input, and the small-signal gain would be unity. Therefore, the source follows the gate, and the circuit is also known as a s*ource follower*. In practice, the body effect changes the threshold voltage, and the overdrive depends on the drain current, which changes as the output voltage changes unless $R_L \rightarrow \infty$. Furthermore, even if the current were exactly constant, the overdrive depends to some extent on the drain-source voltage unless the Early voltage is infinite.

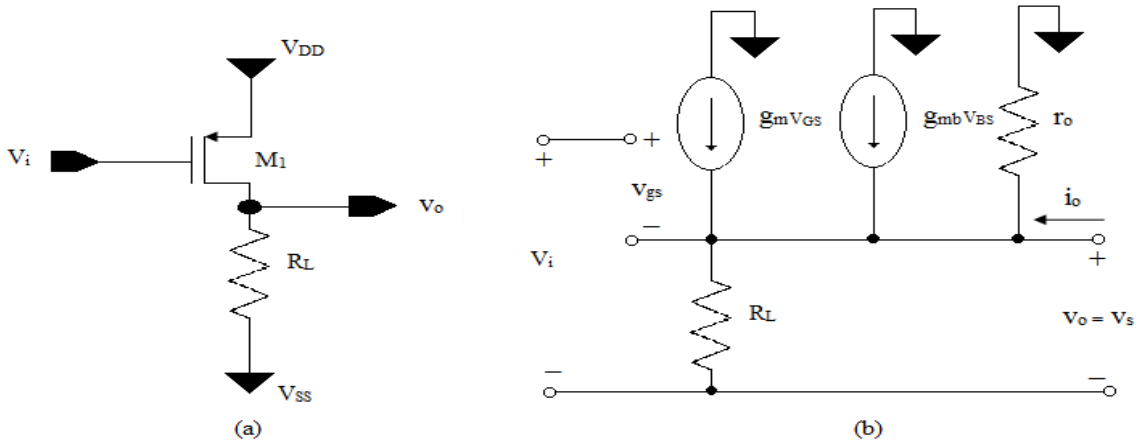


Figure 2.1: (a) Source follower. (b) Small-signal equivalent circuit of the source follower [8].

We will use small signal analysis to study these effects. The small-signal equivalent circuit is shown in Figure 2.1(b)**.** Since the body terminal is not shown in Figure 2.1(a), we assume that the body is connected to the lowest supply voltage (ground here) to keep

the source-body *p-n* junction reverse biased. As a result, V_{BS} changes when the output changes because the source is connected to the output, and the g_{mb} generator is active in general.

From KVL around the input loop,

$$V_i = V_{GS} + V_o \tag{2.1}$$

With the output open circuited, $i_0 = 0$, and KCL at the output node gives

$$g_m V_{GS} - g_{mb} V_o - \frac{V_o}{R_L} - \frac{V_o}{r_o} \tag{2.2}$$

Solving (2.1) for $i_o = 0$ substituting into (2.2) and rearranging gives

$$\frac{V_o}{V_i}\Big|_{i_o=0} = \frac{g_m}{g_m + g_{mb} + \frac{1}{R_L} + \frac{1}{r_o}} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o + \frac{r_o}{R_L}} \tag{2.3}$$

If $R_L \to \infty$, (2.3) simplifies to

$$\lim_{R_L \to \infty} \frac{V_o}{V_i}\Big|_{i_o=0} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} \tag{2.4}$$

Equation (2.4) gives the open circuit voltage gain of the source follower with the load resistor replaced by an ideal current source. If r_o, is finite, this gain is less than unity even if the body effect is eliminated by connecting the source to the body to deactivate the g_{mb} generator. In this case, variation in the output voltage changes the drain-source voltage and the current through r_o. Overdrive voltage ($V_{GS} - V_{TH}$) also depends on the drain-source voltage unless the channel length modulation (λ) is zero. This dependence causes the small-signal gain to be less than unity.

$$\lim_{\substack{R_L \to \infty \\ r_o \to \infty}} \frac{V_o}{V_i}\Big|_{i_o=0} = \frac{g_m r_o}{1 + (g_m + g_{mb}) r_o} = \frac{1}{1 + \eta} \tag{2.5}$$

Equation (2.5) shows that the source-follower gain is less than unity under these conditions and that the gain depends on $\eta = g_{mb}/g_m$, which is typically in the range of 0.1 to 0.3. The output resistance of the source follower can be calculated from Figure 2.1(b) by setting $V_i = 0$ and driving the output with a voltage source V_o.

Then $V_{GS} = -V_o$ and i_o is

$$i_o = \frac{V_o}{r_o} + \frac{V_o}{R_L} + g_m V_o + g_{mb} V_o \tag{2.6}$$

Rearranging (2.6) gives,

$$R_o = \frac{V_o}{r_o} = \frac{1}{g_m + g_{mb} + \frac{1}{r_o} + \frac{1}{R_L}} \tag{2.7}$$

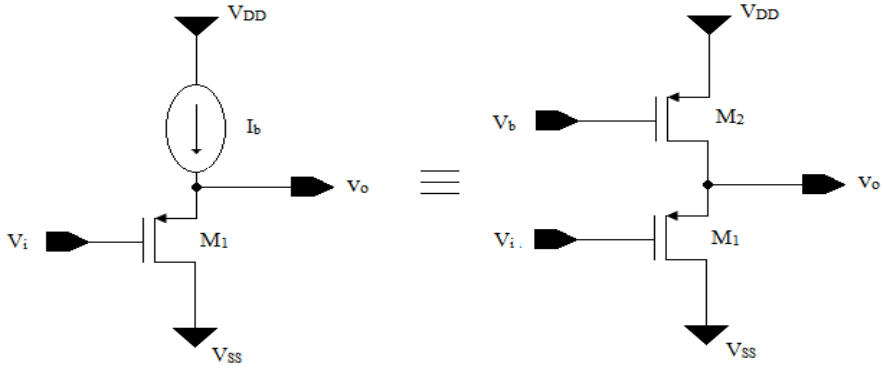


Figure 2.2: PMOS source follower with no body effect [9].

Equation (2.7) shows that the body effect reduces the output resistance, which is desirable because the source follower produces a voltage output. This beneficial effect stems from the nonzero small-signal current conducted by the g_{mb} generator in Figure 2.1(b), which increases the output current for a given change in the output voltage. As $r_o \to \infty$ and $R_L \to \infty$, this output resistance approaches

$$R_o = \frac{1}{(g_m + g_{mb})} \tag{2.8}$$

As mentioned in the relation to Figure 2.1(a), even if a source follower is biased by an ideal current source as shown in Figure 2.2. Its input-output characteristic displays some

nonlinearity due to nonlinear dependence of V_{TH} upon the source potential. In submicron technologies, r_o of the transistor also changes substantially with V_{DS}, thus introducing additional variation in the small-signal gain of the circuit. For this reason source followers suffer from several percent of nonlinearity.

The nonlinearity due to body effect can be eliminated if the bulk is tied to the source. This is usually possible only for PFETs because all NFETs share the same substrate. Figure 2.2 shows a PMOS source follower employing two separate n-wells so as to eliminate the body effect of M_1.

2.2 Flipped voltage follower cell

Let us consider the common drain amplifier in Figure 2.2(a), commonly used as a voltage buffer. This circuit is also known as a "*source follower*". If body effect is neglected the circuit follows the input voltage with a dc level shift, i.e. $V_o = V_i - V_{SG1}$. Where V_{SG1} is the source-to-gate voltage of transistor M_1. Concerning the large-signal behavior, this circuit is able to sink a large current from the load, but it sourcing capability is limited by the biasing current source I_b. A drawback of this circuit is that current through transistor M_1 depends on the output current, so that V_{SG1} is not constant and, hence, for resistive loads, the small and large signal voltage gains are less than unity.

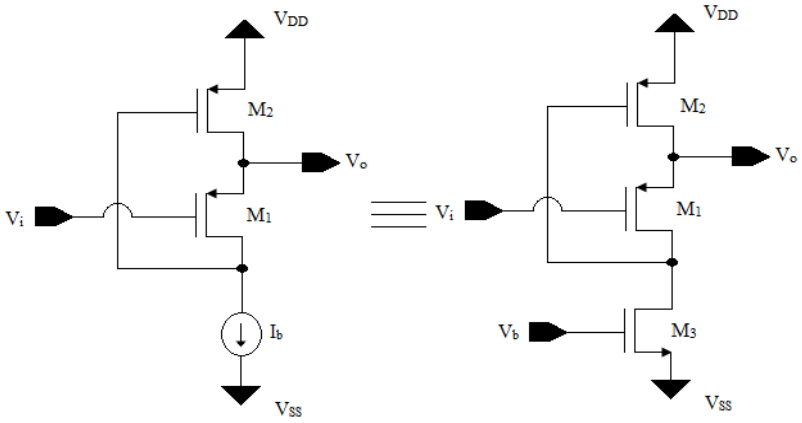


Figure 2.3: (a) Flipped voltage follower cell.

The circuit in Figure 2.3(a) is another source follower where the current through transistor M_1 is held constant, independent on the output current. It could be described as a voltage

follower with shunt feedback. Neglecting the short-channel effect, V_{SG1} is held constant, and voltage gains are unity. Unlike the conventional voltage follower, the circuit in Figure 2.3(a) is able to source a large amount of current, but its sinking capability is limited by the biasing current source I_b, the large sourcing capability is due to the low impedance at the output node ($r_o = 1/g_{m1}\, g_{m2} r_{o1}$), where g_{mi} and r_{oi} are the trans-conductance and output resistance, respectively. This value is in the order of 20-100 Ω.

2.3 Resistance estimation of FVF cell

2.3.1 Resistance at node Y

The open-loop gain analysis of FVF cell and small signal analysis of Figure 2.3 (b) are shown in Figure 2.3(b) and 2.3(c), respectively. The resistance at node Y can be determined by the Figure 2.3 (c) [4].

$$I_Y = \frac{V_Y - V_{S1}}{r_{o1}} + g_{m1} V_{GS1} + \frac{V_Y}{r_b} \tag{2.9}$$

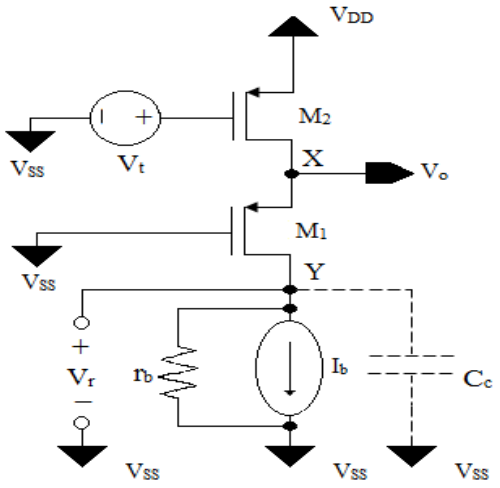


Figure 2.3: (b) Open-loop gain analysis of FVF cell [1].

$$\frac{V_Y - V_{S1}}{r_{o1}} + g_{m1} V_{GS1} = \frac{V_{S1}}{r_{o2}} + g_{m2} V_{GS2} \tag{2.10}$$

$$V_{GS1} = V_{G1} - V_{S1} = -V_{S1} \quad \text{and} \quad V_{GS2} = V_{G2} - V_{S2} = 0$$

From (2.9) we get, $$\frac{V_Y - V_{S1}}{r_{o1}} - g_{m1}V_{S1} = \frac{V_{S1}}{r_{o2}} \tag{2.11}$$

$$V_{S1} = \frac{V_Y r_{o2}}{r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}} \tag{2.12}$$

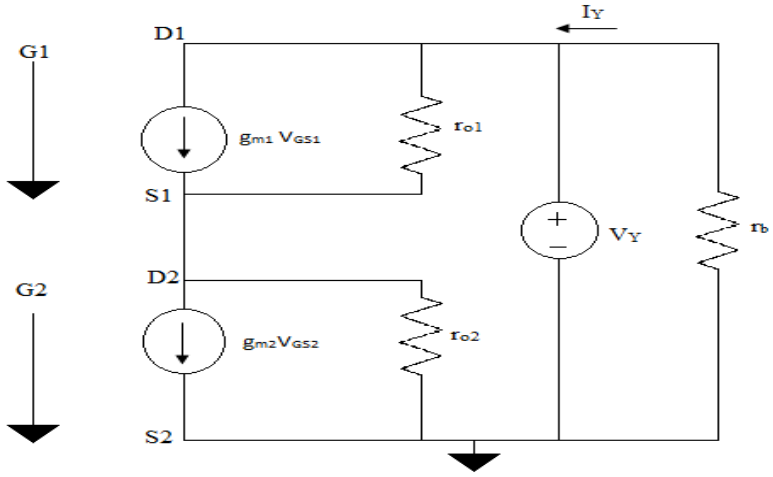


Figure 2.3: (c) Small signal diagram of open-loop gain analysis of FVF cell for node Y.

Substituting V_{S1} from (2.12) in (2.9) and rearranging V_Y and I_Y

$$R_{OLY} = \frac{r_b\left(r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}\right)}{r_b + \left(r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}\right)} \tag{2.13}$$

$$R_{OLY} = r_b \parallel \left(r_{o1} + r_{o2} + g_{m1} r_{o1} r_{o2}\right) \tag{2.14}$$

using approximation $$g_{m1} r_{o1} >> 1 \tag{2.15}$$

and $$g_{m1} r_{o2} >> 1 \tag{2.16}$$

$$R_{OLY} = r_b \parallel g_{m1} r_{o1} r_{o2} \tag{2.17}$$

The resistance R_{OLy} can be calculated directly using the output resistance of common gate amplifier $\left(1 + g_m r_O\right)R_s + r_O$.

For the Figure 2.3(c), $r_o = r_{o1}, R_s = r_{O2}, g_m = g_{m1}$

$$R_{OLY} = (1 + g_{m1} r_{o1}) r_{o2} + r_{o1} \tag{2.18}$$

Using approximation as given in (2.15) and (2.16)

$$R_{OLY} = r_b \parallel g_{m1} r_{o1} r_{o2} \tag{2.19}$$

2.3.2 Resistance at node X

The resistance at node X can be determined by the small signal analysis of open-loop gain analysis of FVF Cell. Small signal diagram of open-loop gain analysis of FVF cell for node X is shown in Figure 2.3(d).

$$I_X = V_X + g_{m1} V_X + \left(\frac{V_X - V_D}{r_{o1}} \right) \tag{2.20}$$

$$g_{m1} V_X + \left(\frac{V_X - V_D}{r_{o1}} \right) = \frac{V_D}{r_b} \tag{2.21}$$

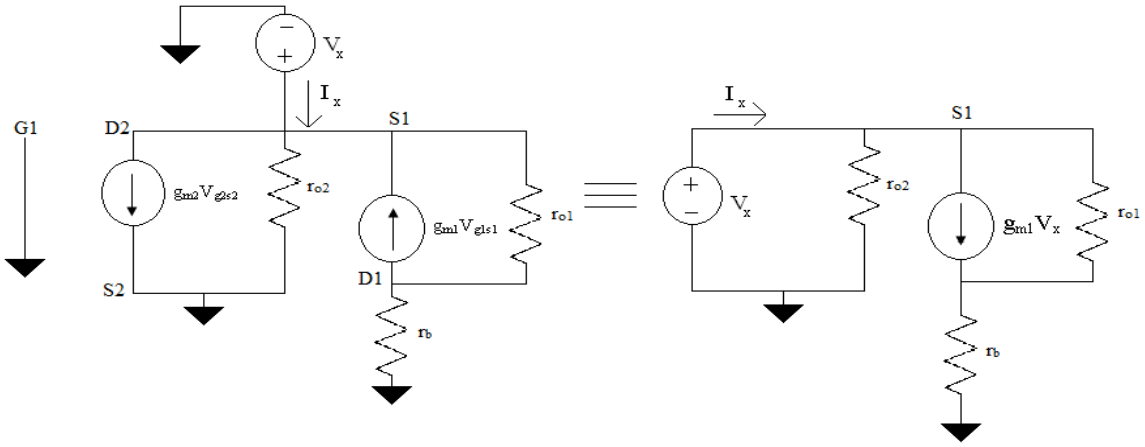


Figure 2.3: (d) Small signal diagram of open-loop gain analysis of FVF cell for node X.

Arranging terms in above equation we get

$$V_D = \frac{(g_{m1} r_{o1} + 1)\left(r_b \big/ r_{o1} \right)}{1 + \left(r_b \big/ r_{o1} \right)} V_X \tag{2.22}$$

Rearranging the equations (2.20) to (2.22)

$$\frac{V_X}{I_X} = \frac{r_{o2}(1 + r_b / r_{o1})1/g_{m1}}{r_{o2}(1 + 1/g_{m1}r_{o1}) + (1 + r_b / r_{o1})/g_{m1}} \tag{2.23}$$

Again using approximation (2.15)

$$R_{OLX} = r_{o2} \parallel (1 + r_b / r_{o1})/g_{m1} \tag{2.24}$$

Open loop gain is $\frac{V_r}{V_t}$ i.e. (A_{OL})

$$\frac{V_X}{V_t} = \text{-g}_{\text{m2}} \text{. (Resistance in drain)} = \text{-g}_{\text{m2}} r_{o2} \tag{2.25}$$

Using gain of the common gate amplifier i.e. $\frac{[(g_{m1} + g_{mb1})r_{o1} + 1]R_D}{r_{o1} + R_D + R_S + (g_{m1} + g_{mb1})r_{o1}R_D}$

$$\frac{V_r}{V_X} = \frac{(g_{m1}r_{o1} + 1)r_b}{r_{o1} + r_b + r_{o2} + g_{m1}r_{o1}r_{o2}} \tag{2.26}$$

Using (2.26) and the two approximations (2.15) and (2.16) we get

$$\frac{V_r}{V_t} = \frac{-(g_{m1}r_{o1} + 1)r_b g_{m2}r_{o2}}{r_{o1} + r_b + r_{o2} + g_{m1}r_{o1}r_{o2}} = \frac{-g_{m1}r_{o1}g_{m2}r_{o2}r_b}{r_b + rg_{m1}r_{o1}r_{o2}} = \text{-g}_{\text{m2}}(r_b \parallel g_{m1}r_{o1}r_{o2}) = \text{-g}_{\text{m2}}R_{OLY}$$

Closed loop gain

$$R_{CLX} = \frac{R_{OLX}}{1 + |A_{OL}|} = \frac{r_{o2} \parallel (1 + r_b / r_{o1})/g_{m1}}{1 + g_{m2}(r_b \parallel g_{m1}r_{o1}r_{o2})} = \frac{r_{o2} \parallel (1 + r_b / r_{o1})/g_{m1}}{g_{m2}(r_b \parallel g_{m1}r_{o1}r_{o2})} \tag{2.27}$$

Case 1: If I_b is simple current mirror then $r_b \approx r_{o1}$

$$R_{CLX} = \frac{2(1/g_{m1} \parallel r_{o2})}{g_{m2}(r_{o1} \parallel (g_{m1}r_{o1}r_{o2}))} \tag{2.28}$$

Using approximation (2.15)

$$R_{CLX} = \frac{2/g_{m1}}{g_{m2}\left(\left(r_{o1}g_{m1}r_{o1}r_{o2}\right)/\left(r_{o1}\left(1+g_{m1}r_{o2}\right)\right)\right)} \approx \frac{2}{g_{m1}g_{m2}r_{o1}} \tag{2.29}$$

Case 2: If I_b is cascode current mirror

$$r_b = \left(1+g_{m1}r_{o1}\right)r_{o2} + r_{O1} \approx g_{m1}r_{o1}r_{o2} \tag{2.30}$$

$$R_{CLX} = \frac{r_{o2} \parallel \left(1+\left(g_{m1}r_{o1}r_{o2}\right)/r_{o1}\right)/g_{m1}}{1+g_{m2}\left(g_{m1}r_{o1}r_{o2} \parallel g_{m1}r_{o1}r_{o2}\right)} = \frac{r_{o2}/2}{1+g_{m1}r_{o1}r_{o2}/2}$$

$$R_{CLX} \approx \frac{1}{g_{m1}g_{m2}r_{o1}} \tag{2.31}$$

In both cases it is observed that R_{CLX} is a very low resistance.

Note that M_2 provides shunt feedback and that M_1 and M_2 form a two pole negative feedback loop. A dominant pole at node Y, $\omega_{pY} = 1/C_Y R_{OLY}$, and a high-frequency pole at node X, $\omega_{pX} = 1/C_X R_{OLX}$,where the open-loop resistance at node Y is given by $R_{OLY} = r_b \parallel g_{m1}r_{o1}r_{o2}$ and the open-loop resistance at node X is given by $R_{OLX} = r_{o2} \parallel \left(1+r_b/r_{o1}\right)/g_{m1}$ and C_X, C_Y are the parasitic capacitances at nodes X and Y respectively (C_X also includes the load capacitor, if any). Figure 2.3(b) shows the same circuit with the feedback loop opens at the gate of M_2 and including a test voltage source V_t. This circuit has an open-loop gain $A_{OL} = V_r/V_t = -g_{m2}R_{OLY}$. The gain bandwidth product is given by $GB = g_{m2}C_Y$.

Note that the FVF can be operated at a very low voltage supply, and that it is the operating condition we are interested in.

From Figure 2.3(a), the following relation can be written as:

$$V_{SD2} = V_{S2} - V_{D2} = V_{DD} - V_{S1} \tag{2.32}$$

Transistor M_1 is in saturation, and neglecting second order effects, the condition of saturation for transistor M_2 is given by the following analysis.

Manipulating V_{S1} we get

$$V_{S1} = V_{G1} + |V_{TP}|_1 + (V_{S1} - V_{G1}) - |V_{TP}|_1$$

$$V_{S1} = V_i + |V_{TP}|_1 + \sqrt{\frac{2I_O}{k_p (W/L)_1}} \tag{2.33}$$

Where I_o is the drain current (I_b in this case), $k_p = \mu_P C_{OX}$, and V_{TP} is the transistor threshold voltage. For saturation of M_2

$$V_{SD2} > V_{SG2} - |V_{TP}|_2 \tag{2.34}$$

Also $$V_{S1} = V_{D2}$$

$$V_{DD} - \left(V_i + |V_{TP}|_1 + \sqrt{\frac{2I_O}{k_p (W/L)_1}} \right) > \sqrt{\frac{2I_O}{k_p (W/L)_1}} \tag{2.35}$$

Now, assuming M_2 is in saturation, and neglecting second order effects, the condition of saturation for transistor M_1 is given by the following analysis

$$V_{SG1} - V_{SD1} < |V_{TP}|_1 \tag{2.36}$$

$$V_{SG1} - V_{SD1} = V_{D1} - V_{G1}$$

$$= V_{D1} - V_{G1} + V_{DD} - V_{S2}$$

$$= V_{G2} - V_i + V_{DD} - V_{S2}$$

$$= V_{DD} - V_{SG2} - V_i$$

$$= V_{DD} - (|V_{TP}|_2 + V_{SG2} - |V_{TP}|_2) - V_i$$

$$= V_{DD} - \left(V_i - |V_{TP}|_2 - \sqrt{\frac{2I_O}{k_p (W/L)_2}} \right) \quad (2.37)$$

From (2.36) and (2.37)

$$V_{DD} - \left(V_i - |V_{TP}|_2 - \sqrt{\frac{2I_O}{k_p (W/L)_2}} \right) < |V_{TP}|_1 \quad (2.38)$$

From (2.35) and (2.38) we get the valid range of operation for the input signal

$$V_{DD} - \left(|V_{TP}|_2 - |V_{TP}|_1 - \sqrt{\frac{2I_O}{k_p (W/L)_2}} \right) < V_i < V_{DD} - \left(|V_{TP}|_1 - \sqrt{\frac{2I_O}{k_p (W/L)_2}} - \sqrt{\frac{2I_O}{k_p (W/L)_1}} \right) \quad (2.39)$$

It is clear from (2.39) that the valid input signal range decreases with the transistor threshold voltage, which limits the applications of the FVF in deep submicron technologies. A dc level shifter between node Y and the gate of transistor M_2 can be used to overcome this problem but at the cost of increased power consumption, and reduced bandwidth [1].

2.4 Properties of the basic FVF cell

- The current through M_1 is constant.
    - This give a more precise copy of the voltage than a traditional source follower can provide or it can be said that the voltage gain is truly 1.
- It can operate at very low voltages (V_{DD} = 1.5V is a common for these circuits).
- It is able to source much more current than a simple source follower.
- It provides a very low impedance output node i.e. $1/g_{m1}g_{m2}r_{o1}$.
- Flipped follower implements an “Active” DC level shift.
- Applications
    - Current mirror
    - Current conveyor
    - Multiplier.
- In a trans-linear loop for multiplicative arithmetic. Fundamental operation: $\sqrt{I_1 I_2}$.

2.5 Basic FVF structures

2.5.1 FVF current sensor (FVFCS)

The FVF can be also considered to be a current sensing cell, and when used in this way it is called a "FVF current sensor (FVFCS) and shown in the Figure 2.4(a)." Let us consider node X in Figure 2.4(a) as the input current sensing node and that all transistors are properly biased to work in the saturation region. Due to the shunt feedback provided by M_2, the impedance at node X is very low and, this way, the amount of current that flows through this node does not modify the value of its voltage. Note that node X can source large current variations at the input and the FVF translates them into compressed voltage variations at output node Y. This voltage can be used to generate replicas of the input current as shown in Figure 2.4(a) by means of M_5. Figure 2.4(b) shows the dc response of FVFCS . The output and the input currents are related through the expression $I_{out} = I_{in} + I_b$. The current I_b can be easily removed from the output node using current mirroring techniques if this is needed for a specific application.

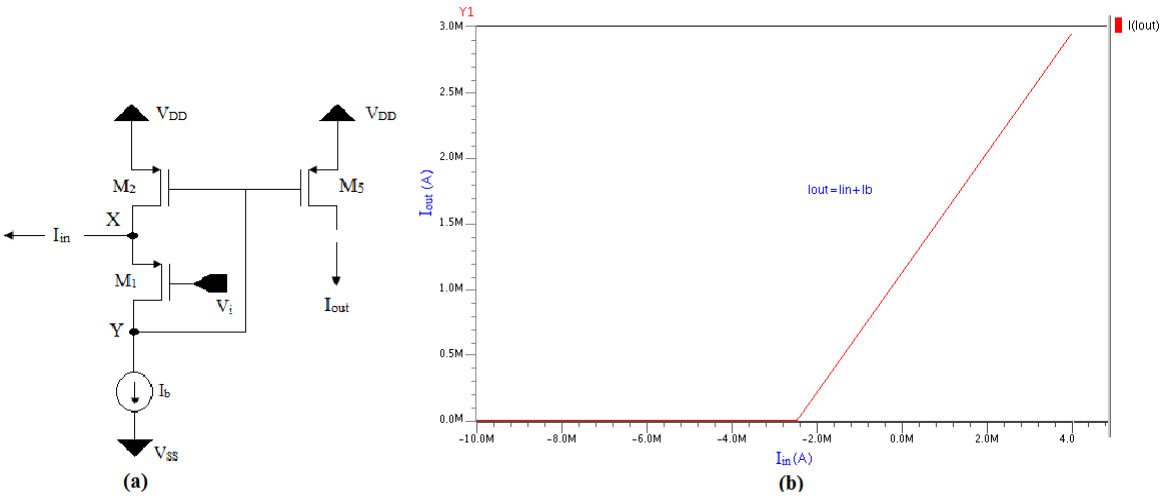


Figure 2.4: (a) Basic implementation of FVFCS. (b) DC response of FVFCS.

Apart from this particular operating condition, the FVFCS can be operated with very low supply voltage. The minimum supply voltage is $V_{DD}^{MIN} = |V_{TP}| + 2V_{DSsat}$, where, V_{TP} is the transistor threshold voltage and V_{DSsat} is the minimum drain-to-source voltage required to maintain a transistor in saturation. The minimum supply voltage V_{DD}^{MIN} can be as low as

950 mV for a 0.35-µm CMOS technology with $V_{TP} = 650\,\text{mV}$ [3]. Obviously, with $V_{DD} = V_{DD}^{MIN}$ there is no room for input current variation; for a given input current I_{in}, ranging from 0 to I_{in}^{MAX}, the minimum supply current is $|V_{TP}| + 2V_{DSsat} + \sqrt{2(I_{in}^{MAX} + I_b)/k_P(W/L)_{M2}}$ [1].

2.5.2 FVF differential structure (DFVF)

The first differential structure based on the FVF cell can be built by adding an extra transistor connected to node X, as it is shown in Figure 2.5(a) [1]. It will be called the "FVF differential structure (DFVF)." As indicated in the previous section, the impedance at node X is very low and its voltage remains approximately constant for large currents through M_3. If we consider quiescent conditions when $V_1 = V_3$, and assuming the same transistor sizes for M_1 and M_3, the condition $I_{DM1} = I_{DM3} = I_b$ is satisfied. A differential voltage $V_1 - V_3$ generates current variations in M_3 that follow the MOS square law. This is a very interesting property of the DFVF as the maximum output current can be much larger than the quiescent current I_b. Figure 2.5(b) shows the dc transfer characteristic for I_{DM3} versus $V_1 - V_3$. The typical Class-AB behavior can be observed.

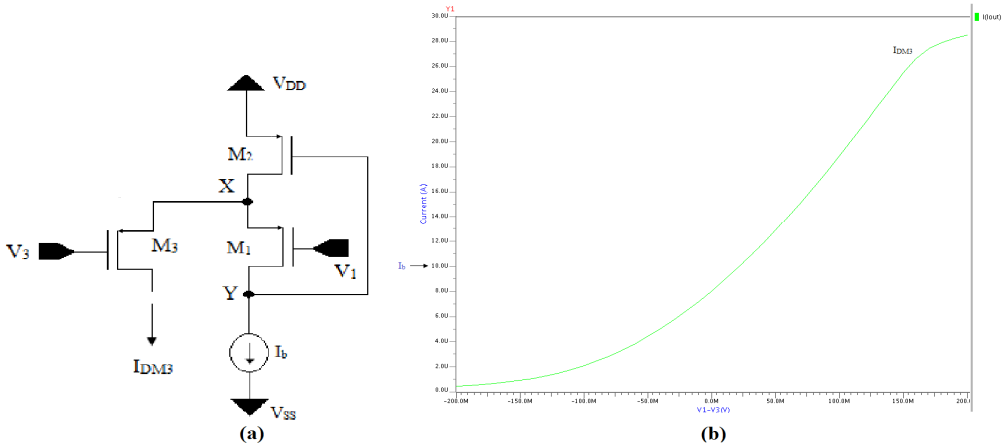


Figure 2.5: **(a)** Basic implements of DFVF. **(b)** DC response of DFVF.

Another characteristic of the DFVF is that the output is available as both a current (I_{DM3}, or the current through M_2 replicated by means of a current mirror), and a voltage (node Y). This feature can be advantageously employed to simplify the circuit implementations

reducing both noise and number of poles and zeros. Finally, the DFVF can also be operated with very low supply voltage. The minimum supply voltage is, as in the case of the FVFCS, $V_{DD}^{MIN} = |V_{TP}| + 2V_{DSsat}$. Once again, with a supply of V_{DD}^{MIN} there would be no room for variation of the input signals V_1 and V_3. It is easy to obtain an expression relating the expected variation of V_1 and V_3 with the minimum supply voltage which maintains the DFVF cell properly biased [1].

2.5.3 FVF pseudo-differential pair (FVFDP)

A pseudo-differential pair can be easily constructed from the DFVF by adding an extra M_4 connected to node X, as shown in Figure 2.6(a). This structure will be called the "FVF pseudo-differential pair (FVFDP)." Figure 2.6(b) shows the dc output currents I_{DM3} and I_{DM4} versus the differential input voltage $V_3 - V_4$, in a typical case. The pseudo-differential pair also exemplifies the characteristic behavior of a Class-AB circuit, where the quiescent output current I_b can be much lower than the peak value. In this case, we have considered that, under quiescent conditions, $V_1 = V_3 = V_4$. That is, assuming perfect matching between M_1, M_3 and M_4, the voltage at the gate of M_1 corresponds to the common mode of M_3 and M_4: $V_1 = (V_3 + V_4)/2 = V_{CMi}$. If the common-mode value V_{CMi} of input voltages V_3 and V_4 is not equal to V_1 the dc output characteristic has the same shape, but a dc level shift is applied to the curves of transistor currents in opposite directions of the horizontal axis.

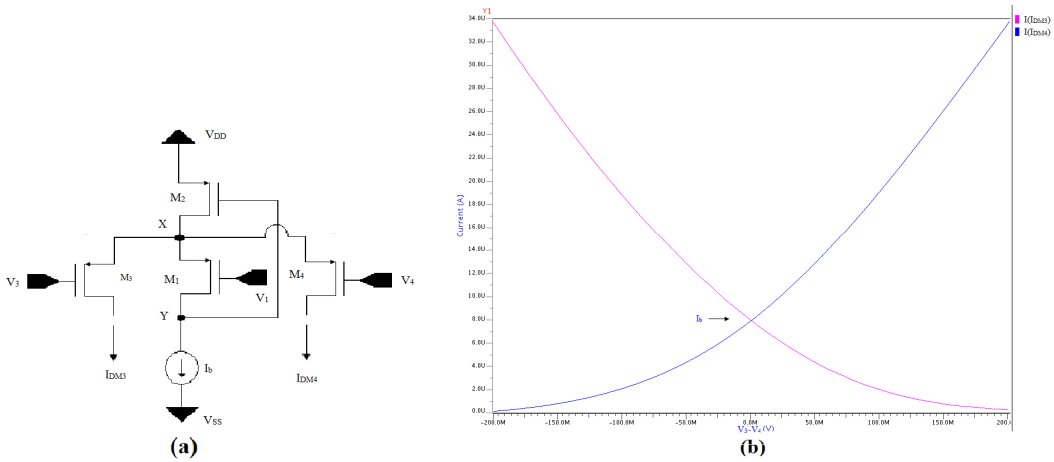


Figure 2.6: (a) Basic implements of FVFDP. (b) DC response of FVFDP.

The main difference between the DFVF and the FVFDP is that the latter has a true differential output. The output current of the DFVF can be large if $V_1 - V_3$ is positive and zero if $V_1 - V_3$ is negative, while in the FVFDP we can have positive or negative large differential output currents $(I_{out} = I_{DM3} - I_{DM4})$ depending on the value of the input differential voltage $(V_{in} = V_3 - V_4)$. This pseudo-differential pair can be also operated with a minimum supply voltage of $V_{DD}^{MIN} = |V_{TP}| + 2V_{DSsat}$, as in the cases of the FVFCS and DFVF [1].

2.6 Simulation results

2.6.1 Voltage follower

The circuit of voltage follower, shown in Figure 2.2, has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions are listed in Table 2.1. The values of input voltage (V_i), bias voltage (V_b), supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.25 V, 0.35 V, 0.9 V and 0 V respectively.

Table 2.1: Transistor dimension of voltage follower.

Transistor	W[µm]	L[µm]
M_1	15	0.2
M_2	13.9	0.2

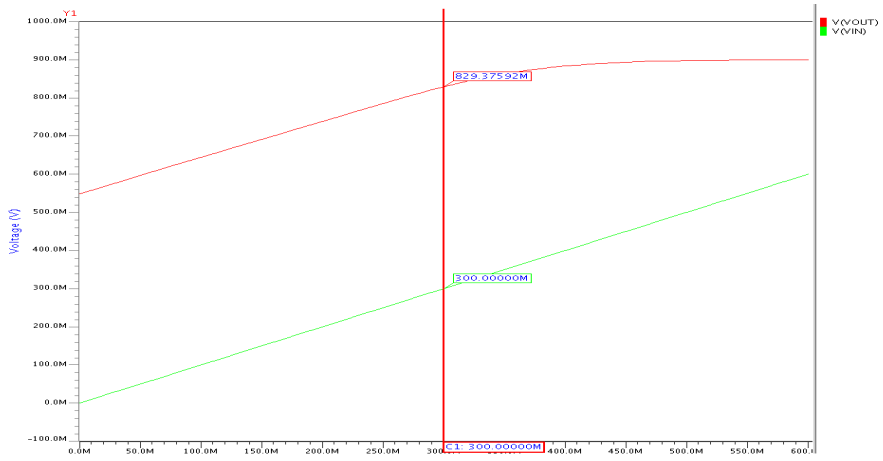


Figure 2.7: DC transfer characteristics of voltage follower.

The DC transfer characteristic of voltage follower is shown in Figure 2.7. The input voltage (V_i) is varied from 0 V to 0.6 V with increment of 0.01 V. Figure 2.7 shows that output of the voltage follower is varied linearly for the input voltage 0 V to 0.3 V. The frequency response of the voltage is shown in Figure 2.8. From figure 2.8, it can be seen that the bandwidth is over 100 MHz with load capacitance $C_L = 10$ fF. The total power consumption of voltage follower is 9.13 µW.

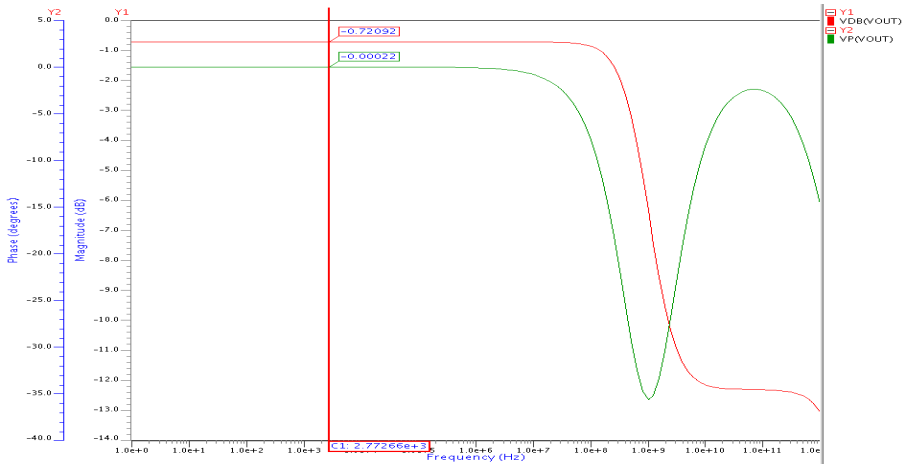


Figure 2.8: Frequency response of voltage follower.

2.6.2 Flipped voltage follower cell

The circuit of FVF cell, shown in Figure 2.3(a), has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions are listed in Table 2.2. The values of input voltage (V_i), bias voltage (V_b), supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.12 V, 0.7 V, 0.9 V and 0 V respectively.

Table 2.2: Transistor dimension of FVF Cell.

Transistor	W[µm]	L[µm]
M_1	110	2
M_2	17.8	2
M_3	0.5	0.5

The DC transfer characteristics of the FVF cell are shown in Figure 2.9. The input voltage (V_i) is varied from 0 V to 0.4 V with increment of 0.01 V with bias Voltage $V_b = 0.7$ V.

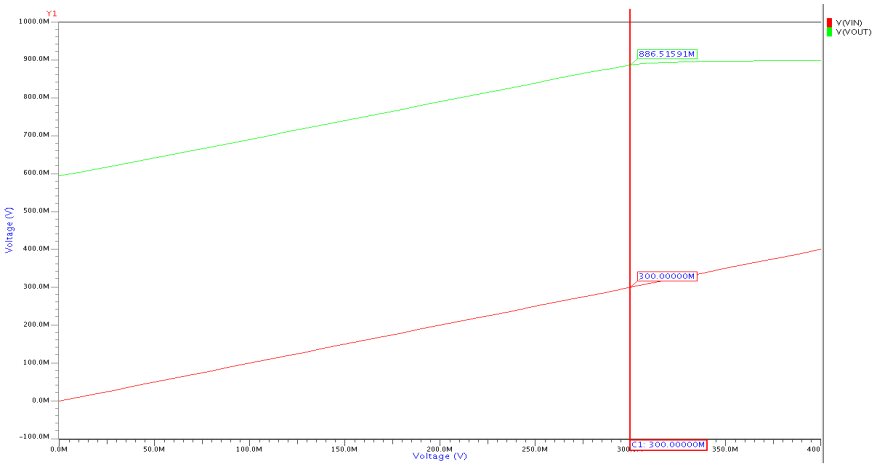


Figure 2.9: DC transfer characteristics of FVF cell.

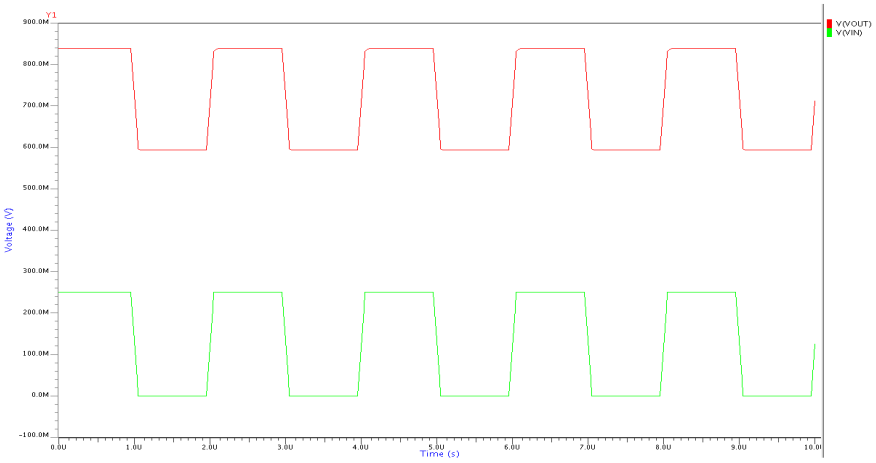


Figure 2.10: Transient response of FVF cell.

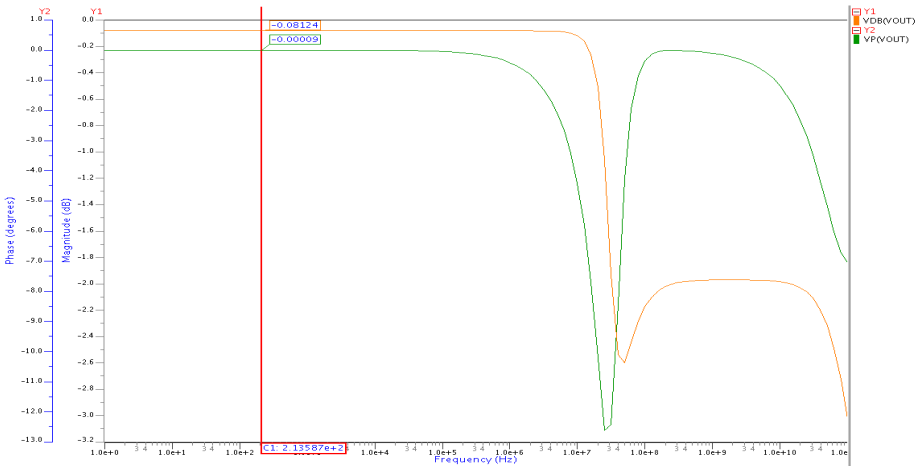


Figure 2.11: Frequency response of FVF cell.

Figure 2.9 shows that output of the FVF cell is varied linearly for the input voltage 0 V to 0.3 V. Figure 2.10 shows the transient response of FVF cell, where an input signal (V_i) of 0.25 V, 0.5 MHz is applied.

The frequency response of the FVF is shown in Figure 2.11. From Figure 2.11, it can be seen that the bandwidth is over 30 MHz with load capacitance $C_L = 10$ fF. The total power consumption of FVF cell is 7.16 µW.

2.7 Layout

Integrated Circuit (IC) Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, Layout is the process by which a circuit *specification* is converted to a *physical implementation* with enough information to deduce all the relevant physical parameters of the circuit. A layout engineer's job is to place and connect all the components that make up a chip so that they meet all criteria. Typical goals are performance, size, and manufacturability.

2.7.1 The role of layout in the design process

From a computer scientist's point of view, the layout process seems familiar enough. We are given a piece of *source code*, this time usually in terms of a circuit diagram, and we want to compile it to an *object code*, the physical layout of the circuit. The layout step is the last major step in the design process before testing and fabrication; it is the step which reveals to the designer all the subtle electrical characteristics of the clean and logical digital systems.

2.7.2 Tolerances and design rules

The layout must pass a series of checks in a process known as Verification. The two most common checks in the verification process are Design Rule Checking (DRC), and Layout Versus Schematic (LVS). When all verification is complete, the data is translated into an industry standard format, typically GDSII, and sent to a semiconductor foundry. The

process of sending this data to the foundry is called tape out, due to the fact the data used to be shipped out on a magnetic tape. The foundry converts the data into another format and uses it to generate the photo masks used in a photolithographic process of semiconductor device fabrication.

2.7.3 Design rule checking

Design rule checking of check(s) (DRC) is the area of Electronic Design Automation that determines whether a particular chip layout satisfies a series of recommended parameters called Design Rules. Design Rule Checking is a major step during Physical Verification of the design, which also involves LVS (Layout Versus Schematic) Check, XOR Checks, ERC (Electrical Rule Check) and Antenna Checks.

Design rules are a set of parameters provided by the semiconductor manufacturer that enable the designer to verify the correctness of the mask set. Design rules are specific to a particular semiconductor manufacturing process. A design rule set specifies a minimum size or spacing requirements between the layers of the same type or of different types.

This provides a safety margin for various process variations, to ensure that the design will still have reasonable performance after the circuit is fabricated. There is a limit to how small features the photolithographic process can generate. Generally, this *feature size* is the width of a single minimum-width polysilicon wire used as a transistor gate (since this is the most important physical circuit dimension in determining circuit speed).

2.7.4 Design rule checking (DRC) software

The main objective of design rule checking (DRC) is to achieve a high overall yield and reliability for the design. If the design rules are violated the design may not be functional. While design rule checks do not validate that the design will operate correctly, they are constructed to verify that the structure meets the process constraints for a given design type and process technology.

DRC software usually takes as input a layout in the GDSII standard format and a list of rules specific to the semiconductor process chosen for fabrication. From these it produces a report of design rule violations that the designer may or may not choose to correct.

DRC products define rules in a language to describe the operations needed to e performed in DRC. For example, Mentor Graphics uses Standard Verification Rule Format (SVRF) language in their DRC rules files.

Some example of DRC's in IC design includes:
Active to active spacing,
Well to well spacing,
Minimum channel length of the transistor,
Minimum metal width,
Metal to metal spacing,
ESD and I/O rules.

2.7.5 CMOS design rules

Basic Design Rules are:
(1) Size Rules.
(2) Separation Rules.
(3) Overlap Rules.

A listing of the design rules is available in the following file:
~cad/Mentor_tool/ASIC_Design_Kit/adk3_1/technology/ic/process/tsmc018.calibre.rules

The most important design rules are summarized below (all distances are *minimum*):

Polysilicon Region Width	2λ	Poly - Poly Spacing	2λ
Polysilicon Gate Extension	2λ	Diffusion Region Width	2λ
Diffusion – Diffusion Spacing	3λ	Contact Extension	1λ
Metal 1 width	3λ	Metal 1 spacing	3λ
Metal 2 Width	3λ	Metal 2 spacing	4λ
Via size	4λ		

2.7.6 Layout versus schematic (LVS)

The Layout Versus Schematic (LVS) is the class of electronic design automation (EDA) verification software that determines whether a particular integrated circuit layout corresponds to the original schematic of circuit diagram of the design.

A successful Design rule check (DRC) ensures that the layout conforms to the rules designed / required for faultless fabrication. However, it does not guarantee if it really represents the circuit you desire to fabricate. This is where an LVS check is used. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram. In most cases the layout will not pass LVS the first time requiring the layout engineer to examine the LVS software's reports and make changes to the layout.

2.8 Layout and post-layout of FVF cell

Layout of the FVF cell has been designed using tool IC Station Editor (Mentor Graphics) for tsmc 0.18 µm CMOS technology libraries. Layout diagram of multiplier based on FVF cell is shown in Figure 2.12. The Design Rule Check (DRC), Layout versus Schematic (LVS) and Post Extraction (PEX) checking has also been performed using tool Calibre (Mentor Graphics).

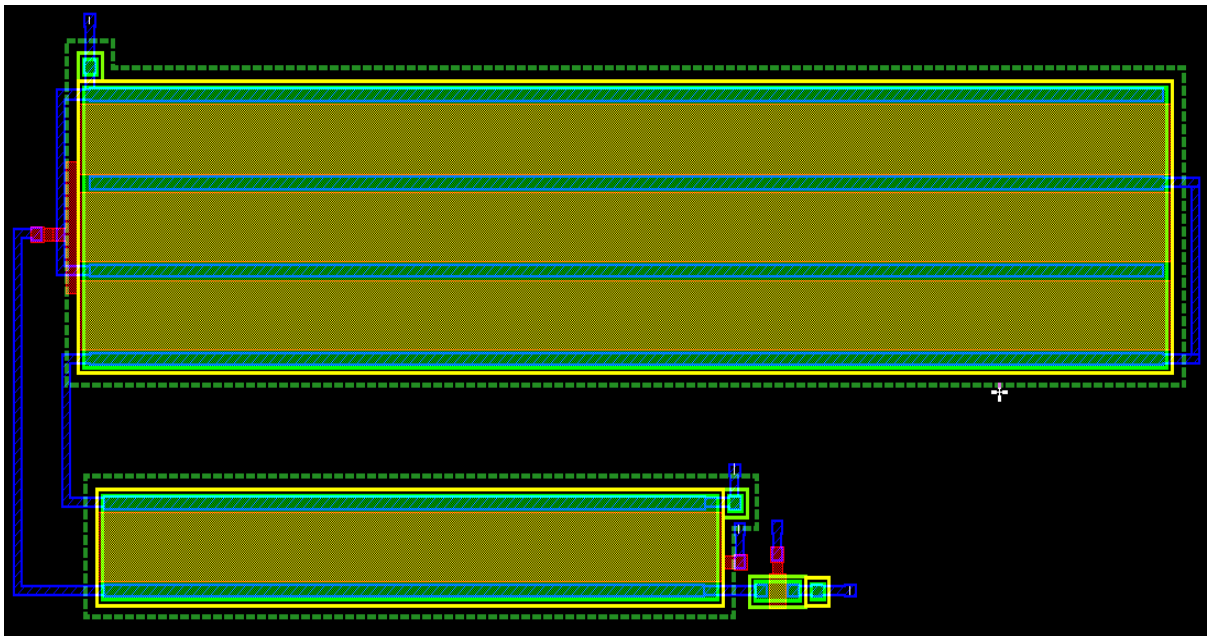
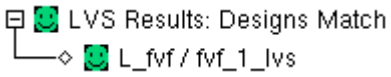


Figure 2.12: Layout of FVF cell.

2.8.1 Layout versus schematic and post extraction

The LVS and PEX have been performed. The LVS report, Source netlist and Layout netlist of FVF cell are generated using tool Calibre (Mentor Graphics) and given in

section 2.8.1.1, 2.8.1.2 and 2.8.1.3 respectively. From LVS report, it can be seen that the layout and schematic of FVF cell are matched.



2.8.1.1 LVS report of of FVF cell

```
##################################################
##                                              ##
##        C A L I B R E    S Y S T E M          ##
##                                              ##
##           L V S   R E P O R T                ##
##                                              ##
##################################################


REPORT FILE NAME:          L_fvf.lvs.report
LAYOUT NAME:               L_fvf.calibre.gds
SOURCE NAME:               /root/nidhi/600861003/fvf_1_lvs/fvf_1_lvs.src.net ('fvf_1_lvs')
RULE FILE:                 /root/nidhi/600861003/_tsmc018.rules_
LVS MODE:                  Mask
RULE FILE NAME:            /root/nidhi/600861003/_tsmc018.rules_
CREATION TIME:             Mon Jun  7 12:06:42 2010
CURRENT DIRECTORY:         /root/nidhi/600861003
USER NAME:                 root
CALIBRE VERSION:           v2006.2_30.26    Fri Jul  7 22:37:10 PDT 2006

******************************************************************************************
                          OVERALL COMPARISON RESULTS
******************************************************************************************

                      #       ###################
                    #         #                 #       ~   ~
                  #   #       #     CORRECT     #         |
                   # #        #                 #        \_/
                    #         ###################


------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               5         5

 Nets:                6         6

 Instances:           1         1          MN (4 pins)
                      4         2    *     MP (4 pins)
                 ------    ------
 Total Inst:          5         3


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                 Layout    Source          Component Type
                 ------    ------          --------------
 Ports:               5         5

 Nets:                6         6

 Instances:           1         1          MN (4 pins)
                      2         2          MP (4 pins)
                 ------    ------
 Total Inst:          3         3

       * = Number of objects in layout different from number in source.
```

2.8.1.2 Source netlist of FVF cell

```
* LVS netlist generated with ICnet by 'amit' on Sun May 30 2010 at 17:06:55
*
* Component pathname : /home/nidhi/600861003/fvf_1_lvs
*
.subckt fvf_1_lvs  vout vdd vi vin vss

        MN1 N$208 vi vss vss n L=0.5u W=0.5u
        MP2 N$208 vin vout vout p L=2u W=17.8u
        MP1 vout N$208 vdd vdd p L=2u W=110u
.ends fvf_1_lvs
```

2.8.1.3 Layout netlist of FVF cell

```
* File: L_fvf.pex.netlist
* Created: Mon Jun  7 14:06:14 2010
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.subckt L_FVF  VDD VIN VI VSS VOUT
*
mM0 VOUT VIN 3 VOUT p L=2.025e-06 W=1.7835e-05 AD=1.03133e-11 AS=1.03133e-11
mM1 VDD 3 VOUT VDD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.81541e-11
mM2 VOUT 3 VDD VDD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.98045e-11
mM3 VDD 3 VOUT VDD p L=2.025e-06 W=3.6675e-05 AD=1.81541e-11 AS=1.98045e-11
mM4 VSS VI 3 VSS n L=5.4e-07 W=5.4e-07 AD=2.673e-13 AS=2.673e-13
c_2 VDD 0 1.09174f
c_3 VIN 0 4.62036f
c_5 3 0 24.5871f
c_6 VI 0 0.1007f
c_7 VSS 0 0.027435f
c_8 VOUT 0 1.44661f
*
.include "L_fvf.pex.netlist.L_FVF.pxi"
*
.ends
*
*
```

CHAPTER

3

LOW-VOLTAGE CURRENT MIRROR BASED ON FVF CELL

3.1 Introduction

Current mirrors made by using active devices have come to be widely used in analog integrated circuits both as biasing elements and as load devices for amplifier stages. The use of current mirrors in biasing can result in superior insensitivity of circuit performance to variations in power supply and temperature. Current mirrors are frequently more economical than resistors in terms of the die area required to provide bias current of a certain value, particularly when the required value of bias current is small. When used as a load element in transistor amplifiers, the high incremental resistances of the current mirror results in high voltage gain at low-power supply voltages [8].

3.2 Current mirrors

3.2.1 General properties

A current mirror is an element with at least three terminals, as shown in Figure 3.1. The common terminal is connected to a power supply, and the input current source is connected to the input terminal. Ideally, the output current is equal to the input current multiplied by a desired current gain. If the gain is unity, the input current is reflected to the output, leading to the name *current mirror.* Under ideal conditions, the current-mirror gain is independent of input frequency, and the output current is independent of the voltage between the output and common terminals. Furthermore, the voltage between the input and common terminals is ideally zero because this condition allows the entire

supply voltage to appear across the input current source, simplifying its transistor-level design.

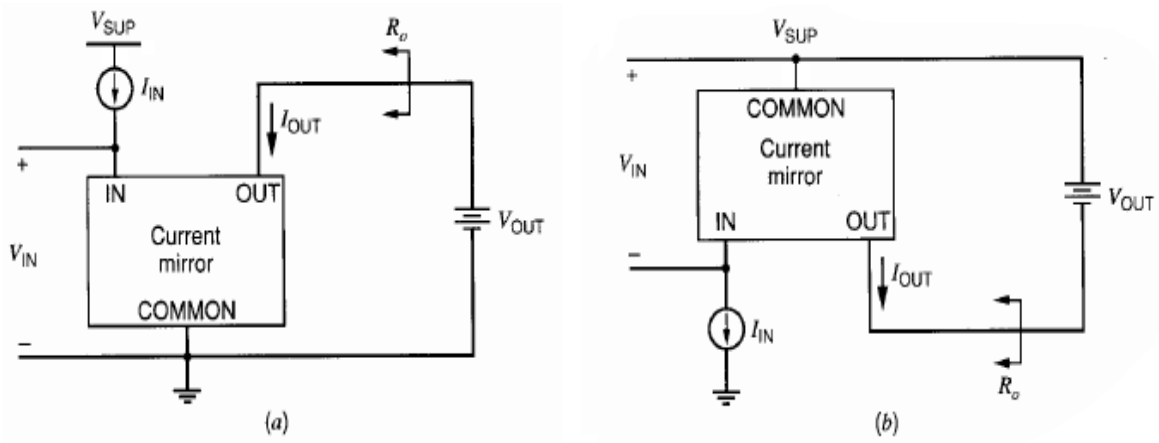


Figure 3.1: Current mirror block diagrams referenced to (a) ground and (b) the positive supply.

3.2.2 Simple current mirror

Figure 3.2 shows an MOS version of the simple current mirror. The drain-gate voltage of M_1 is zero; therefore, the channel does not exist at the drain, and the transistor operates in the saturation or active region if the threshold is positive. Although the principle of operation for MOS transistors does not involve forward biasing any diodes, M_1 is said to be diode connected in an analogy to the bipolar case. Assume that M_2 also operates in the active region and that both transistors have infinite output resistance. Then I_{D2} is controlled by V_{GS2}, which is equal to V_{GS1} by KVL. A KVL equation is at the heart of the operation of all current mirrors. The gate-source voltage of a given MOS transistor is usually separated into two parts: the threshold V_{TH}, and the overdrive V_{ov}. The overdrive for M_2 is

$$V_{ov} = V_{GS2} - V_{TH} = \sqrt{\frac{2I_{D2}}{k(W/L)_2}} \tag{3.1}$$

Since the transconductance parameter k is proportional to mobility, and since mobility falls with increasing temperature, the overdrive rises with temperature. But threshold falls with increasing temperature. From KVL

$$V_{GS2} = V_{TH} + \sqrt{\frac{2I_{D2}}{k(W/L)_2}} = V_{GS1} = V_{TH} + \sqrt{\frac{2I_{D1}}{k(W/L)_1}} \tag{3.2}$$

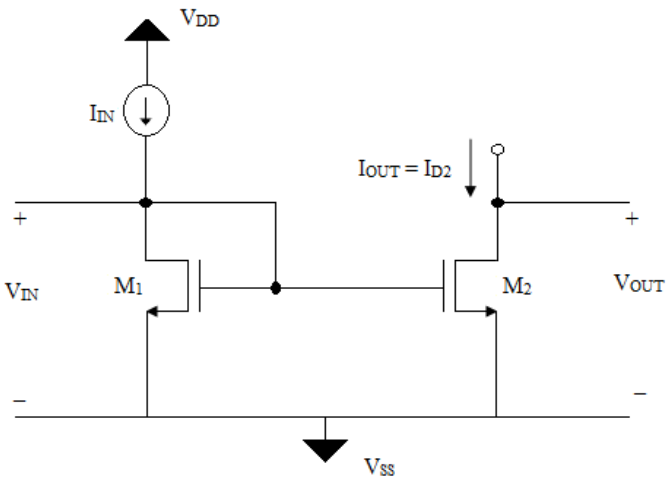


Figure 3.2: Simple MOS current mirror.

Equation (3.2) shows that the overdrive of M_2 is equal to that of M_1.

$$V_{ov2} = V_{ov1} = V_{ov} \tag{3.3}$$

If the transistors are identical, $(W/L)_2 = (W/L)_1$, and therefore

$$I_{OUT} = I_{D2} = I_{D1} \tag{3.4}$$

Equation (3.4) shows that the current that flows in the drain of M_1 is mirrored to the drain of M_2. Since $\beta_F \to \infty$ for MOS transistors, (3.4) and KCL at the drain of M_1 yield

$$I_{OUT} = I_{D2} = I_{IN} \tag{3.5}$$

Thus for identical devices operating in the active region with infinite output resistance, the gain of the current mirror is unity. This result holds when the gate currents are zero; that is, (3.5) is at least approximately correct for dc and low-frequency ac currents. As the input frequency increases, however, the gate currents of M_1 and M_2 increase because each transistor has a nonzero gate-source capacitance. The part of the input current that flows into the gate leads does not flow into the drain of M_1 and is not mirrored to M_2;

therefore, the gain of the current mirror decreases as the frequency of the input current increases. The rest of this section considers dc currents only.

In practice, the devices need not be identical. Then from (3.2) and (3.5),

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{D2} = \frac{(W/L)_2}{(W/L)_1} I_{IN} \tag{3.6}$$

Equation (3.6) shows that the gain of the current mirror can be larger or smaller than unity because the transistor sizes can be ratioed. To ratio the transistor sizes, either the widths or the lengths can be made unequal in principle. In practice, however, the lengths of M_1 and M_2 are rarely made unequal. The lengths that enter into (3.6) are the effective channel lengths and the effective channel length of a given transistor differs from its drawn length by offset terms stemming from the depletion region at the drain and lateral diffusion at the drain and source. Since the offset terms are independent of the drawn length, a ratio of two effective channel lengths is equal to the drawn ratio only if the drawn lengths are identical. As a result, a ratio of unequal channel lengths depends on process parameters that may not be well controlled in practice. Similarly, The effective width of a given transistor differs from the drawn width because of lateral oxidation resulting in a *bird's beak*. Therefore, a ratio of unequal channel widths will also be process dependent. In many applications, however, the shortest channel length allowed in a given technology is selected for most transistors to maximize speed and minimize area. In contrast, the drawn channel widths are usually many times larger than the minimum dimensions allowed in a given technology. Therefore, to minimize the effect of the offset terms when the current-mirror gain is designed to differ from unity, the widths are ratioed rather than the lengths in most practical cases. If the desired current-mirror gain is a rational number, M/N, the ratio is usually set by connecting M identical devices called *units* in parallel to form M_2 and N units in parallel to form M_1 to minimize mismatch arising from lithographic effects in forming the gate regions.

If a transistor is biased in the active region, its drain current actually increases slowly with increasing drain-source voltage. Figure 3.3 shows an output characteristic for M_2. The output resistance of the current mirror at any given operating point is the reciprocal of the slope of the output characteristic at that point. In the active region,

$$R_0 = r_{o2} = \frac{V_A}{I_{D2}} = \frac{1}{\lambda I_{D2}} \tag{3.7}$$

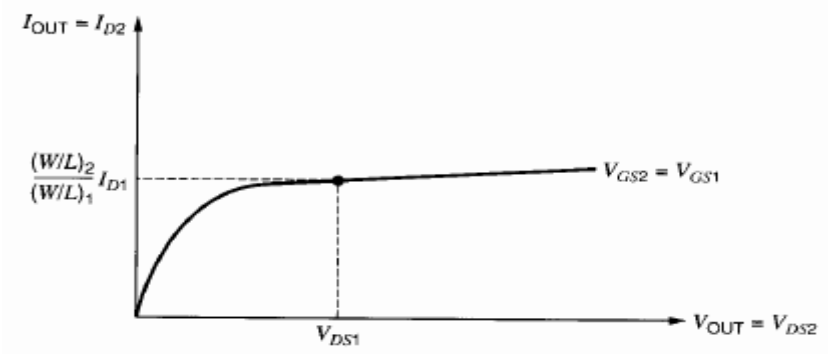


Figure 3.3: Output characteristic of simple MOS current mirror.

The point where $V_{DS2} = V_{DS1}$ and $V_{GS2} = V_{GS1}$ is labeled on the characteristic. Because the drain current is controlled by the gate-source and drain-source voltages, $I_{D2} = [(W/L)_2/(W/L)_1]I_{D1}$ at this point. If the slope of the characteristic in saturation is constant, the variation in I_{D2} for changes in V_{DS2} can be predicted by a straight line that goes through the labeled point. Extrapolation of the output characteristic in the active region back to the V_{DS2} axis gives an intercept at $-V_A = -1/\lambda$, where V_A is the Early voltage. If $V_A >> V_{DS1}$, the slope of the straight line is about equal to

$$I_{OUT} = \frac{(W/L)_2}{(W/L)_1} I_{IN}\left(1 + \frac{V_{DS2} - V_{DS1}}{V_A}\right) \tag{3.8}$$

Since the ideal gain of the current mirror is $(W/L)_2/(W/L)_1$, the systematic gain error, ε, of the current mirror can be calculated from (3.8).

$$\varepsilon = \frac{V_{DS2} - V_{DS1}}{V_A} \tag{3.9}$$

For example, if the drain-source voltage of M_1 is held at 1.2 V, and if the drain-source voltage of M_2 is 5 V, then the systematic gain error is (5 - 1.2)/10 = 0.38 with V_A = 10 V. Thus for a circuit operating at a power-supply voltage of 5 V, the current-mirror currents can differ by more than 35% from those values calculated by assuming that the transistor output resistance is infinite. Although ε stems from finite output resistance, it does not

depend on r_{o2} directly but instead on the drain-source and Early voltages. Since the Early voltage is independent of the bias current, this observation shows that changing the input bias current in a current mirror changes systematic gain error mainly through changes to the drain-source voltages.

For the simple MOS current mirror, the input voltage is

$$V_{IN} = V_{GS1} = V_{TH} + V_{ov1} = V_{TH} + V_{ov} \tag{3.10}$$

With square-law behavior, the overdrive in (3.10) is proportional to the square root of the input current.

Finally, the minimum output voltage required to keep M2 in the active region is

$$V_{OUT(\min)} = V_{ov2} = V_{ov} = \sqrt{\frac{2I_{OUT}}{k(W/L)_2}} \tag{3.11}$$

Equation (3.11) predicts that $V_{OUT(\min)}$ depends on the transistor geometry and can be made arbitrarily small in a simple MOS mirror. However, if the overdrive predicted by (3.11) is less than $2nV_T$, where $n = (1 + C_{js}/C_{ox})$ and V_T is a thermal voltage, the result is invalid except to indicate that the transistors operate in weak inversion. At room temperature with n = 1.5, $2nV_T$ = 78 mV [8].

If the transistors operate in weak inversion,

$$V_{OUT(\min)} \approx 3V_T \tag{3.12}$$

3.3 Low-voltage current mirror based on flipped voltage follower cell

The well known flipped voltage follower (FVF) cell has been employed for realizing low-voltage current mirrors. The minimum supply voltage requirement for the correct operation of the current mirror is equal to $V_{TH} + V_{DS,sat}$, making all of them compatible

with the minimum power supply voltage requirement of the modern signal processing systems.

A comparison of the performance of the current mirror based on FVF cell with that achieved by the conventional cascode current mirrors is performed in this chapter.

One of the most widely used current mirror topologies in low-voltage signal processing is the conventional cascode current mirror shown in Figure 3.4 [5].

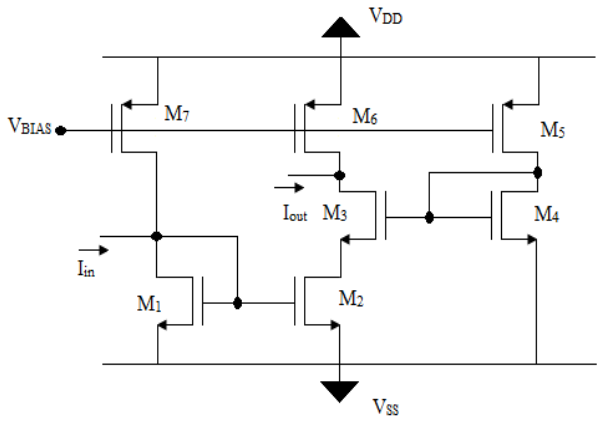


Figure 3.4: Low-voltage cascode current mirror.

With regards to the voltage restrictions, the minimum supply requirement is given by

$$V_{DD,\min} = V_{TH(M_1)} + V_{DS,sat(M_7)} \tag{3.13}$$

where $V_{TH(M_1)}$ is the threshold voltage of the M_1, and $V_{DS,sat(M_7)}$ is the saturation voltage of the M_7.

Other important factors that establish the capability of the current mirror in Figure 3.4 to operate in a low voltage environment are the minimum input and output voltages. The corresponding expression are given by (3.14) and (3.15), respectively

$$V_{in} = V_{TH(M_1)} \tag{3.14}$$

$$V_{out,\min} = V_{DS,sat(M_2)} + V_{DS,sat(M_3)} \tag{3.15}$$

The input and output resistances of the current-mirror in figure 3.4 are given by

$$R_{in} = \frac{1}{g_{m(M_1)}} \tag{3.16}$$

$$R_{out} = g_{m(M_3)}.r_{o(M_2)}.r_{o(M_3)} \tag{3.17}$$

An alternative topology of that shown in figure 3.4 is based on the adaptive bias scheme given in Figure 3.5.

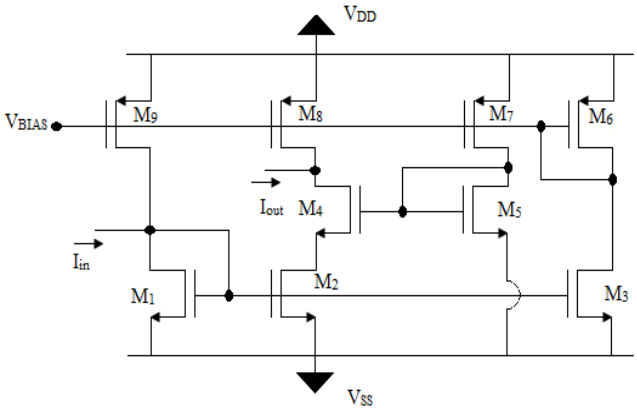


Figure 3.5: Cascode current mirror with adaptive bias scheme.

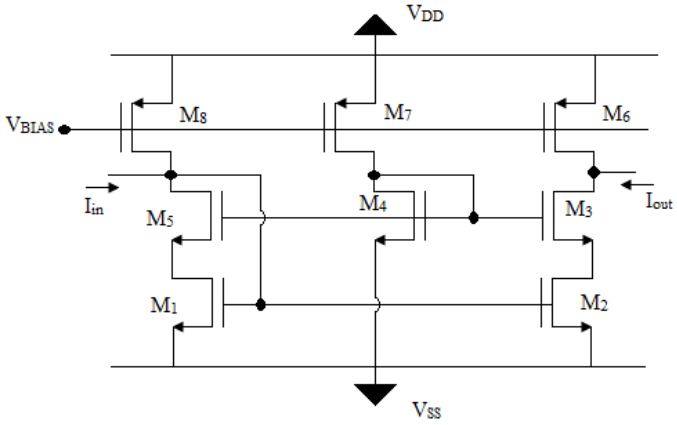


Figure 3.6: Low-voltage current mirror based on FVF cell.

The expressions given in (3.13)-(3.17) are still valid for the circuit in Figure 3.5. Another current mirror configuration that is widely used in low-voltage applications is that depicted in Figure 3.6. This is a cascode current mirror based on the FVF cell. The minimum required supply voltage and the minimum input voltage are also given by (3.13) and (3.14), while the minimum output voltage and output resistance are now [5].

$$V_{out} = V_{ds,sat(M_2)} + V_{DS,sat(M_3)} \tag{3.18}$$

$$R_{out} = g_{m(M_3)} r_{o(M_3)} r_{o(M_2)} \tag{3.19}$$

3.4 Simulation results

3.4.1 Cascode current mirror

The circuit of cascode current mirror, shown in Figure 3.4, has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions are listed in Table 3.1. The values of bias voltage (V_{BIAS}), supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.98 V, 1.5 V and 0 V respectively.

Table 3.1: Transistor dimensions of cascode current mirror.

Transistor	W[µm]	L[µm]
M_5- M_7	49	0.2
M_1 ,M_2, M_4	1.5	1.5
M_3	19	0.2

The frequency response of cascode current mirror is shown in Figure 3.7. From Figure 3.7, it can be seen that the bandwidth is less than 100 MHz with load capacitance $C_L = 500$ fF. The total power consumption of cascode current mirror is 105.9356 µW.

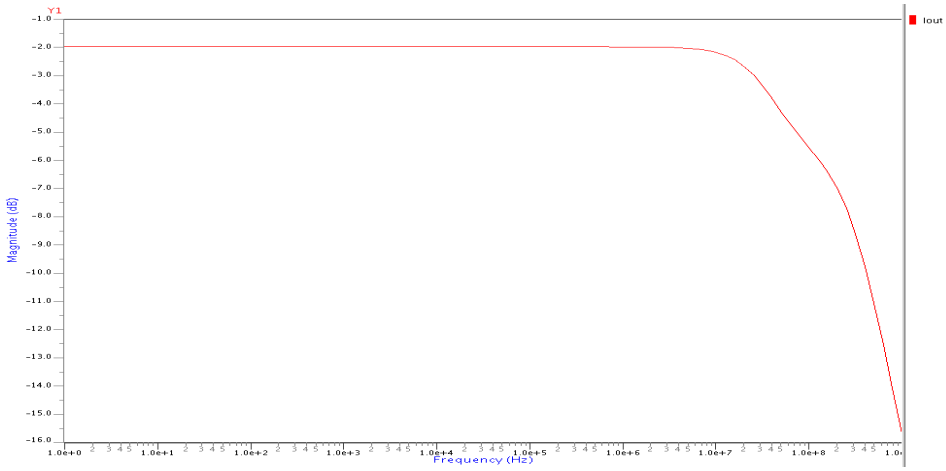


Figure 3.7: Frequency response of cascode current mirror.

Comparative results of the simulated performances between designed cascode current mirror and cascode current mirror in [5] are shown in Table 3.2

Table 3.2: Comparison of simulated performance between the designed cascode current mirror and cascode current mirror in [5].

Performance factor	Designed Cascode Current Mirror	Cascode Current Mirror [5]
Technology used (µm)	0.18	0.18
Supply used (V)	1.5	1.5
DC power dissipation (µW)	105.93	217
Cut-off frequency (MHz)	<100	133

3.4.2 Cascode current mirror with adaptive bias scheme

The circuit of cascode current mirror with adaptive bias scheme, shown in Figure 3.5, has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions are listed in Table 3.3. The values of bias voltage (V_{BIAS}), supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.98 V, 1.5 V and 0 V respectively.

The frequency response of cascode current mirror with adaptive bias scheme is shown in Figure 3.8. From Figure 3.8, it can be seen that the bandwidth is over 100 MHz with load capacitance $C_L = 500$ fF. The total power consumption of cascode current mirror with adaptive bias scheme is 185.53 µW.

Table 3.3: Transistor dimensions of cascode current mirror with adaptive bias scheme.

Transistor	W[µm]	L[µm]
M6- M9	49	0.2
M1 ,M2, M3,M5	1.5	1.5
M4	19	0.2

Comparative results of the simulated performances between designed cascode current mirror with adaptive bias scheme and cascode current mirror with adaptive bias scheme in [5] are shown in Table 3.4

Table 3.4: Comparison of simulated performance between the designed cascode current mirror with adaptive bias scheme and cascode current mirror with adaptive bias scheme in [5].

Performance factor	Designed cascode current mirror with adaptive bias scheme	Cascode current mirror with adaptive bias scheme [5]
Technology used (µm)	0.18	0.18
Supply used (V)	1.5	1.5
DC power dissipation (µW)	185.53	289
Cut-off frequency (MHz)	100	81

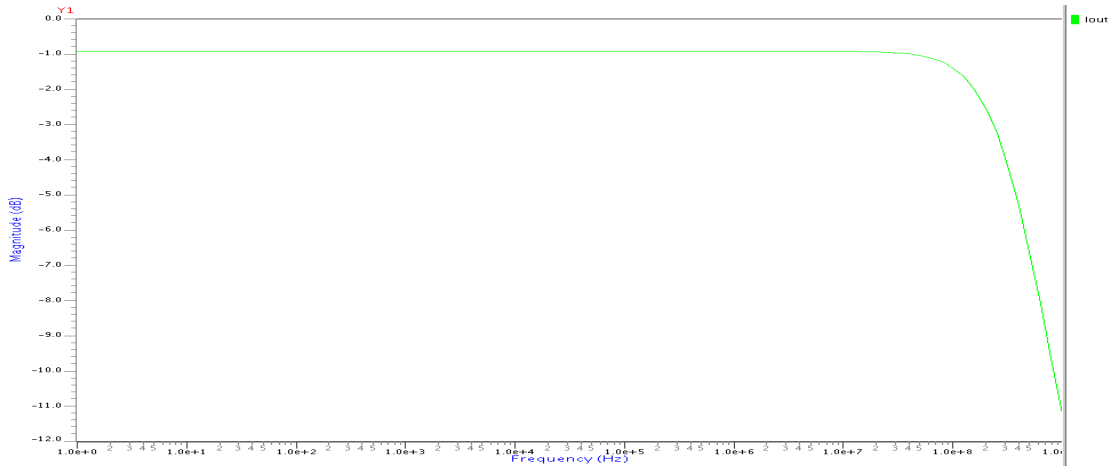


Figure 3.8: Frequency response of cascode current mirror with adaptive bias scheme.

3.4.3 Current mirror based on FVF cell

The circuit of current mirror based on FVF cell, shown in Figure 3.6, has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions are listed in Table 3.5. The values of bias voltage V_{BIAS}, supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.98 V, 1.5 V and 0 V respectively.

The frequency response of the current mirror based on FVF cell is shown in Figure 3.9. From Figure 3.9, it can be seen that the bandwidth is over 1000 MHz with load capacitance $C_L = 500$ fF. The total power consumption of FVF cell based current mirror is 107.01 µW.

Table 3.5: Transistor dimensions of current mirror based on FVF cell.

Transistor	W[µm]	L[µm]
M_6- M_8	49	0.2
M_1 ,M_2, M_4	1.5	1.5
M_3,M_5	19	0.2

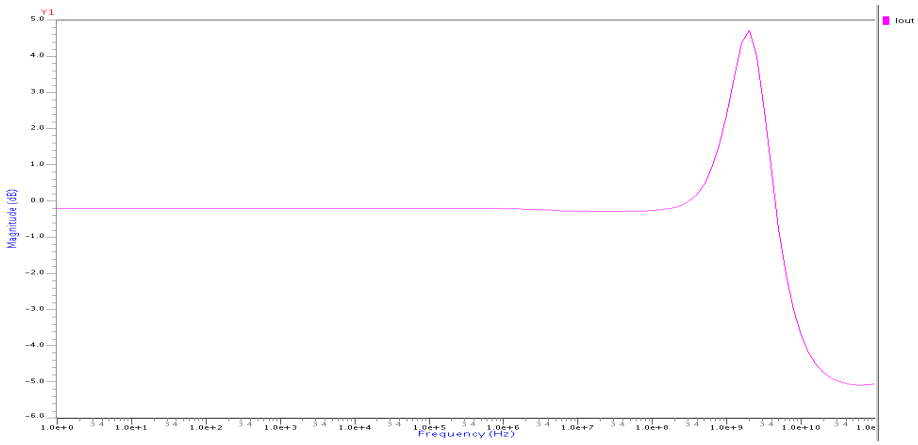


Figure 3.9: Frequency response of current mirror based on FVF cell.

Comparative results of the simulated performances between designed current mirror based on FVF cell and current mirror based on FVF cell in [5] are shown in Table 3.6

Table 3.6: Comparison of simulated performance between the designed current mirror with adaptive bias scheme and cascode current mirror with adaptive bias scheme in [5].

Performance factor	Designed current mirror based on FVF cell	current mirror based on FVF cell [5]
Technology used (µm)	0.18	0.18
Supply used (V)	1.5	1.5
DC power dissipation (µW)	185.53	218
Cut-off frequency (MHz)	1000	212

3.5 Layout of current mirror based on FVF cell

Layout of current mirror based on FVF cell has been designed using tool IC Station Editor (Mentor Graphics) for tsmc 0.18 µm CMOS technology libraries. Layout diagram of current mirror based on FVF cell is shown in Figure 3.10. The design rule check (DRC), layout versus schematic (LVS) and post extraction (PEX) checking has also been performed using tool Calibre (Mentor Graphics).

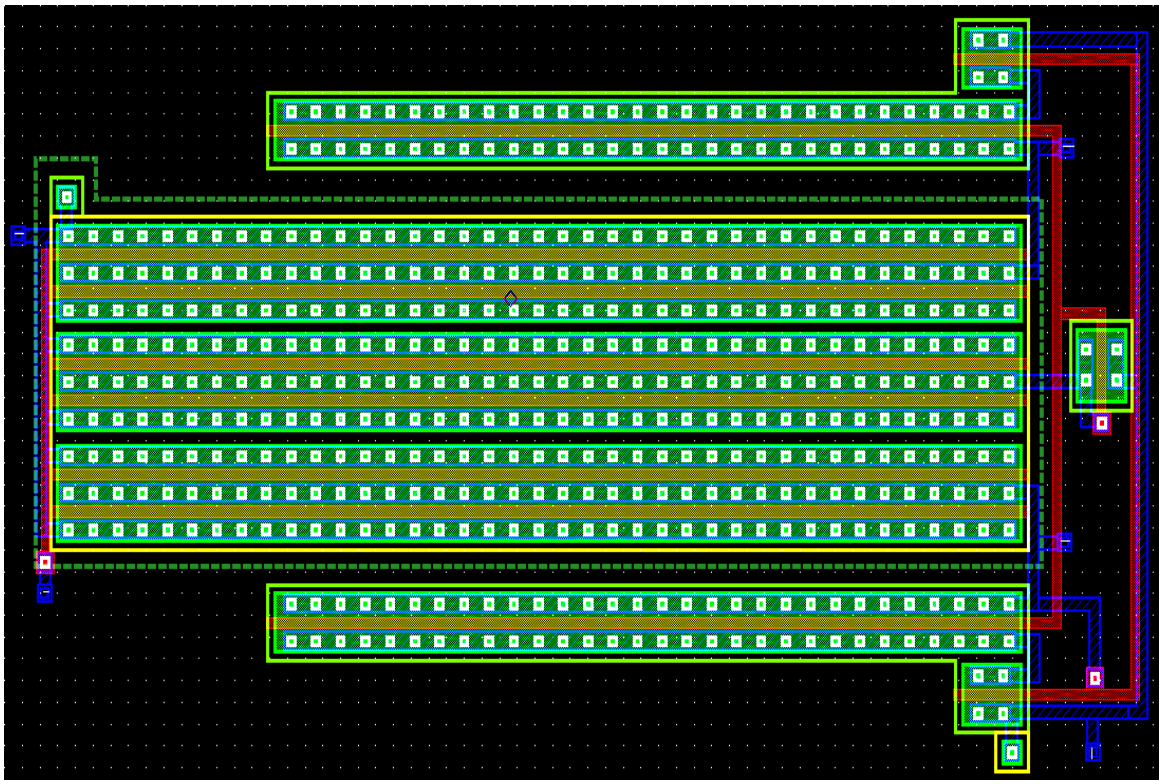
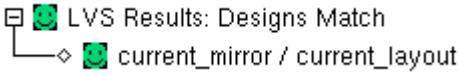


Figure 3.10: Layout of current mirror based on FVF cell.

3.5.1 Layout versus schematic and post extraction

The LVS and PEX have been performed. The LVS report, Source netlist and Layout netlist of current mirror based on FVF cell are generated using tool Calibre (Mentor Graphics) and given in section 3.5.1.1, 3.5.1.2 and 3.5.1.3 respectively. From LVS report, it can be seen that the layout and schematic of FVF cell are matched.



3.5.1.1 LVS report of current mirror based on FVF cell

```
##############################################
##                                          ##
##        C A L I B R E   S Y S T E M       ##
##                                          ##
##           L V S   R E P O R T            ##
##                                          ##
##############################################


REPORT FILE NAME:         current_mirror.lvs.report
LAYOUT NAME:              current_mirror.calibre.gds
SOURCE NAME:              /home/nidhi/600861003/current_layout/current_layout.src.net ('current_layout')
RULE FILE:                /root/_tsmc018.rules_
LVS MODE:                 Mask
RULE FILE NAME:           /root/_tsmc018.rules_
CREATION TIME:            Mon Jun 28 10:41:32 2010
CURRENT DIRECTORY:        /root
USER NAME:                root
CALIBRE VERSION:          v2006.2_30.26    Fri Jul  7 22:37:10 PDT 2006

****************************************************************************************************************
                          OVERALL COMPARISON RESULTS
****************************************************************************************************************

                    #       ###################       _   _
                  #         #                 #       *   *
                #   #       #     CORRECT     #         |
                 # #        #                 #       \___/
                  #         ###################


----------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              5         5

 Nets:               8         8

 Instances:          5         5          MN (4 pins)
                     6         3    *     MP (4 pins)
                ------    ------
 Total Inst:        11         8


NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source          Component Type
                ------    ------          --------------
 Ports:              5         5

 Nets:               6         6

 Instances:          1         1          MN (4 pins)
                     3         3          MP (4 pins)
                     2         2          SMN2 (4 pins)
                ------    ------
 Total Inst:         6         6


       * = Number of objects in layout different from number in source.
```

3.5.1.2 Source netlist of current mirror based on FVF cell

```
* LVS netlist generated with ICnet by 'root' on Mon Jun 28 2010 at 10:20:38
*
* Component pathname : /home/nidhi/600861003/current_layout
*
.subckt current_layout  Iout Iin vb vdd vss

        MN3 Iout N$4 N$414 vss n L=0.2u W=19u
        MN5 N$414 Iin vss vss n L=1.5u W=1.5u
        MN4 N$7 Iin vss vss n L=1.5u W=1.5u
        MN2 N$4 N$4 vss vss n L=1.5u W=1.5u
        MN1 Iin N$4 N$7 vss n L=0.2u W=19u
        MP3 Iout vb vdd vdd p L=0.2u W=49u
        MP2 N$4 vb vdd vdd p L=0.2u W=49u
        MP1 Iin vb vdd vdd p L=0.2u W=49u
.ends current_layout
```

3.5.1.3 Layout netlist of current mirror based on FVF cell

```
* File: current_mirror.pex.netlist
* Created: Mon Jun 28 10:32:56 2010
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.subckt CURRENT_MIRROR  VB VDD IOUT IIN VSS
*
mM0 IIN VB VDD VDD p L=2.25e-07 W=2.4525e-05 AD=1.32435e-11 AS=1.21399e-11
mM1 VDD VB IIN VDD p L=2.25e-07 W=2.4525e-05 AD=1.21399e-11 AS=1.32435e-11
mM2 6 VB VDD VDD p L=2.25e-07 W=2.4525e-05 AD=1.32435e-11 AS=1.21399e-11
mM3 VDD VB 6 VDD p L=2.25e-07 W=2.4525e-05 AD=1.21399e-11 AS=1.32435e-11
mM4 IOUT VB VDD VDD p L=2.25e-07 W=2.4525e-05 AD=1.32435e-11 AS=1.21399e-11
mM5 VDD VB IOUT VDD p L=2.25e-07 W=2.4525e-05 AD=1.21399e-11 AS=1.32435e-11
mM6 3 IIN VSS VSS n L=2.25e-07 W=1.485e-06 AD=7.35075e-13 AS=7.35075e-13
mM7 IIN 6 3 VSS n L=2.25e-07 W=1.899e-05 AD=9.40005e-12 AS=9.40005e-12
mM8 4 6 IOUT VSS n L=2.25e-07 W=1.899e-05 AD=9.40005e-12 AS=9.40005e-12
mM9 VSS IIN 4 VSS n L=2.25e-07 W=1.485e-06 AD=7.35075e-13 AS=7.35075e-13
mM10 VSS 6 6 VSS n L=2.25e-07 W=1.485e-06 AD=7.35075e-13 AS=7.35075e-13
c_4 VB 0 3.72807f
c_6 VDD 0 2.08103f
c_7 3 0 0.289385f
c_8 4 0 0.289385f
c_11 IOUT 0 0.634957f
c_14 6 0 1.67136f
c_18 IIN 0 1.21336f
c_20 VSS 0 0.253192f
*
.include "current_mirror.pex.netlist.CURRENT_MIRROR.pxi"
*
.ends
*
*
```

CHAPTER

4

LOW-VOLTAGE CMOS FOUR-QUADRANT ANALOG MULTIPLIER

4.1 Introduction

Analog circuits are designed to implement some of mathematical operations. Addition, subtraction, integration and differentiation are some of the simple operations compared to multiplication and division of analog signals. If both the inputs of multiplier can be either positive or negative, then it is called as four-quadrant multiplier circuit. The inputs and outputs can be either voltage or current.

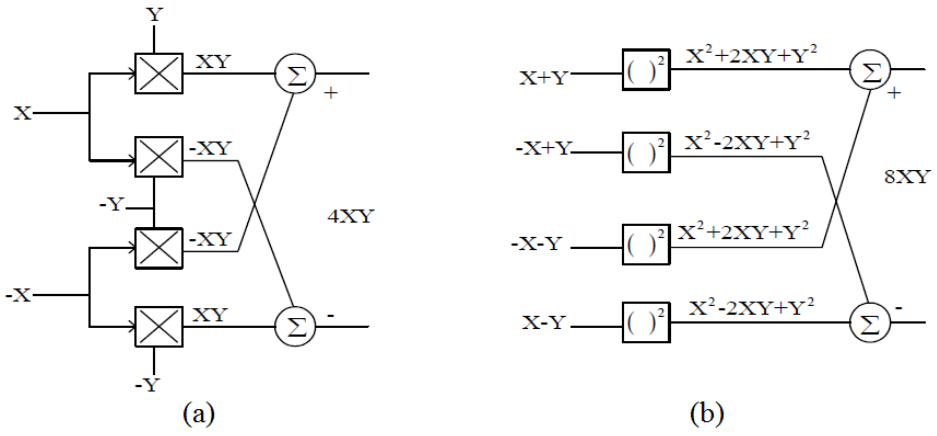


Figure 4.1: Nonlinearity cancellations in four- quadrant multiplier. (a) using four single quadrant multipliers (b) using square devices.

The ideal output of multiplier is related to its inputs by

$$V_{out} = kV_xV_y \tag{4.1}$$

K is the multiplier gain and V_x, V_y are voltage inputs of multiplier circuits.

In reality, the nonlinear characteristics of transistors results in offsets and nonlinearities.

Non ideal output of multiplier can be written as [10].

$$V_{out} = k(V_x + V_{osx})(V_y + V_{osy}) + V_{osout} + V_x^n + V_y^m \quad (4.2)$$

$V_{osx}, V_{osy}, V_{osout}$ are the offset voltages and V_x^n, V_y^m represent nonlinearities in the multiplier [11]. These nonlinearities in four-quadrant multipliers are cancelled by using four single quadrant multipliers or four squared devices as shown in the Figure 4.1.

Barrie Gilbert designed one of successful four-quadrant multiplier in 1968 using the characteristics of bipolar transistor [12]. From Gilbert BJT multiplier to recently designed MOS transconductors based multipliers different topologies of multipliers are proposed. Multipliers are classified based on its MOS region of operation [13]. One type is analog multiplier circuit based on square-law characteristics of MOS transistor and the other type is based on linear characteristics of MOS transistor. Most of these transconductance multipliers are further categorized based on type of non linearity cancellation methods used in each multiplier. In transconductance multipliers, non-linearities are cancelled either by single quadrant multipliers or squared devices as shown in Figure 4.1. In addition to these methods, current mode operation of multipliers is introduced.

Low voltage, low power, wide input range and linearity are the basic criteria in designing multipliers. CMOS multipliers are most widely used compared to BJT multipliers because CMOS multiplier gives low-power and low-voltage capabilities than BJT based multiplier. CMOS designs give low fabrication cost because of much widely used CMOS digital technology.

4.2 Multiplier classification

4.2.1 MOS multiplier operating in voltage saturation region

A simple multiplier configuration using four cross connected MOS transistors is shown in the Figure 4.2. All the four transistors M_1 - M_4 operate in triode region.

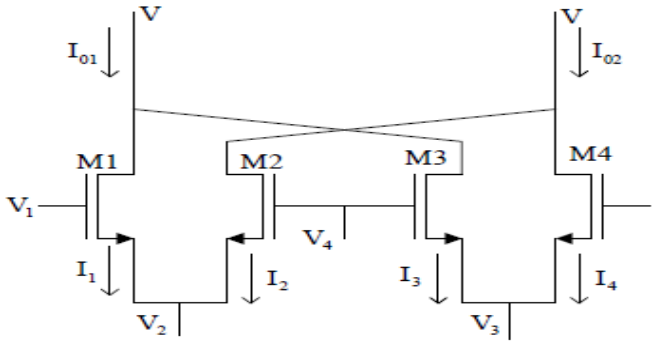


Figure 4.2: MOS multiplier with transistors M1-M4 operating in triode region.

For a NMOS transistor operating in triode region, the drain current (I) is

$$I = k\left(V_{GS} - V_T - V_{DS}/2\right)V_{DS} \tag{4.3}$$

where k is NMOS transconductance parameter

$$I_1 = k\left(V_1 - V_2 - V_T - \left(V - V_2\right)/2\right)\left(V - V_2\right) \tag{4.4}$$

$$I_2 = k\left(V_4 - V_2 - V_T - \left(V - V_2\right)\right)\left(V - V_2\right) \tag{4.5}$$

$$I_3 = k\left(V_4 - V_3 - V_T - \left(V - V_3\right)/2\right)\left(V - V_3\right) \tag{4.6}$$

$$I_4 = k\left(V_1 - V_3 - V_T - \left(V - V_3\right)/2\right)\left(V - V_3\right) \tag{4.7}$$

Output current I_0 of multiplier is given by

$$I_o = I_{o1} - I_{o2} = \left(I_1 + I_3\right) - \left(I_2 + I_4\right) \tag{4.8}$$

$$I_0 = k\left(V_1 - V_4\right)\left(V_2 - V_3\right) \tag{4.9}$$

These triode region multipliers are insensitive to the distributed effects in the channel, and that the four-transistor circuit itself possesses inherent compensation to such effects [14]. Because of better nonlinearity cancellation methods in this fully differential configuration, linearity and power supply rejection ratio (PSRR) are improved. But the inherent limitation of these multipliers is that all the drain voltages of MOS transistors

must be same, to achieve nonlinearity cancellation. An operational amplifier in the output can keep the drain voltages constant.

4.2.2 MOS multiplier operating in current saturation region

The topology shown in Figure 4.2 can also be used as if all the transistors work in current saturation region. The operating current (I) of a saturated NMOS transistor is given as

$$I = \frac{k}{2}(V_{GS} - V_T)^2 \tag{4.10}$$

The drain currents of M_1 - M_4 are

$$I_1 = \frac{k}{2}(V_1 - V_2 - V_T)^2 \tag{4.11}$$

$$I_2 = \frac{k}{2}(V_4 - V_2 - V_T)^2 \tag{4.12}$$

$$I_3 = \frac{k}{2}(V_4 - V_3 - V_T)^2 \tag{4.13}$$

$$I_4 = \frac{k}{2}(V_1 - V_3 - V_T)^2 \tag{4.14}$$

Output current I_o of multiplier is given by

$$I_o = I_{o1} - I_{o2} = (I_1 + I_3) - (I_2 + I_4) \tag{4.15}$$

$$I_0 = k(V_1 - V_4)(V_2 - V_3) \tag{4.16}$$

It is important to note that, the drain current of MOS transistor operating in saturation region is not controlled by drain voltage. Therefore drain voltages need not be equal for this multiplier configuration. Note that the above analysis neglects both channel length modulation (λ) and mobility reduction (θ). Moreover multipliers operating in saturation region have much higher frequency response than multiplier operating in triode region

[15]. Number of practical multiplier topologies is more in case of saturation region multipliers [13].

4.2.3 MOS multiplier based on translinear principle

A translinear circuit should have inputs and outputs in the form of currents and no voltages other than the junction voltages are involved [16]. Initial translinear (TL) circuits used exponential current-voltage characteristics of bipolar transistors. MOS translinear (MTL) circuits are designed using exponential I-V characteristics in subthreshold region. But dynamic range and speed of operation of such circuits are limited due to MOS transistors operating in weak inversion. The widely used MTL circuits are based on linear relationship between transconductance and voltage [17]. Compared to BTL circuits MTL circuits have less current range, bounded at low end by weak inversion and at high end by mobility reduction. But MTL circuits have better matching properties and zero gate leakage current. In MTL circuits all transistors operate in saturation region and generalized TL equation for loop connected MOS transistors is given by (4.17).

$$\sum_{CW}\sqrt{\frac{I_d}{W/L}} = \sum_{CCW}\sqrt{\frac{I_d}{W/L}} \tag{4.17}$$

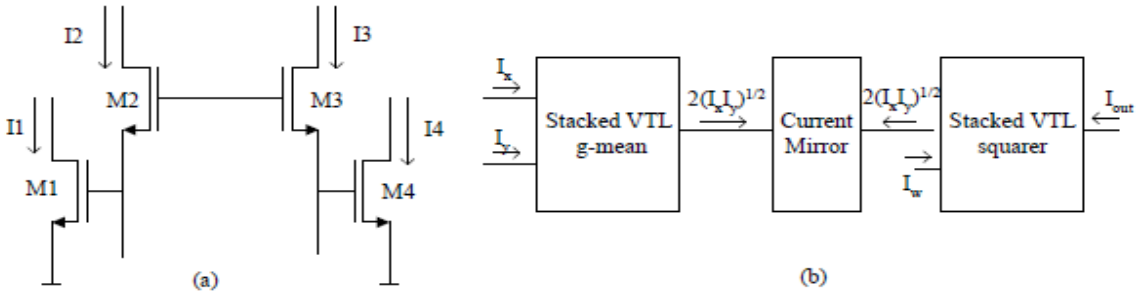


Figure 4.3: Voltage-translinear loop based (a) stacked topology (b) multiplier [22].

Many multipliers ([18], [19], [20]) are designed based on TL principle of MOS transistors. Figure 4.4 shows multiplier voltage translinear principle based multiplier block diagram and its blocks. The stacked VTL circuit gives geometric mean of input currents. Assuming identical transistors, W/L ratios of all transistors becomes same and equation (4.17) reduces to

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \tag{4.18}$$

Squaring on both sides gives

$$I_1 + I_2 + 2\sqrt{I_1 I_2} = I_3 + I_4 + 2\sqrt{I_3 I_4} \tag{4.19}$$

By forcing currents I_3 and I_4 equal to

$$I_3 = I_4 = \frac{I_1 + I_2 + 2I_z}{4} \tag{4.20}$$

I_z is copy of output current. Using equations (4.19), (4.20) and (4.21) I_z obtained as

$$I_z = \sqrt{I_1 I_2} \tag{4.21}$$

Geometric mean and squarer circuits are obtained from stacked topology by enforcing the conditions in equations (4.23) and (4.24).

$$I_1 = I_x \quad I_2 = I_y \quad I_3 = I_4 = I_x + I_y + I_z \tag{4.22}$$

$$4(W_1/L_1) = 4(W_2/L_2) = 4(W_3/L_3) = 4(W_4/L_4) \tag{4.23}$$

$$I_z = 2\sqrt{I_x I_y} \tag{4.24}$$

$$I_{out} = I_z^2 / I_w \tag{4.25}$$

As shown in Figure 4.3(b) first VTL circuit gives geometric mean of input currents as given by equation (4.24). This combined with squarer circuit and one more current input I_w implements multiplier functionality as given by

$$I_{out} = I_x I_y / I_w \tag{4.26}$$

TL based multipliers have high precision, wide current dynamic range (0.024% increase in slope of *THD* with input current) and insensitive to temperature and processing (less than 0.35% change in *THD* for -50^{o}C to 100^{o}C temperature change) [19]. The voltage

translinear principle based stacked and up-down topologies of multipliers [18] have small area (0.32 mm^2 for stacked topology and 0.24mm^2 for up-down topology), low power consumption, less complexity and low nonlinearity error (THD 1% and 1.5%). As shown in Figure 4.4, an improved configuration of multiplier [20] with reduced supply voltages and less *THD* is designed. With same (W/L) ratios for all transistors, the TL loop equation (4.18) modifies as follows:

$$\sqrt{I_1}+\sqrt{I_2}-\sqrt{\frac{k}{2}}(V_1+V_2)=\sqrt{I_3}+\sqrt{I_4}-\sqrt{\frac{k}{2}}(V_3+V_4) \tag{4.27}$$

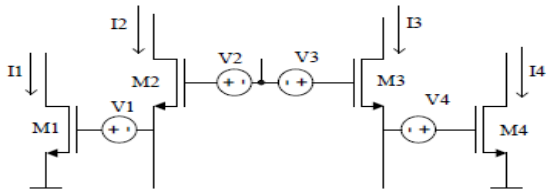


Figure 4.4: Voltage translinear loop with floating voltage sources.

where K is transconductance parameter. Condition $(V_1+V_2)=(V_3+V_4)$ has to be satisfied to get stacked VTL loop equations. This modified configuration also extends its dynamic range of the signals. But these multiplier configurations are single quadrant and have less frequency response at higher values of current gain.

4.2.4 MOS resistors

MOS implementation of resistors has many applications in analog signal processing. Tunable MOS resistors are used in active RC filters, controlled oscillators, variable gain amplifiers, or current and in variable resistive network synthesis [2]. Voltage controlled resistors or current controlled resistors are implemented by MOSFETs operating in linear, saturation region or sub-threshold region. Dependence of MOS resistance on threshold voltage limits tuning capability and injects substrate noise into the signal path and design becomes sensitive to process variations [22]. MOS resistors operating in linear region [23] have limited frequency response because of distributed channel capacitance in the triode region. Degree of nonlinearity is more pronounced especially for MOS control voltages close to threshold voltage. This prohibits application of MOS resistor to large signal applications [24].

MOS resistors using saturated transistors have wide resistance values (3.3 k to 67 kΩ) [25] as well as positive and negative resistance values (50 kΩ to ∞ and -50 kΩ to -∞) [26]. Figure 4.6 shows floating MOS resistor circuit with positive and negative resistance values. The output resistance of this configuration with equal input and output currents is given as

$$R = \frac{1}{2k(V_{c1} - V_{c2})} \tag{4.28}$$

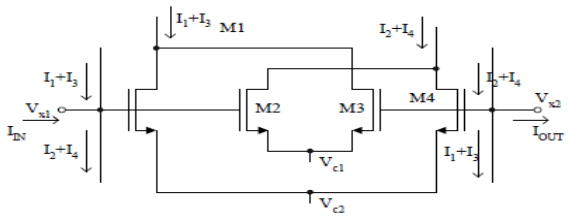


Figure 4.5: Floating MOS resistor circuit.

Where k is transconductance parameter and V_{c1}, V_{c2} are control voltages. Saturated MOS resistors have high frequency of response and many times resistors in active RC filters are replaced with MOS resistors [27]. Resistive networks are used for smoothing signals and filtering of noise. In resistive networks, number of resistors used is large. The important characteristics of MOS resistors are small area, less power consumption at the expense of precision. MOS transistors working in weak inversion are used in low precision resistive networks [22].

4.3 Four-quadrant analog multiplier based on FVF cell

A four-quadrant analog multiplier based on FVF cell is shown in Figure 4.6. The circuit is formed by combining simple common source amplifiers with a differential voltage controlled square rooting circuit. The approach leads to a four-quadrant analog multiplier with low complexity, low static power consumption and good linearity [7].

The multiplier based on FVF cell circuit formed by common source amplifiers $M_1 - M_4$ connected to a pair of differential-flipped voltage followers (DFVF), $M_5 - M_7$ and

$M_8 - M_{10}$. All the transistors are biased in the saturation region, the drain currents of M_1, M_2, M_3 and M_4 are given as:

$$I_{D1} = k_n (V_1 - V_{tn})^2 \tag{4.29a}$$

$$I_{D2} = k_n (V_1 - V_{tn})^2 \tag{4.29b}$$

$$I_{D3} = k_n (V_2 - V_{tn})^2 \tag{4.29c}$$

$$I_{D4} = k_n (V_2 - V_{tn})^2 \tag{4.29d}$$

From (4.29a) and (4.29b), we can write

$$I_{D1} = I_{D2}$$

And from (4.29c) and (4.29d), we can write

$$I_{D3} = I_{D4}$$

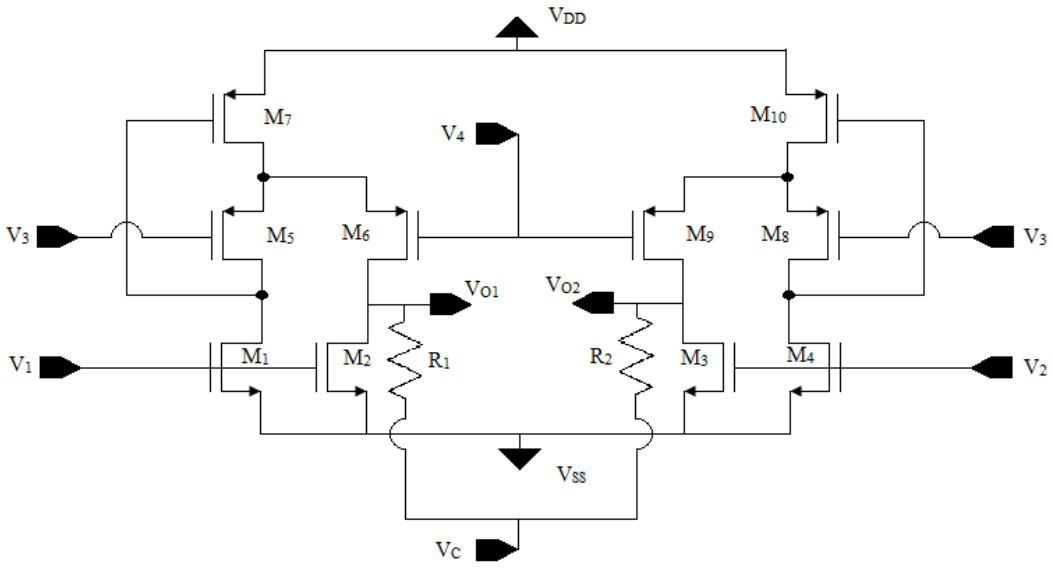


Figure 4.6: Multiplier based on FVF cell circuit [7].

where $k_n = 0.5\mu_n C_{OX} W/L$ is the transconductance parameter and V_{tn} is the threshold voltage of each n-channel MOSFET. To realise the multiplier balanced inputs are applied so $V_1 = V_{C1} + 0.5V_{12}$ and $V_2 = V_{C1} - 0.5V_{12}$. This yields

$$\sqrt{I_{D1}} - \sqrt{I_{D4}} = \sqrt{I_{D2}} - \sqrt{I_{D3}} = \sqrt{k_n V_{12}} \tag{4.30}$$

Where V_{12} is a differential input voltage with DC common mode V_{C1}. The nonlinear relation in (4.30) can be eliminated by injecting the output current into a square-rooting circuit, which will be described shortly. It can be seen from Figure 4.6 that I_{D1} is injected to be the bias current of the differential-FVF (DFVF) $M_5 - M_7$ and, similarly, the bias current of the differential-FVF $M_8 - M_{10}$ is obtained by injecting I_{D4} into the drain terminal of M_8. This results in $I_{D5} = I_{D1}$ and $I_{D8} = I_{D4}$.

Let us now focus on the differential-FVFs, which are incorporated to operate as a voltage-controlled square-rooting circuit. From the gate–source terminals arrangement we can observe that $V_3 - V_4 = V_{SG6} - V_{SG5} = V_{SG8} - V_{SG7}$. By applying the square law relation of a p-channel MOSFET, $I_D = k_p\left(V_{SG} - \left|V_{tp}\right|\right)^2$, and setting $V_3 = V_{c2} + 0.5V_{34}$ and $V_4 = V_{c2} - 0.5V_{34}$, we get:

$$I_{D6} = k_p\left(V_{id2} + \sqrt{\frac{I_{D1}}{k_p}}\right)^2 \tag{4.31}$$

$$I_{D8} = k_p\left(V_{id2} + \sqrt{\frac{I_{D4}}{k_p}}\right)^2 \tag{4.32}$$

Where V_{34} is also a differential input voltage with DC common mode V_{c2}. Considering the output nodes, the differential output voltage is $V_{out} = V_{o1} - V_{o2}$, where

$$V_{o1} = V_{C3} + \left(I_{D6} - I_{D2}\right)R \tag{4.33a}$$

$$V_{o2} = V_{C3} + \left(I_{D8} - I_{D3}\right)R \tag{4.33b}$$

V_{C3} is a reference common mode output voltage and R are load resistors. Substituting (4.31) and (4.32) into (4.33) and subtracting yields

$$V_{out} = 2R\sqrt{k_p}\left(\sqrt{I_{D1}} - \sqrt{I_{D4}}\right)V_{id2} \tag{4.34}$$

Finally, substituting (4.30) into (4.34) yields

$$V_{out} = 2R\sqrt{k_n k_p}V_{id1}V_{id2} \tag{4.35}$$

Thus, an offset-free analog multiplier is obtained. Its gain may be adjusted by the load resistor and the transconductance parameters.

4.4 Simulation results of multiplier based on FVF cell

The circuit of multiplier based on FVF cell, shown in Figure 4.6, has been simulated using tool ELDO (Mentor Graphics) for tsmc 0.18 µm CMOS technology. The transistor dimensions and selected design parameters are listed in Tables 4.1 and 4.2 respectively. The value of supply voltage (V_{DD}) and source voltage (V_{SS}) are chosen as 0.9 V and 0 V respectively.

Table 4.1: Transistor dimensions of multiplier based on FVF cell.

Transistor	W[µm]	L[µm]
M_1- M_4	0.5	0.5
M_5 ,M_6, M_8, M_9	17.8	2
M_7, M_{10}	110	2

Table 4.2: Various parameters of multiplier based on FVF cell.

Parameters	Values
$R_1 = R_2 = R$	4 kΩ
V_{C2}	0.12 V
V_{C1}	0.64 V
V_C	0.35 V

The DC transfer characteristics of the multiplier based on FVF cell is shown in Figure 4.7. The input voltages V_{12} is varied from -0.1 V to +0.1 V with the increment of 0.01 V and V_{34} is varied from -0.08 V to +0.08 V with the increment of 0.01 V. Figure 4.8 shows

the performance of the multiplier based on FVF cell as a balanced modulator where a 0.6 V, 300 MHz sinusoidal V_{id1} carrier signal is multiplied by a 0.6V, 25 MHz sinusoidal V_{id2} modulating signal.

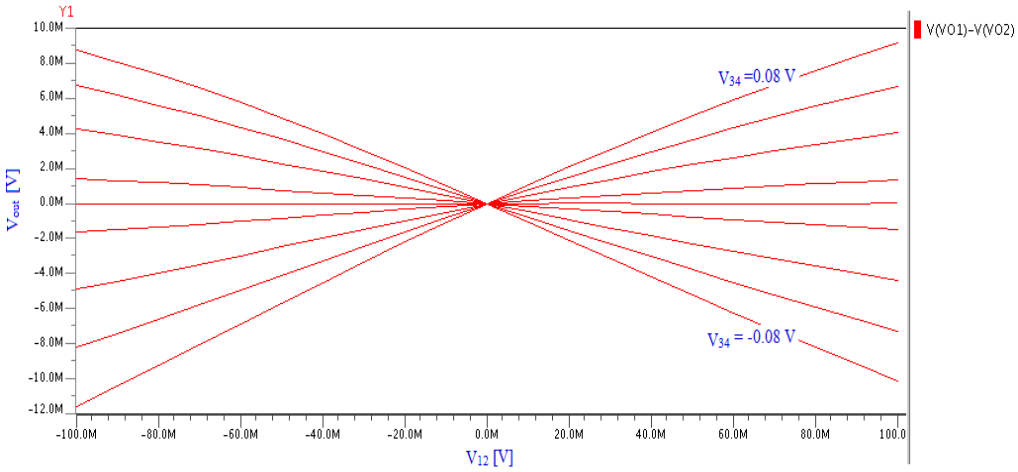


Figure 4.7: DC transfer characteristics of multiplier based on FVF cell.

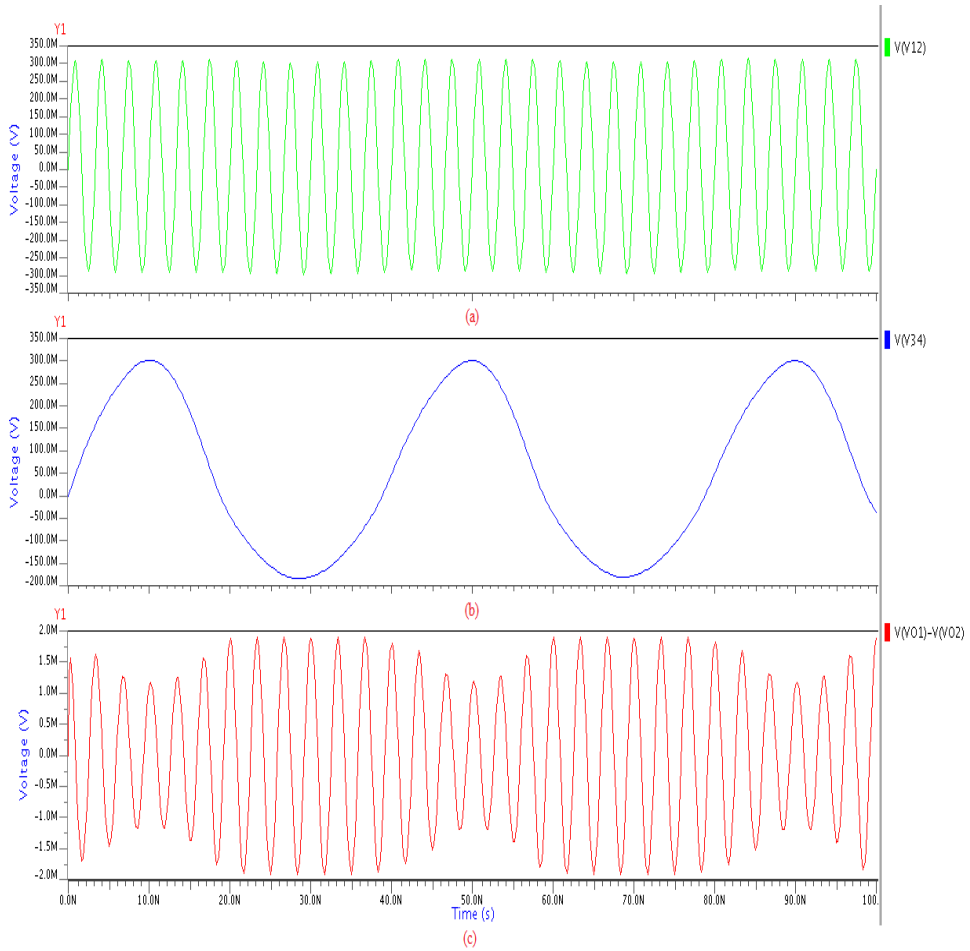


Figure 4.8 : (a) V_{12} sinusoidal. (b) V_{34} sinusoidal signal. (c) transient response of multiplier.

The frequency response of the multiplier is shown in Figure 4.9 for V_{34} =0 V, 0.02 V, 0.04 V, 0.06 V and 0.08V. From Figure 4.9, it can be seen that the circuit bandwidth is over 100 MHz. The quiescent power consumption of multiplier based on FVF is only 22.48 µW.

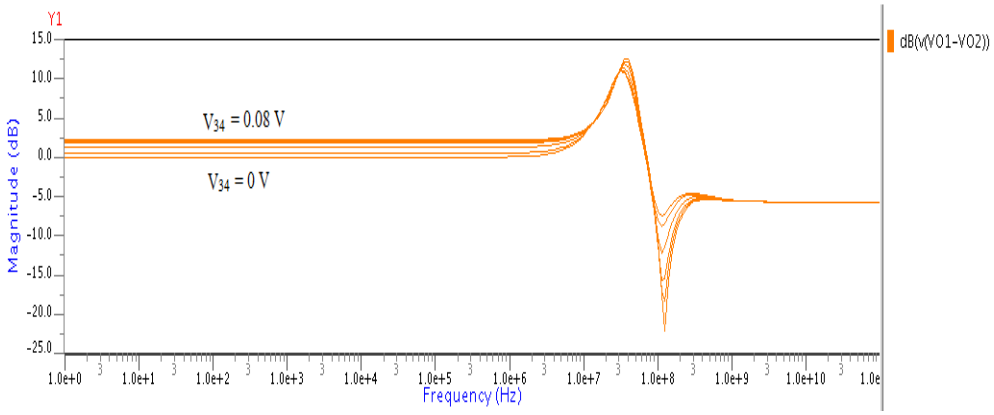


Figure 4.9: Frequency response of multiplier based on FVF cell.

Comparative results of the simulated performances between designed multiplier based on FVF cell and multiplier based on FVF cell in [7] are shown in Table 4.3

Table 4.3: Comparison of simulated performance between the designed multiplier based on FVF cell and multiplier based on FVF cell in [7].

Performance factor	Designed multiplier based on FVF cell	Multiplier based on FVF cell [7]
Technology used (µm)	0.18	0.35
Supply used (V)	0.9	1.8
DC power dissipation (µW)	22.48	200
Cut-off frequency (MHz)	100	100

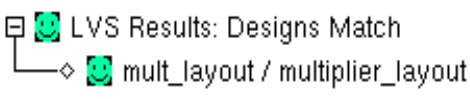
4.5 Layout and post-layout of multiplier based on FVF cell

Layout of the multiplier based on FVF cell has been designed using tool IC Station Editor (Mentor-Graphics) for tsmc 0.18 µm technology libraries. Layout diagram of multiplier based on FVF cell is shown in Figure 4.10. The design rule check (DRC), layout versus

schematic (LVS) and post extraction (PEX) checking has also been performed using Calibre tool (Mentor Graphics).

4.5.1 Layout versus schematic and post extraction

The LVS and PEX have been performed. The LVS report, Source netlist, and Layout netlist of multiplier based on FVF cell are generated using tool Calibre (Mentor Graphics) and given in section 4.5.1.1, 4.5.1.2 and 4.5.1.3, respectively. From LVS report, it can be seen that the layout and schematic of multiplier based on FVF cell are matched.



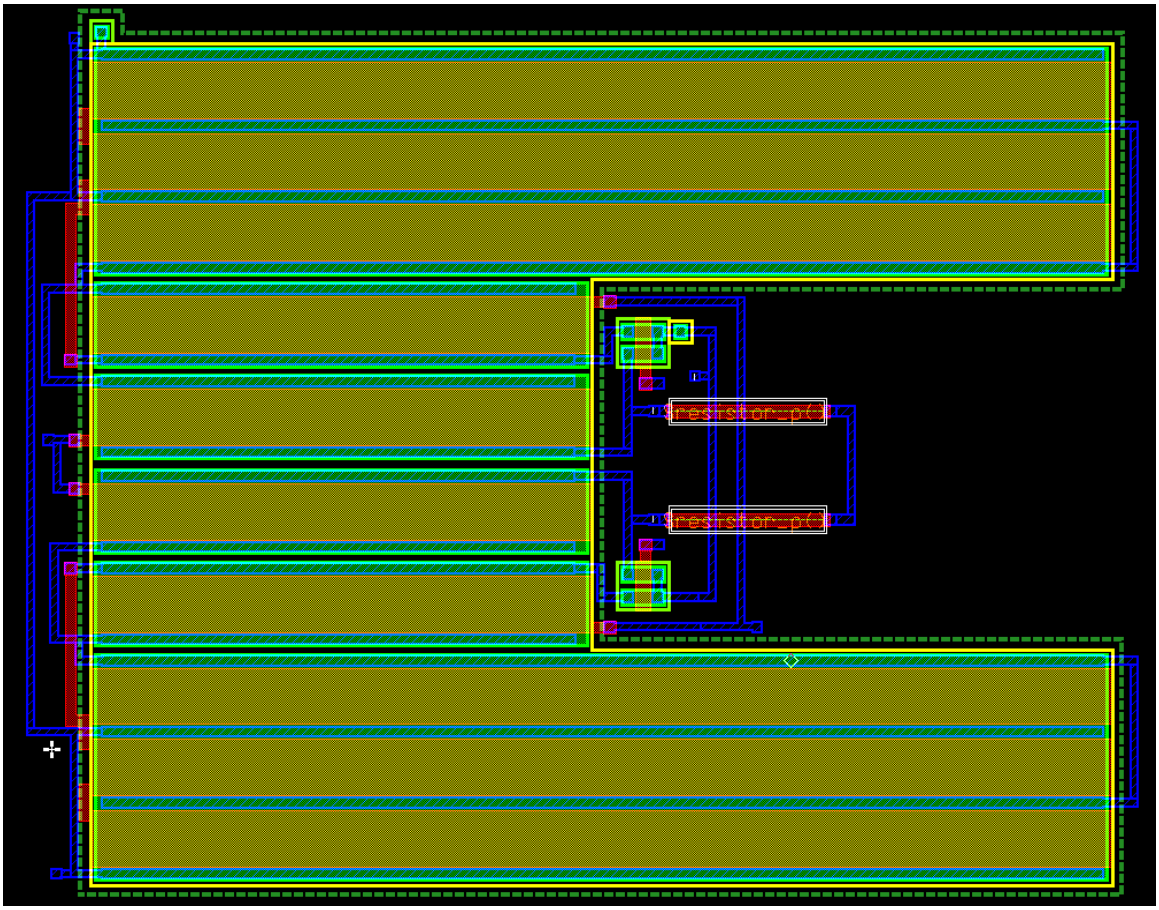


Figure 4.10: Layout of multiplier based on FVF cell.

4.5.1.1 LVS report of multiplier based on FVF cell

```
               ##################################################
               ##                                              ##
               ##          C A L I B R E    S Y S T E M        ##
               ##                                              ##
               ##              L V S   R E P O R T             ##
               ##                                              ##
               ##################################################


REPORT FILE NAME:         mult_layout.lvs.report
LAYOUT NAME:              mult_layout.calibre.gds
SOURCE NAME:              /home/nidhi/600861003/multiplier_layout/multiplier_layout.src.net ('multiplier_layout')
RULE FILE:                /root/_tsmc018.rules_
LVS MODE:                 Mask
RULE FILE NAME:           /root/_tsmc018.rules_
CREATION TIME:            Tue Jun  8 11:58:33 2010
CURRENT DIRECTORY:        /root
USER NAME:                root
CALIBRE VERSION:          v2006.2_30.26    Fri Jul  7 22:37:10 PDT 2006

**************************************************************************************************************
                               OVERALL COMPARISON RESULTS
**************************************************************************************************************


                       #       ###################       _   _
                      #        #                 #       *   *
                 #   #         #     CORRECT     #         |
                  # #          #                 #       \___/
                   #           ###################


--------------------------------------------------------------------------------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              9         9

 Nets:              13        13

 Instances:          4         4         MN (4 pins)
                    10         6    *    MP (4 pins)
                     2         2         R (2 pins)
                ------    ------
 Total Inst:        16        12

NUMBERS OF OBJECTS AFTER TRANSFORMATION
---------------------------------------

                Layout    Source         Component Type
                ------    ------         --------------
 Ports:              9         9

 Nets:              13        13

 Instances:          4         4         MN (4 pins)
                     6         6         MP (4 pins)
                     2         2         R (2 pins)
                ------    ------
 Total Inst:        12        12

       * = Number of objects in layout different from number in source.
```

4.5.1.2 Source netlist of multiplier based on FVF cell

```
* LVS netlist generated with ICnet by 'root' on Tue Jun  8 2010 at 11:57:51
*
* Component pathname : /home/nidhi/600861003/multiplier_layout
*
.subckt multiplier_layout  vd vo1 vo2 v1 v2 v3 v4 vr vss

        R2 vo2 vr hr 4k
        R1 vo1 vr hr 4k
        MN4 vo2 v2 vss vss n L=0.5u W=0.5u
        MP6 vo2 v4 N$216 vd p L=2u W=17.8u
        MN3 N$217 v2 vss vss n L=0.5u W=0.5u
        MP5 N$217 v3 N$216 vd p L=2u W=17.8u
        MP4 N$216 N$217 vd vd p L=2u W=110u
        MN2 vo1 v1 vss vss n L=0.5u W=0.5u
        MP3 vo1 v4 N$211 vd p L=2u W=17.8u
        MN1 N$212 v1 vss vss n L=0.5u W=0.5u
        MP2 N$212 v3 N$211 vd p L=2u W=17.8u
        MP1 N$211 N$212 vd vd p L=2u W=110u
.ends multiplier_layout
```

4.5.1.3 Layout netlist of multiplier based on FVF cell

```
* File: mult_layout.pex.netlist
* Created: Tue Jun  8 12:09:56 2010
* Program "Calibre xRC"
* Version "v2006.2_30.26"
*
.subckt MULT_LAYOUT  V4 VD V1 V2 VO1 VO2 VSS V3 VR
*
mM0 3 V3 12 VD p L=2.025e-06 W=1.782e-05 AD=8.8209e-12 AS=8.8209e-12
mM1 VO1 V4 12 VD p L=2.025e-06 W=1.782e-05 AD=8.8209e-12 AS=8.8209e-12
mM2 13 V4 VO2 VD p L=2.025e-06 W=1.782e-05 AD=8.8209e-12 AS=8.8209e-12
mM3 13 V3 4 VD p L=2.025e-06 W=1.782e-05 AD=8.8209e-12 AS=8.8209e-12
mM4 12 3 VD VD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.81541e-11
mM5 VD 3 12 VD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.98045e-11
mM6 12 3 VD VD p L=2.025e-06 W=3.6675e-05 AD=1.81541e-11 AS=1.98045e-11
mM7 VD 4 13 VD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.81541e-11
mM8 13 4 VD VD p L=2.025e-06 W=3.6675e-05 AD=1.98045e-11 AS=1.98045e-11
mM9 VD 4 13 VD p L=2.025e-06 W=3.6675e-05 AD=1.81541e-11 AS=1.98045e-11
mM10 VSS V1 3 VSS n L=5.4e-07 W=5.4e-07 AD=2.673e-13 AS=2.673e-13
mM11 VSS V1 VO1 VSS n L=5.4e-07 W=5.4e-07 AD=2.673e-13 AS=2.673e-13
mM12 VSS V2 VO2 VSS n L=5.4e-07 W=5.4e-07 AD=2.673e-13 AS=2.673e-13
mM13 VSS V2 4 VSS n L=5.4e-07 W=5.4e-07 AD=2.673e-13 AS=2.673e-13
rR14 VO1 VR 3868.35
rR15 VO2 VR 3868.35
c_1 V4 0 7.95464f
c_4 VD 0 2.39591f
c_7 3 0 24.5584f
c_10 4 0 24.5584f
c_11 V1 0 0.14466f
c_12 V2 0 0.14466f
c_13 VO1 0 0.33055f
c_14 VO2 0 0.33055f
c_15 VSS 0 0.17484f
c_16 V3 0 8.14966f
c_17 VR 0 0.101395f
c_19 12 0 1.63091f
c_21 13 0 1.63742f
*
.include "mult_layout.pex.netlist.MULT_LAYOUT.pxi"
*
.ends
*
*
```

CHAPTER

5

CONCLUSION

In this Thesis, a cell called as Flipped Voltage Follower is designed and simulated. This cell is used to implement few analog circuits such as current mirror and four-quadrant analog multiplier. These circuits have been simulated using Mentor Graphics IC Design Architect tool using standard tsmc 0.18 μm CMOS technology. The layout diagrams of FVF cell, current mirror, and multiplier have been designed using Mentor Graphics IC Station Editor tool. The post-simulation of these circuits have also been performed and simulation results have been compared with the existing circuits.

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APPENDIX A

MOSIS SPICE LEVEL – 53 MOS MODEL PARAMETERS FOR A STANDARD N-WELL CMOS TECHNOLOGY

This appendix includes the SPICE BSIM3v3 Version 3.1 MOS model parameters for TSMC 0.18 μm CMOS process.

(A) MODEL PARAMETERS FOR N-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 2.3549E17	VTH0 = 0.3725327
+K1 = 0.5933684	K2 = 2.050755E-3	K3 = 1E-3
+K3B = 4.5116437	W0 = 1E-7	NLX = 1.870758E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 1.3621338	DVT1 = 0.3845146	DVT2 = 0.0577255
+U0 = 259.5304169	UA = -1.413292E-9	UB = 2.229959E-18
+UC = 4.525942E-11	VSAT = 9.411671E4	A0 = 1.7572867
+AGS = 0.3740333	B0 = -7.087476E-9	B1 = -1E-7
+KETA = -4.331915E-3	A1 = 0	A2 = 1
+RDSW = 111.886044	PRWG = 0.5	PRWB = -0.2
+WR = 1	WINT = 0	LINT = 1.701524E-8
+XL = 0	XW = -1E-8	DWG = -1.365589E-8
+DWB = 1.045599E-8	VOFF = -0.0927546	NFACTOR = 2.4494296
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 3.175457E-3	ETAB = 3.494694E-5
+DSUB = 0.0175288	PCLM = 0.7273497	PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3	PDIBLCB = -0.1	DROUT = 0.7779462
+PSCBE1 = 3.488238E10	PSCBE2 = 6.841553E-10	PVAG = 0.0162206
+DELTA = 0.01	RSH = 6.5	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11

+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 8.53E-10	CGSO = 8.53E-10	CGBO = 1E-12
+CJ = 9.513993E-4	PB = 0.8	MJ = 0.3773625
+CJSW = 2.600853E-10	PBSW = 0.8157101	MJSW = 0.1004233
+CJSWG = 3.3E-10	PBSWG = 0.8157101	MJSWG = 0.1004233
+CF = 0	PVTH0 = -8.863347E-4	PRDSW = -3.6877287
+PK2 = 3.730349E-4	WKETA = 6.284186E-3	LKETA = -0.0106193
+PU0 = 16.6114107	PUA = 6.572846E-11	PUB = 0
+PVSAT = 1.112243E3	PETA0 = 1.002968E-4	PKETA = -2.906037E-3

(B) MODEL PARAMETERS FOR P-MOS TRANSISTORS.

+VERSION = 3.1	TNOM = 27	TOX = 4.1E-9
+XJ = 1E-7	NCH = 4.1589E17	VTH0 = -0.3948389
+K1 = 0.5763529	K2 = 0.0289236	K3 = 0
+K3B = 13.8420955	W0 = 1E-6	NLX = 1.337719E-7
+DVT0W = 0	DVT1W = 0	DVT2W = 0
+DVT0 = 0.5281977	DVT1 = 0.2185978	DVT2 = 0.1
+U0 = 109.9762536	UA = 1.325075E-9	UB = 1.577494E-21
+UC = -1E-10	VSAT = 1.910164E5	A0 = 1.7233027
+AGS = 0.3631032	B0 = 2.336565E-7	B1 = 5.517259E-7
+KETA = 0.0217218	A1 = 0.3935816	A2 = 0.401311
+RDSW = 252.7123939	PRWG = 0.5	PRWB = 0.0158894
+WR = 1	WINT = 0	LINT = 2.718137E-8
+XL = 0	XW = -1E-8	DWG = -4.363993E-8
+DWB = 8.876273E-10	VOFF = -0.0942201	NFACTOR = 2
+CIT = 0	CDSC = 2.4E-4	CDSCD = 0
+CDSCB = 0	ETA0 = 0.2091053	ETAB = -0.1097233
+DSUB = 1.2513945	PCLM = 2.1999615	PDIBLC1 = 1.238047E-3

+PDIBLC2 = 0.0402861	PDIBLCB = -1E-3	DROUT = 0
+PSCBE1 = 1.034924E10	PSCBE2 = 2.991339E-9	PVAG = 15
+DELTA = 0.01	RSH = 7.5	MOBMOD = 1
+PRT = 0	UTE = -1.5	KT1 = -0.11
+KT1L = 0	KT2 = 0.022	UA1 = 4.31E-9
+UB1 = -7.61E-18	UC1 = -5.6E-11	AT = 3.3E4
+WL = 0	WLN = 1	WW = 0
+WWN = 1	WWL = 0	LL = 0
+LLN = 1	LW = 0	LWN = 1
+LWL = 0	CAPMOD = 2	XPART = 0.5
+CGDO = 6.28E-10	CGSO = 6.28E-10	CGBO = 1E-12
+CJ = 1.160855E-3	PB = 0.8484374	MJ = 0.4079216
+CJSW = 2.306564E-10	PBSW = 0.842712	MJSW = 0.3673317
+CJSWG = 4.22E-10	PBSWG = 0.842712	MJSWG = 0.3673317
+CF = 0	PVTH0 = 2.619929E-3	PRDSW = 1.0634509
+PK2 = 1.940657E-3	WKETA = 0.0355444	LKETA = -3.037019E-3
+PU0 = -1.0227548	PUA = -4.36707E-11	PUB = 1E-21
+PVSAT = -50	PETA0 = 1E-4	PKETA = -5.167295E-3