Thesis Report

on

"Ultra Low Power Low Pass Active CMOS Filter Design For Biomedical Application"

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DECLARATION

I hereby certify that the work, which is being presented in this thesis entitled "**Ultra-Low Power Low-Pass Active CMOS Filter Design for Biomedical Applications**", in partial fulfillment of the requirement for the award of Master of Technology in VLSI Design at Thapar University, Patiala is an authentic record of my own work carried out under the supervision of Dr. Alpana Agarwal, Associate Professor, ECED and refers other researcher's work which are duly listed in reference section.

The matter embodied in this thesis has not been submitted for the award of any other degree of this or any other university.

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It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

04/06/12

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Abstract

Ultra low power with biomedical frequency low-pass filters has many applications in sensor interfaces and biomedical signal processing units. Biomedical signals are usually of 10-mHz to 100-Hz frequency range and hence require subhertz frequency filters to condition the signal before processing. The performance of filters designed by the use of passive components degrades at audio frequencies and the required resistances and inductances values calculated from the mathematical expression are very difficult to meet from the market. To find a solution to this problem is a study to realize Passive Filters into Active Filters using Operational Transconductance Amplifier (OTA).

For example, the low pass filter using OTA presented here was designed as part of the breathing monitoring device presented in (although it is not restricted to this use). However, despite their utility, creating large time constant low-pass filters on-chip is a challenging problem. To implement large time constants, switched-capacitor-based topologies require large capacitor ratios, and a sufficiently high power supply must be used to achieve an acceptably low switch
ON-resistance.

In g_m/C-based topologies, the cutoff frequency is generally determined by ratio *gm/C*, where *C* is the integrating capacitance present. However, area limitations restrict the maximum capacitance that accomplish here by MIM capacitor on-chip to picofarad values, limiting the minimum cutoff that can be achieved. Larger *gm* and *C* values must be used to keep the output current above this limit but at the cost of power consumption.

The aim of this work is to determine values of the design parameters that optimize an objective feature whereas satisfying specifications or constraints. This first-order low-pass filter topology is capable of providing cutoff frequencies down to 143 mHz with power consumption of 4.712 nW. The circuit is implemented in a 0.18-μm technology with a 1-V supply In terms of power consumption and cutoff frequency this filter performs better than previous filters from the literature.

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Chapter 1

Introduction

An electrical filter is a circuit that can be designed to modify, reshape or reject all unwanted frequencies of an electrical signal and accept or pass only those signals wanted by the circuits designer. In other words they "filter-out" unwanted signals and an ideal filter will separate and pass sinusoidal input signals based upon their frequency.

Filters are networks that process signals in a frequency-dependent manner. The basic concept of a filter can be explained by examining the frequency dependent nature of the impedance of capacitors and inductors. Consider a voltage divider where the shunt leg is reactive impedance. As the frequency is changed, the value of the reactive impedance changes as a result voltage divider ratio changes. This mechanism yields the frequency dependent change in the input/output transfer function that is defined as the frequency response.

An example of this is a radio receiver, where the signal you wish to process is passed through, typically with gain, while attenuating the rest of the signals. In data conversion, filters are also used to eliminate the effects of aliases in A/D systems. They are used in reconstruction of the signal at the output of a D/A as well, eliminating the higher frequency components, such as the sampling frequency and its harmonics, thus smoothing the waveform.

Filters have many practical applications. A simple, single pole, low-pass filter (the integrator) is often used to stabilize amplifiers by rolling off the gain at higher frequencies where excessive phase shift may cause oscillations.

A simple, single pole, high pass filter can be used to block DC offset in high gain amplifiers or single supply circuits. Filters can be used to separate signals, passing those of interest, and attenuating the unwanted frequencies.

There are a large number of texts dedicated to filter theory. No attempt will be made to go heavily into much of the underlying math: Laplace transforms, complex conjugate poles and the like, although they will be mentioned.

While they are appropriate for describing the effects of filters and examining stability, in most cases examination of the function in the frequency domain is more illuminating.

An ideal filter will have an amplitude response that is unity (or at a fixed gain) for the frequencies of interest (called the pass band) and zero everywhere else (called the stop-band). The frequency at which the response changes from pass-band to stop-band is referred to as the cut-off frequency.

1.1 Types of filter

Filters can be divided into two distinct types:

1.1.4 Based on Component used:

Based on the component used, filters can be divided into two types

A. Active filters
B. Passive filters.

Active filters contain amplifying devices to increase signal strength while passive do not contain amplifying devices to strengthen the signal. As there are two passive components within a passive filter design the output signal has smaller amplitude than its corresponding input signal, therefore passive RC filters attenuate the signal and have a gain of less than one, (unity).

A Low Pass Filter can be a combination of capacitance, inductance or resistance intended to produce high attenuation above a specified frequency and little or no attenuation below that frequency. The frequency at which the transition occurs is called the "cut-off" frequency. The simplest low pass filters consist of a resistor and capacitor but more sophisticated low pass filters have a combination of series inductors and parallel capacitors.

In low frequency applications (up to 100kHz), **passive filters** are usually made from simple RC (Resistor-Capacitor) networks while higher frequency filters (above 100kHz) are usually made from RLC (Resistor-Inductor-Capacitor) components. Passive filters are made up of passive components such as resistors, capacitors and inductors and have no amplifying elements (transistors, op-amps, etc) so have no signal gain, therefore their output level is always less than the input.

1.1.5 Based on frequency of signals they allow to pass through them:

Based on frequency of signals they allow to pass through them, filters can be divided into following categories:

A. Low Pass Filter:

There are **Low-pass filters** that allow only low frequency signals to pass. Where f_c is cut off frequency.

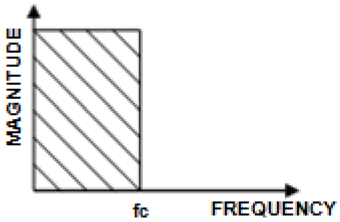


Fig 1.1 Low pass Filter characteristic [11]

An ideal low-pass filter completely eliminates all frequencies above the cut-off frequency while passing those below unchanged, its frequency response is a rectangular function. The transition region present in practical filters does not exist in an ideal filter. An ideal low-pass filter can be realized mathematically (theoretically) by multiplying a signal by the rectangular function in the frequency domain or, equivalently, convolution with its impulse response, a sinc function, in the time domain.

However, the ideal filter is impossible to realize without also having signals of infinite extent in time, and so generally needs to be approximated for real ongoing signals, because the sinc function's support region extends to all past and future times. The filter would therefore need to have infinite delay, or knowledge of the infinite future and past, in order to perform the convolution. It is effectively realizable for pre-recorded digital signals by assuming extensions of zero into the past and future, or more typically by making the signal repetitive and using Fourier analysis.

B. High-Pass Filters:

High-pass filters that allow only high frequency signals to pass through.

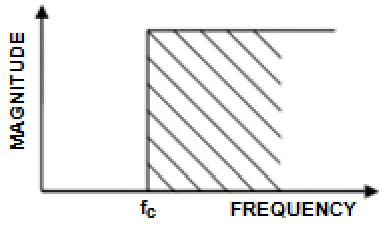


Fig 1.2 High pass filter characteristic[11]

C. Band-Pass Filters

Band pass filter that allow signals falling within a certain frequency range to pass through. If a high-pass filter and a low-pass filter are cascaded, a bandpass filter is created. The bandpass filter passes a band of frequencies between a lower cut-off frequency, f_l, and an upper cut-off frequency, f_h. Frequencies below f_l and above f_h are in the stop-band.

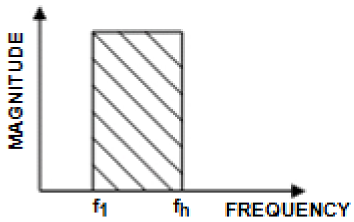


Fig 1.3 Band pass filter characteristic[11]

D. Band Reject Filter:

A complement to the bandpass filter is the bandreject, or notch filter. Here, the pass bands include frequencies below f_l (lower cut-off frequency) and above f_h (upper cut-off frequency) .The band from f_l to f_h is in the stop-band.

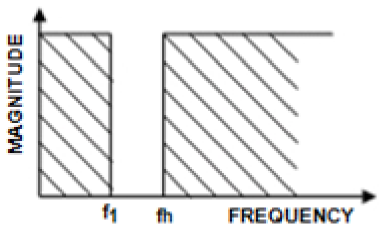


Fig 1.4 Band rejcet filter characteristic[11]

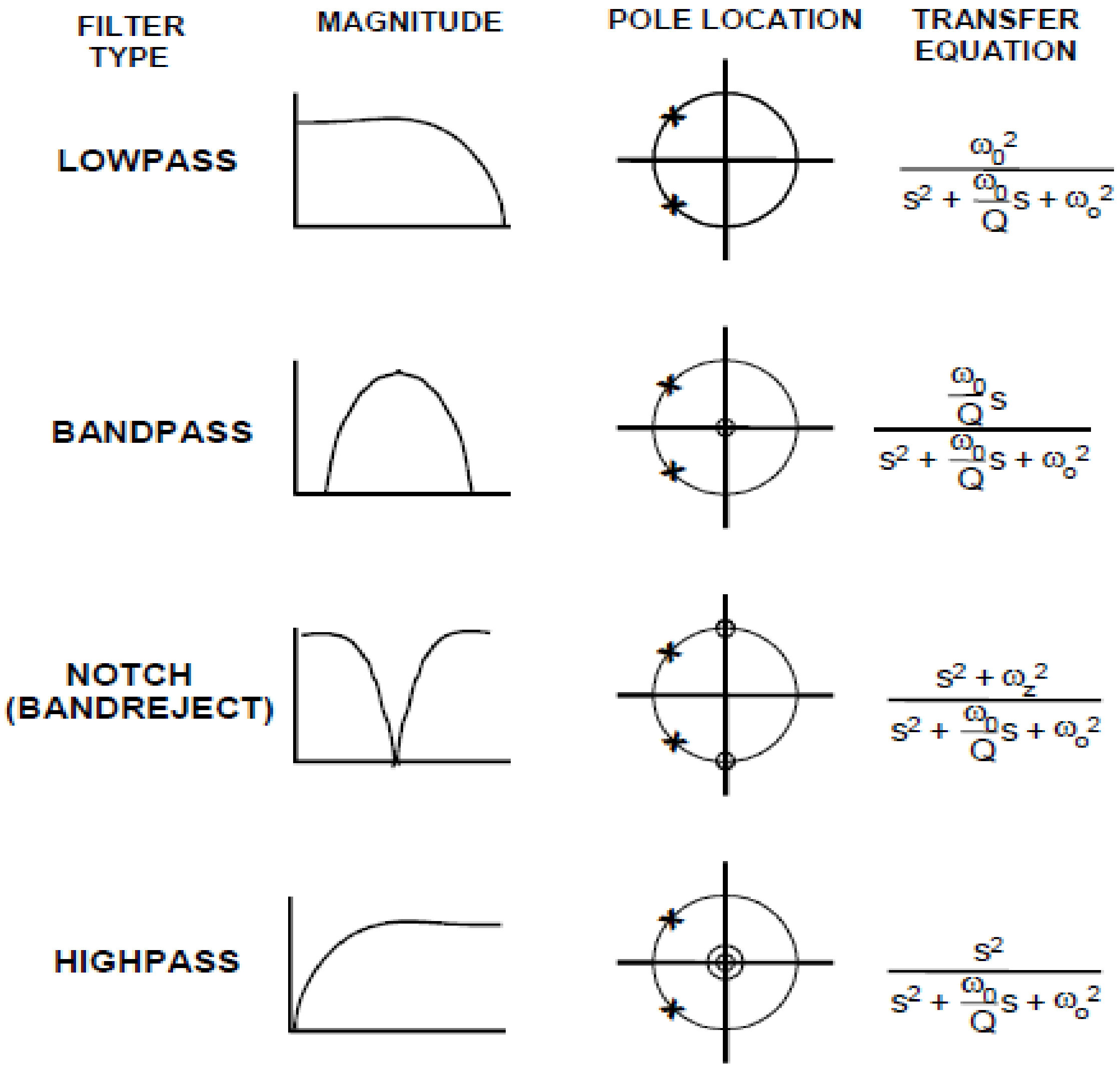


Fig 1.5: Standard second order filter response [11]

1.1.3 Based on performance parameter:

If an ideal low-pass filter existed, it would completely eliminate signals above the cut-off frequency, and perfectly pass signals below the cut-off frequency. In real filters, various trade-offs are made to get optimum performance for a given application. So based on performance filter can be divide into following categories :

a) **Butterworth** filters are termed maximally-flat-magnitude-response filters, optimized for gain flatness in the pass-band. The attenuation is –3 dB at the cut-off frequency. Above the cut-off frequency the attenuation is –20 dB/decade/order. The transient response of a Butterworth filter to a pulse input shows moderate overshoot and ringing. For a Butterworth filter, the nominal transfer function for an n^{th} order low pass filter is given by:

$$G_n(f) = \sqrt{\frac{1}{1 + \eta^{2n}}} \qquad (1.1)$$

Where $\eta = (f / f_0)$, and $f_0 = f_c$, the −3 dB frequency of the response function.

The advantages of each filter type come at the expense of other characteristics. The Butterworth is considered by a lot of people to offer the best all-around filter response. It has maximum flatness in the pass-band with moderate roll-off past cut-off, and shows only slight overshoot in response to a pulse input.

b) **Bessel** filters are optimized for maximally-flat time delay (or constant-group delay). This means that they have linear phase response and excellent transient response to a pulse input. This comes at the expense of flatness in the pass-band and rate of roll-off. The cut-off frequency is defined as the –3-dB point. The Bessel low-pass filters have a linear phase response over a wide frequency range, which results in a constant group delay in that frequency range. Bessel low-pass filters, therefore, provide an optimum square-wave transmission behavior. However, the pass-band gain of a Bessel low-pass filter is not as flat as that of the Butterworth low-pass, and the transition from pass-band to stop-band is by far not as sharp as that of a Tschebyscheff low-pass filter. The Bessel is important when signal-conditioning square-wave signals. The constant-group delay means that the square-wave signal is passed with minimum distortion (overshoot). This comes at the expense of a slower rate of attenuation above cut-off.

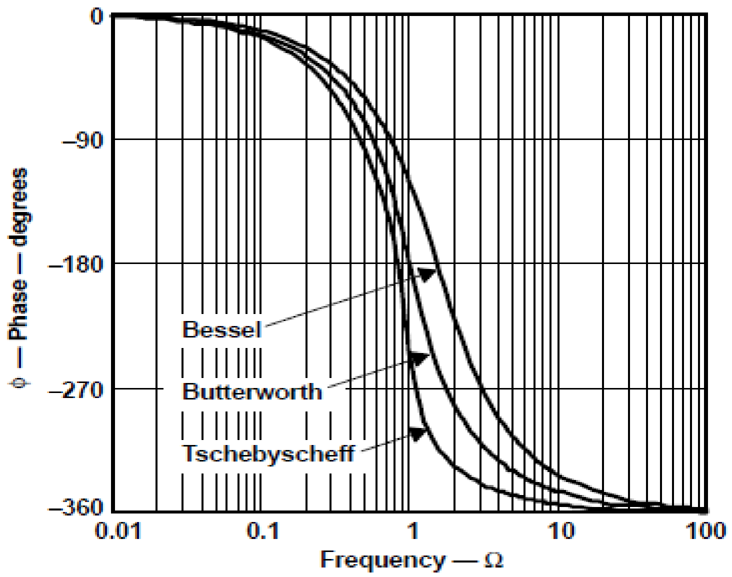


Fig 1.6 Comparison of Phase Responses of Fourth-Order Low-Pass Filters

c) **Chebyshev** filters are designed to have ripple in the pass-band, but steeper roll-off after the cut-off frequency. Cut-off frequency is defined as the frequency at which the response falls below the ripple band. This type of filter has an equal-ripple frequency response in the pass band, together with an ever-descending property in the stop band, where the power of interferences far into the stop band is usually much larger than the signal trying to extract, still, it has a comparatively sharp transient region, that means saving orders of the transfer function (and thus circuits and power) when the same attenuation is to be realized at the same distance from the edge of the pass band. However, Chebyshev type I filters have one apparent drawback, that in compare with their counterparts, they have considerably higher quality factors (Q), it becomes a severe problem to in-band plainness by enhancing ripple height when realizing a filter of too high a quality factor with practical circuits.

Chebyshev type-I has ripples in the pass band, but it rolls off very fast. **Chebyshev type-II** has ripples in the stop band, has the same roll-off as type-I, and has no ripples in the pass band. The elliptic filter mixes Chebyshev type-I and type-II, it has ripples in both the pass and the stop band, but has the steepest roll-off at the cut-off frequency. The Butterworth filter has a slow roll-off compared to the Chebyshev type-I.

For a given filter order, a steeper cut-off can be achieved by allowing more pass-band ripple. The transient response of a Chebyshev filter to a pulse input shows more overshoot and ringing than a Butterworth filter.

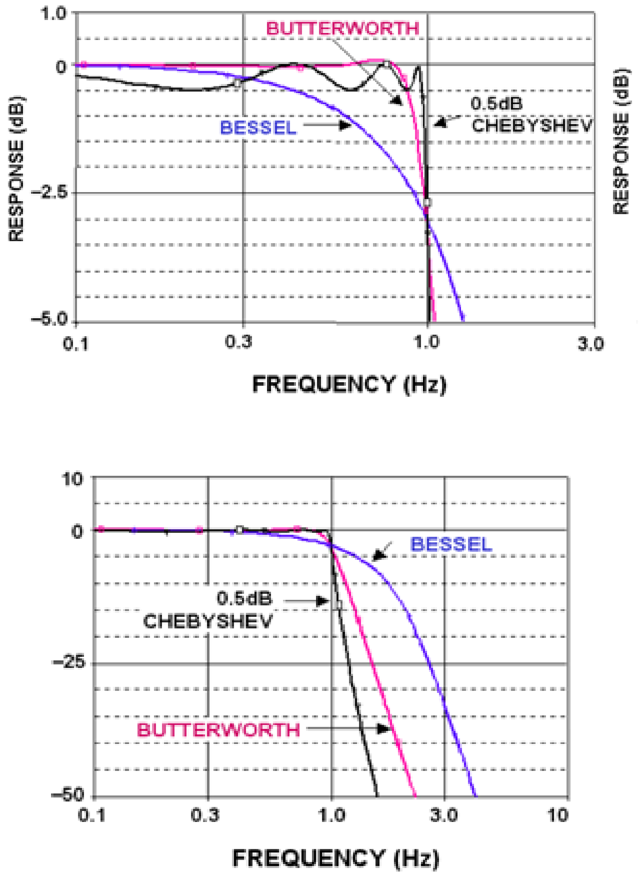


Fig 1.7 Comparision of amplitude response of Bessel, Butterworth and Chebyshev Filter[11]

The responses of several all-pole filters, namely the Bessel, Butterworth and Chebyshev (in this case of 0.5dB ripple) will now be compared. An 8 pole filter is used as the basis for the comparison. The responses have been normalized for a cut-off of 1Hz. Comparing Figure 1.6, it is easy to see the trade-offs in the response types. Moving from Bessel through Butterworth to Chebyshev, notice that the amplitude discrimination improves as the transient behavior gets progressively poorer.

Table 1.1 Summary of Filter Type Trade-Offs

Filter types	Advantages	Disadvantages
Butterworth	Maximum pass-band flatness	Slight overshoot in response to pulse input and moderate rate of attenuation above f_c
Bessel	Constant group delay – no overshoot with pulse input	Slow rate of attenuation above f_c
Chebyshev	Fast rate of attenuation above fc	Large overshoot and ringing in response to pulse input

1.2 Filter topologies :

Two main topologies are available to implement a linear analog filter.

1.2.1 Cauer topology

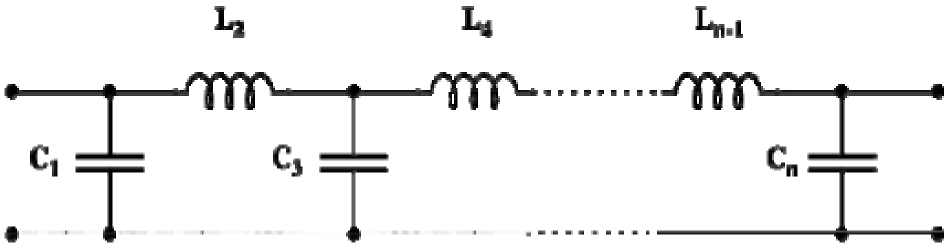


Fig. 1.8 LC resonant network[14]

The Cauer topology uses passive components (shunt capacitors and series inductors) to implement a linear analog filter. For example the Butterworth filter having a given transfer function can be realized using a Cauer 1-form. The kth element is given by:

$$C_k = \sin\left[\frac{(2k-1)}{2n}\pi\right] \; ; k = odd \qquad (1.2)$$

$$L_k = \sin\left[\frac{(2k-1)}{2n}\pi\right] \; ; k = even \qquad (1.3)$$

1.2.2 Sallen-Key topology

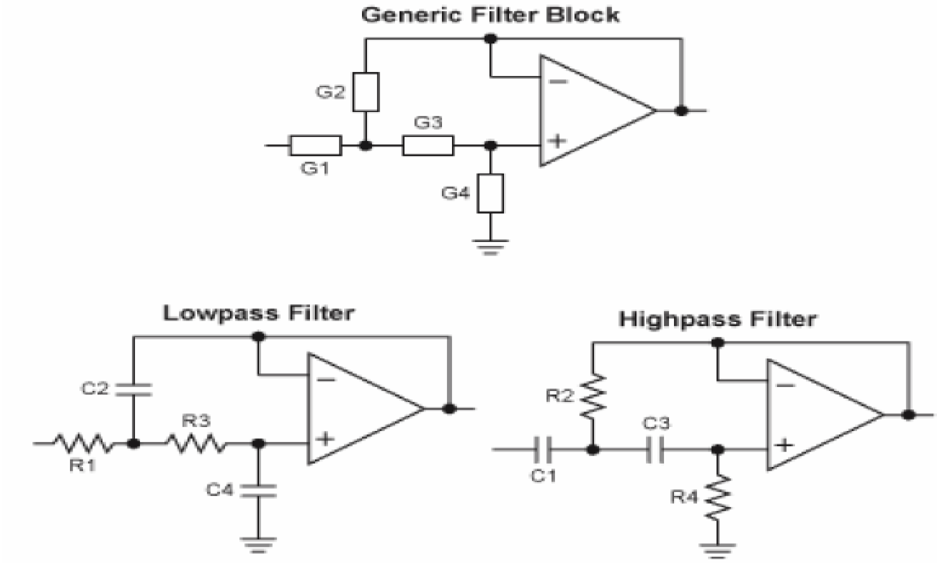


Fig. 1.9 Sallen-Key implementations[14]

The Sallen-Key topology uses active and passive components (operational amplifiers, resistors and capacitors) to implement a linear analog filter. Each Sallen-Key stage implements a conjugate pair of poles. The overall filter is implemented by cascading all stages in series. If there is a real pole (in the case where the order is odd), this must be implemented separately, usually as a RC circuit, and cascaded with the op-amp stages. Sallen-Key filters are relatively resilient to component tolerance, although obtaining high Q factor may require extreme component values or higher gain in the non-inverting amplifier. where the cut-off frequency (f_c) and the quality factor (Q) is:

$$f_c = \frac{1}{2\pi(\sqrt{R_1R_3C_2C_4})} \qquad (1.4)$$

$$Q = \frac{\sqrt{R_1R_3C_2C_4}}{C_4(R_1+R_3)} \qquad (1.5)$$

1.3 Filter parameter :

The idealized filter unfortunately, cannot be easily built. The transition from pass band to stop-band will not be instantaneous, but instead there will be a transition region. Stop band attenuation will not be infinite. The five parameter of practical filter are defined below.

Cut-off frequency (f_C):

The cut-off frequency (f_C) is the frequency at which the filter response leaves the error band (or the −3dB point for a Butterworth response filter).

Stop band frequency(f_s):

The stop-band frequency (f_s) is the frequency at which the minimum attenuation in the stop-band is reached.

Pass band ripple:

The pass-band ripple (Amax) is the variation (error band) in the pass-band response.

Pass band attenuation:

The minimum pass-band attenuation (A_{min}) defines the minimum signal attenuation within the stop-band.

Steepness:

The steepness of the filter is defined as the order (M) of the filter. M is also the number of poles in the transfer function.

A pole is a root of the denominator of the transfer function. Conversely, a zero is a root of the numerator of the transfer function. Each pole gives a -6 dB/octave or -20 dB/decade response. Each zero gives a +6dB/octave, or +20 dB/decade response.

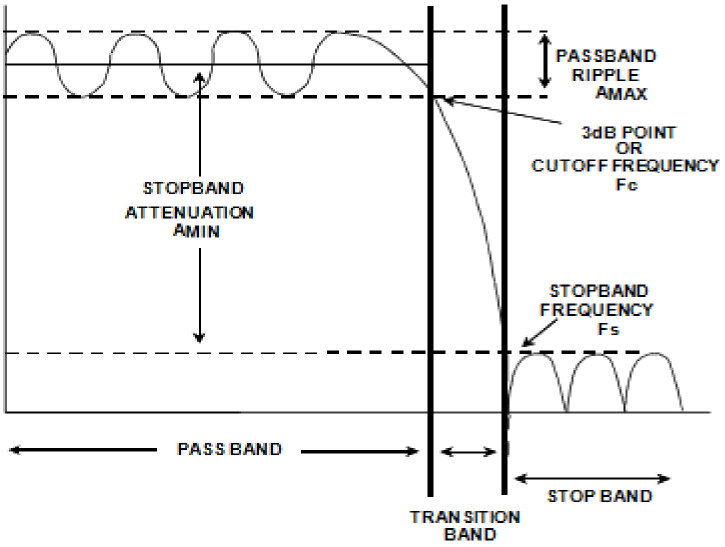


Fig 1.10 : Filter parameter[11]

As the function of any filter is to allow signals of a given band of frequencies to pass unaltered while attenuating or weakening all others those are not wanted, the amplitude response characteristics of an ideal filter by using an ideal frequency response curve of the four basic filter types are shown.

1.4 Applications of filter

i. A typical data acquisition system for **biomedical signals** is shown in Fig. 1.8. The preamplifier must amplify the input signal to a higher level with low distortion and low noise. For example, in electrocardiograph applications where the magnitude of the preamplifier signal has to be processed around hundred milli-voltage by a low-pass filter. Thus, a low cut-off frequency (2-5 Hz) is required to sense the wave signal.

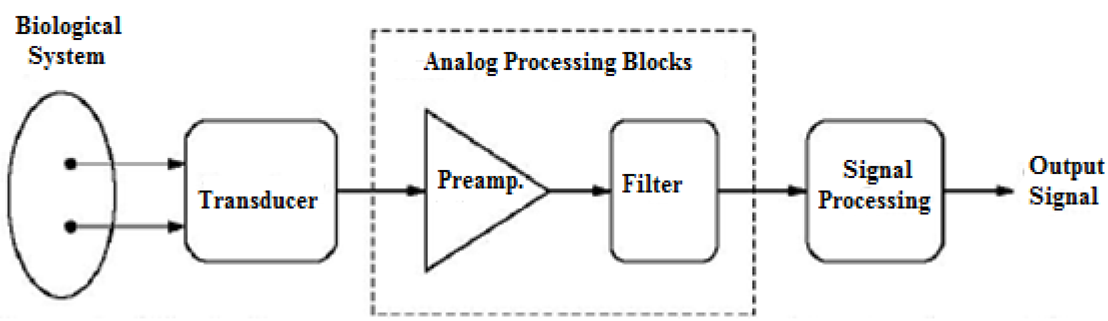


Fig 1.11 Block diagram of a general purpose bioelectric signal acquisition system[1]

ii. Filters have many practical applications. A simple, single pole, low-pass filter (the integrator) is often used to **stabilize amplifiers** by rolling off the gain at higher frequencies where excessive phase shift may cause oscillations.

iii. A simple, single pole, high-pass filter can be used to block DC offset in **high gain amplifiers** or single supply circuits. Filters can be used to separate signals, passing those of interest, and attenuating the unwanted frequencies.

iv. In **integrated wireless receivers**, active filter is often the module that consumes the largest part of total current consumed and chip area, thus a properly designed filter will greatly benefit both cost and power consumption. However, a set of non-ideal effects exist in practical circuits that require the sacrifice of other performances to overcome, in which power consumption (usually accompanied by area) is the biggest victim. Meanwhile, filters composed of on chip capacitors and resistors also suffer from value deviations of their components, which may cause up to 40% frequency deviation.

v. The **electrical activity within living organisms**, one often encounters the terms "low-pass filter" and "purely resistive medium"**.** In network theory it is known, that building any type of frequency selective filters (using continuous elements), capacitive and inductive elements are required. Due to the complicated formalisms, the fundamental reason for the low-pass filter effect of tissue remains somewhat hidden.

vi. A sixth order Butterworth low pass filter for **aerospace extreme environment applications** is implemented in SiGe BiCMOS technology.

vii. **COGNITIVE radio (CR)** is an emerging wireless communication system that intelligently detects and utilizes a temporarily unoccupied spectrum band on a non interfering basis while ensuring coexistence with higher priority users. The IEEE 802.22 working group has been developing a standard for the CR system. An active-*RC* low-pass filter (LPF) that is developed as part of our TV-band CMOS transmitter for IEEE 802.22 CR applications.

viii. A great demand for lighter hand-held mobile phones and longer battery lifetime, low-voltage integrated circuit design solutions must be developed. The Gm-C filter appears to be a better option for the **UWB wireless application**, which uses pulse signals at a high speed.

ix. **L**OW-PASS FILTERS (LPF) are used to **eliminate high order harmonics** and spurious of mixers, voltage controlled oscillators (VCO), and power amplifiers.

Chapter 2

Literature survey

The application is a tiny integrated circuit that is mounted under the patient's skin and monitors cardiac data like ECG. The measurement takes place all over the time, 24/7 and the acquainted data is sent to a central processing unit (e.g. a computer) via radio waves where it is stored and processed. The ECG recordings made by the circuit have very low frequency components that must be separated from the noise that suppresses the useful signal.

Low-frequency filters are important building blocks for biomedical systems, wherein analog pre-processing blocks, such as low noise pre-amplifiers and filters for the acquisition of bioelectric signals are employed. These circuits should not introduce any form of distortion that can destroy the information contained. For this reason, the analog pre-processing blocks must present high performance over the frequency of interest.

The tolerance scheme specifies the pass-band and stop-band bandwidths of the filter and the acceptable ripple in these bands. Because a very steep cut-off filter is needed, filters of higher orders must be examined. The higher the filter order the steeper the cut-off slope is, but proportional to the order it results in a more complex circuit. This trade-off must be kept in view. In this circuit, power consumption is a critical factor thus the complexity of the filter and the steepness must be kept at an optimal value.

The filters employed in biomedical systems are used for sensing bioelectrical signals which, typically, are in the range of 1 V–100 mV while the frequencies are below 100 Hz. At the input, a low-pass filter (LPF) is usually employed in order to limit the frequency band. The design of very low-frequency filters (10 Hz) is not straightforward, especially for integrated circuit implementation.

However, despite their utility, creating large time constant low-pass filters on-chip is a challenging problem. To implement large time constants, switched-capacitor-based topologies require large capacitor ratios [15], and a sufficiently high power supply must be used to achieve an acceptably low switch ON-resistance [14].

Switched-capacitor filter has been successfully applied to many voice band applications. It has good accuracy of time constants and good temperature characteristics; whereas the problem of clock feed-through is difficult to be solved and it also needs continuous-time filters as anti-aliasing filters. Another alternative is to use Gm-C filters which do not have the aliasing problem of sampled-data systems. Due to the dependence of the cut-off frequency of the filter on the absolute values of monolithic components such as capacitors and transistor transconductances, which are both process and temperature dependent, feedback and cancellation techniques are required to control the cut-off frequency of this type of filters. And it also needs a small transconductance in order to avoid using large area capacitors at low frequency. This work describes a low cut-off frequency CMOS low pass filter which utilizes a cross-coupled input structure to cancel the deviation of the cut-off frequency under the influence of different temperature and produce an appropriate transconductance with four auxiliary amplifiers to keep the gain. It is a monolithic filter with low power consumption and low-voltage.

2.1 CMOS transconductance amplifiers (OTA) ant its different architectures:

Prasant K. Mahapatra and *el at.*[4]

The performance of filters designed by the use of passive components degrades at audio frequencies and the required resistances and inductances values calculated from the mathematical expression are very difficult to meet from the market. To find a solution to this problem this paper presents a study to realize Passive Filters into Active Filters using Operational Transconductance Amplifier (OTA). Basic properties of OTA are also discussed. By controlling the Voltage Gain of OTA, one can change its transconductance, which is very useful in the designing the first order and second order active filters. In this article only first order low pass filters using OTA id designed. It is concluded that the new approach gives us a wide range of tunable cut-off frequencies.

Randall L. Geiger and Edgar Sánchez-Sinencio 1985 [5]

Basic properties of the Operational Transconductance Amplifier (OTA) are discussed. Applications of the OTA in voltage-controlled amplifiers, filters, and impedances are presented. A versatile family of voltage-controlled filter sections suitable for systematic design requirements is described. The total number of components used in these circuits is small, and the design equations and voltage-control characteristics are attractive. Applications of OTAs in continuous-time monolithic filters are considered.

A. Veeravalli and *el at.* 2002 [22]

A family of CMOS operational transconductance amplifiers (OTAs) has been designed for very small's (of the order of nanoamperes per volt) with transistors operating in moderate inversion. Several OTA design schemes such as conventional, using current division, floating-gate, and bulk-driven techniques are discussed. A detailed comparison has also been made among these schemes in terms of performance characteristics such as power consumption, active silicon area, and signal-to-noise ratio. The transconductance amplifiers have been fabricated in a 1.2µm n-well CMOS process and operate at a power supply of 2.7 V. Chip test results are in good agreement with theoretical results.

A.Arnaud, R. Fiorelli, and C. Galup-Montoro 2006 [23]

In this paper, series-parallel (SP) current-division will be employed for the design of very low transconductance OTAs. From the theory and measurements, it will be shown that SP mirrors allow the division of currents with division factors of thousands, without reducing matching or noise performance. SP mirrors will be applied to the design of OTAs ranging from 33 pS to a few nS, with up to 1 V linear range, consuming in the order of 100nW, and with a reduced area. Several design concerns will be studied: linearity, offset, noise, and leakages, as well as layout techniques. A final comparative analysis concludes that SP association of transistors allows the design of very efficient transconductor, for demanding applications in the field of implantable electronics, among others.

2.2 Low power and low frequency Low pass filter techniques:

Chun-Lung Hsu and *el at.* 2006 [1]

This paper presents the design method of very low frequency current-mode low-pass filters for biomedical applications. The double-output operational transconductance amplifiers and grounded capacitors (DO-OTA-Cs) are used to realize the proposed low-frequency low-pass filters. The theory focuses mainly on establishing a relationship between the cascaded DO-OTA-Cs and the multiple-loop feedback connections, which make the design formulas. For the implementation of large time constants of the proposed low-pass filters, both linearized DO-OTAs with reduced transconductance and impedance scaler scheme for grounded capacitors are employed. Physical chip design was fabricated by using TSMC 0.35-um 2P4M CMOS process working at 1.5 V, the circuit dissipates about 96.5 nW and the -3 dB frequency is around 3.8 Hz.

Esther Rodriguez-Villegas and *el at.* 2011[2]

In this a first-order low-pass filter topology capable of providing cut-off frequencies down to 2 mHz with power consumption of 5 nW is presented. The circuit is intended for signal conditioning applications, particularly for use with very low frequency physiological signals in low-power portable medical equipment. To achieve a low-frequency cut-off, the filter is based around the use of a clocked transconductor, which provides low transconductance while using a relatively high bias current level. The circuit is implemented in a 0.35-μm technology with a 1-V supply and has 32-μVRMS measured noise. In terms of power consumption and cut-off frequency the reported filter outperforms previous filters from the literature.

Haidong Liu and *el at.*2009 [3]

The design of a low-cut-off-frequency Gm-C low-pass filter is presented. The OTA utilizes a common folded-cascode structure, and the value of the transconductance is equal to the cross coupled input stage, if the transmissions of current mirrors use the same ratio. As the circuit is desired to operate at low frequency, it is necessary to design a small linear trans-conductance amplifier employing a cross-coupled input stage. To compensate the gain loss, the auxiliary amplifiers are added. The differential pairs are off-setted in the sub-threshold zone. The filter is fabricated in a 0.18μm CMOS process, operating with a 1.8 V supply and using a bias current of 4μAand have 10 KHz cut-off frequency. The total power consumption is 225 μW with a total capacitance load of 60 pF.

Francesco Rezzi and *el at.*1995 [7]

The reduction of the supply voltage forces to develop system and circuit solutions able to achieve the same performance previously obtained with higher supply voltage. In this paper, a second-order low-pass continuous-time filter operating at **a** 3 **V** power supply is presented. The prototype filter is implemented using a highly linear pseudo-differential transconductor. The input common-mode signal is cancelled at the transconductor level using a feed-forward path. The output common mode voltage is controlled at the filter level using lossy integrators. A prototype cell has been realized in **1.2 pmV** BiCMOS technology.

Andras Timar and *el at.*2007 [8]

In this paper, specific issues of the most important part of such a data acquisition system is presented, the design of a low pass filter. The device collects cardiac data and monitors hearth and circulation activity and is built into the human body. The device is therefore must be realized as an integrated circuit. The major issue to overcome in the design of a system that is aimed at being built into the human body is creating large value capacitances needed to the realization of filters for the specific application. Through low frequency demands, large resistors and capacitors must be used, which is very difficult to achieve on silicon wafer. A design method of such high valued capacitors was presented. This method complies with the standard CMOS process and design is possible using traditional CMOS methodologies.

Sergio Solís-Bustos and *el at.* 2000[9]

The design and implementation of a fully integrated complementary metal–oxide–semiconductor (CMOS) sixth-order 2.4 Hz low-pass filter (LPF) for medical applications is presented. For the implementation of large-time constants both linearized operational transconductance amplifiers with reduced transconductance and impedance scalers schemes for grounded capacitors are employed. Experimental results for the filter have shown a dynamic range (DR) of 60 dB, while the harmonic distortion components are below 50 dB. The power consumption for the filter is below 10 µW, the power supply is 1.5 V, and the active area is 1 mm^2. The filter was fabricated in a double poly double metal 0.8 m CMOS process.

Z. Yang and *el at.* 2003[13]

A novel differential current-mode integrator (CMI) for voltage controllable low frequency continuo time filters is presented. An example fifth-order low-pass filter using the proposed CMI and on-chip capacitors was implemented in an AMI 1.2 pm CMOS process and it achieved -3dB cut-off frequencies ranging from 160 Hz to 5.6 kHz, by changing a single control voltage.

F. Gozzini and *el at.* 2006 [17]

A new approach to obtain very-small transconductance systems, i.e. large value equivalent resistors, on standard CMOS technology is proposed. The transconductor is characterized by a compact topology, high current dynamic range and linearity up to rail-to-rail input swing and symmetric operation for positive and negative currents. Experimental results show transconductance values as small as 3pA/V with fA working capability, ideal in various applications such as high sensitivity integrators or low-pass filters with sub-Hz cut-off frequencies.

Alfredo Arnaud and *el at.* 2006[24]

In this work a continuous time low pass filter with sub-Hz upper band limit is presented. The circuit is based on a Gm-C approach where the transconductance is stabilised against temperature variations over a wide temperature range (0-80 "C), using a D.C. feedback loop applied to a dummy transconductor (master). Very low transconductance values required to obtain low frequency singularities are achieved by means of multistage current division.

E.Sanchez-Sinencio and J.Silva-Martinez 2000 [27]

An updated version of a 1985 tutorial paper on active filters using operational transconductance amplifiers (OTAs) is presented. The integrated circuit issues involved in active filters (using CMOS transconductance amplifiers) and the progress in the field in the last 15 years is addressed. CMOS transconductance amplifiers, nonlinearised and linearized, as well as frequency limitations and dynamic range considerations are reviewed. OTA-C filter architectures, current-mode filters, and other potential applications of transconductance amplifiers are discussed.

2.3 Comparision of results of different low-frequency low-pass filters design technique

Table 2.1 compares the results of different low-frequency low-pass filters design technique and integrators reported in the literature. For conciseness, only implementations with experimental results that have been reported and, are included in this table.

Table 2.1: Comparison of the performance of different low-frequency low-pass filters

Ref	**[16]**	**[9]**	**[18]**	**[17]**	**[19]**	**[23]**	**[20]**	**[21]**	**[22]**	**[24]**	**[25]**	**[2]**
CMOS process (μm)	0.35	0.80	0.35	0.80	0.35	0.80	0.35	0.50	1.20	0.80	1.00	0.35
Minimum Cut-off/Hz	35	2.4	1.5	0.5	0.5	0.30	0.25	0.18	0.17	0.1	.075	.002
Filter Order	1	6	2	2	1	1	2	1	2	1	1	1
Power Consumption/W	-	10μ	165 μ	2 μ	-	113 n	-	77.4 n	8.2 μ	230n	-	5n
Supply Voltage / V	3.2	3.0	3.3	1.5	-	-	3.0	-	2.7	3.0	5.0	1.0
Integrating Capacitance/F	25f	5p	52.5 p	-	100f	50p	29p	15p	10n	70p	10p	40p

From table 2.1, in terms of power consumption and cut-off frequency the [2] filter outperforms over other filters from the literature.

Chapter 3

OTA Based Low-pass filters

The conventional operational amplifier (op-amp) is used as the active device in the vast majority of the active filter literature. A host of practical filter designs have evolved following this approach. It has also become apparent, however, that operational amplifier limitations preclude the use of these filters at high frequencies, attempts to integrate these filters have been unsuccessful (with the exception of a few no demanding applications), and convenient voltage or current control schemes for externally adjusting the filter characteristics do not exist.

In this chapter, basic first, second and higher-order structures using the transconductance amplifier (often termed the operational transconductance amplifier: OTA) are discussed. It is shown that these structures offer improvements in design simplicity and programmability when compared to op-amp based structures as well as reduced component count. Many of the basic OTA based structures use only OTAs and capacitors and, hence, are attractive for integration and called as Gm-C filter techniques.

The CMOS continuous-time filters have been received a great interest and investigated since the 1980s. A Gm-C filter is a kind of the continuous-time filter which needs the operational transconductance amplifier (OTA) to be a basic building block. The cut-off frequency of a Gm-C filter is directly proportional to the gain of trans-conductance and inversely proportional to the capacitance.

The major limitation of existing OTAs is the restricted differential input voltage swing required to maintain linearity. Since the transconductance gain of the OTA is assumed proportional to an external dc bias current, external control of the filter parameters via the bias current can be obtained.

Most existing work on OTA based filter design approached the problem by either concentrating upon applying feedback to make the filter characteristics independent of the transconductance gain or modifying existing op-amp structures by the inclusion of some additional passive components and OTAs.

Principle difference between operational amplifier and operational transconductance amplifier

a) Its output of a current contrasts to that of standard operational amplifier whose output is a voltage.

b) It is usually used open-loop, without negative feedback in linear applications. This is possible because the magnitude of the resistance attached to its output controls its output voltage. Therefore a resistance can be chosen that keeps the output from going into saturation, even with high differential input voltages.

3.1 OTA Model

The symbol used for the OTA is shown in Fig. 3.1,

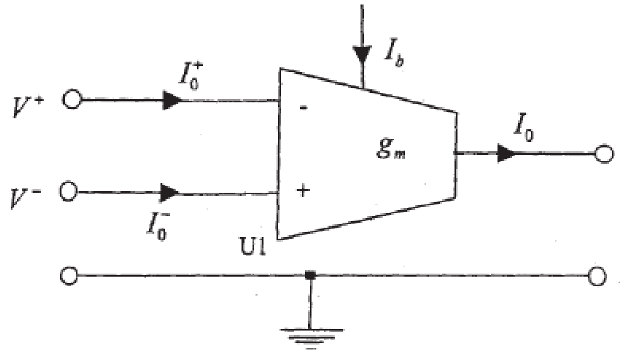


Fig 3.1 Circuit symbol of OTA[4]

Fig 3.2 shows the ideal small signal equivalent circuit.

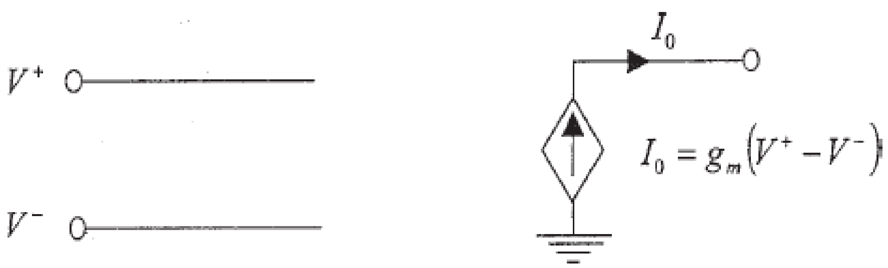


Fig 3.2 Ideal small signal equivalent of OTA[4]

The transconductance gain, *gm*, is assumed proportional to I_b. The proportionality constant *h* is dependent upon temperature, device geometry, and the process.

$$gm = h\,I_b \qquad (3.1)$$

$$I_o = gm(V^+ - V^-) \qquad (3.2)$$

As shown in the model, the input and output impedances in the model assume ideal values of infinity. Current control of the transconductance gain can be directly obtained with control of I_b. Since techniques abound for creating a current proportional to a given voltage, voltage control of the OTA gain can also be attained through the I_b input.

Characteristics of Ideal OTA can be summarized as follows,

Input impedance $(Z_{in}) = \infty$

Output Impedance $(Z_0) = \infty$

Inverting input current I_0^- = Non-inverting input current I_0^+

Bandwidth = ∞

3.2 Basic OTA Building Blocks

Some of the basic OTA building blocks are introduced in this section. A brief discussion about these circuits follows. Voltage amplifiers using OTAs are going to be discussed in this. The basic inverting and non-inverting configurations of OTA is shown in Fig 3.3.

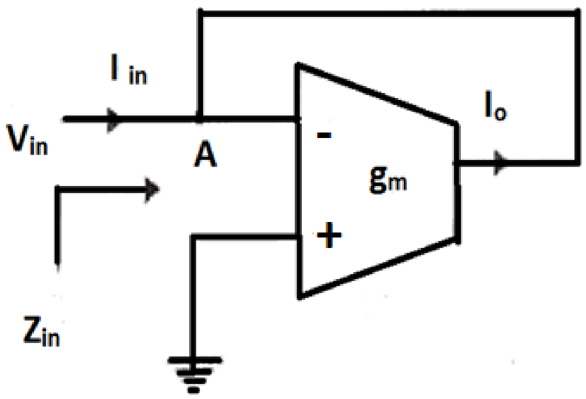


Fig 3.3 Inverting feedback amplifier[4]

Applying KCL at Node A gives us

$$\mathbf{I_{in} + I_0 = 0} \qquad \mathbf{(3.3)}$$

Where $I_0 = -V_m \times gm$

Substituting the value of I_0 in equation (3.3) we have,

$$Z_{in} = 1/ gm \qquad (3.4)$$

Fig 3.4 represents non inverting amplifier. In this, the voltage gain directly proportional to *gm*, which makes current (voltage) control of the gain via I_b straightforward. Furthermore, observe that a differential amplifier can be easily obtained by using both input terminals of the OTA in Figs. 3.3 or Fig 3.4. The major limitation of these circuits is the relatively high output impedance.

Applying KCL at node A, we have

$$I_0 = gm\, V_m \qquad (3.5)$$

Substituting equation (3.5) in equation (3.1) we have,

$$Z_{in} = 1/ g_{in} \qquad (3.6)$$

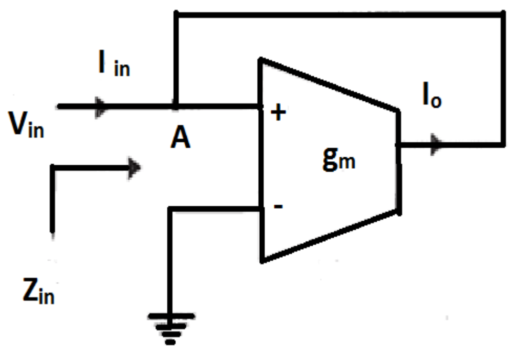


Fig 3.4 Non inverting feedback amplifier [4]

3.3 .Simulation results of Simple differential OTA

3.3.1 Simple differential OTA

Fig. 3.5 shows a basic differential input OTA with one current-mirror. To obtain very high output impedance the OTAs of Fig. 3.5 or Fig. 3.7 with the proper frequency compensation are used. These structures provide guaranteed stability.

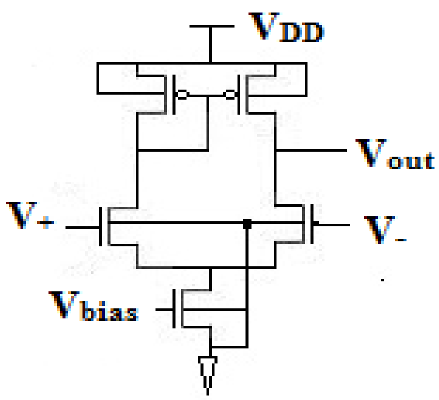


Fig 3.5 Schematic diagram of Basic OTA as differential pair.[27]

This OTA is designed for 5µW and 25 dB with 1.8 V power supply in 0.18µm UMC technology. Then following characteristic has been obtained shown in Fig 3.6.

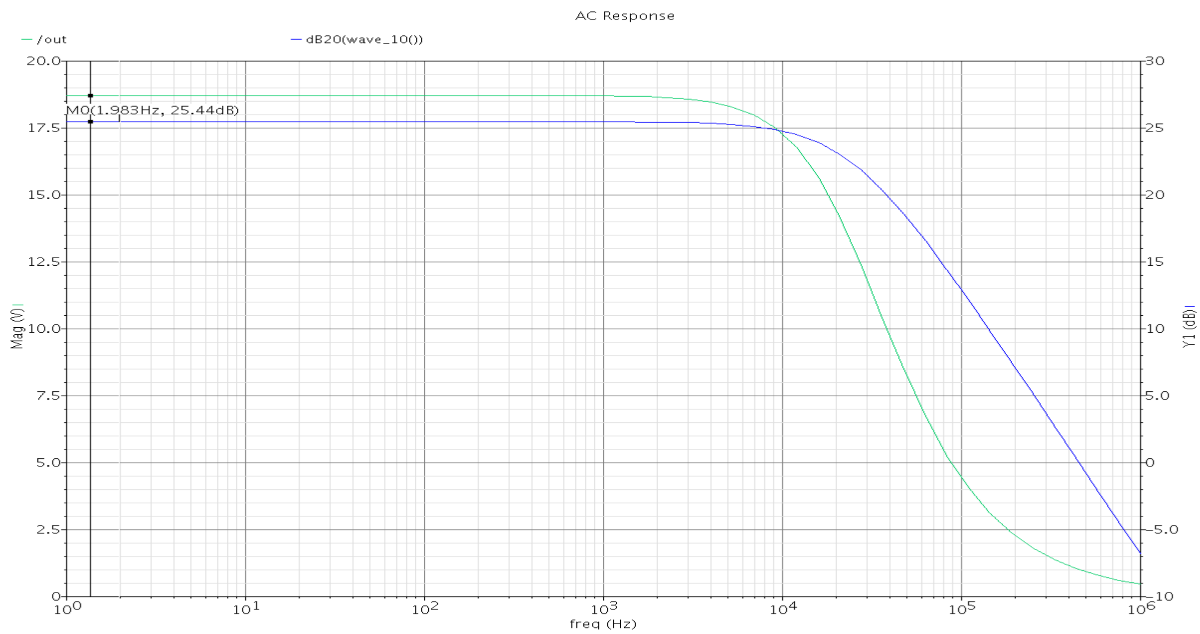


Fig 3.6 Gain plot of basic OTA structure

Obtained Gain is 25.44dB and power consumed is 4.88µW of above differential OTA.

3.3.2 Balanced differential OTA

Fig. 3.7 is a balanced OTA has three current mirrors and a single output. The complexity of differential OTA structures is also provide an improvement in offset reduction and robustness, but not necessarily with an improvement for high-frequency applications. Thus trade-offs between speed and accuracy should be established for each particular application.

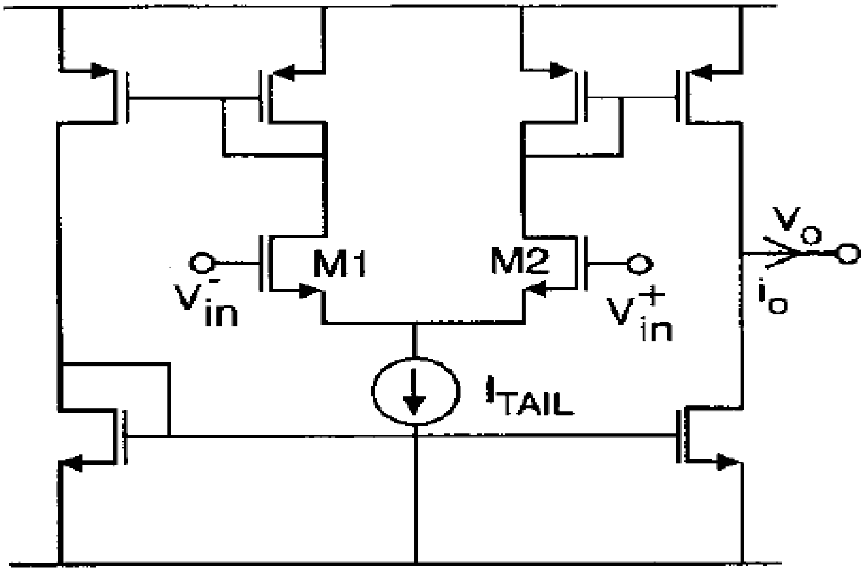


Fig 3.7 balanced differential OTA [27]

This OTA is designed for 5µW and 25 dB with 1.8 v power supply in 0.18µm UMC technology. Then following characteristic has been obtained shown in Fig 3.8.

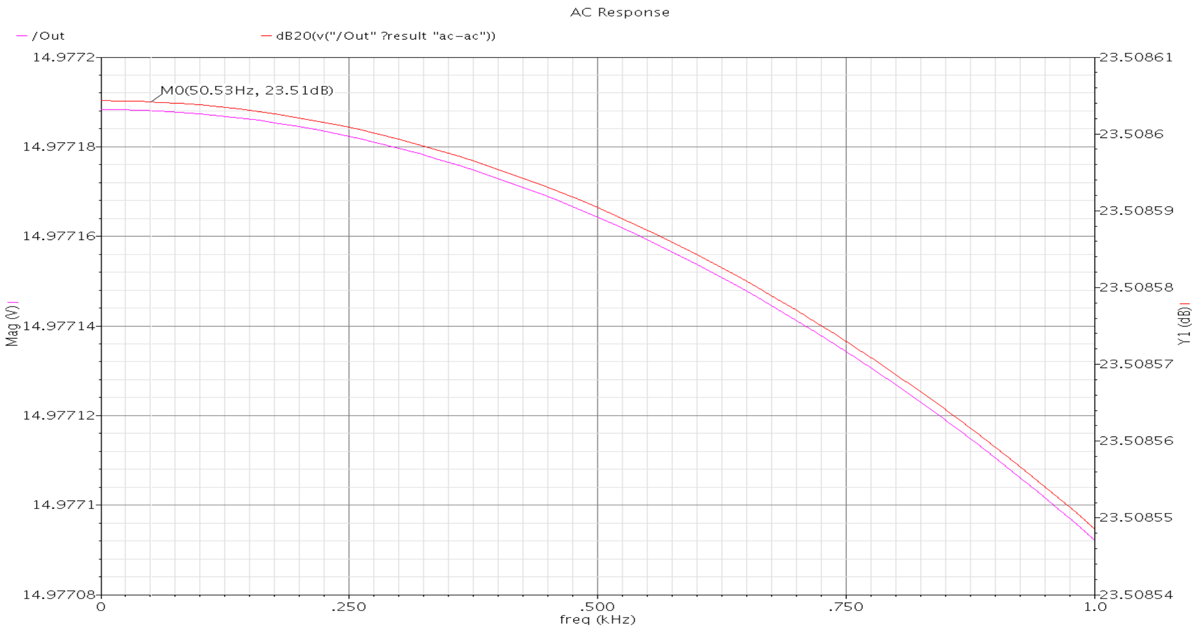


Fig 3.8 Gain characteristic of balanced OTA

Obtained Gain is 23.51dB and power consumed is 11.7µW of above differential OTA.

3.3.3 Folded cascode OTA

The input stage provides the gain of the amplifier. Due to the greater mobility of NMOS device, PMOS input differential pair presents a lower transconductance than carrier a NMOS pair. Thus, NMOS transistor has been chosen to ensure the largest gain required. For a folded OTA bandwidth performance is high.

The designed folded cascode OTA shown in Fig 3.9 is biased at ±1.8V power supply voltage using CMOS technology of 0.18 µm of UMC with the BSIM3V3 MOSFET model.

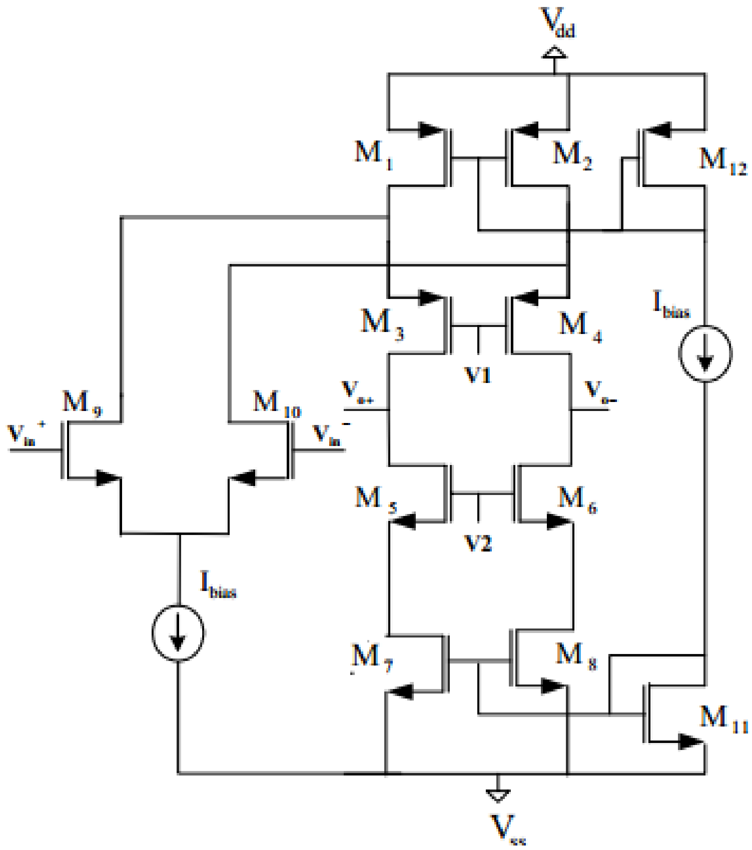


Fig 3.9 Folded OTA[29]

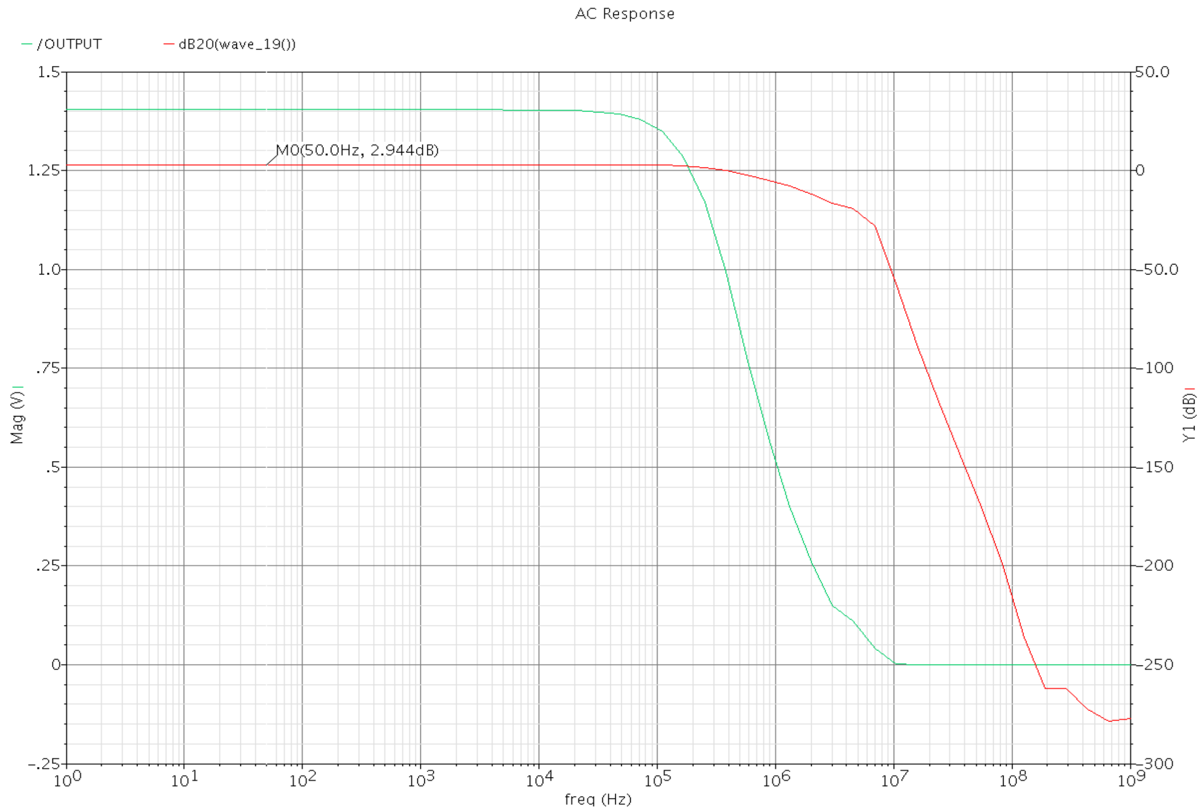


Fig 3.10 Gain characteristic of folded OTA

3.4 Filter formation with simple differential OTA

3.4.1 First order filter

First order low-pass filter with 1 pF capacitor is shown in Fig 3.11. OTA is replaced with simple differential OTA. Schematic view of Fig 3.11 is shown in Fig 3.12. Gm-C filtering has been used for this structure instead of switched capacitor because the problem of clock feed through is difficult to be solved and it also needs continuous-time filters as anti-aliasing filters. In Gm-C filtering due to the dependence of the cut-off frequency of the filter on the absolute values of monolithic components such as capacitors and transistor transconductances, which are both process and temperature dependent, feedback and cancellation techniques are required to control the cut-off frequency of this type of filters. And it also needs a small transconductance in order to avoid using large area capacitors at low frequency.

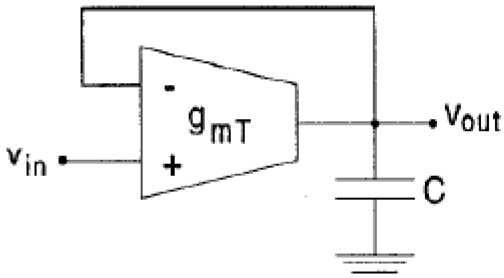


Fig 3.11 First order low-pass filter [28]

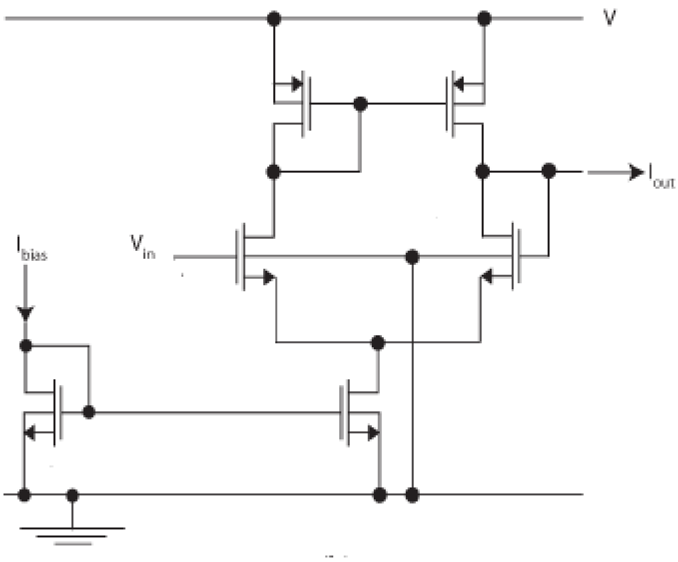


Fig 3.12 First order CMOS schematic [2]

3.4.2 Second order filter

A low-pass 2nd order filter is designed and Fig. 3.13 shows the block diagram of the circuit. In order to reduce the pass-band ripple of the interference from the signal, the low-pass filter utilizes a second-order Butterworth structure which consists of two operational transconductance amplifiers (OTA) and two grounded capacitors. The problem is that the behavior of the filter is highly sensitive to analog integrator non-idealities. Fig 3.14 shows schematic view of Fig3.13. The OTA utilizes a common OTA structure. Thus the value of cut-off frequency can be adjusted by the size of the input stage.

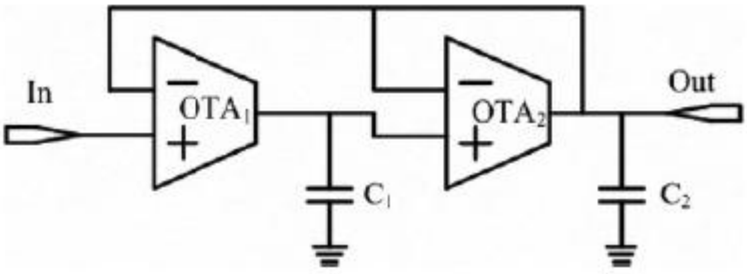


Fig 3.13 Second order low-pass filter[3]

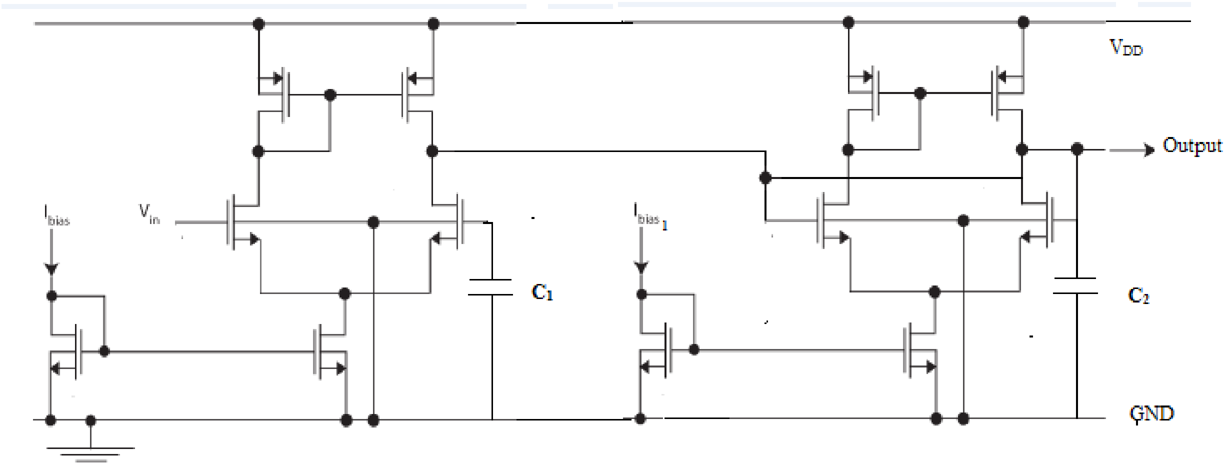


Fig 3.14 Second order CMOS schematic

3.5.3 Higher order filters

Higher order filters are obtained by cascading 1st and 2nd order filters. For example 3rd order filter is obtained by cascading 1st and 2nd order filter. Through this method following gain characteristics are obtained shown in Fig 3.15. From characteristic plot it is clear that steepness of highest order filter is most and further decrease with decreasing filter orders.

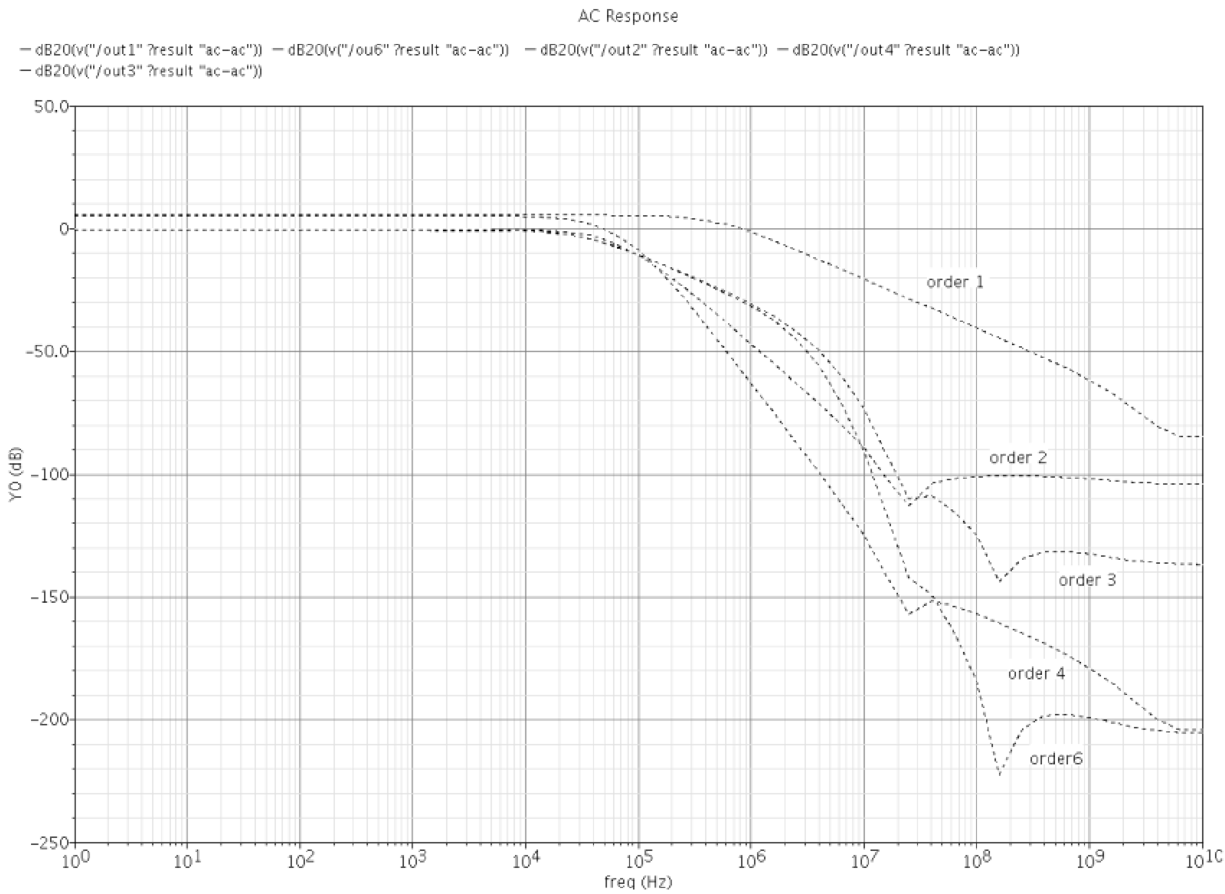


Fig 3.15 Comparison of 1st 2nd 3rd 4th and 6th order filter characteristics

These filters having power range of µW. For making device power efficient more power reduction is required. In next chapter **low-pass** filter is designed with ultra low power in nW ranges and for biomedical frequencies.

Chapter 4

Biomedical Frequency ultra low power Low-pass filter technique

For achieving very low cut-off frequency filter many design techniques have been proposed, they are mainly used in biomedical, audio and neural networks applications. According to these application, filter IC should take small integration and consume very low power. As a result weak inversion region of operation is used. It is clearly seen from gain characteristics that conventional differential OTA cannot use to implement very low frequency filters whether they are operated in strong inversion or weak inversion region since the transconductance value will not be realized with usual values of biasing current in transistor dimensions or the biasing currents will be too low(in the order of pA). Hence the effect of leakage current and noise will dominate the performances of the circuit. All transistors in the circuit are operated in the weak inversion region so that the low supply voltage and very low power consumption is also achieved. [28]

In gm/C-based topologies, the cut-off frequency is generally determined by ratio *gm*/C, where C is the integrating capacitance. However, area limitations restrict the maximum capacitance that can be present on-chip to picofarad values, limiting the minimum cut-off that can be achieved. Large off-chip capacitors can be used, but for a given cut-off frequency, the required *gm* value is decreased, decreasing the transconductor output current. On-chip currents down to femtoampere levels are feasible, but moving off-chip, the current is limited by the leakage currents in the bond pads to picoampere levels [20]. Larger *gm* and *C* values must thus be used to keep the output current above this limit but at the cost of power consumption.

For a fully on-chip solution, impedance scaling techniques, placing the capacitor across an inverting amplifier and utilizing the Miller effect, can be used to increase the effective capacitance, although this introduces increased complexity, power consumption, and noise [9]. More commonly, to achieve low-frequency on-chip cut-offs, the transconductor unit is modified to reduce the effective *gm* value.

Here, a clocked transconductor is used to form the reduced transconductance *gm* element in a *gm/C* filter. The duty cycle of the clock then determines the effective transconductance and allows easy digital control of the filter cut-off frequency.

4.1 Principle of Operation

The basic principle of the proposed low-pass filter topology is based on clocking of the output of a standard transconductor element. A standard transconductor is placed in a feedback loop arrangement with a capacitor forming a first-order *gm/C* low-pass filter, and a switch is then added between the output of the transconductor and the capacitor. This switch allows the output of the transconductor to be connected to and disconnected from the capacitor and the feedback loop.

The output current from the transconductor, i.e., I_1, can only flow into the capacitor when the switch is closed, the average current that flows into the capacitor, i.e., I_2, is reduced.

$$I_2 = \delta \times I_1 \qquad (4.1)$$

Where δ is the duty cycle of switch φ. And I_2, is the effective output current of the transconductor. It is reduced; the effective transconductance of the transconductor is reduced by the same amount. Furthermore, this reduction in transconductance is achieved in the time domain and may be precisely controlled via the clock used to control the switching operation. So there is easy digital control of filter transconductance and cut-off frequency. The clock frequency used must be sufficiently high for correct operation so that the clock harmonics fall out of band.

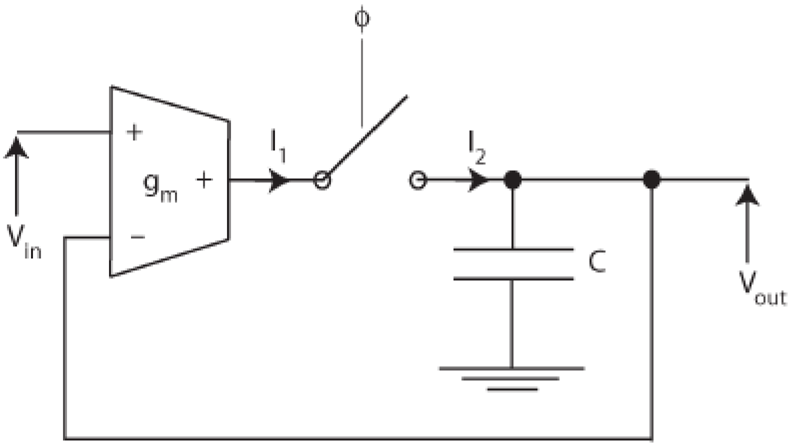


Fig4.1 Principle of operation of the proposed low-pass filter

The switch used in Fig. 4.1 also increases the effective output resistance of the transconductor. The proposed topology overcomes this problem as, when the switch is open, g_o does not affect the capacitor voltage since the two nets are isolated. The capacitor is only loaded by g_o when the switch is closed, and hence, the effective output conductance of the transconductor also scales with the duty cycle. Since both *gm* and g_o scale at the same rate, if transconductor *gm* dominates g_o when no duty cycle is present, then it will still dominate in the proposed topology. So the distinct advantage of this topology is that no additional design of the transconductor for low g_o values is required.

4.2 Complete Low-Pass Filter

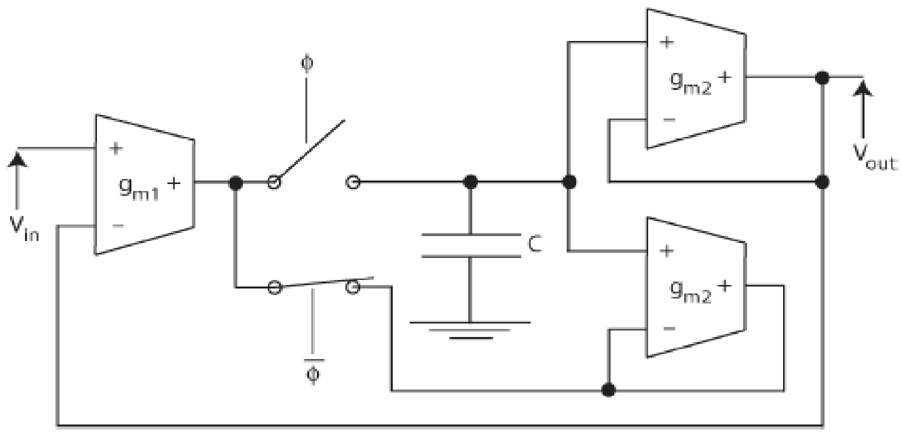


Fig 4.2 The complete block diagram low-pass filter with two buffers for ultra low power application

Practically, the Fig. 4.1 does not obey Kirchoff's current law, when the switch is open; the output current of transconductor has no path to flow. This would cause the output of the transconductor to saturate at (or near) the supply rails as no output current could be provided. To overcome this, two buffer cells are introduced, as shown in Fig. 4.2. The first buffer is placed between the capacitor and the output/feedback node V_{out} to isolate the capacitor node from the load. The second buffer is then placed between the output of the filter transconductor $gm1$ and the capacitor via a second switch $\bar{\varphi}$ in opposite phase to the main switch. This second buffer thus provides a path for the output current of $gm1$ when the φ switch is open. When φ is open, $\bar{\varphi}$ is closed, and the output of $gm1$ is fixed to the same voltage as the capacitor but without any current from $gm1$ flowing into the capacitor. Thus, the voltage at the output of $gm1$ stays approximately constant regardless of whether the current from it is flowing into the capacitor or not, preventing the output of the transconductor changing between the supply rail voltages and the voltage at the capacitor each time the switch is toggled.

This topology also reduces the effects of charge injected through the switches. When φ switches, charge is predominately injected into capacitor C because it offers the lowest impedance. For low-frequency operation, C is generally large. This results very small voltage spikes. When $\bar{\varphi}$ switches, charge is predominately injected into a buffer connected in negative feedback. The load capacitance seen is thus both the buffer output capacitance and the input capacitance of the negative input, increasing the total capacitance present. Additionally, both switches can operate at frequencies much higher than the bandwidth of the filter, and therefore, the remaining voltage ripple can be easily removed if required.

4.3 Schematic description of proposed low-pass filter

Circuit of low-pass filter basically consists of a transconductance amplifier, two buffers, one capacitor and a switch. Fig 4.3 shows complete schematic diagram of low-pass filter. Each element of low-pass filter has been discussed below briefly.

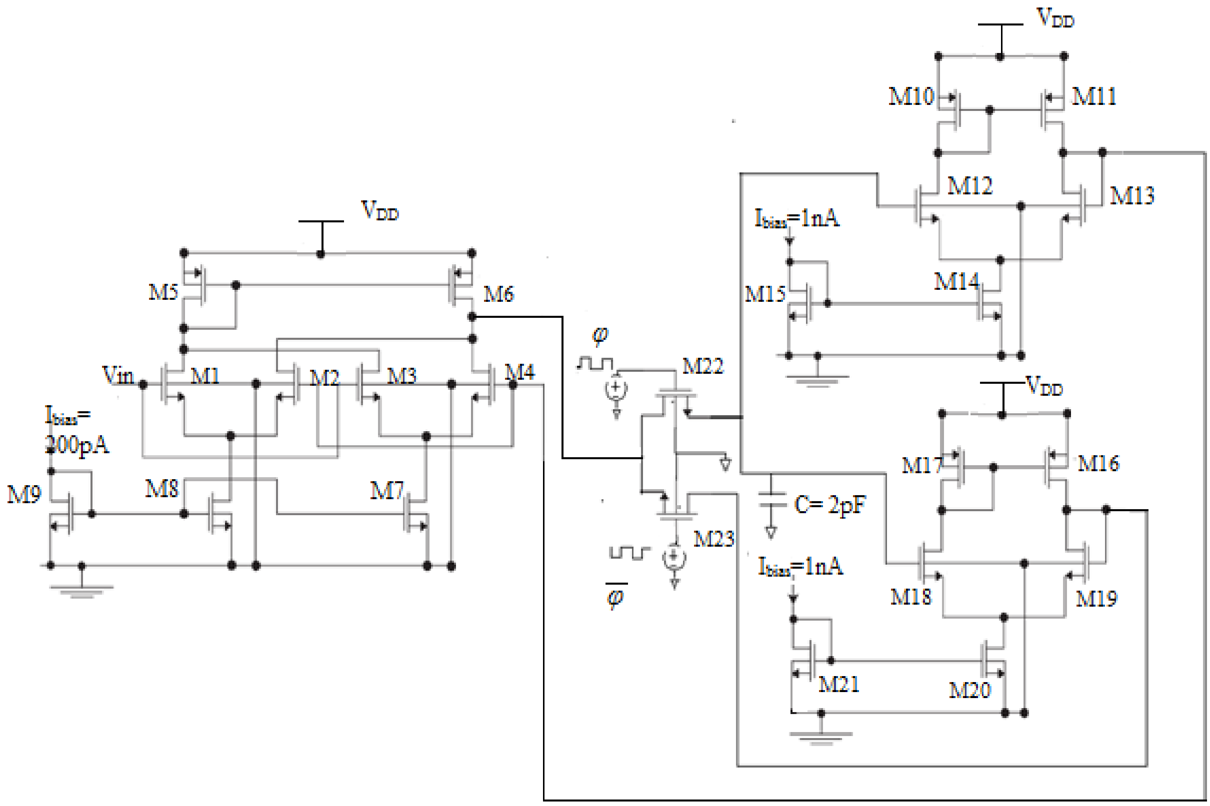


Fig4.3 Complete schematic of filter structure

4.3.1 Implementation of *gm1* of proposed topology (transconductance amplifier)

The schematic diagram of gm_1 transconductor, as shown in Fig 4.5, consists of two differential pairs connected in a doublet arrangement. The design of operational transconductance amplifier is with focus on the realization of small transconductance. The four cross-coupled differential pair is used as an input stage, which M1 and M4, M2 and M3, respectively, the bias current I_{biasl} and I_{bias2} are different. The schematic diagram of cross coupled differential pair is shown in Figure 4.4.

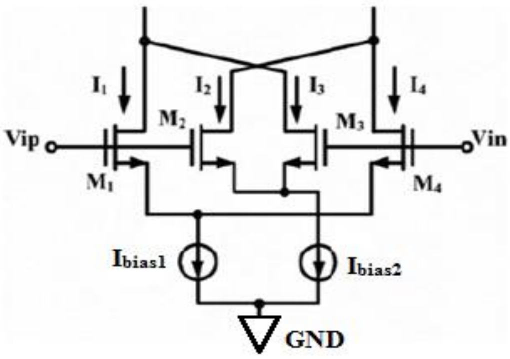


Fig 4.4 Proposed Cross coupled differential pair.[3]

In order to control the input-stage transconductance more precisely, and combined with the characteristics of the small value, the transistors in cross-coupled differential pair are biased in the sub-threshold area. The transconductance and the bias current have a linear relationship in a wide range.

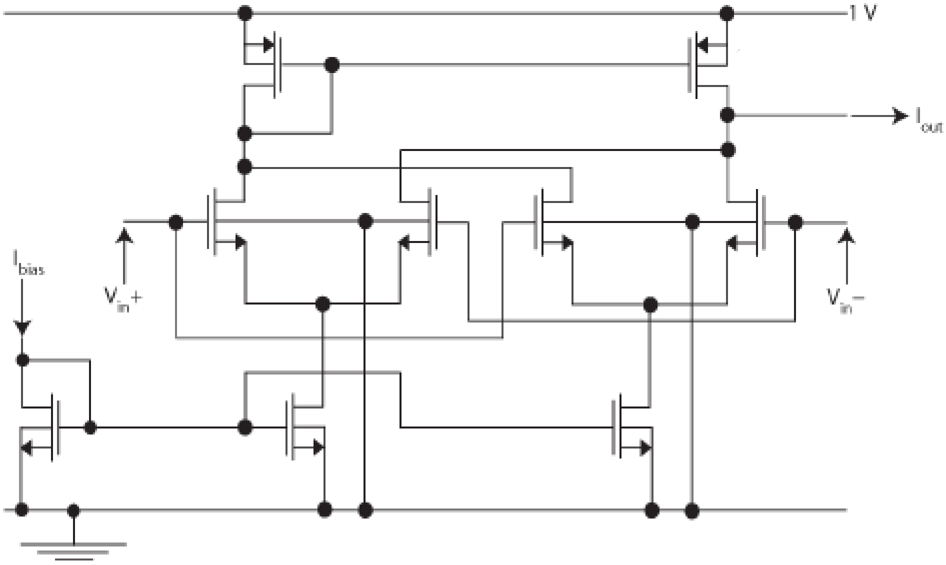


Fig 4.5 Filter having transconductance *gm*1 schematic implemented in CMOS

Implementation of buffers of proposed topology

The *gm*2 transconductors are buffers, as shown in Fig. 4.6. It consists of basic differential pairs with their outputs connected to the negative inputs for unity voltage gain. The bias current is set at 1 nA, and since these buffers operate well below their bandwidth, their inputs are approximately equal and they contribute very little to distortion in the overall filter.

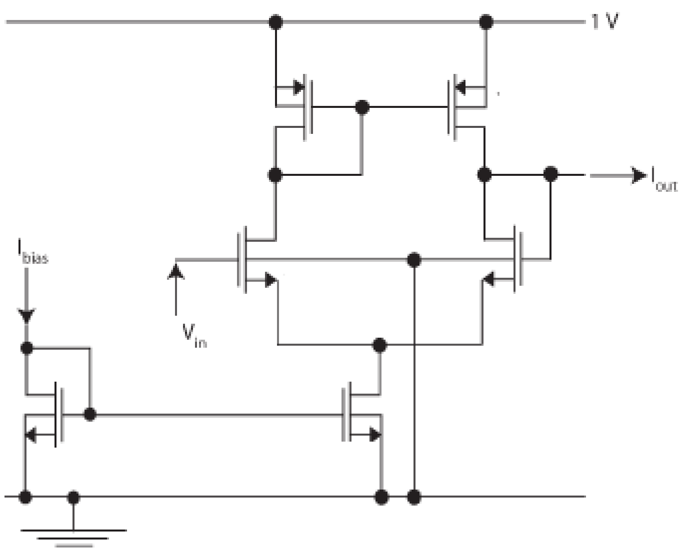


Fig 4.6 Buffer Filter having transconductance *gm*2 schematic implemented in CMOS

In this filter structure two buffers of same configuration are used to make circuit practically feasible. Buffer 1 consists of transistor M10- M15 and buffer 2 consists of M16 –M21.

4.3.2 Implementation of non overlapping clock switch of proposed topology

The switches φ and $\overline{\varphi}$ are implemented as single minimum-sized nMOSFETs shown in fig 4.7. Gate of NMOS is connected with opposite pulse input signal .

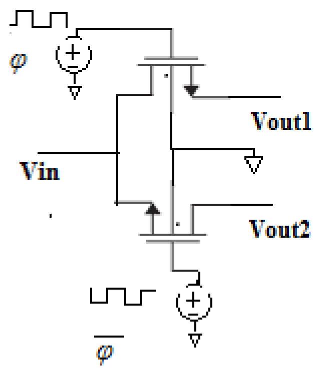


Fig 4.7 Switch used for implementing non inverting clock

4.4 Specifications

Following is the Specifications for designing and Technology parameters and CAD tools to be used in the design of proposed low-pass filter.

Design Specifications:

Table 4.1 Various design specifications of filter.

Parameters	**Values**
Technology	**Cadence UMC_180nm Technology**
Supply voltage	**1V**
Gain	**0 dB**
Power	**<10n*W***
ICMR	**0.031-0.9**
-3 dB frequency	**10Hz**
Load capacitance	**2pF**

Technology Specifications:

Foundry Specification: UMC 0.18 µm twin-tub CMOS 1P6M process

Voltage range: 0V-1.8V ± 10%

SPICE Models: BSIM3v3 (Level 49)

CAD tools:

Schematic Entry : Cadence Schematic Entry Analog Design Environment

Simulator : Cadence SPECTRE and Synopsis HSPICE

4.5 Designing of low-pass filter circuit

The proposed low-pass filter circuit is design for very low power hence MOS of this circuit is working in subthreshold region. So in next section parameter extraction of MOS in subthreshold region by graphical method is going to be explained.

4.5.1 Behaviour and model of MOS transistors in weak inversion:

Symbol specification

W,L = width, length of the channel

C_{ox} = gate capacitance per unit area

μ = mobility of carriers

$V_T = kT/q$ (= 26 mV at 300°K)

V = local non-equilibrium voltage in channel: channel voltage

(Quasi-Fermi potential of electrons)

- at source end of channel: $V = V_S$
- at drain end of channel: $V = V_D$

Qi = local mobile inversion charge in channel (electrons)

V_{T0} = gate threshold voltage for V=0.

Drain current of MOS transistor is,

$$I_D = \beta \int_{V_S}^{V_D} -\frac{Q_i}{C_{ox}}\, dV \qquad (4.3)$$

Where $\beta = \mu\, C_{ox} \frac{w}{l}$

Weak inversion already possible for $V_T = 0$ if $V_{GS} < V_{T0}$ ("subthreshold")

$$\frac{-Q_i}{C_{ox}} = 2nV_T e^{\frac{V_P - V}{V_T}} \ll 2nV_T \qquad (4.4)$$

Therefore,

$$I_F = I_S e^{\frac{V_P - V}{V_T}} \qquad (4.5)$$

Where I_S is specific current of transistor.

$$I_S = 2n\beta {V_T}^2$$

I_S varies from 10 to 300nA for W=L

$$V_p \cong \frac{V_G - V_{T0}}{n} \qquad (4.6)$$

$$I_F = I_S \frac{V_G - V_{T0}}{nV_T}\left[e^{\frac{-V_S}{V_T}} - e^{\frac{-V_D}{V_T}}\right] \qquad (4.7)$$

$$I_D = I_{D0}\ \frac{V_G}{nV_T}\ \ [e^{\frac{-V_S}{V_T}} - e^{\frac{-V_D}{V_T}}] \qquad (4.8)$$

Where $I_{D0} = I_S e^{\frac{-V_{T0}}{nV_T}}$.

$$I_D = I_0\ \frac{w}{l}\, e^{V_{GS} - V_T/_{n}V_T}\left(1 - e^{-V_{DS}/_{nV_T}}\right) \qquad (4.9)$$

4.5.2 Parameter extraction of MOS in subthreshold region:

The transistors are traditionally biased in the saturation mode in analogue circuits. But, they can be operated in strong inversion or weak inversion. Subthreshold equation of MOS in weak inversion is given in equation (4.9).

Subthreshold parameters (I_0 and n) of MOS in weak inversion can be calculated experimentally using I_D and V_{GS} curve in weak inversion region. Parameter extraction (I_o and n) for NMOS in subthreshold region is given here.

Step 1 : Subthreshold slope factor ‘n’ extraction

Step 1(a) Subthreshold parameter ‘n’ is normally measured from the slope of linear region $\ln(I_D)$ and V_{GS} curve in weak inversion region. This curve is also derived by differentiating the drain current in subthreshold region with respect to V_{GS} i.e. slope is obtained by differentiating equation (4.10) and is given as

$$slope = \frac{1}{n\,V_T} \qquad (4.10)$$

Where V_T is thermal voltage which is 25.9mV.

Step 1(b) Now put the value of slope in above equation and calculate n from it since V_T is known.

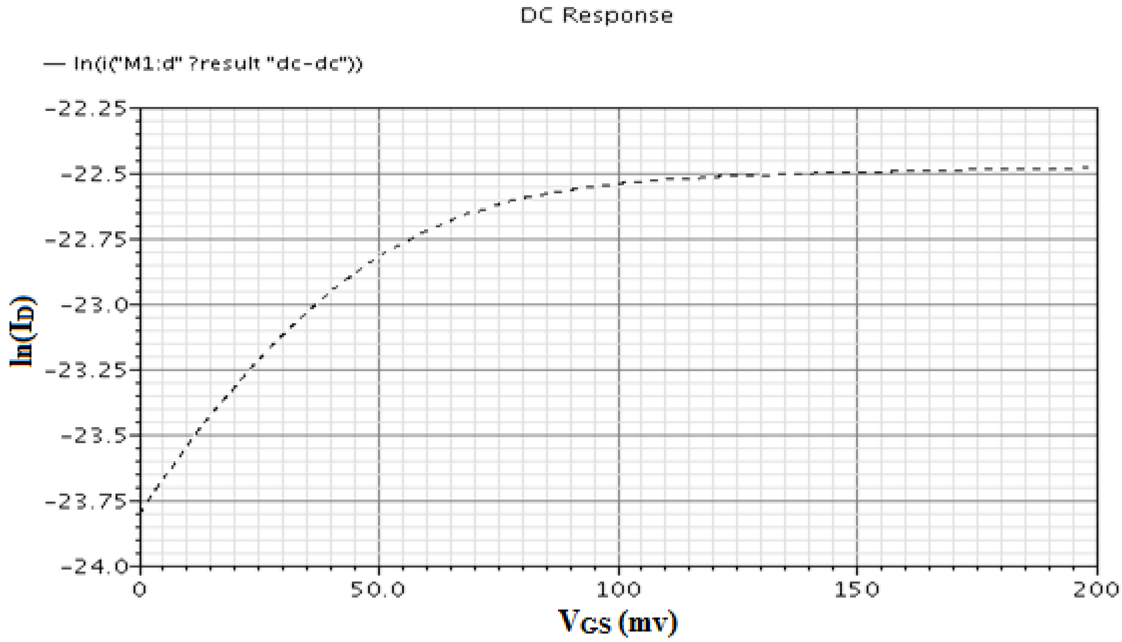


Figure 4.8 ln(I_D) and V_{GS} curve in weak inversion region

From equation (4.2), slope is calculated from linearized area of curve hence subthreshold parameter 'n' can be calculated as **n= 1.02**

Step 2 Procedure for calculating I_0:

Step2 (a) For calculation of I_0 , select four to five set of values of V_{GS} and corresponding values of I_D from Id V_{GS} curve in weak inversion region.

Step 2 (b) Then calculate the value of I_o using equation (4.1) for each set of values (use calculated value of n from step 1).And then averaging all values to get final value of I_o.

For example table 4.1 shows the different values of I_0 .

Table 4.1 Values of current and voltages from I_D vs V_{GS} curve.

V_{GS}(V)	**I_{DS}(nA)**	**I_o(nA)**
0.2	10.46	122
0.225	25.88	118
0.25	57.55	102
0.275	128	88
0.3	265	71

Average value of $I_o = 100.2nA$.

Now I_0 and n are known simply by applying overdrive I_D will be achieved. This way current across each MOSFET has been calculated in subthreshold region. Width and length of the MOSs are calculated by putting values of n, I_0 and other parameters.

For calculation of w and l of transistor

n= 1.794

I_0= 181.78 nA

I_D= 1 nA

Assuming V_{GS}-V_T = 0.2 V

V_{GS}=V_{DS} (for this transistor)

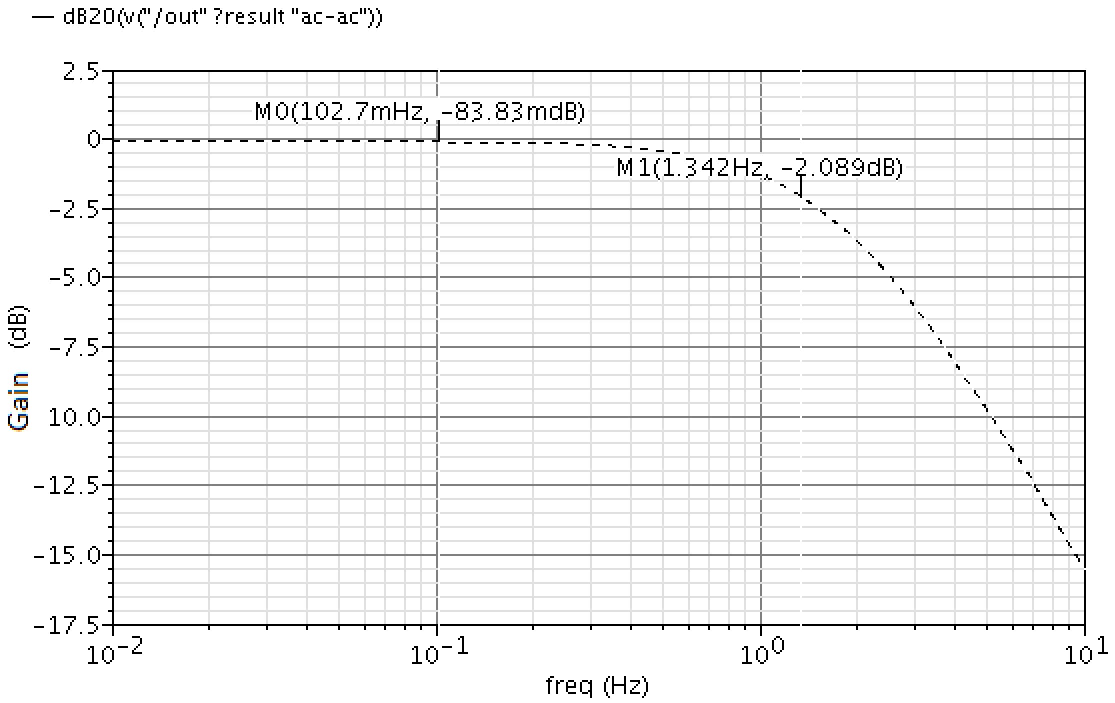
V_{DS} = 0.2 + 0.316 = 0.516

Now by using I_D current equation for subthreshold conduction w and l can be find out.

Here w = l = 129 µm .

4.6 Gain and Phase response of Proposed Low-pass filter:

The circuit is connected in unity gain configuration hence gain of the transistor is unity i.e 0dB. And -3 dB frequency is 1.342 Hz as shown in gain curve of filter shown in Fig 4.9(a).



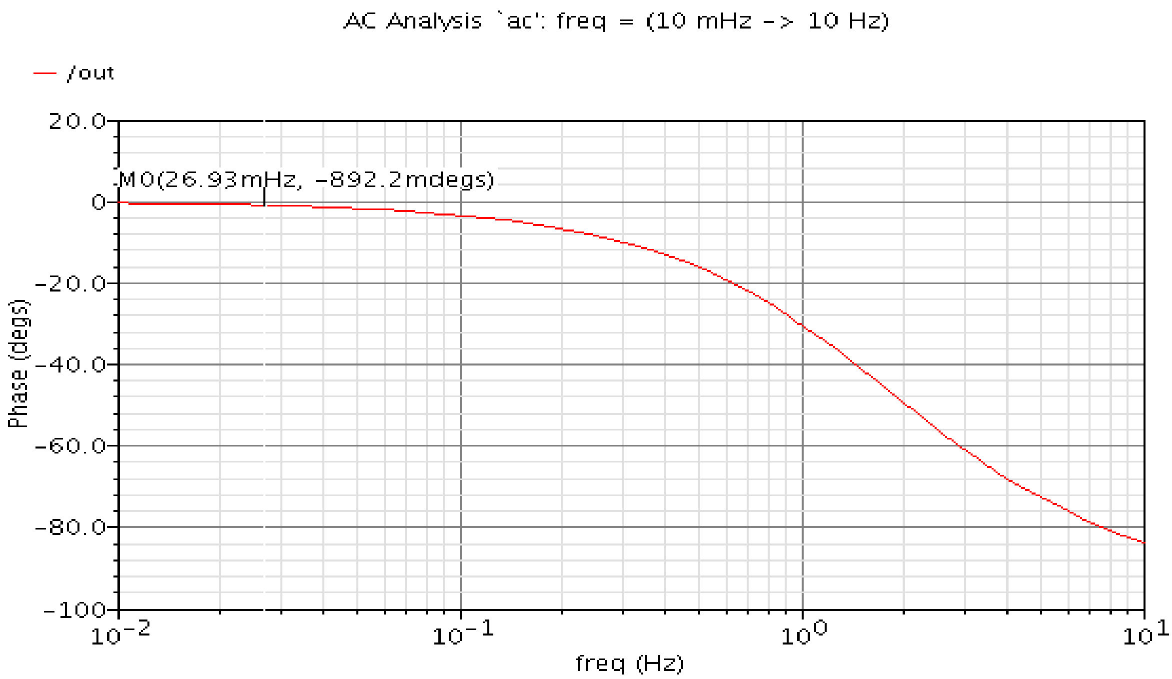


Fig4.9(a) Gain characteristic of proposed low-pass filter

Fig4.9 (b) phase characteristic of proposed low-pass filter

4.7 Performance parameter measurement

The OTA is characterized by various performances like open-loop voltage gain, unity-gain bandwidth, slew rate, ICMR, PSRR and so on. These performances measures are fixed by the design parameters, e.g., transistor sizing, bias currents, and other component values.

4.7.1 PSRR measurement

For the measurement of PSRR, op-amp is connected in unity gain feedback, a DC bias is connected to input and AC signal at VDD terminal for PSRR measurement. Setup for PSRR measurement is shown in figure 4.11 and PSRR response in figure 4.10

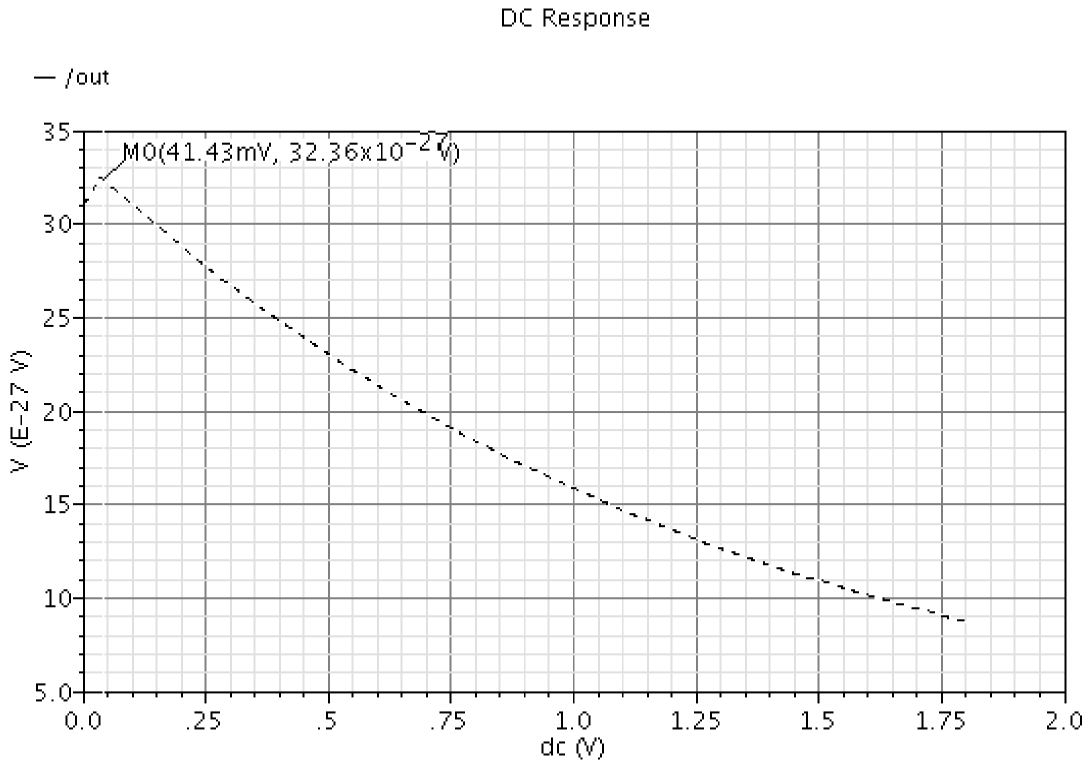


Fig 4.10 Plot for calculation of PSRR of filter

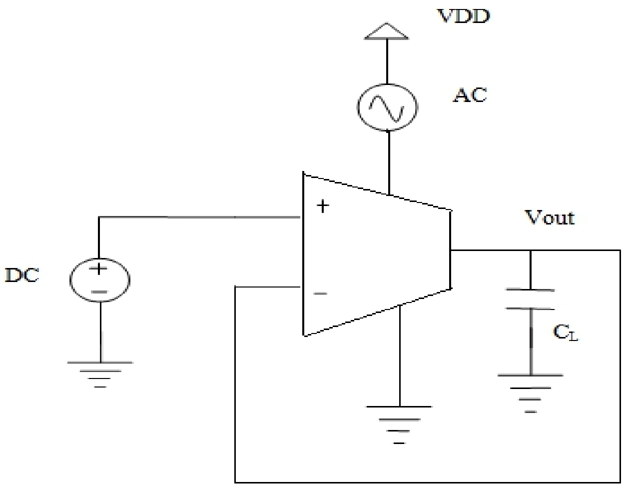


Figure 4.11 Setup for PSRR measurement

4.7.2 ICMR measurement:

For ICMR measurement apply variable DC voltage at input of amplifier in unity gain configuration as shown in figure 4.12 and its response is shown in figure 4.13. From this plot shown in figure 4.13 ICMR (max) is 0.998V and ICMR (min) is 0.391V.

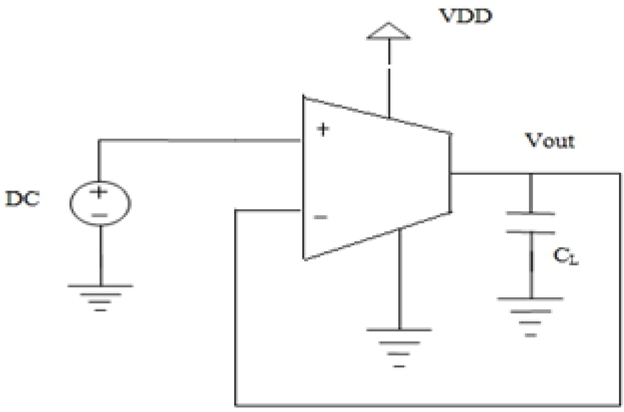


Fig 4.12 Setup for ICMR measurement

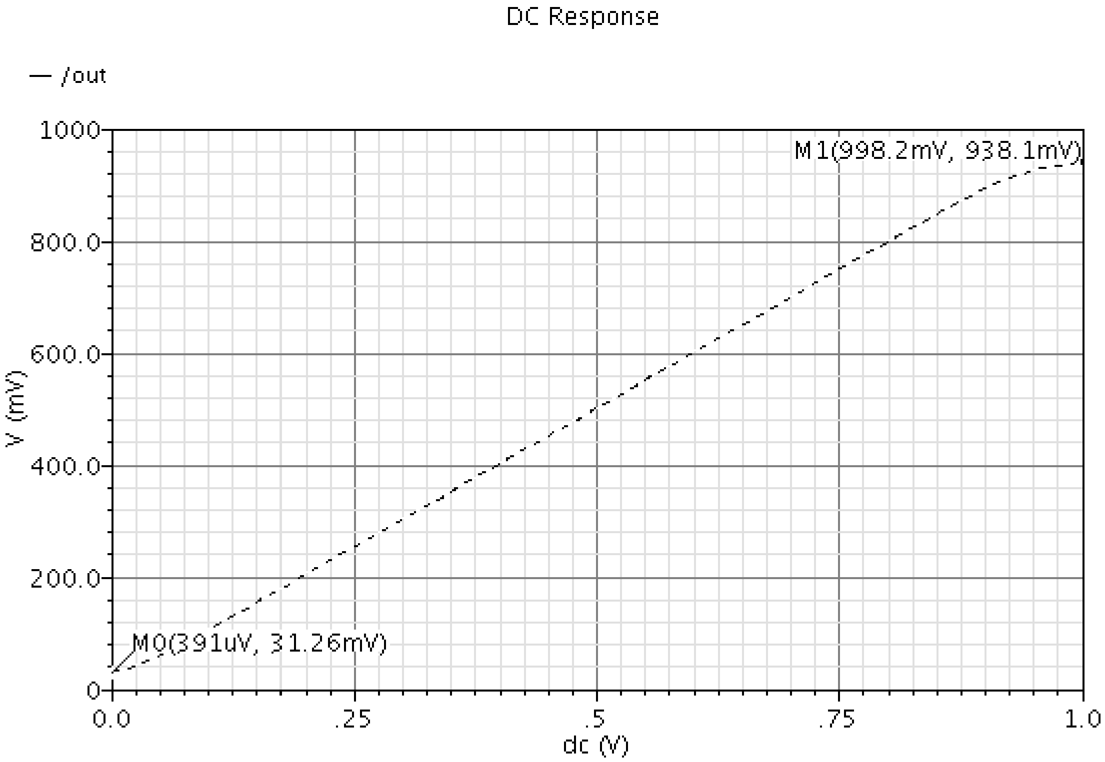


Fig 4.13 Plot for calculation of ICMR of filter

Table 4.1 Various design parameters of filter.

Parameters	**Values**
Technology	Cadence UMC_180nm Technology
Supply voltage	1V
Gain	0 dB
Power	4.712n
-3 dB frequency	1.34Hz
PSRR	0.41V
ICMR	0.031-0.938
Load capacitance	2pF

4.8 Layout of proposed low-pass filter:

Semiconductor foundry allows the designers to design only the layout pattern on the top view. In this thickness of layers are fixed by the semiconductor foundry. The designers have to design the layout according to design rules which is fixed for each technology. The purpose of design rule is as follows.

i) Warranty of dimensional precision in micro fabrication

ii) Warranty of precision on electrical characteristics

iii) Prevention of latch-up

Design rule violation is automatically detected and reported in DRC (Design Rule Check).A semiconductor company accepts only the design that is passed the specified design rules.

Verifications of the layout design have three steps

• DRC (Design Rule Check)

– Detection of the design rule violation

• ERC (Electrical Rule Check)

– Detection of the open/short error

• LVS (Layout VS Schematic)

– Equivalence checking between layout and schematic

Steps for LVS exercise

1. Draw schematic/simulate
2. Draw layout
3. Extract schematic and layout to SPICE netlist
4. Run LVS tool to compare netlists
5. Interpret output to spot differences
6. Fix layout (or maybe schematic) – iterate to 3.

Note: LVS has many options, e.g. check transistor geometry, check R & C values, collapse stacked logic – so make the about of the usage of reasonable options. The layout design checker has a batch processing mode and interactive mode.

Layout of Low-pass filter is divided in three blocks for simplification

1. Transconductance amplifier
2. Buffer
3. Switch with capacitor

Layout of the Transconductance amplifier, buffer and switch with capacitor shown in fig 4.13(a), (b), (c) respectively . Due to subthreshold conduction sizes of the transistors are large.

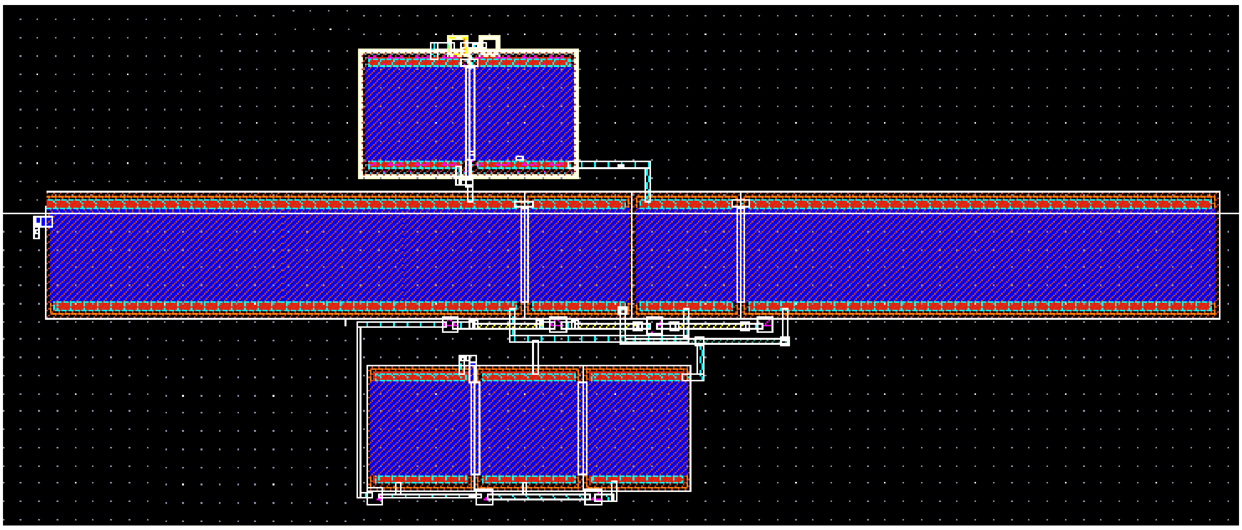


Fig 4.14(a)layout of transconductance amplifier

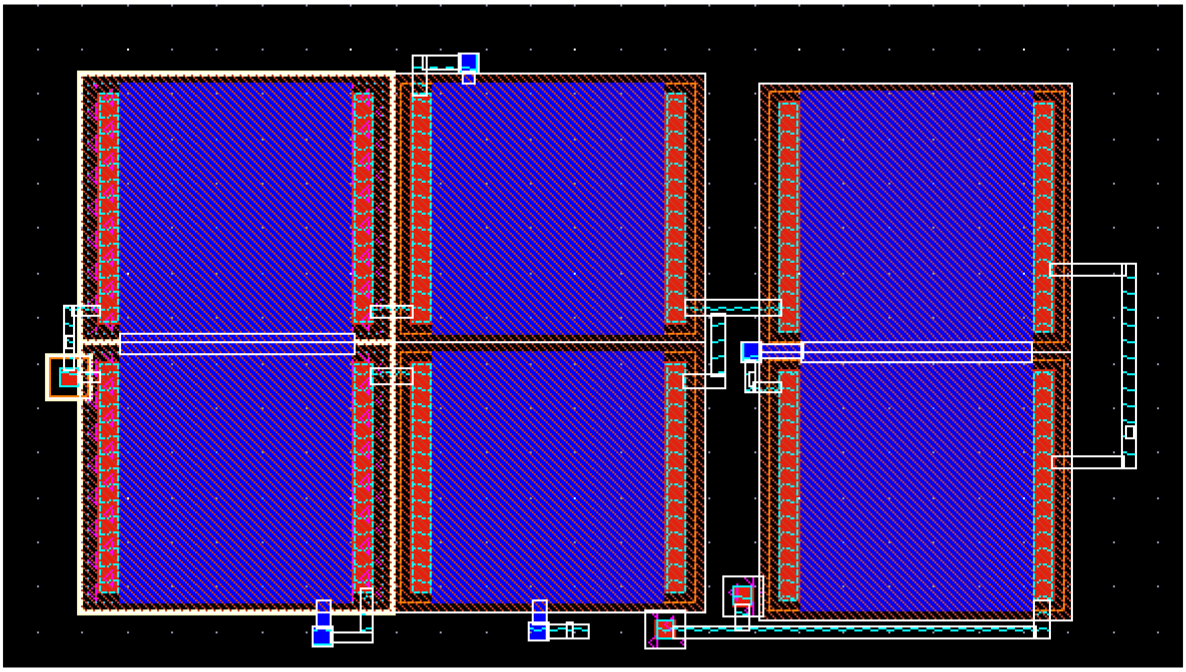


Fig 4.14(b) layout of buffer

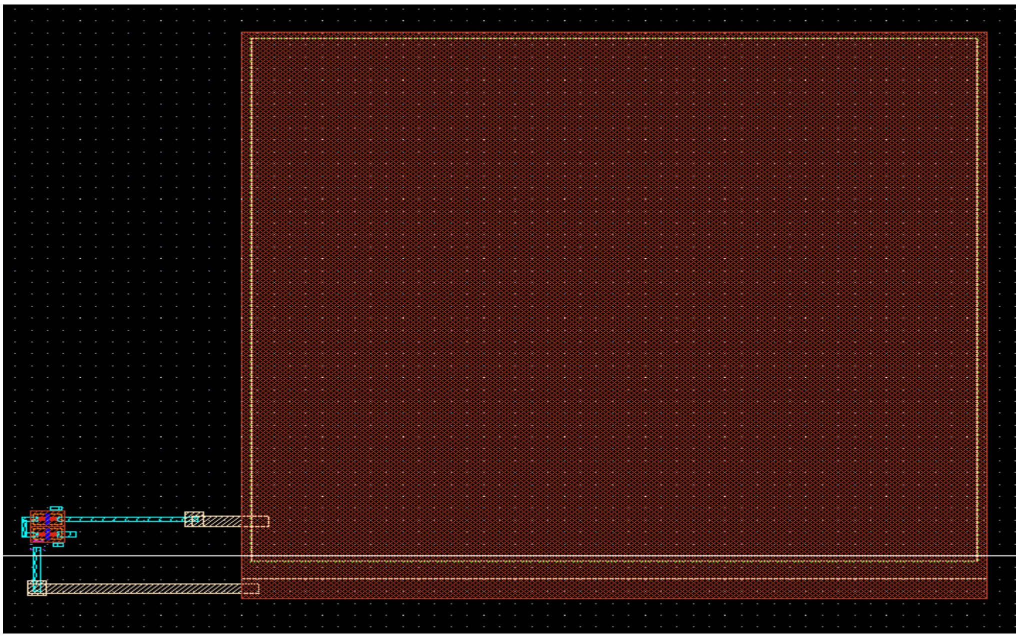


Fig 4.14(c) Layout of switch with capacitor

Layout for low-pass filter has been drawn as shown in Fig 4.14. Design is verified with steps DRC and LVS.

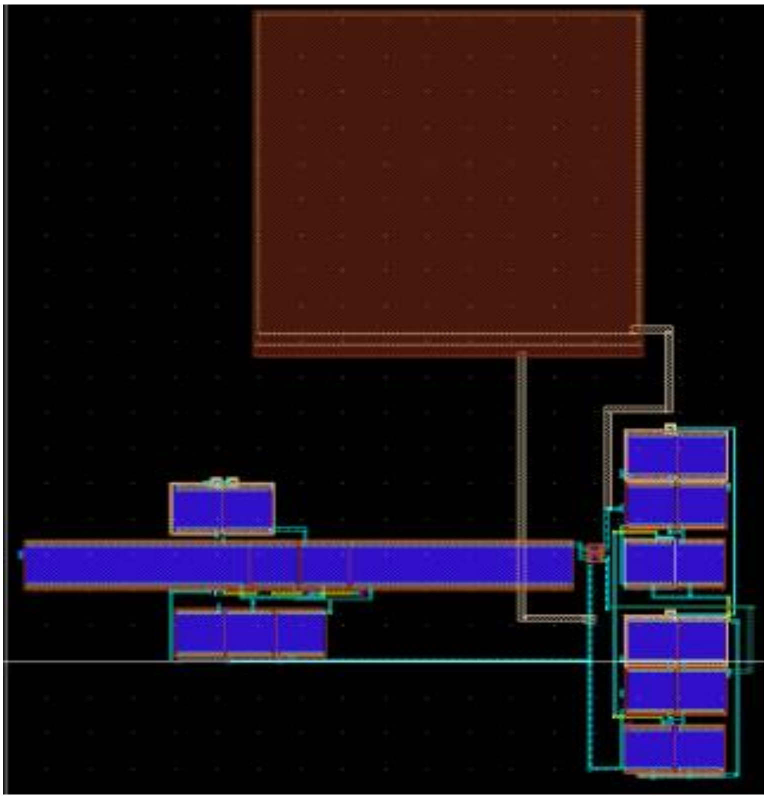


Fig 4.15 Layout of proposed low-pass filter circuit.

Metal-Insulator-Metal (MIM) Capacitor is used as load capacitance. Its size increases with decrease in capacitance. A Metal-Insulator-Metal (MIM) capacitor structure and method of fabricating the same in an integrated circuit improve capacitance density. In a MIM capacitor structure by utilizing a sidewall spacer extending along a channel defined between a pair of legs that define portions of the MIM capacitor structure. Each of the legs includes top and bottom electrodes and an insulator layer interposed there between, as well as a sidewall that faces the channel. The sidewall spacer incorporates a conductive layer and an insulator layer interposed between the conductive layer and the sidewall of one of the legs, and the conductive layer of the sidewall space is physically separated from the top electrode of the MIM capacitor structure.

Comparison of simulation results of this filter with previous literature

Low-pass filter of 4.712nW power is achieved with cut-off frequency 1.342Hz, which is improved version of previous data. Comparison of obtained result from previous research has been shown in table 4.1 below.

Table 4.3: Comparison of the proposed topology performance with other reported low-frequency low-pass filters

Ref	[16]	[9]	[18]	[17]	[19]	[23]	[20]	[21]	[22]	[24]	[25]	[2]	This work
CMOS process (µm)	0.35	0.80	0.35	0.80	0.35	0.80	0.35	0.50	1.20	0.80	1.00	0.35	0.18
Minimum Cut-off/Hz	35	2.4	1.5	0.5	0.5	0.30	0.25	0.18	0.17	0.1	.075	.002	1.342
Filter Order	1	6	2	2	1	1	2	1	2	1	1	1	1
Power Consumption/W	-	10µ	165 µ	2 µ	-	113 N	-	77.4 n	8.2 µ	230n	-	5n	4.712 n
Supply Voltage / V	3.2	3.0	3.3	1.5	-	-	3.0	-	2.7	3.0	5.0	1.0	1.0
Integrating Capacitance/F	25f	5p	52.5 p	-	100f	50p	29p	15p	10n	70p	10p	40p	2p

Chapter 5

Conclusion and Future Scope

Conclusion

There is a great demand of low frequency low pass filter in biomedical and sensor technology at the same time low power consumption is great challenge. Through OTA, filter design become simple hence in this design technique OTA as a basic active element has been discussed.

The device designed collects cardiac data and monitors hearth and circulation activity. It is built into the human body. The device is therefore must be realized as an integrated circuit. A very low frequency low-pass filter for power ranges of nW has been designed . This design shows excellent characteristics when compared with results in the literature. Operation is based on using a switch at the output of a transconductor in a g_m/C filter to decrease the value of the transconductance and to increase the output resistance. This allows very low transconductance values to be achieved, and the clock signal facilitates easy digital tuning. Measured results showing that the current draw of 4.712 nA. In comparison to previous low-pass filters from the literature, the proposed topology provides the lowest power consumption, in addition to a very wide tuning range. In this, the proposed filter circuit has been designed at 0.18μm Technology.

Through low frequency demands, large capacitors must be used, which is very difficult to achieve on silicon wafer. MIM capacitor of such high valued capacitors is used.

Future scope

This work can be extended to designing of low pass filter with low frequency and low power in the future. However, the basic need in order to design low pass filter for low power is to minimize the power of OTA. The proposed clocked transconductor topology is thus highly suitable for use in low power, low-voltage sensor interfaces and in portable medical instrumentation. This can further be used for lower cut-off frequency and power. And since it is 1st order filter so for improved performances higher order filters for few nW power can be designed using this topology.

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