

Design and Development of Dual Channel ECG Simulator and Peak Detector

A thesis

submitted towards the partial fulfillment of

requirements for the award of the degree of

**Master of Engineering
(Electronic Instrumentation & Control)**

Submitted by

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Declaration

I hereby declare that the report entitled “Design and Development of Dual Channel ECG Simulator and Peak Detector” is an authentic record of my own work carried out as requirements for the award of degree of M.E. (Electronic Instrumentation & Control) at Thapar Institute of Engineering & Technology (Deemed University), Patiala, under the guidance of Mr. Mandeep Singh, Assistant Professor and Mr. Nirbhowjap Singh, Lecturer during January to June 2006.

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Abstract

For the training of Doctors as well as for design, development and testing of automatic ECG machines, a subject with a known abnormality of heart is essentially required. ECG Simulator is an electronic device used to simulate such subject for the above-mentioned purpose. The significance of the ECG simulator is that the subject has been replaced by the Data File. In this project dual channel ECG Simulator has been designed, developed and implemented. The waveforms can be displayed on the PC monitor as well as output through a parallel port of the PC. Subsequently these can be displayed on digital storage oscilloscope. The simulated electric waves are presented to electronic peak detectors. The detected peaks exactly tally with the annotated peaks in the given ECG database; thereby authenticating its efficacy. Prerecorded ECG Signals with known diagnostic truths were obtained from MIT-BIH ECG database. Two channel recordings were simulated, with a novel way to segregate the combined text file to two different analog output channels. The simulator produces realistic ECG with the possibility of including other biological signals, e.g. blood pressures. This program can be used as a teaching tool as well as for testing ECG monitors.

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List of Abbreviations

- AV Atrioventricular.
- ADC Analog to Digital Converter
- BPP Bidirectional Parallel Port
- CMOS Complementary Metal Oxide Semiconductor
- DAC Digital to Analog Converter
- DSO Digital Storage Oscilloscope
- DAQ Data Acquisition
- DMA Direct Memory Access
- DTL Diode Transistor Logic
- ECG Electrocardiogram
- EPP Enhanced Parallel Port
- ISA Industry Standard Architecture
- IOPL Input Output Privilege Level
- I/O Input Output
- LED Light Emitting Diode.
- LPT Local Printer Terminal
- MIT-BIH Massachusetts Institute of Technology.
Beth Israel Hospital
- PC Personal Computer
- SA Sinoatrial
- SPP Standard Parallel Port
- TTL Transistor Transistor Logic
- TSS Task State Segment
- USB Universal Serial Bus

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Chapter 1: Introduction to ECG Simulator

1.1 Introduction

For clinical training of doctors to interpret the ECG of a Subject with proved diagnosis (i.e. the exact status of subject's heart is known through the clinical truths) we require the Subject, ECG amplifier and Monitor. The availability of such subject may not be practically feasible in all situations. The Doctors therefore have to mainly rely on recorded signals, which do not give the real time experience to the Doctors.

The trend these days is to build intelligent ECG machines, which automatically detect and classify any abnormality in the ECG signal. For design, development and testing of these automatic machines, again the presence of the subject with the proved diagnosis is required. An ECG simulator is device, which can simulate all types of signals recorded previously in the real time mode. This simulator can be used both for clinical training of doctors as well as for design, development and testing of automatic ECG machine without having real subject for this purpose. Such ECG simulator has been designed for this project.

1.2 Components of ECG simulator

Apart from the **Personal computer (PC)**, the system making use of ECG Simulator has basically three components: - **DAC chip (0808)**, **Channel selection** (sample and hold circuits), **QRS Detection section** (using notch filter).

DAC is a device for converting a digital (usually binary) code to an analog signal (current, voltage or electric charge). Digital-to-analog converters are the interface between the abstract digital world and the analog real life. Simple switches, a network of resistors, current sources or capacitors may implement this conversion.

We have used DAC0808, 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity

and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy.

Channel selection

The ECG text file has two different columns for two leads. A program written in C/C++ segregates these two signals and using the most significant bit as channel identifier, two separate channels of analog output were obtained. The two separate channels are designed by using two LF398 sample and hold ICs connected at the output of the DAC0808. It is a monolithic sample-and-hold circuit, which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low drop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μs to 0.01%.

QRS Detection section

The most important part of the ECG wave is the QRS complex. The QRS complex is a waveform that correlates to the electrical flow through the bundle branches, from which heart rate and many other parameters can be measured. For QRS Detection, a narrow band pass filter has been designed for each channel by using 741 operational amplifier in inverting mode. The filter is designed to have the centre frequency 17 Hz and Quality factor of 2.83. It removes all signal frequencies except for a particular band (i.e. to record 14-20 Hz activity in ECG recordings). The frequencies occurring on either side of this band are not passed. The red colored LEDs at the output of filters remains off under normal operating conditions and flashes a specific number of times indicating which particular channel is selected and every time the occurrence of QRS complex (highest peak of the ECG signal).

1.3 Advantages of ECG Simulator

The use of Simulator has many advantages in the simulation of ECG waveforms, like saving of time and another one is removing the difficulties of taking real ECG signals with invasive and non-invasive methods. The ECG simulator enables us to analyze and study normal and abnormal ECG waveforms without actually using the ECG machine. The various advantages of ECG simulator are described below: -

1. No risk for patients.
2. Procedures and routine events can be practiced, such as the management of non-routine events that may be life threatening to the patient.
3. Participants learn to use the clinical devices directly on simulator without exposing real patients to risks.
4. Students can make mistakes without the supervisor having to intervene during the procedure.
5. The simulator session can be temporarily interrupted to highlight significant elements of the situation and to call attention to more suited treatment to be adopted.
6. Constructive criticism of individual and group performance under the guidance of instructor during review of recorded therapeutic intervention.

1.4 ECG Signal Basics.

The rhythmic behavior of the heart can be monitored and used as a diagnostic tool to detect heart abnormalities by acquiring the electrical activity on the body surface, across the heart, known as ECG. This electrical activity originates from the electrical activation of muscles in the heart, inherently indicating the approach of mechanical motion.

The electric potentials generated by the heart appear throughout the body and can be measured across its surface. Figure 1.1 displays the typical ECG waveform. An ECG signal is characterized by five peaks and valleys labeled in with the successive letters P, Q, R, S, T and U.

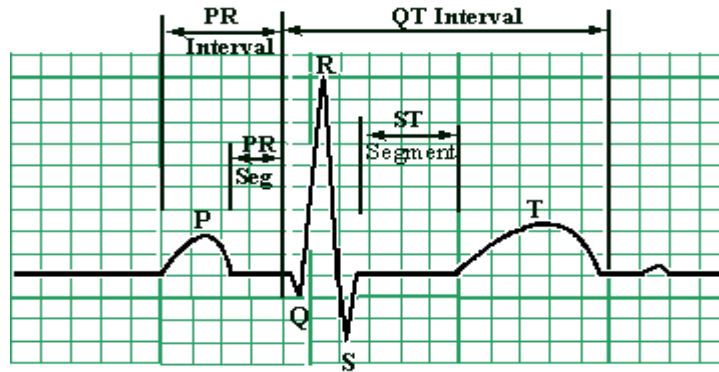


Figure 1.1: Typical ECG detailing the characteristic peaks and valleys.

An ECG signal is the superposition of action potentials that occur throughout the heart. A typical ECG signal for one heartbeat is shown in figure 1.1. An ECG is characterized by the P wave, the QRS wave and the T wave, with each wave created by specific heart activities. The P wave is produced by atrial depolarization, the QRS complex primarily by ventricular depolarization and the T wave by ventricular repolarization. Some ECG signal also contains small amplitude U wave following the T wave; U waves are common in slow heart rates but a prominent U wave may reflect a heart abnormality.

An ECG signal can also be broken down into three main intervals: the P-R interval, the Q-T interval and the S-T interval. The P-R interval is mainly caused by the depolarization of the atrium and slow conductance of the associated impulse to the ventricle by the atrioventricular (AV) node. The Q-T interval is defined by the depolarization and repolarization of the ventricle. The S-T interval corresponds to the “average duration of the plateau regions of individual ventricular cells.

1.5 50/60 Noise in ECG Signal

Signal degradation by 50/60 Hz noise (depending on the country) is a problem with ECG signals. This noise can be regarded as the result of an electromagnetic compatibility issue-background electromagnetic field (EMF) interference from surrounding equipment and from building power conduits corrupt the ECG signal. When recording an ECG signal signal’s path from the patient to machine cannot be completely

shielded from this background EMF, and other measures must be considered to either preserve or improve the ECG signal's quality.

An alternative to shielding would be to filter the signal after it has been sampled and digitized and before it has been displayed on the ECG unit. This solution is possible because the ECG signal and the 50/60 noises are uncorrelated signals. When attempting to solve the 50/60 Hz interference problems after sampling and digitization, several solutions can be considered. For example, 50/ 60 noise could be removed from the ECG signal through band pass filtering, or through the use of a very narrow notch filter.

However, each of these solutions has its drawbacks. Most of the information contained in an ECG signal found below 100 Hz, and substantial indiscriminate filtering could not be tolerated, in terms of preserving signal clarity.

In the case of notch filter, the frequency of the electric power of the ECG signal would have to remain relatively constant in order to remain within the notch of the filter. This problem since ECG signals generally has very small voltages, and signal power is at a premium. Therefore, it is the sensitivity of the signal processing that calls for adaptive filtering. Adaptive noise cancellation requires noise to be subtracted from a received signal using an adaptive process. The desired result is minimized signal to noise ratio. There are two main signals involved in adaptive noise cancellation: a primary signal and a reference signal.

1.6 ECG Amplifier

An ECG signal is usually in the range of 1mV in magnitude and has frequency components from about 0.05 – 100 Hz. To process this signal, it has to be amplified. For the measurement of the electrocardiogram and the other bioelectric signals, the Differential amplifier is used.

A differential amplifier can be considered as two amplifiers with separate inputs but with a common output terminal, which delivers the sum of two amplifier output

voltages. The main features of amplifier includes High Gain (about 1,000), 0.05 -100 Hz frequency response, High input impedance, Low output impedance.


1.7


Applications of ECG Simulator

The simulator facilitates the teaching and learning of clinical aspects that would otherwise be difficult or potentially dangerous to teach. Simulator aims to aid in the development of the capabilities of the individual health care workers in practical management and group interaction, thus improving patient safety.

Teaching and Training

- Technical Procedures
- Heart sounds and lung sounds
- Interactive physiological modeling
- Reducing the need for clinical training using real patients in socially difficult situations.
- Practicum for medical students during emergency medicine rotations

 Human performance evaluation (e.g., responding to simulated critical incidents in emergency room or operating room.

 Human factors engineering and usability engineering studies for medical equipment.

 Studies in cognitive engineering.

1.8 Layout of Thesis

This thesis is divided into various parts as mentioned above. Starting with the Introduction in Chapter 1, the Chapter 2 gives the details of ECG signal. In this chapter the ECG signal characteristics and applications of ECG is discussed. Chapter 3 deals

with the description of ECG Amplifier. Chapter 4 describes the ECG simulator hardware along with Channel Selection and QRS Detection. Chapter 5 presents the Software technique used in designing an ECG simulator. Chapter 6 shows the simulated Results and Observations of the thesis. Chapter 7 presents the Conclusion and Future scope.

Chapter 2: ECG Signal

2.1 Introduction

“ECG” (or EKG) stands for electrocardiogram; which is a measurement of the electrical signals that control the rhythm of the heartbeat. The heart is a muscular organ that beats in rhythm to pump the blood through the body. The signals that make the heart’s muscle fibers contract come from the senatorial node, which is the natural pacemaker of the heart.

The ECG is a method of recording the electrical activity of the heart. Each heartbeat is caused by a section of the heart generating an electrical signal which then conducts through specialized pathways to all parts of the heart. These electrical signals also get transmitted through the chest to the skin where they can be recorded.

An ECG is performed by placing 12 recording leads at certain specific locations on the body. They only record the heart's electrical activity. They do not produce any electricity of their own. The test does not hurt and has no known side effects. It does not require any preparation (except for possibly shaving chest hair to get a better recording). The recording itself takes only a few seconds. Including the setup time and the time to disconnect the leads, the whole procedure takes about 5 minutes.

In an ECG procedure, the electrical impulses made while the heart is beating are recorded and usually printed out on a piece of paper. This is known as electrocardiogram, and records any problems with the heart’s rhythm, and the conduction of the electrical signal through the heart, which may be affected by underlying heart disease.

An ECG can be used to assess if the patient has had a heart attack or evidence of previous heart attack. An ECG can be used to monitor the effect of medicines used for coronary artery disease. These are the main issues that ECG helps doctors with heart attacks. By looking at the electrical patterns on an ECG, doctor can determine the nature of an erratic heartbeat. There are many different types of abnormal heart beats. Not all require treatment. In those that do, the ECG recording lets the doctor know which treatment is best. The presence of a heart attack. It can also be determined whether the heart attack is old or recent. The possibility that there are narrowed arteries in the heart, which may lead to the heart attack in the future. Whether or not discomfort in the chest is being caused by the heart. Degeneration of the conduction system of the heart which can lead to dangerously slow heart beats.

This condition is often treated with a pacemaker. The cells that constitute the ventricular myocardium are coupled together by gap junctions, which for the normal healthy heart, have a very low resistance. As a consequence, activity in one cell is readily propagated to neighboring cells. It is said the heart behaves as a syncytium; a propagating wave once initiated continues to propagate uniformly into the region that is still at rest.

The equivalent fibers are a valid representation because they are consistent with the syncytial nature of the heart. In fact, because the syncytium reflects connectivity in all directions, we may choose the fiber orientation at our convenience (so long as the quantitative values of conductivity assigned to the fibers correspond to those that are actually measured).

2.2 ECG Signal- An Overview

As shown in figure 2.1, heart is divided into four chambers. The upper two chambers, left and right atria are synchronized to act together. Similarly the two lower chambers, the ventricles, operate together. The right atrium receives the blood from the veins of the body and pumps it into the right ventricle. The right ventricle pumps the blood through the lungs, where it is oxygenated. The oxygen-enriched blood then enters

the left atrium, from which is pumped into the left ventricle. The left ventricle pumps the blood into the arteries to circulate throughout the body.

The heart is a pump that pushes blood through the body. Blood enters the heart at a low pressure and leaves at a higher pressure. It is this high arterial pressure that provides the energy to force blood through the circulatory system. Bloods returning from the body is sent to the right side of the heart and then to the lungs to pick up oxygen and release carbon dioxide.

The oxygenated blood is then sent to the left side of the heart and back to the body, where oxygen is liberated and carbon dioxide is collected. The complete left/right division of the heart insures that there is no mixing of deoxygenated blood in the right side) with oxygenated blood (n the left side).

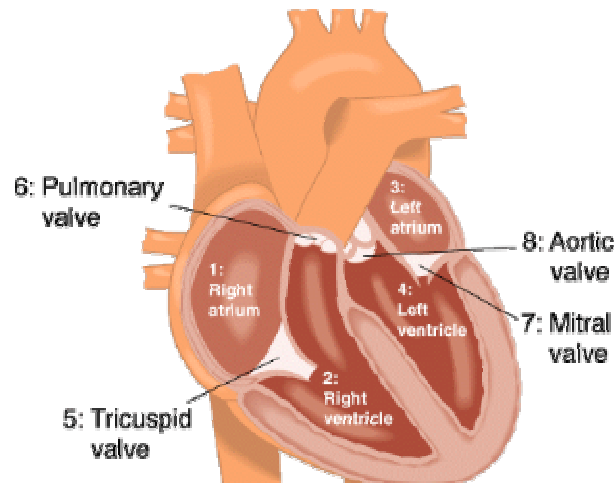


Figure 2.1: The compartments of the heart.

The mammalian heart is auto rhythmic, meaning it will continue to beat if removed from the body (and kept in an appropriate solution). Heart contractions are, therefore, not dependent upon the brain; rather, the rhythm comes from within the heart itself. The heart is composed almost entirely of large, strong muscle fibers, which are responsible for the pumping action of the heart. Other cardiac muscle cells are weakly contractile and produce the rhythm for, and conduct it to, the rest of the heart.

A group of these weak muscle cells is located in the sinoatrial (SA) node and acts as the pacemaker for the heart. These cells rhythmically produce action potentials, which

spread via gap junctions to fibers of both right and left atria. The resulting contraction pushes blood into the ventricles.

While adjacent atrial fibers are connected by gap junctions, the only electrical connection between the atria and the ventricles is via the atrioventricular (AV) node. The action potential spreads slowly through the AV node and then rapidly through the Bundle of His and Purkinje fibers to excite both ventricles.

The semi lunar valves are located between the ventricles and the artery on each side of the heart. In the relaxed heart, the high arterial pressure shuts the semi lunar valves and prevents back flow from the artery into the ventricles. Ventricular contraction increases the pressure of the blood in the ventricle (systole).

When the ventricular pressure is greater than the arterial pressure, the semi lunar valves open and blood flows into the artery. The myocardium then relaxes (diastole), the ventricular pressure declines, and the semi lunar valves close. The regular pattern of peaks produced by the heart repeats for each heartbeat. This pattern of potential peaks is called the electrocardiogram or ECG. The initial small peak, the P-wave, marks the contraction of the atria. The larger peaks following the P-wave, the QRS complex, is a superposition of atrial relaxation and ventricular contraction.

2.3 The Heart Rate and Rhythm

Figure 2.3 shows the compartments and electrical conduction system of the heart.

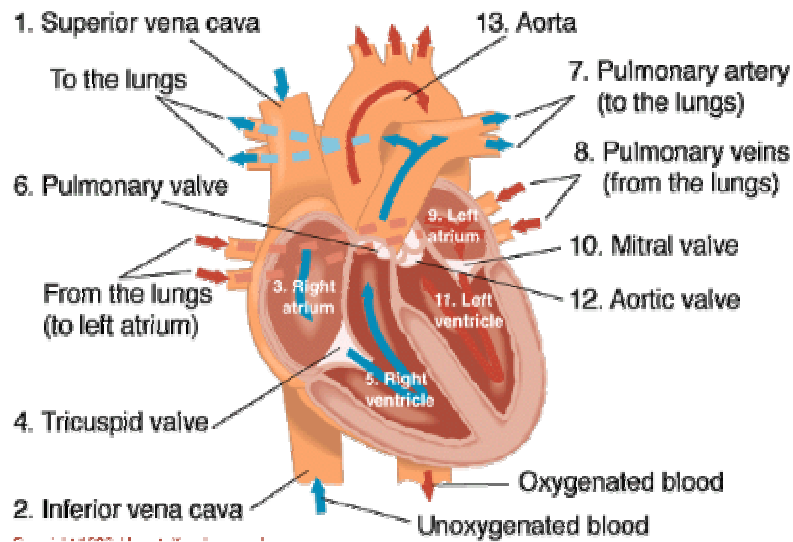


Figure 2.2: Basic conduction system of the heart.

Normally, the heart of an adult is depolarized 60 to 90 times per minute. A depolarization rate lower than this is called sinus bradycardia, while one that is higher is called sinus tachycardia. The heart rate of the normal newborn is much higher than that of an adult. The heart rate can be calculated by dividing the R-R interval into 60. This number is denoted BPM (Beats per minute).

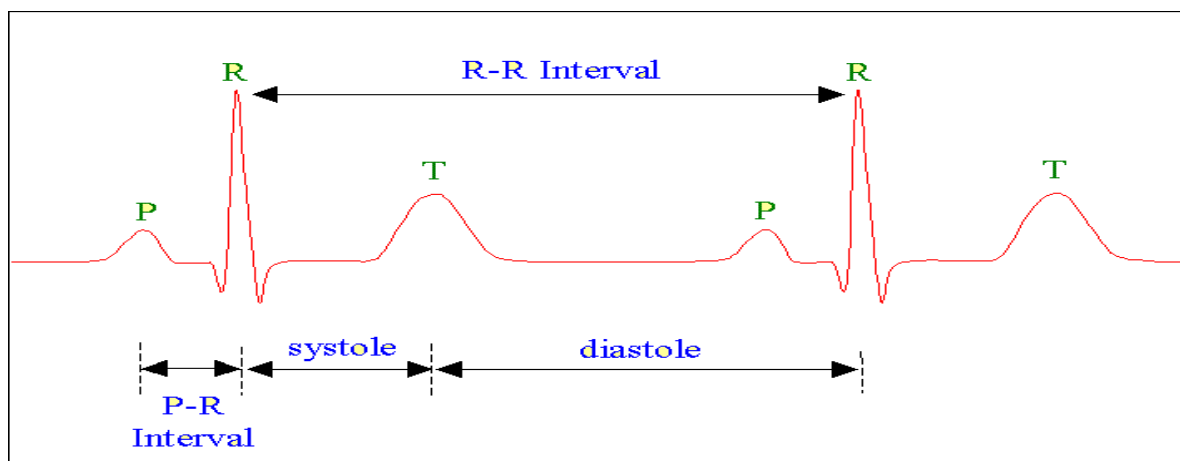


Figure 2.3: Definition of waves, segments and intervals in the normal ECG waveform.

2.4 The Duration of the Complexes and Interval

After determining the heart rate and rhythm, the clinician should measure the duration of the waves and intervals on the electrocardiogram.

2.4.1 Axis

The axis is the general direction of the electrical impulse through the heart. It is usually directed to the bottom left (normal axis: -30° to $+90^{\circ}$), although it can deviate to the right in very tall people and to the left in obesity.

- Extreme deviation is abnormal and indicates a bundle branch block, ventricular hypertrophy or (if to the right) pulmonary embolism.
- It also can diagnose dextrocardia or a reversal of the direction in which the heart faces, but this condition is very rare and often has already been diagnosed by something else (such as a chest X-ray).

2.4.2 The P wave

The duration of P wave is measured from the beginning of the P wave to the end. In normal adults, this period is usually less than 0.12 seconds; in neonates, it is less than 0.08 second. This is the time interval required for the wave of depolarization to spread through the atria and to reach the atrioventricular node. The amplitude of P waves of the normal adult is less than 0.25mV in the extremity leads and smaller than this in children.

2.4.3 The PR Interval

The PR interval represents the amount of time required for the depolarization process to spread from its origin in the sinus node, through the atria, to and through the atrioventricular node (where the impulses are delayed), down the bundle branches and their sub branches (including the purkinje fibers), and to the ventricular muscle. It is measured from the beginning of the P wave to the beginning of the QRS complex.

In reality, this interval should be called the PQ interval, but convention holds that it is called the PR interval. When there is no Q wave, the measurement is made from the beginning of the P wave to the beginning of the R wave.

The difference between the intervals as measured to the beginning of the Q wave, and as measured to the R wave, is usually about 0.02 second but may be as much as 0.04 second. The PR interval is less than 0.20 second in the normal adult and much less than this in normal children.

2.4.4 The Duration of the QRS Complex

The duration of the QRS complex represents the amount of time required for the depolarization of the ventricular musculature. It is measured from the beginning of the Q wave to the end of the S wave. In normal adults, the QRS duration is usually 0.10 second or less and in children, it is usually less than 0.08 second. When the QRS duration is greater than 0.10 second in adults, it is proper to consider the presence of some type of ventricular conduction defect.

2.4.5 QRS Amplitude

The normal QRS voltage may be as small as 0.5 - 0.7mV, but it is usually greater than this. IT is generally accepted that the QRS voltage is definitely small, when it measures 0.4 mV or less in all the extremity leads. When this occurs, it is wise to consider certain abnormalities as possible causes.

2.4.6 The Duration of the ST Segment

The duration of the ST segment represents the amount of time during which the ventricular musculature is depolarized. The depolarization process ends with the end of the QRS complex, and the repolarization begins with, or before, the beginning of the T wave. In some patients, the repolarization process begins during the ST segment.

The ST segment duration is determined by measuring the interval of time from the end of the S wave to the beginning of the T wave. In practice, a prolonged ST segment is identified by detecting a prolonged QT interval, while the duration of the T wave remains normal.

2.4.7 The QT Interval

The QT interval represents the amount of time required for depolarization of the ventricles, plus the amount of the during which the ventricles are excited (ST segment), plus the amount of the time required for their repolarization (T wave). This interval represents the duration of electrical systole, which is different from the duration of mechanical systole.

The QT interval is measured from the beginning of the Q wave of the QRS complex to the end of the T wave. The duration of the QT interval varies with age, gender, and heart rate. It should not exceed 0.40 second, when the heart rate of an adult is 70 depolarization per minute.

2.4.8 The Duration of the T Wave

The T wave is produced by the repolarization process. The duration of the T wave is measured from the beginning of the wave to the end. The repolarization process undoubtedly begins before the T wave and is sometimes quite visible as a displaced ST segment, which is referred to as “early repolarization.” Although the duration of the normal T wave has been studied, and tables have been constructed using the data, the actual measurement is rarely performed in practice.

2.4.9 The Magnitude of the T wave

The area encompassed by the T wave may be a little smaller or a little larger than that encompassed by the QRS complex; it is usually about two-thirds that of the latter. Characteristically, the upstroke of the normal T wave is less steep than the down stroke.

2.4.10 The TQ Interval

The TQ Interval is measured from the end of the T wave to the beginning of the next Q wave. During this period the ventricles are polarized and waiting for stimulation

that initiates depolarization. Under the pathological conditions, several changes may occur in the ECG. These include: -

1. Altered paths of excitation in the heart.
2. Changed Origin of waves.
3. Altered relationships of features.
4. Changed magnitudes of one or more features.
5. Differing durations of waves or intervals.

The instrument used to obtain and record the electrocardiogram is called an electrocardiograph.

Chapter 3: ECG Amplifier

For the measurement of the electrocardiogram and the other bioelectric signals, the Differential amplifier is used. A differential amplifier can be considered as two amplifiers with separate inputs but with a common output terminal, which delivers the sum of two amplifier output voltages.

3.1 Electrodes and Leads

To record the ECG, a number of electrodes are affixed to the body of the patient. The electrodes are connected to the ECG machine by the same number of electrical wires. Current flow, in the form of ions, signals contraction of cardiac muscle fibres leading to the heart's pumping action. The ECG is a valuable, non-invasive diagnostic tool which was first put to clinical use in 1913 with Einthoven's invention of the string galvanometer. Einthoven's recording is known as the "three lead" ECG, with measurements taken from three points on the body (defining the "Einthoven triangle" — an equilateral triangle with the heart at the centre.) The difference between potential readings from L1 and L2 is what is used to produce the output ECG trace. The L3 connection establishes a common ground for the body and the recording device (oscilloscope.)

The voltage generated by the pumping action of the heart is actually a vector whose magnitude, as well as spatial orientation, changes with time. The ECG waveform is dependent on the placement of the electrodes. Usually 5 electrodes are affixed to the body of the patient. The placement of electrodes, as well as the color code is used to identify the each electrode. In the normal electrode placement, 4 electrodes are used to record the ECG.

The right leg is used only for the ground reference and the left leg is selected because it terminates vertically below the heart. The three bipolar limb lead selections first introduced by Einthoven are as follows:

- Lead 1 - Left arm (LA) and Right arm (RA).
- Lead 2 - Left leg (LL) and Right arm (RA).

- Lead 3 - Left leg (LL) and Left arm (LA).

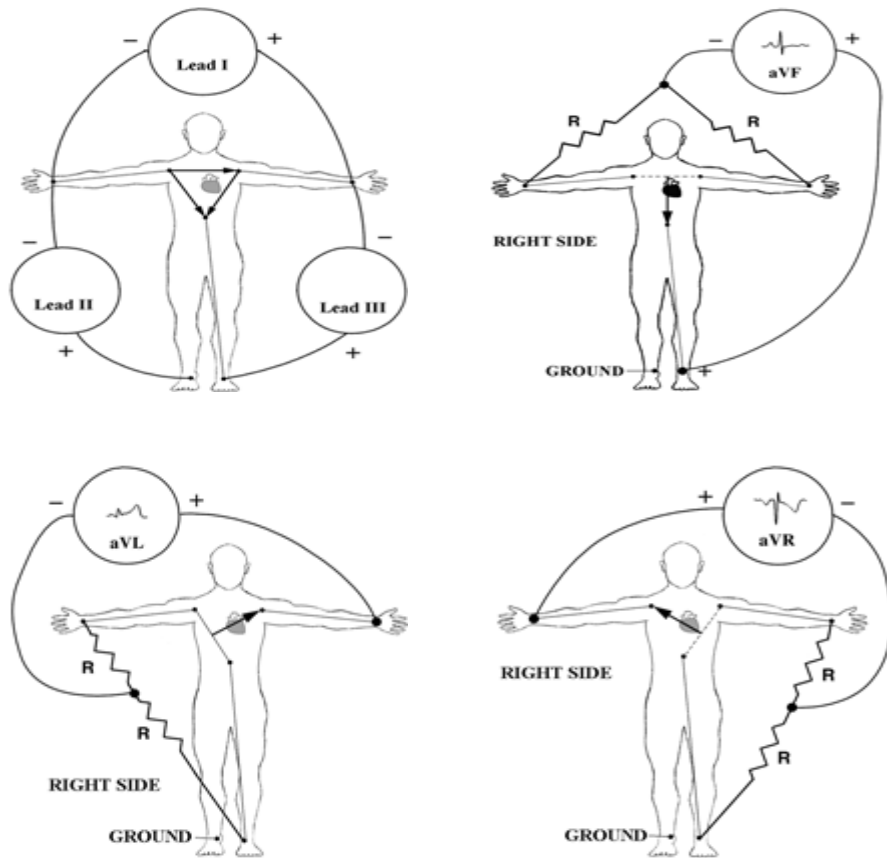


Figure 3.1 Basic Lead Configuration in ECG analysis

These three leads are called bipolar because for each lead the ECG is recorded from two electrodes and the third electrode is not connected. The 12 standard leads used most frequently are displayed in figure 3.1.

The Einthoven postulated that at any given instant of cardiac cycle, the frontal plane representation of electrical axis of heart is two-dimensional vector. And the ECG measured from any one of the three basic limb lead is a time-variant single dimensional component of that vector.

Einthoven also made the assumption that the heart is near to the center of the equilateral triangle, the apexes of which are the right and left shoulder and the crotch. By assuming that the ECG potentials at the shoulders are essentially the same as the wrists

and that the potentials at the crotch differ little from those at either ankle, he let the points of this triangle represent the electrode positions for the three limb leads. This triangle called the Einthoven triangle is shown.

The instantaneous voltage measured from any one of the three limb lead positions is approximately equal to the algebraic sum of the other two, or that the vector sum of the projections on all three lines is equal to zero. In unipolar limb leads, one of the limb electrodes is used as an exploratory electrode as well as contributing to the central terminal.

3.2 ECG Amplifier

An ECG signal is usually in the range of 1mV in magnitude and has frequency components from about 0.05 – 100 Hz. To process this signal, it has to be amplified. The above figure shows the circuit of ECG amplifier. The typical characteristics of an ECG amplifier are: -

1. High Gain (about 1,000)
2. 0.05 -100 Hz Frequency response.
3. High input impedance.
4. Low output impedance.

Monitoring systems typically use the bandwidth of 0.5 – 50 Hz. Various filters like High pass, low pass, band pass , band stop are used to build an ECG amplifier. The inputs RA and LA are given to separate low pass filters. The low pass filters have the low – frequency gain,

$$A_L = -R_2 / R_1$$

The negative sign results because the op amp is in an inverting amplifier configuration. The high corner frequency is given by: -

$$F_h = 1 / 2 * \pi * R_2 * C_1$$

A low pass filter acts as an integrator at high frequencies. The integrator output is given by: -

$$\begin{aligned} V_0 &= - V_i / 1 + j * \omega * R_1 * C_1 \\ &= - \int (V_i) / R_1 * C_1 \end{aligned}$$

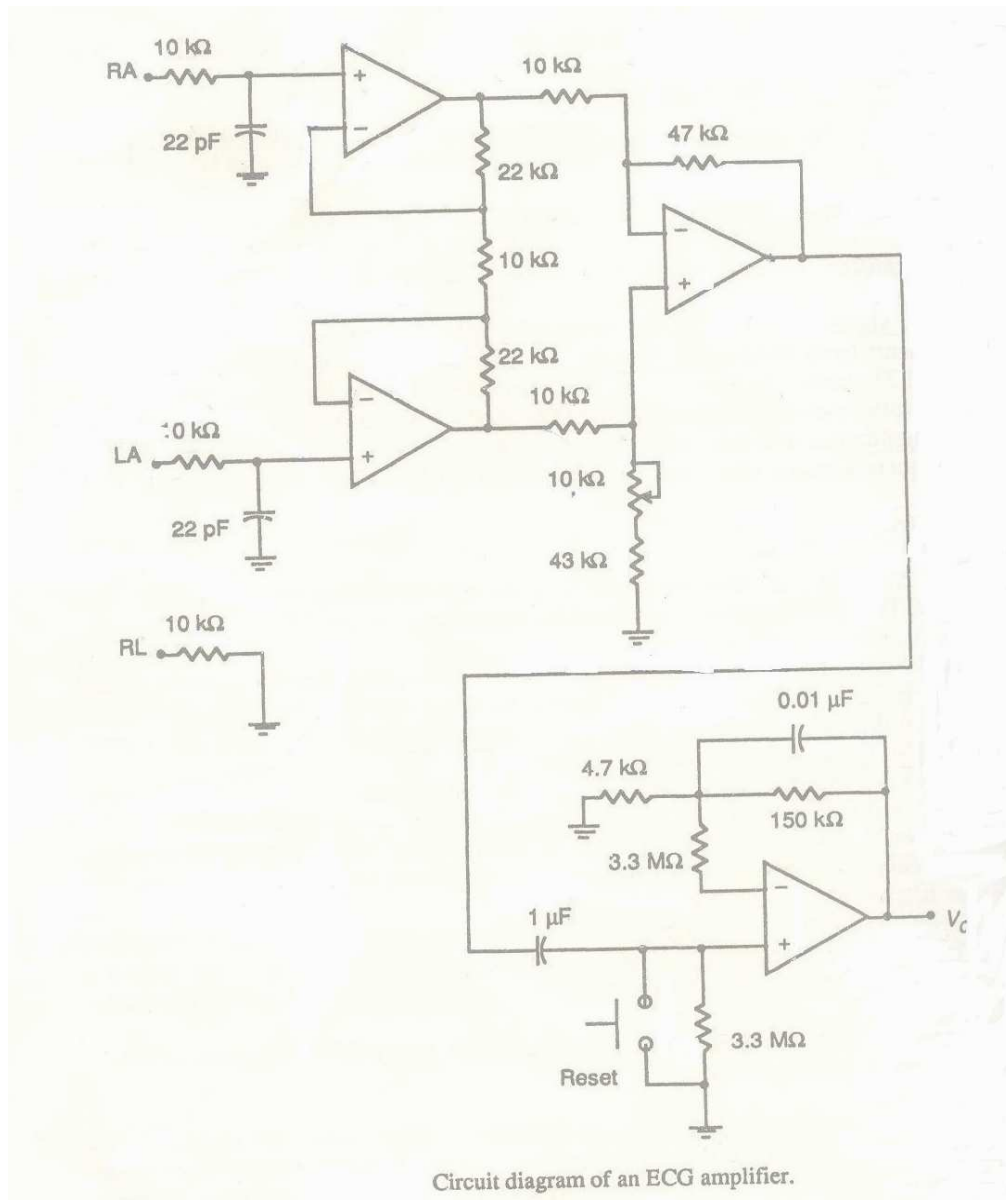


Figure 3.2 Basic circuit diagram of ECG amplifier

The basic diagram of ECG amplifier is shown in figure 3.2. This circuit amplifies the differential ECG signals & introduces a small level shift to bring the negative signals to the positive side and feeds the input of ADC. This circuit has differential Amplifier followed by a High Pass Filter, a non-inverting amplifier with a variable gain and finally a level shifter that adds a 1V offset to the amplified ECG signal.

The high pass filter act like a differentiator at low frequencies. The differentiator gain increases with frequency, up to the low corner frequency. The basic diagram of ECG amplifier is shown

3.3 ORCAD Simulation

Figure 3.3 shows the ECG Amplifier that is simulated using Orcad 9.2 lite edition.

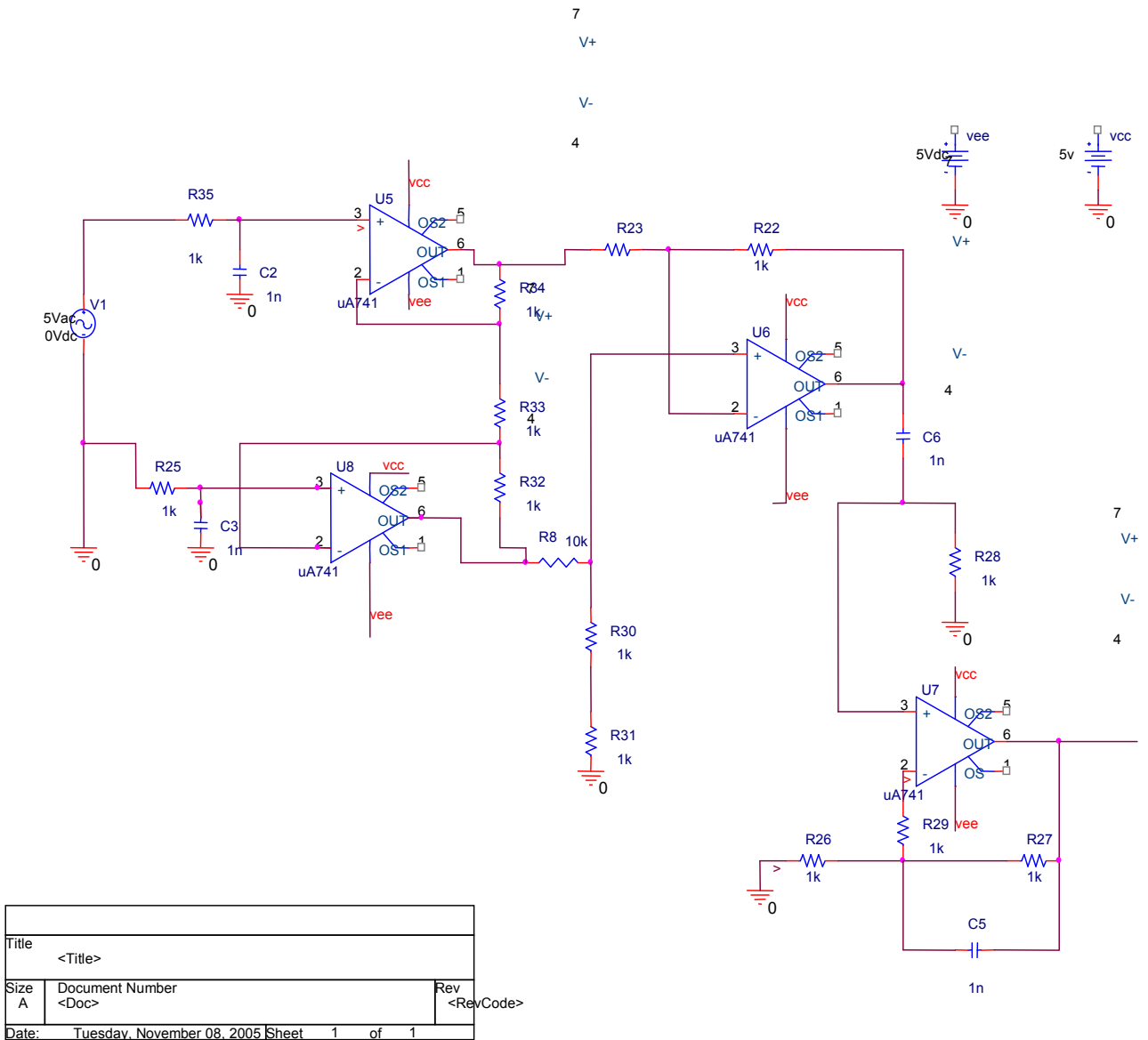


Figure 3.3 ORCAD Simulation of ECG Amplifier

3.4 Digital storage Oscilloscope

To display analog signal onto a digital computer, such as PC, the continuous analog voltage needs to be converted into a discrete digital number that the computer can then take and manipulate.

3.4.1 Analog to Digital Stage

The conversion between analog to digital is done using an A/D converter chip. The continuous signal is changed into discrete signal this implies the faster of an A/D converter we have, the better we will represent the continuous analog signal into discrete digital as well as the fact that we will be able to accurately reproduce higher frequency waves. Today, two methods in A/D technologies seem to give the best speed performance. One is sequential approximation, in which the analog voltage is approximated by sequentially moving from the most significant bit to least significant bit and comparing the digital voltage to the analog voltage. The method works similarly to a binary search in which we do a binary search for the digital number that best represents the analog voltage.

One drawback to this method is the fact that the chip must also contain a digital to analog stage to transform the digital voltage into analog and compare it with the analog input. The second, and by far the most popular method for use in high speed electronics, is a flash A/D converter. Suppose that one uses an 8 bit converter. Then, 256 (2^8) comparators are stacked one on top of each other and the input voltage is passed through a 256 resistor network ladder. The resistor network will distribute the input voltage evenly on each resistor and the comparators compare each node signal against a fixed reference voltage. Based on how many comparators are "on" at one time, a digital number representing the input voltage can be obtained.

In my design, I have used Motorola's triple 8-Bit Video ADC (MC44250). This flash A/D converter has the following feature which made it extremely well suited for my project:-

- 15MHz Sampling Rate.

- ✚ Single 5Volt Power Supply.
- ✚ Flash A/D converters on one chip. (Very well suited for future upgrades where we would like our digital scope to have two or three input channels).

Depending on the environment in which the circuit is being built, large coupling capacitors might be necessary in order to remove any excessive noise around the components (one environment in which this applies is when the circuit is built using a breadboard).

3.4.2 Clock Circuit

The A/D converter requires a clock running at speeds up to 15MHz. Again, caution should be taken on where and how the clock is mounted in the circuit. On a breadboard, the high clock frequencies will cause excessive noise causing certain components to malfunction.

3.4.3 Digital to Analog Scalar Stage

However the D/A converter is rated for only 25V. By using the 3K and 1K resistors it can be made sure that we have a 25V input to the DAC when the original wave is 100V. The rest of the circuit acts just like an inverting amplifier where we are using the DAC as the feedback voltage. Using this setup we are able to divide the input signal by a factor ranging from 4 to 1024.

3.4.4 Analog to Digital Conditioning Stage

The A/D converter requires the input voltage for V_{in} to range from around 1.7 volts to about 4.9 volts, with an average range of about 3 volts. Moreover, since the A/D data specs did not contain any information on the input impedance it would be nice to have something that would provide high impedance to the analog input as well as shift the voltage in the +2V to +5V range.

3.4.5 Aliasing Detection Circuit

When sampling continuous signals caution should be taken to prevent aliasing. By definition alias is a false signal caused from beats between signal frequency and sampling frequency. In 1928 Nyquist discovered that in order to prevent aliasing the

signal must be sampled at a frequency twice its own. That's why it is appropriate to incorporate an alias detection circuit in PC Oscilloscope.

Chapter 4: Hardware for Dual Channel ECG Simulator

4.1 Introduction

Electrocardiogram is record of electrical activity of human heart and is of vital utility to know the status of heart. Each heartbeat is caused by a section of the heart generating an electrical signal that then conducts through specialized pathways to all parts of the heart. These electrical signals also get transmitted through the chest to the skin where they can be recorded.

For clinical training of doctors to interpret the ECG of a Subject with proved diagnosis (i.e. the exact status of subject's heart is known through the clinical truths) we require the Subject, ECG amplifier and Monitor. The availability of such subject may not be practically feasible in all situations. The Doctors therefore have to mainly rely on recorded signals that do not give the real time experience to the Doctors.

The trend these days is to build intelligent ECG machines which automatically detect and classify any abnormality in the ECG signal. For design, development of testing of these automatic machines, again the presence of the subject with the proved diagnosis is required.

The figure 4.1 shows the various segments of the ECG simulator. The text file of ECG signal with proper annotation (Markings) is downloaded from Physionet.org and stored in the folder. By using 'C' program, this file is compiled and its executable file i.e. ECG.EXE is stored in the same folder. Upon running this executable file, the signal from the parallel port of PC is transferred to DAC0808. The ECG text file has two different columns for two leads. A program written in C/C++ segregates these two

signals and using the most significant bit as channel identifier, two separate channels of analog output are obtained.

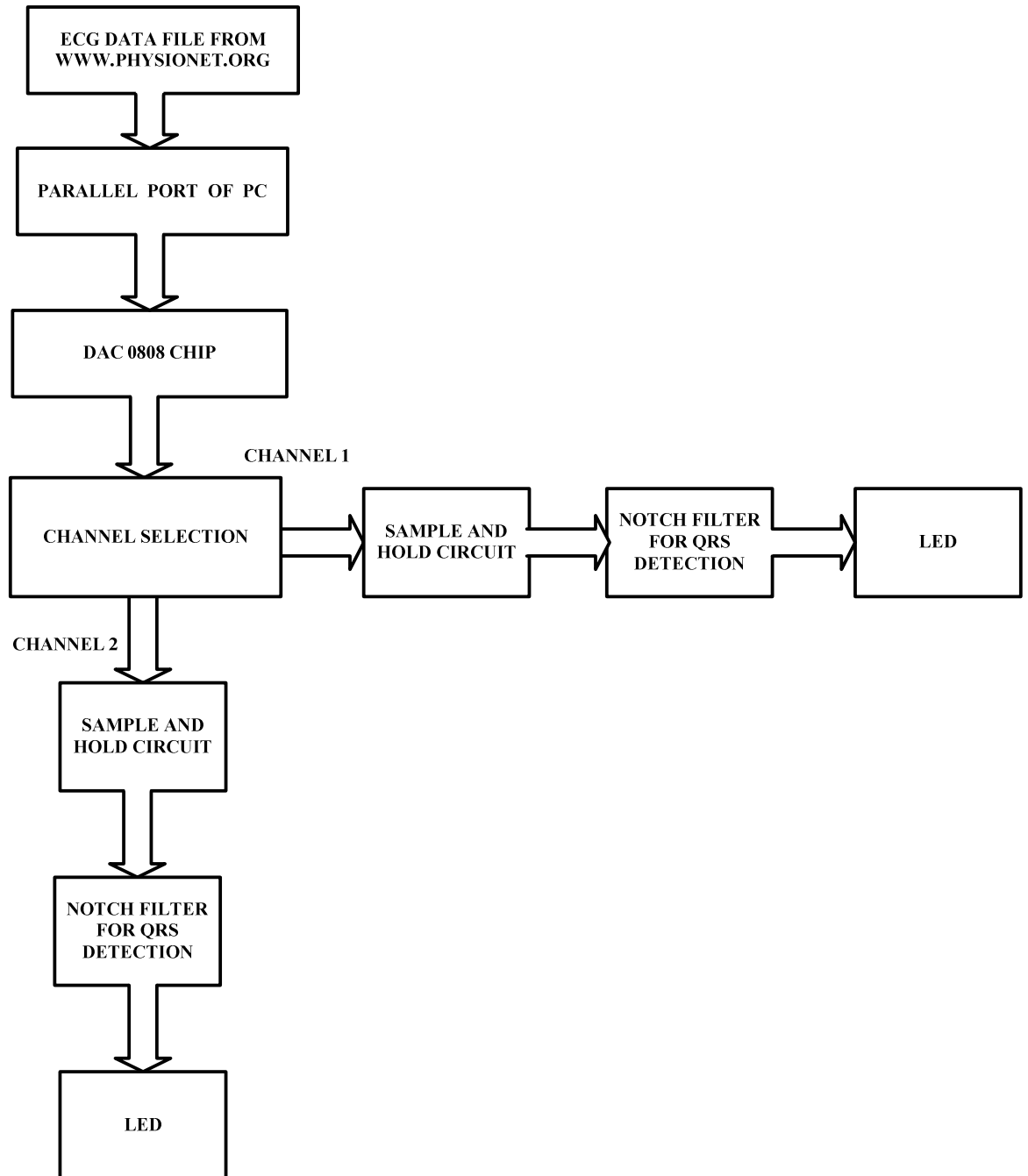


Figure 4.1 Basic Elements of ECG Simulator

The channel is selected by feeding the MSBs of the signal to the selection logic input of the sample and hold ICs. The narrow band pass filter is designed by using 741 operational amplifier, to detect the QRS complex from the ECG signal. The red colored LEDs at the output of filters remains off under normal operating conditions and flashes a specific number of times indicating which particular channel is selected and every time the occurrence of QRS complex (highest peak of the ECG signal).

An ECG simulator is device that can simulate all types of signals recorded previously in the real time mode. This simulator can be used both for clinical training of doctors as well as for design, development and testing of automatic ECG machine without having real subject for this purpose. Such ECG simulator has been designed for this project.

4.2 System Requirements and Installation

For the proper working of ECG Simulator, system must meet the following minimum requirements

- Personal computer using a 233 MHz Pentium-class processor. Using a Pentium III or Celeron 600 MHz or equivalent is recommended.
- Compiler installed on PC for execution of the application program.
- Microsoft Windows 2000/NT/XP.
- Direct I/O device driver for accessing the parallel port of Windows XP (whichever is used).
- Source code written in any language like C / C++, visual basics etc
- ECG Data file of patient loaded from site www.physionet.org
- Complete hardware for displaying ECG wave, Channel selection, QRS detection circuitry.

4.3 Connections

- A Program is written in C language, which reads the data of ECG file and sends it to the port of the PC.

- Direct I/O device driver is installed, which allows us to access parallel port
- Parallel port of the PC is used to send data to the DAC chip. 8 pins of the parallel port are used for transferring the data (2 to 9) and rests are grounded.
- DAC is provided with power supply and other reference voltages.
- A 741 operational amplifier is connected to the output of the DAC for converting the output current into output voltage.
- The main circuit for Channel Selection comprising of LF398 ICs and QRS Detection by using notch filters are connected to DAC.
- We can have monitor or DSO for taking display of real time ECG Signal and it is directly connected to power supply.
- LEDs connected glow according to ECG signal which represents the selection of channel and detection of QRS complex.

4.4 ECG Data file

The ECG data file is taken from the ECG Databases available at site www.physionet.org. Several databases of ECG and other physiological recordings are available for various purposes including the evaluation of ECG analyzers. Of particular relevance is PhysioNet, apparently the largest and best-organized network at present. The project offers free access via the web to large collections of recorded physiologic signals and related open-source software. There are many databases available in the PhysioBank archives, organized according to the types of signals and annotations contained in each database. For e.g. –

- Multi-Parameter Databases. Available signals vary, but may include ECG, continuous invasive blood pressure, respiration, oxygen saturation, and EEG, among others.
- ECG Databases
- MIT-BIH ECG Compression Test Database
- Interbeat (RR) Interval Databases. These contain beat annotations obtained from ECG recordings, but the ECG signals are not available.
- Neurological Databases

- Synthetic databases
- Gait Dynamics in Neuro-Degenerative Disease Database

The data file is the record (of a heart patient) obtained from mit.bh database (Massachusetts Institute of Technology. Beth Israel Hospital.). This is a rich database containing hundreds of recordings extending over 200 hours. The recordings were digitized at 360 samples per second per channel with 11-bit resolution over a 10 mV range. Approximately all of the signals have been annotated on beat-by-beat basis. During 1989 CD ROM was produced containing the original MIT-Arrhythmia along with many assembled recordings for various research projects between 1981 and 1989. There are approximately 600 M bytes of digitized ECG recordings, mostly with beat-by-beat annotations [Moody and Mark, 1990]. This data was made available on Internet during September 1991, on physionet (<http://www.physionet.org>). It is a web-based resource that supplies physiologic signals and the related open source software to bio-medical field. The MIT-BIH Arrhythmia Database contains 48 half-hour excerpts of two-channel ambulatory ECG recordings, obtained from 47 subjects studied by the BIH Arrhythmia Laboratory between 1975 and 1979. The recordings were digitized at 360 samples per second per channel with 11-bit resolution over a 10 mV range. Two or more cardiologists independently annotated each record; disagreements were resolved to obtain the computer-readable reference annotations for each beat (approximately 110,000 annotations in all) included with the database. This directory have the complete MIT-BIT Arrhythmia-database. Almost half i.e. 25 out of 48 complete records, and reference annotation files for all 48 records has been freely available here since physionet's inception in September 1999[Goldberger et al.2000].

Table 4.1 ECG Data file

TIME In seconds	CHANNEL 1 In volts	CHANNEL 2 In volts
0.361	-0.335	-0.205
0.364	-0.335	-0.190

0.367	-0.340	-0.180
0.369	-0.330	-0.185
0.372	-0.340	-0.200
0.375	-0.350	-0.215
0.378	-0.355	-0.205
0.381	-0.350	-0.210
0.383	-0.345	-0.200
0.386	-0.330	-0.185
0.389	-0.320	-0.205
0.392	-0.335	-0.200
0.394	-0.330	-0.210
0.397	-0.345	-0.205
0.400	-0.330	-0.185
0.403	-0.335	-0.185
0.406	-0.335	-0.200
0.408	-0.345	-0.215
0.411	-0.345	-0.225
0.414	-0.355	-0.220
0.417	-0.340	-0.200
0.419	-0.340	-0.200
0.422	-0.335	-0.215
0.425	-0.330	-0.225

4.5 Simulator Hardware Overview

The below figure shows basic structure of the ECG simulator. By using ‘C’ program, this file is compiled and its executable file i.e. ECG.EXE was stored in the same folder. Upon running this executable file, the signal from the parallel port of PC is transferred to DAC0808. The significance of the ECG simulator is that the subject has been replaced by text file

The ECG text file has two different columns for two leads. A program written in C/C++ segregates these two signals and using the most significant bit as channel identifier, two separate channels of analog output were obtained.

The two separate channels are designed by using two LF398 sample and hold ICs connected at the output of the DAC0808. The ECG wave can be displayed on the PC monitor as well as at the Digital storage oscilloscope connected at the output of DAC.

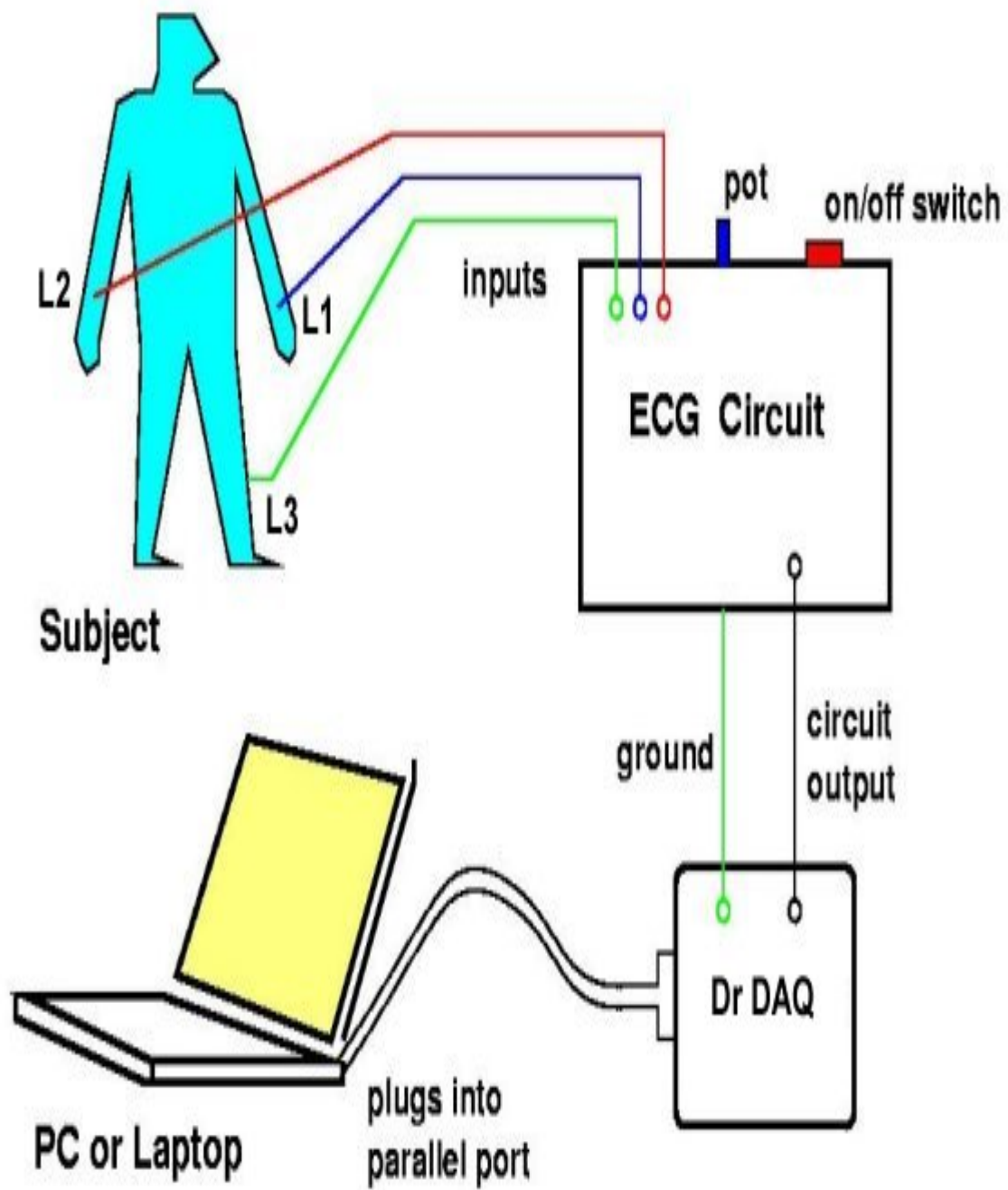


Figure 4.2 Structure of ECG Simulator

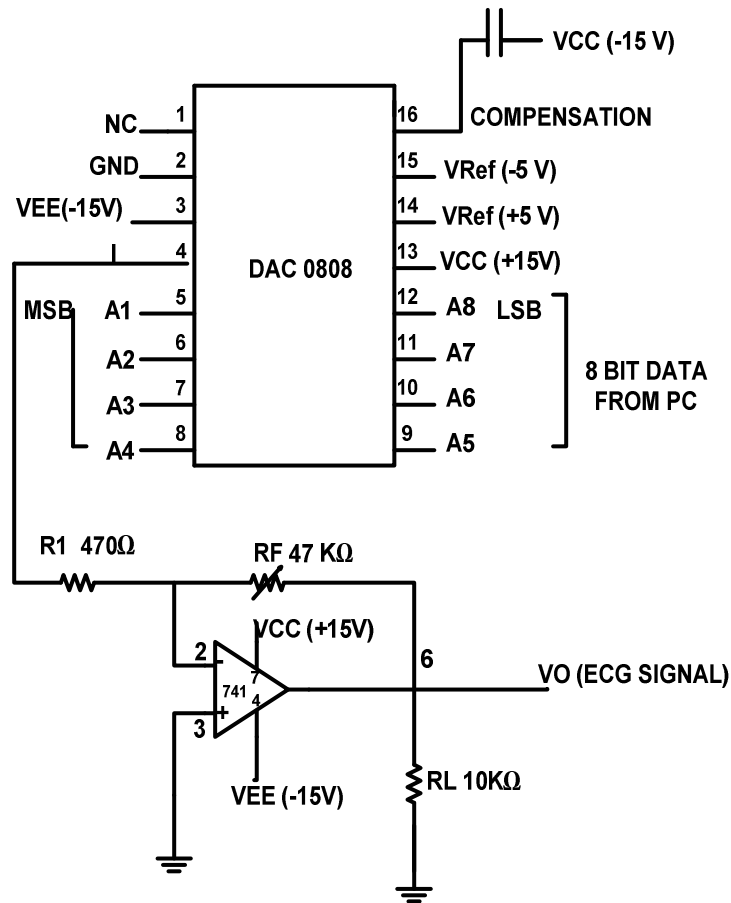


Figure 4.3 Circuit connections of ECG Simulator

The digital output of the parallel port is connected to DAC 0808(Digital-to-Analog Converter). DAC 0808 is an 8 bit digital to analog converter. The digital output signal is converted to analog signal by the DAC. The reference voltage given to pin 14 decides the output range. The DAC output is current in the milli amperes range. This current is converted into voltage by 741 opamp as shown in figure 4.3. The feedback resistance R_F connected between the pins 2 and 6 decides the conversion ratio. The output of the opamp is in the range of few volts.

4.5.1 DIGITAL TO ANALOG CONVERTER (DAC 0808)

4.5.1.1 General Description: - The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. Relative accuracies of better than $\pm 0.19\%$

assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero ac-curacy

The power supply current of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range. The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, DAC0800 data sheet can be viewed.

4.5.1.2 Features:-

- Relative accuracy: $\pm 0.19\%$ error maximum.
- Full scale current match: ± 1 LSB typ.
- Fast settling time: 150 ns type.
- Non inverting digital inputs are TTL and CMOS compatible.
- High speed multiplying input slew rate: 8 mA/ μs .
- Power supply voltage range: $\pm 4.5\text{V}$ to $\pm 18\text{V}$.
- Low power consumption: 33 mW @ $\pm 5\text{V}$.

4.5.1.3 Specifications

Power Supply Voltage

- | | |
|----------------------------------|----------------------|
| • VCC | +18 VDC |
| • VEE | - 18 VDC |
| • Digital input voltage, v5-v12 | - 10 VDC to + 18 VDC |
| • Applied Output Voltage, V0 | -11 VDC to + 18 VDC |
| • Reference Current, I14 | 5mA |
| • Reference Amplifier Inputs, | VCC,VEE ,V14, V15 |
| • Power Dissipation | 1000 m W |
| • ESD Susceptibility | TBD |
| • Dual-In-Line Package (Plastic) | 260°C |
| • Dual-In-Line Package (Ceramic) | 300°C |

4.5.1.4 Operating Ratings

Temperature Range	$T_{MIN} < T_A < T_{MAX}$
DAC0808	$0 < T_A < +75^{\circ}\text{C}$

4.5.1.5 Accuracy

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder. The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536 or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.019\%$ specification provided by the DAC0808.

4.5.1.6 Operational amplifier

The mA741 is a high performance operational amplifier with high open-loop gain, internal compensation, high common mode range and exceptional temperature stability. The mA741 is short-circuit-protected and allows for nulling of offset voltage.

The DAC output is current in the milli amperes range. This current is converted into voltage by 741 opamp. The feedback resistance R_F connected between the pins 2 and 6 decides the conversion ratio. The output of the opamp is in the range of few volts.

PIN CONFIGURATION

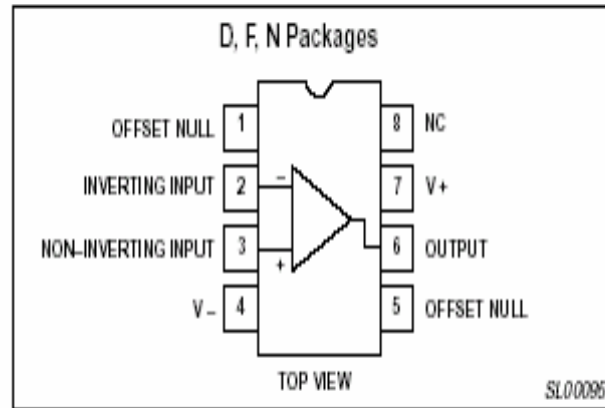


Figure 1. Pin Configuration

4.5.1.7 Features

- Internal frequency compensation.
- Short circuit protection.
- Excellent temperature stability.
- High input voltage range.

4.5.2 DIGITAL STORAGE OSCILLOSCOPE

The output of the simulator can be connected to a digital storage oscilloscope to get a clear picture of the waveform. For further analysis, the output can also be fed to a computer through the soundcard.

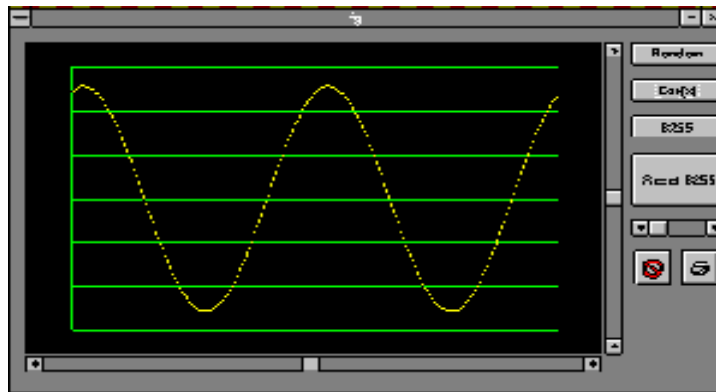


Figure 4.4 Digital storage oscilloscope

The conversion between analog to digital is done using an A/D converter chip. The continuous signal is changed into discrete signal this implies the faster of an A/D converter we have, the better we will represent the continuous analog signal into discrete digital as well as the fact that we will be able to accurately reproduce higher frequency waves. Today, two methods in A/D technologies seem to give the best speed performance.

One is sequential approximation, in which the analog voltage is approximated by sequentially moving from the most significant bit to least significant bit and comparing the digital voltage to the analog voltage. The method works similarly to a binary search in which we do a binary search for the digital number that best represents the analog voltage. One drawback to this method is the fact that the chip must also contain a digital to analog stage to transform the digital voltage into analog and compare it with the analog input.

The second, and by far the most popular method for use in high speed electronics, is a flash A/D converter. Suppose that one uses an 8 bit converter. Then, 256 (2^8) comparators are stacked one on top of each other and the input voltage is passed through a 256-resistor network ladder. The resistor network will distribute the input voltage evenly on each resistor and the comparators compare each node signal against a fixed reference voltage. Based on how many comparators are "on" at one time, a digital number representing the input voltage can be obtained. In my design; I have used Motorola's triple 8-Bit Video ADC (MC44250).

Depending on the environment in which the circuit is being built, large coupling capacitors might be necessary in order to remove any excessive noise around the components (one environment in which this applies is when the circuit is built using a breadboard). The A/D converter requires a clock running at speeds up to 15MHz. Again, caution should be taken on where and how the clock is mounted in the circuit. On a breadboard, the high clock frequencies will cause excessive noise causing certain components to malfunction.

However the D/A converter is rated for only 25V. By using the 3K and 1K resistors it can be made sure that we have a 25V input to the DAC when the original

wave is 100V. The rest of the circuit acts just like an inverting amplifier where we are using the DAC as the feedback voltage. Using this setup we are able to divide the input signal by a factor ranging from 4 to 1024.

The A/D converter requires the input voltage for V_{in} to range from around 1.7 volts to about 4.9 volts, with an average range of about 3 volts. Moreover, since the A/D data specs did not contain any information on the input impedance it would be nice to have something that would provide high impedance to the analog input as well as shift the voltage in the +2V to +5V range.

When sampling continuous signals caution should be taken to prevent aliasing. By definition alias is a false signal caused from beats between signal frequency and sampling frequency. In 1928 Nyquist discovered that in order to prevent aliasing the signal must be sampled at a frequency twice its own. That's why it is appropriate to incorporate an alias detection circuit in PC Oscilloscope

4.5.3 CHANNEL SELECTION: -

The ECG text file has two different columns for two leads. A program written in C/C++ segregates these two signals and using the most significant bit as channel identifier, two separate channels of analog output were obtained. The two separate channels are designed by using two LF398 sample and hold ICs connected at the output of the DAC0808. The most significant bit of the signal decides which channel is being selected is fed at the eighth pin of the sample and hold IC. The notch filter is designed at the output of the channel selector which passes signal of specific band i.e. 14-20 Hz.

General description of sample and hold circuit

Figure 4.5 shows the basic connection diagram of sample and hold circuit. It is a monolithic sample-and-hold circuit, which utilizes BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low drop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 μ s to 0.01%.

A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

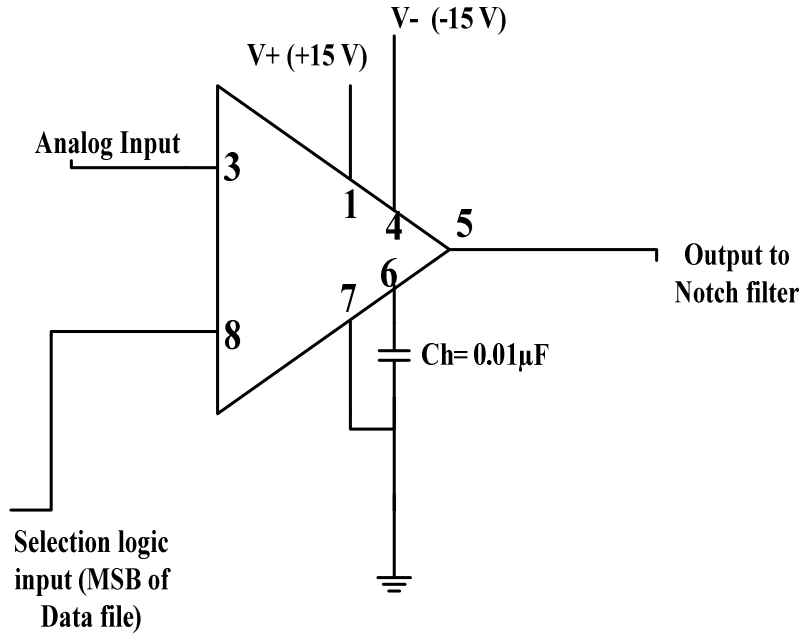


Figure 4.5 basic circuit connections of sample and hold circuit

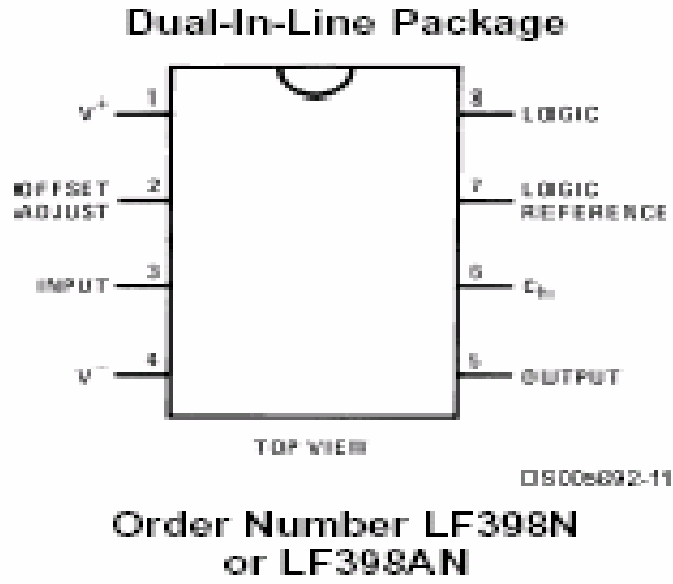


Figure 4.6 Pin diagram of Sample and Hold IC

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 μ F hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities.

The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

Features

- Less than 10 μ s acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at $C_h = 0.01$ F
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth

- Space qualified, JM38510

4.5.4 QRS DETECTION

The QRS complex is the most striking waveform within the electrocardiogram (ECG). Since it reflects the electrical activity within the heart during the ventricular contraction, the time of its occurrence as well as its shape provide much information about the current state of the heart.

For QRS Detection, a narrow band pass filter has been designed for each channel by using 741 operational amplifier in inverting mode. The filter is designed to have the centre frequency 17 Hz and Quality factor of 2.83. It removes all signal frequencies except for a particular band (i.e. to record 14-20 Hz activity in ECG recordings).

The frequencies occurring on either side of this band are not passed. The red colored LEDs at the output of filters remains off under normal operating conditions and flashes a specific number of times indicating which particular channel is selected and every time the occurrence of QRS complex (highest peak of the ECG signal).

Due to its characteristic shape it serves as the basis for the automated determination of the heart rate, as an entry point for classification schemes of the cardiac cycle, and often it is also used in ECG data compression algorithms.

In that sense, QRS detection provides the fundamentals for almost all automated ECG analysis algorithms. Software QRS detection has been a research topic for more than 30 years. The evolution of these algorithms clearly reflects the great advances in computer technology.

Within the last decade many new approaches to QRS detection have been proposed; for example, algorithms from the field of artificial neural networks, genetic algorithms, wavelet transforms, filter banks as well as heuristic methods mostly based on nonlinear transforms.

The QRS complex is a waveform that correlates to the electrical flow through the bundle branches, from which heart-rate and many other parameters can be measured. The accurate detection of the R-peak of the QRS complex is the prerequisite for the reliable function of EKG analyzers. The recognition of almost all EKG parameters is based on a fixed point identifiable at each cycle. R-peak is suitable for use as the datum point, because it has the largest amplitude and sharpest waveform that can be extracted from EKG. The time and amplitude measurements can be performed when the apex of the R-peak is detected at each cycle.

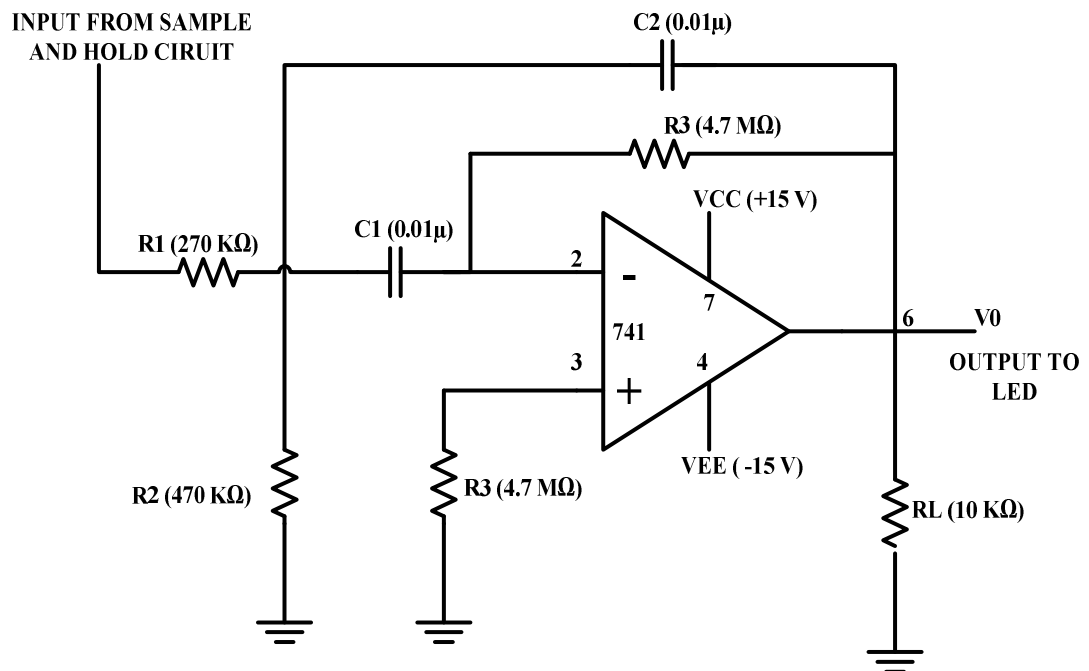


Figure 4.7 Circuit connection of QRS Detection stage.

One can implement the filtering at the software level using digital filters as well to remove the noise present in the captured digital EKG. Digital filters are required to be designed to reduce noise interferences and thereby improve the signal-to-noise ratio. Filtering EKG signal is not an easy task.

The important EKG signals are found at very low frequencies and are relatively distributed in the mid frequencies. Typically the important EKG signals are in the range of 0.5–150Hz.

Chapter 5: ECG Simulator Software

5.1 Introduction

The text file of ECG signal with proper annotation (Markings) was downloaded from Physionet.org and stored in the folder. The 'C' program file named ECG.C was compiled and its executable file i.e. ECG.EXE was stored in the same folder.

Upon running this executable file, the signal from DAC connected to the parallel port was displayed on DSO. The flowchart in figure 5.1 shows the step-by-step procedure of basic program involved in ECG Simulation. A problem that plagues Windows NT/2000 and Windows XP is its strict control over I/O ports. Unlike Windows 95 & 98, Windows NT/2000/XP will cause an exception (Privileged Instruction) if an attempt is made to access a port that we are not privileged to talk too. Actually it is not Windows NT that does this, but any 386 or higher processor running in protected mode.

Direct I/O is the world's first device driver for Microsoft Windows NT, Windows 2000, Windows XP and Windows Server2003 which enables the direct hardware access

for your existing software without any programming efforts on your side. We have downloaded Direct I/O device driver from site www.direct-io.com.

However for accessing the parallel port correctly, the Direct I/O driver must be in the same directory than the user mode executable ran and the user must have administrator privileges. Once the driver has been installed for the first time, any user with normal user privileges can access the device driver normally. This is ideal in classroom/corporate environments where security is paramount.

The basic flowchart in figure 5.1 shows the software procedure involved in ECG simulator. The downloaded ECG data file is opened along with the Direct I/O for accessing the parallel port of PC. By using the C/C++ programming, the analog variables of the data file are read and converted into 7- bit digital values. The most significant bit (MSB) is used for the selection of the dual channel of ECG Simulator. With the proper time delay calculated by formula $T_n - T_{n-1}$, these values are sent to parallel port of PC until the end of file is reached.

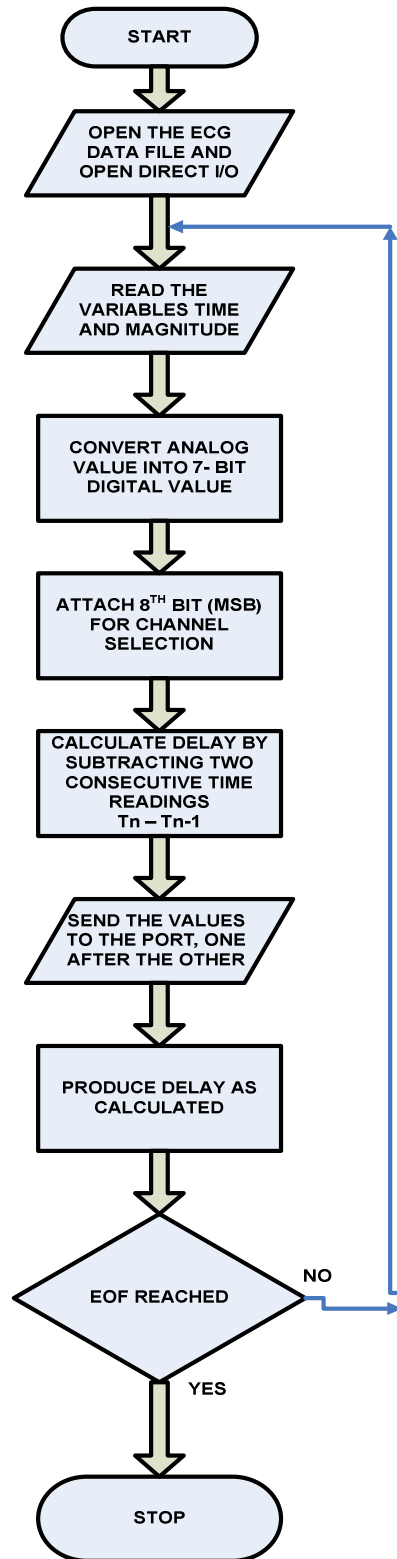


Figure5.1 Flowchart of simulator software

5.2 Parallel Port

PC parallel port can be very useful I/O channel for connecting circuits to PC. PC parallel port is 25 pin D-shaped female connector in the back of the computer. It is normally used for connecting computer to printer, but many other types of hardware for that port is available today.

Not all 25 are needed always. We can easily do with only 8 output pins (data lines) and signal ground. I have presented those pins in the table below. Those output pins are adequate for many purposes.

5.2.1 Pin function

2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7

Pins 18,19,20,21,22,23,24 and 25 are all ground pins. Those data pins are TTL level output pins. This means that they put out ideally 0V when they are in low logic level (0) and +5V when they are in high logic level (1). In real world the voltages can be something different from ideal when the circuit is loaded. The output current capacity of the parallel port is limited to only few mill amperes.

5.2.2 Parallel port programming in DOS

The following examples are short code examples how to write to I/O ports using different languages. I have used I/O address 378h which is one of the addresses where parallel port can be. The typical parallel port I/O addresses configurations seen on PCs with ISA bus:

- LPT1: 3BCh, LPT2: 378h, LPT3: 278h.
- LPT1: 378h, LPT2: 278h.
- LPT1: 378h.

Those are the typical I/O addresses used in ISA bus based systems. In PCI bus based systems the LPT1 port on motherboard is typically at I/O-address 378h or 3BCh the following examples are for DOS system (they might or might not work on other systems). The code examples are designed to be used with LPT1 port that resides in I/O address 378h.

Assembler

```
MOV DX, 0378H
```

```
MOV AL, n
```

```
OUT DX,AL
```

Where n is the data you want to output.

Basic

```
OUT &H378, N
```

Where N is the number you want to output.

C

```
Outp (0x378, n);
```

or

```
Outportb (0x378, n);
```

Where N is the data that we want to output. The actual I/O port controlling command varies from compiler to compiler because it is not part of standardized C libraries. The following port description applies to Standard Parallel Port (SPP).

Offset	Name	Read/Write	Bit No.	Properties
Base + 0	Data Port	Write	Bit 7	Data 7
			Bit 6	Data 6

			Bit 5	Data 5
			Bit 4	Data 4
			Bit 3	Data 3
			Bit 2	Data 2
			Bit 1	Data 1
			Bit 0	Data 0

This Data Register is simply used for outputting data on the Parallel Port's data lines (Pins 2-9). If the port is bi-directional, we can receive data on this address.

Offset	Name	Read/Write	Bit No.	Properties
Base + 1	Status Port	Read Only	Bit 7	Busy
			Bit 6	Ack
			Bit 5	Paper Out
			Bit 4	Select In
			Bit 3	Error
			Bit 2	IRQ (Not)
			Bit 1	Reserved
			Bit 0	Reserved

The Status Port (base address + 1) is a read only port. Any data written to this port will be ignored.

Offset	Name	Read/Write	Bit No.	Properties
Base + 2	Control Port	Read/Write	Bit 7	Unused
			Bit 6	Unused

			Bit 5	Enable Bi-Directional Port
			Bit 4	Enable IRQ Via Ack Line
			Bit 3	Select Printer
			Bit 2	Initialize Printer (Reset)
			Bit 1	Auto Linefeed
			Bit 0	Strobe

The Control Port (base address + 2) is intended as a write only port. When a printer is attached to the Parallel Port, four "controls" are used. These are Strobe, Auto Linefeed, Initialize and Select Printer, all of which are inverted except Initialize. The first PC-compatible parallel printer ports were unidirectional, allowing 8-bit data transfer only from the host to the peripheral. These early Standard Printer Ports (SPP) implemented eight data lines and used nine handshaking lines, four output from the host and five input to the host.

The SPP type implemented three registers for the control and monitoring of the data and handshaking lines; these are the data port, status port, and control port. The SPP type parallel ports are most commonly used for printers, plotters, keys, etc. Generally all modern parallel ports can operate in SPP mode. The maximum cable distance between computer and peripheral could only extend 6 feet.

Later came the PS/2 type bi-directional parallel port (BPP); this bi-directional port simply added the capability to read 8-bit data from the peripheral to the host. This parallel port type also implemented the same three registers as used by SPP for the control and monitoring of the data and handshaking lines; these are the data port, status

port, and control port. In addition to normal operations there is one extra bit on control port that can set the data pins to output or input mode.

The IEEE 1284 standard, "Standard Signaling Method for a Bi-directional Parallel Peripheral Interface for Personal Computers", sought to correct the major drawbacks to the original parallel port structure. IEEE 1284 sets standards for the cable, connector, and electrical interface, which guarantee interoperability between all parallel peripherals.

The specified configuration ensures that data integrity is maintained, even at the highest data rates, and at a distance of up to 30 feet. Two new types of parallel ports with extended features are now available: the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). EPP and ECP are standards defined by IEEE 1284 and Microsoft ECP Specifications.

Both EPP and ECP ports may be operated in the SPP and bi-directional modes; however, operation in their feature modes requires both compatible peripherals and appropriate software drivers. Generally, EPP is used primarily by non-printer peripherals, CD ROM, tape drive, hard drive, network adapters, etc., while ECP is aimed at newer generation of printers and scanners. Currently, new products have been released having support for a mixture of these protocols. With EPP, the software driver may intermix read and write operations without any overhead or protocol handshaking. With the ECP protocol, changes in the data direction must be negotiated.

The I/O interface on EPP and ECP ports is somewhat different from normal I/O port controls. They can be viewed as supersets of SPP. An EPP parallel port implements two registers in addition to the standard data, status, and control ports. The outputs are tri-state able outputs allow the EPP port to be used as a data bus for multiple EPP compatible devices. The entire data transfer occurs within one ISA I/O cycle. An ECP parallel port features two special modes, namely data and command cycles. The ECP Parallel Port Mode allows bi-directional data transfer using automatic interlocked handshaking via the ECP protocol. When the ECP protocol was proposed, a standard register implementation was also proposed through Microsoft ECP Specification. ECP

protocol is meant to be driven by DMA rather than explicit I/O operations. ECP protocol is commonly seen on parallel port on motherboards and on high-end parallel port cards that plug to ISA bus, but often not on PCI bus parallel port cards (because PCI bus does not support ISA bus type DMA transfers).

Many modern parallel ports support SPPI, BPP, ECP and EPP modes, or at least most of them. On some systems and interface cards there has been even options to see USB parallel port adapters

The USB-Parallel Port Adapter enables users to connect parallel port interfaced devices like printers to a desktop or laptop PC via the PC's USB port. As USB becomes increasingly popular and newer laptop PCs are without parallel and/or serial ports. Older PCs tend to have a parallel port but no USB, newer PCs have both, and tomorrow's PCs will typically have USB but no parallel port.

The parallel port through this kind of adapter looks pretty same as normal parallel port for high level programs on Windows system. The low level implementation of them is completely different, and the low level I/O control operations described in this document do not work with USB parallel port adapters.

At this port we can forget using the USB parallel ports for your own hardware controlling. In some cases USB Parallel Printer Adapter can be useful. With USB Parallel Printer Adapter we can attach the printer to our USB port and make room for your own circuits on the existing legacy parallel ports on our system.

5.3 DIRECT I/O - A Windows NT I/O Port Device Driver

Accessing I/O Ports in protected mode is governed by two events, The I/O privilege level (IOPL) in the EFLAGS register and the I/O permission bit map of a Task State Segment (TSS). Under Windows NT, there are only two I/O privilege levels used, level 0 & level 3. User mode programs will run in privilege level 3, while device drivers

and the kernel will run in privilege level 0, commonly referred to as ring 0. This allows the trusted operating system and drivers running in kernel mode to access the ports, while preventing less trusted user mode processes from touching the I/O ports and causing conflicts. All usermode programs should talk to a device driver which arbitrates access. The I/O permission bitmap can be used to allow programs not privileged enough (I.e. usermode programs) the ability to access the I/O ports. When an I/O instruction is executed, the processors will first check if the task is privileged enough to access the ports. Should this be the case, the I/O instruction will be executed. However if the task is not allowed to do I/O, the processor will then check the I/O permission bitmap.

The I/O permission bitmap, as the name suggests uses a single bit to represent each I/O address. If the bit corresponding to a port is set, then the instruction will generate an exception however if the bit is clear then the I/O operation will proceed. This gives a means to allow certain processes to access certain ports. There is one I/O permission bitmap per task.

5.3.1 Accessing I/O Ports under NT/2000/XP

There are two solutions to solving the problem of I/O access under Windows NT. The first solution is to write a device driver which runs in ring 0 (I/O privilege level 0) to access your I/O ports on your behalf. Data can be passed to and from your usermode program to the device driver via IOCTL calls. The driver can then execute your I/O instructions. The problem with this is that it assumes we have the source code to make such a change.

Another possible alternative is to modify the I/O permission bitmap to allow a particular task, access to certain I/O ports. This grants your usermode program running in ring 3 to do unrestricted I/O operations on selected ports, per the I/O permission bitmap. This method is not really recommended, but provides a means of allowing existing applications to run under windows NT/2000. Writing a device driver to support your hardware is the preferred method. The device driver should check for any contentions before accessing the port.

However, using a driver such as Port Talk can become quite inefficient. Each time an IOCTL call is made to read or writes a byte or word to a port, the processor must switch from ring 3 to ring 0 perform the operation, then switch back.

5.3.2 Starting and Installing the Direct I/O driver

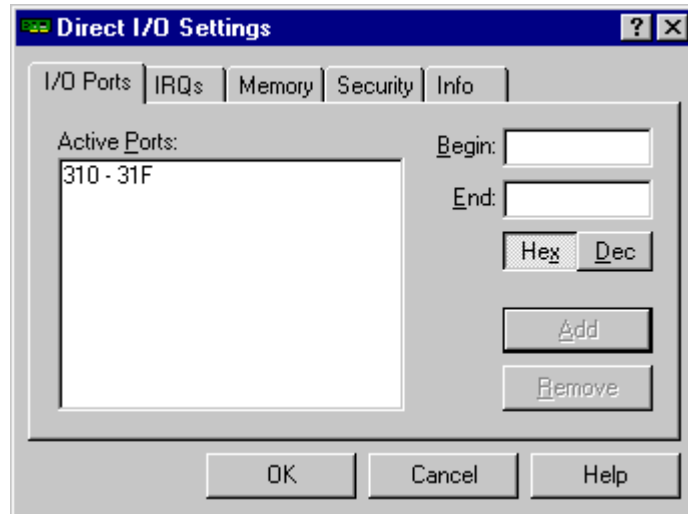
However for accessing the parallel port correctly, the Direct I/O driver must be in the same directory than the user mode executable ran and the user must have administrator privileges. Once the driver has been installed for the first time, any user with normal user privileges can access the device driver normally. This is ideal in classroom/corporate environments where security is paramount.

Direct I/O is the world's first device driver for Microsoft Windows NT, Windows 2000, Windows XP and Windows Server2003 which enables the direct hardware access for your existing software without any programming efforts on your side. We have downloaded Direct I/O device driver from site www.direct-io.com.

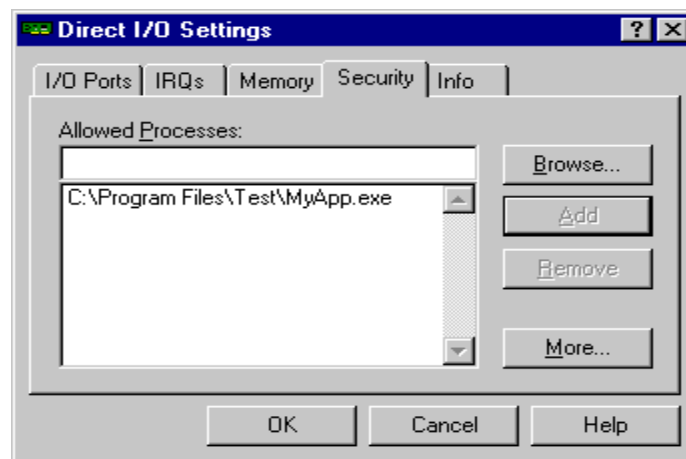
It is especially useful for existing 16bit software which accesses special hardware, e.g. programmers or data acquisition boards. Even 32bit software developed can have benefits from the easy access to the hardware.

We never have to bother with complex and expensive DDK toolkits again. With Direct I/O one can continue to use your existing software and hardware after migrating to Microsoft Windows NT, Windows 2000, Windows XP and Windows Server2003. There is no need to update to 32bit versions any more. Here is a brief idea how easy it is to use Direct I/O. It shows step-by-step how to integrate Direct I/O with your own application. Let's imagine we have to write an application named MYAPP.EXE to control a special hardware with I/O ports in the range 310-31Fh.

1. Enter the resources needed:



2. Give your application the right to access these resources:



Write your application: - C / C++ ,Visual Basic ,Delphi . Here is an example of C code.

5.3.3 Features of Direct I/O

Direct I/O is an Application Software with the following features:-

- Direct I/ O is a kernel mode driver together with a Virtual Device Driver (VDD).
- Direct I/ O enables access to I/O ports and memory mapped I/O for both 16bit and 32bit programs.

- I/O access is extremely fast. There is no impact on performance caused by Direct I/O.
- Interrupt emulation is supported for all 16bit and 32bit programs.
- Specify the programs which are allowed to use Direct I/ O. The risk of system corruption is minimal.
- It is controlled with its own control panel.
- It comes with a state-of-the-art installer with complete uninstall support.
- Customization and seamless integration of the installation into your setup can easily be done by yourself.
- It is fully compatible with Windows NT, Windows 2000, Windows XP and Windows Server2003.
- Direct I/ O includes comprehensive online help.
- It is shareware. It can be evaluated before buying it.

Chapter 6: Simulated Results and Observations

Simulation is an emerging area of technology. It is completely an interactive system of medical training based on user of innovative educational tools in highly realistic context of a clinical scenario. Arterial blood pressure, ECG, Heart frequency, Sp_{o2}, CO₂ production and other vital parameters trigger by the simulator are viewed on monitor. There are different software tools available for simulation and analysis. In this project ECG data file is executed using a C program and Direct I/O device driver is installed to make the process easy, fast and accurate.

The advantage of the system offers is that it can mimic in real time responses to treatment, whether technical or pharmacological. For clinical training of doctors to interpret the ECG of a Subject with proved diagnosis (i.e. the exact status of subject's heart is known through the clinical truths) we require the Subject, ECG amplifier and Monitor. The availability of such subject may not be practically feasible in all situations. The Doctors therefore have to mainly rely on recorded signals which do not give the real time experience to the Doctors.

An ECG simulator is device which can simulate all types of signals recorded previously in the real time mode. This simulator can be used both for clinical training of doctors as well as for design, development and testing of automatic ECG machine without having real subject for this purpose. The text file of ECG signal with proper annotation (Markings) was downloaded from <http://physionet.org> and stored in the folder. The 'C' program file named ECG.C was compiled and its executable file i.e. ECG.EXE was stored in the same folder. Upon running this executable file, the signal from DAC connected to the parallel port was displayed on DSO.

The quality of signal in terms of amplitude, duration and wave shape was similar to those obtained by signals from human subject & ECG amplifier. In absence of any Polaroid camera available in the lab, these signals could not be recorded to be reproduced in this report. However, the peaks annotated in the data file matched with those detected by peak detector.

Results

The below tables shows the results obtained with the ECG Simulator. The simulated electric waves were presented to electronic peak detectors. The red colored LEDs at the output of filters remained off under normal operating conditions and flashed a specific number of times indicating which particular channel is selected and every time the occurrence of QRS complex (highest peak of the ECG signal). The detected peaks exactly tallied with the annotated peaks in the given ECG database, thereby authenticating its efficacy.

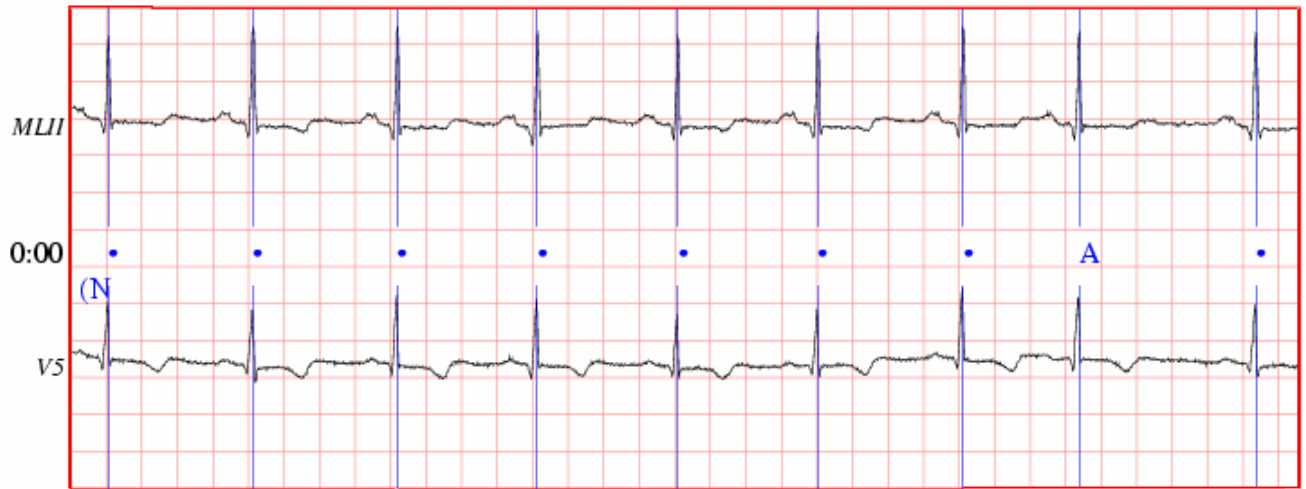


Figure 6.1 The peaks detected in ECG signal with leads MLII and V5

Table 6.1 Results for mitdb/100

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	13	13
V 5	0:00 – 0:10	13	13
ML II	0:10 – 0:20	12	12
V 5	0:10 – 0:20	12	12
ML II	0:20 – 0:30	12	12
V 5	0:20 – 0:30	12	12
ML II	0:30 – 0:40	12	12
V 5	0:30 – 0:40	12	12
ML II	0:40 – 0:50	13	13
V 5	0:40 – 0:50	13	13
ML II	0:50 – 0:60	12	12
V5	0:50 – 0:60	12	12

Table 6.2 Results for mitdb/102

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
V 5	0:00 – 0:10	12	12
V 2	0:00 – 0:10	12	12
V 5	0:10 – 0:20	12	12
V 2	0:10 – 0:20	12	12
V 5	0:20 – 0:30	12	12
V 2	0:20 – 0:30	12	12
V 5	0:30 – 0:40	12	12
V 2	0:30 – 0:40	12	12
V 5	0:40 – 0:50	13	13
V 2	0:40 – 0:50	13	13
V 5	0:50 – 0:60	12	12
V 2	0:50 – 0:60	12	12

Table 6.3 Results for mitdb/103

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	11	11
V 2	0:00 – 0:10	11	11
ML II	0:10 – 0:20	12	12
V 2	0:10 – 0:20	12	12
ML II	0:20 – 0:30	11	11
V 2	0:20 – 0:30	11	11
ML II	0:30 – 0:40	12	12
V 2	0:30 – 0:40	12	12
ML II	0:40 – 0:50	12	12
V 2	0:40 – 0:50	12	12
ML II	0:50 – 0:60	12	12
V 2	0:50 – 0:60	12	12

Table 6.4 Results for mitdb/104

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
V 5	0:00 – 0:10	13	13
V 2	0:00 – 0:10	13	13
V 5	0:10 – 0:20	12	12
V 2	0:10 – 0:20	12	12

V 5	0:20 – 0:30	12	12
V 2	0:20 – 0:30	12	12
V 5	0:30 – 0:40	13	13
V 2	0:30 – 0:40	13	13
V 5	0:40 – 0:50	12	12
V 2	0:40 – 0:50	12	12
V 5	0:50 – 0:60	12	12
V 2	0:50 – 0:60	12	12

Table 6.5 Results for mitdb/105

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	14	14
V 1	0:00 – 0:10	14	14
ML II	0:10 – 0:20	13	13
V 1	0:10 – 0:20	13	13
ML II	0:20 – 0:30	14	14
V 1	0:20 – 0:30	14	14
ML II	0:30 – 0:40	14	14
V 1	0:30 – 0:40	14	14
ML II	0:40 – 0:50	14	14
V 1	0:40 – 0:50	14	14
ML II	0:50 – 0:60	14	14
V 1	0:50 – 0:60	14	14

Table 6.6 Results for mitdb/108

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	11	11
V 1	0:00 – 0:10	11	11

ML II	0:10 – 0:20	10	10
V 1	0:10 – 0:20	10	10
ML II	0:20 – 0:30	10	10
V 1	0:20 – 0:30	10	10
ML II	0:30 – 0:40	10	10
V 1	0:30 – 0:40	10	10
ML II	0:40 – 0:50	10	10
V 1	0:40 – 0:50	10	10
ML II	0:50 – 0:60	9	9
V 1	0:50 – 0:60	9	9

Table 6.7 Results for mitdb/112

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	14	14
V 1	0:00 – 0:10	14	14
ML II	0:10 – 0:20	15	15
V 1	0:10 – 0:20	15	15
ML II	0:20 – 0:30	14	14
V 1	0:20 – 0:30	14	14
ML II	0:30 – 0:40	14	14
V 1	0:30 – 0:40	14	14
ML II	0:40 – 0:50	14	14
V 1	0:40 – 0:50	14	14
ML II	0:50 – 0:60	14	14
V 1	0:50 – 0:60	14	14

Table 6.8 Results for mitdb/113

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	9	9

V 1	0:00 – 0:10	9	9
ML II	0:10 – 0:20	10	10
V 1	0:10 – 0:20	10	10
ML II	0:20 – 0:30	10	10
V 1	0:20 – 0:30	10	10
ML II	0:30 – 0:40	10	10
V 1	0:30 – 0:40	10	10
ML II	0:40 – 0:50	9	9
V 1	0:40 – 0:50	9	9
ML II	0:50 – 0:60	10	10
V 1	0:50 – 0:60	10	10

Table 6.9 Results for mitdb/116

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	13	13
V 1	0:00 – 0:10	13	13
ML II	0:10 – 0:20	13	13
V 1	0:10 – 0:20	13	13
ML II	0:20 – 0:30	13	13
V 1	0:20 – 0:30	13	13
ML II	0:30 – 0:40	13	13
V 1	0:30 – 0:40	13	13
ML II	0:40 – 0:50	13	13
V 1	0:40 – 0:50	13	13
ML II	0:50 – 0:60	13	13
V 1	0:50 – 0:60	13	13

Table 6. 10 Result for mitdb/117

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	9	9
V 2	0:00 – 0:10	9	9
ML II	0:10 – 0:20	8	8
V 2	0:10 – 0:20	8	8
ML II	0:20 – 0:30	8	8
V 2	0:20 – 0:30	8	8
ML II	0:30 – 0:40	9	9
V 2	0:30 – 0:40	9	9
ML II	0:40 – 0:50	8	8

V 2	0:40 – 0:50	8	8
ML II	0:50 – 0:60	8	8
V 2	0:50 – 0:60	8	8

Table 6.11 Result for mitdb/121

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	10	10
V 1	0:00 – 0:10	10	10
ML II	0:10 – 0:20	10	10
V 1	0:10 – 0:20	10	10
ML II	0:20 – 0:30	10	10
V 1	0:20 – 0:30	10	10
ML II	0:30 – 0:40	10	10
V 1	0:30 – 0:40	10	10
ML II	0:40 – 0:50	10	10
V 1	0:40 – 0:50	10	10
ML II	0:50 – 0:60	10	10
V 1	0:50 – 0:60	10	10

Table 6.12 Result for mitdb/122

LEAD	INTERVAL In seconds	ANNOTATED PEAKS	PEAKS DETECTED
ML II	0:00 – 0:10	15	15
V 1	0:00 – 0:10	15	15
ML II	0:10 – 0:20	15	15
V 1	0:10 – 0:20	15	15
ML II	0:20 – 0:30	15	15
V 1	0:20 – 0:30	15	15
ML II	0:30 – 0:40	14	14
V 1	0:30 – 0:40	14	14
ML II	0:40 – 0:50	14	14
V 1	0:40 – 0:50	14	14
ML II	0:50 – 0:60	14	14
V 1	0:50 – 0:60	14	14

Chapter 7: Conclusions and Future Scope

The project was successfully implemented to simulate Dual channel ECG signal in terms of signal amplitude, duration and waveform. The simulated electric waves were presented to electronic peak detectors. The detected peaks exactly tallied with the annotated peaks in the given ECG database, thereby authenticating its efficacy.

Since, all the output lines of the parallel port were not fully exploited in this endeavour an attempt should be made to develop multichannel ECG simulator.

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