STUDY THE SUBTHRESHOLD LOGIC DESIGN

Dissertation submitted in the partial fulfillment of requirement for the award of degree of

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in
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DECLARATION

I hereby declare that the work which is being presented in the dissertation entitled, **"Study the Subthreshold Logic Design"** in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of Mr. Mayank Kumar Rai, Assistant Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

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My greatest thanks are to my parents who always wished me success. They have always wanted the best for me and I admire their determination and sacrifice.

Date: Hemant Sharma

Place: Patiala

ABSTRACT

In this report, an equivalent RC delay approach to study the subthreshold operation for inverter, AND logic and OR logic circuits is presented. In these subthreshold circuits, the supply voltage is below the threshold voltage of the device. The symmetric inverter is designed for subthreshold current model, which is exponential in nature and is a more accurate model which considers the effect of thermal energy on the Boltzmann distribution of electron energies. Based on the inverter, the other static circuits and domino circuits are designed and various bulk biasing schemes are used. Taking the effect of miller capacitance, equivalent capacitance is calculated. The average resistance is also calculated for each circuit and based on this, the 90% delay is calculated for each case. The results of RC delay are compared with SPICE simulation in 32nm technology.

The results reveal the domino OR type 4 has least delay among all domino OR circuits and AND type 1 has least delay among all domino AND circuits. This is due to the fact that these circuits have least output capacitances. Comparison on the basis of Power Delay Product (PDP) is also done for all the circuits in subthreshold regime. Domino OR type 2 and domino AND type 2 are more efficient due to the lower value of the power delay product.

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ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
EDA	Electronic Design Automation
ITRS	International Technology Road Map for Semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
PTM	Predictive Technology Model

Chapter 1

Introduction

With the reduction in the MOS technology and the growing demand for system portability, the number of devices per chip increase which results in high power consumption. Delay and power reduction are two primary design constraints. One of the approach to reduce power is to decrease supply voltage but this also reduces drain currents which in turn decrease circuit speed. So there is a compromise between delay and power as decreasing one, increases other.

MOSFETs or Metal oxide Semiconductor Field Effect Transistors are used almost in every electronic circuit. They have the property of amplifying electrical signals and can also be used for switching activity. Although the MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals, the body (or substrate) of the MOSFET often is connected to the source terminal, making it a three-terminal device like other Field Effect Transistors.

1.1 Modes of operation:

The operation of a MOSFET can be separated into three different modes, depending on the voltages at the terminals[1].

1. Cutoff, subthreshold, or weak-inversion mode
2. Triode mode or linear region
3. Saturation mode

1.1.1 Cutoff, subthreshold, or weak-inversion mode :

According to the basic threshold model, the transistor is turned off, and there is no conduction between drain and source. A more accurate model considers the effect of thermal energy on the Boltzmann distribution of electron energies which allow some of the more energetic electrons at the source to enter the channel and flow to the drain. This current is due to weak inversion so it is

called weak inversion current. This current is an exponential function of gate–source voltage.

$$I_{ds} = I_0\left[1 - e^{-V_{ds}/V_t}\right]e^{((V_{gs}-V_{th}-V'_{off})/nV_t)} \quad (1.1)$$

$$I_0 = \mu\frac{W}{L}\sqrt{\frac{q\epsilon_{si}(NDEP)}{2\varphi_s}}V_t{}^2 \quad (1.2)$$

where, I_{ds} = SubthresholdCurrentfrom drain to source terminals

V_t = Thermal voltage

n = Subthreshold slope factor (1 + NFACTOR. C_{dep}/C_{ox})

μ= Charge-carrier effective mobility.

W= The gate width

L= The gate length

V_{th} = Threshold voltage

NDEP= Channel Doping concentration at zero bias

V'_{off} = Offset voltage.

1.1.2 Triode mode or linear region :

When $V_{GS} > V_{th}$ and $V_{DS} < (V_{GS} - V_{th})$

The transistor turns on, and a channel has been created which allows current to flow between the drain and the source. The channel is created when strong inversion occurs i.e. gate to source voltage is above the threshold voltage of the device. The MOSFET operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. The current from drain to source is modeled as:

$$I_D = \mu_0 C_{ox}\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}{}^2}{2}\right) \quad (1.3)$$

1.1.3 Saturation or active mode :

When $V_{GS} > V_{th}$ and $V_{DS} > (V_{GS} - V_{th})$

The switch is turned on, and a channel has been created, which allows current to flow between the drain and source. Since the drain voltage is higher than the gate voltage,

the electrons spread out, and conduction is not through a narrow channel but through a broader, two- or three-dimensional current distribution extending away from the interface and deeper in the substrate. The onset of this region is also known as pinch-off to indicate the lack of channel region near the drain. The drain current is now weakly dependent upon drain voltage and controlled primarily by the gate–source voltage, and modeled approximately as:

$$I_D = \mu_0 C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \left(1 + \lambda (V_{DS} - V_{DSsat})\right) \qquad (1.4)$$

λ is the channel-length modulation parameter.

1.2 Subthreshold conduction:

With the scaling of devices and a reduction in the technology, the threshold voltage of NMOS and PMOS also decreases which makes subthreshold operation more challenging task. In this region the current flows due to weak inversion so gate to source voltage is bellow threshold voltage of the device. This current is also called leakage current[2].

The reason for a growing importance of subthreshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. The amount of subthreshold conduction is set by the threshold voltage, which sits between the ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device off, and as subthreshold conduction varies exponentially with gate voltage, it becomes more and more significant as MOSFETs shrink in size. Subthreshold conduction is only one component of leakage: other leakage components that can be roughly equal in size depending on the device design are gate-oxide leakage and junction leakage.

1.3 MOS Capacitances in Subthreshold Regime：

The capacitances strongly influence gate delay and dynamic energy consumption. The device parasitic capacitancesare depicted in Fig. 1.1 and discussed as follows [3]:

1) Junction capacitance C_j

2) Overlap capacitance C_{ov}
3) Inner fringing capacitance C_{if}
4) Outer fringing capacitances $C_{off,side}$, $C_{off,top}$, $C_{off,dif}$.

1) Junction Capacitance: Source/drain junction capacitances are composed of a bottom and sidewall parts. Capacitance values depend on the doping level of the substrate and of the source/drain diffusion. The junction capacitance per area to grow with technology scaling because of higher doping levels.

2) Overlap Capacitance: The overlap capacitance per width unit is C_{ov} , with the overlap length L_{ov}. C_{ov} per side has been shown to be roughly equivalent to 20% of the intrinsic gate capacitance $C_{g,sup}$, for minimum length devices for a wide range of technology nodes. Therefore, we set to 20% of the minimum channel length. The resulting follows the evolution of C_{ox} and $C_{g,nom}$.

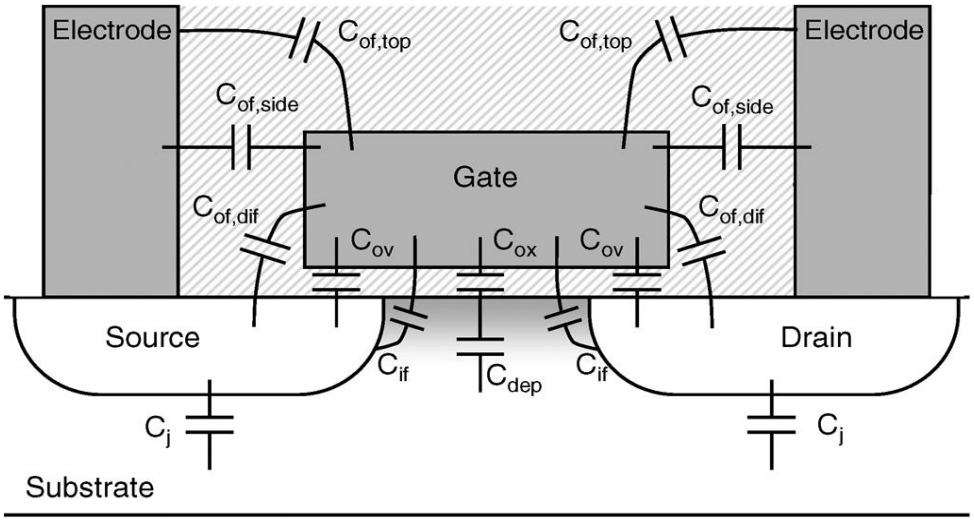


Fig 1.1MOS capacitances in subthreshold regime [3].

3) Fringing Capacitance: The last parasitic gate capacitance category is fringing capacitance, which becomes more and more important with technology scaling because of the proximity of source/drain electrodes. It is composed of the inner fringing capacitance through the channel C_{if} and the outer fringing capacitances: from gate side to the electrodes $C_{of,side}$, from gate top to the electrodes $C_{of,top}$, and from gate side to the diffusions $C_{of,dif}$.

1.4 Dynamic CMOS logic:

In integrated circuit design, dynamic logic (or sometimes clocked logic) is a design methodology in combinatorial logic circuits, particularly those implemented in MOS technology [4]. It is distinguished from the so-called static logic by exploiting temporary storage of information in stray and gate capacitances.Dynamic logic is distinguished from so-called *static logic* in that dynamic logic uses a clock signal in its implementation of combinational logic circuits.

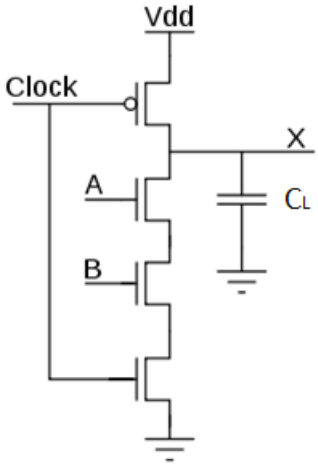


Fig 1.2 Dynamic logic implementation [4].

Dynamic logic has a few potential problems that static logic does not. For example, if the clock speed is too slow, the output will decay too quickly to be of use.Also, when both *A* and *B* are high, so that the output is low, the circuit will pump one capacitor-load of charge from Vdd to ground for each clock cycle, by first charging and then discharging the capacitor in each clock cycle. This makes the circuit (with its output connected to a high impedance) less efficient than the static version.Its popular implementation is Domino logic.

1.5 Domino Logic:

Domino logic is a CMOS-based evolution of the dynamic logic techniques based on either PMOS or NMOS transistors [4]. It allows a rail-to-rail logic swing. It was developed to speed up circuits. Here an inverter is cascaded after Fig 1.2. In a domino logic cascade structure consisting of several stages, the evaluation of each stage ripples

the next stage evaluation. Once fallen, the node states cannot return to "1" (until the next clock cycle).

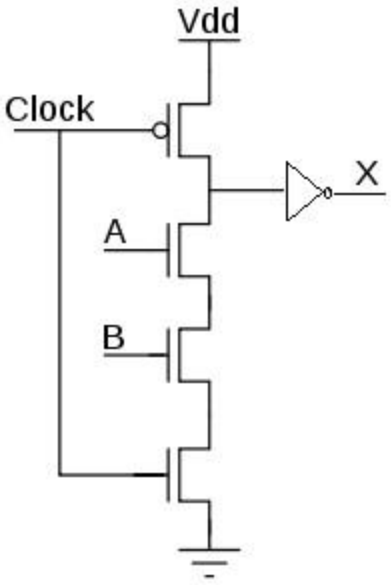


Fig 1.3 Domino logic.

Important Domino Logic features include:

1. They have smaller areas than conventional CMOS logic.
2. Parasitic capacitances are smaller so that higher operating speeds are possible.
3. Operation is free of glitches as each gate can make only one transition.
4. Only non-inverting structures are possible because of the presence of inverting buffer.
5. Charge distribution may be a problem.

1.6 Domino Logic with a Keeper:

During evaluate phase, If both A & B are “1”, the output node comes to “0”. In the same clock cycle if A or B or both become “0” afterwards then the output node can't be charged again until the next clock cycle. This problem was solved by using a keeper transistor (PMOS). The keeper transistor is weak in nature. When the above situation arises, it automatically charges the output node. This has been shown in fig 1.4.

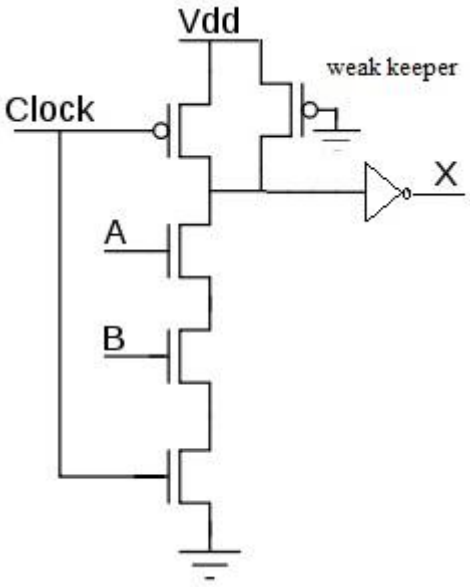


Fig 1.4 Domino logic with a keeper.

The weak keeper means the dimensions of keeper transistor should be minimum i.e. it should be weak in nature. Whenever there is the strong path from the output node to ground, this weak keeper will not have much effect on the node voltage but if there is no path to ground then the node will be charged to “logic 1” or Vdd.

Chapter 2

Literature Review

Over last decade, subthreshold logic has become a popular way to achieve ultralow power consumption for digital circuits.Earlier papers were more of theoretical explanations of subthreshold logic. Effects like scaling of supply voltage, threshold voltage were considered, But the technology used was 90um technology. In today's simulations we generally use 180-32 nm technology.

Ultralow power applications fields such as biomedical devices, sensor networks and radio frequency identification(RFID) tags typically require low cost robust circuits. Therefore, CMOS technologies are used to implement subthreshold logic. The technology nodes considered in research articles on subthreshold logic are considered in International Technology Roadmap for Semiconductors (ITRS) reports [5]. Many analytical solutions for Short-channel effects on the subthreshold behavior on self-aligned gate in the subthreshold region were being proposed [6]. Other analytical approaches were followed to get the expressions of subthreshold current by self reverse biasing [7]. Current-voltage models in the subthreshold regime for sub micrometer SOI MOSFETs were formed which take effective depleted charge on the drain [8]. Three dimensional device physics based analytical models were developed for subthreshold conduction. Some models take flicker noise in n-MOSFET in various regions [9,10]. Subthreshold swing was calculated and taken into consideration in 1997 [11]. Technology scaling comes with some drawbacks: increase of short channel effects [6], leakage currents and variability. Among them variability has been shown to be a severe limitation for subthreshold logic [12].

From last decade, the more papers were focused on power and delay. Logic families like variable threshold voltage subthreshold CMOS and subthreshold dynamic threshold voltage MOS logic, were proposed [13]. Both logic families have comparable power consumption as a regular subthreshold CMOS logic with a superior robustness and tolerance to process and temperature variations. Analytical models with simulations were done to minimize energy operation for subthreshold circuits [14]. Till now, the only power or delay was considered in subthreshold circuits. In early 2005, device designs apt

for subthreshold operation were proposed [15]. The optimized device improves the delay and the power delay product (PDP) of an inverter chain by 44% and 51%, respectively. Designing of Operational amplifiers in subthreshold region for Low voltage and Low current were proposed with supply voltage of 0.6V [16]. For getting low voltage and low current Bulk-driven technique is used to operate in low power. After this, a new full adder (FA) circuit optimized for ultra low power operation was proposed [17]. The circuit is based on modified XOR gates operated in the subthreshold region to minimize the power consumption. The simulation results show a 5%-20% for frequency ranges from 1 KHz to 20 MHz and supply voltages lower than 0.3 V. The temperature dependence of transistor mismatch in 65-nm CMOS platform over a temperature range of 0degC to 125degC were considered [18]. This analysis shows, for the first time, that although relative-current-mismatch fluctuation standard deviations estimated on whole populations are reduced at higher temperatures, the current mismatch of individual pairs can change substantially over temperature.

Subthreshold logic is an efficient technique to achieve ultralow energy per operation for low-to-medium throughput applications. The interests and limitations of technology scaling for subthreshold logic are investigated from 0.25 um to 32 nm nodes [3]. Scaling to 90/65 nm nodes is shown to be highly desirable for medium-throughput applications (1–10 MHz) due to great dynamic energy reduction. However, this interest is limited at 45/32 nm nodes by high static energy due to degraded subthreshold swing and delay variability.Operation with power supply as low as 60 mV is demonstrated to design ultra low power operation devices [19].In addition, it is shown that subthreshold leakage current can be useful for other applications like thermal sensors. The concepts of critical path and pipelining to reduce the delay were considered in designing asynchronous circuits[20]. The silicon nano wire transistor (SNWT) -based circuits of current mirrors (NWCMs) have been successfully fabricated for the first time [21]. The key figures of merit of current mirrors (CMs) make circuits more reliable. Low power, low noise amplifier with subthreshold operation for Global Position System (GPS) L1-band radio frequency (RF) receiver using a 0.18 um CMOS process was proposed [22]. A level converter based on dynamic logic style for sub-threshold I/O part, having a large dynamic range of conversion was proposed [23]. A test chip is fabricated in 130-nm CMOS technology and results show that the level converter successfully converts 0.3 V 8 MHz pulse to 2.5 V signal.

Recently, the focus has been put on using Carbon Nano Tube interconnects (CNT) in subthreshold operation. The individual SWNTs can be used as interconnects in subthreshold circuits to improve delay and energy-per-bit by up to 5 times and 6 times, respectively [24-25]. In light of recent advances in wafer-level fabrication of long aligned isolated SWNTs, the results can potentially open up a new and less challenging path toward SWNT interconnects.

Various parasitic capacitances in deep sub micrometer technology are calculated and their equations are modeled [26]. The ultra low power digital circuits based on various biasing schemes in domino logic are simulated on 65nm technology & their corresponding PDP is compared [27].Subthreshold currents increase exponentially and many models were developed which calaculate subthreshold current and swing[28]. Delay variations are studied and analytically derieved for PVT(Pressure, voltage and temperature) variations in subthreshold circuits[29]. Many of these delay models are complicated and lack clear formulas. In [30-31], the models are derived from direct use of Gaussian law rather than using poison equation. To reduce delay many bulk biasing schemes are used in [27].

So, we will be more concentrating on improving the delay and power of subthreshold logic circuits. Optimization will be done on the basis of compromise between delay and power to get best Power-Delay Product (PDP). To reduce the delay we will be using various bulk biasing schemes mentioned in [27]. Based on the current Predictive Technology Model BSIM 4.0 [33], we will derive the expression for symmetrical inverter and other circuits will be designed. Their internal capacitances will be calculated from expressions given in [3,26]. Based on these capacitances the output capacitance is calculated and RC delay is compared with simulated delay for different bulk biasing schemes.

Chapter 3

Design of Bulk Biasing Schemes

With the reduction of power supply voltage in subthreshold logic design, the power consumption decreases. So our main concern now remains to reduce delay. Delay can be reduced by using the dynamic logic style instead of using static logic style. Dynamic logic in turn increases the power so there is a compromise between delay and power consumption. Domino logic is a type of dynamic logic style in which we will implement basic AND & OR gates.

Various Bulk biasing schemes are to be used as mentioned in [27]. The different bulk biasing schemes have effect on threshold voltage of device and hence provide more flexibility in subthreshold region. The bulk bias is related to threshold voltage by a relation

$$V_T = V_{T0} + \gamma\left[\sqrt{|2\varphi + V_{SB}|} - \sqrt{|2\varphi|}\right] \qquad (3.1)$$

From above equation, it can be seen that the threshold volatege (V_T) is dependent on source to bulk voltage (V_{SB}). With the various bulk biasing schemes, the V_{SB} changes which changes the threshold voltage of device and hence varies the performance of circuit in subthreshold regime.

3.1Bulk Biasing schemes

The subthreshold operation is analyzed under six bulk biasing schemes [27] as shown in figure 3.1.

Type1. Bulk of NMOS connected to Gnd and bulk of PMOS connected to supply voltage.
Type2. Bulk of NMOS connected to clock and bulk of PMOS connected to supply voltage.
Type3. Bulk of NMOS connected to Gnd and bulk of PMOS connected to clock.
Type4. Bulk of NMOS and PMOS connected to supply voltage.
Type5. Bulk of NMOS and PMOS connected to Gnd.

Type6. Bulk of NMOS connected to supply voltage and Bulk of PMOS connected to Gnd.

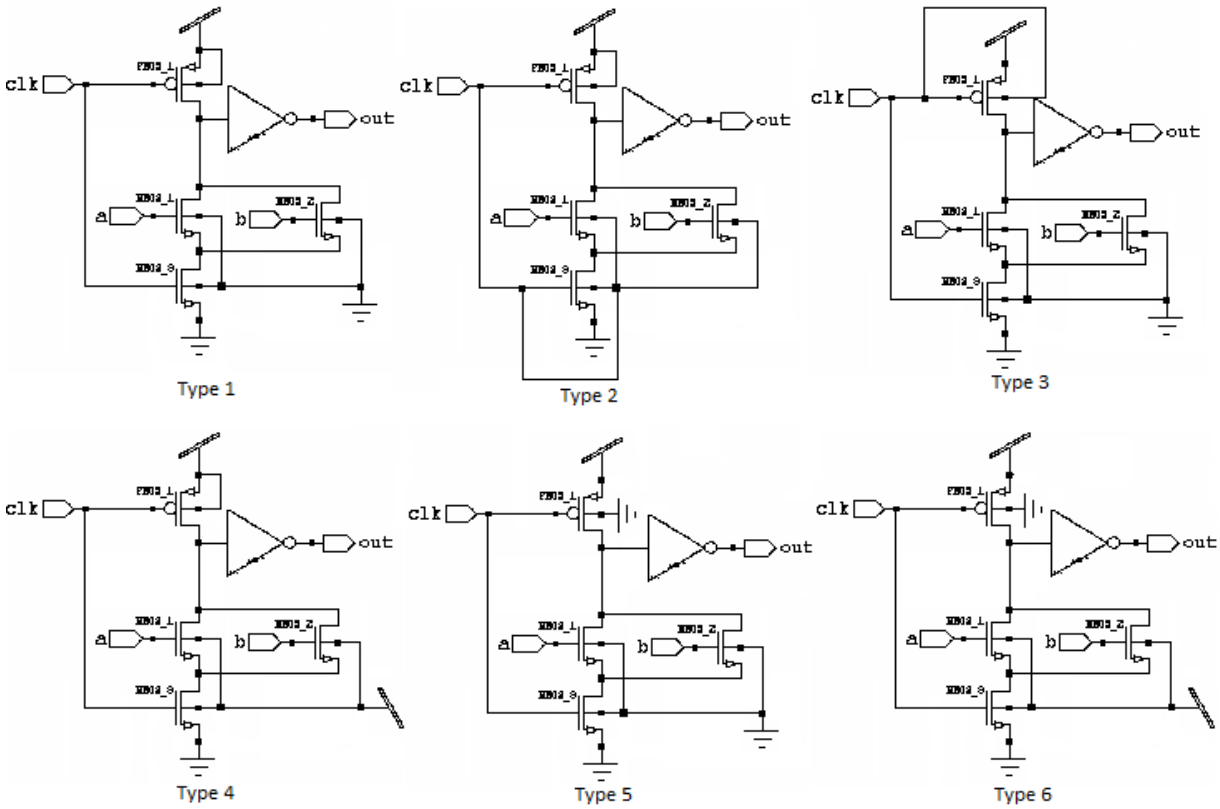


Fig 3.1 Various bulk biasing schemes [27].

In the above figure, we can see that in Type 1, the bulk of NMOS is connected to ground and bulk of PMOS is connected to supply voltage. So the threshold voltage of NMOS and PMOS in this case are minimum equal to V_{T0n} and V_{T0p} respectively. Similarly for other cases in which Bulk of NMOS or PMOS are connected to some other voltage, the V_{SB} is non-zero and hence we will have higher threshold voltage for both. Based on these biasing schemes we will make various gates (AND / OR).

3.2 Design of an Inverter

As the current flowing in the subthreshold region is exponential in nature with respect to voltages so a little change in V_{ds} or V_{gs} will change the current by many folds. The equation given below shows the dependence and the symmetric inverter is designed assuming the current is equal at logic threshold which should lie exactly at $V_{dd}/_2$.

$$I_{ds} = I_0\left[1 - e^{-V_{ds}/V_t}\right]e^{((V_{gs}-V_{th}-V'_{off})/nV_t)} \quad (3.2)$$

$$\text{Where, } I_0 = \mu \frac{W}{L}\sqrt{\frac{q\epsilon_{si}(NDEP)}{2\varphi_s}}V_t^{\,2} \quad (3.3)$$

$$I_{0n}\left[1 - e^{-V_{dsn}/V_t}\right]e^{((V_{gsn}-V_{thn}-V'_{off})/nV_t)} = I_{0p}\left[1 - e^{-V_{sd}/V_t}\right]e^{((V_{sg}-|V_{thp}|-V'_{off})/nV_t)} \quad (3.4)$$

Solving this equation and eliminating variables by putting expressions of I_{0n} and I_{0p} we get finally

$$\frac{\mu_n\left(\frac{W}{L}\right)_n}{\mu_p\left(\frac{W}{L}\right)_p}\sqrt{\frac{NDEP_n}{NDEP_p}}e^{(|V_{Tp}|-V_{Tn})/nV_t} = 1 \quad (3.5)$$

Now, the values of various parameters are to be substituted from Predictive Technology model (PTM) and assuming $n = 1.35$ we get

$$(W/L)_n = 2.1\ (W/L)_p \quad (3.6)$$

Equation 3.6 needs attention as this shows that size of NMOS should be larger than size of PMOS for a symmetrical inverter in subthreshold region. This is due to the fact that the exponential dependence of current on threshold voltage of device. As the absolute value of threshold voltage of NMOS is more than PMOS so the little change in gate to source of PMOS will have more effect on current than NMOS and to balance that effect NMOS should be stronger or has higher dimensions than PMOS.

In the following figure (Fig 3.2), the symmetricity of the designed inverter is verified by dc analysis. The Voltage Transfer Characterstics (VTC) is shown and the sizes used are in analogous to equation 3.6. From the figure, we can see clearly that the logic threshold occurs exactly at $V_{dd}/_2$ (i.e. 150 mV). This important result can be further used to design other circuits based on this symmetric inverter.

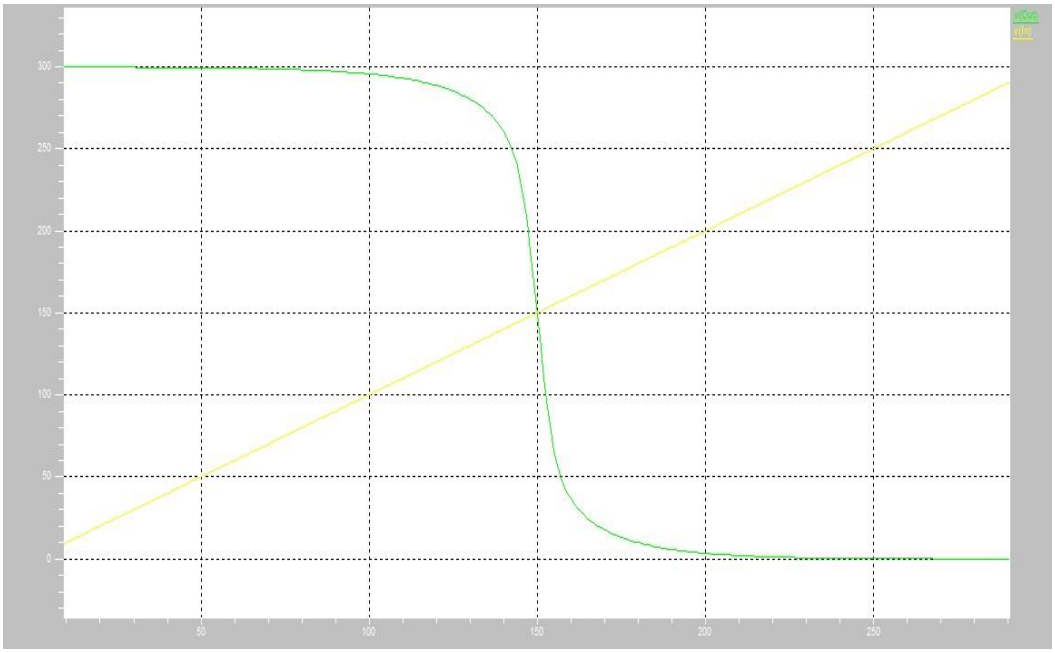


Fig 3.2 Voltage Transfer Characteristics of an inverter.

3.3 Design of Circuits

On the basis of above designed symmetric inverter for subthreshold region, the other circuits like static OR, static AND, domino OR(with keeper) and domino AND (with keeper) are designed for the worst case.

The worst case analysis for static AND shows $(W/L)_n = 4.2\,(W/L)_p$ and for static OR it is $(W/L)_n = 1.905\,(W/L)_p$ .For the domino circuits, the domino AND (with keeper) should have $(W/L)_n = 12.6\,(W/L)_p$ and the domino OR (with keeper) should have $(W/L)_n = 8.4\,(W/L)_p$ to make the circuits symmetric in nature. Figure 3.3 a) shows the VTC of a static AND andfigure 3.3 b) shows the VTC of a static OR.

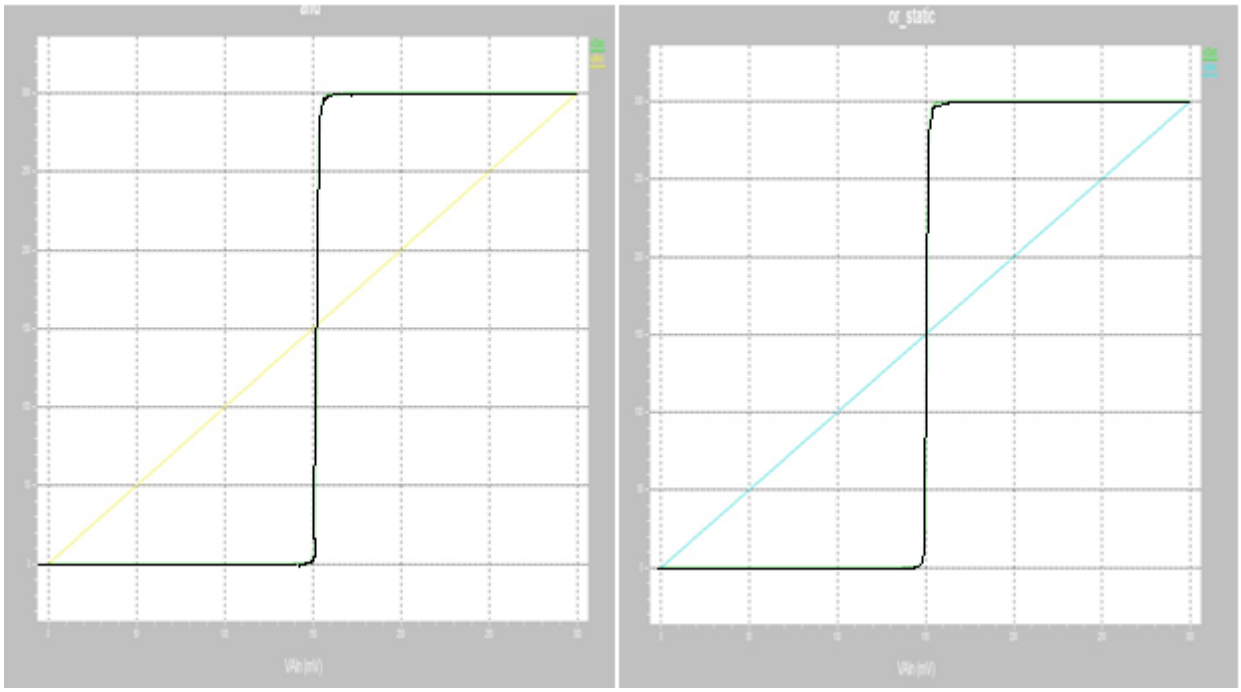


Fig 3.3 a) VTC of a static AND b) VTC of a static OR

In the above figure, we can see that the logic gates are symmetric in nature as designed and their logic threshold is exactly at $V_{dd}/_2$.

Chapter 4

Parasitic Capacitances

4.1 Capacitance in subthreshold region

Here we study, the various capacitances formed inside the MOS and how these capacitances effect the delay of the circuit. As discussed earlier they are divided into four categories [3,26]

1) Junction capacitance C_j.
2) Overlap capacitance C_{ov}.
3) Inner fringing capacitance C_{if}.
4) Outer fringing capacitances C_{ofside} ,C_{oftop} ,C_{ofdif} .

The capacitances per unit width are modeled by

$$C_{ov} = \frac{\epsilon_{ox} L_{ov}}{t_{ox}} \tag{4.1}$$

$$C_{if} = 2\epsilon_{si} \ln\left(1 + \frac{X_j}{2t_{ox}}\right) \tag{4.2}$$

$$C_{ofside} = \epsilon_{ox}\left(\frac{t_{ox} + t_{gate}}{L_{gsd}} - 0.55\right) \tag{4.3}$$

$$C_{oftop} = \frac{2*0.8\epsilon_{ox}}{\pi} ln\left(1 + \frac{L_g}{2L_{gsd}}\right) \tag{4.4}$$

$$C_{ofdif} = \frac{0.8\,\epsilon_{ox}}{\pi} ln\left((M^2 - 1)\left(\frac{M^2}{M^2-1}\right)^{M^2}\right) \tag{4.5}$$

$$C_{BX} = \frac{C_j * AX}{\left[1 - \frac{v_{BX}}{PB}\right]^{MJ}} + \frac{C_{jsw} * PX}{\left[1 - \frac{v_{BX}}{PB}\right]^{MJSW}} \tag{4.6}$$

$$C_{gdox} = 0.4\, WL_{eff}\, C_{ox} \tag{4.7}$$

$$C_{gsox} = 0.6\, WL_{eff}\, C_{ox} \tag{4.8}$$

Where, t_{gate} is gate electrode height, X_j is source/drain diffusion depth and L_{gsd} is distance between gate and the source/drain metal electrodes. Here, M is defined as $M = \frac{L_{gsd}}{t_{ox}}$. From the design rule, we see that $L_g = 2L_{gsd}$.

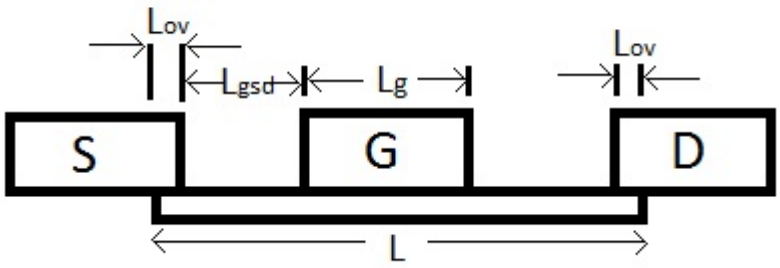


Fig 4.1 Crossectional view showing various lengths.

From the figure 4.1 and the design rule stated above, we see that $L = L_{ov} + L_{gsd} + L_g + L_{gsd} + L_{ov}$ and $L_g = 2L_{gsd}$. So, the values can be easily found as all lengths are technology dependent.

In equations 4.7 and 4.8, we can see that 40/60 partitioning is used in which 40% contribution of total oxide capacitance is taken in drain and 60% contribution is taken by source terminal.

The values from Predictive Technology Model (PTM) [33] with BSIM v 4.0 are taken and the capacitances per unit width are

$$C_{ov} = 69.576\ pF/m$$
$$C_{if} = 122.143\ pF/m$$
$$C_{ofside} = 15.750\ pF/m$$
$$C_{oftop} = 12.189\ pF/m$$
$$C_{ofdif} = 50.184\ pF/m$$
$$C_{gdox} = 590\ pF/m$$
$$C_{gsox} = 896.58\ pF/m$$

So, the value of gate to source and gate to drain capacitance per unit width are $C_{gs} = 1.167\ nF/m$ and $C_{gd} = 0.860 nF/m$. From equation 4.6, we can see that C_{BX} (X is either source or drain terminal) is dependent on voltage of bulk to source or drain terminal and also

dependent on area of source/drain (AS/AD) or perimeter of source/drain (PS/PD). So, there value will be different for different biasing schemes depending on the bulk voltages.

4.2 Parasitic Extractions

4.2.1 Output capacitance of Inverter

As we know during each cycle of input (rise and fall), the internal capacitances are charged and discharged. Here capacitances which are charged and discharged are to be analyzed for an inverter. Figure 4.2 shows the schematic of a CMOS inverter with In as input port and Out as output port.

When there is a constant ‘logic 0’ at the In then the PMOS is ON and NMOS is OFF. So, the Out node is charged to ‘logic 1’ through the PMOS. During this charging of Out node, the various output capacitances formed inside the PMOS or NMOS (which are connected to Out) are charged. Similarly, when the In is ‘logic 1’, PMOS is OFF and NMOS is ON so, the Out port comes to ‘logic 0’ as there is a direct path from Out port to ground through NMOS. Here, the capacitances charged in the previous case and also connected to Out port are to be discharged.

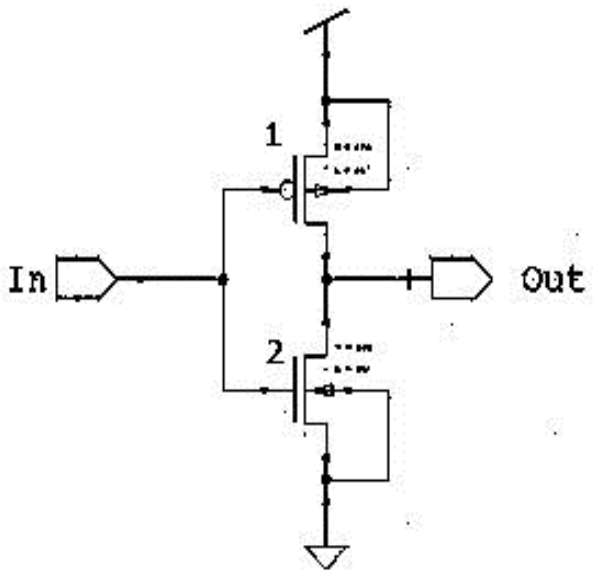


Fig 4.2 A CMOS Inverter

In table 4.1, the output capacitance of an inverter is shown during each input. Here C_{gd1} , C_{bd1} are the gate to drain and bulk to drain capacitance of PMOS respectively.C_{gd2}, C_{bd2} are the gate to drain and bulk to drain of NMOS respectively.

Table 4.1 Output capacitance of an inverter.

V_{in}	C_{out}
0	$C_{gd1} + C_{bd2} + C_{gd2}$
1	$C_{gd1} + C_{bd1} + C_{gd2}$

In fig 4.3, we can see the various capacitances formed between different terminals. Here bulk of PMOS is connected to supply voltage and bulk of NMOS is connected to ground so bulk to source capacitance of both is not taken as they are being shorted.

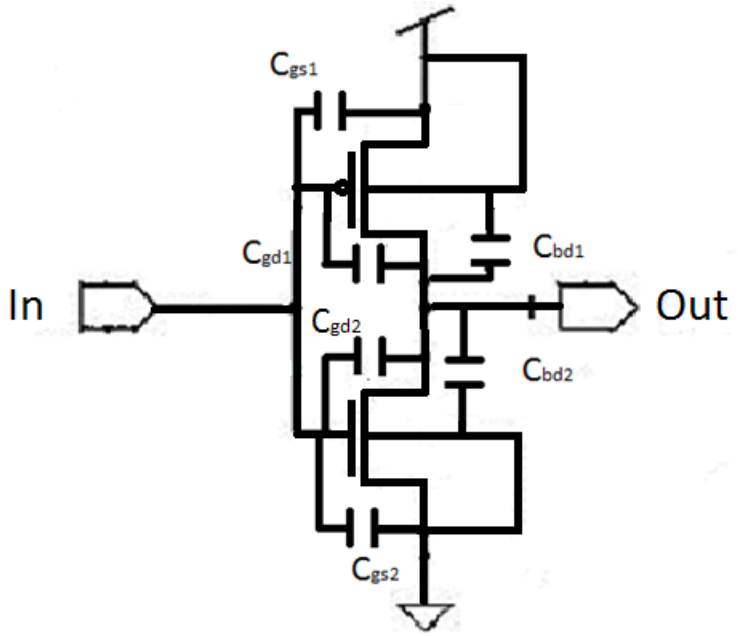


Fig 4.3 Capacitances formed inside an inverter.

In the following figure 4.4, the capacitance for the first case i.e. In=0 are shown. C_{gd1} has one of the terminal connected to input port (In=0) and other connected to output port (Out=1) so it is being charged due to the potential difference so contribute in output capacitance. Similarly, C_{bd2} and C_{gd2} are connected to output port and also have potential difference across their terminals. But all other capacitances either have no potential difference (same potential) or are not connected to output port so do not contribute to C_{out}.

In the same way for In=1, the expression of output capacitance is to be calculated and is same as shown in table 4.1.

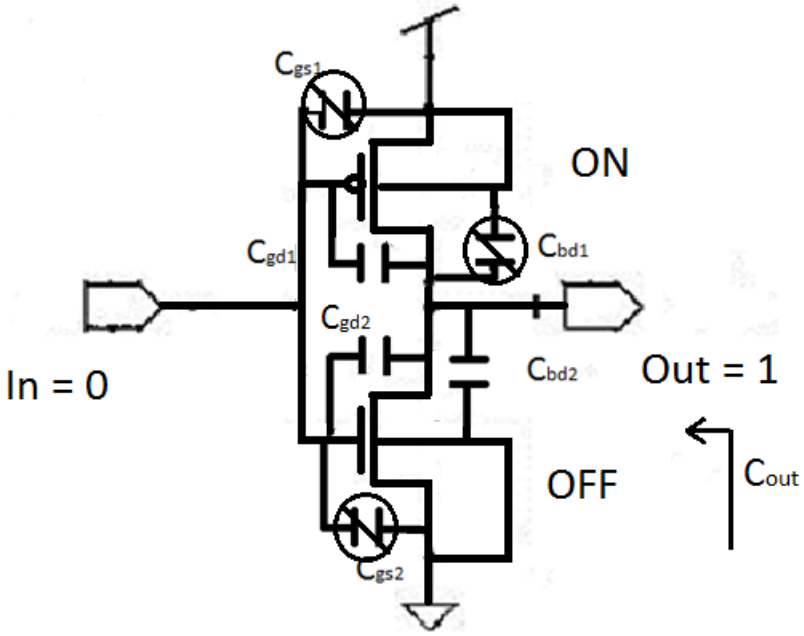


Fig 4.4 Capacitance formed when In =0 and Out =1.

4.2.2 Output capacitance of other circuits

From the previous section, the procedure to calculate the expressions of output capacitance is clear. This same approach is applied to static OR, static AND, domino OR and domino AND (type1 to type6). In figure 4.5, the internal capacitances for domino OR type1 are shown. The case shown here is when A=0, B=1 and Phi=1. So, the Out1 node (intermediate node before inverter) is 0. From this figure we can see that $C_{gd\,1}$ will be charged as its one node is connected to Phi(=1) and other node is connected to Out1(=0) so there is a potential difference between two terminals of the capacitor. Similarly, $C_{bd\,1}, C_{bd\,5}, C_{gs\,3}, C_{gd\,4}$ and $C_{gd\,3}$ are charged due to difference in potential across their terminals and other capacitors like $C_{gd\,2}$ are not charged as their both terminals are at same potential (in this case A=0 and Out1=0).

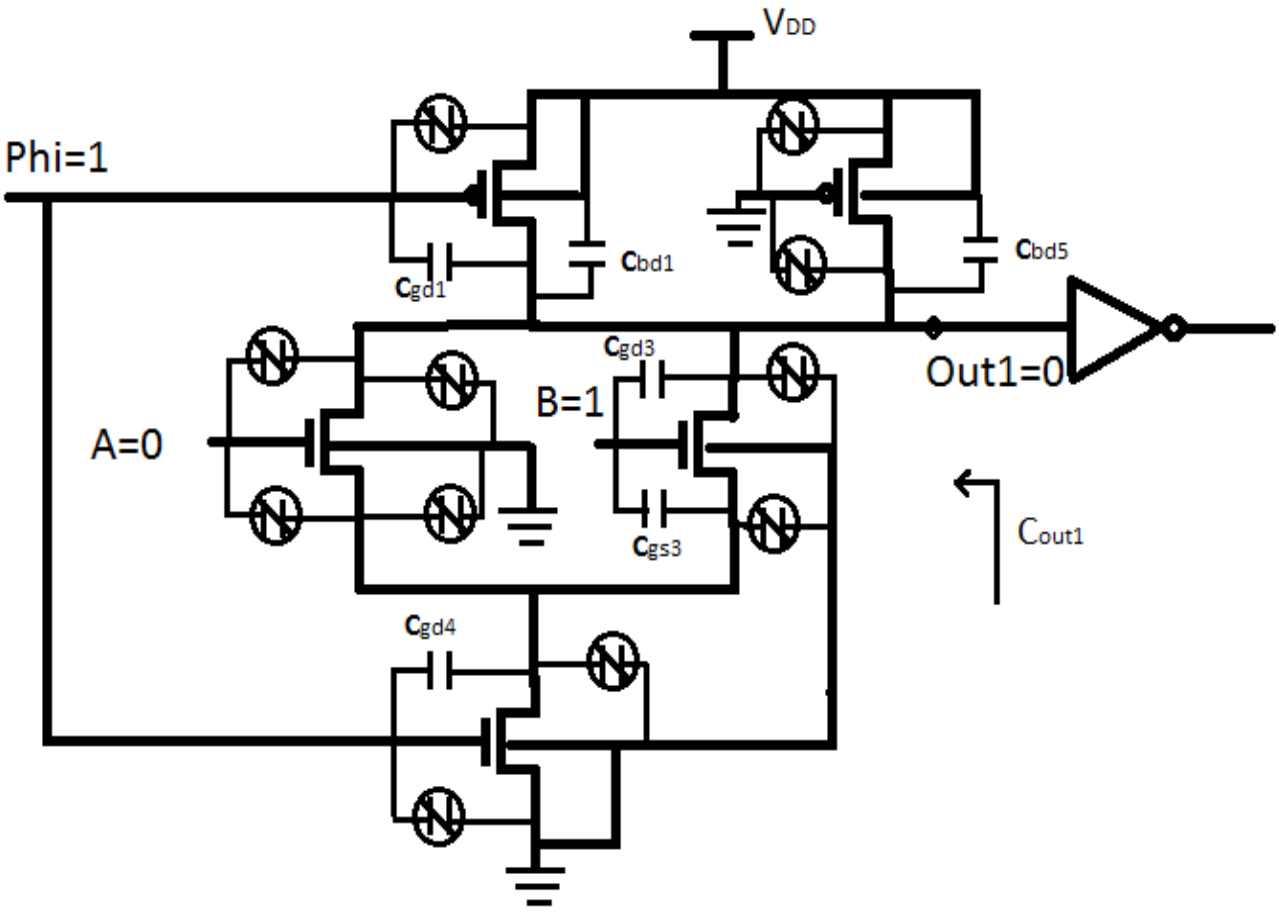


Fig 4.5 Capacitance formed in domino OR type1 for A=0,B=1,Phi=1 up till Out1 node.

Table 4.2 shows the various capacitances which are charged or discharged during each input case for different schemes in domino OR and static OR. Here the expressions of output capacitance are shown up to the intermediate node (Out1) after that the capacitance will be formed by the inverter which is already discussed in table 4.1. Similarly, in table 4.3 the expressions of the domino AND (type 1 to type 6) and static AND are shown up to the intermediate node (out1). These capacitors contribute to the delay which we will see in the next chapter.

Table 4.2 Output capacitance up till Out1 for OR.

GATE		A=0, B=1,Phi=1and Out1=0	A=0, B=0,Phi=1 and Out1=1
Domino OR	Type 1	$C_{gd1}, C_{bd1}, C_{bd5}, C_{gs3}, C_{gd4}, C_{gd3}$	$C_{gd5}, C_{gd2}, C_{bd2}, C_{bd3}, C_{gd3}$
	Type 2	$C_{gd1}, C_{bd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{bs3}, C_{gs3}, C_{gd4}$ C_{bd4}, C_{gd3}	$C_{gd5}, C_{gd2}, C_{gd3}$
	Type 3	$C_{gd3}, C_{gd1}, C_{bd1}, C_{bd5}, C_{gs3}, C_{gd4}$	$C_{gd5}, C_{gd2}, C_{bd2}, C_{gd3}, C_{bd3}$
	Type 4	$C_{gd1}, C_{bd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{gs3}, C_{bs3}, C_{gd4},$ C_{bd4}, C_{gd3}	$C_{gd5}, C_{gd2}, C_{gd3}$
	Type 5	$C_{gd1}, C_{bd5}, C_{gs3}, C_{gd4}, C_{gd3}$	$C_{bd1}, C_{gd5}, C_{gd2}, C_{bd2}, C_{bd3}, C_{gd3}$,
	Type 6	$C_{gd1}, C_{bd5}, C_{bd2}, C_{bd3}, C_{gs3}, C_{bs3}, C_{gd4},$ C_{bd4}, C_{gd3}	$C_{bd1}, C_{gd5}, C_{gd2}, C_{gd3}$
Static OR		$C_{bd2}, C_{gd4}, C_{gd2}$	$C_{gs2}, C_{gd1}, C_{gd2}, C_{gd3}, C_{bd3}, C_{bd4},$ C_{gd4}

Table 4.3 Output capacitance up till Out1 for AND.

GATE		A=1, B=1, Out1=0	A=1, B=0, Out1=1
Domino AND	Type 1	$C_{gd2}, C_{gs2}, C_{gs3}, C_{gd4}, C_{gd1}, C_{bd1}, C_{bd5},$ C_{gd3}	$C_{bd2}, C_{bs2}, C_{bd3}, C_{gd5}, C_{gd3}$
	Type 2	$C_{bd1}, C_{gd1}, C_{gd2}, C_{bd2}, C_{gs2}, C_{bs2}, C_{bd3}, C_{gs3},$ $C_{bs3}, C_{gd4}, C_{bd4}, C_{bd5}, C_{gd3}$	C_{gd5}, C_{gd3}
	Type 3	$C_{gd2}, C_{gs2}, C_{gd3}, C_{gs3}, C_{gd4}, C_{gd1}, C_{bd1}, C_{bd5},$	$C_{bd2}, C_{bs2}, C_{bd3}, C_{gd5}, C_{gd3}$
	Type 4	$C_{gd1}, C_{bd1}, C_{gd2}, C_{bd2}, C_{gs2}, C_{bs2}, C_{bd3}, C_{gs3},$ $C_{bs3}, C_{gd4}, C_{bd4}, C_{bd5}, C_{gd3}$	C_{gd5}, C_{gd3}
	Type 5	$C_{gd1}, C_{gd2}, C_{gs2}, C_{gs3}, C_{gd4}, C_{bd5}, C_{gd3}$	$C_{bd1}, C_{bd2}, C_{bs2}, C_{bd3}, C_{gd5}, C_{gd3}$,

	Type 6	$C_{gd1}, C_{gd2}, C_{bd2}, C_{gs2}, C_{bs2}, C_{bd3}, C_{gs3}, C_{bs3}, C_{gd4}, C_{bd4}, C_{bd5}, C_{gd3}$	$C_{bd1}, C_{gd5}, C_{gd3}$
Static AND		$C_{gd1}, C_{bd1}, C_{gd3}, C_{gs3}, C_{gd4}, C_{gd2}, C_{bd2}$	$C_{gd2}, C_{bd3}, C_{bs3}, C_{bd4}, C_{gd4}$

4.3 Miller Capacitance

Miller capacitance is due to the miller effect which says, there is a change in the equivalent capacitance of the input terminal and output terminal of a inverting amplifier due to capacitance formed between input and output terminals. The capacitance formed between input terminal (Gate) and output terminal (Drain) is C_{gd}.

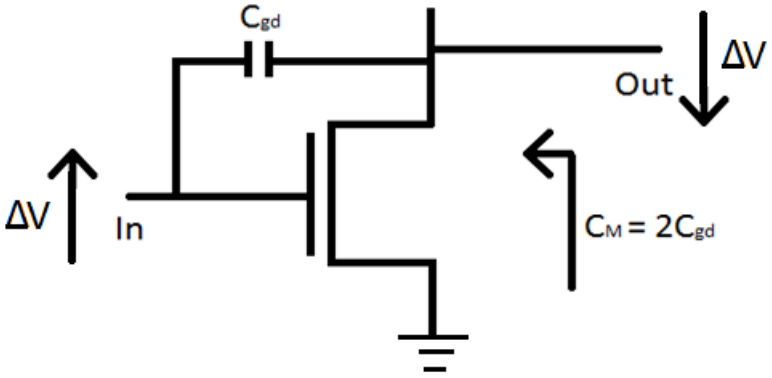


Fig 4.6 Miller capacitance in NMOS

Due to inverting nature of circuit, the input and output are out of phase by 180°. So, when input rises, output falls and vice versa. Due to this the miller effect comes in and the capacitance formed at the output side is doubled i.e. $2C_{gd}$. This effect has been explained by figure 4.6 in which the output capacitance has been doubled.

4.4 Capacitance during rise time and fall time

During rise time(10% to 90% output) calculations, all the capacitances (both Out1=0 & 1) are to be considered and during fall time calculations, only capacitances which were charged during previous case and also connected to output are to be considered. These observations are quiet obvious as during transition of output, neither it is complete logic 1 or logic 0 so we have to take the effect of both the cases during rise time. But when

output node is falling, the capacitances charged during previous case(when out=1) are to be discharged.

Moreover, some of the capacitances are connected with the nodes which don't get full output swing (i.e. their node potential is less than V_{DD}) so, equivalent capacitance on that node will be lesser than these values. Let us assume V_n is the node voltage of a node n and capacitances connected with this node n are C_{n1}, $C_{n2}$and C_{n3}.

$$C_{Total_n} = \frac{V_n}{V_{DD}}(C_{n1} + C_{n2} + C_{n3}) \qquad (4.9)$$

In the following table 4.4 and table 4.5, the value of total output capacitance in fF has been shown for the rise time and the fall time. In table 4.4 the output capacitance is shown for the OR gate up to the intermediate node Out1. Considering the rise time, the maximum capacitance is in the domino OR type5 and for the fall time the maximum capacitance is also for domino OR type5. But if table 4.5 is considered the maximum capacitance for rise time case is in domino AND type4 and for the fall time is in domino AND type5.

Table 4.4 Total capacitance values of OR gate up to Out1.

GATE		Total Capacitance during rise time (fF)	Total Capacitance during fall time (fF)
Domino OR	Type 1	1.5156	1.4060
	Type 2	1.6	1.09167
	Type 3	1.515	1.40607
	Type 4	1.6	1.09
	Type 5	1.978	1.433
	Type 6	1.593	1.1189
Static OR		0.472	0.36

Table 4.5 Total capacitance values of AND gate up to Out1.

GATE		Total Capacitance during rise time (fF)	Total Capacitance during fall time (fF)
Domino AND	Type 1	1.60472	0.68775
	Type 2	1.6892	0.86067
	Type 3	1.6177	0.983
	Type 4	1.6947	0.86067
	Type 5	1.611	1.0103
	Type 6	1.688	0.8879
Static AND		0.9634	0.68

Chapter 5

Resistance in Subthreshold Regime

The resistance is the opposition of the passage of the current through the conductor. If we take the case of NMOS or PMOS, the resistance we take is the opposition offered by the channel formed between drain and source terminals. This resistance is different in different regions. The resistance we generally talk about is either in linear region or the saturation region but here we will be concentrating on resistance offered in subthreshold or weak inversion region.

In subthreshold region, the resistance plays a very critical role. As according to the basic definition of resistance

$$R = V / I \qquad (5.1)$$

The order of the voltage is few milli volts and of the current is few nano amperes But this current change drastically with a little increase of voltage. So, the resistance increases drastically with the current. This resistance offered by NMOS or PMOS is being very critical in calculation of RC delay.

5.1 Average Resistance

As discussed earlier the magnitude of current changes drastically with a little change of voltage. So, the instantaneous resistance may vary from few killo ohms to several mega ohms. Moreover, calculating resistance at each value of voltage will be a tedious and time consuming process so average resistance should be calculated across the whole range of voltage. This approximation of resistance should be made and should accurately predict the actual value of it.

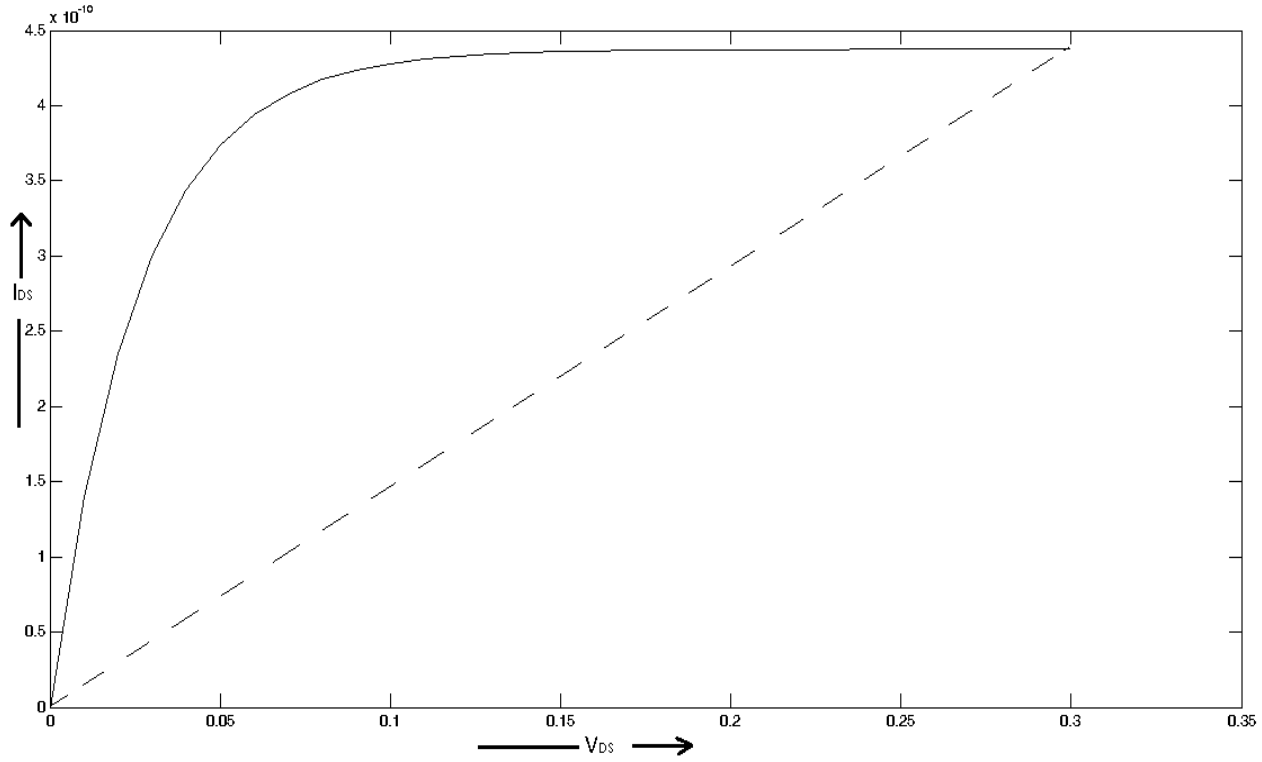


Fig 5.1 Average resistance in subthreshold region

In figure 5.1, the dotted line has been shown. This slope represents the average resistance (1/Slope) from 0 to V_{DD} which can be calculated as follows

$$R = \frac{\Delta V_{DS}}{\Delta I} \tag{5.2}$$

Here, V_{DS} changes from 0 to V_{DD} and ΔI from I(V_{DD}) to I(0). So, finally we get

$$R = \frac{V_{DS}}{\mu \frac{W}{L} \sqrt{\frac{q\epsilon_{si}(NDEP)}{2\varphi_s}} V_t{}^2 \left[1 - e^{-V_{ds}/V_t}\right] e^{\left((V_{gs} - V_{th} - V'_{off})/nV_t\right)}} \tag{5.3}$$

By putting values from PTM BSIM model 4.0, the practical value of average resistance comes out to be $1.388 * 10^5 \Omega$ for NMOS of 101nm/32nm and PMOS of 48nm/32nm. This value is very obvious as the V_{DS} is of the order of a few millivolts and the current is of the order of a few nano Amperes.

This value of average resistance is same for NMOS with an aspect ratio of 101nm/32nm and PMOS with an aspect ratio of 48nm/32nm because we have designed this for symmetric inverter in equation 3.6.

$$(W/L)_n = 2.1\ (W/L)_p$$

For all the other circuits whose dimensions are different from these, the resistance can be easily calculated by following method

For NMOS,

$$R_{new} = 1.388 * 10^5 \left(\frac{101/32}{(W/L)_{new}}\right) \quad (5.4)$$

For PMOS,

$$R_{new} = 1.388 * 10^5 \left(\frac{48/32}{(W/L)_{new}}\right) \quad (5.5)$$

Chapter 6

Results and Discussions

Predictive Technology Model [33](PTM) has been used for simulations at 32nm technology node. A rectangular pulse of 0.1 GHz with rise time and fall time of 0.5ns has been used as an input pulse with a load of 1fF. This load capacitance is calculated for the FO4 for the inverter. The SPICE simulations are performed with a supply voltage of 0.3V using tool tanner EDA 12.5.

90% propagation delay approach is used. Average delay is defined as average of rise time and fall time. For inverter, Rise time is defined as "Time interval between 10% input & 90% output" and fall time is defined as "Time interval between 90% input & 10% output." For other circuits (AND/OR), Rise time is defined as "Time interval between 90% input & 90% output" and Fall time is defined as "Time interval between 10% input & 10% output".

6.1 Total delay calculation

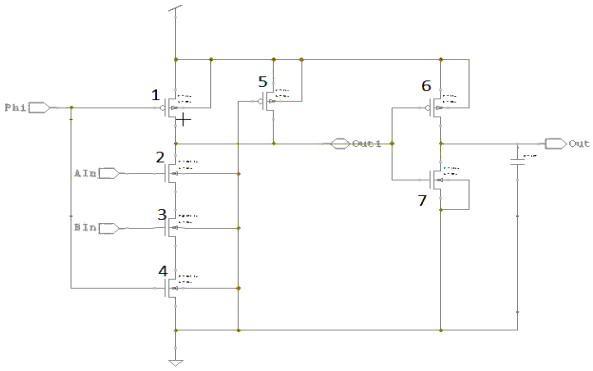
As the OR and AND circuits are cascaded structures. They have NOR and NAND gate respectively followed by the inverter. So, theoretical RC delay up to intermediate node (before inverter) is being calculated and then the pulse of this delay acts as a input to the inverter. Total delay is being calculated by the root mean square value of the inverter delay (calculated separately for inverter) and the delay offered by the NOR/NAND circuits.

$$TotalRCDelay = \sqrt{(Avg.Inverterdelay)^2 + (Avg.DelayuptoOut1)^2} \qquad (6.1)$$

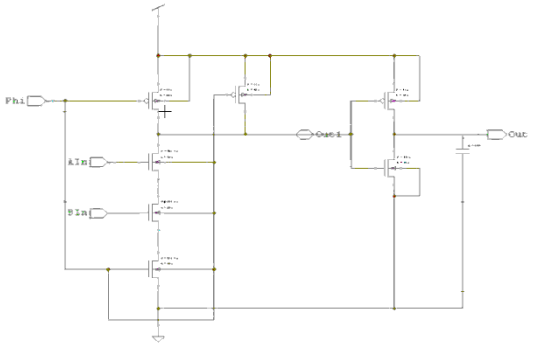
The 90% RC delay defined earlier has been calculated and found out to be 2.2 RC. These values for different circuits will be calculated and then compared with the simulated values in tanner EDA 12.5.

6.2 Theoretical and Simulated Results

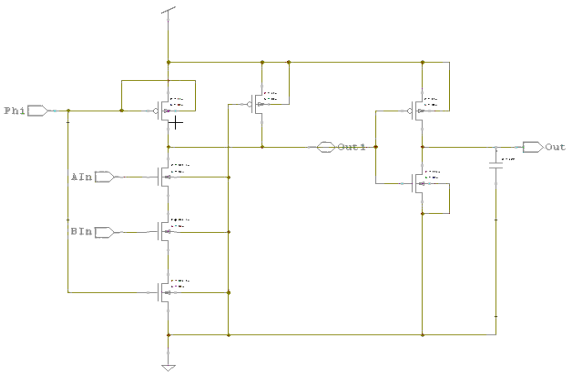
In figure 6.1, the circuits has been shown for domino AND type1 to type6. Delay up to intermediate node (Out1) has been calculated theoretically by calculating the average resistance and total capacitance (as explained earlier).



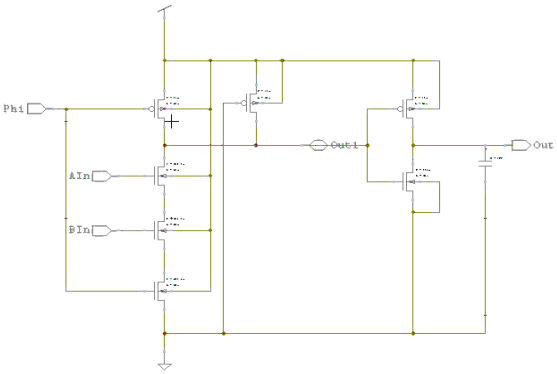
Type 1



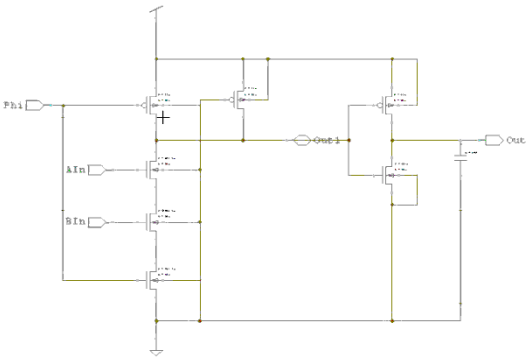
Type 2



Type 3



Type 4



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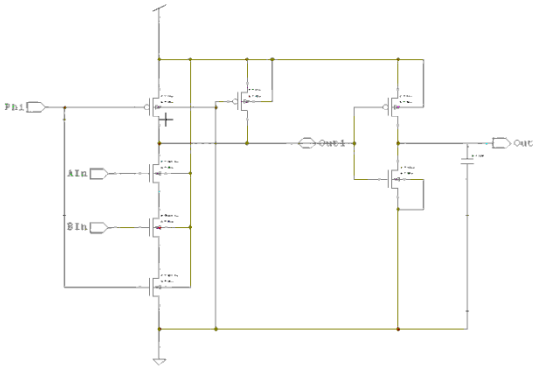
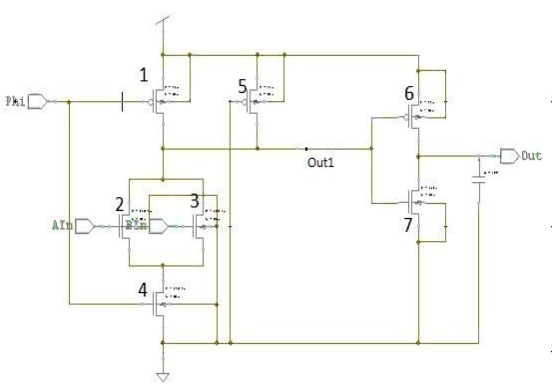
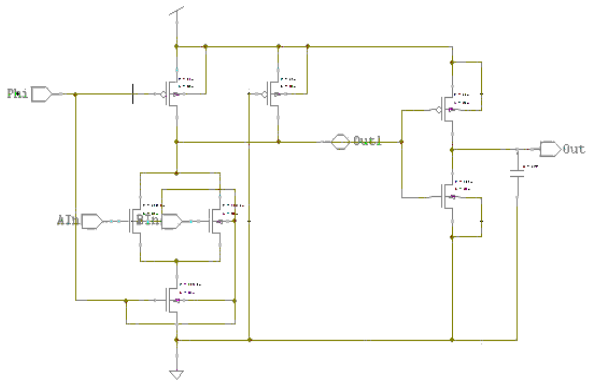


Type 6

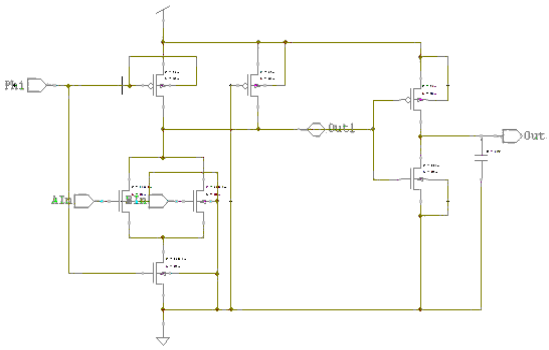
Fig 6.1 Domino AND type1to type6.



Type 1



Type 2



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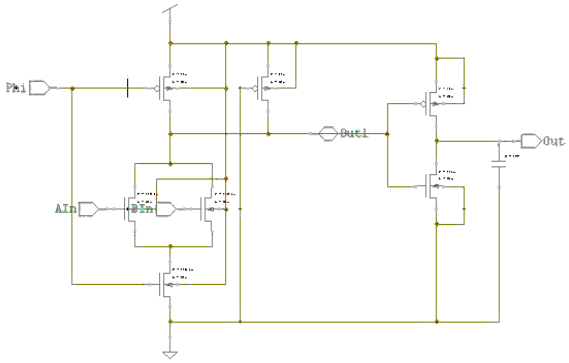

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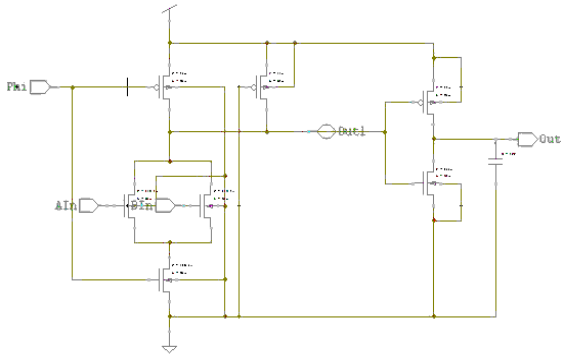
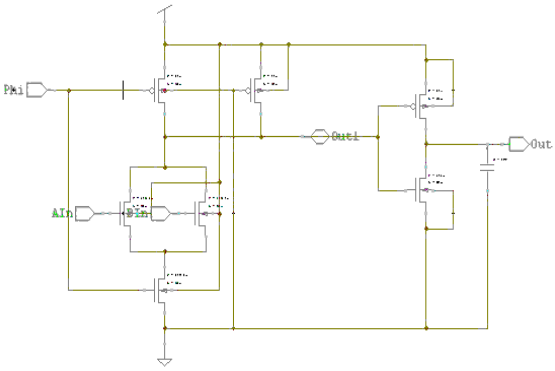


Type 5



Type 6

Fig 6.2 Domino OR type1 to type6.

Figure 6.2 shows the domino OR type1 to type6. Table 6.1 shows calculated the rise time, fall time and the average delay for all the circuits up till intermediate node Out1. From this table we can infer that minimum average delay is for the domino AND type1 and for domino OR it is minimum for type4. This is due to the fact that output capacitance is

minimum in these cases which reduces the overall average delay of the circuit up to intermediate node Out1.

Table 6.1 Calculated delays up to Out1.

GATE		Rise time (ps)	Fall time (ps)	Average Delay
Static AND		294.18	207.65	250.92
Static OR		288.26	120.92	204.59
Domino AND	Type 1	490.01	105.00	297.51
	Type 2	515.81	131.41	323.61
	Type 3	493.98	150.08	322.03
	Type 4	517.49	131.41	324.45
	Type 5	491.93	154.25	323.09
	Type 6	515.45	135.56	325.51
Domino OR	Type 1	462.81	214.68	338.74
	Type 2	488.58	166.68	327.64
	Type 3	462.62	214.68	338.65
	Type 4	488.57	166.68	327.62
	Type 5	604.01	218.79	411.40
	Type 6	486.44	170.83	328.64

Table 6.2 Calculated delay of Inverter with load of 1fF.

GATE	Rise time (ps)	Fall time (ps)	Average Delay
Inverter	400.73	394.93	397.83

In table 6.2, the rise time and the fall time of an inverter are shown for a load of 1fF. Average delay is calculated from this rise time and fall time. By using the equation 6.1, the total delay of the circuits are being calculated and is shown in table 6.3.

Table 6.3 Simulated and calculated values of delay.

GATE		Theoretical RC Delay (ps)	Simulated RC Delay (ps)	Theoretical Normalized Delay	Simulated Normalized Delay	Total Power (nW)	PDP (10^{-18}Ws)
Inverter		397.83	436.59	1	1	10.75	4.691
Static AND		470.35	473.11	1	1	21.39	10.118
Static OR		447.35	460.65	1	1	14.81	6.822
Domino AND	Type 1	496.77	570.42	1.056	1.2056	115.63	65.958
	Type 2	512.83	525.77	1.0903	1.111	117.99	62.036
	Type 3	511.83	561.73	1.088	1.187	115.02	64.610
	Type 4	509.45	528.54	1.083	1.117	121.70	64.323
	Type 5	512.32	568.09	1.093	1.20	115.79	65.779
	Type 6	514.03	517.51	1.092	1.094	121.87	63.069
Domino OR	Type 1	522.51	544.04	1.168	1.181	113.49	61.743
	Type 2	515.37	504.61	1.152	1.095	114.92	57.989
	Type 3	522.45	547.32	1.168	1.188	112.92	61.803
	Type 4	515.36	498.05	1.152	1.081	119.62	59.577
	Type 5	572.29	547.03	1.279	1.188	113.65	62.169
	Type 6	516.02	503.57	1.154	1.093	119.80	60.328

The table 6.3 shows the simulated and the calculated values of delay for all the circuits with the power consumed in each case. Based on the Power Delay Product (PDP), the analysis is done. In case of domino AND, type 2 has least PDP but if we consider the delay then type 1 has minimum theoretical delay. If we consider domino OR, then type 2 is best on considering PDP and type 4 is best when delay is considered.

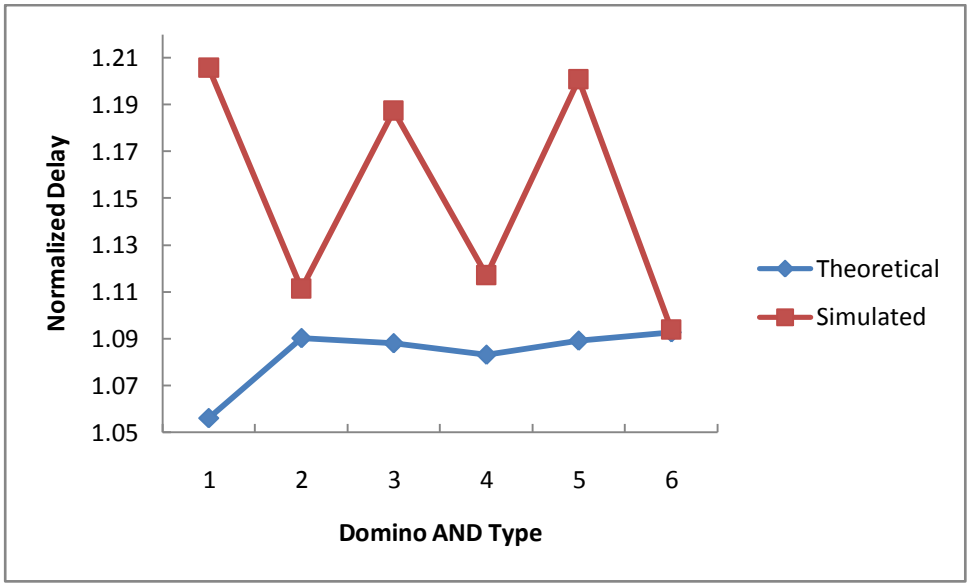


Fig 6.3 Theoretical & simulated normalized delay for different domino AND types.

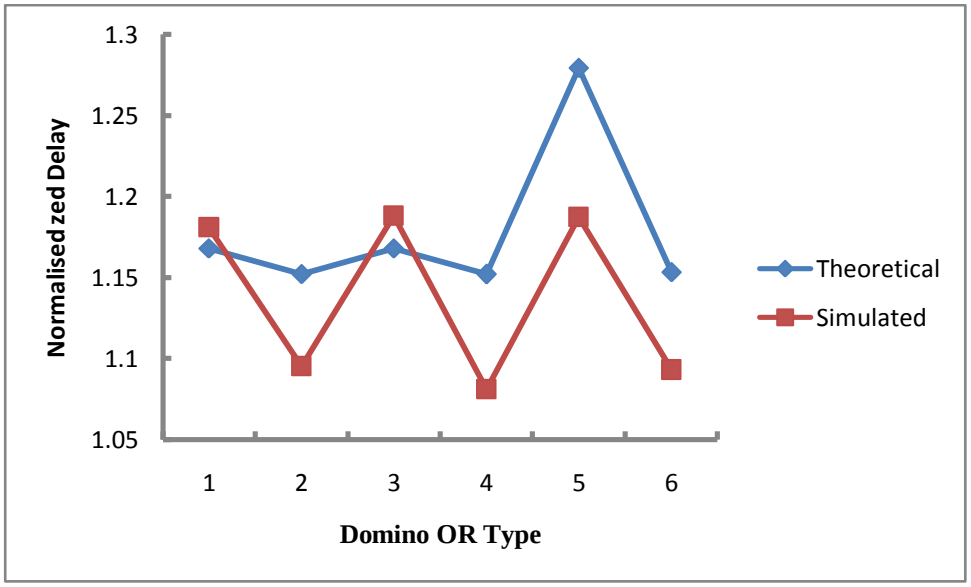


Fig 6.4 Theoretical & simulated normalized delay for different domino OR types.

Figure 6.3 and figure 6.4 shows the normalized delay for Domino AND and domino OR respectively. The average delay is normalized by their respective value of average delay of their static counter parts. It is clear from these figures that type 1 is best if we consider theoretical delay for domino AND. In case of domino OR, type 4 has least theoretical delay which is being verified by the simulations. This is due to the fact that the output capacitance in type 4 is minimum from all the types of domino OR and from domino AND circuits, type 1 has minimum value of the output capacitance.

6.3 Rise time and fall time simulations

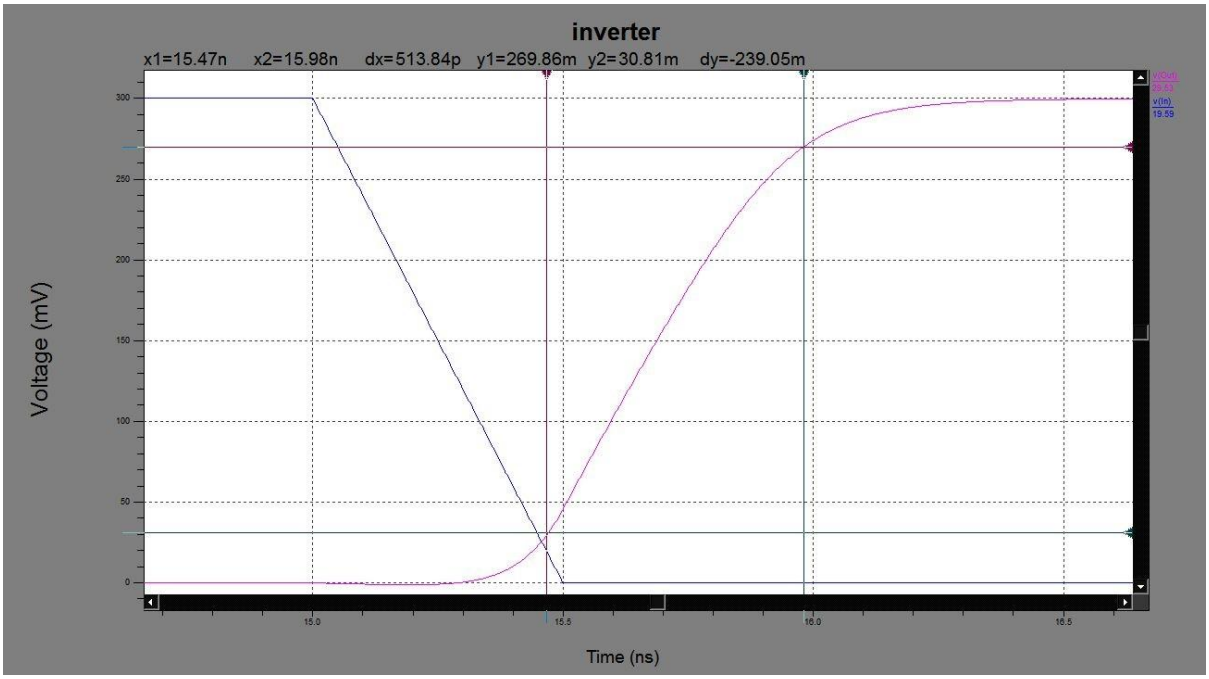


Fig 6.5 Rise time of an inverter with a load of 1fF.

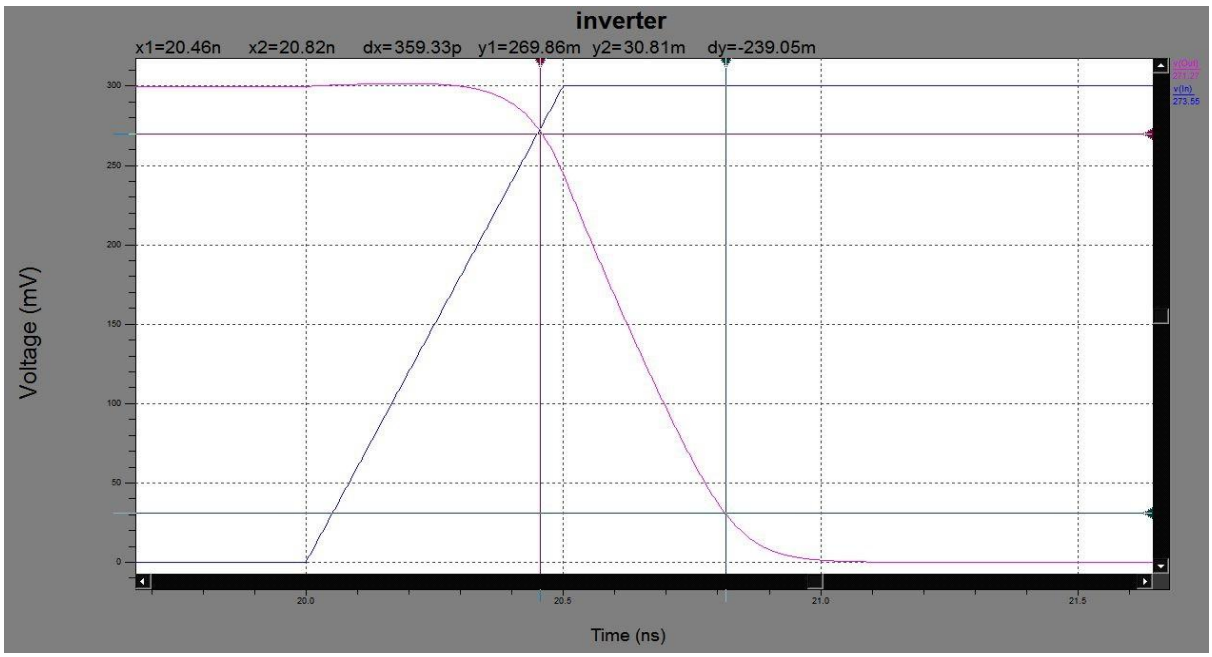


Fig 6.6 Fall time of an inverter with a load of 1fF.

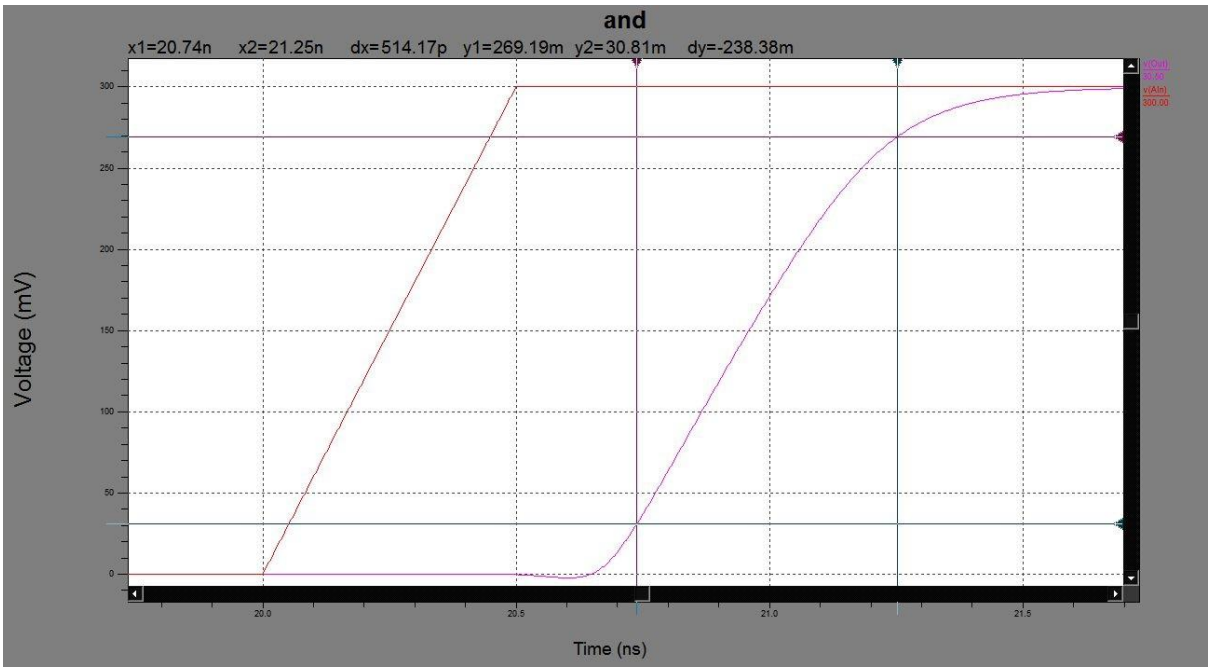


Fig 6.7 Rise time of static AND.

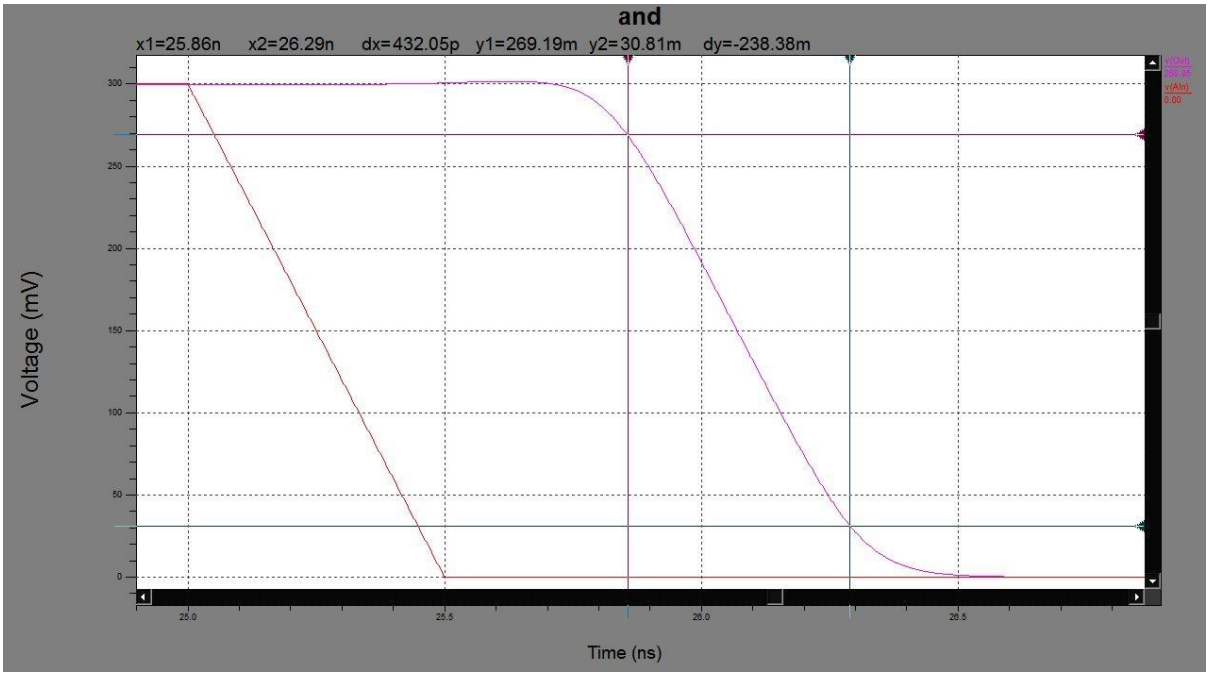


Fig 6.8 Fall time of static AND.

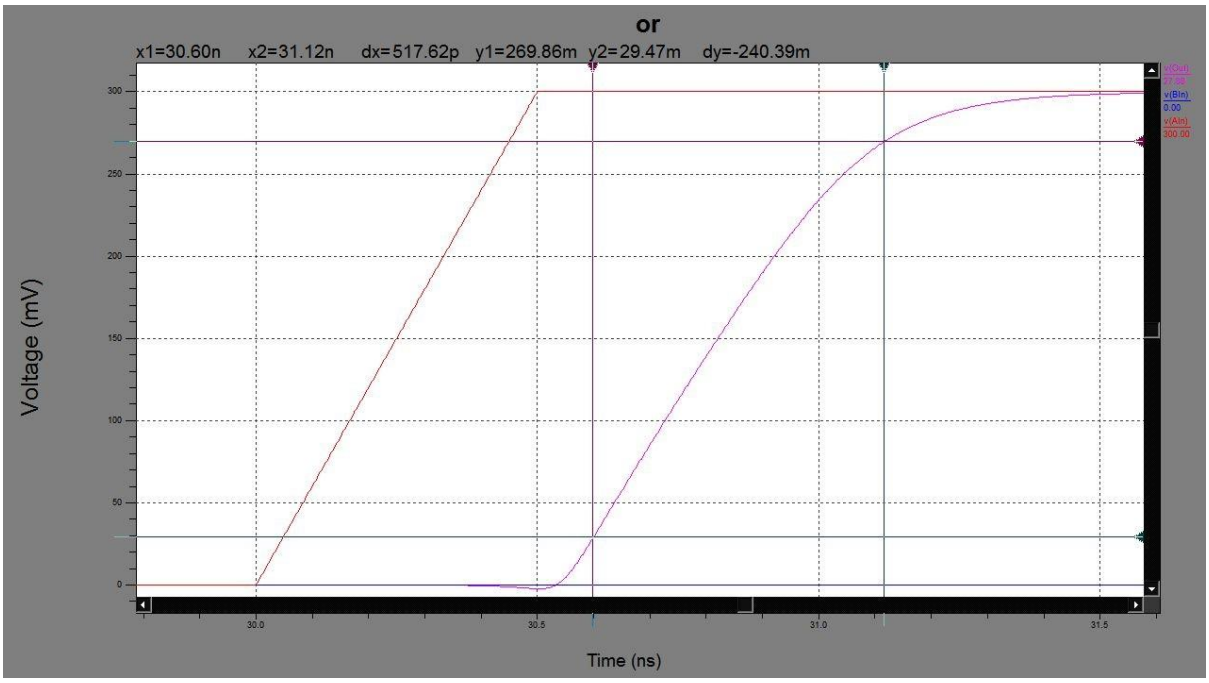


Fig 6.9 Rise time of static OR.

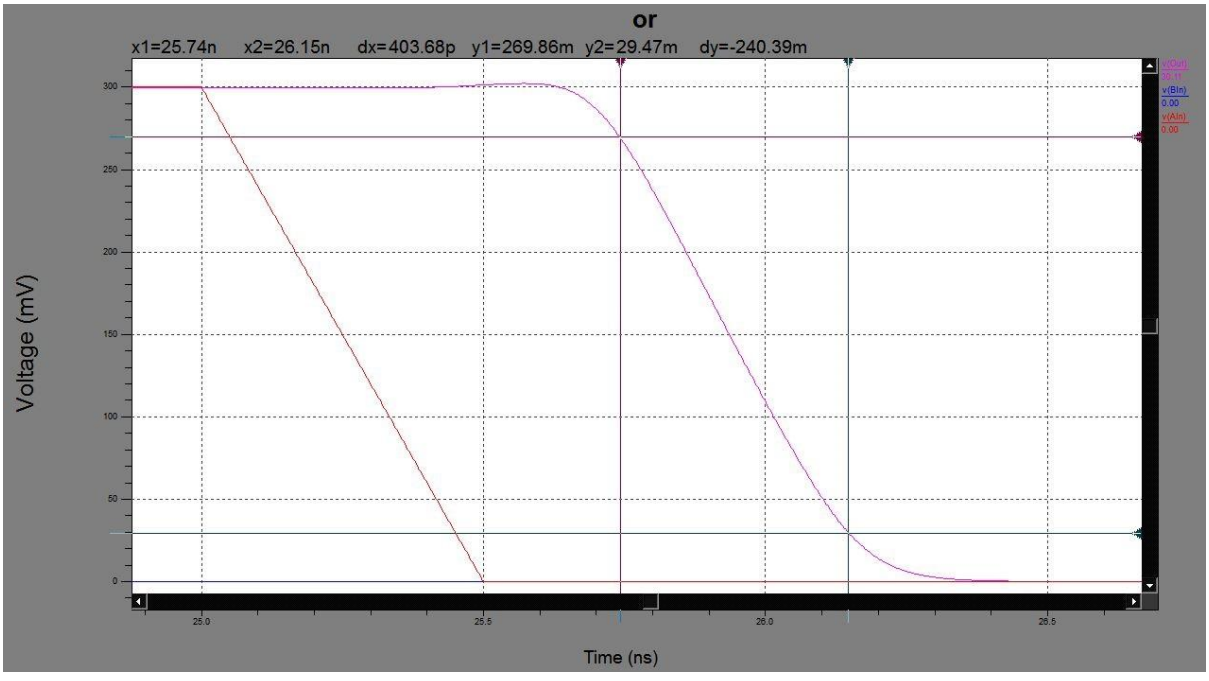


Fig 6.10 Fall time of static OR.

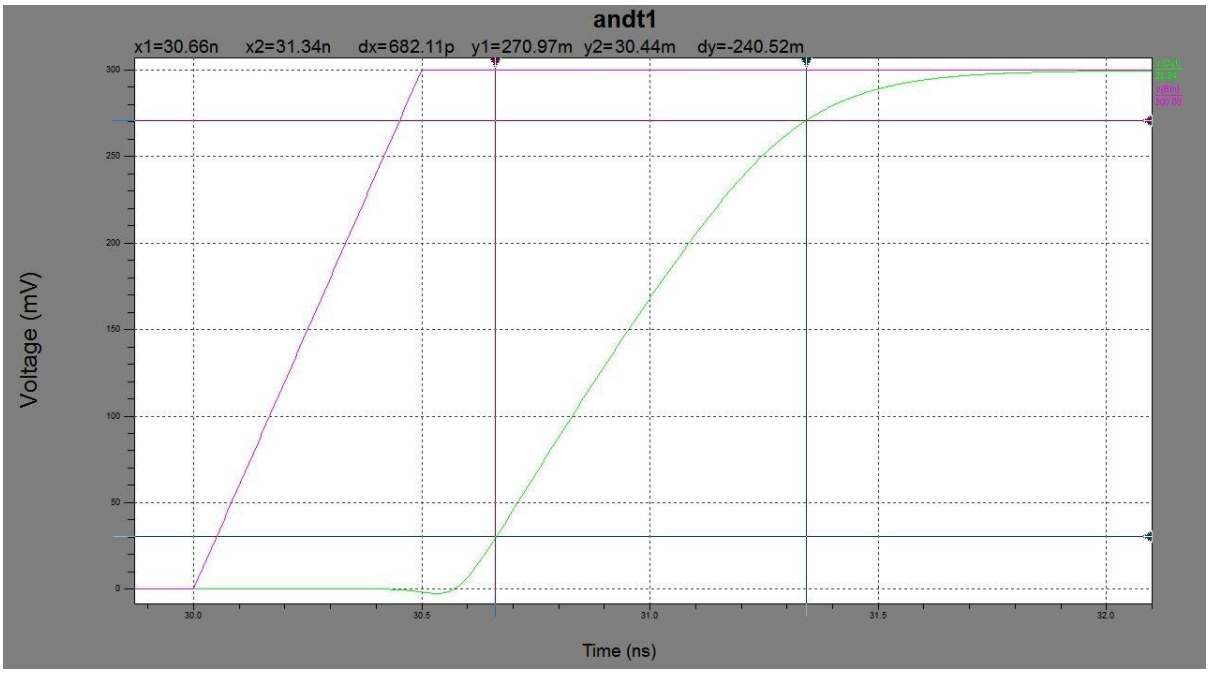


Fig 6.11 Rise time of domino AND type 1.

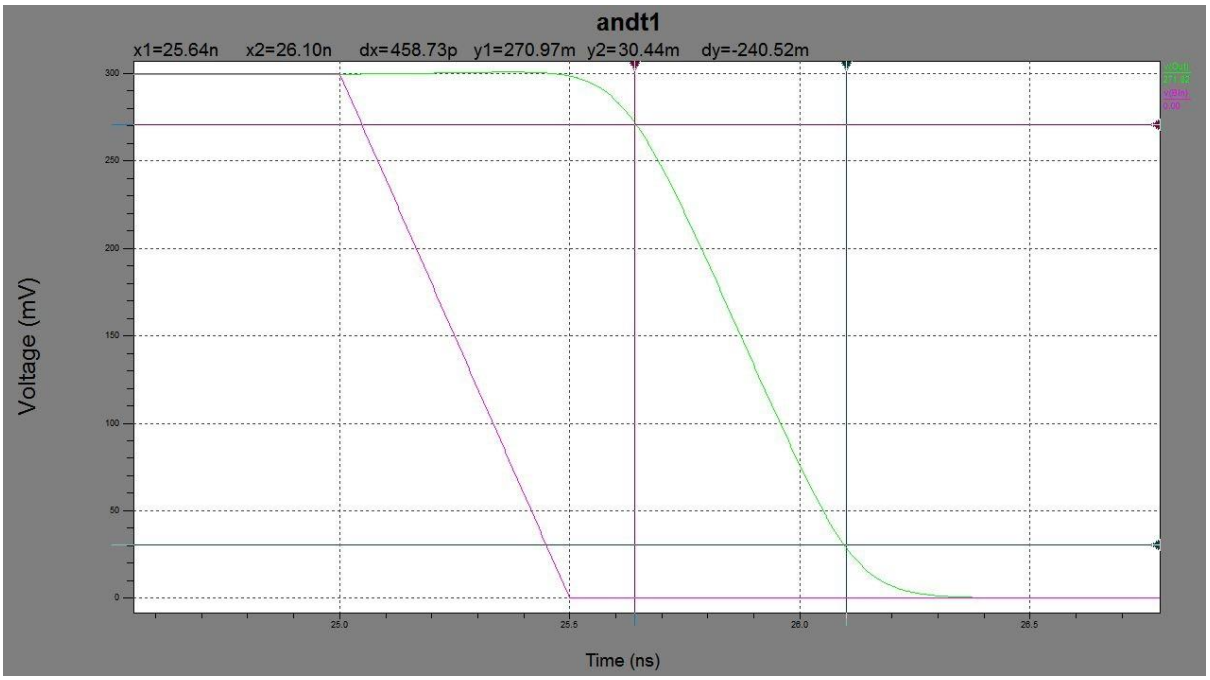


Fig 6.12 Fall time of domino AND type 1.

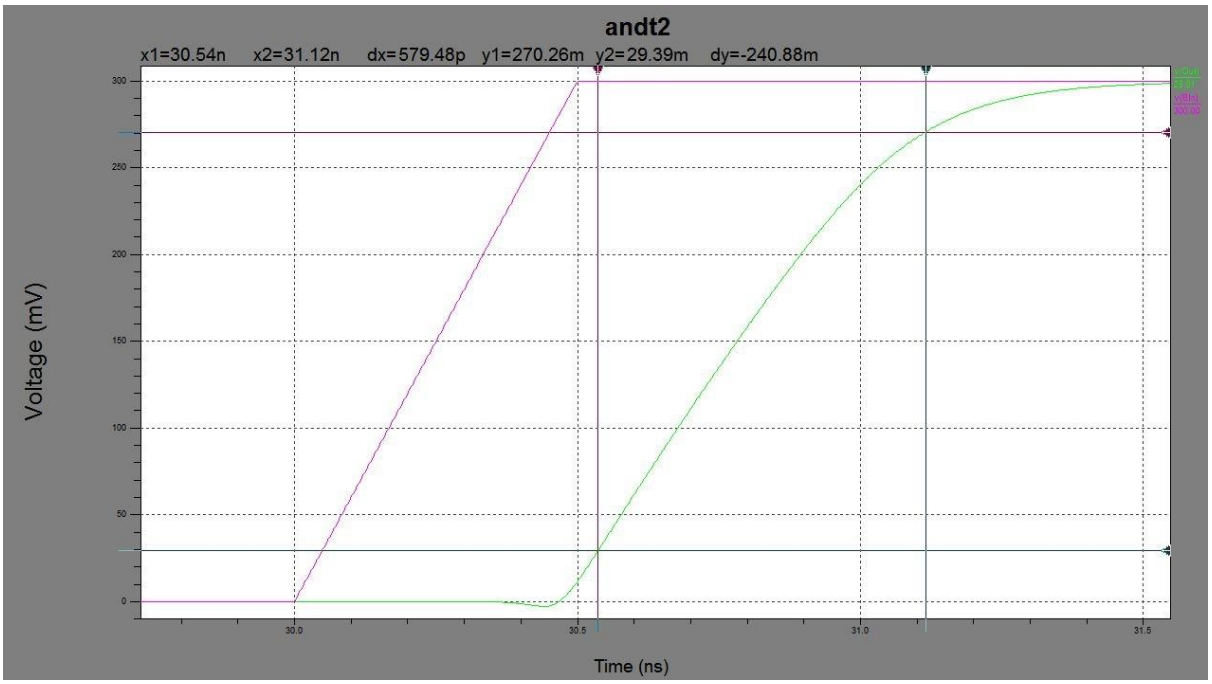


Fig 6.13 Rise time of domino AND type 2.

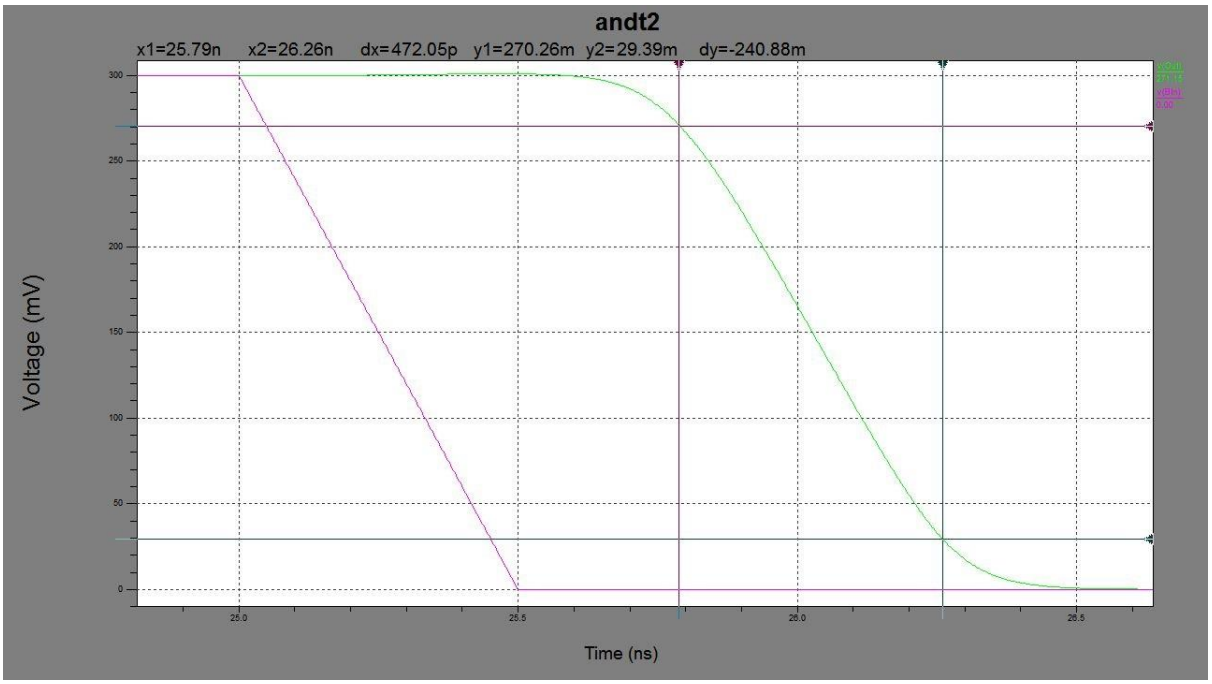


Fig 6.14 Fall time of domino AND type 2.

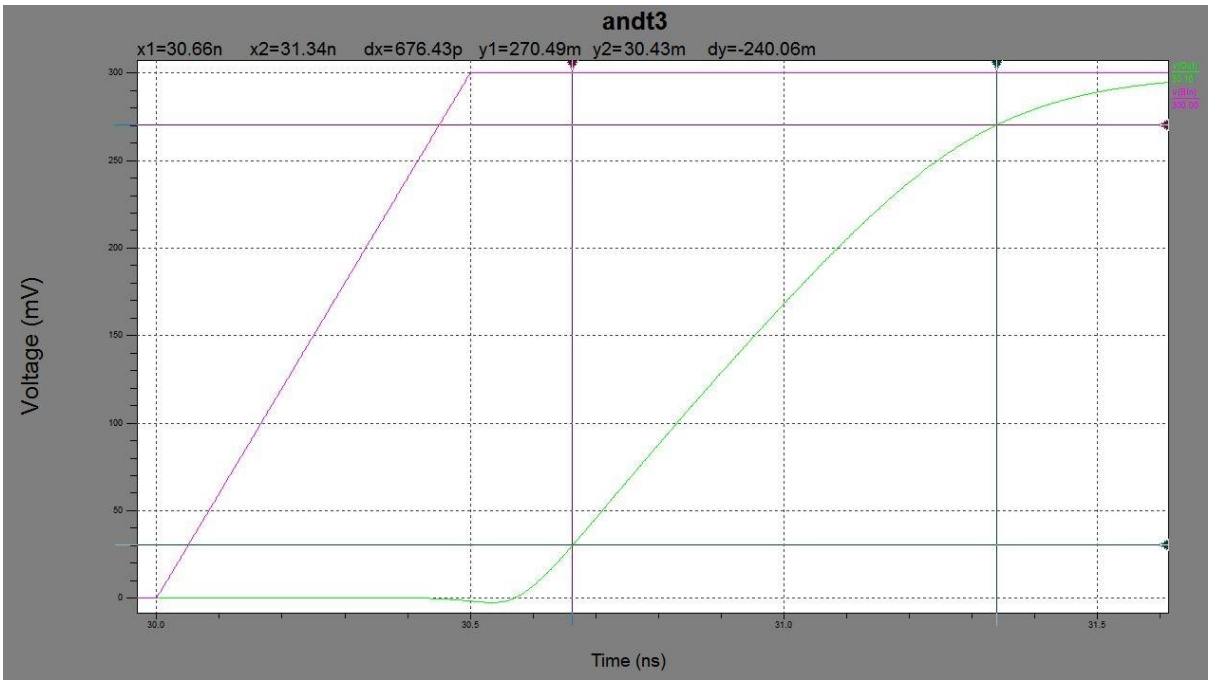


Fig 6.15 Rise time domino AND type 3.

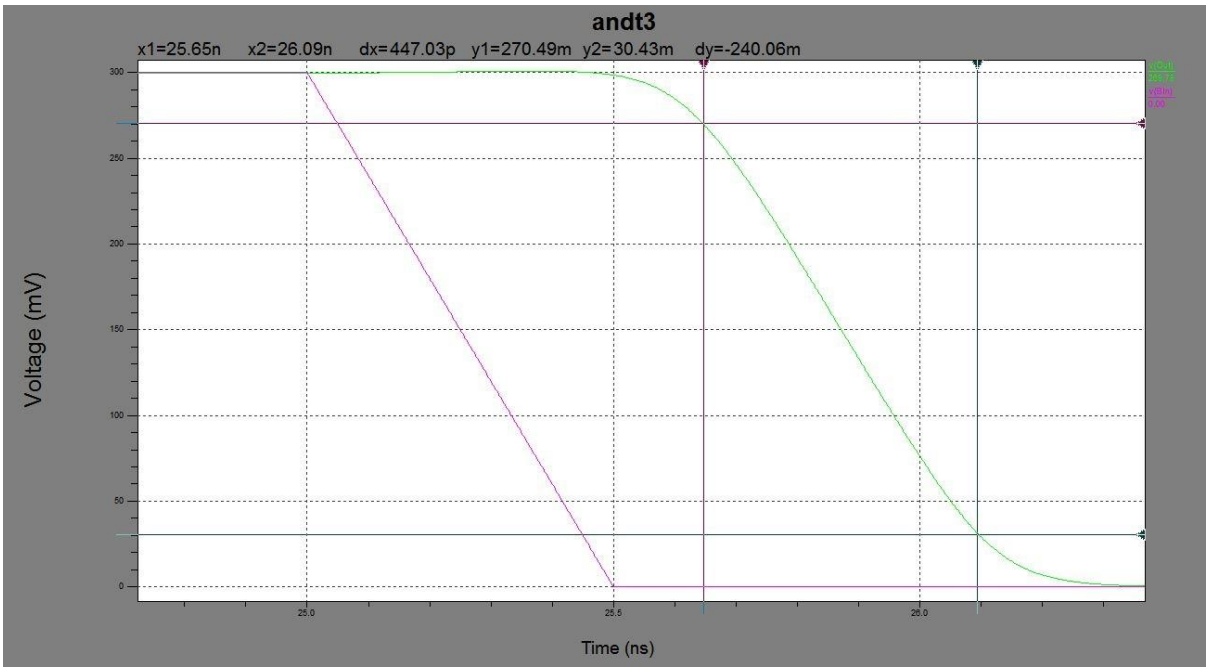


Fig 6.16 Fall time of domino AND type 3.

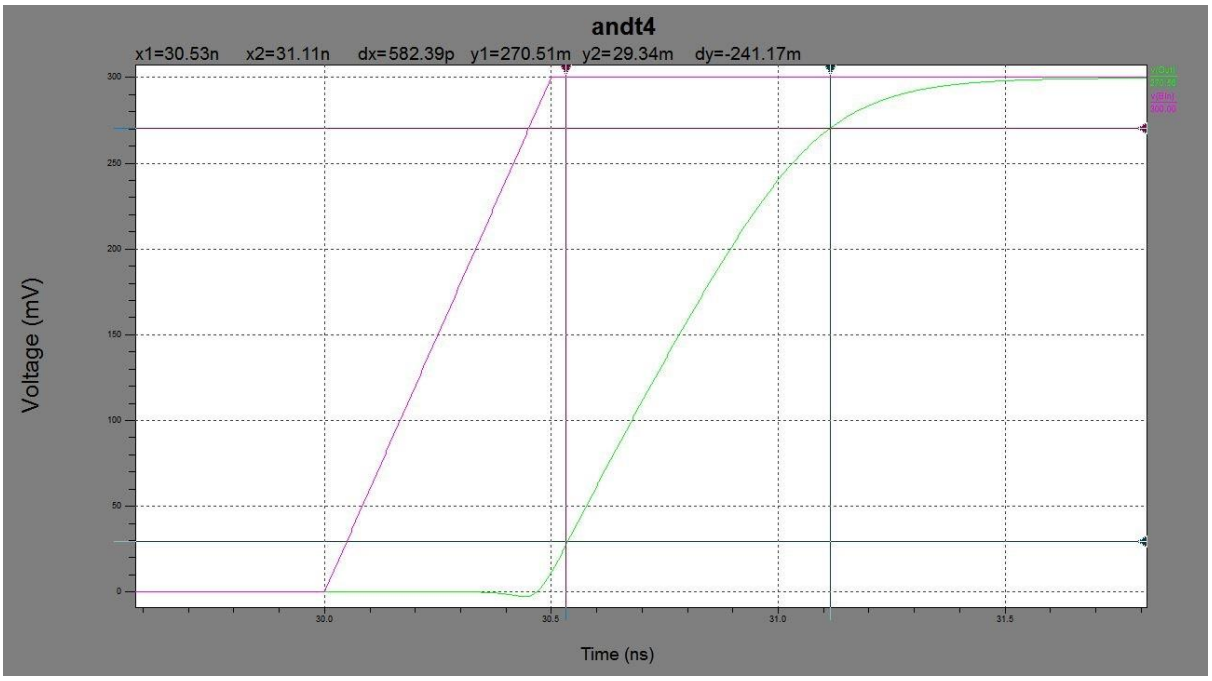


Fig 6.17 Rise time of domino AND type 4.

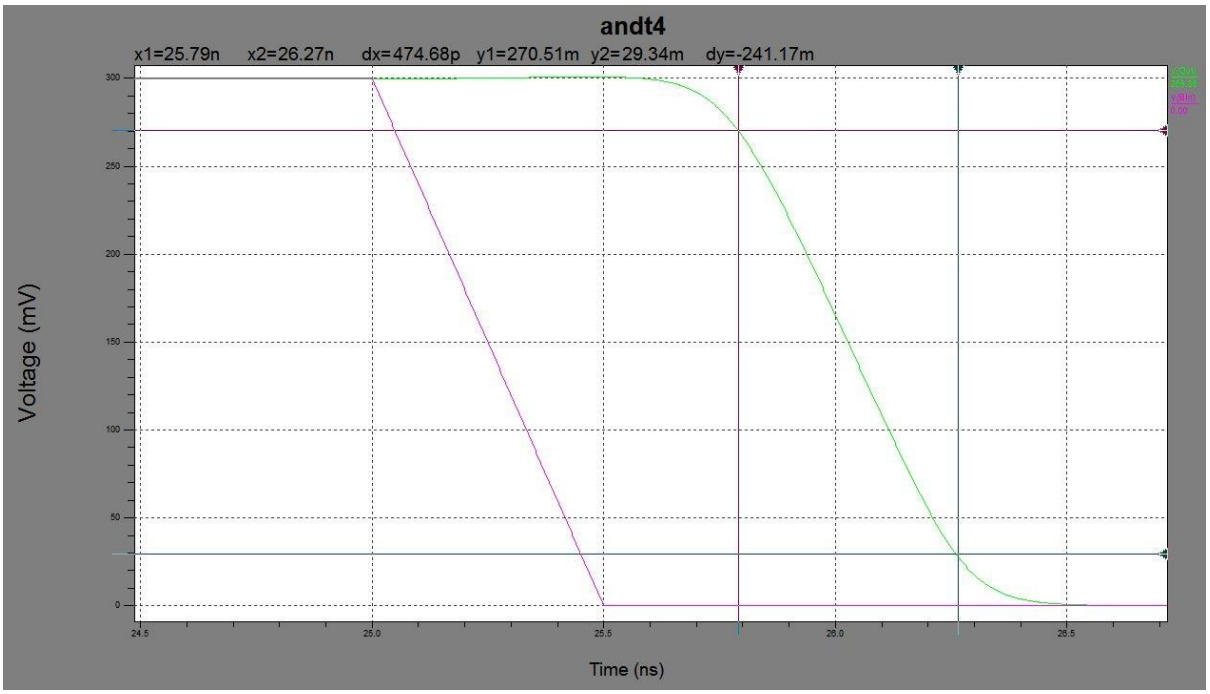


Fig 6.18 Fall time of domino AND type 4.

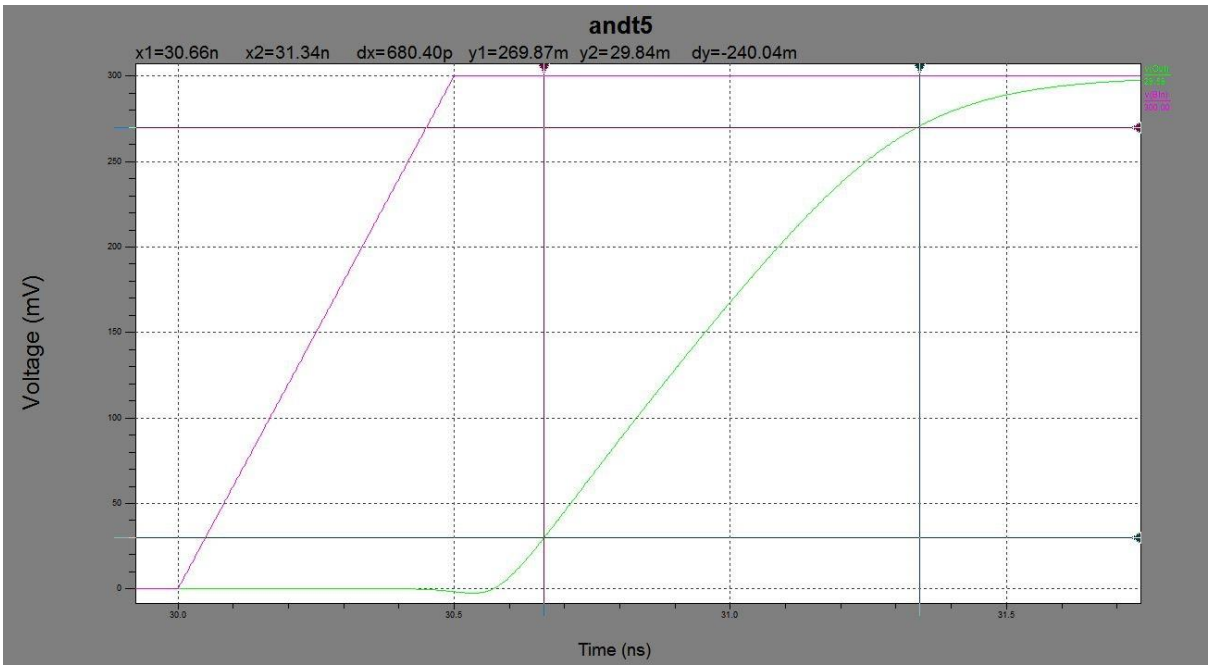


Fig 6.19 Rise time of domino AND type 5.

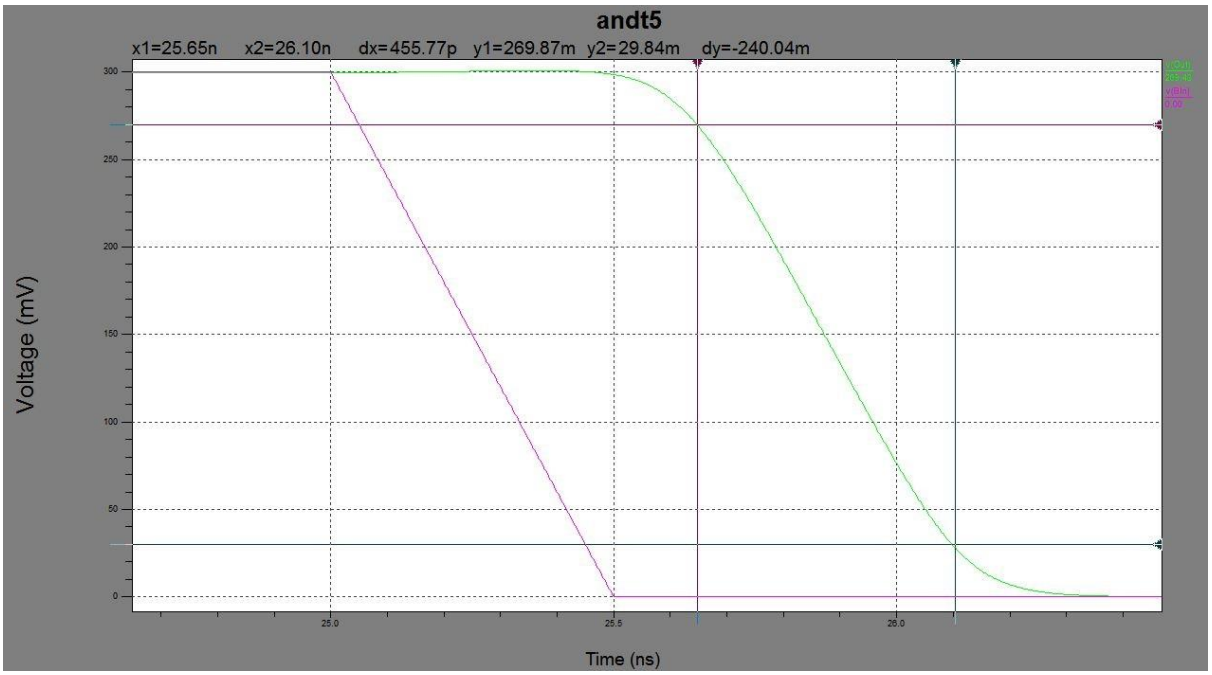


Fig 6.20 Fall time of domino AND type 5.

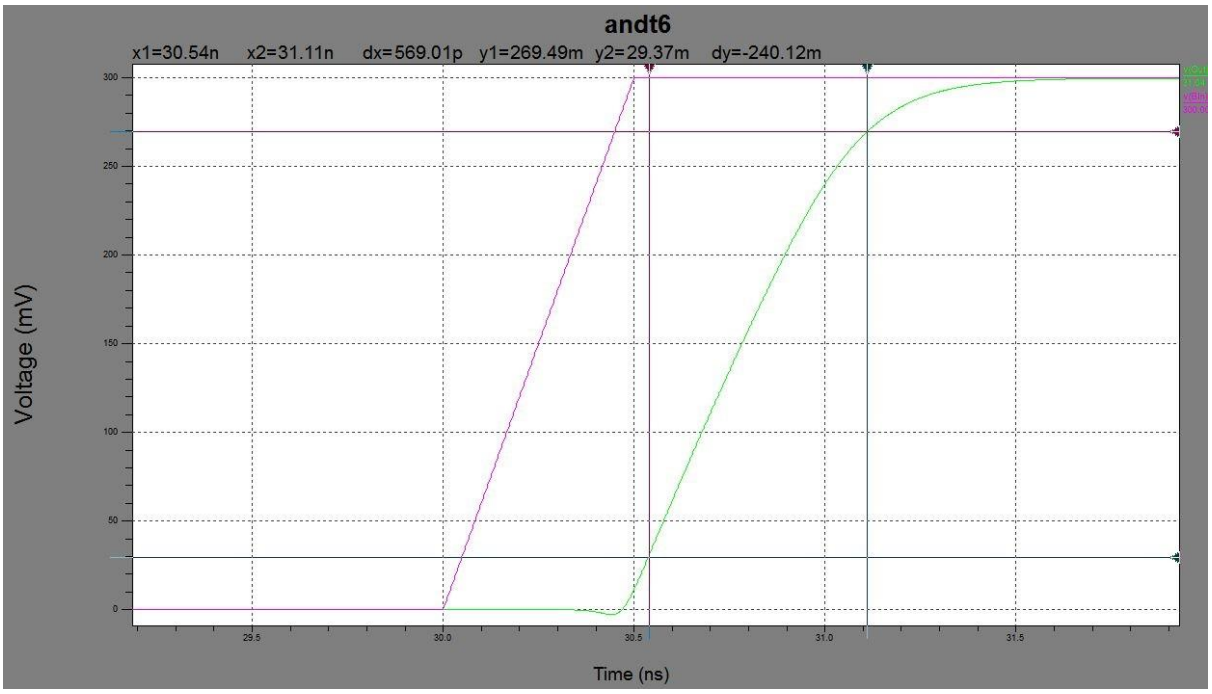


Fig 6.21 Rise time of domino AND type 6.

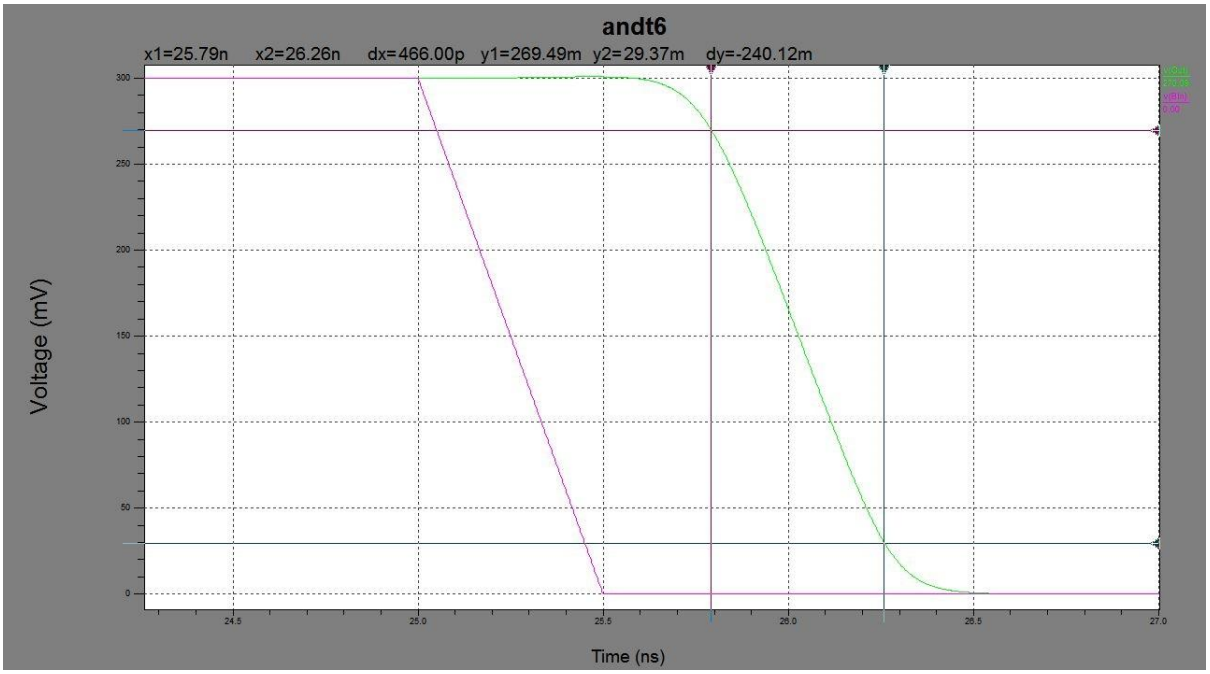


Fig 6.22 Fall time of domino AND type 6.

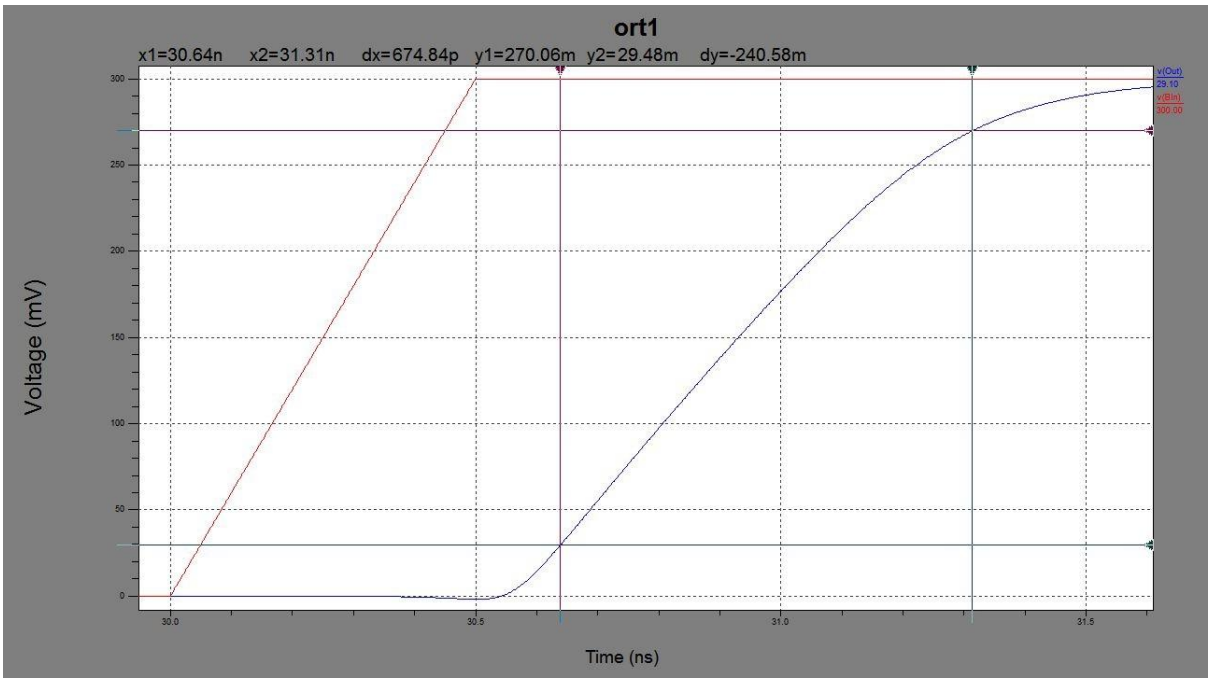


Fig 6.23 Rise time of domino OR type 1.

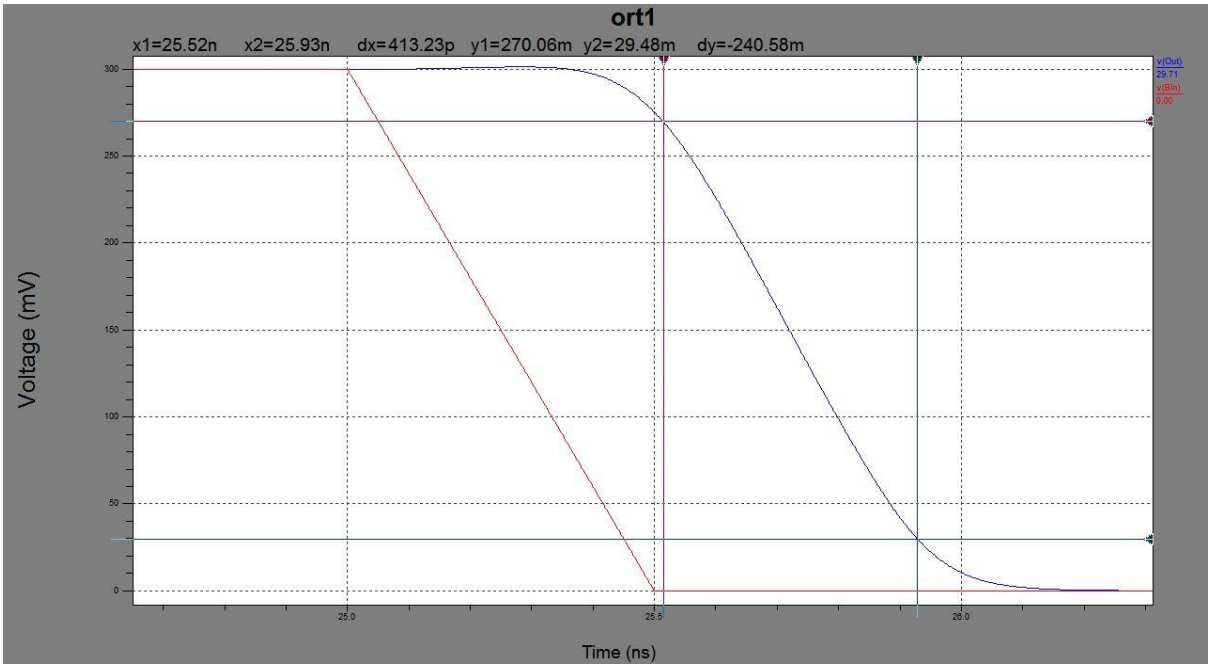


Fig 6.24 Fall time of domino OR type 1.

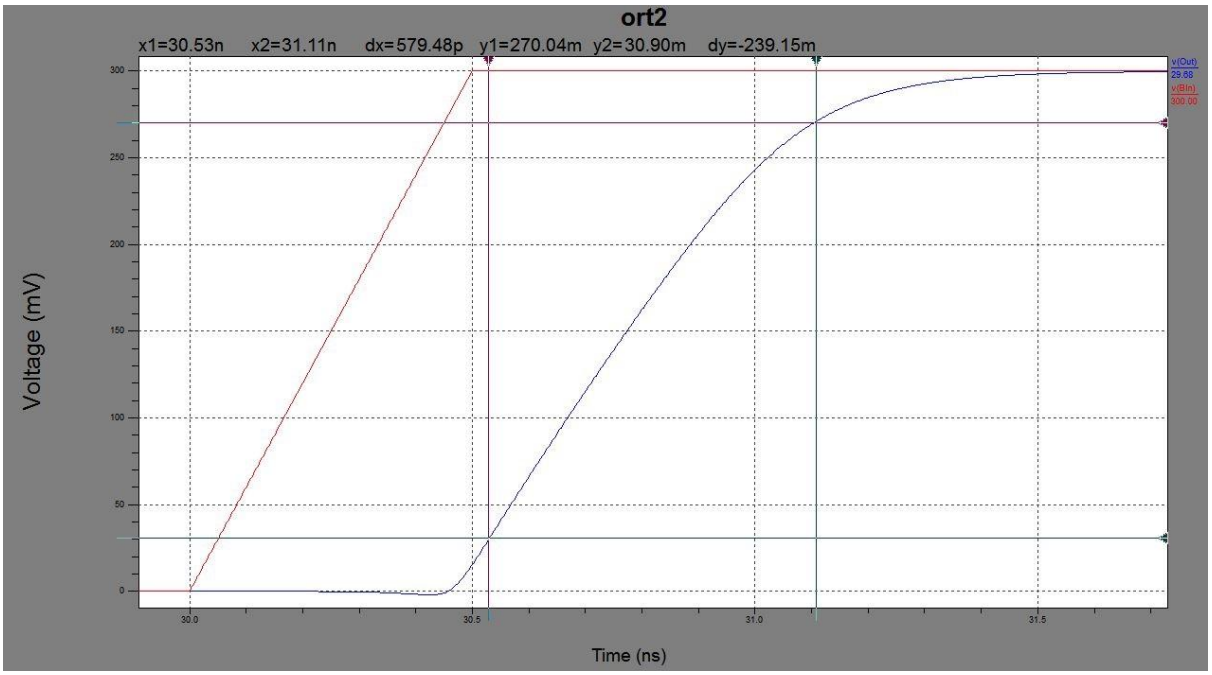


Fig 6.25 Rise time of domino OR type 2.

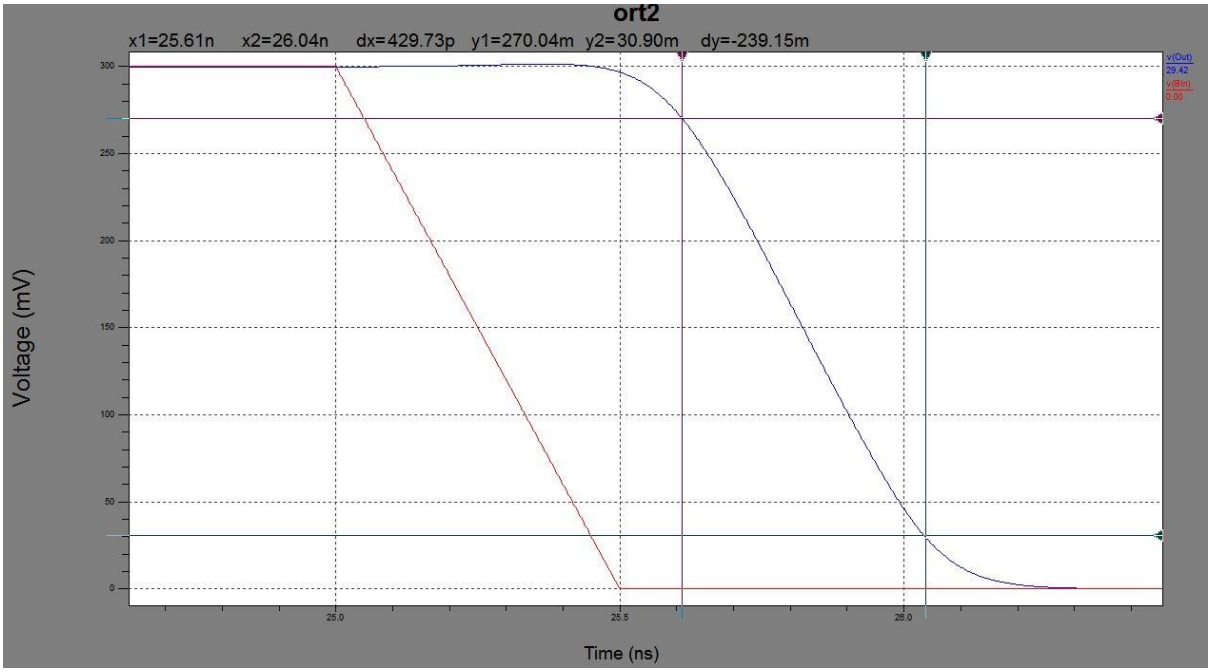


Fig 6.26 Fall time of domino OR type 2.

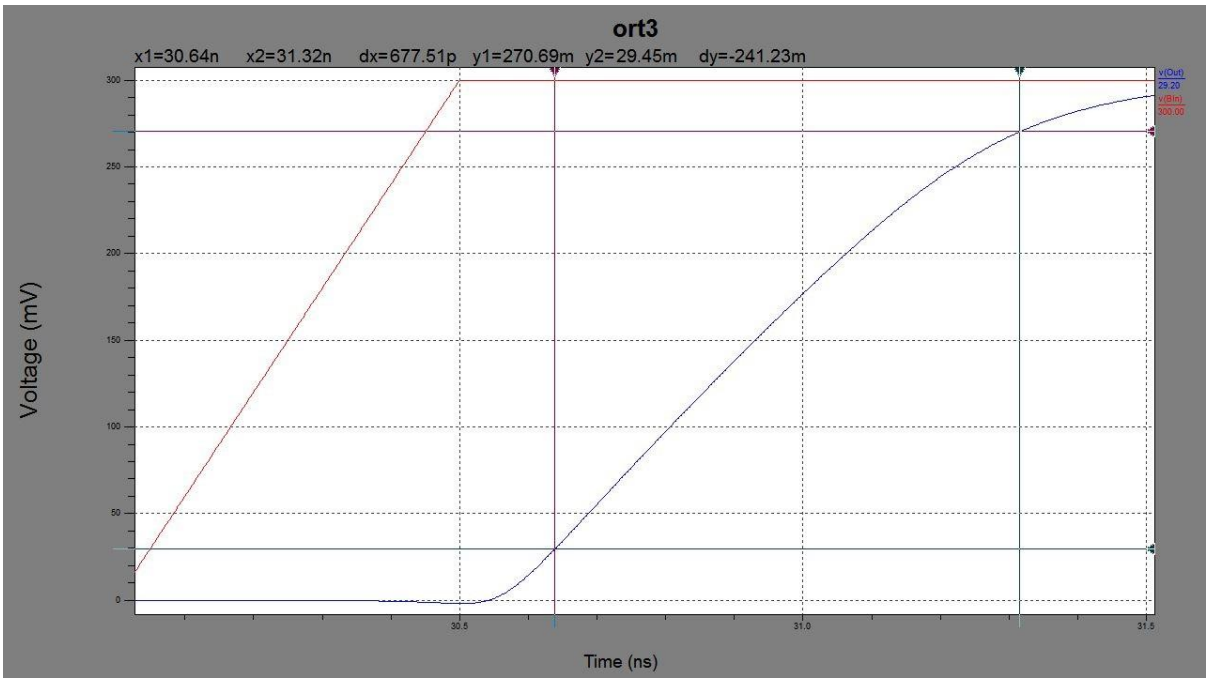


Fig 6.27 Rise time of domino OR type 3.

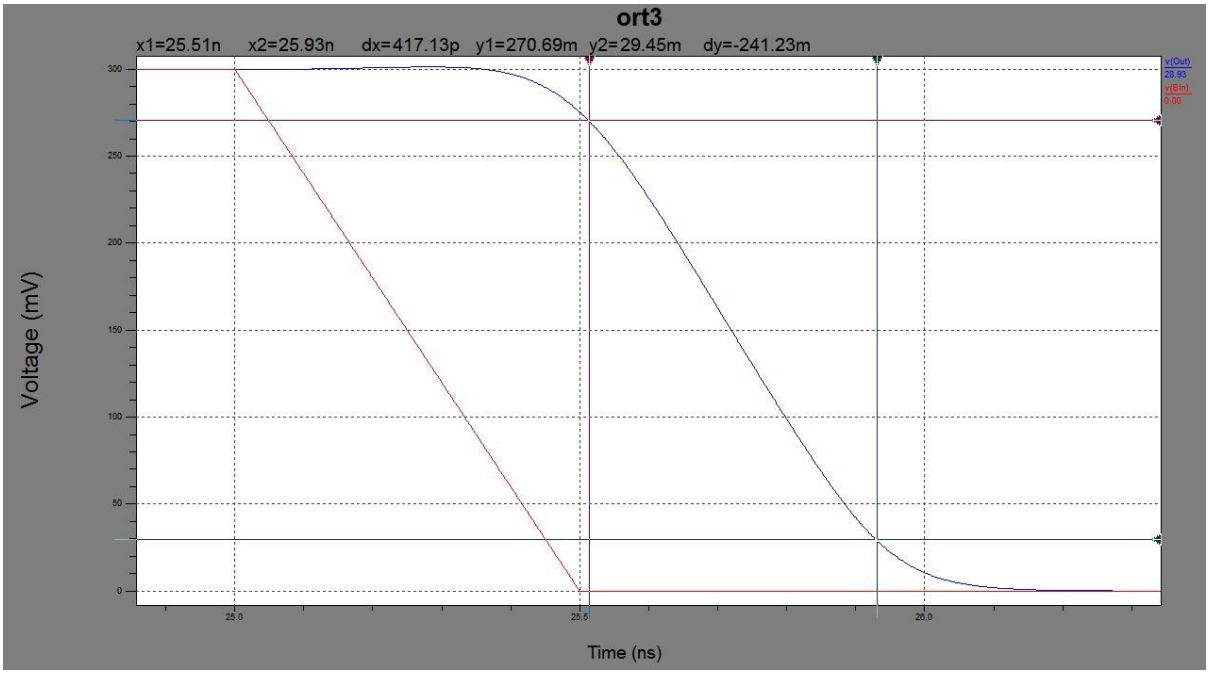


Fig 6.28 Fall time of domino OR type 3.

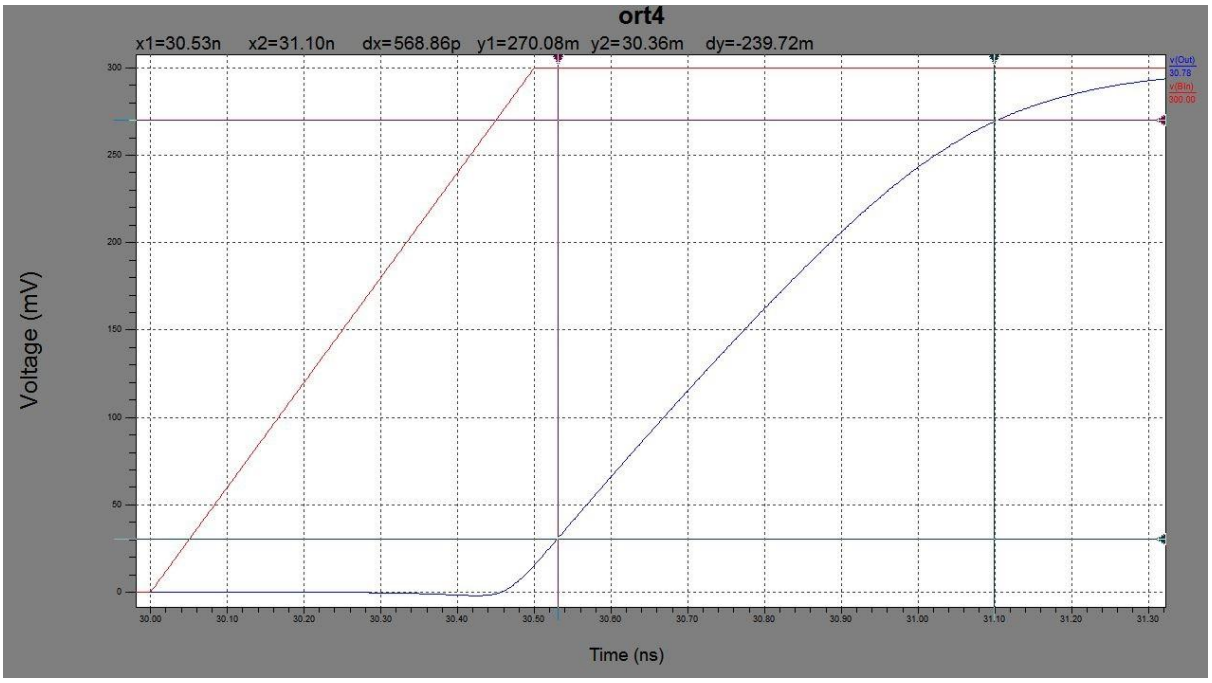


Fig 6.29 Rise time of domino OR type 4.

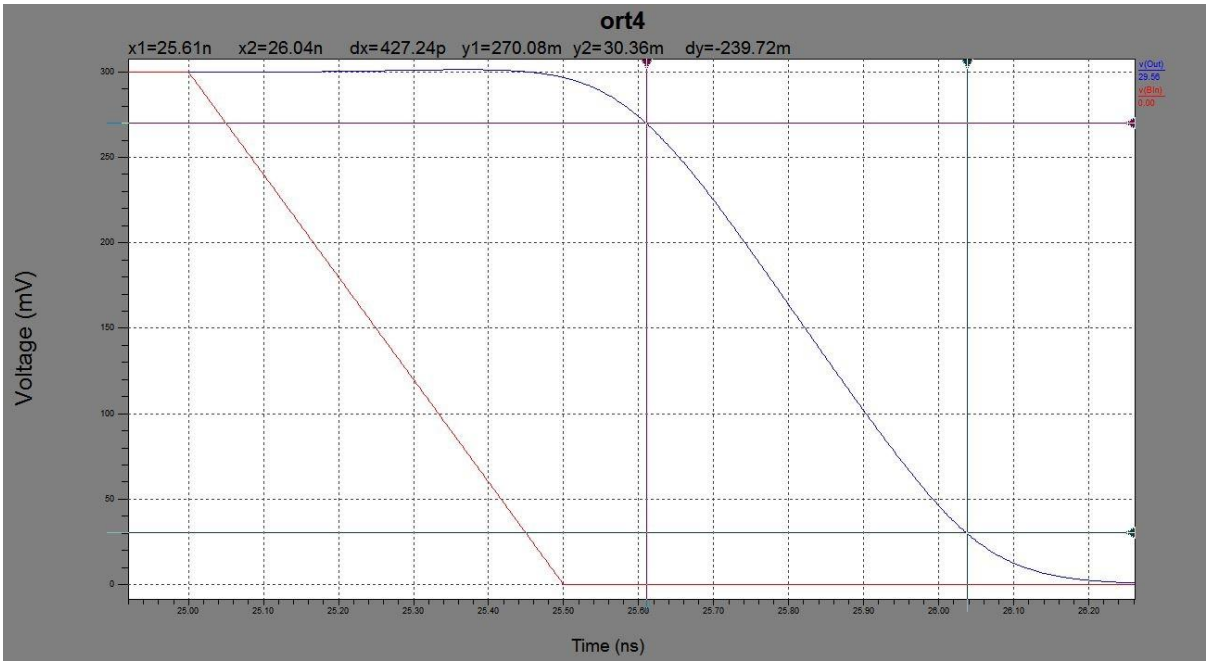


Fig 6.30 Fall time of domino OR type 4.

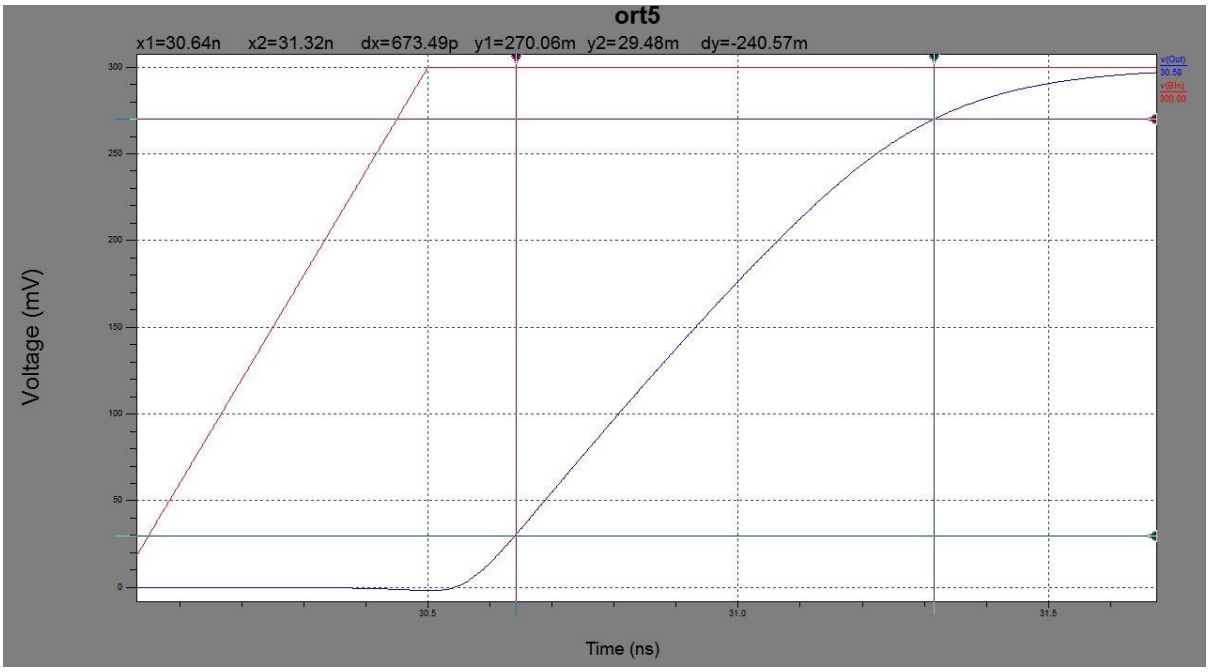


Fig 6.31 Rise time of domino OR type 5.

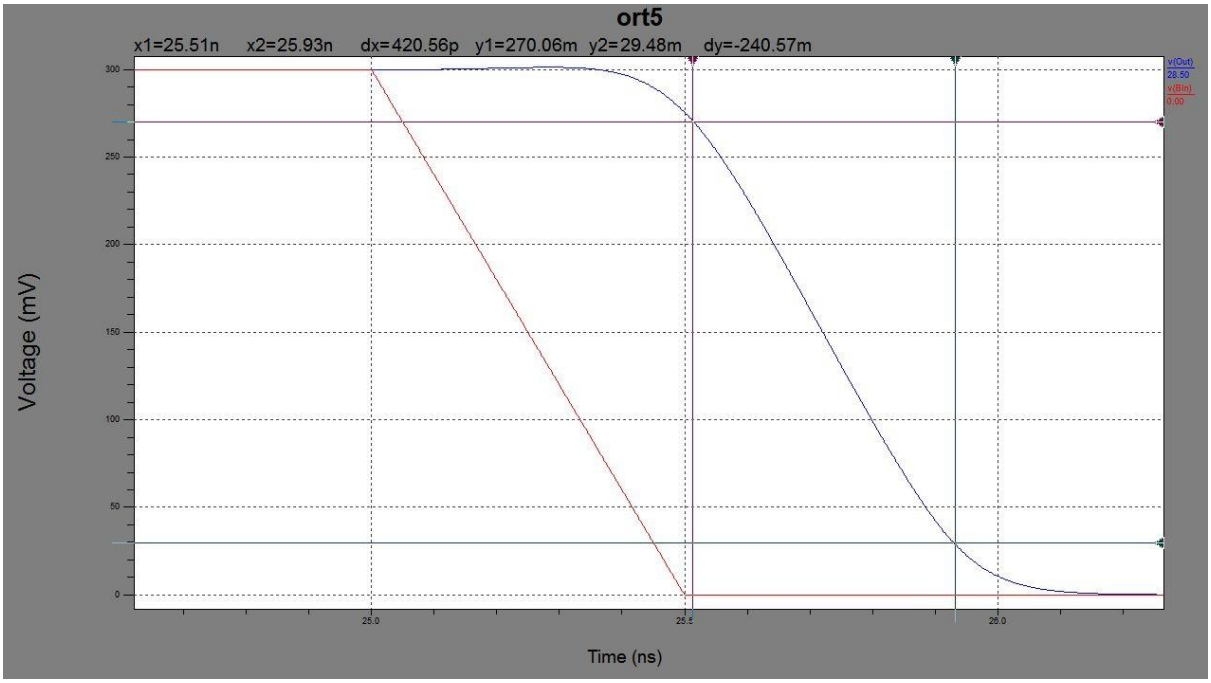


Fig 6.32 Fall time of domino OR type 5.

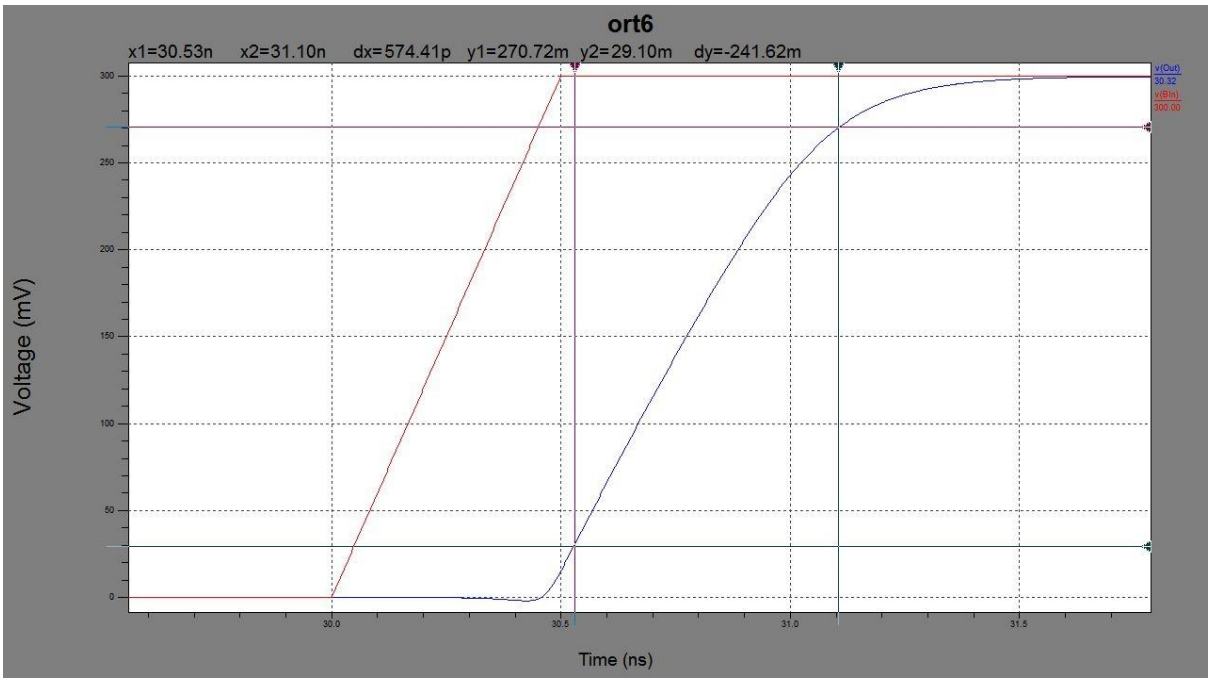


Fig 6.33 Rise time of domino OR type 6.

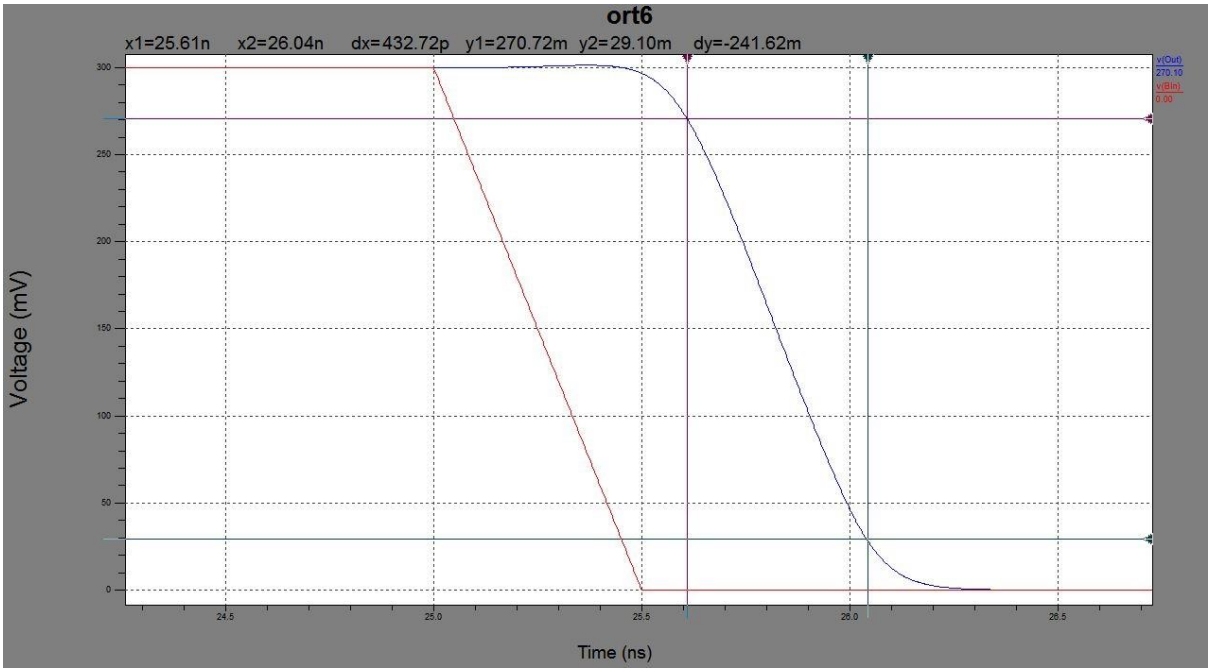


Fig 6.34 Fall time of domino OR type 6.

Chapter 7

Conclusion

A new RC delay approach for high speed domino OR and domino AND circuits using six different bulk biasing techniques for subthreshold operation are analyzed. Based on predictive technology model (PTM), the inverter and other circuits are designed for symmetricity. We observe that, the size of NMOS is smaller than the size of PMOS to make circuits symmetric. This is due to the fact that the subthreshold current is exponential in nature. Analytical results are verified by SPICE simulations. It is observed that the analytical results are accurately matched with simulated results with minimum error for all circuits.

It is found that type 4 circuit has a smaller delay as compared to type 2 OR circuit. If domino AND is considered, type 1 has least theoretical delay. It has been also seen that the domino OR type 4 and domino AND type 1 has least output capacitances which make these circuits faster than their counterparts. In terms of power delay product consideration in subthreshold operation, domino OR type 2 and domino AND type 2 are more efficient due to the lower value of the power delay product.

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APPENDIX

A.1 PTM level 54 model

.model nmos nmos level = 54

+version = 4.0	binunit = 1	paramchk= 1	mobmod = 0
+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	+tnom = 27
toxe = 6.5e-010	toxp = 4e-010	toxm = 6.5e-010	+dtox = 2.5e-010
epsrox = 3.9	wint = 5e-009	lint = 1.35e-009	+ll = 0 wl = 0
lln = 1	wln = 1	+lw = 0	ww = 0
lwn = 1	wwn = 1	+lwl = 0	wwl = 0
xpart = 0	toxref = 6.5e-010	xl = -9e-9	+dlcig = 1.35e-009
+vth0 = 0.3692	k1 = 0.2 k2 = 0	k3 = 0	+k3b = 0
w0 = 2.5e-006	dvt0 = 1	dvt1 = 2	+dvt2 = 0
dvt0w = 0	dvt1w = 0	dvt2w = 0	+dsub = 0.078
minv = 0.05	voffl = 0	dvtp0 = 1e-011	+dvtp1 = 0.1
lpe0 = 0	lpeb = 0	xj = 7.2e-009	+ngate = 1e+023
ndep = 1.2e+019	nsd = 2e+020	phin = 0	+cdsc = 0
cdscb = 0	cdscd = 0	cit = 0	+voff = -0.13
nfactor = 2.3	eta0 = 0.0045	etab = 0	+vfb = -1.058
u0 = 0.0181	ua = -5e-010	ub = 1.7e-018	+uc = 0
vsat = 200000	a0 = 1	ags = 0	+a1 = 0
a2 = 1	b0 = 0	b1 = 0	+keta = 0.04
dwg = 0	dwb = 0	pclm = 0.06	+pdiblc1 = 0.001
pdiblc2 = 0.001	pdiblcb = -0.005	drout = 0.5	+pvag = 1e-020
delta = 0.01	pscbe1 = 2.0e+009	pscbe2 = 1e-007	+fprout = 0.2
pdits = 0.01	pditsd = 0.23	pditsl = 2300000	+rsh = 5
rdsw = 60	rsw = 30	rdw = 30	+rdswmin = 0
rdwmin = 0	rswmin = 0	prwg = 0	+prwb = 0
wr = 1	alpha0 = 0.074	alpha1 = 0.005	+beta0 = 30
agidl = 0.0002	bgidl = 2.1e+009	cgidl = 0.0002	+egidl = 0.8
aigbacc = 0.012	bigbacc = 0.0028	cigbacc = 0.002	+nigbacc = 1
aigbinv = 0.014	bigbinv = 0.004	cigbinv = 0.004	+eigbinv = 1.1
nigbinv = 3	aigc = 0.0213	bigc = 0.0025889	+cigc = 0.002
aigsd = 0.0213	bigsd = 0.0025889	cigsd = 0.002	+nigc = 1
poxedge = 1	pigcd = 1	ntox = 1	+xrcrg1 = 12
xrcrg2 = 5	+cgso = 7e-011	cgdo = 7e-011	cgbo = 0
cgdl = 7.5e-013	+cgsl = 7.5e-013	clc = 1e-007	cle = 0.6
cf = 1.1e-010	+ckappas = 0.6	ckappad = 0.6	vfbcv = -1
acde = 195	+moin = 15	noff = 1	voffcv = 0
+kt1 = -0.154	kt1l = 0	kt2 = 0.022	ute = -1.1
+ua1 = 1e-009	ub1 = -1e-018	uc1 = -5.6e-011	prt = 0
+at = 33000	+fnoimod = 1	tnoimod = 0	noia = 6.25e+041
noib = 3.125e+026	+noic = 8.75e+009	em = 41000000	af = 1
ef = 1	+kf = 0	tnoia = 1.5	tnoib = 3.5
ntnoi = 1	+jss = 1.2e-006	jsws = 2.4e-013	jswgs = 2.4e-013
njs = 1	+ijthsfwd= 0.1	ijthsrev= 0.1	bvs = 10
xjbvs = 1	+jsd = 1.2e-006	jswd = 2.4e-013	jswgd = 2.4e-013

xjbvd = 1	+pbs = 1	cjs = 0.0018	mjs = 0.5
pbsws = 1	+cjsws = 1.2e-010	mjsws = 0.33	cjswgs = 2.1e-010
cjd = 0.0018	+cjswd = 1.2e-010	mjswd = 0.33	pbswgd = 1
cjswgd = 2.1e-010	+mjswgd = 0.33	tpb = 0	tcj = 0
tpbsw = 0	+tcjsw = 0	tpbswg = 0	tcjswg = 0
xtis = 3	+dmcg = 0	dmci = 0	dmdg = 0
dmcgt = 0	+dwj = 0	xgw = 0	xgl = 0
+rshg = 0.4	gbmin = 1e-010	rbpb = 5	rbpd = 15
+rbps = 15	rbdb = 15	rbsb = 15	ngcon = 1

.model pmos pmos level = 54

+version = 4.0	binunit = 1	paramchk= 1	mobmod = 0
+capmod = 2	igcmod = 1	igbmod = 1	geomod = 1
+diomod = 1	rdsmod = 0	rbodymod= 1	rgatemod= 1
+permod = 1	acnqsmod= 0	trnqsmod= 0	+tnom = 27
toxe = 6.7e-010	toxp = 4e-010	toxm = 6.7e-010	+dtox = 2.7e-010
epsrox = 3.9	wint = 5e-009	lint = 1.35e-009	+ll = 0
wl = 0	lln = 1	wln = 1	+lw = 0
ww = 0	lwn = 1	wwn = 1	+lwl = 0
wwl = 0	xpart = 0	toxref = 6.7e-010	xl = -9e-9
+dlcig = 1.35e-009	+vth0 = -0.25399	k1 = 0.2	k2 = -0.01
k3 = 0	+k3b = 0	w0 = 2.5e-006	dvt0 = 1
dvt1 = 2	+dvt2 = -0.032	dvt0w = 0	dvt1w = 0
dvt2w = 0	+dsub = 0.1	minv = 0.05	voffl = 0
dvtp0 = 1e-011	+dvtp1 = 0.05	lpe0 = 0	lpeb = 0
xj = 7.2e-009	+ngate = 1e+023	ndep = 4.4e+018	nsd = 2e+020
phin = 0	+cdsc = 0	cdscb = 0	cdscd = 0
cit = 0	+voff = -0.13	nfactor = 2.3	eta0 = 0.0037
etab = 0	+vfb = -1.058	u0 = 0.0023	ua = -5e-010
ub = 1.6e-018	+uc = 0	vsat = 78000	a0 = 1
ags = 1e-020	+a1 = 0	a2 = 1	b0 = 0
b1 = 0	+keta = -0.047	dwg = 0	dwb = 0
pclm = 0.1	+pdiblc1 = 0.001	pdiblc2 = 0.001	pdiblcb = 3.4e-008
drout = 0.6	+pvag = 1e-020	delta = 0.01	pscbe1 = 2e+009
pscbe2 = 9.58e-007	+fprout = 0.2	pdits = 0.08	pditsd = 0.23
pditsl = 2300000	+rsh = 5	rdsw = 60	rsw = 30
rdw = 30	+rdswmin = 0	rdwmin = 0	rswmin = 0
prwg = 096	+prwb = 0	wr = 1	alpha0 = 0.074
alpha1 = 0.005	+beta0 = 30	agidl = 0.0002	bgidl = 2.1e+009
cgidl = 0.0002	+egidl = 0.8	aigbacc = 0.012	bigbacc = 0.0028
cigbacc = 0.002	+nigbacc = 1	aigbinv = 0.014	bigbinv = 0.004
cigbinv = 0.004	+eigbinv = 1.1	nigbinv = 3	aigc = 0.012731
bigc = 0.00115	+cigc = 0.0008	aigsd = 0.012731	bigsd = 0.00115
cigsd = 0.0008	+nigc = 1	poxedge = 1	pigcd = 1
ntox = 1	+xrcrg1 = 12	xrcrg2 = 5	+cgso = 7e-011
cgdo = 7e-011	cgbo = 0	cgdl = 3e-011	+cgsl = 3e-011
clc = 1e-007	cle = 0.6	cf = 1.1e-010	+ckappas = 0.6
ckappad = 0.6	vfbcv = -1	acde = 1	+moin = 15
noff = 1	voffcv = 0	+kt1 = -0.14	kt1l = 0
kt2 = 0.022	ute = -1.1	+ua1 = 1e-009	ub1 = -1e-018

uc1 = -5.6e-011	prt = 0	+at = 33000	+fnoimod = 1
tnoimod = 0	noia = 6.25e+041	noib = 3.125e+026	+noic = 8.75e+009
em = 41000000	af = 1	ef = 1	+kf = 0
tnoia = 1.5	tnoib = 3.5	ntnoi = 1	+jss = 2e-007
jsws = 4e-013	jswgs = 4e-013	njs = 1	+ijthsfwd= 0.1
ijthsrev= 0.1	bvs = 10	xjbvs = 1	+jsd = 2e-007
jswd = 4e-013	jswgd = 4e-013	xjbvd = 1	+pbs = 1
cjs = 0.0015	mjs = 0.5	pbsws = 1	+cjsws = 9.4e-011
mjsws = 0.33	cjswgs = 2e-010	cjd = 0.0015	+cjswd = 9.4e-011
mjswd = 0.33	pbswgd = 1	cjswgd = 2e-010	+mjswgd = 0.33
tpb = 0	tcj = 0	tpbsw = 0	+tcjsw = 0
tpbswg = 0	tcjswg = 0	xtis = 3	+dmcg = 0
dmdg = 0	dmcgt = 0	xgw = 0	+xgl = 0
+rshg = 0.1	gbmin = 1e-012	rbpb = 50	rbpd = 50
+rbps = 50	rbdb = 50	rbsb = 50	ngcon = 1