# Analysis of Current and Breakdown Voltages in 3C-SiC Lateral Power MOSFET

*A Thesis Submitted in partial fulfillment of the requirement for the award of degree of*

**MASTER OF ENGINEERING**

**IN**

**ELECTRONICS AND COMMUNICATION ENGINEERING**


Submitted by

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**JUNE-2009**


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# CERTIFICATE

I, Vivek kumar hereby declare that the work, which is being presented in the thesis, entitled **"Analysis of Current and Breakdown Voltages in 3C-SiC Lateral Power MOSFET"** in partial fulfillment of the requirements for the award of degree of Master of Engineering (M. E.) in Electronics and Communication Engineering, at Thapar University, (Formerly as Thapar Institute of Engineering & Technology), Patiala under the guidance of Dr. A. K. Chatterjee, (Professor and Head, ECED).

The matter presented in this thesis has not been submitted in any other University or Institute for the award of any degree.

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# ABSTRACT

High avalanche breakdown field ( 1.0 – 3.0 MV/cm) for SiC makes it alternative material for high voltage, high power devices. Due to high thermal conductivity ( 5 W/cm-$^{o}$C) and high electric field strength, Silicon Carbide can be used at high temperature, high voltage and high power applications.

A 3C-SiC Lateral Double Implanted MOSFET is designed in a uniform lightly doped n $^{+}$ epilayer on an insulating 4H-SiC substrate. After depleting through the epilayer the depletion region continues to move laterally toward the drain. The result is an increase in blocking voltage (Avalanche Breakdown voltage of 4.31 kV , and Punch through breakdown voltage of 4 kV for a doping level of $5\times10^{14}$ $cm^{-3}$ in drift region). This punch through breakdown voltage results in a depletion width of 65.52 μm in drift region.

The current in the device was found to decrease due to reducing mobility of electrons as we increase the doping level of the p-base region ($\mu$ = 580 $cm^2$/V.s, for $N_B$=$10^{16}$ $cm^{-3}$, to 192 $cm^2$/V.s, for $N_B$ =$10^{18}$ $cm^{-3}$ respectively), for the device with Active Channel Length = 2μm and Width = 100μm. The V-I Characteristics of the MOSFET that has been developed with and without channel length modulation (λ), and the value of Early-Voltage has been found to decrease with increase in doping level of the p-base.



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# LIST OF USED ACRONYM

| | |
|---|---|
| CVD | : Chemical Vapor Deposition |
| eV | : Electron Volt |
| MOSFET | : Metal-Oxide Semiconductor Field Effect Transistor |
| SiC | : Silicon Carbide |
| $SiO_2$ | : Silicon dioxide |
| VPE | : Vapor Phase Epitaxy |
| $E_g$ | : Energy bandgap |
| $E_C$ | : Energy Conduction Band |
| $E_{fm}$ | : Metal Fermi Level |
| $\phi_m$ | : Metal Work Function |
| $\phi_S$ | : Semiconductor Work Function |
| $E_{fs}$ | : Semiconductor Fermi Level |
| $E_0$ | : Vacuum Level |
| $\phi_{Bn}$ | : Barrier height of n-type semiconductor |
| $\phi_{Bp}$ | : Barrier height of p-type semiconductor |
| $\phi_B$ | : Barrier height |
| $V_{bi}$ | : Built in voltage |
| $\chi_S$ | : Electron affinity of semiconductor |
| $\in_S$ | : Permittivity of semiconductor |
| $\in_0$ | : Permittivity of free space |
| $N_d$ | : Doping concentration of drift region |
| k | : Boltzmn constant |
| T | : Temperature |
| q | : Electronic Charge |
| $n_i$ | : Intrinsic Carrier Concentration |
| $\delta$ | : Fitting parameter |
| α | : Fitting parameter |
| $V_B$ | : Breakdown Voltage |
| $\in_{cr}$ | : Critical electric field |



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$R_{on-sp}$ : Specific on-resistance

$\mu_n$ : Electron mobility

$W_d$ : Depletion width

$V_R$ : Reverse Bias Voltage

$\gamma$ :Body effect term

$C_{ox}$ :Oxide capacitance

$V_{FB}$ :Flat band voltage

$N_B$ :Doping concentration of p-base

$V_{Dsat}$ :Drain to source saturation voltage

$\lambda$ :Channel length modulation parameter

$V_{BPT}$ :Punch through breakdown voltage



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# CHAPTER 1

# INTRODUCTION

## BRIEF HISTORY OF SILICON CARBIDE

Silicon carbide was first observed in 1824 by the Swedish scientist, Jons Jacob Berzelius in an attempt to synthesize diamond, while naturally occurring SiC has been discovered by Henri Moissan in 1905, who found small hexagonal platelets in a meteorite. The mineral is now called Moissanite in his honor, and this has also become the name of commercial gemstones made from SiC. However, SiC is very rare in nature and has not been found freely yet, this is probably one cause of its relatively late discovery. The history of man-made SiC starts in 1891, when Acheson produced SiC in an electric melting furnace, mainly for grinding and polishing purposes. Later, in the 1950s, when research on solid state electronic devices has started, SiC was one of the semiconductor materials studied. In 1955 Lely introduced a crystal growth technique to produce high quality bulk SiC, but the problem of producing large-area defect-free single crystals has not been solved, making device fabrication impossible. Later, in 1978 the so-called seeded sublimation epitaxy or modified Lely method was developed by Tairov and Tsvetkov, advancing the research field. Recently the most commonly used technique for epitaxial growth of SiC is the vapor phase epitaxy (VPE) method usually realized in a chemical vapor deposition (CVD) reactor [1].

Due to the increased interest that SiC received, series of conferences was introduced, such as the International Conferences on Silicon Carbide and Related Material (ICSCRM) and the European Conferences on Silicon Carbide and Related Materials (ECSCRM). The rapid growth in SiC research is reflected in the number of contributions, which increased from 28 at the first ICSCRM conference held in Washington, D.C. in 1987 (by that time called as First International Conference on Amorphous and Crystalline Silicon Carbide and Related Materials) to 430 at the latest one in Lyon, France 2003, making this conference the largest meeting of its kind worldwide.

Silicon-based power devices have long dominated the power electronics and power systems applications. Devices such as bipolar, unipolar, controlled, uncontrolled, and MOS-gated made by Si are widely used by power electronics and power systems designers. Examples of such devices are diodes ( p-i-n and Schottky rectifiers), thyristors,



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gate turn-off thyristors (GTOs), bipolar junction transistors (BJTs), insulated-gate bipolar transistors (IGBTs), and power metal–oxide–semiconductor field-effect transistors (MOSFETs).

Large-area devices that are capable of handling thousands of amperes and kilovolts such as IGBTs are now able to handle voltages up to 6 kV and currents up to 1200 A [2]. IGBTs are being widely used for motor drives, resonant converters, and power supplies [3–5]. GTOs and thyristors are still widely used for very high power applications, such as power systems conditioning equipment, dynamic voltage regulators, transfer switches, and large direct-current rectifiers [6–9]. MOSFETs have high conduction losses due to their high on-state resistance, $R_{dson}$. As the blocking voltage increases, so does their on-state resistance $R_{dson}$, hence, making MOSFETs less attractive for high-voltage applications (beyond 600 V). Recent enhancements in power MOSFET technology such as the Cool MOS allow for substantial reduction of the conduction losses.

But the need for faster devices with high voltage and high switching frequency capability is growing, Silicon-based devices are not able to meet these requirements without costly cooling systems, so Wide band-gap based semiconductor devices such as silicon carbide and gallium nitride offer multiple advantages for power electronic designers. The superior physical properties of these semiconductors offer a lower intrinsic carrier concentration (10–35 orders of magnitude), a higher electric breakdown field (4–20 times), a higher thermal conductivity (3–13 times), a larger saturated electron drift velocity (2–2.5 times) which is suitable for faster devices with high voltage and high switching frequency.

## 1.1 WBG SEMICONDUCTOR

Wide band gap (WBG) semiconductor is a semiconductor with an energy band gap wider than about 2eV. Examples of WBG semiconductors are gallium nitride (GaN, $E_G$ = 3.4eV), aluminum nitride (AlN, $E_G$ = 6.2eV), and silicon carbide (SiC, $E_G$ between 2.2eV to 3.25eV depending on polytype). Polytype mean 3C, 4H, 6H, and 15R- Silicon Carbide [10].

Since the electronic properties of a semiconductor are dominated by the highest partially empty band and the lowest partially filled band, it is often sufficient to only consider those bands. This leads to a simplified energy band diagram for semiconductors.



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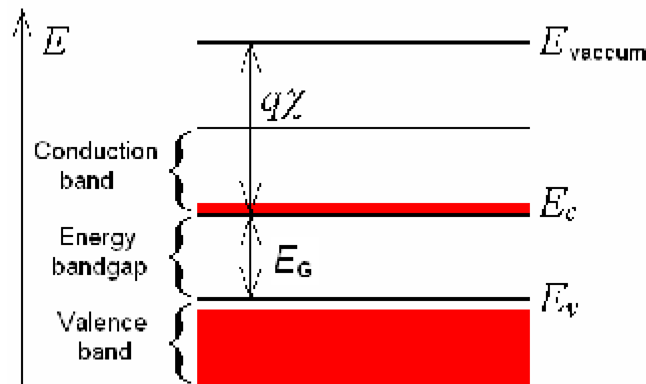


**FIGURE. 1.1:** Energy band diagram

The numerous polytype forms of silicon carbide, 4H-SiC and 6H-SiC electronic devices presently most useful due to the availability and quality of reproducible single crystal wafers of these polytypes. The availability of 6H-SiC and 4H-SiC polytypes in bulk wafer form has helped SiC to emerge as one of the relatively mature wide-band semiconductor technologies. SiC is a material with immense potential for use in hetero-structure electronic devices, which take advantage of differing band gaps, carrier mobilities, etc. However, there are many crucial crystal growth and device fabrication issues that have to be addressed before SiC-based devices and circuits are ready for scale up and reliable incorporation into electronic systems.

## 1.2 SILICON CARBIDE

Silicon carbide is a WBG semiconductor that possesses extremely high thermal, chemical, and mechanical stability. It is so thermally stable that dopant impurities cannot be diffused at any reasonable temperature.Single-crystal SiC forms in the hexagonal lattice, with alternating hexagonal planes of silicon and carbon atoms, (as shown in Fig.1.2). Each silicon atom bonds to four nearest-neighbor carbon atoms, and each carbon atom bonds to four nearest-neighbor silicon atoms (bonds are not shown). Note that the atoms in the second silicon plane are offset with respect to the atoms in the first silicon plane. As successive planes are added, each plane must be offset with respect to the plane below. This stacking sequence leads to different flavors, or polytypes, of the basic SiC crystal. There are large number of possible polytypes, but the most important are 3C, 4H, and 6H. The polytypes differ in band gap energy, carrier mobility, and



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breakdown field. For example, the $E_G$ = 2.2, 3.25, and 3.0 eV for 3C, 4H, and 6H-SiC respectively [10].

Silicon atoms (blue) and carbon atoms (red) form alternating hexagonal planes. The sticks in this rendering are intended to emphasize the hexagonal lattice arrangement, do not represent bonds. Each carbon atom bonds to three silicon atoms in the plane below and to one silicon atom in the plane above (bonds not shown). Note that the silicon atoms in the top plane are offset with respect to the silicon atoms in the bottom plane.

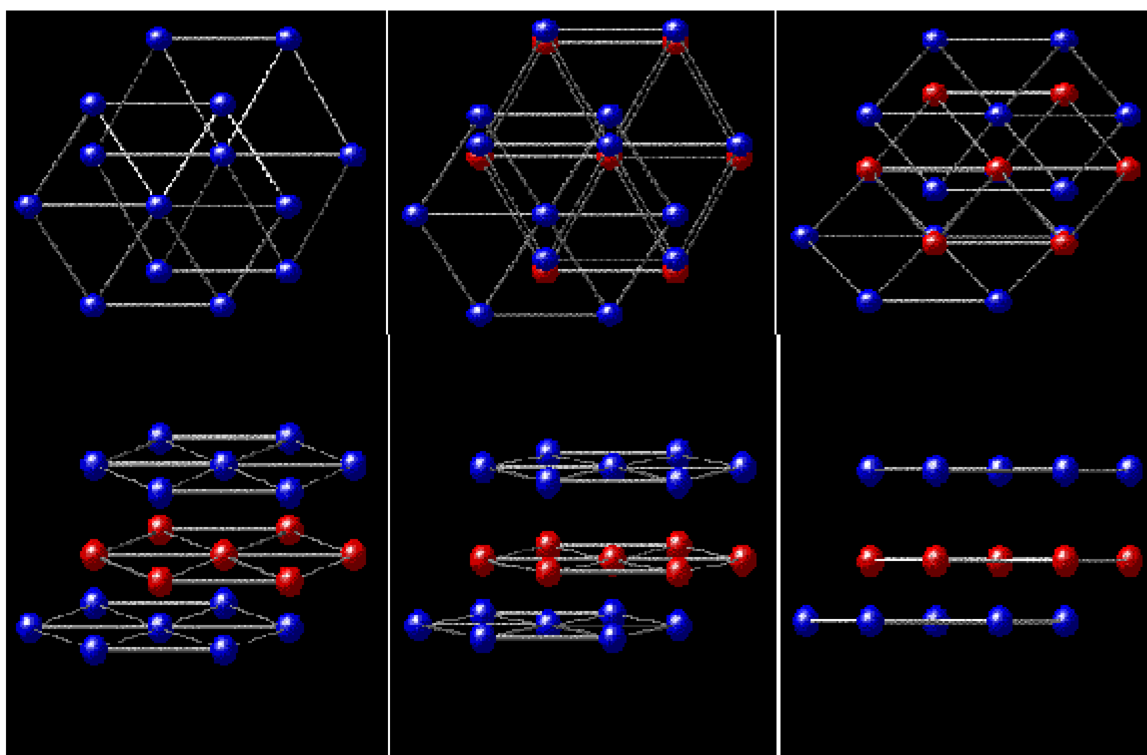

**FIGURE.1.2:** Primitive crystal structure of SiC [10].

### 1.2.1 Importance of SiC

Silicon carbide is the only WBG semiconductor that possesses a high-quality native oxide suitable for use as an MOS insulator in electronic devices. Thermal oxidation of SiC produces a layer of $SiO_2$ on the surface, while the carbon atoms from the SiC form CO, which escapes as a gas. Thus it is possible to make all the devices found in silicon IC



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technology in SiC, including high quality, stable MOS transistors and MOS integrated circuits.

The breakdown field in SiC is about 8 times higher than in silicon. This is important forhigh-voltage power switching transistors. For example, a device of given size in SiC will have a blocking voltage 8 times higher than the same device in silicon. More importantly, the on-resistance of the SiC device will be about 100 times lower than the silicon device [10].

Because  the band-gap of SiC is so much wider than silicon. Thermal generation of electron-hole pairs is many orders of magnitude lower at any given temperature. This makes it possible to build “dynamic” memories (DRAMs) in SiC that only need to be refreshed about once every 100 years at room temperature. This also makes it possible to operate SiC devices at temperatures as high as 650°C without degradation in electrical performance.

### 1.2.2 Silicon Carbide Polytypes

Silicon carbide is known as a wide band-gap semiconductor existing in many different polytypes. All polytypes have a hexagonal frame with a carbon atom situated above the center of a triangle of Si atoms and underneath a Si atom belonging to the next layer Fig.1.3. The distance, ‘a’ between neighbouring silicon or carbon atoms is approximately 3.08 Å for all  polytypes. The carbon atom is positioned at the center of mass of the tetragonal structure
outlined by the four neighboring Si atoms so that the distance between the C atom to each of the Si atoms is the same. Geometrical considerations give that this distance, C-Si, is $a(3/8)^{1/2}$ i.e. approximately equal to 1.89 Å. The distance between two silicon planes is, thus, $a(2/3)^{1/2}$ i.e. approximately 2.52 Å. The height of a unit cell, c, varies between the different polytypes. The ratio c/a, thus, differs from polytype to polytype, but is always close to the ideal for a closed packed structure. This ratio is for instance approximately 1.641, 3.271 and 4.908 for the 2H-SiC, 4H-SiC and 6H-SiC polytypes, respectively whereas the equivalent ideal ratios for these polytypes are $(8/3)^{1/2}$, $2(8/3)^{1/2}$ and $3(8/3)^{1/2}$, respectively. The difference between the polytypes is the stacking order between succeeding double layers of carbon and silicon atoms [3].



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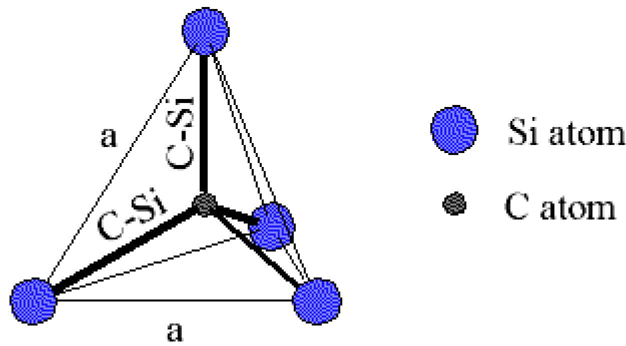


**FIGURE 1.3:** Tetragonal bonding of a carbon atom with the four nearest silicon neighbors [11].

In Fig.1.5 the stacking sequence is shown for the three most common polytypes, 3C, 6H and 4H. If the first double layer is called the A position, the next layer that can be placed according to a closed packed structure will be placed on the B position or the C position. The different polytypes will be constructed by permutations of these three positions. For instance will the 2H-SiC polytype have a stacking sequence ABAB… The number thus denotes the periodicity and the letter the resulting structure which in this case is hexagonal. The 3C-SiC polytype is the only cubic polytype and it has a stacking sequence ABCABC… or ACBACB… A common crystalline defect is the so called Double Positioning Boundary (DPB), which is commonly seen in 3C-SiC grown on on-axis 6H-SiC substrates. The defect arises when islands of the two possible stacking sequences ABCABC and ACBACB meet. There are some 200 polytypes proven in existence, some with a stacking period of several hundred double layers. It is hard to understand how these crystals grow since there has to exist some 'memory' which guides the atoms into the right stacking sequence. The 6H-SiC polytype grows each atom landing on the surface must sense at least 6 layers down in order to find its proper site. When the stacking sequence amounts several hundred double layers.

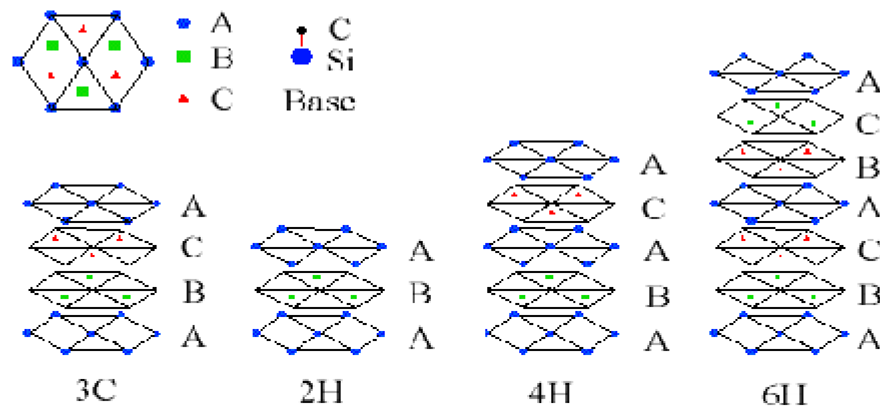


**FIGURE. 1.4:** Stacking sequence of double layer of the three most common SiC polytypes [11].



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it becomes even more difficult to understand how these crystals can grow. There are however growth mechanisms which aid the atoms into finding the correct site. By looking at a SiC crystal along the c-direction all polytypes would look the same since this is the direction the layers are stacked. If one would look at the crystals from the edge, the stacking sequence would easily be seen provided one was gifted with atomic resolution eyesight. The spiral will provide a step which may show the whole or part of the stacking sequence on the side. Since the growth proceeds at the edge of the spiral, the impinging atoms will be guided both by the underlying atoms and the atoms on the side of the spiral. A similar approach is used in order to grow Chemical Vapor Deposition (CVD). Layers at lower temperatures. In this case off-axis polished substrates are used in order to produce the necessary steps. It is possible to grow 6H-SiC on on-axis substrates by CVD, however, it normally requires slightly elevated temperatures. It is not established if the growth in this case proceeds as spiral growth. It is likely that the surface energy of different sites differs. This energy would be a superposition of energies ranging far down in the crystal, which would be acting as a sort of 'memory'. The impinging atoms must have a surface mobility which is high enough in order to move to the most favorable position. This energy difference between two possible positions may be very small and it is possible that the growth eventually develops into a spiral which would provide the highest growth rates at the lowest cost in energy (fewer stacking faults) [11].

By observing the SiC crystal from the side as previously proposed, the stacking sequence can be projected as in Fig.1.6 where the 6H-SiC polytype is shown. When the stacking sequence is drawn in this manner a zig zag pattern is revealed. The surrounding lattice does not, however, look the same for each position. In the Fig.1.5, the A position has a different surrounding lattice than the B and C positions. We call this position the hexagonal site, h. It is simply characterized as the turning point of the zig zag pattern. The other two positions (B and C) are called cubic, k1 and k2. An impurity replacing a host atom at one of the three sites will obtain a different binding energy depending on the site it replaces. A very illustrative example is the nitrogen donor in 6H-SiC. The hexagonal site gives rise to the P-level of the nitrogen donor with a binding energy of approximately 85 meV. The two cubic sites will give the R- and S-levels with binding energies around 138 meV and 142 meV, respectively. In the 4H-SiC polytype there are only two in-equivalent sites, one hexagonal and one cubic ( Fig.1.5). The two levels of the nitrogen donor are in this case called P and Q. In 3C there is of course only one cubic



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site and in 2H there is only one hexagonal site (Fig.1.5). The 6H-SiC polytype can thus be characterized as being 33% hexagonal, whereas the 4H- and 2H-SiC polytypes are 50% and 100% hexagonal, respectively.

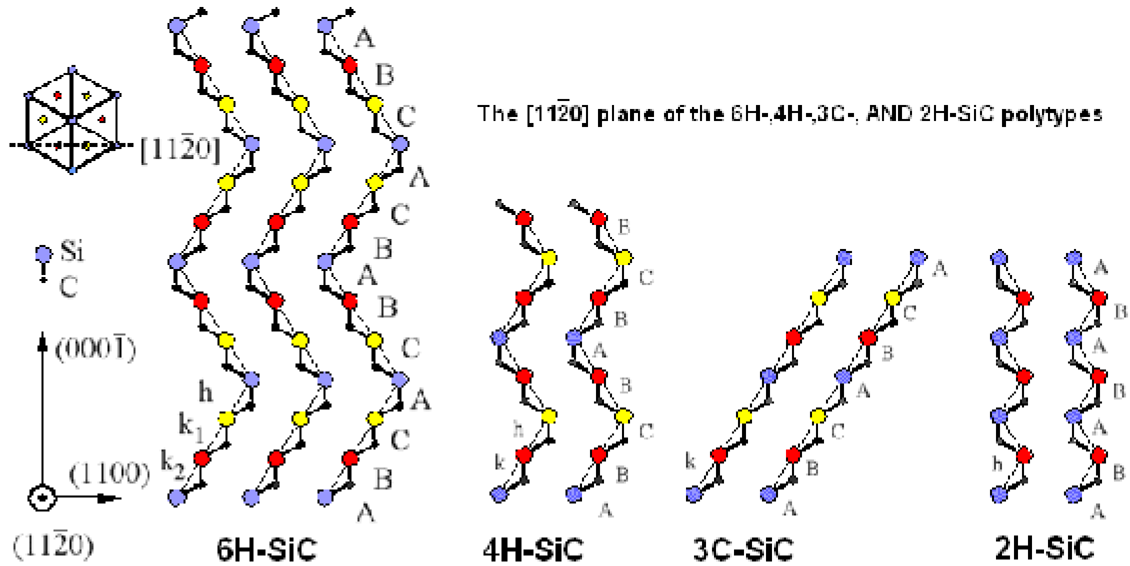


**FIGURE 1.5:** The plane of the 6H-, 4H-, 3C-, and 2H-SiC polytypes [11].

There are four hexagonal Miller indices describing the directions in all SiC polytypes except for the 3C polytype where the normal cubic notation is used. The last hexagonal index refers to the c-direction, whereas the three first describes directions in the basal plane. The angle between two adjacent basal plane axis is 120$^o$ as shown in Fig 1.6. By definition, the sum of the first three indices must be zero. One of them is thus redundant but is kept for simplicity.

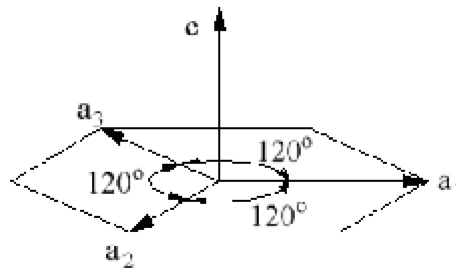


**FIGURE 1.6:** The Miller indices describing the hexagonal structure [11].

The plane formed by a bi-layer sheet of Si and C atoms is known as the basal plane, while the crystallographic c-axis direction, also known as the stacking direction or the [0001]



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direction, is defined normal to Si-C bi-layer plane. Fig.1.8 schematically depicts the stacking sequence of 6H-SiC polytype, which requires six Si-C bi-layers to define the unit cell repeat distance along the c-axis [0001] direction. The [1100] direction depicted in Fig.1.8 is often referred to as the a-axis direction. The silicon atoms labeled “h” or “k” in Fig.1.8 denote Si-C double layers that reside in “quasi-hexagonal” or “quasi-cubic” environments with respect to their immediately neighboring above and below bilayers. SiC is a polar semiconductor across the c-axis, in that one surface normal to the c-axis is terminated with silicon atoms while the opposite normal c-axis surface is terminated with carbon atoms. As shown in Fig.1.8, these surfaces are typically referred to as “silicon face” and “carbon face” surfaces [12].

### 1.3 COMPARISON OF PROPERTIES OF SiC, Si & GaAs

Silicon Carbide (SiC), has superior properties for power devices as compared to silicon. Silicon carbide (SiC) device development is increasing due to the need for electronic devices capable of operation at high power levels and high temperature. The main strength of silicon carbide is that it can resist high field strengths, offers better heat-conducting capacity than

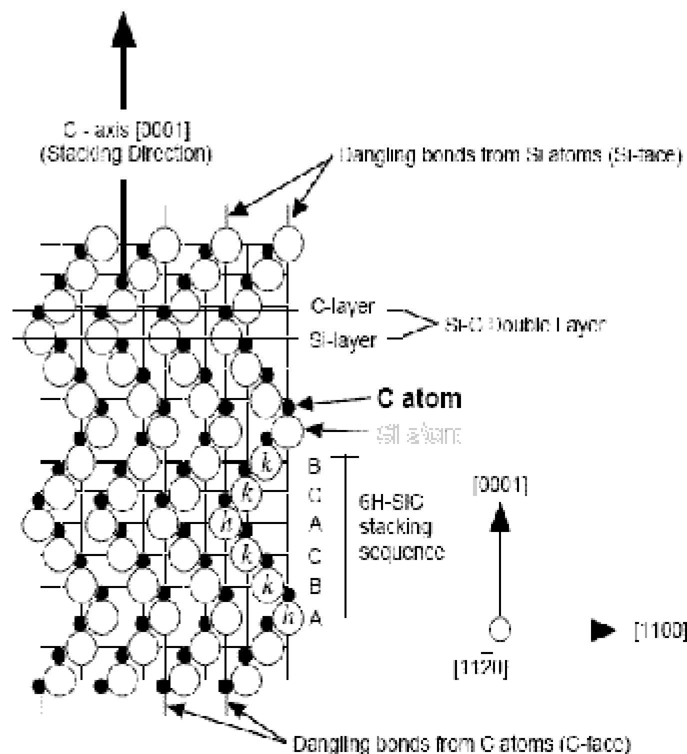


**FIGURE 1.7:** Schematic cross-section of SiC of {(1120) plane} the 6H SiC polytype [12].



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copper at room temperature andt has a large energy band gap, which means that electrical components continue functioning even when the mercury starts climbing. With very high thermal conductivity (~5.0W/cm-K), high saturated electron drift velocity (~2.7x$10^7$cm/s) and high breakdown electric field strength (~3MV/cm), SiC is a material of choice for high temperature, high voltage, high frequency and high power applications[5]. Table 1.1 lists electrical properties of the common SiC polytypes in comparison to that of Si and GaAs [13].

The most important SiC property of all is the large bandgap, which is nearly three times larger than that of silicon. The large S-C bonding energy makes SiC resistant to chemical attack and radiation. Silicon carbide belongs to a class of semiconductors commonly known as wide band gap semiconductors, where conventional semiconductors like Si and GaAs cannot adequately perform under extreme conditions. The wider band gap of SiC also enables one to design smaller, higher density devices that will withstand high voltages. The high thermal conductivity of SiC decreases the need for special packaging and system cooling for device operation [13].

**TABLE 1.1:** Comparison of Properties of SiC with Si and GaAs at Room Temperature [14].

| | **Si** | **GaAs** | **GaN** | **6H-SiC** | **4H-SiC** | **3C-SiC** |
|---|---|---|---|---|---|---|
| Bandgap(eV) | **1.1** | **1.142** | **3.39** | **3** | **3.26** | **2.2** |
| Breakdown field @$10^{17}$ $cm^{-3}$ (MV/cm) | **0.6** | **0.6** | **3.3** | **3.2** | **3.0** | **1.5** |
| Electron mobility @ $10^{16}$ $cm^{-3}$ ($cm^2$/Vs) | **1100** | **6000** | **1000** | **370** | **800** | **750** |
| Hole mobility @$10^{16}$ $cm^{-3}$ ($cm^2$/Vs) | **420** | **320** | **200** | **90** | **115** | **40** |
| Saturated electron drift velocity(cm/s) | **$10^7$** | **$10^7$** | **$2.5\times10^7$** | **$2\times10^7$** | **$2\times10^7$** | **$2\times10^7$** |
| Intrisic concentration, $n_i$ ($cm^{-3}$) | **$1.5\times10^{10}$** | **$1.9\times10^{-10}$** | **$2.1\times10^6$** | **$2.3\times10^{-6}$** | **$8.2\times10^{-9}$** | **6.9** |
| Thermal conductivity | **1.5** | **0.55** | **1.3** | **4.9** | **4.9** | **5** |



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## 1.4 SiC SEMICONDCUTOR CRYSTAL GROWTH

Historical examination shows that serious shortcomings in SiC semiconductor material manufacturability and quality have greatly hindered the development of SiC semiconductor electronics. From a simple point of view, SiC electronics development has followed the general rule that a solid-state electronic device can only be as good as the semiconductor material from which it is made.

Many semiconductor materials can be melted and reproducibly recrystallized into large single-crystals with the aid of a seed crystal, such as in the Czochralski method [15] employed in the manufacture of almost all silicon wafers, enabling reasonably large wafers to be mass-produced. However, because SiC sublimes instead of melting at reasonably attainable pressures, SiC cannot be grown by conventional melt-growth techniques. This prevented the realization of SiC crystals suitable for mass production until the late 1980’s. Sublimate limits the size of the SiC crystals. A modified bulk growth process, called modified sublimation, has been developed and preferred means to produce single crystal SiC wafers [16]. In this method, a single crystal seed and polycrystalline SiC source container are placed in close proximity to each other in a container. The polycrystalline source container is heated to about 24000 $^{0}$C in argon at reduced pressure (~200Pa). The seed crystal is maintained at a temperature of 22000C, and geometry of the reactor is such that a temperature gradient of 10K cm-1 to 20 K cm-1 is maintained along the reactor walls. Under these conditions, sublimation of the polycrystalline source and subsequent nucleation and crystallization on the single crystal seed layer occur at growth rates of up to 4 mm h-1[17]. The modified method is currently used to produce commercial grade 4H-SiC. Limited progress has been made in producing 3C-SiC substrates in the laboratory using 3C-SiC seeds grown by chemical vapor deposition (CVD) [15] on Si wafers. Difficulties in producing 3C-SiC wafers by sublimation method may be due to the high temperatures used in the sublimation method, which promote the crystallisation of hexagonal and rhombohedral polytypes. Polycrystalline SiC wafers can be fabricated using sintered pressed powders or using CVD.

### 1.4.1 Epitaxial Growth

CVD is undoubtedly the most common technique for growing epitaxial SiC films. 6H-



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SiC and 4H-SiC are grown homoepitaxially on 6H-SiC and 4H-SiC wafers respectively[9,10]. 3C-SiC is usually grown heteroepitaxially on Si [18] or on 6H-SiC [19]. Growth of 3C-SiC on Si substrates has been demonstrated in the 1960s using processes that were based on carbonization of Si at high temperatures in a hydrocarbon gas [20]. The carbonisation process is self limiting; therefore growth of only very thin films, of the order of hundreds of nanometers is practical. For a thicker film, a two step deposition process is employed where; step two involves film growth using a silicon containing precursor gas [20]. However single crystalline 3C-SiC grown on Si substrates has a lot of defects due to lattice mismatch etc.

## 1.5 SILICON CARBIDE DEVICES

Silicon carbide has several unique properties (higher breakdown field, wider band-gap, lower thermal generation rate, and lower intrinsic carrier concentration) to enhanced performance in devices.

### Power MOSFETs

The breakdown electric field of SiC is approximately 8 times higher than silicon. This makes it possible to design power switching devices having correspondingly higher blocking voltages than their silicon counterparts. More importantly, the specific on-resistance (i.e. resistance-area product) of a power device scales inversely as the cube of the breakdown field, so the on-resistance of SiC power MOSFETs are 100-200 times lower than comparable devices in silicon [21].

### Lateral Power MOSFETs

The maximum blocking voltage of vertical power devices in SiC is presently limited by the thickness of commercially available epi-layers. The developed lateral power MOSFETs in 3C-SiC exhibit blocking voltages of 2.6 kV.

### Schottky Barrier Diodes

Schottky barrier diodes (SBD's) are attractive as power rectifiers because they do not store minority carriers in the on-state, and therefore can be switched off quickly with negligible reverse current. It is widely felt that SBD's will be the first SiC power devices to go into commercial production. The fabricated SBD's on 4H-SiC that exhibit blocking voltages of 1720 V.



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### Microwave Devices

The high saturated drift velocity, high breakdown field, and high thermal conductivity of SiC make it an ideal material for high-power microwave amplifiers in the 1-10 GHz regime. Two types of devices are under development: a vertical device known as a static induction transistor (SIT) and a lateral MESFET with sub-micron gate.

### IMPATT Diode Microwave Oscillators

IMPATT diodes are two-terminal semiconductor devices that generate RF power by introducing a 180° phase shift between current and voltage waveforms at microwave frequencies.

### CMOS Integrated Circuits

The first 6H-SiC CMOS digital integrated circuits completed in September 1996. A second generation was completed in March 1997. These are the first SiC CMOS circuits fabricated with an implanted P-well process, and the first to operate on a single 5V power supply [22].

### Nonvolatile Memories

The thermal generation rate in semiconductors is proportional to the intrinsic carrier concentration $n_i$, and $n_i$ decreases exponentially with band gap energy. Wide band gap semiconductors have dramatically lower thermal generation, with the thermal generation rate of 6H-SiC being about 16 orders-of-magnitude lower than silicon. This makes it possible to construct one-transistor memory cells in SiC which retain information for many years without power.

### Charge Coupled Devices

CCDs are unique MOS devices in which charge packets are shifted laterally along the semiconductor surface by appropriate clocking applied to surface electrodes. CCDs are widely used as imagers in video cameras and digital still cameras. They have developed the first CCDs in SiC, where the wider bandgap makes it possible to image scenery in the UV portion of the spectrum without being overwhelmed by visible light.

### NMOS Integrated Circuits

The low thermal generation rate in SiC makes it possible to operate integrated circuits at much higher temperatures than silicon. Their group developed the first digital integrated



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circuits in SiC in late 1993. These early circuits were implemented in enhancement mode NMOS.

### 1.6 LATERAL MOSFET

MOSFETs and thyristors had been fabricated as vertical structures with the substrate acting as an anode. In the off state, the voltage was blocked by a reverse-biased pn junction. To achieve high blocking voltage, the drift region should be lightly doped and thick. For a given device thickness, there was a maximum possible blocking voltage regardless of doping. For SiC lateral MOSFETs with a 10 μm drift region, the maximum possible voltage is 1600V. To overcome the limitations of vertical-type MOSFETs we use the lateral type MOSFET. The structure of lateral DMOSFET is as shown in Figure 1.8.

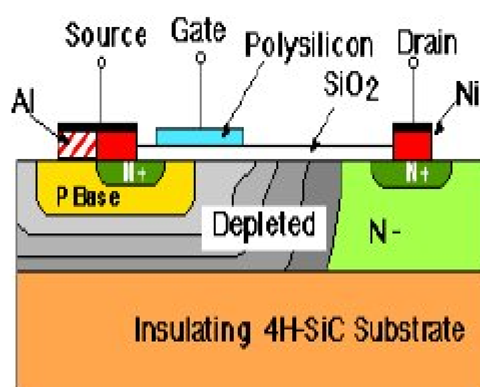


**FIGURE 1.8:** Cross section of lateral MOSFET [7].

From the figure it can be observed that the insulating substrate is of SiC. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer. Figure 1.8 shows the current voltage characteristics of lateral DMOSFET. From the characteristics, it is observed that the device withstands a maximum drain voltage of 2.6 kV. From the above discussion one can say that the device should be implemented laterally rather than vertically because there is no necessity for an increase of surface area required for the device[14].



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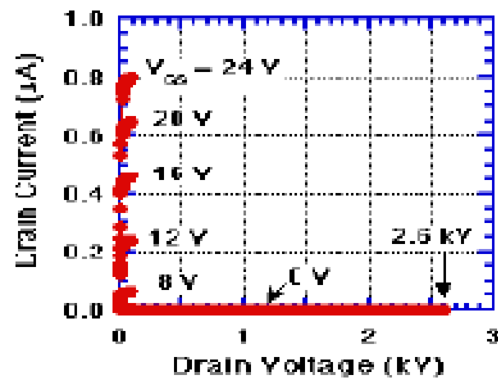


**FIGURE 1.9:** Current-voltage characteristics at room temperature [14].

## 1.7 ORGANIZATION OF THESIS

**Chapter 2** explains doping profile of $n^+$ source, p-base and drift region. Theory and working principle of Lateral Power MOSFET is given thereafter. In the later part, Energy Band Diagram and different type of charges associated with the silicon dioxide ($SiO_2$) has been discussed. At the end, theory of Flat Band Voltage, Mobility of electron and Threshold Voltage is given.

**Chapter 3** deals with the calculation of Drain current with respect to drain voltage, firstly without the channel length modulation and current-voltage characteristic is plotted. Then channel length modulation parameter (λ) has been calculated. At last the current-voltage characteristics for Lateral Power MOSFET has been plotted with channel length modulation (λ).

In **Chapter 4** breakdown voltages has been calculated. Values of Avalanche breakdown, Punch through breakdown and Depletion width in the drift region is calculated.

Finally **Chapter 5** describes the conclusion and future work.



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## CHAPTER 2

# THEORY OF LDMOS

## 2.1 INTRODUCTION

3C-SiC lateral double-implanted metal-oxide semiconductor (LDMOS) field effect transistor is fabricated in a lightly doped n-epilayer on an insulating 4H-SiC substrate. The p-base region and the $n^+$ -source region are diffused through a common window defined by the edge of the polysilicon gate. The p-base region driven in deeper than the $n^+$ source. The difference in the lateral diffusion between the p-base and $n^+$ source regions defines the surface channel region. The channel length L is determined by the higher rate of diffusion of the p-dopant (e.g boron), compared to the $n^+$ dopant region(e.g phosphorous) of the source. The channel is followed by a lightly doped drift region.

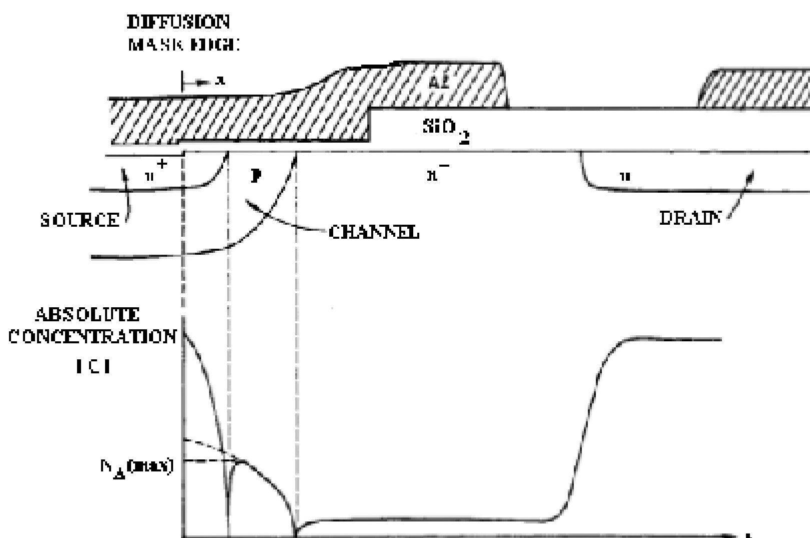


**FIGURE 2.1:** LD-MOS Structure and doping profiles [23].

## 2.2 DOPING PROFILE

A typical doping profile along the semiconductor surface for the device is shown in Fig2.1. The peak p-base doping is an parameter for the doping profile because it controls the threshold voltage of the power MOSFET, that is, minimum voltage required to induce a surface channel. For a typical threshold voltage of 3 V for an n-channel power MOSFET, the peak concentration $N_{A(max)}$ is about $1\times10^{17}$[22]. This structure has good



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punch through control because of heavily doped p-shield. Varying $N_{Amax}$ leads to $p^+$ variations in $V_T$.

## 2.3 WORKING PRINCIPLE

The p-n junction between the p- base region and the n-drift region provides the forward blocking capability. The p- base region is connected to the source metal by a break in the $n^+$ source diffusion as shown in fig 2.2.

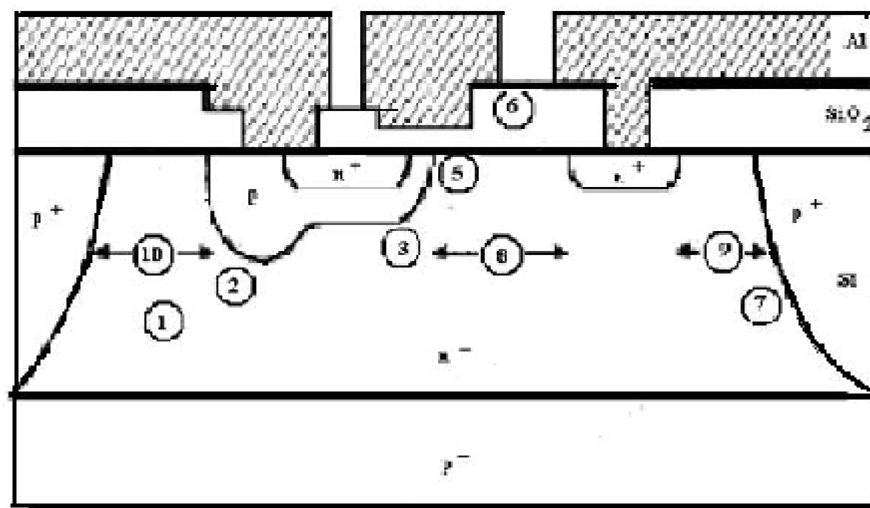


**FIGURE 2.2:** High Voltage Double Diffused MOS Structure [24].

| | | |
|---|---|---|
| 1. | Epitaxial Thickness | 25μm |
| 2. | $P^+$ contact junction depth | 5 μm |
| 3. | Channel junction depth | 4.5 μm |
| 4. | $N^+$ source-drain junction depth | 1.5 μm |
| 5. | Gate oxide thickness | 0.3 μm |
| 6. | Field oxide thickness | 1.5 μm |
| 7. | Isolation junction depth | 30 μm |
| 8. | Drain source spacing (mask) | 30 μm |
| 9. | Drain isolation spacing(mask) | 60 μm |
| 10. | Source isolation spacing(mask) | 65 μm |

This is important to establishing a fixed potential to the p-base region during device operation. If the gate electrode is externally short circuited to the source, the surface of the p-base region under the gate (i.e channel region) remains unmodulated at a carrier concentration determined by the doping level. When a positive drain voltage is applied it



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reverse biases the p-base/n-drift region junction. This junction supports the drain voltage by the extension of a depletion layer on both sides. Because of the higher doping level of the p-base region, the depletion layer extends primarily into the n-drift region. Its doping concentration and width must be chosen in accordance with the criteria for the avalanche breakdown of the p-n junctions. Higher drain blocking voltage capability requires a lower drift region doping and a greater width.

Threshold voltage ($V_{th}$) is defined as the gate-to-source voltage ($V_{GS}$) at the onset of the current conduction. The electrons flow through the surface channel and then through the bulk in the lightly doped epitaxial "drift region" to the drain contact. This drift region contributes an additional component to the on resistance. The additional resistance is much lower than that for a series MOSFET since current spreads into the n-type bulk[24].

After depleting through the epilayer, the depletion region continues to move laterally toward the drain. In the blocking state, the depletion layer spreads mainly into the lightly-doped drift region. Once the depletion region reaches the insulating substrate, it continues spreading toward the drain. Here, the maximum voltage is not limited by the thickness of the layer so there is no necessity for increase of surface area required for the device [14]. The lateral extent of the depletion layer region is not limited by the thickness of the epilayer [25].

## 2.4 MOS PHYSICS

### 2.4.1 Ideal MIS Diode

The metal-insulator semiconductor (MIS) structure is shown in fig 2.3, where d is the thickness of the insulator and V is the applied voltage on the metal field plate. The energy band diagram of an ideal MIS structure of p-type semiconductor for V=0 is shown in fig 2.3.

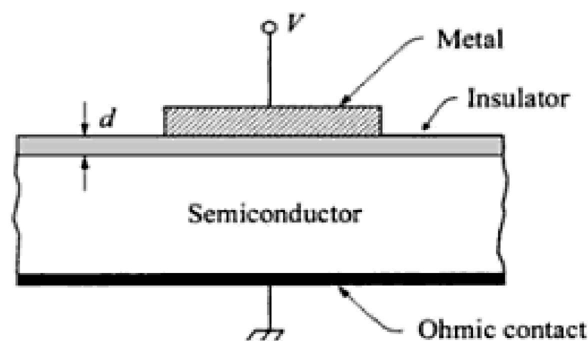


**FIGURE 2.3:** Metal-Insulator-Semiconductor (MIS) diode.



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An ideal MIS diode is defined as follows.

(1) At zero applied bias energy difference between metal work function $\Phi_m$ and the semiconductor is zero, or the work-function difference $\Phi_{ms}$ is zero:

$$\phi_{ms} = \phi_m - \left( x + \frac{E_g}{2q} + \psi_B \right) \qquad \text{for p-type} \qquad ...(2.1)$$

$$\phi_{ms} = \phi_m - \left( x + \frac{E_g}{2q} - \psi_B \right) \qquad \text{for n-type} \qquad ...(2.2)$$

Where $\phi_m$ is the metal work function, $\chi$ the semiconductor electron affinity, $\chi_i$ the insulator electron affinity, $E_g$ the bandgap, q is electronic charge $\phi_B$ the potential barrier between the metal and the insulator, and $\psi_B$ the potential difference between the Fermi level $E_F$ and the intrinsic Fermi level $E_i$. In other words, the band is flat (flat-band condition) when there is no applied voltage.

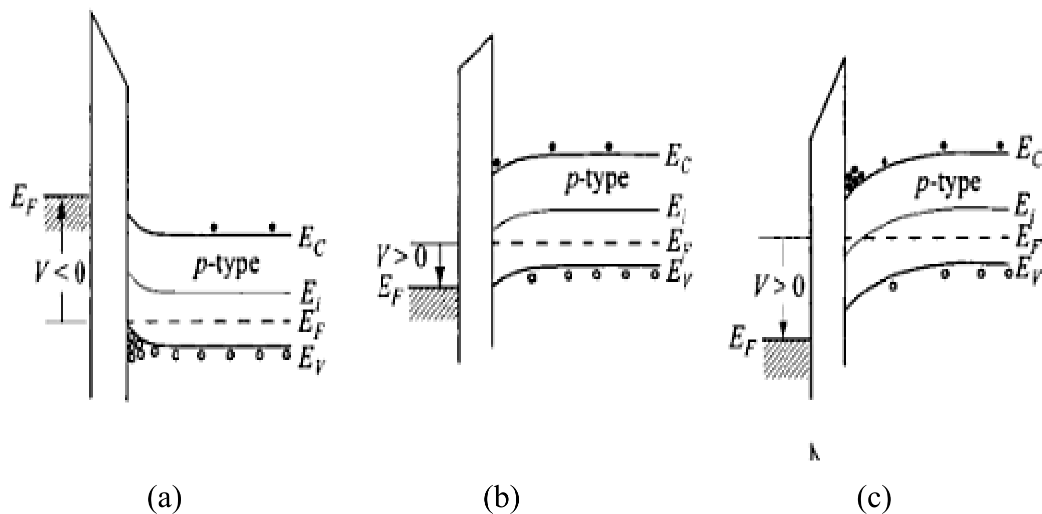
(2) The only that can exist in the structure under any biasing condition are those in the semiconductor are and those with the equal but opposite sign on the metal surface adjacent to the insulator.

(3) There is no carrier transport through the insulator under dc biasing conditions or the resistivity of the insulator is infinity.

When the ideal MIS diode is biased with positive or negative voltages, basically three cases may exist at the semiconductor surface as shown in fig 2.3.

The three cases are as follows:

(a) Accumulation; (b) Depletion; (c) Inversion.




(a) (b) (c)

**FIGURE 2.4:** Energy Band diagram (p-type) for an ideal MIS diode when V≠ 0 [26].



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For the p-type semiconductor, when a negative voltage (V<0) is applied to the metal plate, the top of the valence band bend upward and is closer to the Fermi level fig 2.4(a). For an ideal MIS diode , no current floes in the structure , so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference ($E_F$-$E_V$), this band bending causes an accumulation of majority carriers (holes) near the semiconductor surface. This is the "accumulation" case. When a small positive voltage (V>0) is applied, the bands bend downward, and the majority carriers are depleted fig 2.4(b). This is the "depletion" case. When a larger positive voltage is applied, the bands bend even more downward so that the intrinsic level $E_i$ at the surface crosses over the Fermi level $E_F$. Fig 2.4(c). At this point the number of electrons (minority carriers) at the surface is larger than that of the holes, the surface is thus inverted, and this is the "inversion" case.

### 2.4.2 Surface Space Charge Region

Surface space charge region to the intrinsic Fermi level $E_i$ as shown. At the semiconductor surface $\psi = \psi_S$, and $\psi_S$ is called the surface potential. The electron and hole concentration as a function of $\psi$ are given by the following relations:

$$n_p = n_{p0} \exp(q\psi / kT) = n_{p0} \exp(\beta\psi) \quad ....(2.3)$$

$$p_p = p_{p0} \exp(-q\psi / kT) = p_{p0} \exp(-\beta\psi) \quad ....(2.4)$$

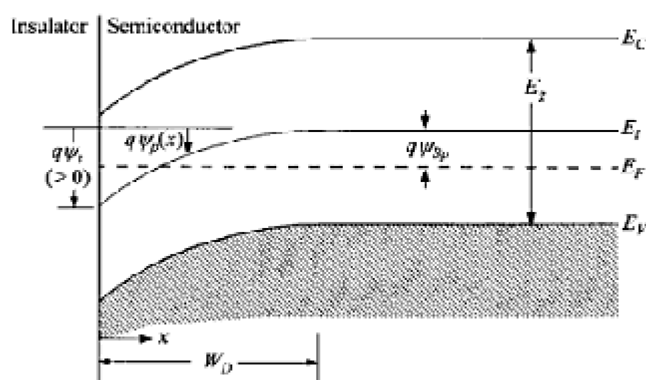


**FIGURE 2.5:** Energy- band diagram at the surface of p-type semiconductor. (a) Accumulation occurs at $\psi_S$<0. (b)Depletion occurs when $\psi_B > \psi_s$>0. (c) inversion occurs when $\psi_s > \psi_B$ [26].



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Where $\psi$ is positive when the band is bent downward $n_{p0}$ and $p_{p0}$ are the equilibrium densities of the electrons and holes, respectively, in the bulk of the semiconductor, and β=q/kT. At the surface the densities are

$$n_s = n_{p0} \exp(\beta\psi_s) \quad ...(2.5)$$

$$p_s = p_{p0} \exp(-\beta\psi_s) \quad ...(2.6)$$

It can be summarises as:

$\psi_S<0$ accumulation of holes (bands bend upward)

$\psi_S=0$ flat-band condition

$\psi_B>\psi_s>0$ depletion of holes (bands bend downward)

$\psi_s=\psi_B$ midgap with $n_s= p_s= n_i$ (intrinsic concentration)

$\psi_s>\psi_B$ inversion (electron enhancement, bands bend downward)

Strong inversion begins at a surface potential,

$$\psi_{S(inv)} = 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \quad ...(2.7)$$

## 2.5 INTERFACE TRAPPED AND OXIDE CHARGES

**Interface Trapped charges:** It has been shown that interface-trapped charges $Q_{it}$ exits within the forbidden gap due to the interruption of the periodic lattice structure, at the surface of a crystal. Shockley and Pearson experimentally found the existence of $Q_{it}$ in their conduction measurement. Measurements on clean surfaces in an ultra -high-vacuum system confirm that $Q_{it}$ is very high of the order of $10^{12}$ atoms $cm^{-2}$.

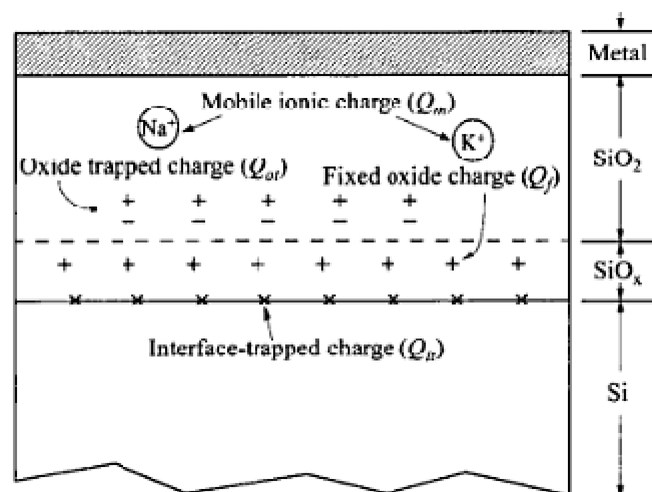


**FIGURE 2.6:** Terminology for charges associated with thermally oxidized silicon [26].



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An interface trap is considered a donor if it can become neutral or positive by donating (giving up) an electron. An acceptor interface trap can become neutral or negative by accepting an electron. Fig 2.6 shows the distribution of these charges.

**Oxide Charges:** Oxide charges include the oxide fixed charge $Q_f$, the oxide trapped charge $Q_{ot}$, and the mobile ionic charges $Q_m$, as shown in fig 2.6. The fixed oxide charges $Q_f$ has the following properties: It is fixed and cannot be charged or discharged over a wide variation of $\psi_s$. Its density is not greatly affected by the oxide thickness or by the type of concentration of the impurities in the semiconductor; it is generally positive and depends on oxidation and annealing condition [26].

## 2.6 FLAT BAND VOLTAGE

To illustrate the Flat Band voltage, a simple MOS transistor has been taken in this section. Let us consider a transistor connected to external voltage source as in fig 2.7. The drain is short-circuited to the source, making $V_{DS}$=0. The external source-body bias $V_{SB}$ is fixed at a positive value $V_{SB1}$, since the source is short-circuited to the drain, acts as the reverse bias for the pn junction. Let us consider the pn junction associated with the source. The shadow around the junction indicates the presence of the depletion region i.e., a region where most mobile charges have been removed, with holes in the body having moved away from the junction toward the negative terminal of the $V_{SB}$ of the battery and electrons in the $n^+$ region having moved in the opposite direction toward the positive terminal of the battery. This means that, on the p side, immobile acceptor atoms are left with a net negative charge(they have been "uncovered"); also, on the n+ side, immobile donor atoms are left with a net positive charge. The total charges revealed on each side of the junction are equal in magnitude, preserving charge neutrality. Because the n+ region is much more heavily doped, only a very narrow strip need be uncovered on that side, to balance the charges on the much deeper strip on the p side. In the figure, only the depletion region on the p side is shown, and it is indicated by the depletion region on the p side is shown, and it is indicated by the shadow around the n+ region.

The depth of the depletion region is related to the charge density in it and the electrostatic potential across it, according to basic electrostatic laws. This depth is such that the resulting electrostatic potential drop across the region, along with the *contact potentials* at the contacts to the device, and the external bias $V_{SB}$ algebraically add up to zero. A depletion region will exist even with $V_{SB} = 0$; the potential across it balances the contact potentials around the loop. If $V_{SB}$ is



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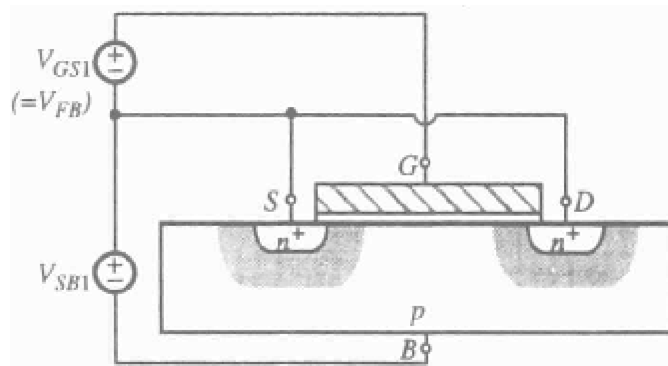
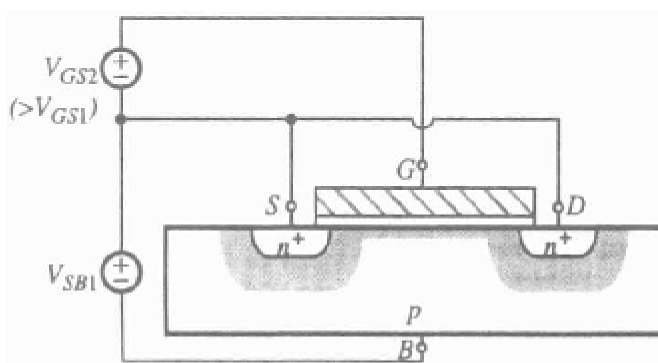
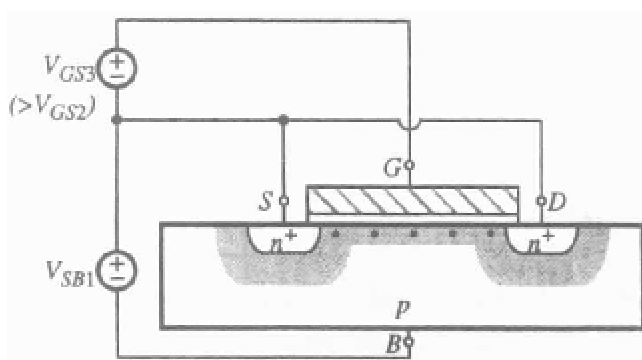
increased, the depletion region will deepen accordingly to support the extra drop. It can be shown that since the $n+$ region is much more heavily doped than the $p$ region, practically all the potential drop across the depletion region occurs on the $p$ side.




(a) Flat Band




(b) Depletion




(c) Inversion

**FIGURE 2.7:** MOS transistor with $V_{DS}=0$ and successively increased values of $V_{GS}$ [27].



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On the drain side, another depletion region forms in the same way. Since the drain is short-circuited to the source, the drain-body junction sees the same reverse bias as the source-body junction, and thus both depletion regions have the same depth. If $V_{GS}$ is sufficiently negative, positively charged holes can be attracted at the surface (the substrate interface to the oxide); this condition is known as *accumulation*. If the surface is accumulated, and subsequently $V_{GS}$ is made less and less negative, the accumulation will become lighter and lighter, and at a certain value of $V_{GS}$ it will disappear altogether, leaving the body neutral. This is the *flat-band* condition, assumed in Fig. *2.7a.*. The corresponding value of $V_{GS}$ is called the *flat-band voltage* and is denoted by $V_{FB}$. At the flat-band condition, each immobile negatively charged acceptor atom in the body outside the two depletion regions is, on average, covered by a mobile, positively charged hole, resulting in macroscopic neutrality.

If $V_{GS}$ is now made more positive than its flat-band value, the charge on the gate will become more positive, too. This will tend to repel holes from the surface, resulting in a depletion region in the channel as shown in Fig. *2.7b.* This condition is called *depletion.*

If $V_{GS}$ is raised still farther, more positive charges will be placed on the gate, which must be balanced by more negative charges in the channel; to uncover the extra negative charges, the depletion region in the channel must become deeper. Assume now that $V_{GS}$ is increased to the point that the depletion region in the channel becomes almost as deep as that under the *n*+ regions. This means that the electrostatic potential at the surface (with respect to the body) is now almost the same as that on the *n*+ regions. Thus the surface becomes almost as attractive for electrons as the *n*+ regions. Electrons now enter from the *n*+ regions into the channel, next to the surface, despite the fact that the body is *p* type. The surface is now said to be *inverted,* and the electrons next to the surface what is known as an *inversion layer.* The larger the value of $V_{GS}$ the more the electrons are attracted to the surface and the "heavier" the inversion [27].

The MOSFET Flat Band voltage value is given by



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$$V_{FB} = \phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{Q_{ot}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \quad ...(2.8)$$

$C_{ox}$ is the oxide capacitance given by the equation,

$$C_{ox} = \frac{A\varepsilon}{t_{ox}}, \varepsilon = \varepsilon_0 \varepsilon_s, \quad \varepsilon_s = \text{relative permittivity of 3C-SiC} \quad ...(2.9)$$

Where $Q_f$ is the oxide fixed charges, $Q_{ot}$ is the oxide trap charge, and, $Q_{it}$ is the interface trap charge [28].

## 2.7 ELECTRON MOBILITY MODELS FOR 3C-SiC

In the 3C-SiC the samples are heteroepitaxially grown on either Si or 6H-SiC, because no 3C-SiC substrate exists. This results in large lattice mismatches (about 20% for Si substrates), and a corresponding high defect density. This coupled with the fact that there is currently little drive to establish 3C-SiC commercially (unlike the 4H and 6H SiC), results in large differences in the quality of the material reported on. The mobility [29] equation is given as,

$$\mu = \frac{C\left(\frac{N}{N_{ref}}\right)^{\alpha-\delta} + \mu_{max}}{1+\left(\frac{N}{N_{ref}}\right)^{\alpha}} cm^2/Vs \quad ....(2.10)$$

Where $\mu_{max}$, C, $N_{ref}$, α, δ are fitting parameters. The fit for the 3C-SiC mobility were found to be:

$$\mu_{max} = 650\left(\frac{T}{300K}\right)^{-2.5} cm^2/Vs \quad ...(2.11)$$

$$C = 350\left(\frac{T}{300K}\right)^{-1.5} cm^2/Vs \quad ...(2.12)$$

$$N_{ref} = 3X10^{16} cm^{-3} \quad ...(2.13)$$

$$\alpha = 0.8, \delta = 0.2 \quad ...(2.14)$$

## 2.8 THRESHOLD VOLTAGE ($V_{th}$)

In LDMOS the threshold voltage is determined by the charge distribution under the gate



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oxide in the channel region. The "*threshold*" voltage at any point in the channel can be calculated from the equation below

$$V_{th} = \phi_{ms} + 2\phi_f - \frac{\sqrt{2q\varepsilon N_{a(x)} 2\phi_f}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad ...(2.15)$$

Where $N_{a(x)}$ is assumed constant along the channel, a maximum $V_t$ will occur where $N_{a(x)}$ is maximum. We define the LD-MOS threshold voltage $V_t$=Vt(Na(max)) [24].

## 2.9 BREAKDOWN VOLTAGES

### Oxide Breakdown

This is destructive breakdown. It occurs when the electric field in the gate insulator exceeds a certain value [(about $7\times10^6$ V/cm) 0.07 V/A$^o$ in silicon dioxide]. The result is a permanent short circuit through the insulator. Static charge, such as that gate by handling devices with bare hands, is known to cause oxide breakdown. For this reason, protective devices are used at those input terminals of an MOS integrated circuit that are connected to transistor gates.

### Avalanche breakdown

The junction formed by the substrate and drain or source region will conduct a large current if the reverse bias applied to them exceeds a certain value (because the field in the junction near the surface is influenced by the presence of the gate, the above value depends on the gate potential and can be different from the predicted common pn junction theory). When the device is on, carriers, moving fast in the channel can impact on silicon atoms and ionize them, producing electron-hole pairs; this is referred to as *impact ionization.* The newly generated pairs can gain enough energy to impact on silicon atoms and produce more electron-hole pairs. This is called *avalanche effect* and is more pronounced in the pinch-off region near the drain where field can be high. Currents larger than those predicted by common device model will then flow, and the phenomenon is referred to as *channel breakdown*.

### Punch-Through breakdown

It occurs in devices with relatively short channels when the drain voltage is increased to the point that the depletion region surrounding the drain region extends through the channel to the source. The drain current then increases rapidly. Normally, punch-through does not result in permanent damage to the device [30].



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# V-I CHARECTERISTICS USING CHANNEL LENGTH MODULATION

## 3.1 DEVICE EQUATIONS

With the reference of fig.2.2 all the calculation are done for uniform doping profile in the drift region.

The current in the device is given by the relation[24]

$$I_D = \beta_o \left\{ \left[ V_{GS} - \left( V_{FB} + 2\phi_F \right) \right] V_{DS} - \frac{1}{2} V_{DS}^{\ 2} - \frac{2}{3} \gamma \left[ \left( V_{DS} + V_{SB} + 2\phi_F \right)^{\frac{3}{2}} - \left( V_{SB} + 2\phi_F \right)^{\frac{3}{2}} \right] \right\} \quad ...(3.1)$$

Where $\beta_0$ =constant for a fixed valve of doping ( µmho/Vµm)

$V_{GS}$=Gate to source voltage $=V_G$ (Source has been grounded $V_{S=0}$ volts)

$C_{ox}$ = Oxide capacitance ($F/cm^2$)

$V_{FB}$ = Flat band voltage ( volts)

$V_{DS}$ =Drain to Source voltage (volts)

$\phi_F$ = Bulk potential(volts)

$V_{SB}$ = Source to p base voltage (volts)

$\gamma$ =Body effect term

The value of different parameters for different values of doping is calculated and is given in Table 1 below:

**TABLE 3.1:** Values of different parameter against different value of doping

| S.No | Doping($N_B$) ($cm^{-3}$) | Mobility(µ) ($cm^3$/v-s) | Bulk Potential ($2\Phi_F$) (volts) | $\beta_o$ (µmho/Vµm) | γ µmho/$(volt)^{0.5}$ | $V_{FB}$ (volts) |
|---|---|---|---|---|---|---|
| 1 | $10^{16}$ | 580 | 1.815 | $1.005\times10^{-3}$ | 1.55 | 0.2863 |
| 2 | $5\times10^{16}$ | 440 | 1.899 | $0.759\times10^{-3}$ | 3.46 | 0.3278 |
| 3 | $10^{17}$ | 368 | 1.935 | $0.635\times10^{-3}$ | 4.9 | 0.3458 |
| 4 | $5\times10^{17}$ | 232 | 2.019 | $0.400\times10^{-3}$ | 10.96 | 0.3873 |
| 5 | $10^{18}$ | 192 | 2.055 | $0.331\times10^{-3}$ | 15.51 | 0.4053 |

Active Channel length L=2µm, Channel width W=100 µm

Now the current in the device for saturation part can be calculated by substituting the saturation voltage $V_{DSAT}$ for $V_{DS}$ in the eq. (3.1)



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$$V_{Dsat} = V_{GS} - (V_{FB} + 2\phi_F) + \left(\frac{\gamma^2}{2}\right)\left\{1 - \left[1 + 4\left(\frac{V_{GS} - V_{FB} + V_{SB}}{\gamma^2}\right)\right]^{\frac{1}{2}}\right\} \qquad ...(3.2)$$

## 3.2 CALCULATION OF PINCH OFF VOLTAGE ($V_P$)

By taking different values of doping, all the parameters appearing in eq. (3.1) and Table 1, the graph between $I_{DS}$ and $V_{DS}$ can be plotted as below.

For linear and saturation part without Early Voltage the graph can be plotted as:

(1) For doping, $N_B=10^{16}$ $cm^{-3}$

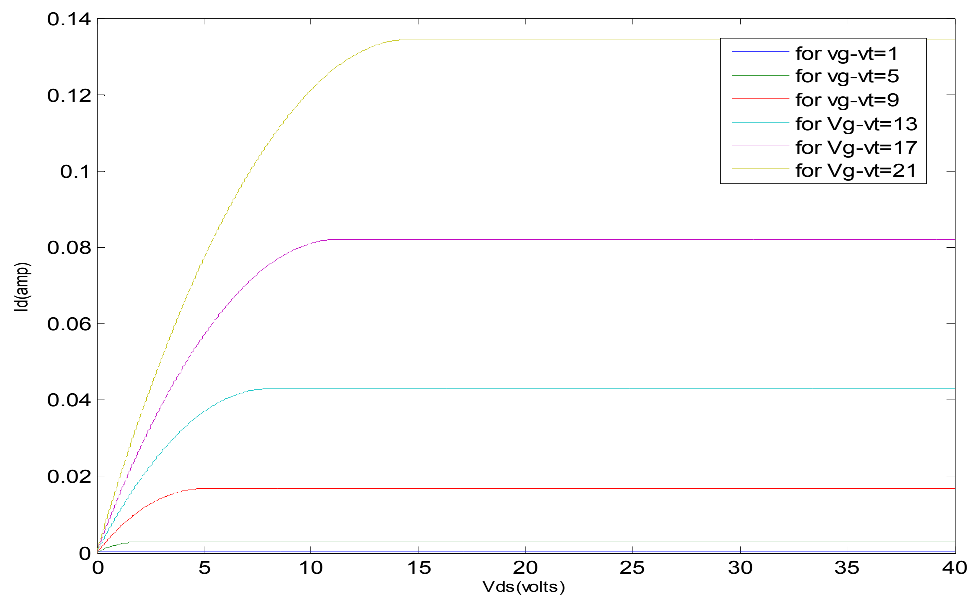


**FIGURE 3.1:** Current-Voltage Characteristic for $N_B=10^{16}$ $cm^{-3}$ without Channel length modulation ($\lambda$).

This gives the value of Pinch off Voltages for different values of $V_g$-$V_t$ as listed in table 3.1.

**TABLE 3.2:** Values of Pinch-off Voltage for different values of $V_{g-}V_t$ for $N_B=10^{16}$ $cm^{-3}$

| Value of Vg-$V_t$ (volts) | 5 | 9 | 13 | 17 | 21 |
|---|---|---|---|---|---|
| Value of Pinch off voltage(volts) | 1.984 | 4.968 | 8.120 | 11.377 | 14.707 |



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(2) For doping, $N_B=5\times10^{16}\ cm^{-3}$

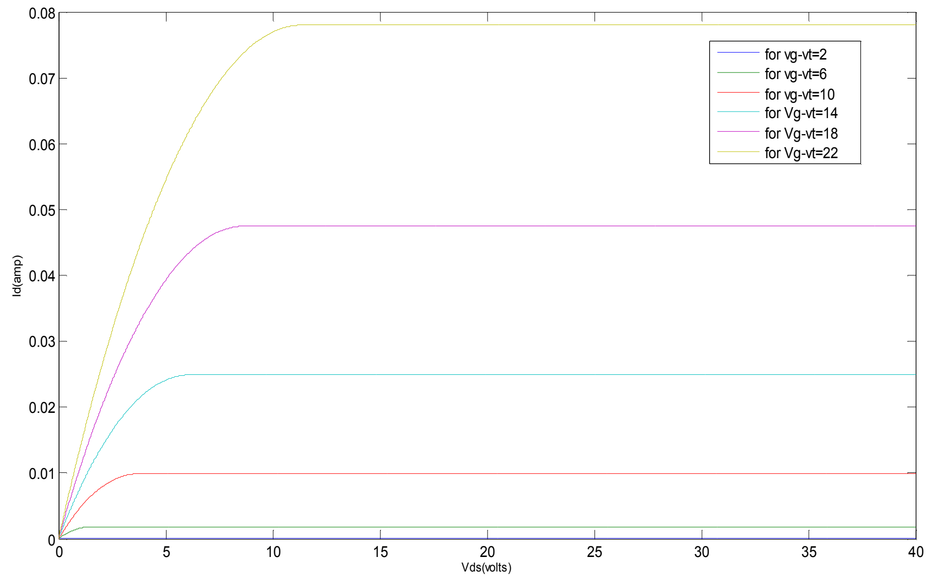


**FIGURE 3.2:** Current-Voltage Characteristic for $N_B=5\times10^{16}\ cm^{-3}$ without Channel length modulation ($\lambda$).

This gives the value of Pinch off Voltages for different values of $V_g$-$V_t$ as listed in table 3.2.

**TABLE 3.3** Values of Pinch-off Voltages for different values of $V_g$-$V_t$ for $N_B=5\times10^{16}\ cm^{-3}$

| Value of Vg-$V_t$ (volts) | 6 | 10 | 14 | 18 | 22 |
|---|---|---|---|---|---|
| Value of Pinch off voltage(volts) | 1.563 | 3.765 | 6.173 | 8.726 | 11.391 |

(3) For doping, $N_B=10^{17}\ cm^{-3}$

The value of Pinch off Voltages for different values of $V_g$-$V_t$ as listed in table 3.3.

**TABLE 3.4** Values of Pinch-off Voltage for different values of $V_g$-$V_t$ for $N_B=10^{17}\ cm^{-3}$

| Value of Vg-$V_t$ (volts) | 10 | 14 | 18 | 22 | 24 |
|---|---|---|---|---|---|
| Value of Pinch off voltage(volts) | 1.252 | 3.054 | 5.049 | 7.194 | 9.459 |



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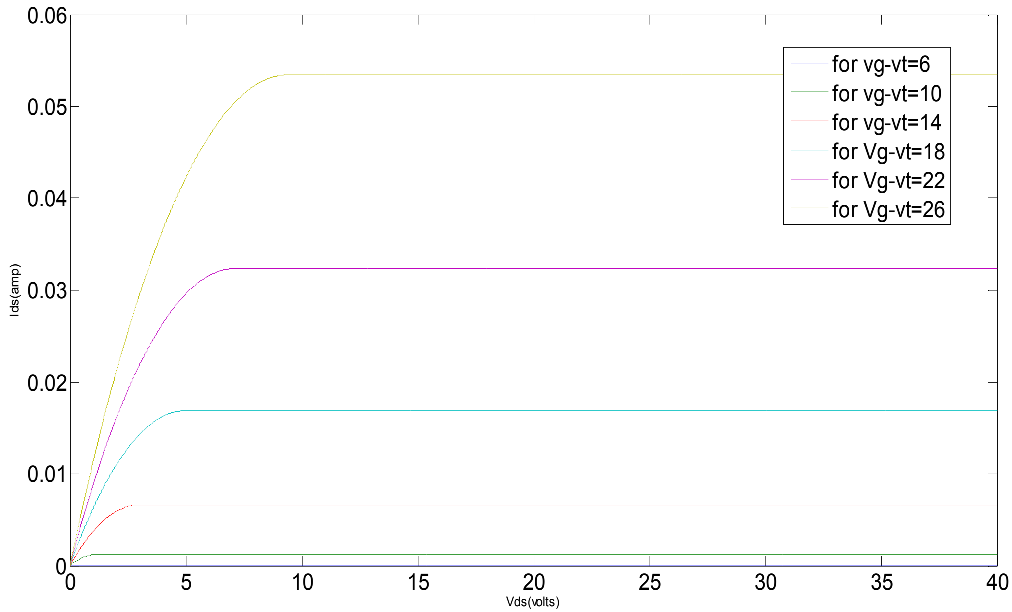


**FIGURE 3.3:** Current-Voltage Characteristic for $N_B=10^{17}$ $cm^{-3}$ without Channel length modulation (λ).

(4) For doping, $N_B=5\times10^{17}$ $cm^{-3}$

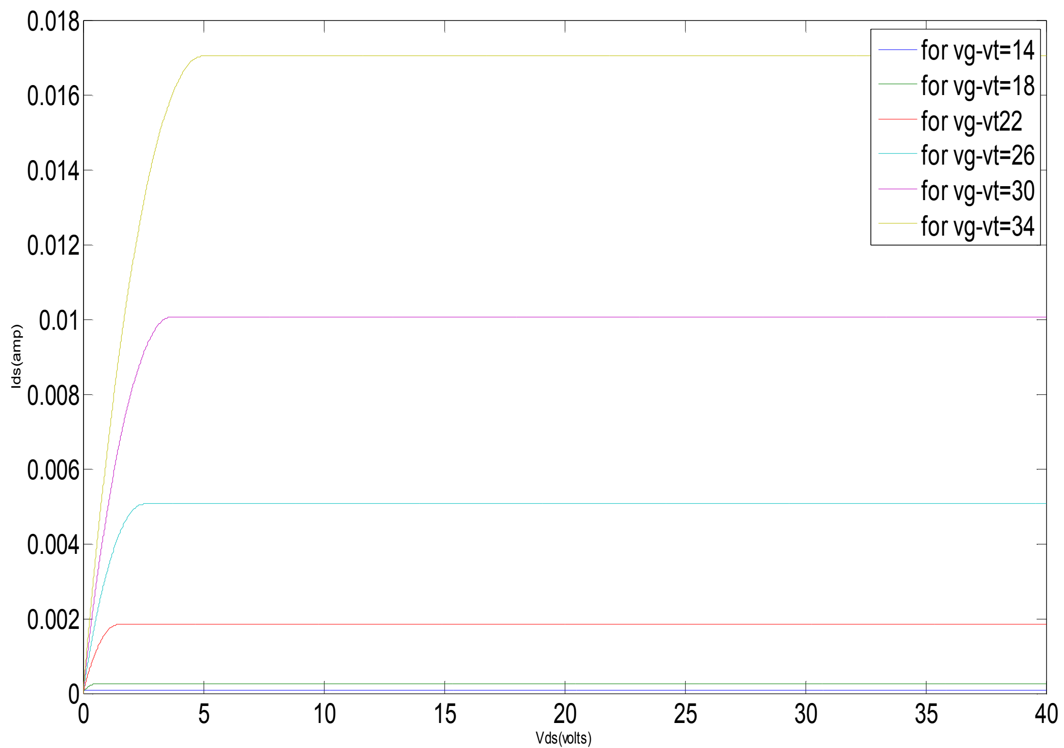


**FIGURE 3.4:** Current-Voltage Characteristic for $N_B=5\times10^{17}$ $cm^{-3}$ without λ

This gives the value of Pinch off Voltages for different values of $V_g$-$V_t$ as listed in table 3.4.



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**TABLE 3.5** Values of Pinch-off Voltage for different values of $V_g$-$V_t$ for $N_B$=5×10$^{17}$ cm$^{-3}$

| Value of Vg-$V_t$ (volts) | 18 | 22 | 26 | 30 | 34 |
|---|---|---|---|---|---|
| Value of Pinch off voltage(volts) | 0.523 | 1.484 | 2.556 | 3.727 | 4.988 |

(5) For doping, $N_B$=10$^{18}$ cm$^{-3}$

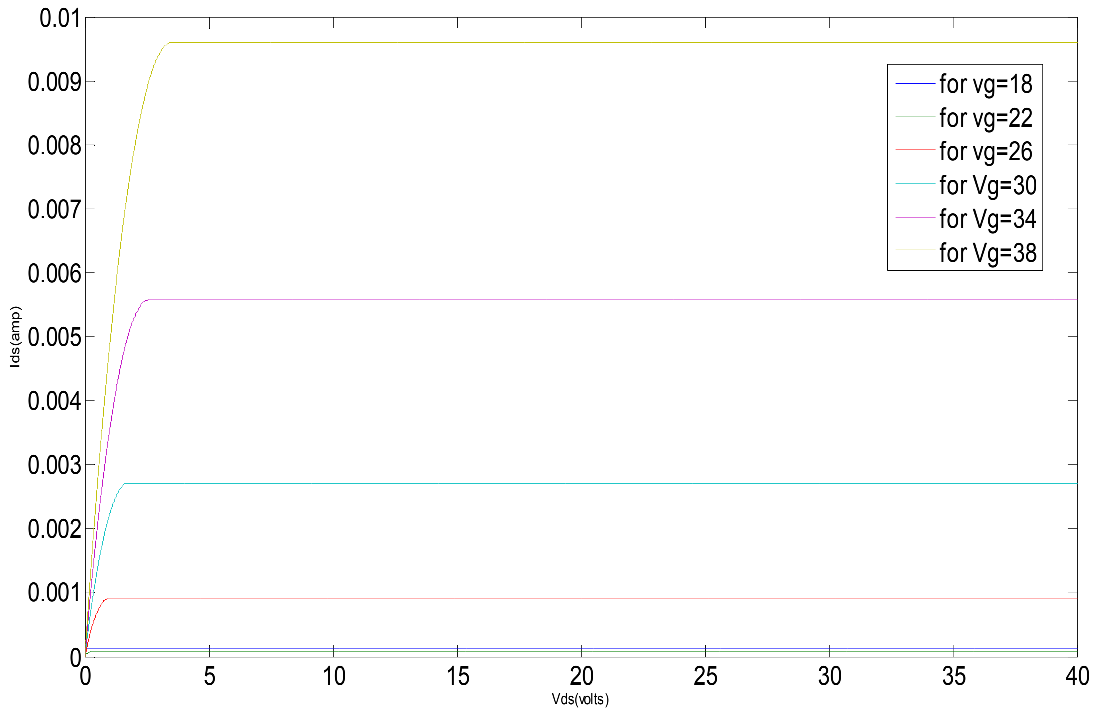


**FIGURE 3.5:** Current-Voltage Characteristic for $N_B$=10$^{18}$ cm$^{-3}$ without Channel length modulation (λ).

This gives the value of Pinch off Voltages for different values of $V_g$-$V_t$ as listed in table 3.5.

**Table 3.6** Values of Pinch-off Voltage for different values of $V_g$-$V_t$ for $N_B$=10$^{18}$ cm$^{-3}$

| Value of Vg-$V_t$ (volts) | 22 | 26 | 30 | 34 | 38 |
|---|---|---|---|---|---|
| Value of Pinch off voltage(volts) | 0.284 | 0.976 | 1.745 | 2.582 | 3.483 |

After identifying the pinch off points on the graph we draw a tangent at that point and then we can calculate the Early Voltage to get the channel length modulation parameter lambda λ by extra plotting the tangent backward.



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### 3.3 Determination of λ [30] (Channel Length Modulation Parameter)

$$\lambda = \frac{1}{|-V_A|} \qquad \text{...(3.3)}$$

(1) For doping, $N_B=10^{16}\ cm^{-3}$

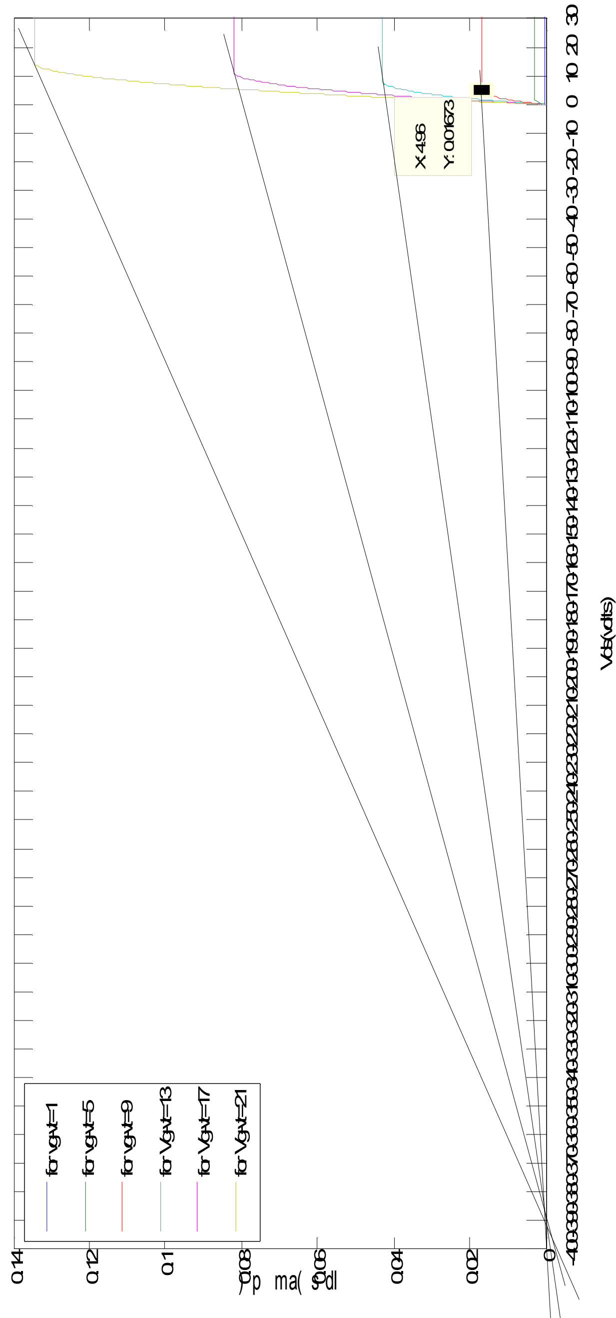


**FIGURE 3.6:** Plot of Tangent at Pinch-off voltage for $N_B=10^{16}\ cm^{-3}$

This gives value of $V_A$= -390 volts => $\lambda$ = 0.002564 $volt^{-1}$



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(2) For doping , $N_B$=5×10$^{16}$ cm$^{-3}$

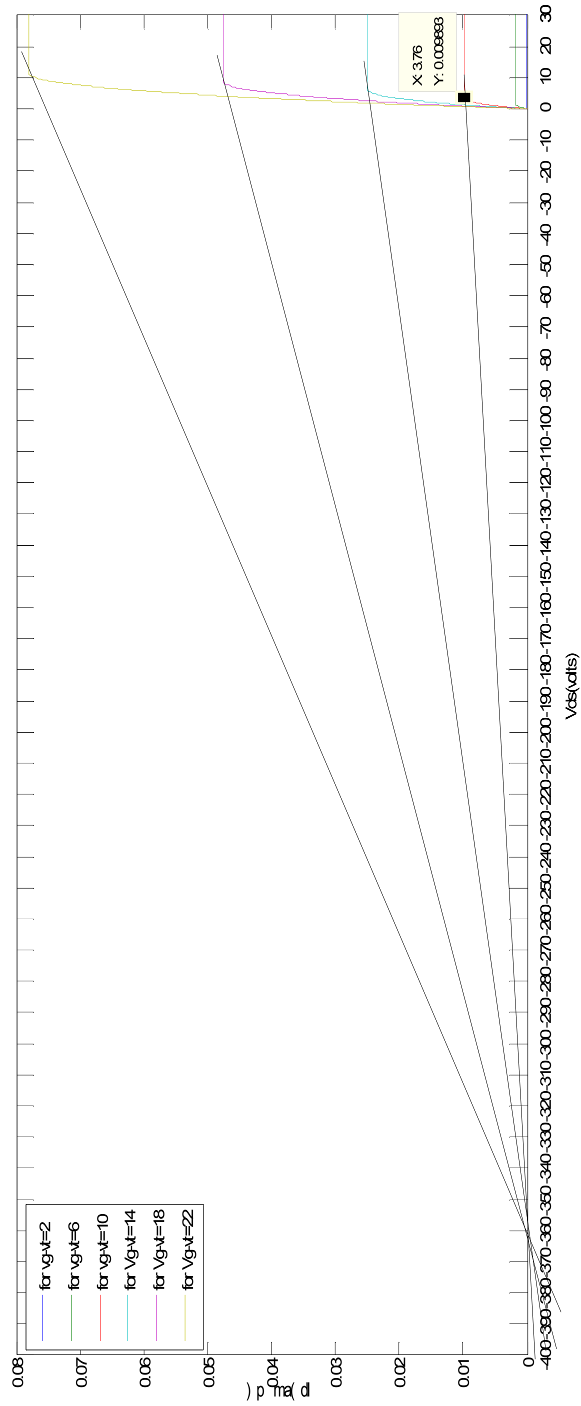


**FIGURE 3.7:** plot of tangent at Pinch-off voltage for $N_B$=5×10$^{16}$ cm$^{-3}$

This gives value of $V_A$= -362volts => $\lambda$ = 0.002762 volt$^{-1}$



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(3) For doping, $N_B=10^{17}$ $cm^{-3}$

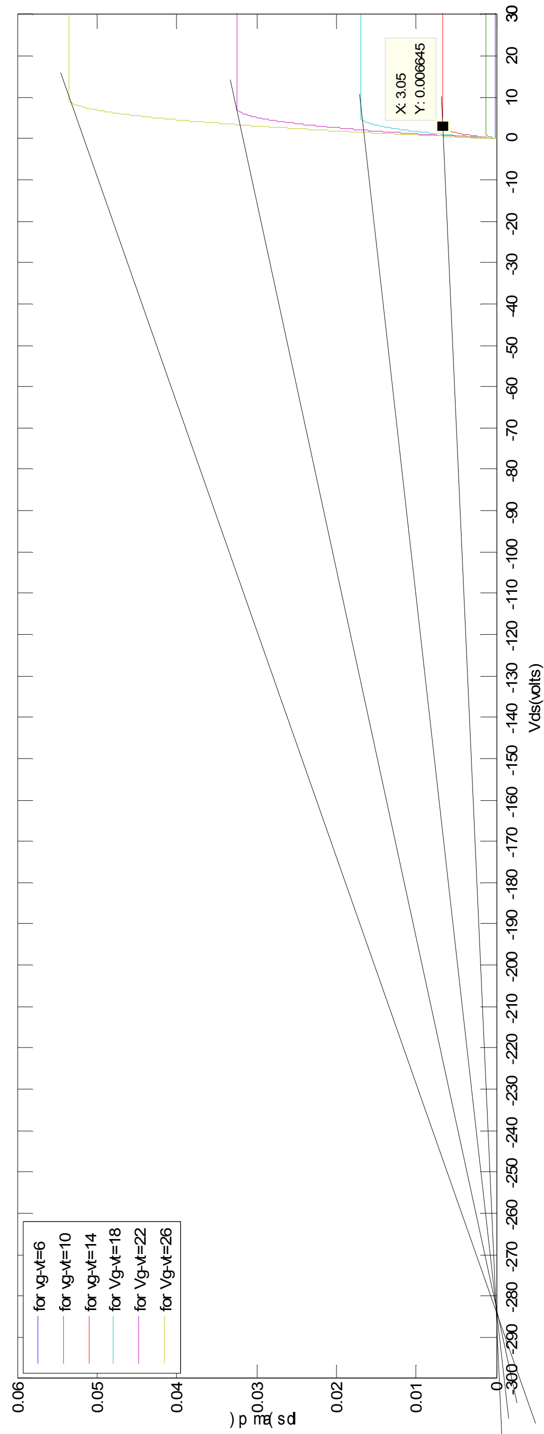


**FIGURE 3.8** Plot of Tangent at Pinch-off voltage for $N_B=10^{17}$ $cm^{-3}$

This gives value of $V_A$= - 282 volts => $\lambda$ = 0.003546 $volt^{-1}$



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(4) For doping, $N_B=5\times10^{17}\ cm^{-3}$

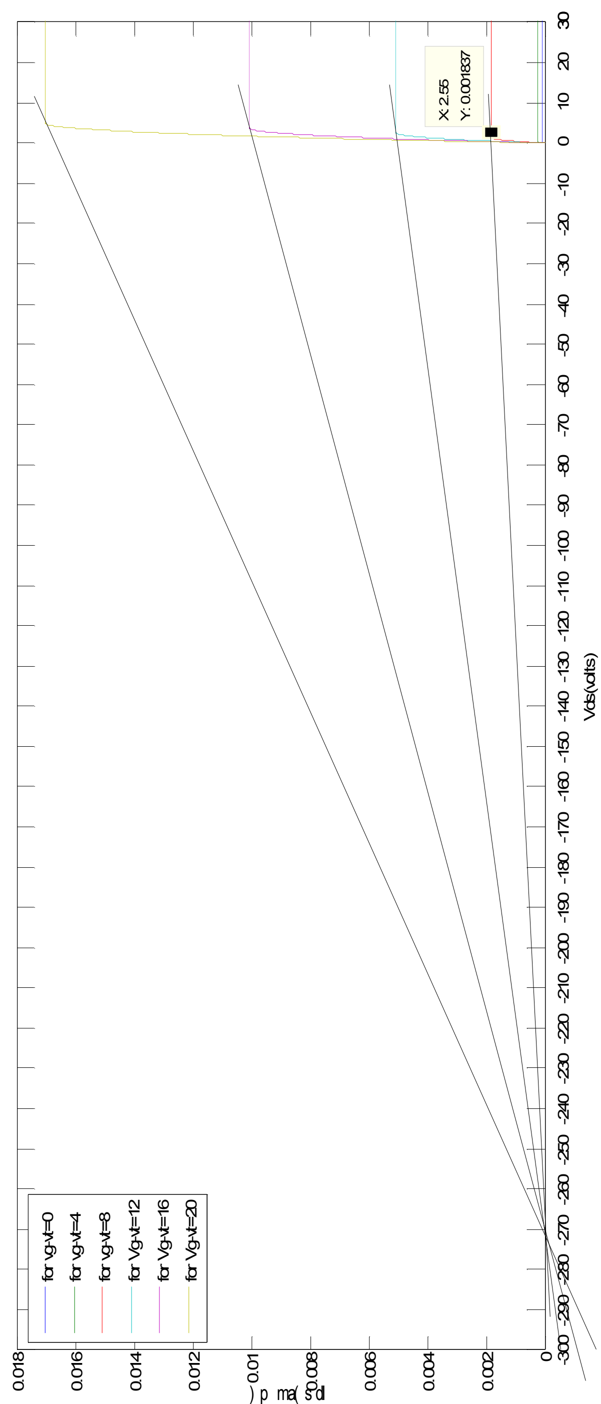


**FIGURE 3.9:** Plot of Tangent at Pinch-off voltage for $N_B=5\times10^{17}\ cm^{-3}$

This gives value of $V_A = -271$ volts => $\lambda = 0.0037\ volt^{-1}$



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(5) For doping, $N_B=10^{18}\ cm^{-3}$

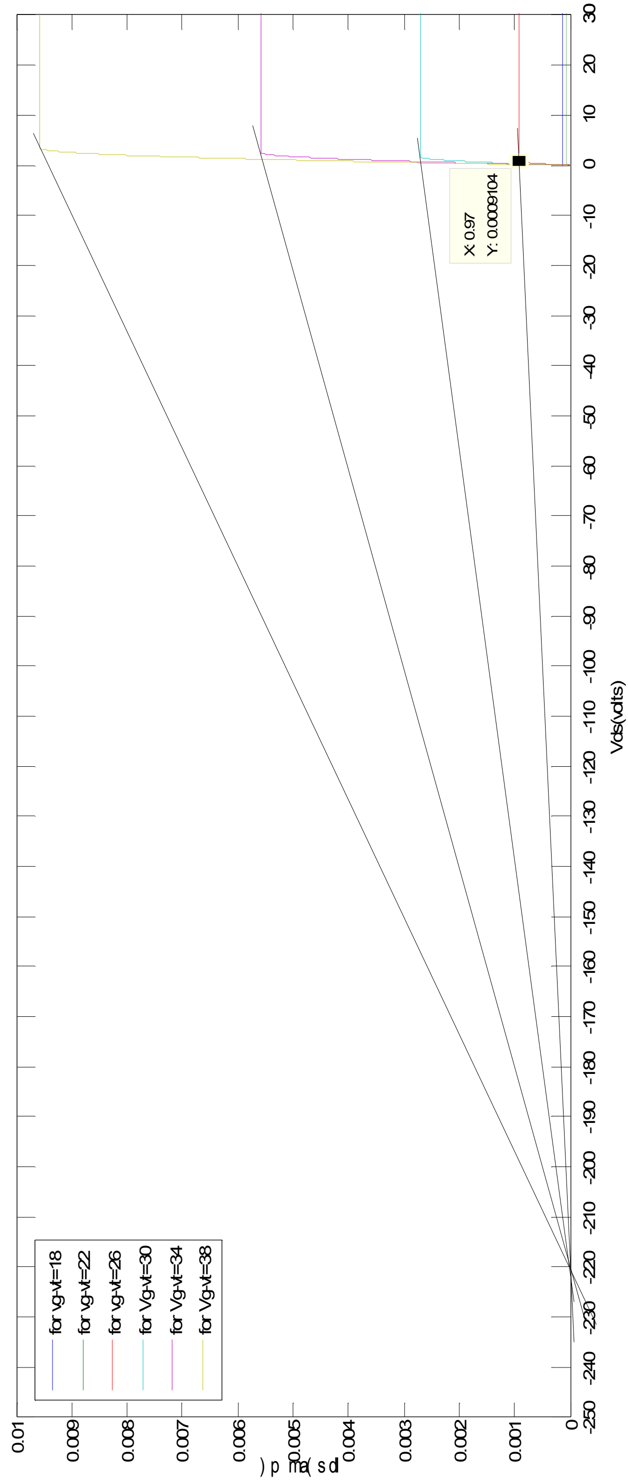


**FIGURE 3.10:** Plot of Tangent at Pinch-off voltage for $N_B=10^{18}\ cm^{-3}$

This gives value of $V_A$= - 220 volts => $\lambda$ = 0.004545



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### 3.4 Plotting of final Current-Voltage characteristics of linear and saturation part including λ

(1) For doping, $N_B=10^{16}$ cm$^{-3}$

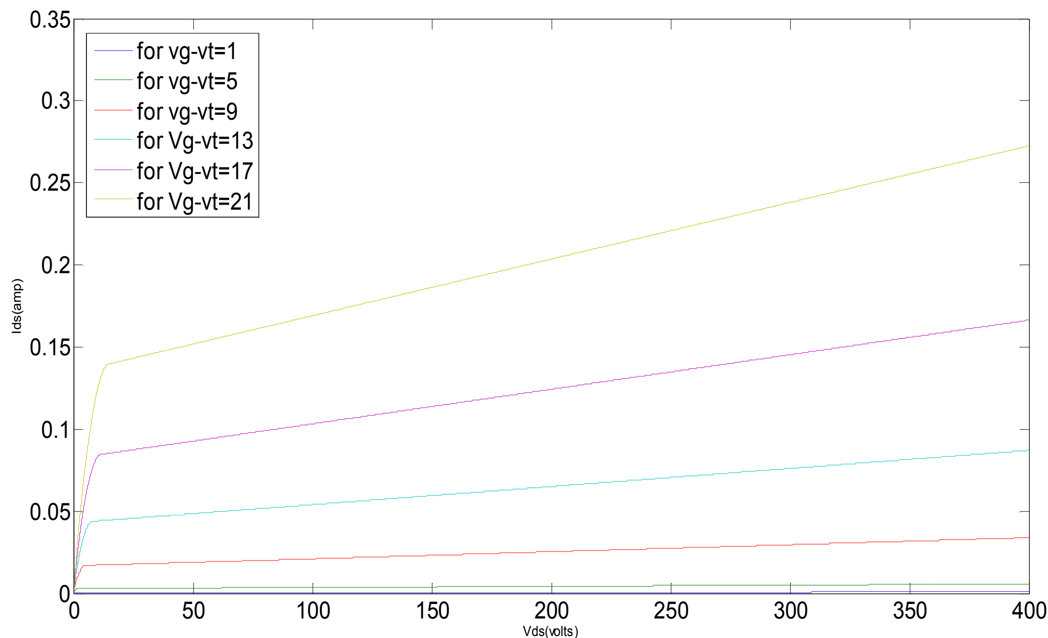


**FIGURE 3.11:** Current-Voltage Characteristic for $N_B=10^{16}$ cm$^{-3}$ with λ

(2) For doping, $N_B=5\times10^{16}$ cm$^{-3}$

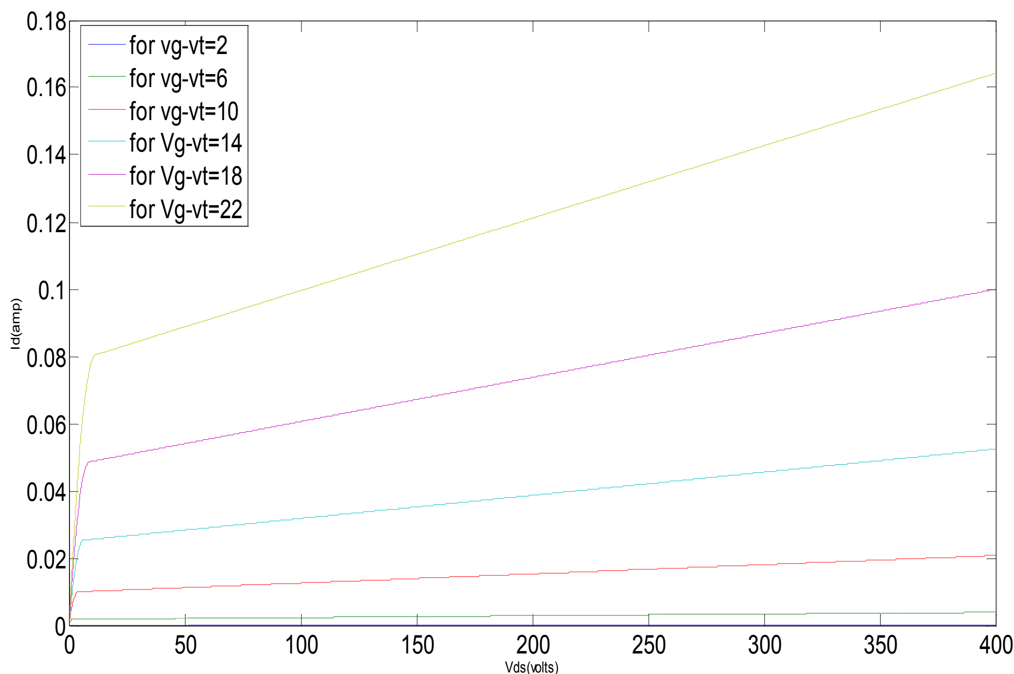


**FIGURE 3.12:** Current-Voltage Characteristic for $N_B=5\times10^{16}$ cm$^{-3}$ with λ



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(3) For doping, $N_B=10^{17}$ $cm^{-3}$

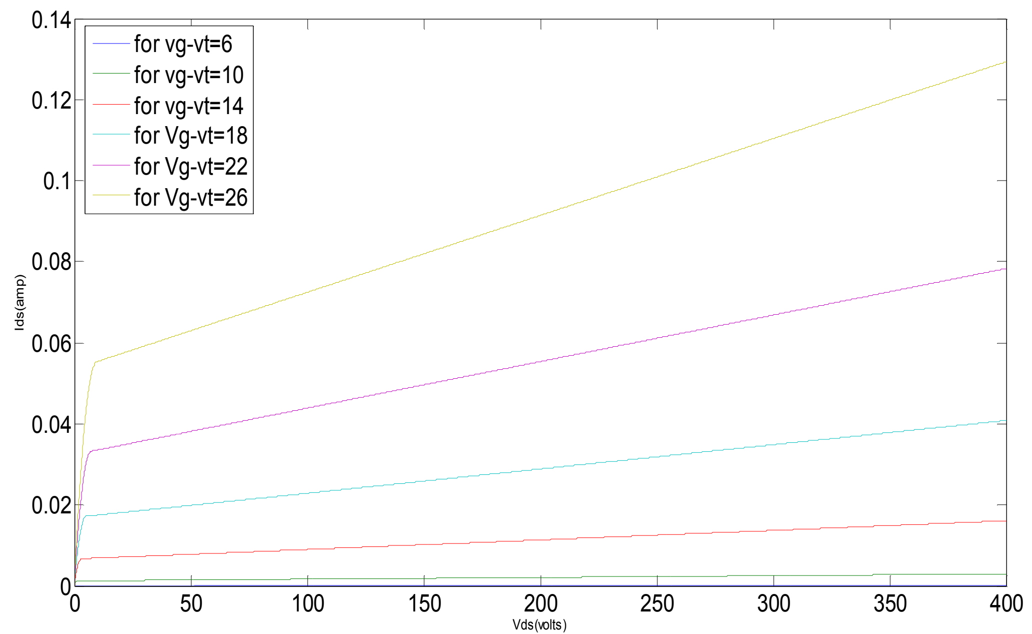


**FIGURE 3.13:** Current-Voltage Characteristic for $N_B=10^{17}$ $cm^{-3}$ with $\lambda$

(4) For doping, $N_B=5\times10^{17}$ $cm^{-3}$

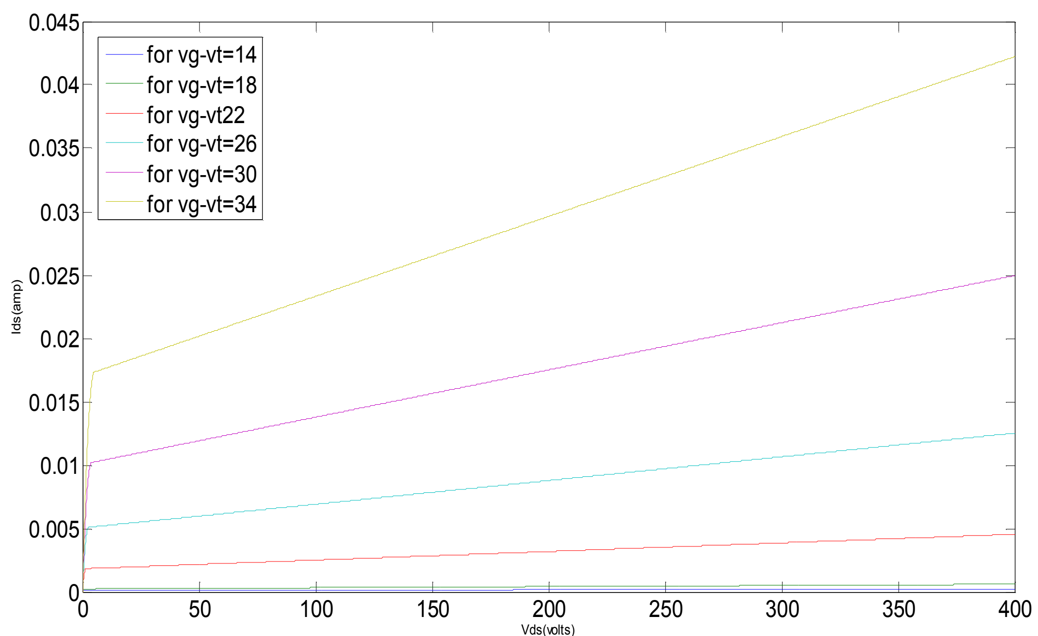


**FIGURE 3.14:** Current-Voltage Characteristic for $N_B=5\times10^{17}$ $cm^{-3}$ with $\lambda$



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(5) For doping, $N_B=10^{18}$ $cm^{-3}$\

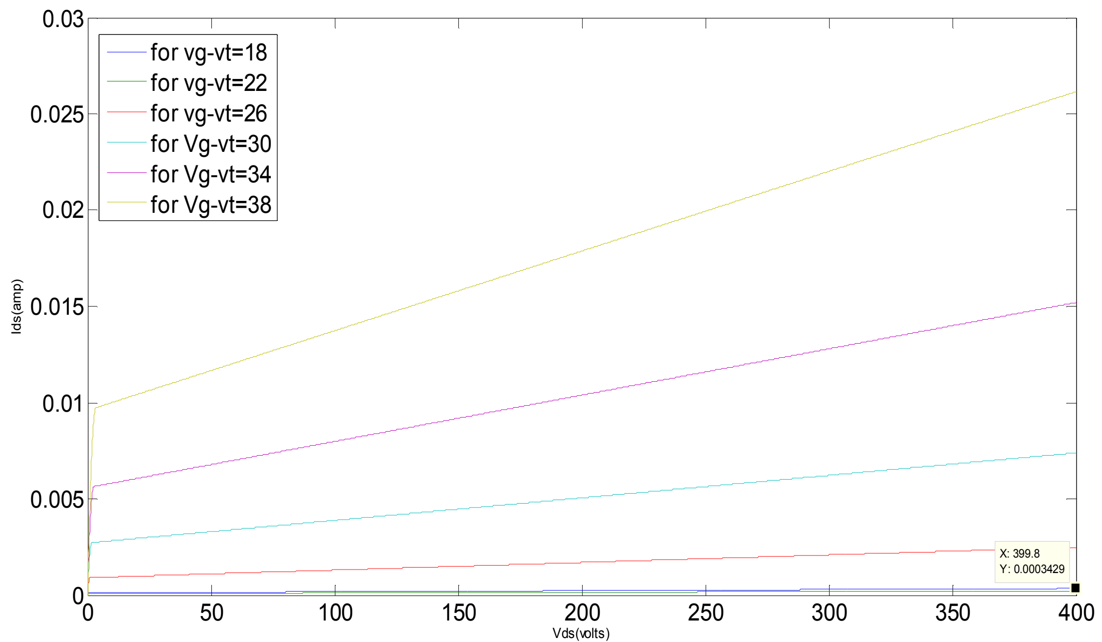


**FIGURE 3.15:** Current-Voltage Characteristic for $N_B=10^{18}$ $cm^{-3}$ with λ

The value of λ for different values of doping is tabulated in table 3.6

**TABLE 3.5:** Values of λ for different value of doping.

| S.No. | Doping Value $N_B$ ($cm^{-3}$) | Value of λ ($volts^{-1}$) |
|---|---|---|
| 1 | $10^{16}$ | 0.002564 |
| 2 | $5\times10^{16}$ | 0.002762 |
| 3 | $10^{17}$ | 0.003546 |
| 4 | $5\times10^{17}$ | 0.00370 |
| 5 | $10^{18}$ | 0.004545 |

From the above table it is clear that the value of λ is increas as we increase doping level in the p-base region. The value of doping ( $N_B$) against λ is plotted as



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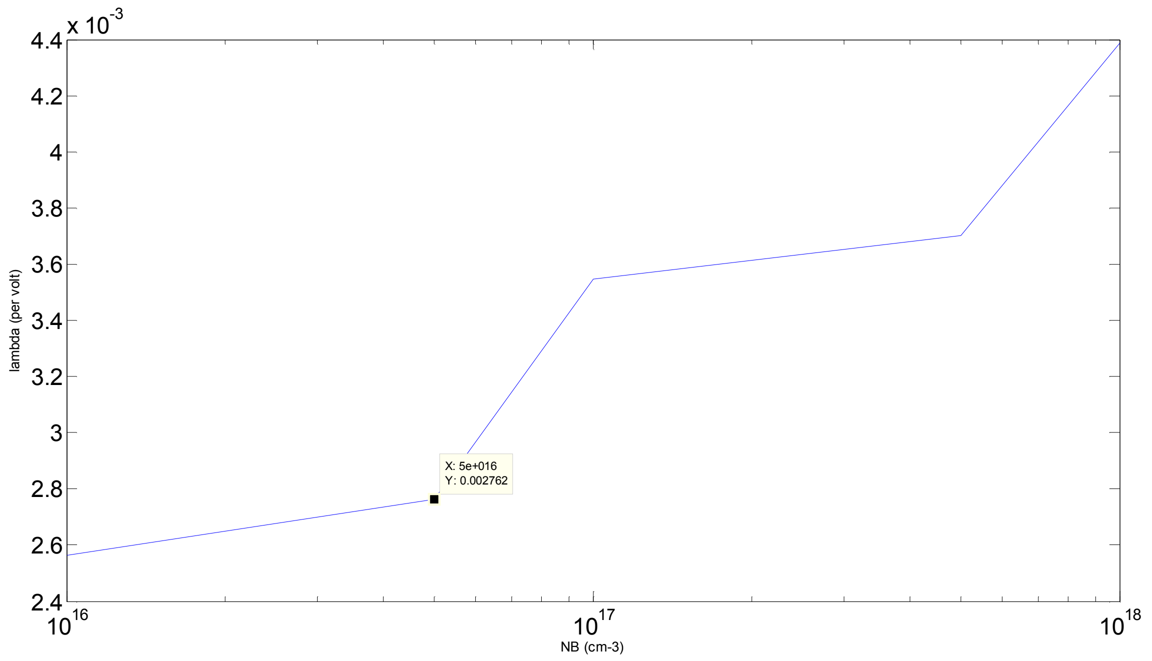


**FIGURE 3.16:** Plot of Doping versus Lambda (λ)

Above graph shows that value of λ increases with increase in doping level.



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# CHAPTER 4

## BREAK DOWN VOLTAGES AND DEVICE DESIGN CALCULATION

### 4.1 CALCULATION OF BREAK DOWN VOLTAGE

The relation for the Avalanche Breakdown voltage is given by [31]

$$BV = \varepsilon_s . E_{C_r} \left[ \frac{E_{C_r}}{2qN_D} + \frac{1}{C_{ox}} \right] \quad ...(4.1)$$

Where $E_{C_r}$ = Electric field produced at break down voltage $BV$

$N_D$ = Doping of the drift region

$C_{ox}$= Oxide capacitance

$E_{cr}$ = Critical electric field

Critical electric field for the 3C-SiC is given as [32]

$$E_{C_r}{}^{3C-SiC} = 1.5X10^4 N_D{}^{0.131} V/cm \quad ...(4.2)$$

And $w = \sqrt{\dfrac{2\varepsilon_s (V_{BPT} + V_{bi})}{qN_D}}$ ...(4.3)

Where $V_{bi}$ is the built in potential of the p-base and n-drift region

$V_{BPT}$ is the Punch through breakdown voltage

W is the depletion width in drift region

So, by substituting the values of $N_D$ from $10^{16}$ $cm^{-3}$ to $10^{18}$ $cm^{-3}$, the calculated value of break down voltages and depletion width can be tabulated as,

**TABLE 4.1** Values of Critical Electric Field, Avalanche Breakdown voltage, Punch-through Breakdown voltage and corresponding Depletion Width in the drift region.



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| S. No | Doping($cm^{-3}$) | Critical Electric Field $E_C$(V/cm) $\times 10^6$ | Breakdown voltage (kvolts) | Punch Through voltage (kvolts) | Depletion width (μm) |
|---|---|---|---|---|---|
| 1 | $10^{14}$ | 1.023 | 28.085 | 25 | 517.9 |
| 2 | $3.0\times10^{14}$ | 1.182 | 12.522 | 11 | 198.35 |
| 3 | $3.5\times10^{14}$ | 1.206 | 11.173 | 10 | 175 |
| 4 | $5\times10^{14}$ | 1.264 | 8.598 | 7 | 122.56 |
| 5 | $10^{15}$ | 1.38 | 4.315 | 4 | 65.52 |
| 6 | $2\times10^{15}$ | 1.52 | 3.135 | 3 | 40.12 |
| 7 | $2.25\times10^{15}$ | 1.54 | 2.85 | 2.8 | 36.54 |
| 8 | $2.5\times10^{15}$ | 1.56 | 2.65 | 2.5 | 32.35 |
| 9 | $3\times10^{15}$ | 1.59 | 2.323 | 2 | 26.75 |

The values of breakdown voltage against doping is plotted as shown in fig 4.1.

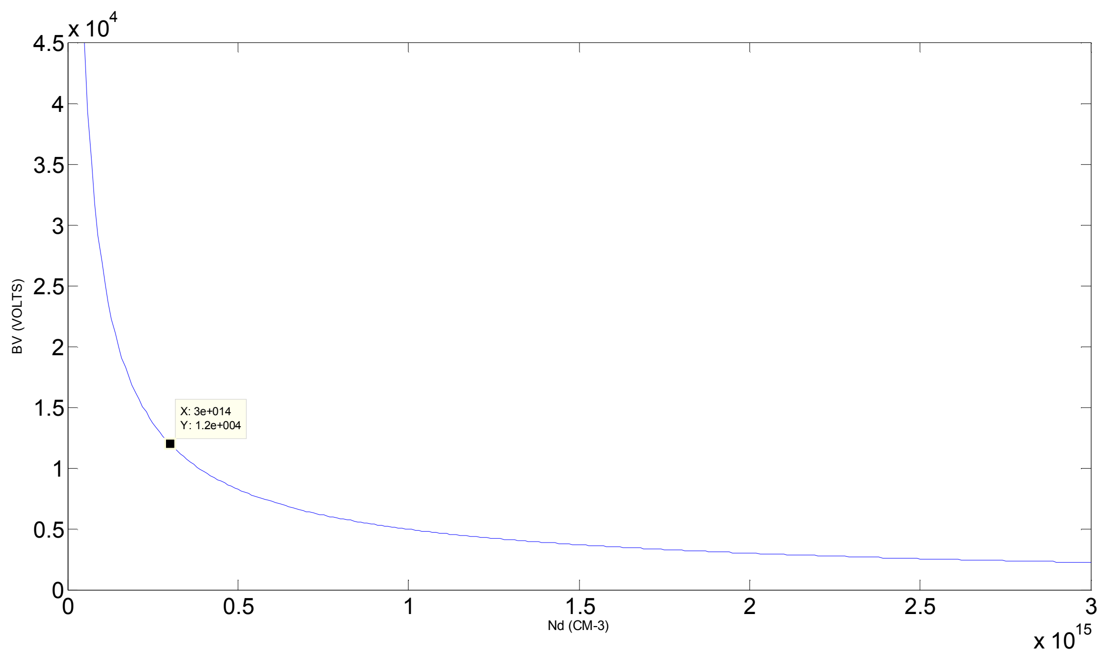


**FIGURE 4.1:** Plot of Doping versus Breakdown voltage

It is clear from the above figure that the breakdown voltage decreases as doping level in the p-base region is increased.

From the table 4.1 the doping and depletion width in the drift region can be plotted as



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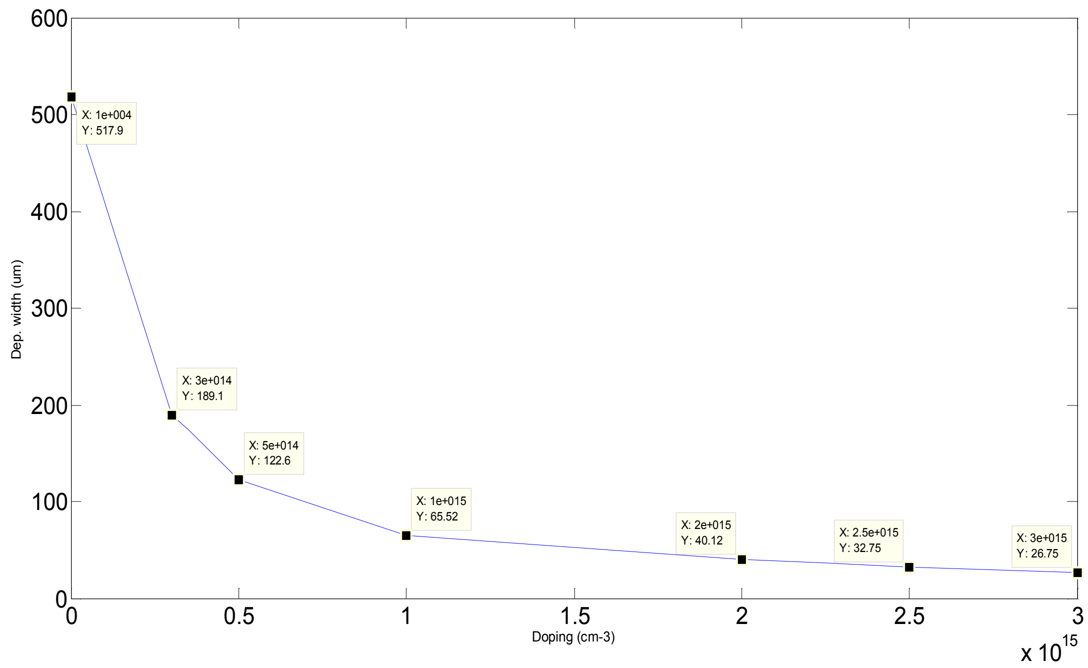


**FIGURE 4.2:** Plot of Doping versus Depletion width

From above graph it is clear that as we increase the doping concentration of drift region, the depletion width decreases.



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# CHAPTER 5

## CONCLUSION AND FUTURE WORK

Analysis of Current-Voltage characteristics for the Lateral DMOSFET shows that it can block high drain voltages without the need for thick epilayer. Under reverse bias , the depletion region surrounding the p-well has punch-through to the insulating substrate, then it moves laterally towards the drain. The lateral extent of the depletion region is not limited by epilayer thickness (uniform doping profile in drift region), but at the same time the depletion width along the channel increases.

From Table 4.1 the avalanche breakdown was found to decrease as we increase the doping in drift region ( from 28kV for $N_D=10^{14}$ $cm^{-3}$ to 2.29 kV for $N_D=3\times10^{15}$ $cm^{-3}$). If we take corresponding punch through voltages as given in the table 4.1, the value of depletion width (W=517.9µm for $V_{BPT}$=25 kV, and $N_D=10^{14}cm^{-3}$ to w=28.75 µm for $V_{BPT}$=2 kV and $N_D = 3\times10^{15}cm^{-3}$ ) was found to decrease.

The drain current is calculated including channel length modulation parameter. Table 3.1 shows that value of Flat Band voltage increases as we increase the doping of p-base. This implies that we need high gate to source voltage to start the conduction of the device. Body effect parameter also has been included. The doping of $n^+$ source and $n^+$ drain is kept very high ($10^{19}$ $cm^{-3}$).

The value of current was found to decrease (0.27 amp for $N_B=10^{16}cm^{-3}$ to 0.343 mamp, for $N_B=10^{18}cm^{-3}$ for a fixed $V_G$-$V_T$ = 21 volts), due to decreasing mobility of electron (µ = 580 $cm^2$/V.s, for $N_B=10^{16}$ $cm^{-3}$, to 192 $cm^2$/V.s, for $N_B=10^{18}$ $cm^{-3}$ ) .

**FUTURE WORK**

So for large Avalanche Breakdown and Punch Through Breakdown voltage, the doping profile of the drift region should be changed (to graded) so that the depletion width is small as compared to uniform doping to stand with high breakdown voltage, and use of thinner devices.



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