"Effect of Tunneling Conductance on the Performance of Multi Walled Carbon Nanotubes as VLSI Interconnects"

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In

VLSI Design

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CERTIFICATE & DECLARATION

I hereby declare that the work which is being presented in the dissertation titled **"Effect of Tunneling Conductance on the Performance of Multi Walled Carbon Nanotubes As VLSI Interconnects"** in the partial fulfillment of the requirement for the award of the degree of Master of Technology in VLSI Design submitted in Electronics and Communication Engineering Department of Thapar University, Patiala is an authentic record of my study carried out as under guidance of **Dr.Karamjit Singh Sandha** (Assistant Professor, ECED) during 2014-2016.

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The study has indeed helped me to explore knowledge and avenues related to my topic and I am sure this will help me in my future.

Prakhar Litoria

ABSTRACT

With the scaling in technology nodes, researchers observed that the resistivity of copper as an interconnect increase resulting in increasing its time delay. Due to these drawbacks an alternative for copper as an interconnect was required.

This report studies Carbon Nanotube (CNT) as a suitable alternative for VLSI interconnect. Different fabrication methods for the growth of CNT are discussed. Most of these fabrication approaches prefer MWCNT's growth over SWCNT; however there is a lack of proper modeling technique for analyzing MWCNT as an interconnect. This report discusses the various parameters of MWCNT as interconnect for global lengths for deep sub micron technology levels. Based on these parameters a multi conductor circuit (MCC) model is derived. As MCC model is quite complex which is difficult to analyze and simulate therefore a derived equivalent single conductor (ESC) model is proposed for simulation.

Effect of change in driver size, imperfect contact resistance and load capacitance on propagation delay at global length of 1000μm is discussed. Variation in RLC parameters with increasing length and its impact on propagation delay is also discussed and the obtained results are compared with Copper so as to prove the superiority of MWCNT for global lengths deep sub micron technology levels. The role of repeaters in reduction of delay and the impact of change of D_{min} to D_{max} ratio onto propagation delay is also studied.

Further, to study the effect of intershell tunneling conductance on the resistance and propagation delay, a model is proposed for deriving equivalent resistance by including tunneling conductance. Based on the derived equivalent resistance, previously derived ESC model is modified and simulations are performed for delay analysis. The resistance and propagation delay obtained by considering tunneling conductance are compared with the results without considering tunneling conductance and results are analyzed to observe its effect on interconnect performance.

All the calculations and simulations are carried out for 32nm, 22nm and 16nm technology nodes using ITRS 2013 parameters.

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LIST OF ACRONYMS

CNT	Carbon Nanotube
SWCNT	Single-Walled Carbon Nanotube
MWCNT	Multi-Walled Carbon Nanotube
ESC	Equivalent Single Conductor
MCC	Multi Conductor Circuit
MFP	Mean free paths
CVD	Chemical Vapour Deposition
PECVD	Plasma Enhanced Chemical Vapour Deposition
MW PECVD	Microwave plasma enhanced Chemical Vapour Deposition
AAO	Anodic Aluminum Oxide

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CHAPTER 1
INTRODUCTION

With the world moving forward towards future, the technology advancement has overpowered the expectations and its major impact is observed in the field of electronics. In the field of electronics, the device size has reduced year by year and the number of transistors on an integrated circuits (IC) have increased each year, in fact in 1965 co-founder of Intel, Gordon Moore, made a prediction from careful observation of emerging trends, that the number of transistors on per square inch of integrated circuits will double every year and this will dramatically increase the required power, and decrease the relative cost exponentially. Moore predicted that this trend will be followed in the upcoming future; however the rate at which the technology has advanced, his expectations have long been surpassed and now deep sub micron technology level has been reached.

With the technology scaling we are mostly concerned with power dissipation and propagation delay or the speed of operation of the device. The conventional approach for delay estimation is based on the fact that delays are mainly caused by three main components that are: (i) input transistors gate, (ii) interconnect line and (iii) fan-out of output gates [12].

For most of the last decade the gate delays were the main reasons for propagation delay, but since the fabrication technologies have moved to a finer submicron design level, gate delays have decreased significantly. As the numbers of transistor gates have increased, the complexity of chip also increased, and therefore at submicron technology the importance of interconnect delay increases.

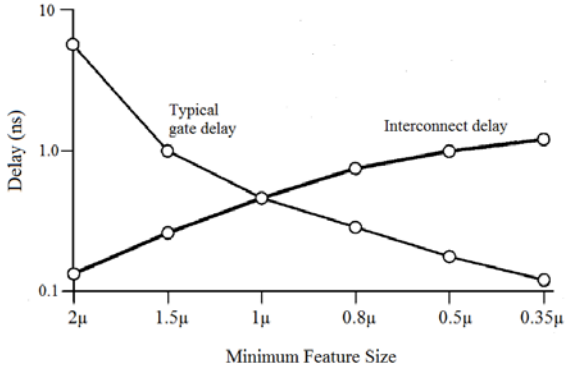


Fig. 1.1 Domination of interconnect delay over gate delay at sub micron technology.[12]

In Fig.1 1 it can be seen that at submicron technology level, the interconnect delay will start to dominate gate delay. For the better understanding of interconnect delay we first need to understand what is interconnect and how it operates?

1.1 Interconnects

Interconnect is defined as a conducting material which provides an electrical path between nodes for a given circuit formed on the chip. It can also be defined as a set of conducting wires that are needed to connect the transistor to perform the circuit function and these set of wire which connect the device on chip are called Interconnect [2,15].

The basic operation of an interconnects is to distributes the clock, power supply, I/O and other interlinking signals in an integrated circuits. The basic structure of interconnect is given by Fig.1.2.

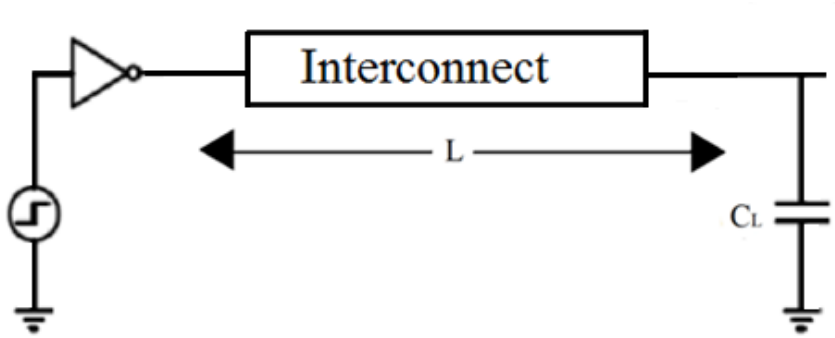


Fig.1.2 The basic structure of an interconnect.

Interconnects based on length can more simply be classified into three categories: local, intermediate, and global [15,25].

- **Local interconnects:-**

This connects gate-transistors with each other within a function block. The length of these interconnects ranges within a function block.

- **Intermediate interconnects:-**

These interconnects are longer, wider as compared to the local interconnects in order to provide lower resistance; intermediate interconnects are used to provide clock distribution as

well as signal distribution within a few functional block (intra-module) and are valid up to a typical lengths up to 0.5 to 1 mm.

- **Global interconnects:-**

These are also intra-module connections. The role of global interconnect is to provide clock and input-output signals between functional blocks. The length of global interconnects may be as long as half of the chip parameter starting from few thousand micrometers (μm) i.e. few millimeters (mm).

Starting integrated circuits (ICs) used aluminum as a material for interconnects and it proved to be a good choice due to its high conductivity and bond with Silicon dioxide. The other advantage of Aluminum was its good ohmic connection with the silicon. But with the reduction of device size, the current density of interconnect increased. The disadvantage of Aluminum interconnect was that at high current density, electron migration effect was observed. Electron migration is a process in which high current density causes alteration of shape of conductor which eventually leads to breaking of conductor [2,3,32].

1.1.1 Copper as an Interconnect

The first alternative for the problems faced by Aluminum was to change material itself and so the Copper was introduced as a replacement. The improved electron-migration resistance of the copper conductor as interconnect [17,25] resulted in high current density of copper conductor as compared to that of aluminum. Copper replaced aluminum as a VLSI interconnects as it could withstand five times larger current density when compared with aluminum. The combinations of increase in conductivity of interconnect material along with the improvement in its electron migration proved very useful. Due to all these advantages copper become the promising candidate for μm technology.

To analyze Copper as interconnect, first of all there is a need to understand its structure as shown by Fig. 1.3, in which a copper as an interconnect bar of width ‘W’, thickness ‘H’ and length ‘L’ is placed at a height ‘Y’ above the ground plane. The gap between ground plane and interconnect is filled with a dielectric material.

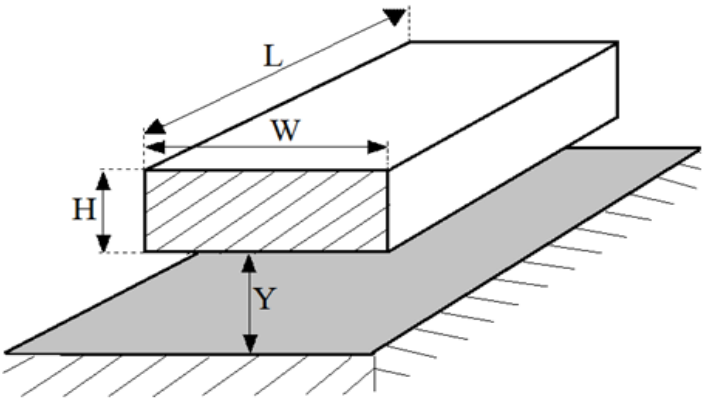


Fig. 1.3 An insight to an interconnect Structure.[12]

Using Fig. 1.3, the values of resistance, capacitance and inductance of a Copper interconnect are determined as:-

- **Resistance :-**

The parasitic resistance of an interconnect line has a significant influence on the propagation delay of a signal. Parasitic resistance of interconnect depends on the resistivity of used material (e.g., Copper, Aluminum or Gold) and the dimensions of interconnect [12]. The contacts made by interconnects contributes to contact resistance. From the interconnect line shown in Fig. 1.3, the parasitic resistance is given as:-

$$R_{Cu} = \frac{\rho L}{W.H} \qquad (\mathrm{k}\Omega) \tag{1.1}$$

Where ρ, W, H and L are the characteristic resistivity, width, thickness and length of the interconnect line.

- **Inductance :-**

In a rectangular conductor the inductance is produced due to the changing of current in the wire. In this a magnetic-field is created due to the change in current flow which induces a voltage, thus producing an inductance called self inductance [45,48] and is given by the formula:-

$$L_{Cu} = \frac{\mu}{2\pi} L\left[\ln\left(\frac{2L}{W+H}\right) + \frac{1}{2} + 0.22\left(\frac{W+H}{L}\right)\right] \qquad (\mathrm{pH}) \tag{1.2}$$

Here W, H and L are the width; height and length of the rectangular wire respectively while the μ is the permeability of the wire.

- **Capacitance :-**

Now the interconnect line is considered as a conducting plate which is parallel to a ground plane acting as another plate, both separated by a distance Y filled by a dielectric material of permittivity (ε). As a signal is passed through the interconnect it acquires some charge and acts as a parallel plate capacitance. However the thickness of interconnect (H) is quit noticeable therefore creating fringing electric fields which contributes to another type of capacitance called as fringing capacitance. So the total capacitances C_{Cu} is the summation of both parallel plate capacitances and fringing capacitance and is given as:-

$$C_{Cu} = \varepsilon \left\{ \frac{W}{Y} + \frac{\pi\left(1 - 0.0543\frac{H}{2Y}\right)}{\ln\left[1 + \frac{2Y}{H} + \sqrt{\frac{2Y}{H}}\cdot\left(\frac{2Y}{H} + 2\right)\right]} + 1.47 \right\}.L \qquad (\text{aF}) \qquad (1.3)$$

Using these RLC parameters a simple RLC circuit driven by CMOS inverter is obtained which is used for estimating the propagation delay of an interconnect line.

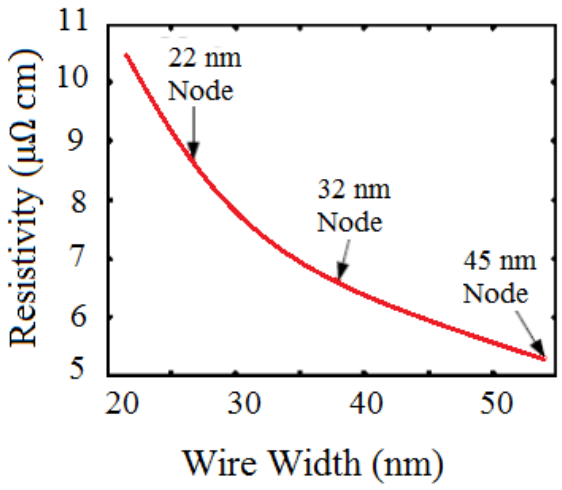


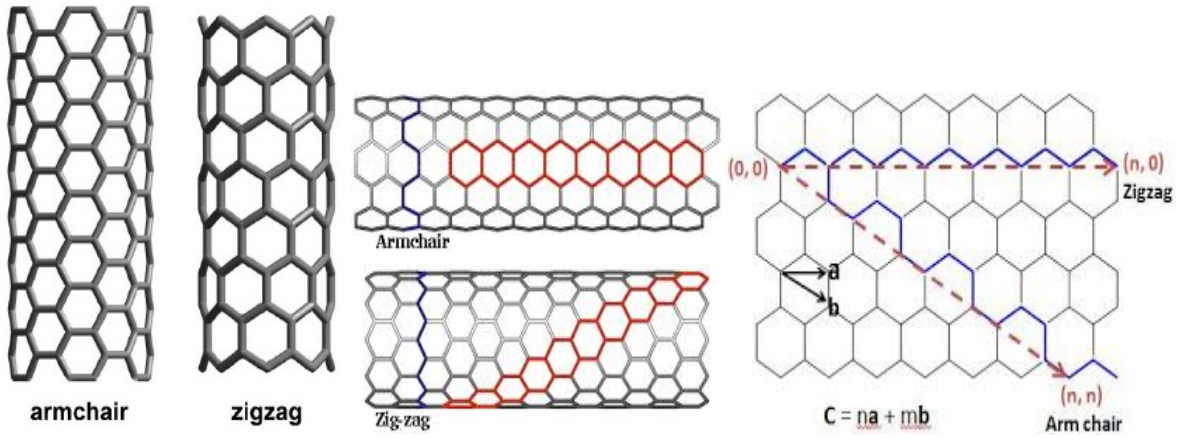
Fig. 1.4 Change in Cu interconnects resistivity with respect to technology node. [14]

With the further scaling of technology nodes, the resistivity of copper interconnect is increased due to grain boundary scattering and surface roughness phenomenon. The result is increase in propagation delay and power dissipation [14,29] which is seen Fig. 1.4.

To solve these problems, researches are going on to replace copper with other materials. The most promising candidate for replacing copper as VLSI interconnect and to overcome its disadvantages is carbon Nanotube (CNT) [25,32].

1.2 Carbon Nanotubes (CNT) as Interconnects

These are hollow cylindrical tubes with diameter in nanometers formed by rolling of graphene sheets. Based on the directions in which a CNTs is rolled, different chirality arrangements observed are armchair (metallic), zigzag (mostly semiconductor) or chiral (mostly semiconductor) [6,32]. Its structures are shown in Fig. 1.5.



(a) (b)

Fig. 1.5 (a) Metallic (armchair structure) or semi-conducting (zigzag structure)
(b) Direction of rolling of Graphene sheet to obtain desired structure. [43]

The Carbon Nanotube (CNT) as an interconnect possesses highly desirable properties, which is its current carrying capacity, high thermal conductivity and high mechanical thermal stability, [2,3].

Another advantage of CNTs over copper is that CNT has a long mean free path (MFP) ranging in several micrometers whereas copper has only 40 nm MFP at room temperature, which provides low resistance for short length interconnects [17]. Due to these properties CNTs have attracted researchers for its applicability as future VLSI interconnects [25].

On the basis of number of shells CNTs are classified into two categories:-

(a) Single-Walled CNT (SWCNT) :- comprising single cylindrical shell.
(b) Multi-Walled CNT (MWCNT) :- comprising multiple concentric cylindrical shells.

1.2.1 Single-Walled Carbon Nanotubes (SWCNTs)

SWCNT are hollow cylindrical nanometer-diameter tubes whose diameter ranges from 0.4 to 4 nm. These are made from a single graphene layer wrapped in a form of tube [19,30]. With their discovery in the early 90s, there have been a lot of researches in exploring the electrical properties and on different methods for using this technology in field of electronics. SWCNTs are distinguished based on its chirality and can either be metallic or semiconductor based on the direction in which it is rolled. The difference lies at the point where two ends of the graphene sheets are joined forming zig-zag (mostly semiconducting) or arm-chair (metallic) structure [6,43] as seen in Fig 1.5. SWCNT has a drawback that its growth type is not controllable, it can either be metallic or semiconductor and this cannot be determined beforehand. SWCNTs with metallic chirality are better conductor than Copper [17,30], but this cannot be said for SWCNTs with semiconductor chirality.

To avoid this problem MWCNTs are used which always acts as metal conductor [26]. Current carrying capacity of MWCNTs is similar to that of metallic SWCNTs. But MWCNTs are preferred over SWCNT as they are easy to fabricate and provides better control on its growth process, whereas SWCNT structure is simple and can be modeled more easily when compared with MWCNT. However, few models have been proposed for the better study of MWCNT as an interconnect [15, 31].

In general, metallic SWCNTs are best for Intermediate and local interconnects but the perfect growth is not easily possible (1 out of 3 times metallic SWCNT grown), therefore SWCNT bundles are used to enhance the chances of metallic SWCNTs. We use MWCNTs for the global and Intermediate interconnects, whereas Copper are still the best choice for local interconnects based on its resistivity [29,45].

1.2.2 Multi-Walled Carbon Nanotubes (MWCNTs)

MWCNTs are made of several coaxial cylindrical CNT shells (Fig.1.6) with each shell having different diameters; each adjacent shell is separated by a minimum distance of 0.34 nm which is the Van der Waal gap. MWCNT have different chiralities based on their rolling direction, i.e. shells in MWCNT can be semiconductor or metallic but all together acts similar to the metal conductor but with lower resistivity and better MFP [18,20,21].

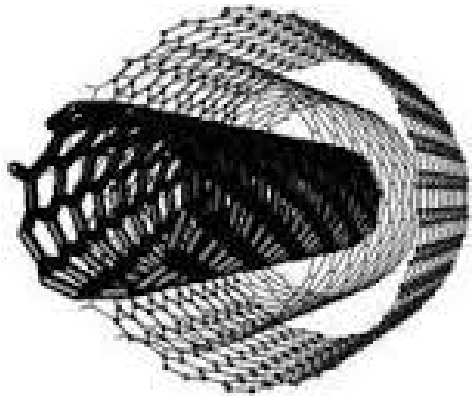


Fig. 1.6 MWCNT Structure. [20]

Before studying the parameters and electrical properties of an interconnect we first need to understand the fabrication process for the growth of carbon nanotubes (CNT).

1.3 Growth of Carbon Nanotubes

The growth techniques for carbon nanotubes are mainly characterized based on the fact that whether the growth technique uses catalyst or not. Widely followed approach for CNT growth is catalyst based approach while non catalyst approach is still in its research phase.

1.3.1 Catalyst based CNT growth

One of the most commonly practiced way or growing Carbon Nanotubes (CNT's) is by using Catalysts. Transition metals (Fe, Mo, Co, Ni) are catalysts providing a base for the growth of CNT's [4,13]. These catalyst materials can either be in solid, liquid, or gaseous state. These are deposited onto the substrate either directly by using some special techniques or by applying in the form of solution onto the substrate or even by releasing in the CVD chamber

in the form of gaseous solution [31]. To further understand the growth of CNT using catalyst we first need to understand the role of the metal catalyst.

1.3.1.1 Role of catalyst in CNT growth

Catalyst are the metal nano particles which provides a base to the decomposed carbon species which dissolves into metal catalyst, but due to a finite solubility of carbon in the metallic particles, super saturation is reached in the partical which is followed by carbon precipitating out of the catalyst and exceeding to form a carbon cylinder structure called a carbon nano tube [13,22]. The major difficulty in growth of CNT's using catalyst approach is to confine a catalyst within small patterns and at a specified location. Physical techniques such as electron gun evaporation, thermal evaporation, ion beam sputtering, and magnetron sputtering are been successfully used for the catalyst preparation [23].

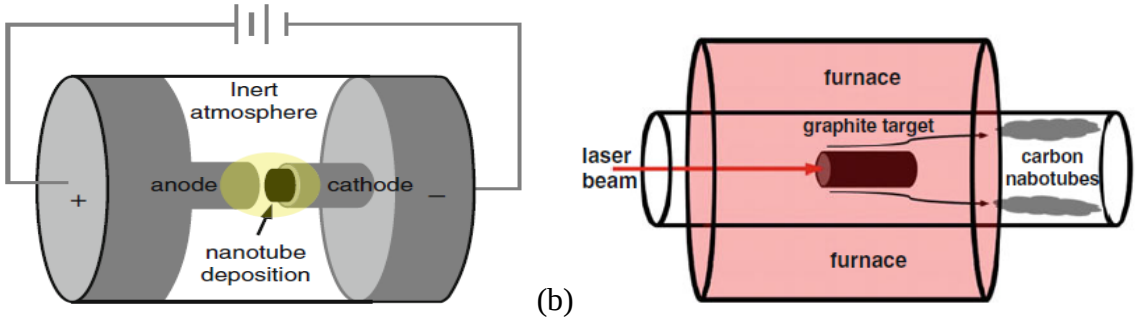
Thermodynamics and kinetic studies indicate that by combining a catalyst with a non catalytic metal in order to form an alloy will eventually increases the number of reactive sites through surface and thus enhancing the rate of growth of nanotubes. In addition to this, interactions between the catalysts and the metal electrodes is needed to be low, therefore an under layer of metal with natural thin oxide layers (Al, Cu, Ti, Ta) are used as supporting metal electrodes which also acts as a barrier layer between an substrate and catalyst metal in order to prevent back-diffusion due to ion bombardment [4,10].

The growth of CNT's directly depends on the thickness, width and the reaction rate of catalyst. Depending on the choice of the catalyst used, the diameter of the nanotubes can either be increased or decreased. The change in temperature also effects the growth of CNT i.e. as the temperature increases the diameter of the CNT also increases [23,31]. In addition to that the growth of CNTs also depends on the thickness of the oxide layer of silicon wafer surface. Below a specified oxide thickness (Y_1) no detectable growth of the nanotubes was observed, as catalyst diffuses through SiO_2 layers to reacts with the silicon substrate, eventually deactivating the role of catalyst for the growth of CNTs. For another specified oxide thickness (Y_2), above this thickness the growth depends only on CVD time. However between specified oxide thickness Y_1 and Y_2 the growth of aligned nanotube depends on both SiO_2 layer thickness and CVD time [10].

1.3.1.2 Different CNT growth techniques based on catalyst approach

1) Arc-Discharge method

One of the first carbon nanotubes examined was by Iijima [1] and was synthesized using arc discharge method (Fig. 1.7(a)). In this system a graphite rod contains metal catalysts (Fe, Co, etc.) acts as cathode and a pure graphite rod acts as anode, when a voltage supply is connected pure graphite decays releasing carbon atoms which act as a source for growth of nanotubes on catalyst. In this process a SWNT is grown in an inert atmosphere in form of soot. However to generate MWCNT having a inter-layer spacing of 0.34 nm the chamber is filled with the hydrogen gas for its optimum growth.



(a) (b)

Fig. 1.7 (a) Arc discharge setup, [1] (b) Laser Ablation setup. [10]

2) Laser Ablation

This process consists of a laser, a graphite rod acting as a target, and copper collector (with or without catalyst) on which the nanotubes are grown. These all are located inside the well sealed high temperature (around 3000 ºC) operated reactor tube with inert atmosphere (generally argon gas) as shown by Fig. 1.7(b). Now when the laser beam is focused onto the targets and carbon particles are emitted which are carried to the catalyst acting as a collector by vaporized argon gas. It's important to note that if copper uses no catalyst then MWCNT is grown and if it uses catalyst then SWCNT is grown. This process is mainly used to produce SWCNT with purity of around 90%.

The diameter of the nanotubes generated is controlled by changing the furnace temperature, metal catalyst, or the intensity of the laser [10]. If the temperature of the furnace is raised, the nanotube structures with larger diameters are formed.

However the advantage of both the laser ablation and arc-discharge techniques is to produce high quality carbon nanotubes, but both had some defects. Of the two, Laser ablation cannot be used on a large scale production whereas arc-discharge method is suitable for large scale CNT production, but the CNT produced have relatively high percentage of impurities (around 30%) mostly amorphous carbon [30]. Both these process requires the reactors to operate at a very high temperature which is difficult to achieve and maintain.

Therefore in order to achieve high quality Carbon nanotubes with minimum impurities, a new method was required, therefore Chemical Vapour Deposition (CVD) method was introduced for the growth of CNTs.

3) Chemical Vapour Deposition (CVD)

Currently, this is a most commonly used and widely accepted method for the synthesis of nanotubes, mainly because of its simplicity and low cost [10,31].

Some other advantages of CVD method are:-

(i) The nanotube formed by CVD tends to be much purer i.e. with far fewer impurities when compared with above defined techniques.
(ii) In CVD the growth is at low temperatures which make the process to be cheap and more accessible for laboratory application.
(iii) Lastly, CVD methods are suitable for growing well aligned carbon nanotubes on a desirable substrate for specific applications.

Catalyst based Chemical Vapour Deposition (CVD) process is subdivided into:

i. Thermal Catalytic Chemical Vapour Deposition
ii. Plasma Enhanced Chemical Vapour Deposition

i) Thermal Catalytic Chemical Vapour Deposition

In this method, CNTs are produced from the carbon containing source (usually gaseous) obtained by decomposition of hydrocarbons (acetylene, ethylene, propylene, methane, benzene, toluene etc.) or other carbon feedstock (polymers, carbon monoxide). The use of

pure hydrocarbon feedstock may results in deposition of substantial amount of amorphous carbon onto the substrate, therefore to avoid this the hydrocarbon feedstock are diluted with argon, hydrogen or ammonium and the diluted mixture is then fed into the furnace system and is passed over the surface of metal catalysts to form carbon nanotubes (CNT). The growth of CNT in thermal CVD method is observed at atmospheric pressure and typical temperature range of 550 –1,200 ºC [23,31].

The setup for thermal CVD method contains a horizontal reaction tube placed inside a furnace as seen in Fig. 1.8. A diluted mixture of hydrocarbon gas is passed over the catalyst placed in a reaction tube.

The parameters that affect the growth of CNT in CVD are the atmosphere, carbon source, catalyst, and growth temperature. Temperature of the furnace has a very important role to play in the growth of specific type of nanotubes i.e at low temperature (550~900ºC) growth of MWCNT is more favored, while at higher temperature (900~1200ºC) SWCNTs are more likely to grow.

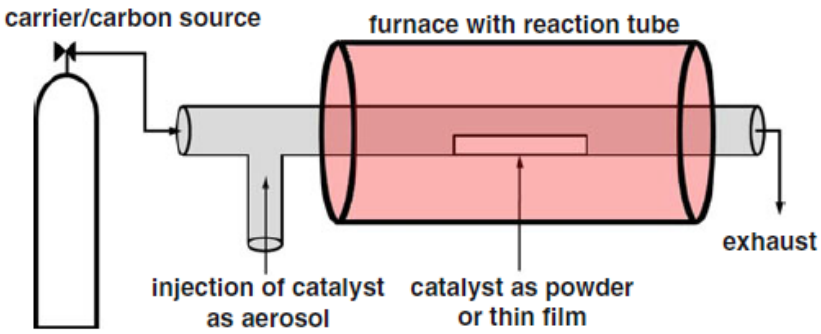


Fig. 1.8 A setup for Thermal CVD process. [10]

ii) Plasma Enhanced Chemical Vapour Deposition

As Thermal Catalytic Chemical Vapour Deposition operated at a high temperature range (550~1200ºC) and this elevated temperature in some cases cannot be tolerated by chemical layers present on wafers, therefore an alternative to thermal CVD for these special case was required, thus Plasma Enhanced Chemical Vapour Deposition (PECVD) was introduced [4]. This method operated at substantially low temperature (i.e. it ranges between room temperature and 100 ºC) however the pressure of the reactor in PECVD typically ranges from

1~20 torr [21]. Another advantage of PECVD over Thermal CVD is that CNT grown using PECVD are more vertically aligned with the substrate when compared to that grown using Thermal CVD process [4].

In this method the hydrocarbon gas is ionized to form plasma and is placed over the transition metal catalyst inside the reactor furnace. Plasma is created when a gaseous solution energizes until some electron breaks free from atom, but still travels with their nucleus.

PECVD based on the plasma energy source used are further classified into:- direct current PECVD, hot filament PECVD, radio-frequency PECVD and microwave PECVD. [10]

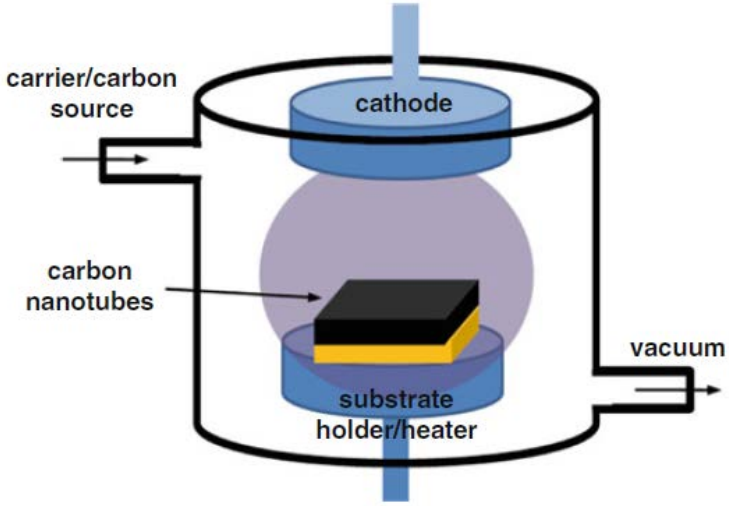


Fig. 1.9 A setup for dc PECVD process. [4]

A direct current PECVD (dc PECVD) shown in Fig. 1.9 consists of a dc plasma reactor which uses a pair of electrodes with one of the electrodes connected to a power supply while other is suspended into ground. The chamber is filled with the diluted hydrocarbon gas while the wafer with catalyst can either be placed on cathode or anode. Negative dc bias is applied to the cathode which breaks the hydrocarbon gas into plasma and the carbon nanotubes are formed onto the wafers. A heating source is placed below the electrode holding the wafer in order to obtained desired growth of the CNT. A resistive heater is used as heating source in dc PECVD, however if resistive heater is replaced by a tungsten wire suspended into the plasma stream which acts as a heating source, then the system is called hot filament PECVD system. At the end of operation all the supplies are turned off and system is treated with argon flow to cool the reactor.

The growth rate of CNT in PECVD is much slower than that in thermal CVD and PECVD can only be used for the growth of MWCNT at low temperature however growth of SWCNT is still known to grow at high temperature using arc discharge, laser ablation or thermal CVD techniques.

4) Different iteration schemes for CVD method

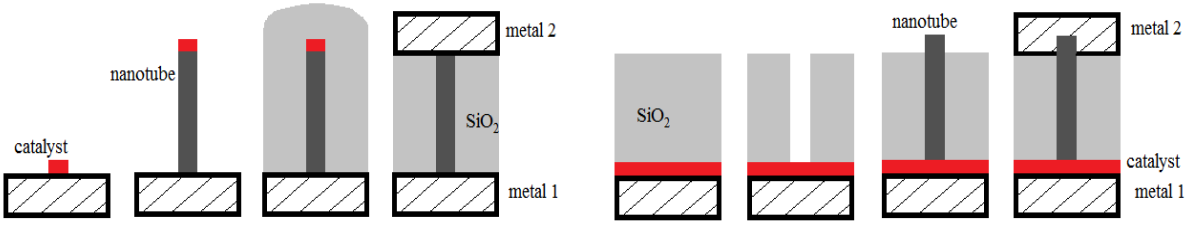
The two basic approaches for growing of nanotubes by CVD methods are:-

(i) Bottom-up approach based on tip growth model.

In this a piece of catalyst of required size and thickness is placed onto the metal contact at a specified location where the nanotube is to be grown. Now when the catalyst is exposed to the carbon source, the catalyst dissolves the carbon until it precipitates forming a graphene cylinder. In this method the catalyst always sits on the top of nanotube. Now SiO_2 layer is grown and top portion is etched for forming another metal contact. As the catalyst sits on the top of the nanotube therefore it is also removed in the process of etching. This approach uses PECVD to grow MWCNTs which sometimes grows imperfect structures [9,11].

(ii) Buried catalyst approach which is based on base growth model.

In this a layer of catalyst is pre-grown on to the contact metal buried under SiO_2 layer. The location at which the nanotube is to be grown is reached by etching a via in the SiO_2 layer till it reaches catalyst. Now the catalyst is exposed to the carbon source, the catalyst dissolves the carbon until it precipitates on to the top of the catalyst forming a graphene cylinder. Another metal contact is grown on the top of the SiO_2 layer around the nanotube. Arrays of MWCNTs are grown using hot filament CVD [9].



(a) Bottom-up, (b) Buried catalysts

Fig. 1.10 Various approaches for growing CNT. [9]

These approaches used for growing CNTs are based on the substrate catalyst interaction, i.e. if it's strong then buried catalyst approach used and if the interaction is weak then bottom-up approach is used [11]. The interaction between the catalyst and metal is preferred to be low so as to suppress inter diffusion therefore bottom-up approach preferred, however for the nanotubes below 22nm node technologies buried catalyst approach is preferred for its low metal contact resistance [9].

All the above defined methods used catalyst for the growth of CNT but here exist some methods which grows CNTs without using the metal catalyst. One of such method is stated below.

1.3.2 CNT growth using MW PECVD

In this process highly aligned CNTs can be directly grown onto the channels of anodic aluminum oxide (AAO) at a significantly low temperature by using Microwave plasma enhanced CVD (MW PECVD) technique [5]. In MW PECVD hydrocarbon gas which acts as a source is transformed into plasma by using high frequency (GHz range) electromagnetic radiation.

Anodic aluminum oxide (AAO or Al_2O_3) films are prepared by anodically oxidizing pure aluminum plates in a sulfuric acid electrolyte under a dc voltage at a low temperature (5~17ºC). Anodic oxidation is a electrochemical process of producing thin oxide films onto a metallic substrate. In this process the surface of the metal reacts with the electrolyte forming a oxide layer on the surface of the metal. The AAO films are mesoporous in nature i.e. it contains channels. These films are thermally and chemically stable, therefore the nanotube formed are highly pure.

The length of the nanotube is equal to the thickness of the AAO film. The nanotubes formed by this method are MWCNT whose diameter is equal to that of the AAO channel. In this the nanotubes are directly formed on the walls of the channels and follows layer by layer deposition process. Tip of some channels are closed due to the abnormal growth of nanotubes. These are removed by etching the surface of the AAO film. Complete step by step process is shown in Fig. 1.11.

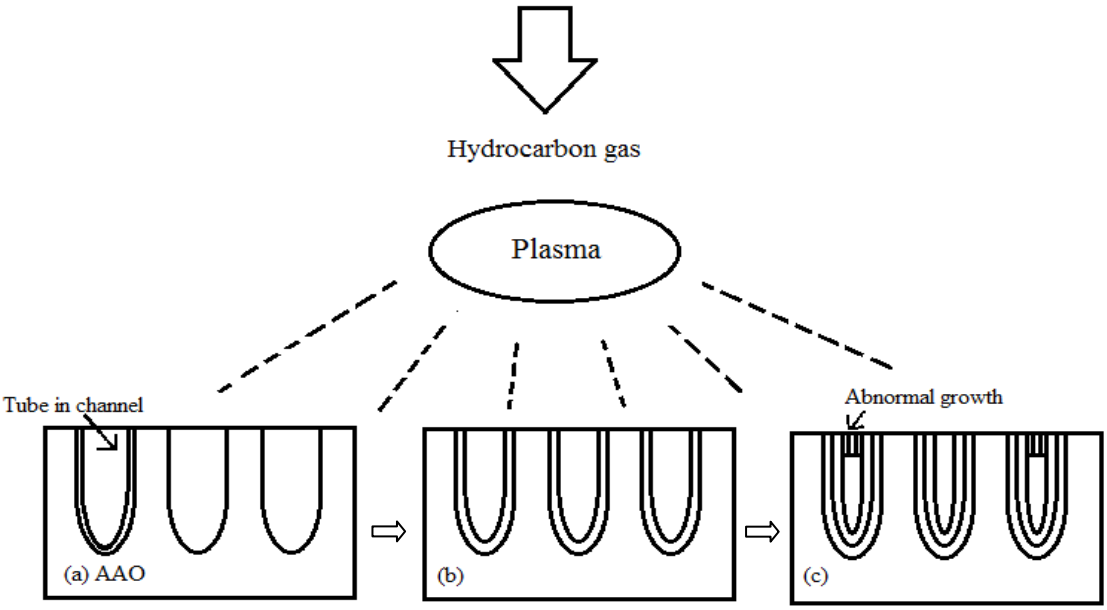


Fig. 1.11 CNT formation using AAO channels. (a) The initial deposition of graphite on the walls of the channels; (b) The layer-by-layer deposition of graphite; (c) Some nanotubes closed due to abnormal growth. [5]

The deposition of AAO film is slow process however the formation of the nanotubes in AAO film is much faster. This approach is best suited for growth of MWCNTs with a ultra small diameters.

1.4 Modeling of MWCNT as an Interconnect

1.4.1 Parameters of MWCNT model

An isolated MWCNT is placed onto a infinite ground plane (Fig. 1.12) with the outermost shell diameter D_{max}, the diameter of innermost shell is D_{min}, separation between outermost shell and the ground is Y, each shell is separated by a minimum distance of 0.34 nm which is the Van der Waal gap [28].

Before understanding the MWCNT model we first need to understand the properties of single shell structure of CNT which is nothing but a simple structure of a SWCNT as shown in Fig. 1.12. These parameters are given as:-

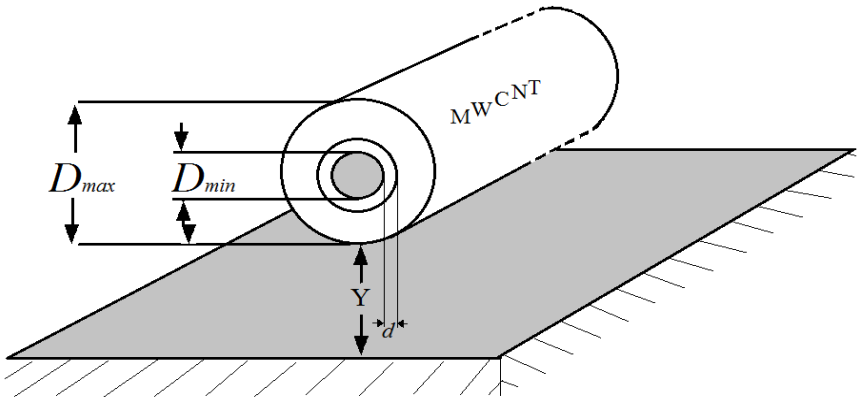


Fig. 1.12 MWCNT structure on a ground plane. [46]

1.4.1.1 Number of channels, shells

Every shell in CNT has multiple conducting channels which provide the path for an electron to flow. These conducting channels are formed because of the spin and sub-lattice degeneracy of electron in CNT. The number of conducting channels for a single shell is given by the equation:-

$$N_{shell}\left(D_i\right) \approx a.D_i + b, \qquad D_i > 3 \text{ nm} \tag{1.4}$$

Where D_i is the diameter of the shell, a = 0.0612 nm^{-1}, and b = 0.425. The ratio between D_{min}/D_{max} ranges from 0.3 to 0.8 [27], but for our convenience we take it as 0.5. p denotes the number of shells in a MWCNT [46], obtained by equation:-

$$p = 1 + Inter\left[\frac{D_{max} - D_{min}}{2 \cdot d}\right] \tag{1.5}$$

Where "Inter[·]" refers that the integer part is only considered, d denotes the Van der Waals gap i.e. the minimum distance for adjacent shells.

The numbering of shells is done from the outer shell towards the inner shell and ranges from 1, 2, . , i upto p (innermost shell), the diameter of the i_{th} shell is given as:-

$$D_i = D_{max} - 2d.(i-1), \qquad 1 \le i \le p \tag{1.6}$$

The diameter of the outermost shell depends on the technology node used. Various other parameters such as number of shells, minimum height of the center of an interconnect from ground plane etc. also depends on the technology node used.

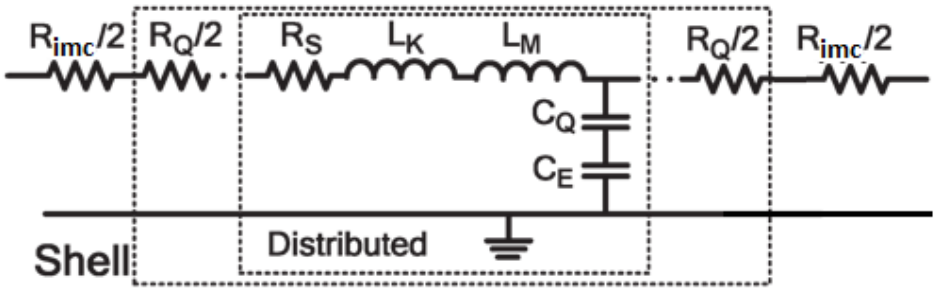


Fig. 1.13 Equivalent Single conductor circuit model for CNT. [33]

1.4.2 R, L, and C for an Individual Shell in MWCNT

- **Resistance :-**

Resistance arises when electrons while moving inside a conducting medium gets scattered due to impurities or defects. The fundamental resistance (R_F) of the nanotube mainly arises due to contact quantum resistance (R_Q) and scattering resistance (R_S). Contact quantum resistance arises due to Ballistic transport phenomena. This happens when the mean free path (λ) of electron is much larger than the length of the medium and in this the electrons alters there motion due to collisions with walls only and not because scattering. However scattering resistance (R_{SC}) is considered for the length of interconnect greater than the electrons Mean free path [18]. Scattering resistance appears as a distributed resistance along the length of the nanotube. The fundamental resistance (R_F) [7,27] is given as:-

$$R_F = R_Q + R_S \cdot L = \frac{h}{2e^2 N} + \frac{h}{2e^2 N} \cdot \frac{L}{\lambda} \qquad (\text{k}\Omega) \qquad (1.7)$$

Where, $h/2e^{-2} \sim 12.9$ kΩ, and L, N, λ are the length, conducting channels in shell and Mean Free Path (MFP) respectively. However it is observed practically that the resistance value of interconnect is much higher than the resistance of the CNT calculated using above formula. This is the due to the effect of imperfect contact resistance (R_{imc}), as it adds to the resistance of nanotube, increasing the overall resistance of the interconnect. The imperfect contact resistance (R_{imc}) can range from zero to hundreds of kilo-Ohms for different growth processes. Reportedly R_{imc} in MWCNT could be very small compared to the equivalent resistance observed at global length.

As per [17] it is noted that irrespective of the nature of shells in an MWCNT, metallic or semiconducting, its MFP always depends on its diameter and is stated as $\lambda \approx 1000D$.

- **Inductance :-**

CNT contains magnetic inductance (L_M) and kinetic inductance (L_K). The magnetic inductance (L_M) is caused by the magnetic field formed by an isolated current carrying wire of diameter D placed a placed at a distance (Y) from ground plane (Fig. 1.12). While, the kinetic inductance ($L_{K/\text{channel}}$) is calculated by using the expression for the kinetic energy stored in each conducting channel of the CNT. Each shell of CNT has N parallel conducting channels which give rise to an effective kinetic inductance ($L_{K/\text{shell}}$) for each shell. The per unit length expression for magnetic inductance (L_M), kinetic inductance ($L_{K/\text{channel}}$) and effective kinetic inductance ($L_{K/\text{shell}}$) is given as:-

$$L_M = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2Y}{D_i}\right) \qquad \left(\text{pH}/\mu\text{m}\right) \tag{1.8}$$

$$L_{K/channel} = \frac{h}{2e^2 v_F} \times \frac{1}{2} \qquad \left(\text{nH}/\mu\text{m}\right) \tag{1.9}$$

$$L_{K/shell} = \frac{L_{K/channel}}{N} \tag{1.10}$$

It is seen that magnetic inductance (in pH/μm) is very much small as compared to kinetic inductance (in nH/μm) [7,27]. Therefore we say that Kinetic inductance has significant impact on the delay model of an interconnect when compared to that of magnetic inductance.

- **Capacitance :-**

The capacitance of a CNT is mainly caused due to quantum capacitance (C_Q), coupling (shell-to-shell) capacitance (C_S) and electrostatic capacitance (C_E) (as shown in Fig. 1.13). Quantum capacitance ($C_{Q/\text{channel}}$) is due to quantum electro-static energies stored within a channel of CNT while carrying current. Each shell of CNT has '*N*' parallel conducting channels therefore contributing to form a effective quantum capacitance ($C_{Q/\text{shell}}$) for each shell. The per unit length expression C_Q (in aF/μm) is :-

$$C_{Q/channel} = 2 \times \frac{2e^2}{v_F} \qquad \left(\text{aF}/\mu\text{m}\right) \tag{1.11}$$

$$C_{Q/shell} = C_{Q/channel} \times N \tag{1.12}$$

Now, electrostatic capacitance (C_E) is obtained by treating the nanotube as a thin cylindrical conductor of diameter '*D*' (outermost shell), placed at a '*Y*' distance from ground plane (Fig. 1.12).

$$C_E = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{2Y}{D_{\max}}\right)} \qquad \text{for } Y > 2d \qquad \left(\text{aF}/\mu\text{m}\right) \tag{1.13}$$

Before calculating coupling (shell-to-shell) capacitance (C_S), first we need to understand that how it is caused? To understand this first we need to know the structure of MWCNT which is a set of concentric shells, which look as several shells arranged in parallel to one another each having different diameters, which translate to different number of channel and different MFPs, resulting in different circuit parameters. Hence, the parameters of each shell cannot be combined in a simple way. Moreover, the potentials of different shells cannot be assumed to be equal as circuit parameters of each shells vary with one another in MWCNTs, , therefore shell-to-shell capacitive coupling is induced [27,34]. This coupling capacitance is a kind of electrostatic capacitance and which is very large due to the small separation between two adjacent shells. Therefore in order to obtain shell-to-shell capacitance per unit length (*Cs*) there is a need to use the coaxial capacitance formula.

$$C_S = \frac{2\pi\varepsilon}{\ln\left(\frac{D_{Out}}{D_{In}}\right)} \qquad \left(\text{fF}/\mu\text{m}\right) \tag{1.14}$$

Where, D_{in} and D_{out} are the diameters of the inner and outer shells of adjacent coaxial shells, and *d* equals 0.34 nm.

1.5 Multi-conductor circuit (MCC) model of MWCNT

After analyzing all the RLC parameters, the Multi-conductor circuit [49] is represented as Fig. 1.14 where *p* is the number of shells.

Multi-conductor circuit gives a proper view of the RLC arrangements of MWCNT interconnects. The number of shells or the number of concentric cylinders is given by '*p*',

where '*p*' being the innermost shell while '1' being the outermost shell. As it can be clearly seen in Fig. 1.14 that both imperfect contact resistance (R_{imc}) and contact quantum resistance (R_C) are equally distributed at both the contact ends of the interconnect. However it is important to note that imperfect contact resistance (R_{imc}) is caused by the complete interconnect treated as one, while quantum contact resistance (R_Q) is caused due to the each shell of MWCNT. In MWCNT the electrostatic capacitance (C_E) arises b/w outer most shell and ground plane, and if an interconnect contains several MWCNTs then it exist b/w MWCNT nearest to ground plane and ground plane.

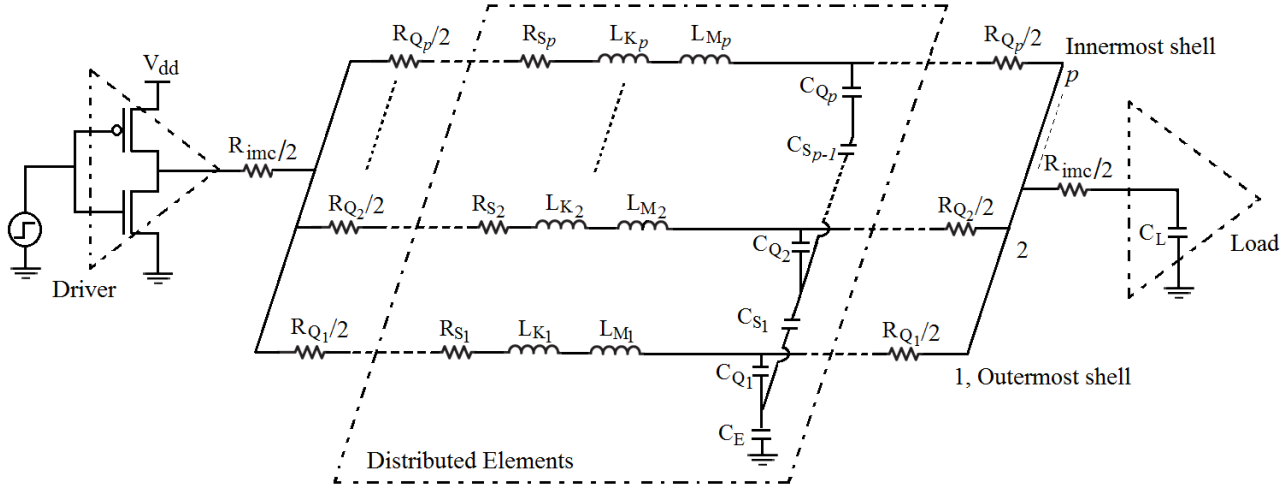


Fig. 1.14 MCC model of a *p* shell MWCNT. [49]

Some parameters such as scattering resistance, quantum capacitance, and inductances arises due to the intrinsic properties of each shell based on its diameter and number of conducting channels, and therefore varies from shell to shell as seen in the Fig. 1.14.

A CMOS inverter is used as a driver for the interconnect [34] because of its fast switching, small size and moderate noise margin, C_L depicts the input capacitance of the fan-out gates acting as a load to the interconnect line.

1.6 Thesis Organization

The remaining chapters are organized as follows:-

CHAPTER 1 – This chapter gives an introduction to CNT as an interconnect. Various growth techniques for CNT are discussed. Parameters required for the analysis of MWCNT as an interconnect is also studied in this chapter.

CHAPTER 2 – This chapter discusses various literature surveys on different growth techniques of CNT and performance analysis of CNT as an interconnect.

CHAPTER 3 - On the basis of literature survey, research gaps are proposed in this chapter and based on which some objectives are determined.

CHAPTER 4 - This chapter describes the methodology used for evaluating the objectives proposed in previous chapter.

CHAPTER 5 - In this chapter simulation results are obtained for various parameters and reasons for the variation in results are provided.

CHAPTER 6 – In this chapter the effect of intershell intersection on different parameters of an interconnect are discussed and simulations are performed for analyzing the effect of tunneling conductance on interconnect parameters.

CHAPTER 7 – Based on results obtained, this chapter describes the conclusion and future scope with respect to the work done.

CHAPTER 2
LITERATURE REVIEW

Carbon Nanotube Arrays Prepared by MWCVD [5]

- B. D. Yao, N. Wang

As most of the techniques used in the growth of carbon nanotubes (CNTs) are based on catalyst approach, however this paper provides a non catalyst approach for growing highly aligned nanotubes. This approach uses channels of anodic aluminum oxide (AAO) at low temperature for directly growing the nanotubes on the metallic surface. Microwave plasma enhanced CVD (MW CVD) is used for breaking and ionizing the hydrocarbon as a source. The growth result viewed by using scanning electron microscope (SEM) images showed a highly aligned MWCNT grown in the channels of AAO film. A more clear view was obtained from the plane view TEM image. The growth results observed showed that in AAO the shells of MWCNT were formed by layer by layer deposition process.

Carbon nanotube growth by PECVD: a review [10]

- M Meyyappan, Lance Delzeit, Alan Cassell, David Hash

As in recent years plasma enhanced CVD has emerged as one of the better techniques for producing well aligned nanotube structures. Various plasma sources currently used for the growing multi walled carbon nanotubes (MWCNT) at a much lower temperature as compared with other techniques are also discussed. A reactor model is also presented along with the procedure for growing nanotubes using PECVD technique. The result given in the paper for grown MWCNTs using scanning electron microscope (SEM) images provides evidence of a well aligned CNTs. The role of catalysts for catalyst based growth of CNTs are also been discussed briefly.

Interconnect Challenges for Nanoscale Electronic Circuits [15]

- Navin Srivastava, Kaustav Banerjee

With the reduction in feature size of the transistor, the speed of the transistor has increased but the case is not same with interconnects. This paper briefly discusses the problems faced

by interconnects when the feature size is reduced below 90 nm technology node. This paper discusses the problems faced by copper with the scaling down of technology. The main causes of these problems i.e. increase in resistivity of Cu interconnects, because of surface roughness and boundary scattering and the effect of electro migration due to increased current density and their impact on the interconnect delay is also been discussed briefly. The paper also throws some light on the emerging technologies such as carbon nanotubes; 3-D ICs, optical interconnects as a replacement of copper.

Determination of the Intershell Conductance in Multiwalled Carbon Nanotubes [16]

- B. Bourlon, C. Miko, L. Forro , D.C. Glattli,, A. Bachtold

This paper reports the intershell electron transport mechanism for a MWCNT. It studies the current path followed through the different shells of MWCNT by using local and non local four point measurement technique. The paper concludes that the intershell conductance is the tunneling conductance caused due to the overlapping of π orbital's of neighboring shells and an expression for its calculation has also been provided.

Circuit Modeling and Performance Analysis of Multi-Walled Carbon Nanotube Interconnects [27]

- Hong Li, Wen-Yan Yin, Kaustav Banerjee, Jun-Fa Mao

This paper discusses the structural differences between SWCNT and MWCNT and it also investigates the behavior of MWCNT as an interconnect. The paper provides the RLC parameter to study the impact of these parasitic parameters and based on these parameters an ESC model of a MWCNT has been derived. Parameters caused due to the Quantum effects and intershell effect are also been discussed. The simulations are performed for global, intermediate and global lengths. Simulation results based on delay analysis presented in the paper proves the effectiveness of MWCNT over SWCNT and copper at intermediate and global levels. This paper also discusses the impact of imperfect contact resistance and the role of interconnects aspect ratio on its propagation delay. The paper concludes that for a long length interconnect (mainly global or intermediate levels); the delay caused by MWCNT is much lower than that caused by copper. However for short local interconnects copper is better than MWCNTs.

Synthesis of Carbon Nanostructures by CVD Method [31]

- Krzysztof Koziol, Bojan Obrad Boskovic, Noorhana Yahya

This paper throws light on the various catalyst based techniques used for the synthesis of CNTs. It provides the advantages and the disadvantages of using these various techniques. This paper also provides significant evidence on why the CVD techniques are more preferred over other for the growth of CNTs. This paper discusses both thermal and plasma enhanced CVD techniques. In the paper, the two major approaches, bottom up and buried catalyst approach for the growth of CNTs are well discussed. The effect of catalyst size, thickness, its reaction rate along with the effect of temperature and SiO_2 thickness on the growth rate and the diameter of the CNT are also discussed.

Analyzing Carbon Nanotube Interconnects in VLSI Application [32]

- Mahmudur Rahman, Ahrar Ahmed Chowdhury

In this paper the electrical properties of carbon nanotubes as an interconnect in VLSI circuits have been analyzed. Accordingly, the effectiveness of metallic SWNT interconnect has been studied using Raman spectroscopy for its outstanding ballistic conductivity, low resistance and low capacitance. The performance analysis of SWCNT bundle based on RLC parameters is discussed. Impact of Resistivity on MWCNT, SWCNT bundles with full and one-third metallic portion is studied and by using this result, the paper concludes that metallic interconnects is the future of VLSI technologies.

Efficient Model for Delay Estimation of MWCNT Interconnects [35]

- Morteza Gholipour, Nasser Masoumi

This paper studies MWCNT as a future of VLSI interconnects based on propagation delay. The paper proposed a semi-analytical model for numerical analysis of delay at various technology nodes based on ITRS 2005 parameters. An efficient MWCNT model has been discussed and delay at different lengths and at different technologies has been simulated. The role of repeater in reduction of the delay has also been discussed. The paper based on simulated concludes that at intermediate and at global lengths MWCNT is faster than copper. The simulation analysis showed that the result obtained by the semi analytical model is very

close to that of result obtained by simulations proves the efficiency of the proposed model. Based on obtained results, paper concludes that at a given length MWCNT requires lesser buffers then copper specially at global lengths.

A RC Model for Multiwalled Carbon Nanotubes as Interconnects [36]

- Hossein Sheikhassadi, Nasser Masoumi

A compact RC model for both MWCNT and MWCNT bundle is presented in the paper. The delay analysis performed under this paper is based on Elmore delay model. The paper discusses the various parameters of MWCNT and transforms it for MWCNT bundle based model. In this paper the delay based SPICE simulation was focused on interconnects at global lengths with one MWCNT, a bundle with 3 MWCNTs arranged parallel and a bundle of 9 MWCNT arranged in 3 rows and 3 columns. The paper concludes that the scattering resistance is inversely proportional to the mean free path (MFP) of the electrons and as it decreases the overall resistance increases and therefore the propagation delay also increases. The proposed model when compared with equivalent model of MWCNT, the difference between delays observed by simulation of the two models is found to be less than 2% for both MWCNT and its bundles.

Estimation of Time Delay and Repeater Insertion in Multiwall Carbon Nanotube Interconnects [38]

- Feng Liang, Gaofeng Wang, Wen Ding

This paper uses a finite difference time domain (FDTD) method on a derived equivalent single conductor model for interconnect line. Based on this a 50% time delay analysis is performed for a driver-interconnect-load structure using SPICE simulation. In this paper a CMOS gate is used as a driver for interconnect line. Based on the simulation results the impact on propagation time delay with the variation of length at intermediate length has been plotted for 14nm and 22nm technology nodes. Simulations are also carried to study the optimum number of repeaters required by MWCNT and copper at 1000μm intermediate length and at 2000μm and 5000μm global length. The paper concludes that the propagation time delay in MWCNT is much less than that observed in copper at global, intermediate

level. The number of repeaters used by MWCNT at a particular length is one third of that used by copper in order to reduce the time delay.

Study on Equivalent Single Conductor Model of Multi-Walled Carbon Nanotube Interconnects [39]

- Min Tang, Jiaqing Lu, Junfa Mao

This paper provides an effective way for study and simulating the complex MWCNT interconnect using ESC model. The effectiveness and the accuracy of ESC model were tested by comparing the simulation results obtained by ESC model to that of multi conductor model (MCC). The impact of imperfect resistance along with the tunneling conductance of MWCNT was also studied for MCC model. The paper also states that the accuracy of the system is largely dependent on the value of imperfect contact resistance i.e. lower the values better the accuracy.

Transmission-Line Model for MWCNT with Intershell Tunneling [40]

- Carlo Forestiere, Antonio Maffucci, Sergey A. Maksimenko, Giovanni Miano,

This paper talks about the structure, conduction phenomena and electromagnetic response of CNT as an interconnect. In the paper the electromagnetic propagation is studied for SWCNT based on two different approaches, one was based on the equations based on the boundary conditions of Maxwell's equations which are solved numerically, the other is based on transmission line (TL) model. This paper is based on the fact that SWCNT behaves like a quantum wire which can be modeled by using TL model. The paper also discusses intershell tunneling in MWCNT and the impact it brings on the parameters of adjacent shells by using proposed TL model for a frequency range of microwave to terahertz. The paper concludes that the action of intershell tunneling is similar to that of magnetic coupling of shells and therefore the intershell magnetic coupling remains valid even at the limits of vanishing magnetic inductance.

Modeling and fast simulation of multiwalled carbon nanotube interconnects [49]

- Tang, Min, Junfa Mao

This paper investigates modeling and fast simulation analysis of MWCNT for global interconnects. A effective realization of MCC model into ESC model is also provided. Both intershell tunneling conductance and imperfect contact resistance are studied in the paper. On the basis of ESC model a highly efficient approach based on delay extraction algorithm has been proposed for fast simulations of MWCNT interconnect. The proposed ESC model provides an accurate 50% time delay estimation, its accuracy and efficiency has been demonstrated by numerical analysis. On analyzing ESC and MCC models for different locations of imperfect contact resistance, it was observed that the electrical properties of MWCNT interconnect are affected, this effect can be by introduction of intershell tunneling conductance in model analysis.

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CHAPTER 3
RESEARCH GAPS

The main objective of an interconnect is to carry the signal from driver source to load with minimum propagation delay and minimum power consumption. Propagation delay and power consumed increase with increasing length. This effect was minimized by insertion of Repeaters.

Majority of the research is based on Multi-Conductor Circuit (MCC) model of MWCNTs without considering tunneling effect.

Therefore, a modified Multi-Conductor Circuit (MCC) model of MWCNT considering tunneling effect is needed to be realized and then analyzed using simulation. The changes it brings to MWCNTs propagation delay when compared with MWCNT without tunneling is also needed to be studied.

3.1 Objectives

Based on the proposed research gaps, the objectives to be analyzed are :-

1. To derive an Equivalent single conductor (ESC) model from Multi-Conductor Circuit (MCC) model using mathematical analysis.
2. To study the effect of driver size, Capacitive load, imperfect contact resistance on propagation delay for an ESC model at different technology nodes for a fixed global length.
3. To study the change in propagation delay with respect to length at different technology nodes for a above derived ESC model.
4. To study the effect of repeaters on propagation delay for a distributed ESC model at fixed global length.
5. To study the effect of change in D_{min} *to* D_{max} ratio with respect to length.
6. To study the impact of .intershell tunneling on the value of equivalent resistance and delay with respect to length.
7. To prove that MWCNT better than Copper as global interconnect, based on obtained results.

CHAPTER 4
PROPOSED METHODOLOGY

The simulation of MCC model is complex and complicated as compared to that of ESC model [35,37]. Therefore for analysis of MWCNT, MCC model is needed to be converted into ESC model.
The mathematical analysis in order to obtain different parameters for ESC model from MCC model at different technology nodes is done using MATLAB.

At a particular technology node the different values of RLC are obtained at different lengths. The results obtained are provided to SPICE simulator and propagation delay is calculated. These simulations are done at different driver size so as to obtain optimized driver size which provides minimum propagation delay.

ESC model for a fixed length and technology and optimized driver size is distributed into N sections by insertion of repeaters (buffers). The value of N is chosen using simulation which provides minimum propagation delay.

4.1 Realization of ESC model from MCC model

As seen in Fig. 1.14, *p* represents the different shells of MWCNT each connected in parallel to each other. In order to obtain equivalent Resistance, Capacitance and Inductance so as to evaluate ESC model (Fig. 1.13) we need to derive an expression in order to obtain these values.
The realization is based on the assumption that all the shells are parallel and separated by a fixed distance Vander Waal distance of 0.34nm [39,49].

The resulting equivalent Scattering Resistance (R_S) and Quantum Contact Resistance (R_Q) is formulated as :-

$$R^{-1} = \sum_{i=1}^{p} \left(R_{Q\,i} + R_{S\,i} \right)^{-1} \qquad for\ (i = 1,\ 2, \ldots . p) \tag{4.1}$$

Similarly the equivalent Magnetic Inductance (L_M) and Kinetic Inductance (L_K) is formulated as :-

$$L^{-1} = \sum_{i=1}^{p} \left(L_{K\,i} + L_{M\,i} \right)^{-1} \qquad for\ (i = 1,\ 2, \ldots . p) \tag{4.2}$$

The derivation of equivalent Capacitance is slightly difficult and has to be done in parts. The obtained simplified circuit for evaluating Capacitance is shown in Fig. 4.1

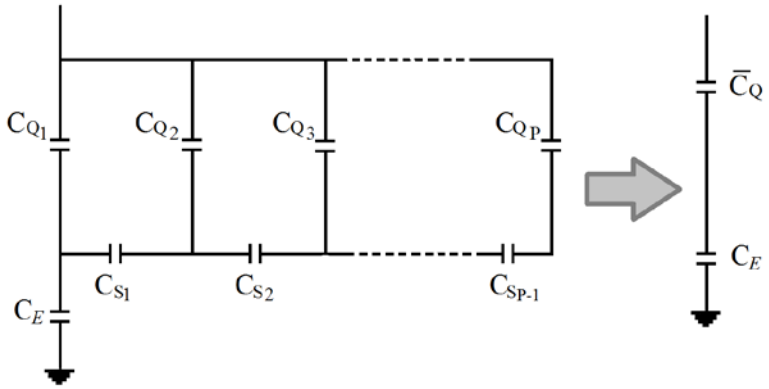

Fig. 4.1 Realization of equivalent capacitance. [45]

Let $\overline{C}_Q$ be equivalent Capacitance and C_{Qj} is Quantum Capacitance C_S is Scattering Capacitance

$$\overline{C}_Q = C_1, \tag{4.3}$$

Where C_1 is calculated in a recursive way :-

$$C_p = C_{Qp} \tag{4.4}$$

$$C_{j-1} = \left(C_j^{-1} + C_{S(j-1)}^{-1} \right)^{-1} + C_{Q(j-1)} \qquad for\ (j = p, \ldots . . 3, 2) \tag{4.5}$$

The values obtained are put in ESC model given in Fig. 1.13 and the obtained circuit is simulated. The total capacitance in ESC model is taken as:

$$C = \left(C_1^{-1} + C_E^{-1} \right)^{-1} \tag{4.6}$$

4.2 Delay analysis of MWCNT

One of the most important aspects of performance analysis is delay analysis. Delay is dominantly caused by the RLC parameters of interconnect and is measured as:-

$$Delay\ (\tau) = \frac{\tau_{PHL} + \tau_{PLH}}{2} \tag{4.7}$$

Where τ_{PHL} is given as fall time while is τ_{PLH} given as rise time. For the analysis the length (L) of interconnect is considered to be at global level and is driven by a CMOS inverter with a digital signal of 50% duty cycle. CMOS inverters are based on PTM parameters [50]. Capacitive load (C_L) is considered at output whose value may range from 1fF to 10fF [26].

Table 4.1 ITRS 2013 based simulation parameters for global interconnects. [42]

Technology Node	**32nm**	**22nm**	**16nm**
Width W(nm)	40	28	18
Thickness H(nm)	120	84	54
Aspect Ratio(A/R)	3	3	3
Oxide Thickness *Y* (nm)	93.6	65.5	40
V_{dd} (volts)	0.9	0.8	0.7
Dielectric constant (ε_r)	2.77	2.59	2.31
D_{ratio} (D_{min}/D_{max})	0.5	0.5	0.5
ρ_{Cu} (μΩ.cm)	3.66	4.2	5.69

The interconnect parameters based on the technology node are considered according to ITRS 2013 and based on these parameters equivalent model MWCNT is derived [43]. As seen in Table 4.1, aspect ratio of interconnect at global level is considered to be 3. Therefore at global level interconnect consist of a MWCNT bundle which has 3 MWCNT connected vertically in parallel to each other as shown in Fig. 4.2(b) [41,47]. With mathematical analysis an ESC model is derived and is simulated using SPICE simulation in order to study delay analysis.

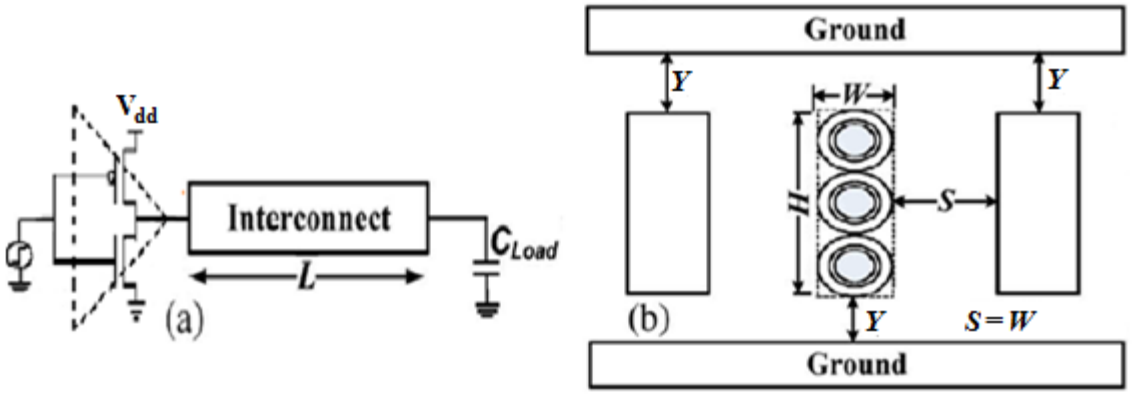

Fig. 4.2 (a) Structure of a CMOS driven interconnect
(b) placement of interconnect of aspect ratio 3 w.r.t. its surroundings. [26]

4.3 Repeaters (or Buffers)

It is seen that almost all the parameters (RLC, propagation delay) are dependent on Length of interconnect.

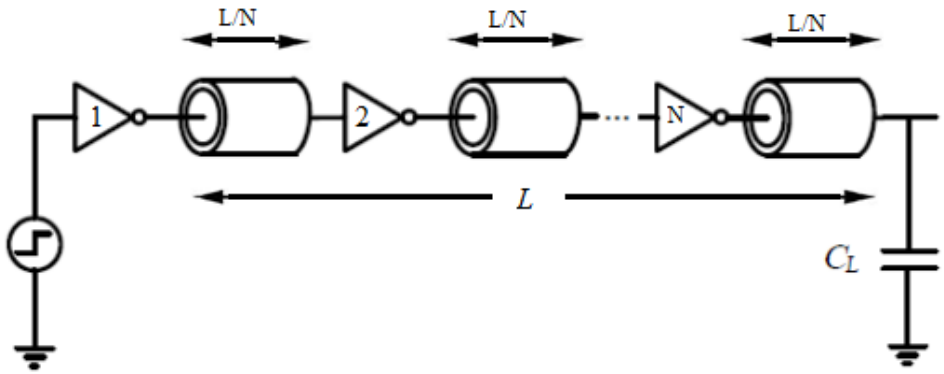

Fig. 4.3 Distributed model of ESC circuit.

The relation between them is observed to be directly proportional. Thus if length increases RLC parameters also increases resulting in increases in delay as it is proportional to RLC. For the global length (L >500µm) the RLC parameters and propagation delay may be very large and may produce an error i.e. propagation delay may be larger than ON time and unwanted output may be observed for a fixed frequency of signal. Therefore to avoid this error it is needed to minimize the length of an interconnect.

In order to minimize the length a distributed network consisting of N buffers is inserted in order to reduce the length. Inserting N buffers will divide the lumped ESC model in N segments thus reducing the Length by N. This also includes reduction of RLC by factor N for each segment. This reduces overall delay of interconnect but the power consumed increases, thus a trade off is required between them. The repeater size can be varied in order to obtain minimum delay [38,44].

CHAPTER 5
RESULTS AND DISCUSSIONS

In order to prove that at global length MWCNT is preferred over Copper we first need to analyze copper as an interconnect at different technology node and then the obtained results are needed to be compared with the results for MWCNT as interconnect at respective technology nodes.

5.1 Analyzing Copper as an interconnect

For analyzing Copper as a global interconnects, we need to obtain the RLC parameters of the copper and observe its impact on variation of length on delay. This is observed by using SPICE simulation tool. The value of RLC is obtained by using formulas given by equation 1.1, 1.2 and 1.3, and the parameters used are given by Table 4.1. The change in RLC with varying length is observed and its impact on propagation delay is studied for 32nm, 22nm, and 16nm technology node.

At 32nm technology node

Table 5.1 Impact of length on RLC parameters and delay at 32nm technology node

Length (μm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	0.733	0.152	8.4695	43p
500	3.667	0.9265	42.347	478p
1000	7.33	1.992	84.695	1.67n
1500	11.00	3.110	127.04	3.59n
2000	14.67	4.262	169.39	6.22n
2500	18.33	5.493	211.74	9.55n
3000	22.00	6.637	254.08	13.6n

At 22nm technology node

Table 5.2 Impact of length on RLC parameters and delay at 22nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	1.7857	0.1602	7.92	63p
500	8.93	0.962	39.6	948p
1000	1.857	2.063	79.2	3.53n
1500	26.786	3.217	118.8	7.75n
2000	35.714	4.405	158.4	13.53n
2500	46.643	5.6185	198.0	21.03n
3000	53.571	6.8516	237.59	29.94n

At 16nm technology node

Table 5.3 Impact of length on RLC parameters and delay at 16nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	5.535	0.169	7.173	132p
500	27.675	1.00	35.865	2.47n
1000	55.35	2.15	71.73	9.56n
1500	83.025	3.35	107.60	21.23n
2000	110.70	4.58	143.46	37.49n
2500	138.37	5.84	179.33	57.95n
3000	166.05	7.11	215.19	81.55n

Comparison of Delay in Copper at different technology node.

Table 5.4 Impact of length on propagation delay at various technology node for copper.

Length (µm)	Delay (s)		
	32nm	**22nm**	**16nm**
100	43p	63p	132p
500	478p	948p	2.47n
1000	1.67n	3.53n	9.56n
1500	3.59n	7.75n	21.23n
2000	6.22n	13.53n	37.49n
2500	9.55n	21.03n	57.95n
3000	13.6n	29.94n	81.55n

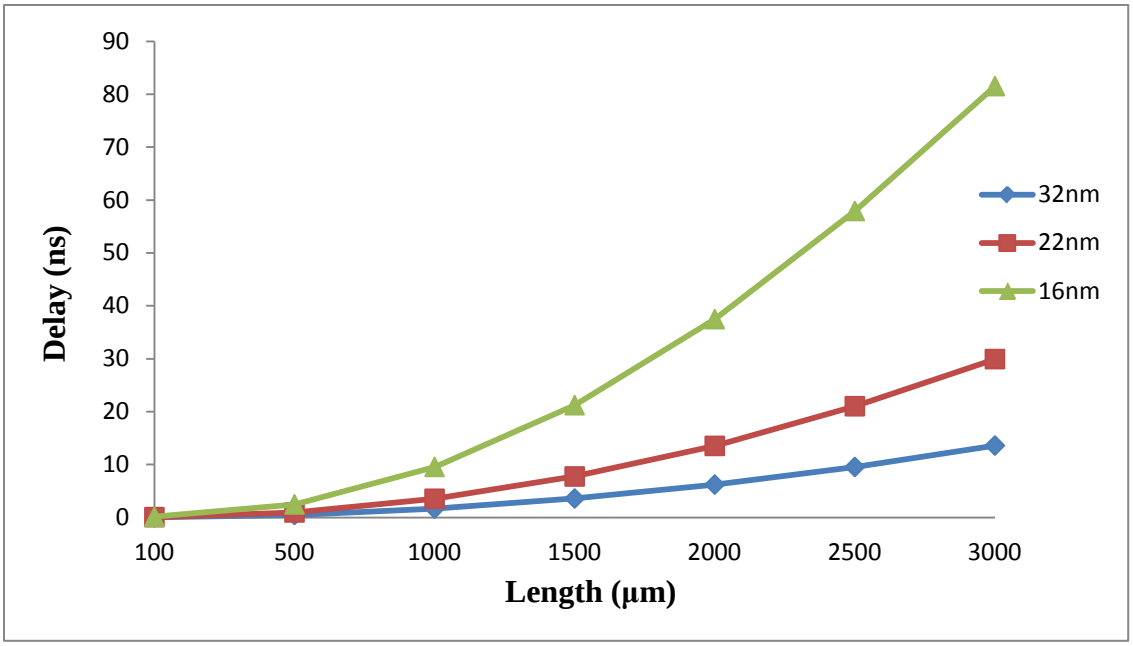

Fig. 5.1 Impact of Length on delay of Copper interconnects at 32nm, 22nm and16nm technology nodes.

Based on above Table 5.4 and Fig. 5.1, we observed that as the length of a copper interconnects is increased its propagation delay also increases, this increase is observed because the scattering resistance, inductance and capacitance as given by equation 1.1, 1.2 and 1.3are direct functions of length i.e. as the length increases the values of these parameters also increase as seen in Table 5.4. As we know that delay is directly proportional to these RLC parameters, therefore delay also increases.

It was also observed that the rate of increase in delay is exponential even when the rate of increase of length is linear. This is so because the rate of increase in RLC parameters product with respect to length is also exponential which results in exponential increase in delay. It is also interesting to see that rate of exponential rise varies with technology node i.e. smaller the technology node sharper the rise.

5.2 Analyzing MWCNT as an interconnect

Is MWCNT a better interconnect than copper for global length? In order to provide the answer, we need to study the delay analysis of MWCNT and compare it with that of copper by varying length and technology nodes.

In this section, the impact of variation of other parameters such as driver size, load, contact resistance, on the delay are also analyzed for the better understanding of MWCNT as interconnect. Further observation of the impact of repeaters on reduction of delay is also done. The RLC parameters for MWCNT are obtained using equation 1.4- 1.16, and a MCC model is realized. Based on the MCC model, an ESC model is derived using by using equations 4.1-4.6.

The Tables given below gives the values of derived RLC parameters of an ESC model. Simulations are performed on this derived ESC model.

In this case a ESC model for MWCNT at global length of 1000μm is considered, few parameters are assumed to be as:

Length = 1000μm; R_{imc} = 2kΩ;

C_L= 1fF; $v_F = 8x10^5 m/s$

MFP (λ)= 1000.D_i; D_{min} to D_{max} ratio = 0.5

The other parameters are based on ITRS 2013 (Table 4.1). And the simulations are carried to evaluate delay based on equation 4.7.

The RLC value at 1000μm is taken as:

Table 5.5 RLC values for ESC model simulation at 32nm, 22nm and16nm technology nodes for global length of 1000μm.

Technology node	**R (kΩ)**	**L (nH)**	**C (fF)**
32nm	1.771	33.185	68.614
22nm	4.4043	58.432	64.082
16nm	11.753	99.55	58.275

5.2.1 Optimum Driver size

For the SPICE simulation of ESC model a CMOS inverter as a driver is considered using PTM model file [50]. As it is known that in a CMOS inverter the size of a PMOS is 3 times that of NMOS and is fixed, however the W/L ratio (driver size) of the CMOS can be varied in order to achieve a size with minimum propagation delay. The simulation results to study the impact of driver size can be seen in Table 5.6 and in Fig.5.2

Table 5.6 Delay analysis for different driver size at 32nm, 22nm and16nm technology nodes for global length of 1000μm.

Driver Size (W/L of NMOS)	**Delay (s)**		
	32nm	**22nm**	**16nm**
10	511p	926p	1.90n

20	470p	870p	1.84n
30	459p	853p	1.80n
40	452p	844p	**1.78n**
50	448p	**840p**	1.78n
60	**446p**	840p	1.79n
70	447p	841p	1.81n

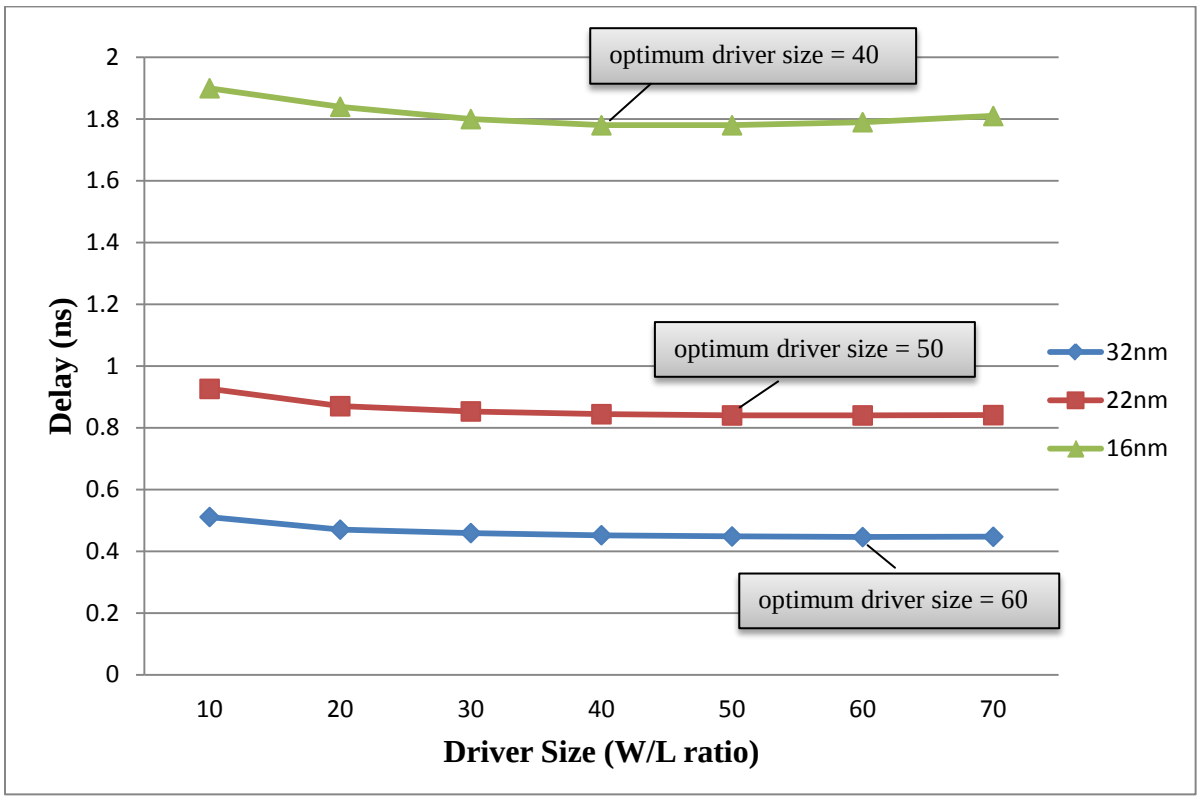

Fig. 5.2 Impact of CMOS Driver size on MWCNT interconnects delay at global length of 1000μm for 32nm, 22nm and16nm technology nodes.

It is interesting to observe that propagation delay changes while changing driver size. As the driver size increases propagation delay decreases initially till it reaches to a certain value and after that it tends to increase. The driver size at which the propagation delay reaches its minimum value is called as optimum driver size, at this point the impedance of interconnect

line matches with the driver thus experiencing minimum propagation delay. However the simulation results also shows that as the technology node is becoming smaller the optimum driver size required also decreases as seen in Fig. 5.2.

5.2.2 Frequency determination

The simulation results carried out for different operating frequencies but at fixed length and technology node shows that propagation delay of the interconnect is immune to varying operating frequencies i.e. propagation delay is independent to the changes in operating frequencies and therefore remains unchanged for a fixed length and technology node.

However, the maximum operating frequency of interconnect do depends on its propagation delay and load capacitor (C_L) which depicts the input capacitance of the fan-out gates acting as a load to the interconnect line. The reason for the dependency of maximum operating frequency on propagation delay is that, the output of interconnect is measured across a load capacitor (C_L), the time required by interconnects to charge or to discharge the capacitor (C_L) denotes its propagation delay if the operating frequency is set above its maximum value (obtained by equation 5.1) i.e. if the half time period is set below the propagation delay, the load capacitor (C_L) will not be able charge upto 90% or discharge upto 10% of the input signal, therefore a corrupted signal is obtained at the output across the load capacitor (C_L).

Now, let the operating frequency $f = \frac{1}{T}$, where T is the time period of the signal with 50% duty cycle. Then the relation between propagation delay and maximum operating frequency is given by:-

$$\frac{T_{\min}}{2} > Delay \Leftrightarrow \frac{1}{Delay} > 2 f_{\max} \qquad (5.1)$$

For irregular duty cycle, the time period should be set such that *Delay* should always be smaller than T_{ON} or T_{OFF} (whichever is small).

For the above cases the value of the value of load capacitance (C_L) was kept constant at 1fF. But the value of load capacitance (C_L) ranges from 1fF to 10fF and as its value increases the propagation delay also increases as observed in Table 5.7.

Table 5.7 Impact on delay with variation of Load Capacitance (C_L) at 32nm, 22nm and16nm technology node at 1000μm length.

C_L (fF)	Delay (s)		
	32nm	**22nm**	**16nm**
1	446p	840p	1.78n
4	471p	881p	1.88n
7	494p	924p	1.97n
10	518p	966p	2.06n

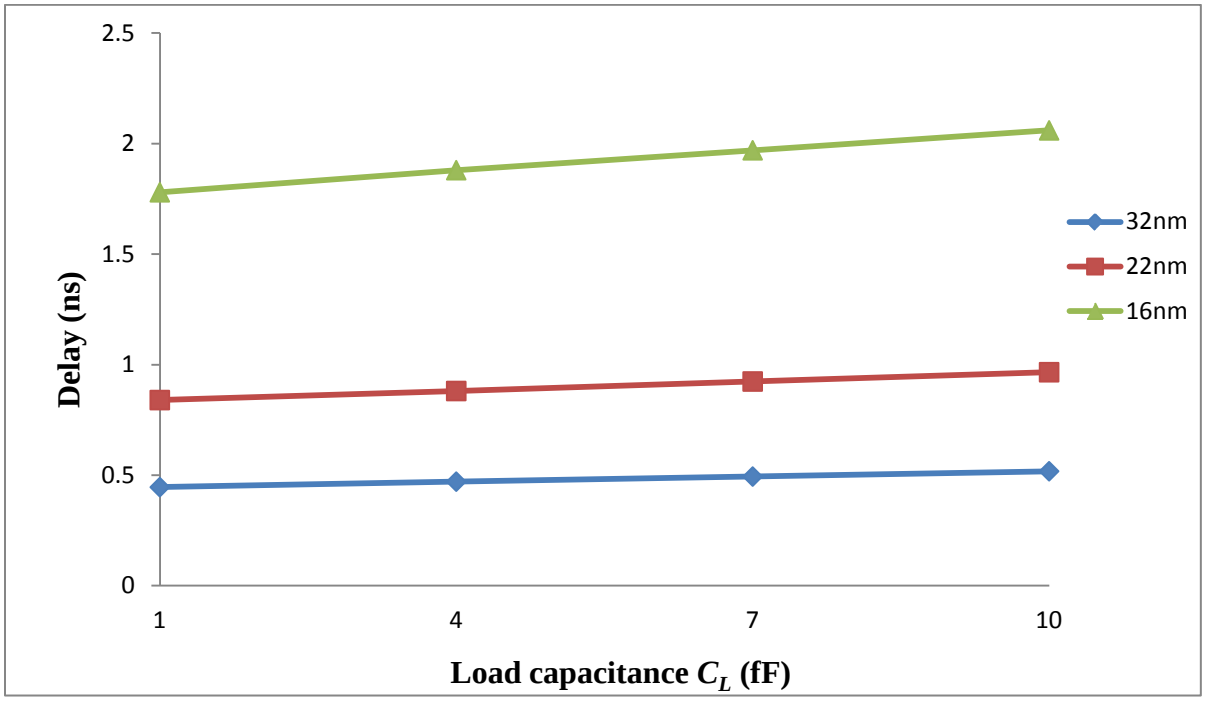

Fig. 5.3 Dependency of propagation delay on Load Capacitance (C_L) for a MWCNT interconnects at global length of 1000μm for 32nm, 22nm and16nm technology nodes.

In Fig 5.3 it is observed that as the value of load capacitance (C_L) increases the delay also increases. This is because as the capacitance value increases it requires more time for charging and discharging which increases the overall delay of the interconnect.

5.2.3 Impact of R_{imc}

The imperfect contact resistance R_{imc} is induced in fabrication process can range from zero to hundreds of kilo-Ohms for different growth processes. Reportedly R_{imc} in MWCNT could be very small compared to the total resistance and ranges 2kΩ~20kΩ.

In general for all the observations R_{imc} is kept constant at 2kΩ. But in order to see its impact on the overall delay of the system, R_{imc} is varied it from 2kΩ~20kΩ.

Table 5.8 Variation in delay due to imperfect contact resistance (R_{imc}) at 32nm, 22nm and16nm technology node at 1000μm length.

R_{imc} (kΩ)	**Delay (s)**		
	32nm	**22nm**	**16nm**
2	446p	840p	1.78n
4	613p	992p	1.92n
6	779p	1.14n	2.06n
8	940p	1.29n	2.20n
10	1.11n	1.45n	2.34n
12	1.27n	1.60n	2.47n
14	1.43n	1.75n	2.62n
16	1.59n	1.90n	2.75n
18	1.76n	2.05n	2.89n
20	1.92n	2.20n	3.04n

As observed in Table 5.8 and Fig. 5.4, as the value of imperfect contact resistance (R_{imc}) increases the propagation delay also increases delay. The increase in delay is observed to be linear.

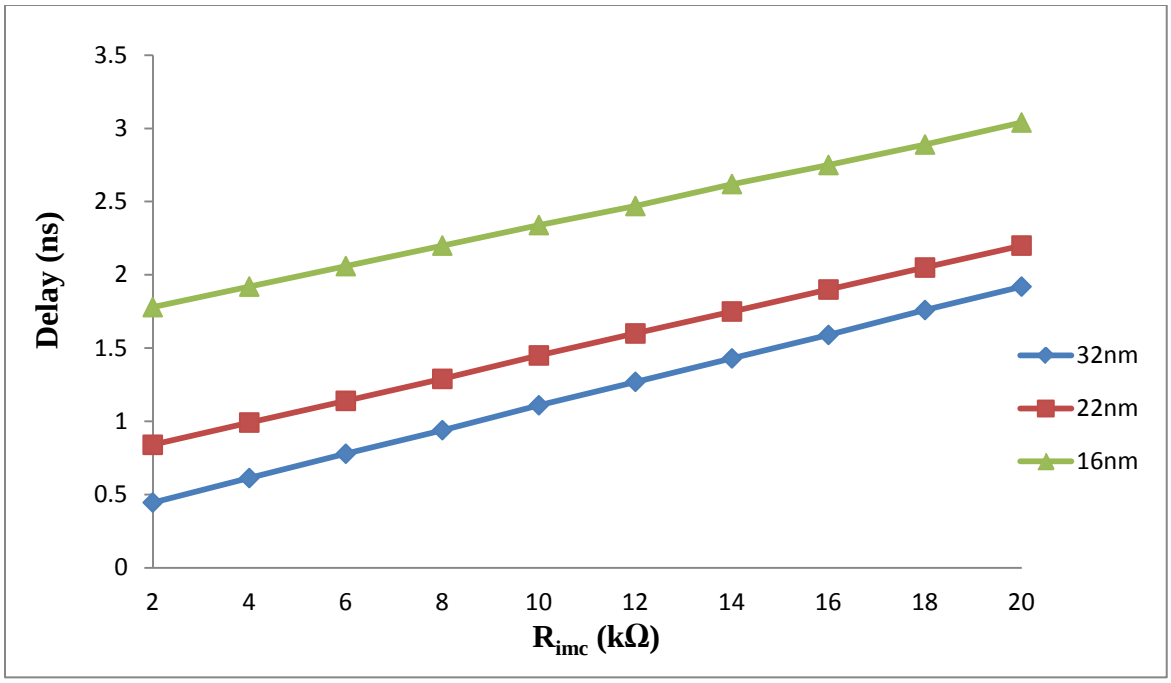

Fig. 5.4 Impact of R_{mc} on propagation delay of MWCNT interconnects at global length of 1000μm for 32nm, 22nm and16nm technology nodes.

The total resistances observed in interconnect line is the sum of contact resistances and the intrinsic resistances and as the contact resistances increases the overall resistance of the interconnect line also increases. As it is already known that as the total resistances of an interconnect line increases the propagation delay also increases. However its interesting to observe that the rate at which delay increase is linear in nature w.r.t R_{imc}. This is because the change in R_{imc} is constant which results in constant rise in total resistance of the interconnect line and therefore having a constant rise in delay which gives it a linear characteristic.

This observation proves that R_{imc} is a fabrication dependent parameter and not a technology dependent parameter as the change in delay is linear irrespective of the technology node.

5.2.4 Impact of length and technology scaling on propagation Delay

The RLC parameters of interconnect are intrinsic in nature and therefore varies with length. This variation of RLC with respect to length is directly proportional in nature. As RLC parameters increases with increase in length, it altogether results in increase of propagation delay (Fig. 5.4) .

However the impact of scaling on delay is slightly different. As it can be seen in that as technology node is scaled down, there is a increase in resultant propagation delay. It is important to note that the rate of increase of propagation delay with respect to length varies differently for different technology node.

32nm technology node

Table 5.9 Variation in parameters with respect to Length for 32nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	0.226	3.3185	6.8614	23p
500	0.913	16.593	34.307	154p
1000	1.77	33.185	68.614	446p
1500	2.63	49.778	102.92	879p
2000	3.49	66.37	137.92	1.44n
2500	4.34	82.96	171.54	2.15n
3000	5.2	99.55	205.84	3.01n

22nm technology node

Table 5.10 Variation in parameters with respect to Length for 22nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	0.527	5.8432	6.408	31p
500	2.25	29.212	32.041	262p
1000	4.404	58.432	64.082	840p
1500	6.558	87.648	96.112	1.73n

2000	8.7115	116.86	128.16	2.95n
2500	10.865	146.08	160.20	4.50n
3000	13.019	175.30	192.24	6.35n

16nm technology node

Table 5.11 Variation in parameters with respect to Length for 16nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	1.3233	9.995	5.8375	38p
500	5.959	49.774	29.137	500p
1000	11.753	99.55	58.275	1.78n
1500	17.547	149.32	87.412	3.85n
2000	23.341	199.10	116.55	6.71n
2500	29.135	248.87	145.69	10.30n
3000	34.929	298.65	174.82	14.65n

Comparison between MWCNT delays at different technology nodes

Table 5.12 Variation of delay in MWCNT with respect to Length for different technology nodes.

Length	**MWCNT Delay (s)**		
(µm)	**32nm**	**22nm**	**16nm**
100	23p	31p	38p
500	154p	262p	500p
1000	446p	840p	1.78n

1500	879p	1.73n	3.85n
2000	1.44n	2.95n	6.71n
2500	2.15n	4.50n	10.30n
3000	3.01n	6.35n	14.65n

Comparison between MWCNT/ Cu delay ratio at different technology nodes

Table 5.13 Variation of delay in MWCNT/Copper ratio with respect to Length for different technology node.

Length (µm)	**MWCNT/Cu Delay ratio**		
	32nm	**22nm**	**16nm**
100	0.54	0.492	0.287
500	0.322	0.276	0.202
1000	0.267	0.238	0.186
1500	0.245	0.223	0.111
2000	0.231	0.218	0.179
2500	0.225	0.214	0.177
3000	0.220	0.212	0.179

Based on above Tables and figures shown below, it is observed that when the length of an interconnects is increased its propagation delay also increases. This is because the intrinsic parameters of MWCNT are direct functions of length i.e. as the length increases the values of these parameters also increase as seen in Table 5.9-5.11. And as it is known that delay is directly proportional to these RLC parameters, therefore it also increases.

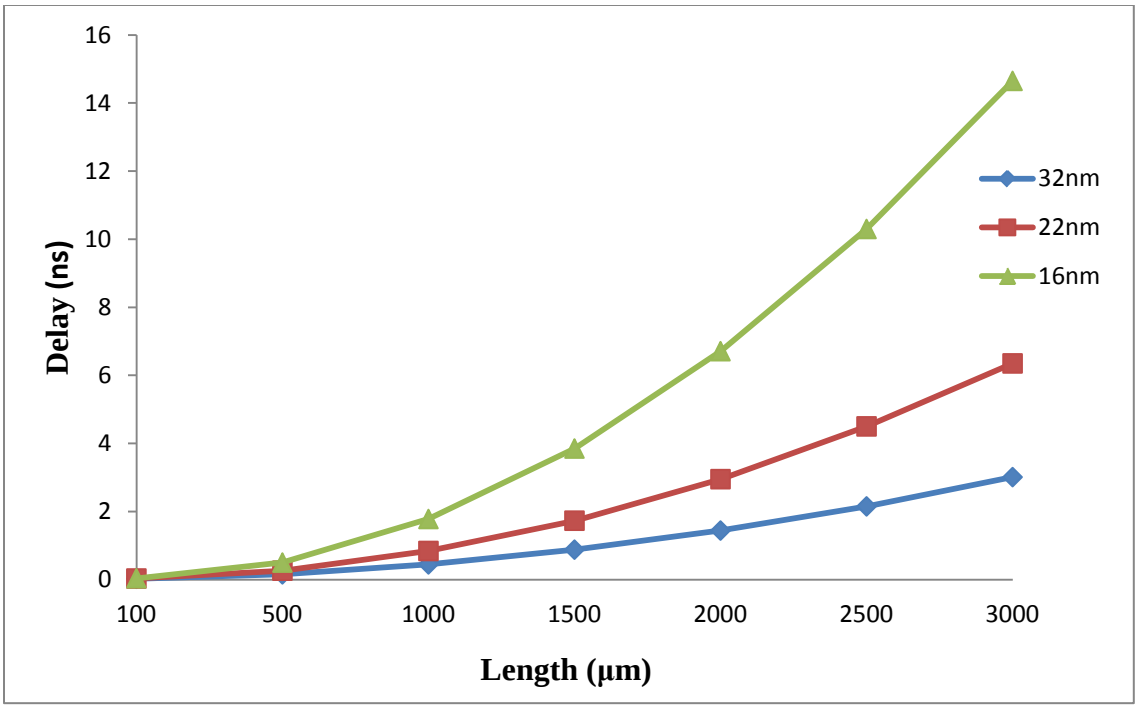

Fig. 5.5 Variation of delay in MWCNT at different Lengths for different technology node.

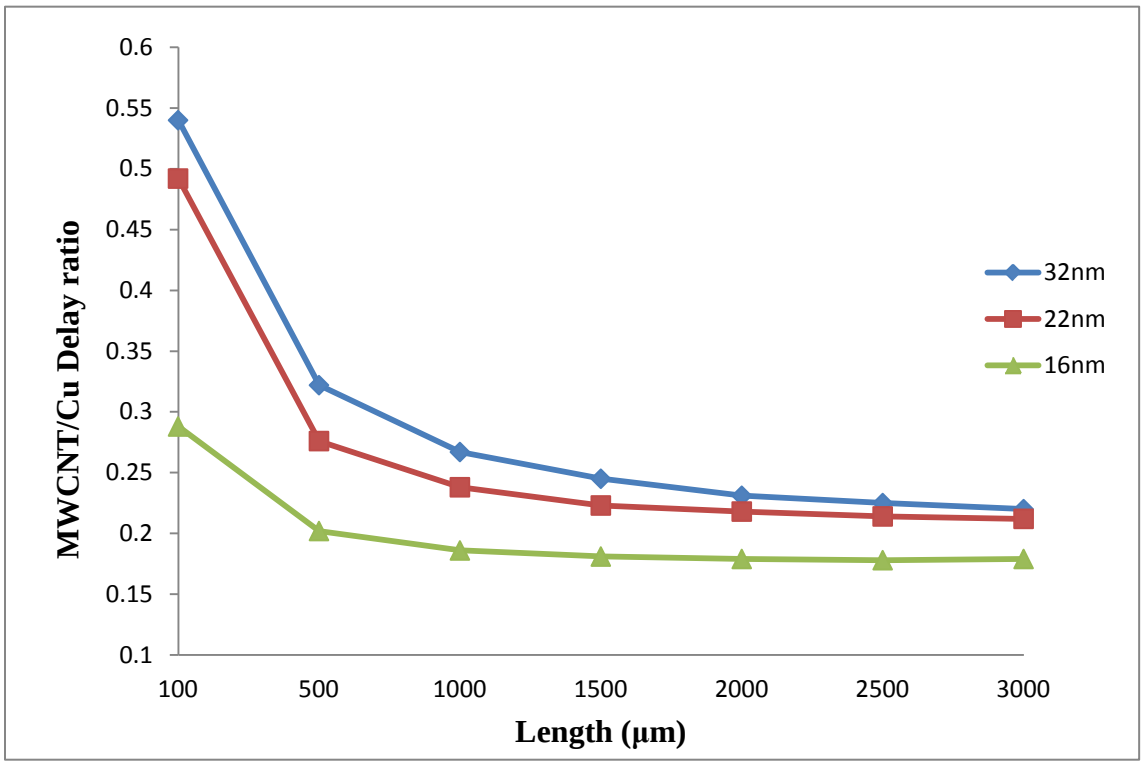

Fig. 5.6 Variation of delay in MWCNT/Copper ratio at different Lengths for different technology node.

Another observation is made that the rate of increase in delay is exponential even when the rate of increase of length is linear. This is so because the rate of increase in RLC parameters product with respect to length is also exponential which results in exponential increase in delay. It is also interesting to see that rate of exponential rise varies with technology i.e. smaller the technology node sharper the rise.

5.2.5 Repeaters (or Buffers) insertion

Repeaters are nothing but the buffers or inverters used in order to reduce the propagation delay. The role of repeaters is to reduce the length of interconnect into 'N' segments, where N represent number of repeaters and as it is already shown that propagation delay is dependent on Length of interconnect and therefore insertion of repeaters results in reduction of propagation delay. The repeater insertion causes reduction in the distributed parameters of interconnects by the factor of N as seen in Fig. 5.7.

For the simulation of ESC model the repeaters used are CMOS inverters and length of interconnect is considered to be 1000μm. The simulation results in Fig. 5.7. For the value 'N' at which the propagation delay reaches to its minimum value is considered to be optimum number of repeaters to be inserted.

Table 5.14 Delay variation due to insertion of repeaters at 32nm, 22nm and16nm technology nodes at 1000μm length.

No. of Repeaters	**Delay (s)**		
	32nm	**22nm**	**16nm**
1	446p	840p	1.78n
3	**222p**	282p	469p
5	237p	**248p**	337p
7	274p	255p	**300p**
9	316p	274p	300p

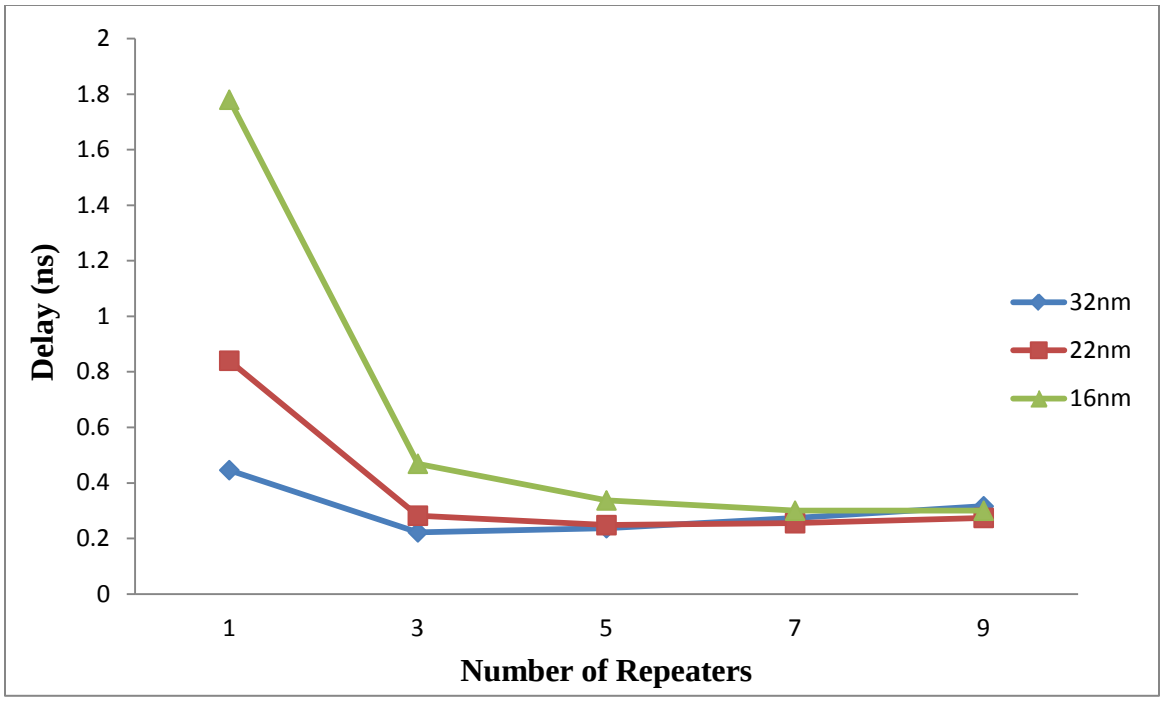

Fig. 5.7 Impact of Repeaters on propagation delay of MWCNT interconnect at global length of 1000μm for 32nm, 22nm and16nm technology nodes.

From Fig. 5.7 it is seen that as the number of repeaters inserted in an interconnect line increases the delay initially tends to decrease but after a certain value it again increases. This trend is because delay has a direct relation between the interconnect parameters and length, initially delay is dominated by length and with insertion of repeaters the overall length is divided into small length sections. For certain number of repeaters the delay of interconnect is minimum, this gives the value of optimum number of repeaters to be inserted. As the number of repeaters to be inserted is increased further, the domination of length is overshadowed by domination of the interconnect parameters on delay analysis and now the increase in delay is due to the interconnect parameters.

5.3 Variation in D_{max} to D_{min} Ratio

All the above analysis was based on the assumption that the ratio between D_{min} to D_{max} was 0.5 or in other words D_{min} was 0.5 times of D_{max}. But the growth procedures for MWCNT are not so accurate that it always maintains the D_{min} to D_{max} ratio to be 0.5. So now there is a need to study the effects when D_{min} to D_{max} is varied.

To study this variation, calculation and then simulations of RLC parameters for D_{min} to D_{max} ratio of 0.4, 0.5 and 0.6 at different technology nodes and different lengths is done.

At 32nm technology node.

(i) D_{min} = 0.4 D_{max} Number of shells (p) = 36

Table 5.15 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.4 at 32nm technology node.

Length (µm)	R (kΩ)	L (nH)	C (fF)	Delay (s)
100	0.206	2.89	6.8614	23p
500	0.839	14.45	34.307	149p
1000	1.63	28.90	68614	425p
1500	2.42	43.35	102.92	829p
2000	3.21	57.80	137.23	1.36n
2500	4.04	72.26	171.54	2.02n
3000	4.79	86.71	205.84	2.80n

(ii) D_{min} = 0.5 D_{max} Number of shells (p) = 30

Table 5.16 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.5 at 32nm technology node.

Length (µm)	R (kΩ)	L (nH)	C (fF)	Delay (s)
100	0.226	3.3185	6.8614	23p
500	0.913	16.593	34.307	154p
1000	1.771	33.185	68.614	446p
1500	2.63	49.778	102.92	879p

2000	4.487	66.372	137.23	1.44n
2500	4.340	82.961	171.54	2.15n
3000	5.200	99.553	205.84	3.01n

(iii) D_{min} **= 0.6** D_{max} **Number of shells (*p*) = 24**

Table 5.17 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.6 at 32nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	0.255	3.89	6.8614	23p
500	1.02	19.48	34.307	161p
1000	1.98	38.95	68.614	480p
1500	2.94	58.43	102.92	951p
2000	3.90	77.91	137.23	1.58n
2500	4.86	97.39	171.54	3.36n
3000	5.82	116.9	205.84	3.29n

Comparison with copper

Table 5.18 Variation of delay of Copper, MWCNT, and MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) at 32nm technology node.

Length (µm)	**Copper Delay (s)**	**MWCNT Delay (s)** D_{min} **= X.** D_{max}			**MWCNT/ Cu Delay Ratio** D_{min} **= X.** D_{max}		
		X=0.4	**X=0.5**	**X=0.6**	**X=0.4**	**X=0.5**	**X=0.6**
100	43p	23p	23p	23p	0.535	0.535	0.535
500	478p	149p	154p	161p	0.312	0.322	0.337
1000	1.67n	425p	446p	480p	0.254	0.267	0.287
1500	3.59n	829p	879p	951p	0.231	0.245	0.265

2000	6.22n	1.36n	1.44n	1.58n	0.218	0.231	0.254
2500	9.55n	2.02n	2.15n	2.36n	0.211	0.225	0.247
3000	13.6n	2.80n	3.01n	3.29n	0.206	0.220	0.242

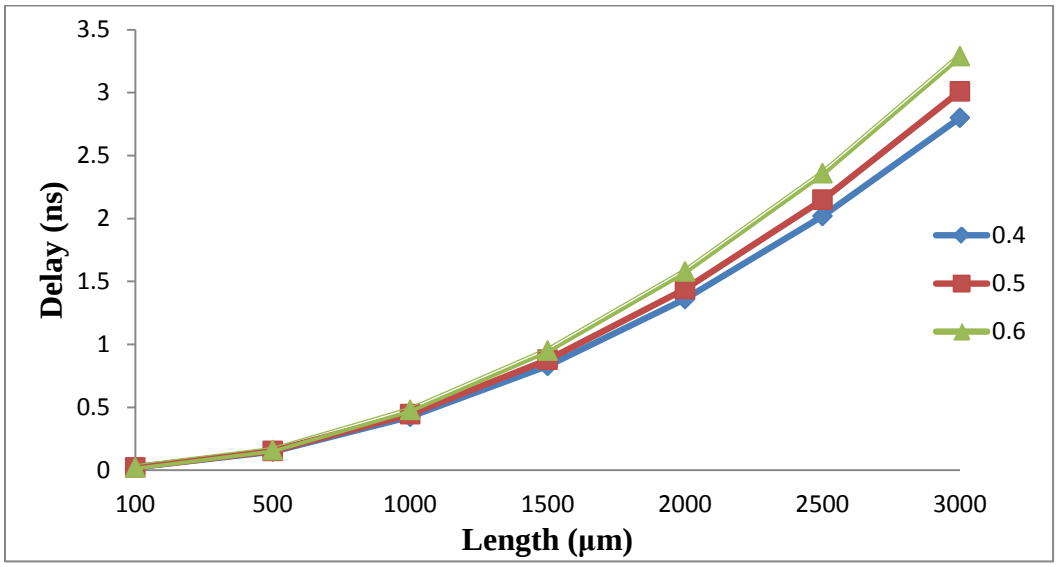

Fig. 5.8 Variation of delay in MWCNT at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 32nm technology node.

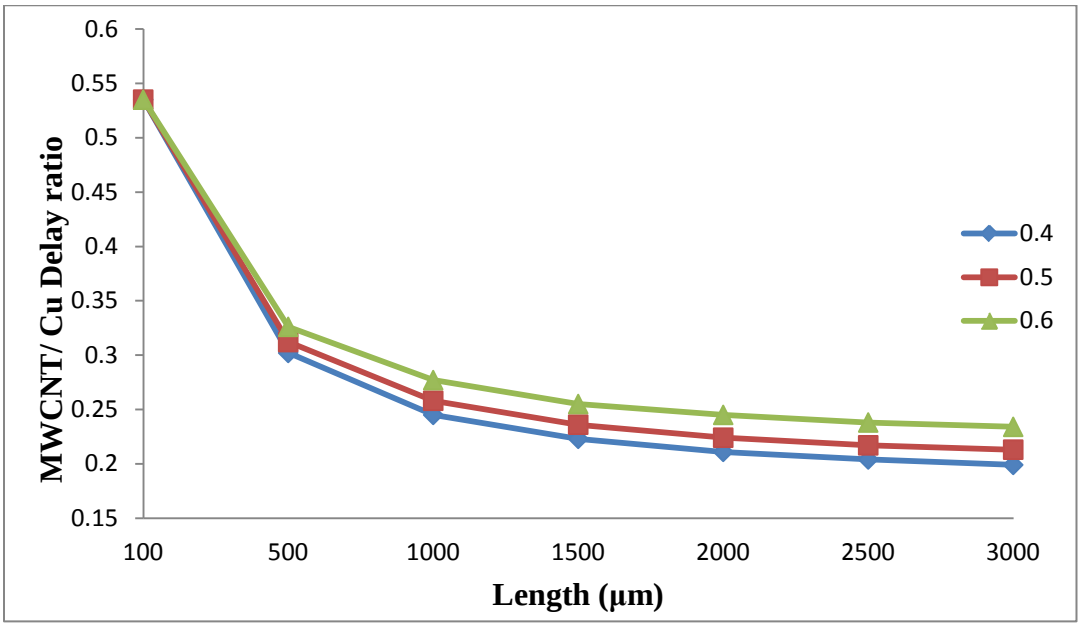

Fig. 5.9 Variation of delay in MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 32nm technology node.

The change in RLC parameters and delay with variation of length at D_{min} to D_{max} ratio 0.4, 0.5 and 0.6 is observed in Table 5.15-5.17 respectively for 32nm technology node.

Based on Table 5.18 delay in MWCNT and a delay ratio of MWCNT and copper vs length has also been plotted for different D_{min} to D_{max} ratio as seen in Fig. 5.8-5.9 respectively

At 22nm technology node.

(i) D_{min} = 0.4 D_{max} Number of shells (p) = 25

Table 5.19 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.4 at 22nm technology node.

Length (µm)	R (kΩ)	L (nH)	C (fF)	Delay (s)
100	0.474	4.9776	6.408	30p
500	2.039	24.89	32.041	246p
1000	3.994	49.77	64.082	779p
1500	5.949	74.663	96.122	1.60n
2000	7.903	99.55	128.16	2.71n
2500	9.858	124.44	160.20	4.10n
3000	11.813	149.33	192.24	5.82n

(ii) D_{min} = 0.5 D_{max} Number of shells (p) = 21

Table 5.20 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.5 at 22nm technology node.

Length (µm)	R (kΩ)	L (nH)	C (fF)	Delay (s)
100	0.527	5.8432	6.408	31p
500	2.253	29.216	32.041	262p
1000	4.4043	58.432	64.082	840p

1500	6.5581	87.648	96.122	1.73n
2000	8.7115	116.86	128.16	2.95n
2500	10.865	146.08	160.20	4.50n
3000	13.019	175.30	192.24	6.35n

(iii) $D_{min} = 0.6\ D_{max}$ **Number of shells (*p*) = 17**

Table 5.21 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.6 at 22nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	0.606	7.07	6.408	32p
500	2.5728	35.367	32.041	288p
1000	5.03	70.734	64.082	935p
1500	7.4874	106.10	96.122	1.95n
2000	9.9447	141.47	128.16	3.31n
2500	12.402	176.83	160.20	5.05n
3000	14.859	212.20	192.24	7.17n

Comparison with copper

Table 5.22 Variation of delay of Copper, MWCNT, and MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) at 22nm technology node.

Length (µm)	**Copper Delay (s)**	**MWCNT Delay (s)** $D_{min} = X.\ D_{max}$			**MWCNT/ Cu Delay Ratio** $D_{min} = X.\ D_{max}$		
		X=0.4	**X=0.5**	**X=0.6**	**X=0.4**	**X=0.5**	**X=0.6**
100	63p	30p	31p	32p	0.476	0.492	0.508
500	948p	246p	262p	288p	0.259	0.276	0.303

1000	3.53n	779p	840p	935p	0.212	0.238	0.256
1500	7.75n	1.60n	1.73n	1.95n	0.206	0.223	0.251
2000	13.53n	2.71n	2.95n	3.31n	0.200	0.218	0.244
2500	21.03n	4.10n	4.50n	5.05n	0.195	0.214	0.240
3000	29.94n	5.82n	6.35n	7.17n	0.194	0.212	0.239

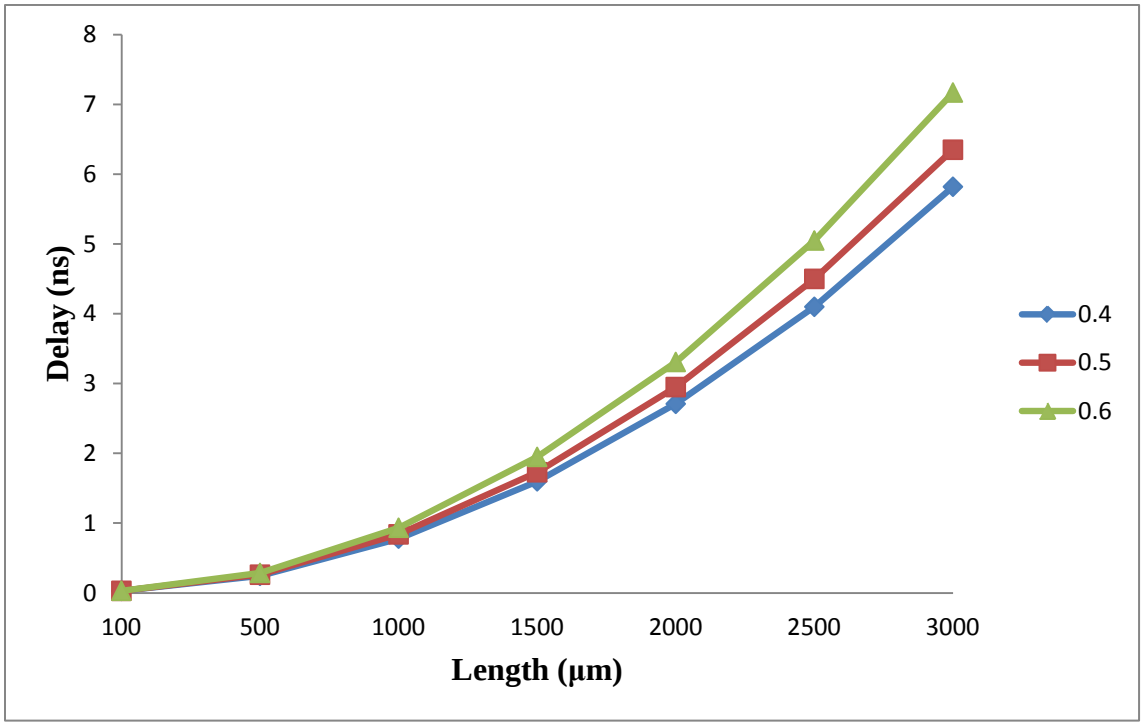

Fig. 5.10 Variation of delay in MWCNT w.r.t Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 22nm technology node.

The change in RLC parameters and delay with variation of length at D_{min} to D_{max} ratio 0.4, 0.5 and 0.6 is observed in Table 5.19-5.21 respectively for 22nm technology node.

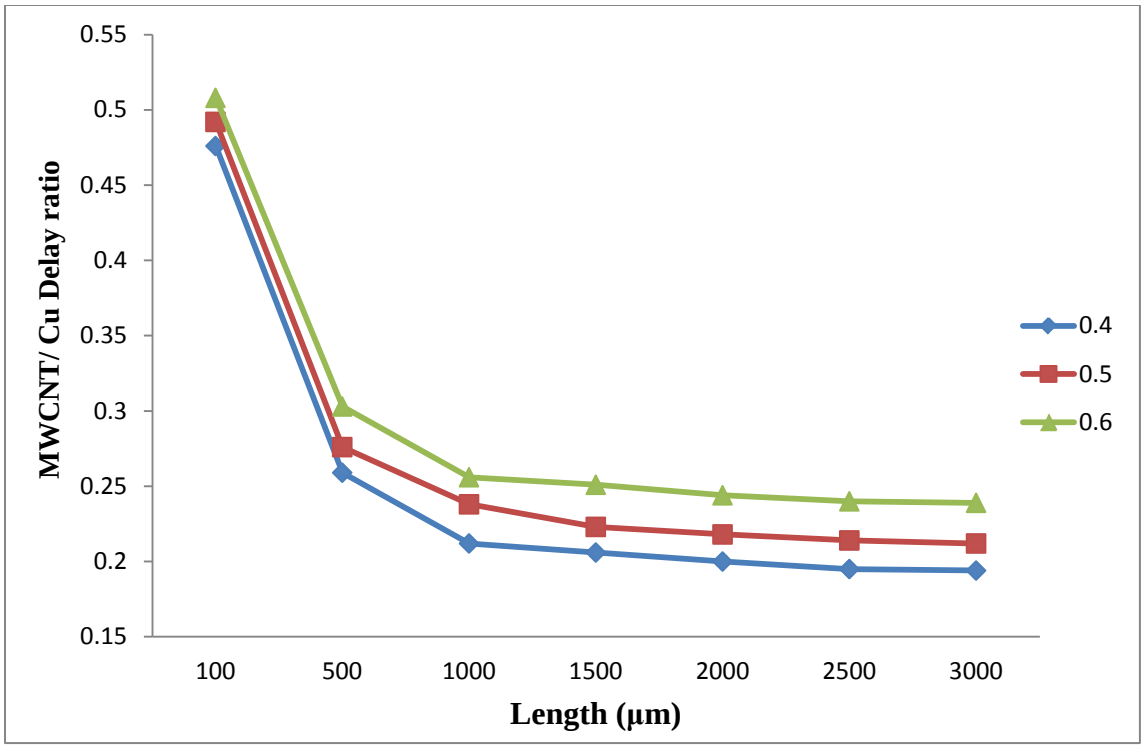

Fig. 5.11 Variation of delay in MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 22nm technology node.

Based on Table 5.22 delay in MWCNT vs length and delay ratio of MWCNT and copper vs length length has also been plotted for different D_{min} to D_{max} ratio as seen in Fig respectively

At 16nm technology node.

(i) D_{min} = 0.4 D_{max} Number of shells (p) = 16

Table 5.23 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.4 at 16nm technology node.

Length (µm)	R (kΩ)	L (nH)	C (fF)	Delay (s)
100	1.2647	9.268	5.8275	37p
500	5.705	46.34	29.137	483p

1000	11.256	92.68	58.275	1.71n
1500	16.807	139.02	87.412	3.70n
2000	22.357	185.37	116.55	6.43n
2500	27.907	231.71	145.69	9.91n
3000	33.485	278.05	174.82	14.01n

(ii) $D_{min} = 0.5\ D_{max}$ **Number of shells (*p*) =14**

Table 5.24 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.5 at 16nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	1.3233	9.955	5.8275	38p
500	5.959	49.774	29.137	500p
1000	11.753	99.55	58.275	1.78n
1500	17.547	149.32	87.412	3.85n
2000	23.341	199.10	116.55	6.71n
2500	29.135	248.87	145.69	10.30n
3000	34.929	298.65	174.82	14.65n

(iii) $D_{min} = 0.6\ D_{max}$ **Number of shells (*p*) = 11**

Table 5.25 Variation of parameters with respect to Length for D_{min} to D_{max} ratio as 0.6 at 16nm technology node.

Length (µm)	**R (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**
100	1.538	12.217	5.8275	40p

500	6.893	61.087	29.137	564p
1000	13.587	122.17	58.275	2.03n
1500	20.974	183.26	87.412	4.41n
2000	26.974	244.35	116.55	7.67n
2500	33.668	305.43	145.69	11.87n
3000	40.362	366.52	174.82	16.71n

Comparison with copper

Table 5.26 Variation of delay of Copper, MWCNT, and MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) at 16nm technology node.

Length (µm)	**Copper Delay (s)**	**MWCNT Delay (s)** D_{min} = X. D_{max}			**MWCNT/ Cu Delay Ratio** D_{min} = X. D_{max}		
		X=0.4	**X=0.5**	**X=0.6**	**X=0.4**	**X=0.5**	**X=0.6**
100	132p	37p	38p	40p	0.270	0.288	0.303
500	2.47n	483p	500p	564p	0.195	0.202	0.228
1000	9.56n	1.71n	1.78n	2.03n	0.179	0.186	0.212
1500	21.23n	3.70n	3.85n	4.41n	0.174	0.181	0.208
2000	37.49n	6.43n	6.71n	7.67n	0.172	0.179	0.204
2500	57.95n	9.91n	10.30n	11.87n	0.171	0.178	0.201
3000	81.55n	14.01n	14.65n	16.71n	0.172	0.179	0.205

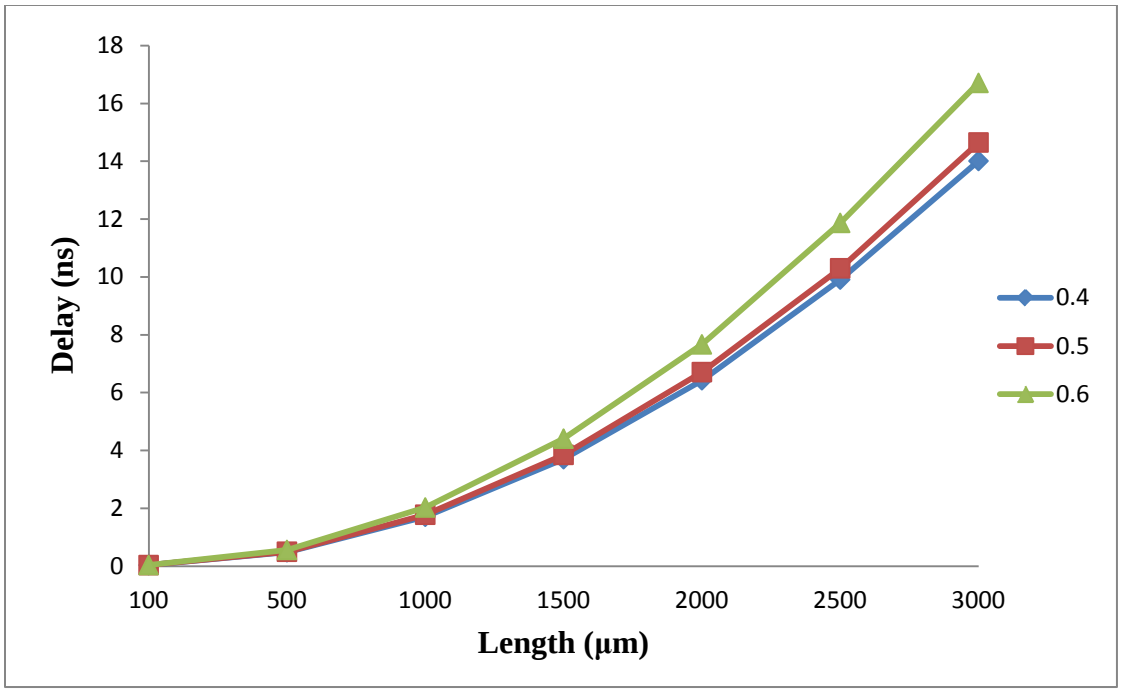

Fig. 5.12 Variation of delay in MWCNT at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 16nm technology node.

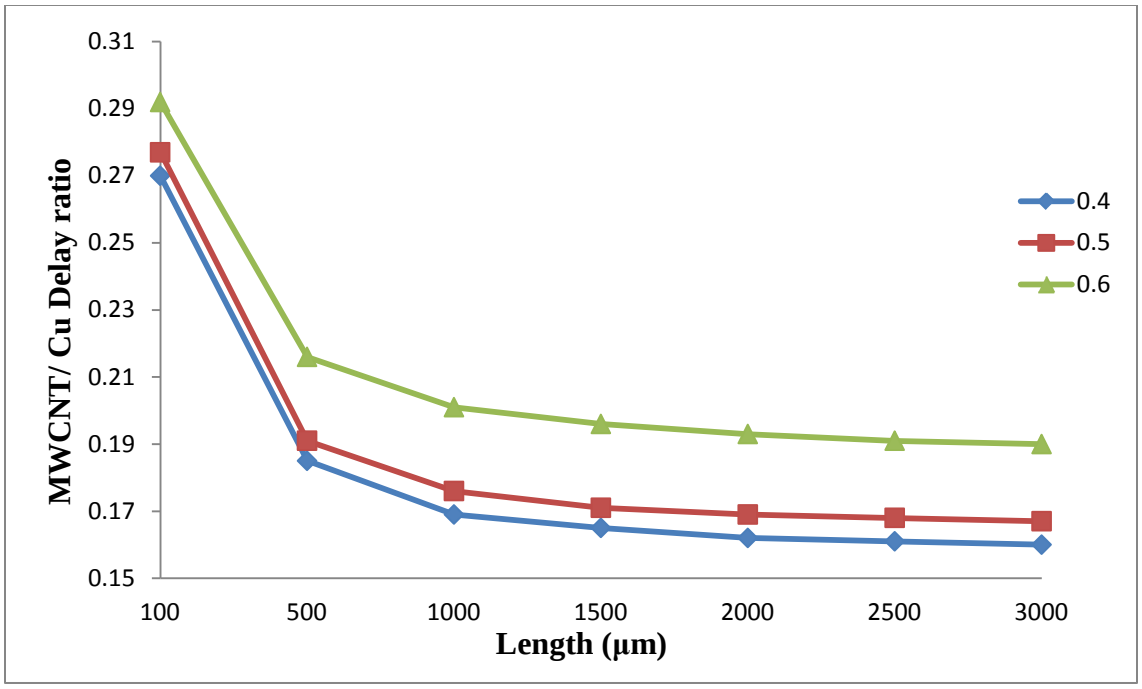

Fig. 5.13 Variation of delay in MWCNT/Copper ratio at different Lengths for different D_{min} to D_{max} ratio (0.4, 0.5, 0.6) for 16nm technology node.

The change in RLC parameters and delay with variation of length at D_{min} to D_{max} ratio 0.4, 0.5 and 0.6 is observed in Table 5.24-5.27 respectively for 16nm technology node.

Based on Table 5.23-5.26 delay in MWCNT vs length and delay ratio of MWCNT and copper vs length has also been plotted for different D_{min} to D_{max} ratio as seen in Fig. 5.12-5.13 respectively

From Table 5.28 and Fig. 5.12 it is observed that as length increases delay of the system also increases but it is also observed that the delay at a particular length is more for D_{min} to D_{max} ratio of 0.6 than that compared at 0.4. This is because as D_{min} to D_{max} ratio of a MWCNT is varied the total number of shells are also varied i.e. lower the ratio more number of shells and as number of shells increases propagation delay decreases. As the propagation delay is dependent on the intrinsic parameters of MWCNT interconnect and as number of shells increases, more number of parallel network which altogether reduces the impact of intrinsic parameters which indeed results in decrease of the propagation delay.

CHAPTER 6
INTERSHELL INTERACTION

6.1 Intershell interaction

Intershell interaction is caused due to intershell tunneling where tunneling is a quantum phenomena which come into effect when a partical travels through a forbidden region neglecting the laws of classical physics [8]. In other words, in classical physics electrons move through conductors only and not through insulators, however if a thin film of insulator is placed between two conductors, the electrons can tunnel through one conductor to reach the other conductor. This happens due to extended wave function of the conductors into the insulating layer.

In a CNT shell, each carbon atom contains four valance electrons, three are tightly bonded by the neighboring carbon atoms while the fourth electron (called π-orbital electron) is independent and moves freely contributing to the conduction phenomena of CNT. In MWCNT two adjacent shells are separated by a small distance *d* (≈ *0.34nm)* Van der Waal distance) which causes π-orbital overlap resulting in intershell interaction caused due to intershell tunneling or hopping [16]. These intershell interactions are responsible for electromagnetic propagation in MWCNT [40].

Intershell interaction observed in MWCNT is of two types :-

(i) Intershell inductance (Mutual inductance)

(ii) Intershell conductance (Tunneling conductance)

6.1.1 Intershell Mutual inductance

For an MWCNT there exists another type of inductance called mutual inductance. It arises due to magnetic coupling between shells of an interconnect. The mutual inductance per unit length between shells is obtained using equation:-

$$M_{shell} = \frac{\mu}{2\pi}\left[\ln\left(\frac{4L}{D_{Out}}\right) - 1 + \frac{D_{Out} + D_{In}}{\pi L}\right] \tag{6.1}$$

Where L is the length, and D_{in} and D_{out} are the diameters of the inner and outer shells of the coaxial structure. The mutual inductance between shells can ranges around few pH/μm and therefore can be ignored as it is much smaller when compared with the kinetic inductance of the shell which lies in range of nH/μm. [27,40]

6.1.2 Intershell Tunneling conductance

In MWCNT, ideally the two adjacent shells are insulated from one another separated by a small distance '*d*', but when the electrons in a shell get excited it crosses the small distance '*d*' reaching to the adjacent shell and thus creating a conductive path between two shells. As the conductive path is due to the tunneling of electrons from one shell to another and therefore the conductance introduced is called intershell tunneling conductance and is given by the formula:-

$$G_{T_i} = \frac{\sigma}{d} \cdot \pi D_i \tag{6.2}$$

In this σ is tunneling conductivity $(\Omega.m)^{-1}$ and D_i is diameter of the outer one of the two adjacent shells. The σ/d is called as normalized tunneling conductivity and for $d= 0.34nm$ its given as $0.3(\mu\Omega.cm^2)^{-1}$ [27]. Theoretically the impact of tunneling conductance only exist if the distance between the two adjacent shell i.e.'*d*' is less than or equal to the Van der Waal distance (i.e $d \leq 0.34nm$). For the distance greater than Van der Waal distance the impact of tunneling conductance is negligible and is therefore ignored [16].

6.2 Modified Multi-conductor circuit (MCC) model of an MWCNT

In the above given MCC model (Fig. 1.4) the influence of intershell tunneling on to the circuit was neglected. In order to study the impact of intershell tunneling, MCC model is to be modified. The modified MCC model can be seen in Fig. 6.1

In modified MCC model, the tunneling conductance is observed between two adjacent shells while mutual inductance is between different shells. Impact of tunneling conductance is from outer shell onto the adjacent inner shell. Similarly the impact of mutual inductance is also from outer shell onto the inner shells. Other parameters of the MCC model remain unchanged [40].

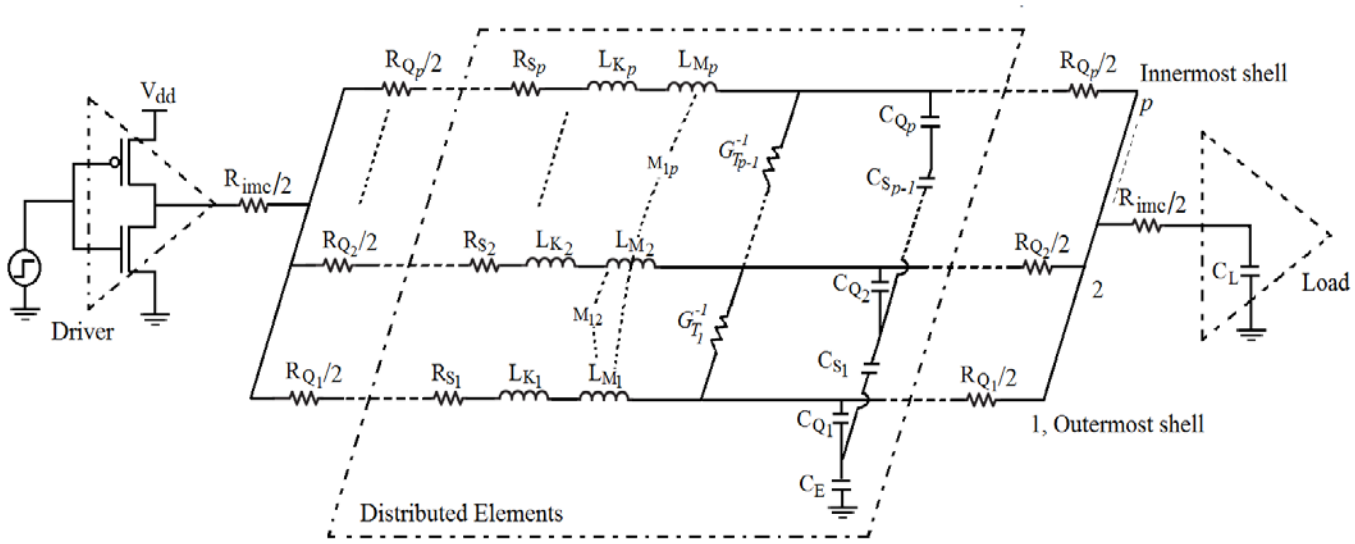

Fig. 6.1 Modified MCC model of a *p* shell MWCNT. [27,49]

6.3 Realization of ESC model from modified MCC model

ESC model has already been designed for MCC model without considering intershell tunneling (both mutual inductance, tunneling conductance). However if tunneling conductance is only considered (i.e. mutual inductance is ignored), the overall resistance of the model changes whereas the total inductance and the capacitance still remains unchanged.

The arrangement for resistances in the modified MCC model is shown in the Fig. 6.2

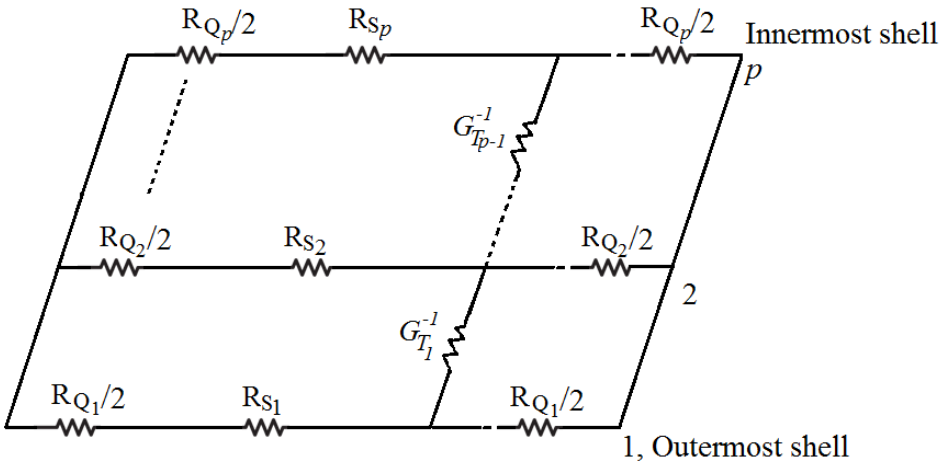

Fig.6.2 Realization of equivalent resistance by including tunneling conductance.

In order to obtain equivalent resistance considering tunneling,

Let, $R_{SS}(i) = R_S(i) + R_Q(i)/2$ (6.3)

The values are calculated using Star to Delta transformation technique:-

Assume,

$R_a(1) = R_{SS}(1)$ and $R_b(1) = R_Q(1)/2$ (6.4)

$\Delta R(i) = R_a(i) \times G_T^{-1}(i) + R_a(i) \times R_b(i) + R_b(i) \times G_T^{-1}(i)$, $i = 1,2.....p$ (6.5)

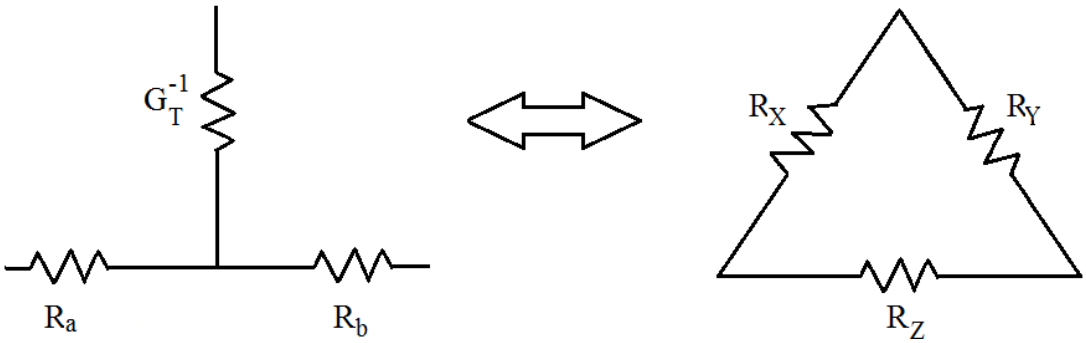

Fig. 6.3 Star-Delta transformation

Now applying Star to Delta transform,

$$R_X(i) = \frac{\Delta R(i)}{R_b(i)}, \quad R_Y(i) = \frac{\Delta R(i)}{R_a(i)}, \quad R_Z(i) = \frac{\Delta R(i)}{G_T^{-1}(i)} \tag{6.6}$$

$$\begin{cases} R_a^{-1}(i+1) = R_{SS}^{-1}(i+1) + R_X^{-1}(i) \\ R_b^{-1}(i+1) = R_Q^{-1}(i+1)/2 + R_Y^{-1}(i) \end{cases} \quad i = 1,2.....p \tag{6.7}$$

$$G_Z = \sum_{i=1}^{p-1} R_Z^{-1} \tag{6.8}$$

The equivalent resistance including tunneling (R_T) is given as:-

$$R_T^{-1} = (R_a(p) + R_b(p))^{-1} + G_Z \tag{6.9}$$

Using the above obtained equation for equivalent resistance with tunneling (R_T) and the previously obtained equations for equivalent inductance (equation 4.2) and equivalent capacitance (equation 4.6) an ESC model is also modified and used for simulation.

6.4 Results and discussions

In chapter 5 the impact of tunneling conductance was ignored. Whereas this section tries to prove that as the technology node decreases the impact of tunneling conductance increases and can no longer be ignored

By considering the previous defined ITRS parameters (in Table 4.1), the impact of tunneling conductance and the variation it bring in equivalent resistance and propagation delay is studied. In Table 6.1-6.3 both the impact of equivalent resistance with and without considering tunneling conductance on to the propagation delay is shown with respect to length for D_{min} to D_{max} ratio 0.5 and at different technology nodes. Impact of mutual inductance is still ignored therefore equivalent inductance remains unchanged, equivalent capacitance also remains unchanged for both the cases. In the tables given below, R is equivalent resistance without considering tunneling while R_T is equivalent resistance when tunneling conductance is considered. Similarly is for delay with and without tunneling.

32nm technology node

Table 6.1 Variation in parameters with respect to Length for 32nm technology node when tunneling conductance is considered.

Length (µm)	**R (kΩ)**	**R_T (kΩ)**	**L (nH)**	**C (fF)**	**Delay (s)**	**Delay.T (s)**
100	0.226	0.234	3.3185	6.8614	23.27p	23.62p
500	0.913	0.940	16.593	34.307	154p	157p
1000	1.77	1.818	33.185	68.614	446p	453.6p
1500	2.63	2.69	49.778	102.92	879p	892p
2000	3.49	3.56	66.37	137.92	1.44n	1.459n
2500	4.34	4.415	82.96	171.54	2.15n	2.175n
3000	5.2	5.28	99.55	205.84	3.01n	3.042n

22nm technology node

Table 6.2 Variation in parameters with respect to Length for 22nm technology node when tunneling conductance is considered.

Length (µm)	R (kΩ)	R_T (kΩ)	L (nH)	C (fF)	Delay (s)	Delay.T (s)
100	0.527	0.551	5.8432	6.408	31.4p	32.4p
500	2.25	2.337	29.212	32.041	262p	269p
1000	4.404	4.53	58.432	64.082	840p	859p
1500	6.558	6.708	87.648	96.112	1.73n	1.762n
2000	8.711	8.87	116.86	128.16	2.95n	2.995n
2500	10.865	11.03	146.08	160.20	4.50n	4.558n
3000	13.019	13.195	175.30	192.24	6.35n	6.422n

16nm technology node

Table 6.3 Variation in parameters with respect to Length for 16nm technology node when tunneling conductance is considered.

Length (µm)	R (kΩ)	R_T (kΩ)	L (nH)	C (fF)	Delay (s)	Delay.T (s)
100	1.32	1.43	9.995	5.8375	38.18p	40.24p
500	5.96	6.27	49.774	29.137	500p	521p
1000	11.75	12.135	99.55	58.275	1.78n	1.834n
1500	17.547	17.96	149.32	87.412	3.85n	3.938n
2000	23.34	23.77	199.10	116.55	6.71n	6.833n
2500	29.135	29.576	248.87	145.69	10.30n	10.456n
3000	34.93	35.38	298.65	174.82	14.65n	14.837n

Comparison between Resistance with and without considering tunneling conductance.

Table 6.4 Determining difference, ratio and percentage change between resistance with and without considering tunneling conductance at different technology nodes.

Length (μm)	**$R_T - R$ (kΩ) (equivalent resistance difference)**			**R / R_T (equivalent resistance ratio)**			**$(R_T - R)/R \times 100$ (%) (equivalent resistance percentage change)**		
	32nm	**22nm**	**16nm**	**32nm**	**22nm**	**16nm**	**32nm**	**22nm**	**16nm**
100	0.008	0.024	0.11	0.966	0.956	0.923	3.5398	4.5540	8.3334
500	0.028	0.087	0.31	0.970	0.963	0.950	3.0701	3.6667	5.2013
1000	0.048	0.13	0.385	0.9736	0.971	0.968	2.7118	2.9545	3.2766
1500	0.09	0.148	0.413	0.9777	0.978	0.977	2.2813	2.2561	2.3536
2000	0.07	0.16	0.43	0.980	0.982	0.982	2.0057	1.8369	1.8423
2500	0.075	0.17	0.441	0.983	0.9846	0.985	1.7281	1.5653	1.5136
3000	0.08	0.175	0.45	0.985	0.9867	0.9877	1.5384	1.3440	1.2882

It can be seen in Table 6.4 that as the length increases or technology node decreases, the difference and ratio between equivalent resistance with and without tunneling conductance also increases which can be seen in Fig. 6.4 -6.5.

However the overall impact of tunneling conductance onto the equivalent resistance decreases with respect to increasing length or decreasing technology node, which is seen in Fig. 6.6. It is because the rate of increase in equivalent resistance with respect to length is greater than the effect caused by the increase in tunneling conductance onto the equivalent resistance. Fig. 6.4 also proves that tunneling conductance is more serious issue at smaller (local) length than that at global length.

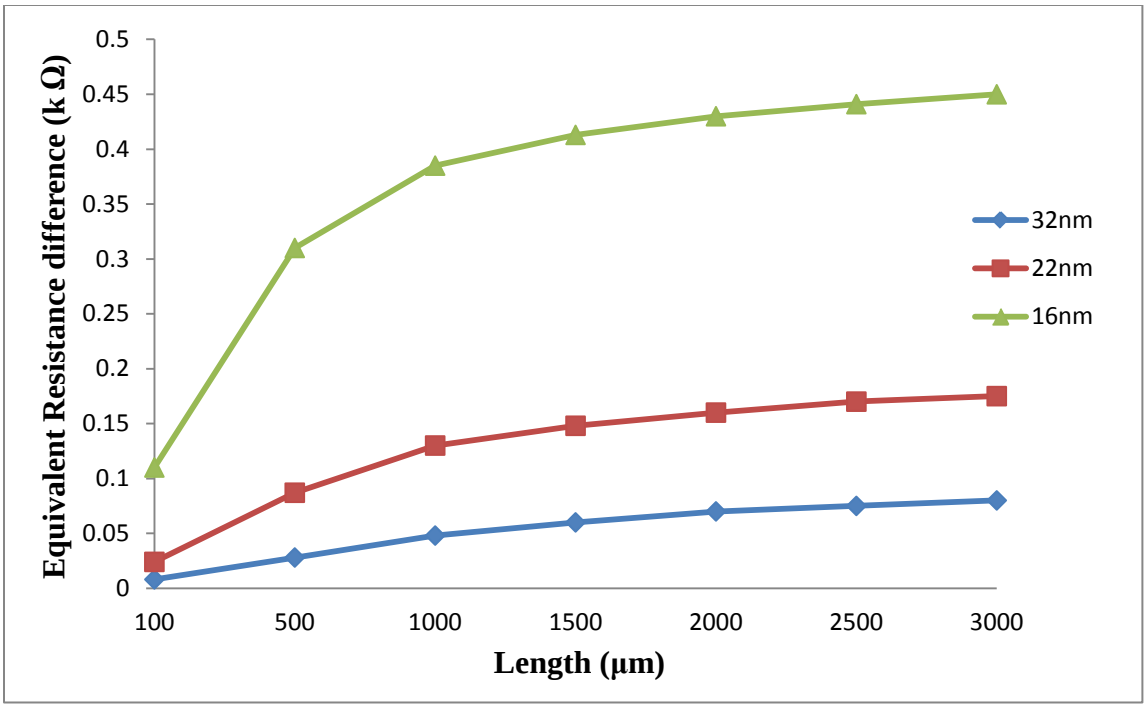

Fig. 6.4 Equivalent Difference between resistance with and without considering tunneling effect with respect to length at different technology nodes.

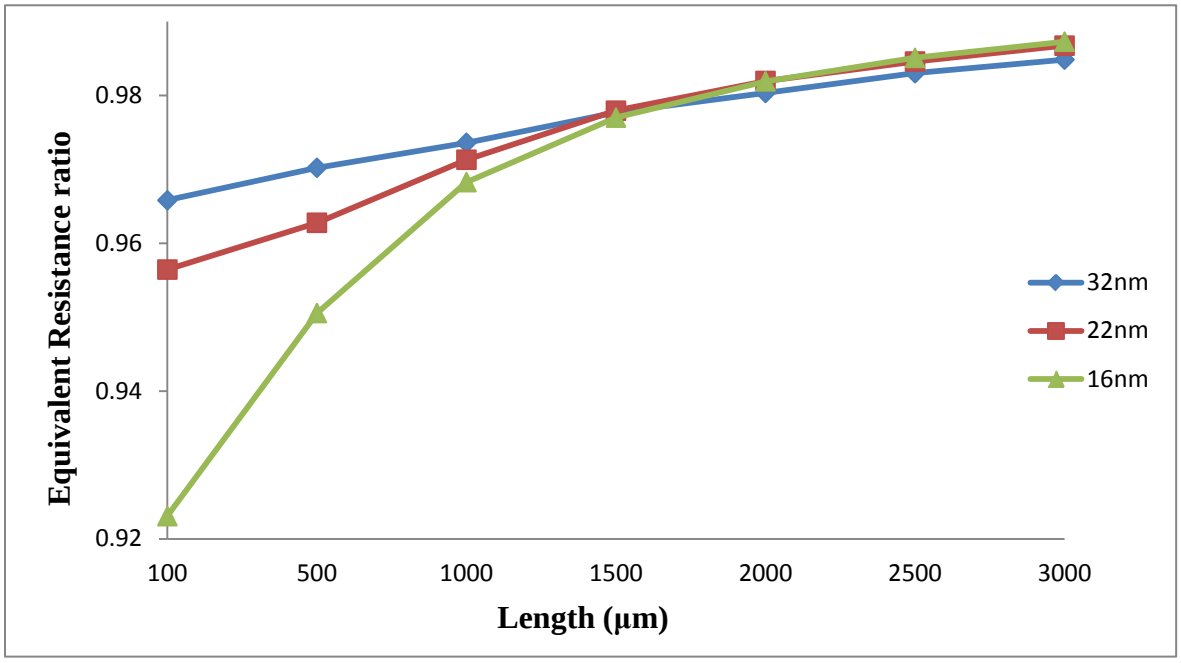

Fig. 6.5 Equivalent Resistance ratio with and without considering tunneling effect with respect to length at different technology nodes.

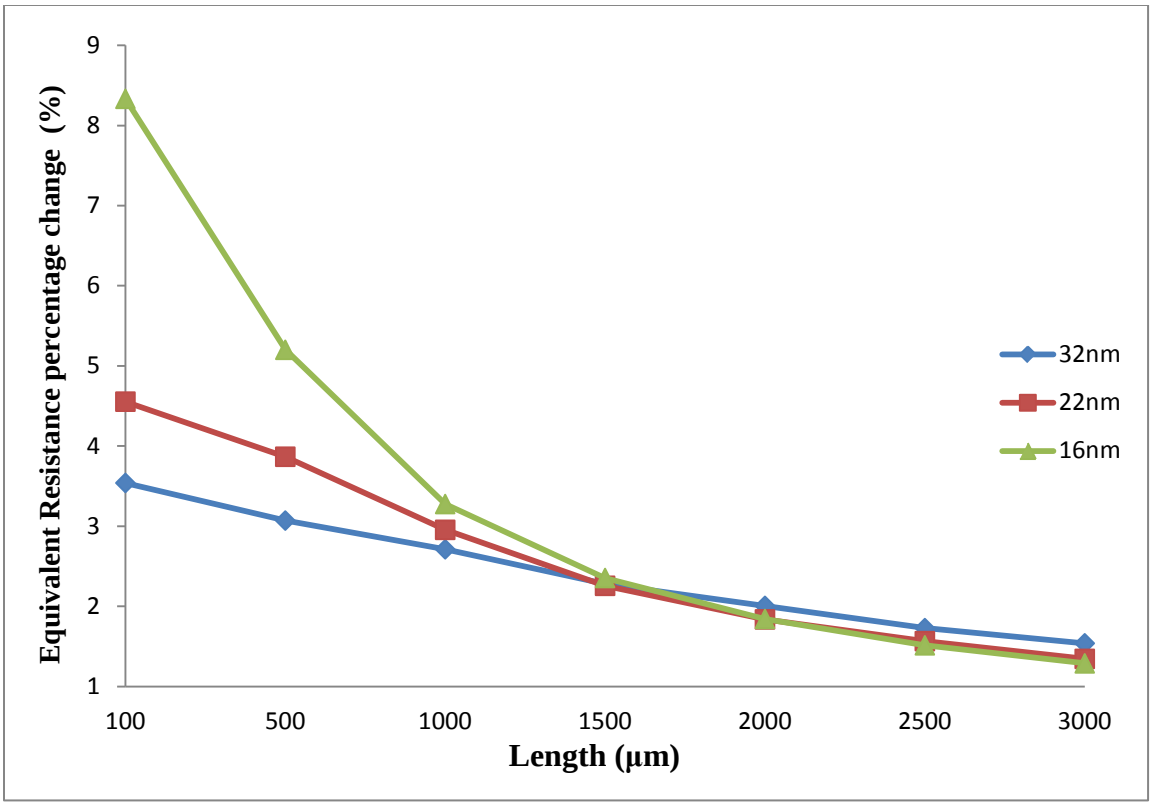

Fig. 6.6 Equivalent percentage change between resistance with and without considering tunneling effect with respect to length at different technology nodes.

It is interesting to observe that rate of increase in R_T/R ratio (Fig. 6.5) and rate of decrease in percentage change in resistance (Fig. 6.6) becomes faster with decreasing technology nodes with respect to length.

This is because as the technology node decreases, the number of shells in MWCNT decreases whereas the rate of change of equivalent resistance with respect to length increases. The rate of increase in equivalent resistance is observed to be sharper than the impact of tunneling conductance onto the equivalent resistance at lower technology nodes, which proves that as with decreasing technology nodes the rate of increase in R_T/R ratio (Fig. 6.5) and rate of decrease in percentage change in resistance (Fig. 6.6) becomes faster or sharper.

Due to tunneling conductance the equivalent resistance increase which results in the increase in propagation delay. The variation in delay due to tunneling conductance is analyzed in Table 6.5.

Comparison between Delay with and without considering tunneling conductance.

Table 6.5 Determining difference, ratio and percentage change between Delay with and without considering tunneling conductance at different technology nodes.

Length (μm)	**Delay.T- Delay (s) (normalized delay difference)**			**Delay / Delay.T (normalized delay ratio)**			**$(\text{Delay.T} - \text{Delay})/\text{Delay} \times 100$ (%) (normalized delay percentage change)**		
	32nm	**22nm**	**16nm**	**32nm**	**22nm**	**16nm**	**32nm**	**22nm**	**16nm**
100	0.53p	1p	2.06p	0.9777	0.9691	0.9488	2.277	3.184	5.395
500	3p	7p	21p	0.9809	0.9739	0.9596	1.948	2.671	4.20
1000	7.6p	19p	54p	0.9832	0.9778	0.9705	1.704	2.262	3.034
1500	13p	32p	88p	0.9854	0.9818	0.9776	1.479	1.849	2.285
2000	19p	45p	123p	0.9869	0.9849	0.9820	1.319	1.525	1.833
2500	25p	58p	156p	0.9885	0.9872	0.9850	1.162	1.289	1.514
3000	32p	72p	187p	0.9895	0.9887	0.9873	1.063	1.134	1.276

It can be seen in Table 6.5 that as the length increases or technology node decreases, the difference and ratio between delay with and without tunneling also increases which can be seen in Fig. 6.7 -6.8.

However the overall impact of tunneling conductance onto the delay decreases with respect to increasing length or decreasing technology node, which can be seen in Table. 6.5. It is because delay is proportional to resistance and as the rate of percentage change in resistance (as seen in Table 6.4) decreases with length which also causes the percentage delay change to decrease which can be seen in Fig. 6.9.

Fig. 6.9 strengthens the observation made above that tunneling conductance is more serious issue at smaller (local) length than that at global length.

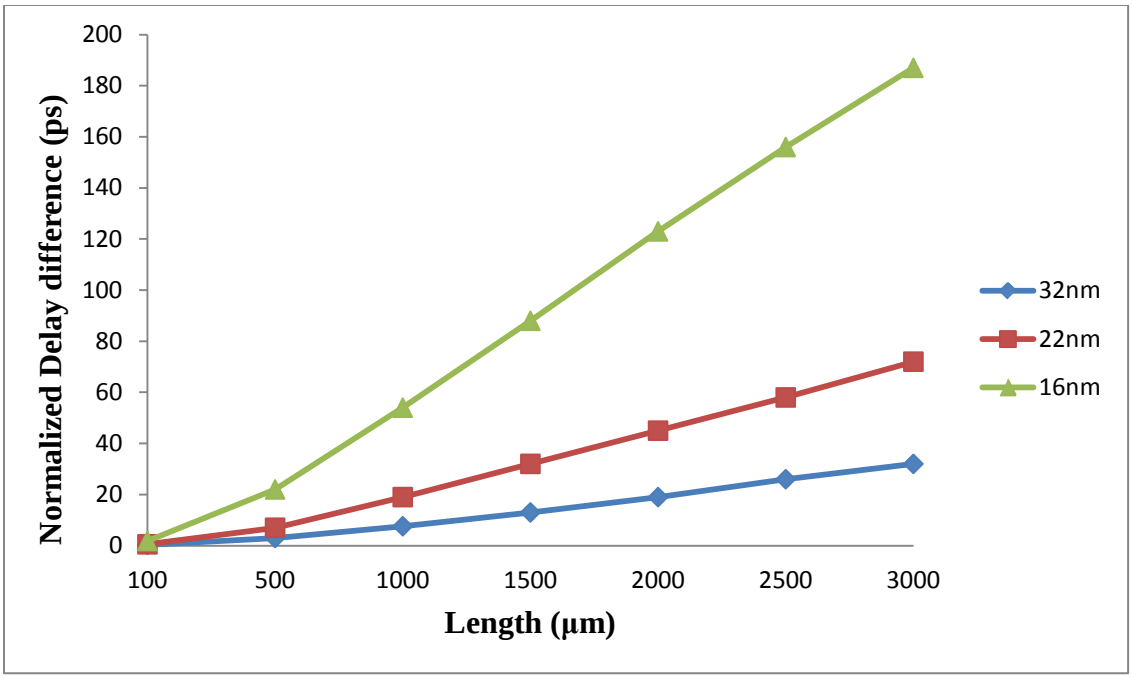

Fig. 6.7 Normalize difference between Delay with and without considering tunneling effect with respect to length at different technology nodes.

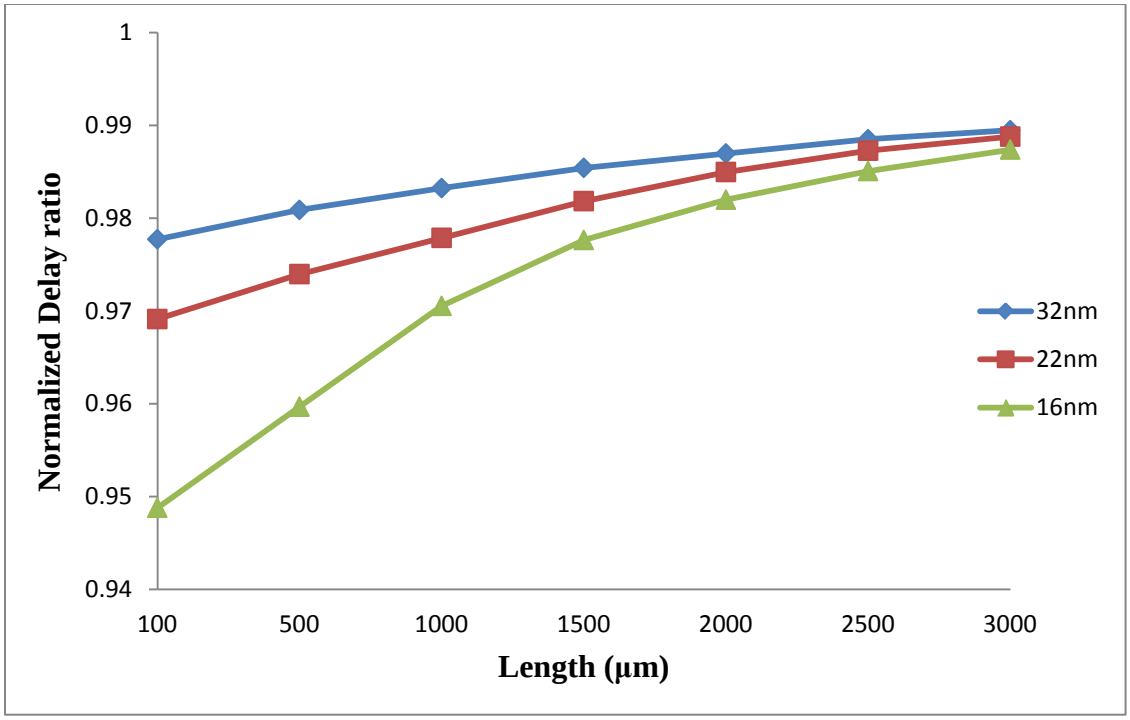

Fig. 6.8 Normalize delay ratio with and without considering tunneling effect with respect to length at different technology nodes.

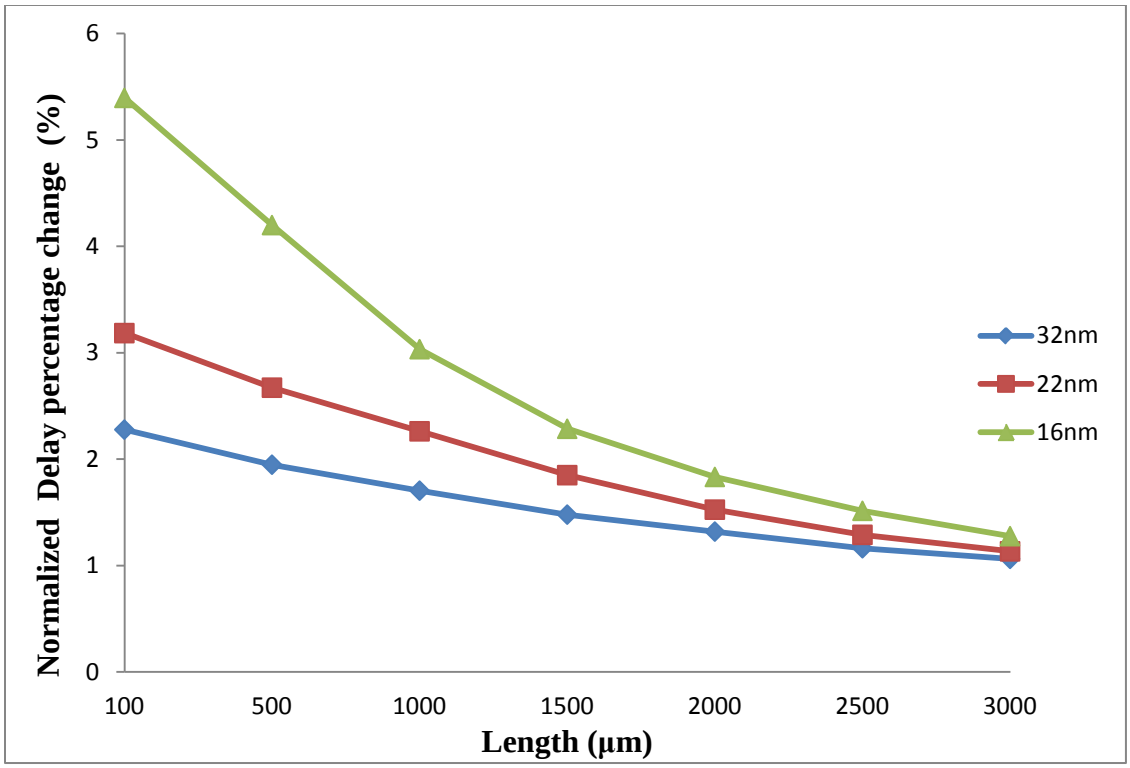

Fig. 6.9 Normalize percentage change between delay with and without considering tunneling effect with respect to length at different technology nodes.

CHAPTER 7
CONCLUSION AND FUTURE SCOPE

This report discusses the different types of CNTs along with its various growth techniques. Various parameters of MWCNT as an interconnect are also discussed and based on which a Multi-Conductor circuit (MCC) model is derived. A mathematical model is realized to convert MCC model into Equivalent single conductor (ESC) model for the better analysis of MWCNT as an interconnect. The ESC model parameters are obtained using ITRS 2013.

The SPICE simulations are performed on proposed ESC model for 32nm, 22nm and 16nm technology nodes. The obtained results show that as length increases, propagation delay also increases. This increase in propagation delay can be significantly reduced by inserting optimum number of repeaters. Use of optimum driver size also helps in reduction of propagation delay. It is observed from simulation results that imperfect contact resistance is purely a fabrication induced effect and has a linear relation with propagation delay. The increase in propagation delay due to increasing capacitive load is also observed. On varying D_{min} *to* D_{max} ratio from 0.4-0.6, it is observed that as the ratio increases, number of shells in MWCNT decreases and therefore its resistance and propagation delay increases.

Further, the effect of tunneling conductance is also studied in order to observe its impact on equivalent resistance and propagation delay. A model is proposed for deriving equivalent resistance by including the effect of tunneling conductance and modified ESC model is proposed. It is observed from the simulation results that as length increases effect tunneling on resistance and propagation delay also increases, however the overall percentage change brought by these parameters decrease with length. On the basis of the analysis and results presented in the report, it is concluded that tunneling is a serious issue as it has a comparable affect on the performance of the MWCNT in terms of propagation delay for local interconnect lengths. With the scaling in technology node, the effect of tunneling conductance on equivalent resistance and propagation delay further increase and no longer be ignored.

On the basis of simulation results carried out to compare the different aspects of propagation delay proved MWCNT as one of the prominent contender for replacing copper as a VLSI interconnect for global length at deep submicron technology nodes.

The effect of mutual inductance on propagation delay is ignored in the report and is required to be studied in the future. Several studies have been done to observe the effect of temperature on the performance of MWCNT as an interconnect. However these studies have ignored the effect of temperature on intershell interaction and therefore it is required to be studied in the future. More effective CNT growth techniques are also needed to be developed and studied in order to further reduce the impact of imperfect contact resistance on the performance of MWCNT.

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