Design of Multi-Output Second Generation Current Controlled Conveyor

Dissertation submitted towards the partial fulfillment of the requirement for the award of the degree of

Master of Technology

in

VLSI Design

Submitted by:

Ankit Kumar

Roll No: 601361005

Under the guidance of:

Dr. Rishikesh Pandey

Assistant Professor, ECED

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

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DECLARATION

I, Ankit Kumar, hereby certify that the work which is being presented in the thesis titled **"Design of Multi-Output Second Generation Current Controlled Conveyor"** by me in partial fulfillment of the requirements for the award of the degree of Master of Technology in VLSI Design Thapar University, Patiala is an authentic record of my own work carried under the supervision of **Dr. Rishikesh Pandey**, Assistant Professor, ECED, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any University/Institute for the award of Master of Technology.

Date: 11/07/2015

Ankit Kumar
Roll No. 601361005

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Date: 14/07/2015

Dr. Rishikesh Pandey
Assistant Professor, ECED
Thapar University, Patiala

Prof. Sanjay Sharma
Head of Department
ECED, Thapar University, Patiala

Date:

Dr. S.S. Bhatia
Dean of Academic Affairs
Thapar University, Patiala

Date:

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Ankit Kumar

601361005

ABSTRACT

In the dissertation, an improved translinear based Multi-Output Second Generation Current Controlled Conveyor (MOCCCII) with programmable gain is proposed. The MOCCCII circuit is developed using current mirror with programmable gain and cross coupled current mirrors. The inherent advantages of the proposed circuit are low supply voltage requirements of ±0.85V, small input parasitic resistance of 65.80Ω for a current of 50µA, low power dissipation of 79.39µw, low DC current error of 0.068% for a current 90µA and low DC voltage error of 1.83%.

The proposed MOCCCII has been used as a basic building block to develop oscillator, voltage-mode band-pass filter, current-mode band-pass filter, differentiator and integrator. SPICE simulation results using TSMC (Level 53) 0.18µm CMOS Technology have been presented for the proposed CCCII and its applications to validate the performance of the proposed circuits. The performance parameters of the proposed MOCCCII has also been compared with the existing MOCCCII circuits available in literature and the comparison shows that the proposed MOCCCII has low input resistance, low power dissipation and low DC current error.

CONTENTS

ABBREVATIONS

CCI	First Generation Current Conveyor
CCI+	First Generation Positive Current Conveyor
CCI-	First Generation Negative Current Conveyor
CCII	Second Generation Current Conveyor
CCII+	Second Generation Positive Current Conveyor
CCII-	Second Generation Negative Current Conveyor
CCC	Current Controlled Conveyor
CCCII	Second Generation Current Controlled Conveyor
DVCCCII	Differential Voltage Current Control Conveyor
LP	Low-Power
LV	Low-Voltage
MFCCCII	Multi-Function Second Generation Current Controlled Conveyor
MOCCCII	Multi-Output Current Controlled Conveyor
Op-amp	Operational Amplifier

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With reduction in the supply voltage and device threshold voltage of CMOS technology, the performance of CMOS voltage-mode circuits has very influenced by which result in an expanded propagation delay and decreased low noise margins and a decreased dynamic range. The effect of supply voltage diminishment on the performance of current-mode circuits, however, is less as compared of voltage-mode circuits. This is because the design significance of current-mode circuits is on branch current as opposed to nodal voltage. Current-Mode circuits have some recognized advantages such as they do not oblige a high voltage gain and high precision passive components and also current-mode circuits show high performance in terms of speed, data transmission and precision. Current mirrors, translinear loops, source coupled differential pair amplifiers *etc.* are the essential building blocks of the current-mode systems. Current conveyor is a vital current-mode building block, which have simple structure, wide data transfer and capability to operate at low voltage.

1.2 MOTIVATION

In voltage-mode circuits, Signals are broadly disseminated as voltages. The parasitic capacitances are charged and discharged with the full voltage swing, which restrains the speed and increases the power utilization of voltage-mode circuits. Current-Mode circuits can’t stay away from nodes with high voltage swing either however these are usually local nodes with less parasitic capacitances. Therefore, it is conceivable to reach higher speed and lower dynamic power utilization with current-mode circuit methods.

Recently, low-power utilization and low-voltage, wide data transfer capacity, operations are required at the same time. the current-mode circuits have characteristics that are required. One simple procedure for finding the option in circuit realizations is to utilize current signals rather than voltage signals for signal processing. MOS current

mirrors are more precise and less delicate to process variation than bipolar current-mirrors because with the latter the base currents limit the exactness. In this way, at the very least, MOS-transistor circuits should be rearranged by utillizing current signals in preference to voltage signals. Therefore, integrated current-mode system realizations are closer to the transistor level than the conventional voltage-mode realizations and therefore less difficult circuits and systems should result.

1.3 KEY CONTRIBUTION

The work in the dissertation is summarized as follows:

1. Design and simulate a Second Generation Current Controlled Conveyor (CCCII), which lead to decrease of the input resistance at port X.
2. CCCII has been used to implement Multi-Output Current Controlled Conveyor (MOCCCII) by adding additional current mirror with adjustable gain and cross-coupled current mirror.
3. Design and simulate oscillator, voltage-mode band pass filter, current-mode band-pass filter, differentiator and integrator by using MOCCCII.

In the dissertation, a Second Generation Current Controlled Conveyor (CCCII) with reduced input parasitic resistance at port X has been proposed and also CCCII has been used to implement Multi-Output Current Controlled Conveyor (MOCCCII) by adding additional current mirror with adjustable gain and cross-coupled current mirror. The MOCCCII is used in many applications such as oscillator, impedance simulator, differentiator, integrator, voltage-mode band-pass filter and current-mode band-pass filter. The MOCCCII proposed in the dissertation has been simulated using TSMC 0.18µm CMOS technology process parameters and the simulation results are presented. The performance parameters of the circuit has also been compared with the existing CCCIIs available in literature and the comparison shows that the proposed CCCII has low input parasitic resistance at port X and large bandwidth.

1.4 ORGANIZATION OF THE THESIS

The organization of the thesis is as follows:

CHAPTER 1: This chapter discusses the motivation, key contributions and organization

of the thesis.

CHAPTER 2: The description of current conveyor block diagram in detail along with its various specifications is discussed in this chapter.

CHAPTER 3: In this chapter available literature on translinear loop based Second Generation Current Conveyor (CCII) and differential pair based CCII are discussed. The Second Generation Current Controlled Conveyor (CCCII) is also discussed in this chapter.

CHAPATER 4: In this chapter, a CCCII with reduced input parasitic resistance at port X has been proposed and also CCCII has been used to implement Multi-Output Current Controlled Conveyor (MOCCCII) by adding additional current mirror with adjustable gain and cross-coupled current mirror. This chapter addresses some of the applications of MOCCCII such as oscillator, differentiator, integrator, voltage-mode band-pass filter and current-mode band-pass filter.

CHAPATER 5: The simulation results of proposed Multi-Output Current Controlled Conveyor (MOCCCII) have been discussed in this chapter and also simulation results of MOCCCII's applications such as oscillator, differentiator, integrator, voltage-mode band-pass filter and current-mode band-pass filter are also presented

CHAPATER 6: This chapter summarizes the dissertation and suggests future scope of the work.

CHAPTER 2

CURRENT CONVEYORS

2.1 INTRODUCTION

The current conveyor is the basic building block of current-mode system. This chapter gives the basic idea of current conveyors and also explains different topology of current conveyors. The chapter is organized as follows. Section 2.2 addresses basics of current-mode and voltage-mode circuits. The operation and applications of various generations of current conveyors are discussed in section 2.3.

2.2 CURRENT-MODE AND VOLTAGE-MODE CIRCUITS

Current-Mode circuits are usually the outcomes of the function controlled by the current signals instead of voltage signals. Current mirrors, translinear loops, CFOA, differential pair amplifiers are the key building block of the current-mode system.

Operational Amplifier is mostly used voltage-mode device. The characteristics of voltage-mode device are high input resistance and low output resistance and also constant voltage gain. Its natural characteristics enable cascading without degradation in performance, and the characteristics are determined solely by the external components. A current-mode device is entirely different and the characteristics of current-mode device are low input resistance, high output resistance and a constant current gain. For perfect current-mode circuits, the current gain is situated to unity because amplification in current will prompt to high level of power utilization, Due to this constant current gain up to extensive frequency range, current-mode circuits are applicable to be utilized for high frequency application whereas at high frequencies, the gain falls in case of voltage-mode circuits. The current conveyor is the perfect current-mode device.

Current-Mode circuits have some advantages such as no need high gain, high performance amplifiers and also no need to high precision components. Current-Mode

system can be realized fully by the transistors. Current-Mode systems have better bandwidth, speed and accuracy as compare to their voltage-mode counterparts.

2.3 CURRENT CONVEYORS

The current conveyor is a basic building block of analog circuit that can be used in analog circuit design like op-amp approach and it also represent an effective alternative of the same op-amp for designers. The current conveyors have been introduced by Sedra and Smith in 1968 as First Generation Current Conveyor (CCI) [1]. In 1970, CCII was proposed by Sedra and Smith [2] for various applications [3], which is a three terminal device (X, Y, Z), where X terminal is low impedance terminal and Y, Z terminals are high impedance terminal. There are three versions of generations of the idealized device First Generation current conveyor (CCI), Second Generation Current Conveyor (CCII) and Third Generation Current Conveyor (CCIII). When configured with other circuit elements, real current conveyors can perform numerous analogue signal preparing functions, in a comparable way to the way op-amps and the perfect concept of the op-amp are used.

Sedra and Smith at first presented the current conveyor in 1968; it was not clear what the advantage of the idea would be. As of late, current-mode circuits have risen as a vital class of circuits with properties of exactness, high frequency range [4] and adaptability in an extensive variety of uses. Current conveyor represents the rising class of high performance analog circuit design based on current-mode approach. It has basic building design, more extensive data transfer capacity and ability to work at low voltage.

Current conveyors can be utilized in variety of applications [5] such as multifunction, band pass filter, universal filters, oscillators, integrators and differentiators. Unlike operational amplifier [6], current conveyors do not have a low frequency dominant pole and their utilizable frequency extent is much higher.

The current conveyors can be classified into three generations:

1. First Generation Current Conveyor, CCI.
2. Second Generation Current Conveyor, CCII.
3. Third Generation Current Conveyor, CCIII.

All the three generations have different characteristics but their structures are the same and also current conveyor consists of three ports X, Y and Z. The current conveyor assures two functionalities between its terminals, a current follower between X and Z terminals and a voltage follower between Y and X terminals. To achieve ideal transfers, a current conveyor should be characterized by high impedance at terminals Y and Z and low impedance at terminal X. Port X is functions as input port for current signals and output port for voltage signals at the same time, port Y is a voltage input port and port Z is a current output port. Over a wide range of frequency, the current and voltage following action should be performed as accurate as possible. In mirroring of current from port X to port Y, current mirrors have played an important role so current mirrors design should be accurate in order to ensure proper mirroring with minimum offset.

2.3.1 FIRST GENERATION CURRENT CONVEYOR (CCI)

The CCI was presented by the Sedra and Smith in 1968, which was the first current-mode device. The CCI [2] is a three terminal device with the terminals assigned X, Y and Z. The potential at port X equals whatever voltage is connected to port Y. Whatever current flows into port Y also flows into port X, and is reflected at port Z with high output impedance, as a variable consistent current source. In sub-type Positive First Generation Current Conveyor (CCI+), current into X produces current into port Z; in a Negative First Generation Current Conveyor (CCI-), current into port X results in an equivalent current flowing out of port Z. The circuit diagram and symbol of CCI have been shown in Figure 2.1.

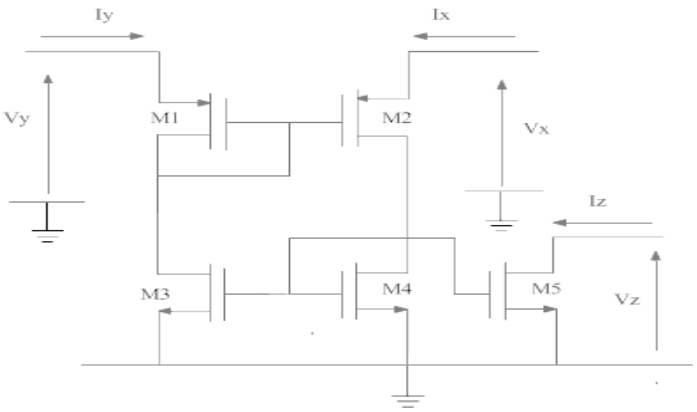


Figure 2.1 Class A CCI [7].

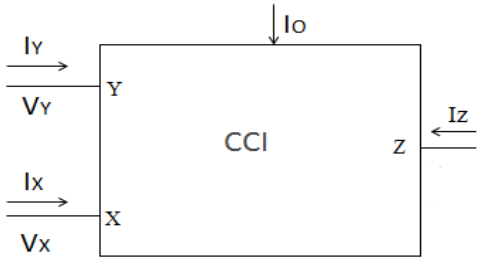


Figure 2.2 Block Diagram of CCI.

The input and output relation of CCI could be described by the following matrix equation

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{2.1}$$

where the plus and minus signs in the third row of the R.H.S matrix specify the polarity of the current conveyor i.e. CCI+, CCI-. In CCI, if parasitic elements are introduced, the characteristic equation is modified as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} V_Y & 1 & 0 \\ \beta & Z_X & 0 \\ 0 & \pm\alpha & V_Z \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{2.2}$$

where α and β denotes voltage and current gain, respectively and impedance Z_X on terminal X is the parasitic resistor R_X.

From the above equation 2.1, it is found that if a potential is applied on port Y then equal voltage will appear at port X and this voltage is independent of the current supplied to port X. Thus the circuit presents a virtual short circuit at port X. The current flow through port Y is equal to the current supplied to port X and this current is independent of voltage at port Y. Thus circuit presents a virtual open at port Y. Finally, the current supplied to Port X is also conveyed to the output port Z which is at a high impedance level. The CCI's impedances levels at different port are listed in Table 2.1.

The ports X and Y have zero input impedance in order to sink currents so the application of CCI± becomess difficults. The requirement of controlling current is fulfill by the port Y which is a difficult task in practically designs rather than controlling

voltage. It is the limitation of CCI device which leads to reduction in flexibility and versatility.

Table 2.1 Impedance level at different ports of CCI.

CCI Ports	Impedance Level
Port X	Low (ideally zero)
Port Y	Low (ideally zero)
Port Z	High (ideally infinite)

The CCI based on class AB topology has been shown in Figure 2.3, which extend the current handling capability of CCI.

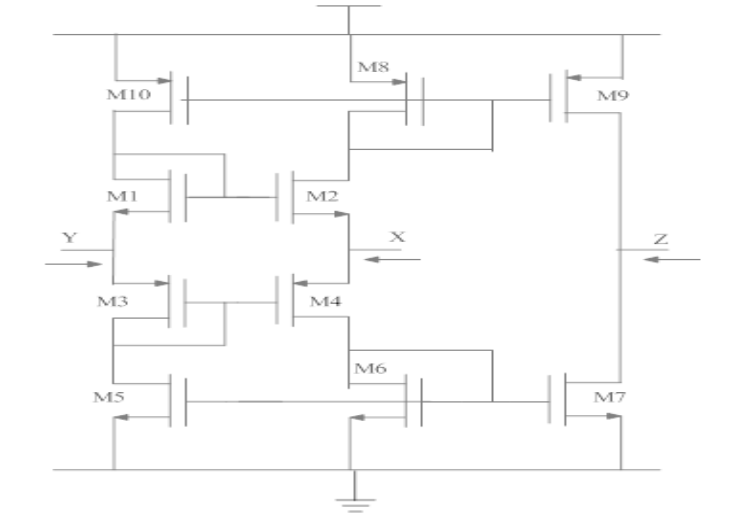


Figure 2.3 Class AB Topology Based CCI [7].

In Class AB configuration, if the current mirror are ideal then the current mirror gain is exactly one and the output current at port Z must be equal to the input current applied at port X but in non-ideal, the mirror gain is not exactly one and this adds some significant variation to the output current.

2.3.1.1 APPLICATIONS OF FIRST GENERATION CURRENT CONVEYOR

There are so many applications of First Generation Current Conveyor (CCI) such as:

- The CCI can be used as a current amplifier due to low impedance at the input terminal.

- A differential negative impedance converter can be formed, using the CCI.
- The CCI block is used in design of the sinusoidal oscillators, universal filters and all pass filters.
- The CCI can also be used as voltage to current and current to voltage convertor.

2.3.2 SECOND GENERATION CURRENT CONVEYOR (CCII)

The CCII was introduced in 1970, It's is one of the most versatile CM building block. In order to avoid loading effect, for many applications, a high impedance input port is preferred. This requirement was fulfill by CCII. CCII has one low and one high impedance input port as compare to CCI, which have two low impedance input ports. The basic block diagram of second generation current conveyor has been shown in Figure 2.4.

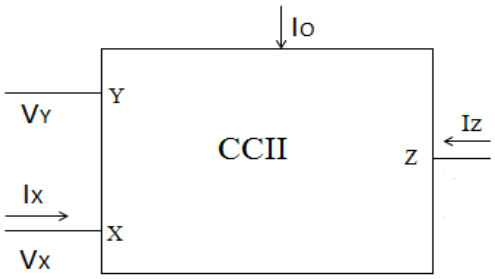


Figure 2.4 Block Diagram of CCII.

In actual practice due to some non-linearity, there is some deviation from the ideal characteristic. A real and non-ideal CCII where α and β are the voltage transfer function and current transfer function, respectively, which are non-perfect voltage and current transfer functions. The value of voltage and current transfer function is very close to unity. The CCII's impedances levels at different port are listed in Table 2.2.

Table 2.2 Impedance level at different ports of CCII.

CCII Ports	Impedance Level
Port X	Low (ideally zero)
Port Y	High (ideally infinite)
Port Z	High (ideally infinite)

2.3.2.1 DESIGN APPROACH OF SECOND GENERATION CURRENT CONVEYOR

In a more adaptable later design, no current flows through terminal Y. The perfect CCII [2] can be seen as a perfect transistor, with consummated characteristics. No current streams into the gate which is represented by Y. There is no gate-source voltage drop, so the source voltage (X) follows the voltage Y.

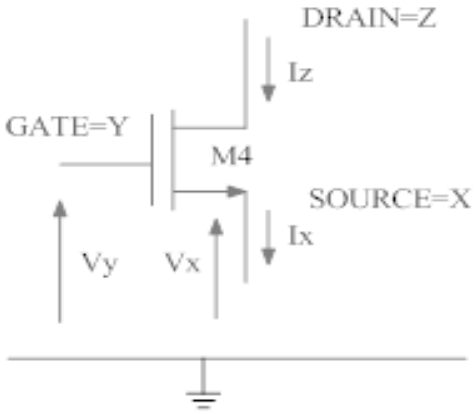


Figure 2.5 NMOS Transistor and its Equivalent with CCII.

Current out of the source (X) reflects at the drain (Z) as current in, but with infinite output impedance. If current flowing out of X resulted in the same high -impedance current is flowing out of at port Z, it would be a Positive Second Generation Current Conveyor (CCII+). The small signal analysis of circuit in Figure 2.5 is given as follows. The voltage and current transferred have been expressed as,

$$\alpha = \frac{V_X}{V_Y} = \frac{g_m r_o R_{L:oad}}{1+g_m r_o R_{Load}} \tag{2.1}$$

$$\beta = \frac{I_X}{I_Z} = 1 \tag{2.2}$$

Current at node X (I_X) and current at node Z (I_Z) are equal, as cleared from the above equation (2.2). For small signals, a single MOS transistor can be seen as a CCII, but the relative difference between bias voltage at X and Y comes out to be one threshold voltage. A traditional current mirror can eliminate this difference. The CCII characteristic in the NMOS traditional current mirror has been shown in Figure 2.6.

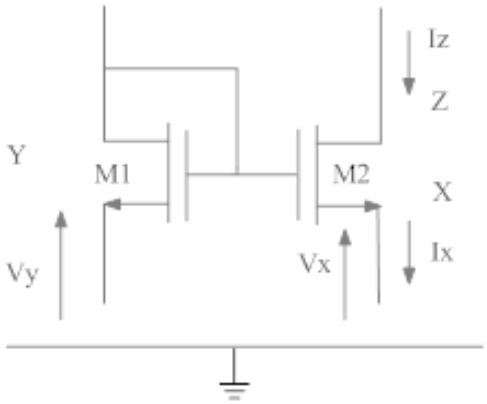


Figure 2.6 CCII Characteristics in the NMOS Traditional Current Mirror [8].

In Figure 2.6, current mirror is a CCII-. For a CCII+, it is possible to add a current mirror as shown in Figure 2.7, where current I_X and I_Z flow in same direction. To obtain a class AB CC, the CCII illustrated in Figure 2.6 can be doubled.

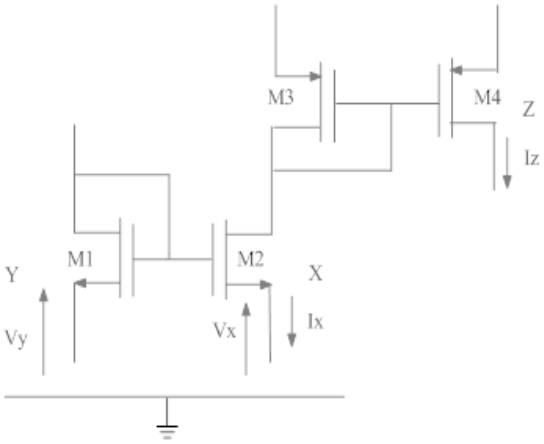


Figure 2.7 Current Mirror Used for Positive CCII Implementation [8].

The CCII works as a CCII+; i.e., ($I_Z = I_X$) or a CCII-; i.e., ($I_Z = -I_X$) current follower between terminals X and Z and a voltage follower between terminals Y and X i.e., ($V_X = V_Y$). The CCII has received significant attention because of wider dynamic range, more prominent linearity, wide transfer speed, basic hardware and low power utilization [8-9]. The input and output relation of CCII could be described by the following matrix equation,

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.3)$$

where the plus and minus signs in the third row of the R.H.S matrix specify the type of current controlled conveyor i.e. CCII+, CCII-. In CCII, if parasitic elements are introduced, the characteristic equation is modified as

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} V_Y & 0 & 0 \\ \beta & Z_X & 0 \\ 0 & \pm\alpha & V_Z \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (2.4)$$

where α and β denotes voltage and current gain, respectively and impedance Z_X on terminal X is the parasitic resistor R_X. The translinear loop based CCII has been shown in Figure 2.8.

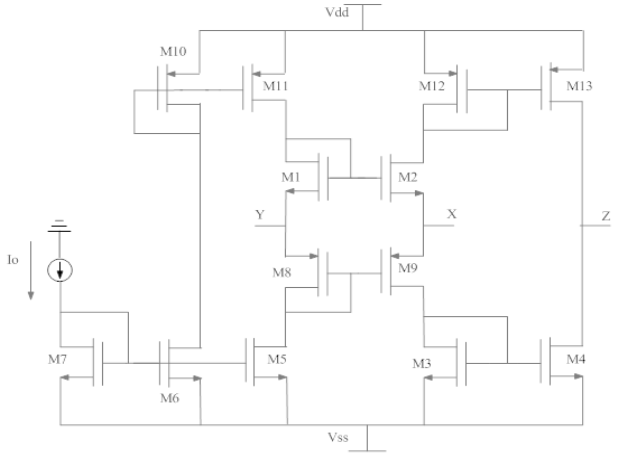


Figure 2.8 Translinear Loop Based CCII.

2.3.2.2 APPLICATIONS OF SECOND GENERATION CURRENT CONVEYOR

There are so many applications of CCII such as:

- All pass filter
- Multi-function generator,
- Band-pass filter,
- Oscillator,
- Differentiator
- Integrator.

2.3.3 THIRD GENERATION CURRENT CONVEYOR (CCIII)

The CCIII is a current controlled current source device with unity gain and it was proposed in 1995 [10]. The following current can be taken out through floating branch of a circuit using this current conveyor [10-12]. To enable cascadability, good dynamic swing and high output resistance is needed and is provided by high performance current mirror in CMOS structure of CCIII. The main features of the CCIII are:

1. Low gain errors (high accuracy)
2. Wide frequency response
3. High linearity

The CCIII is three port devices. The input and output relation of CCIII could be described by the following matrix equation,

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \tag{2.5}$$

The CCIII has been show in Figure 2.9. The circuit acts as an inverting class AB current follower shown in figure 2.9. By using the translinear principle, the current I_Y entering at port Y is equal to the current I_X entering at port X.

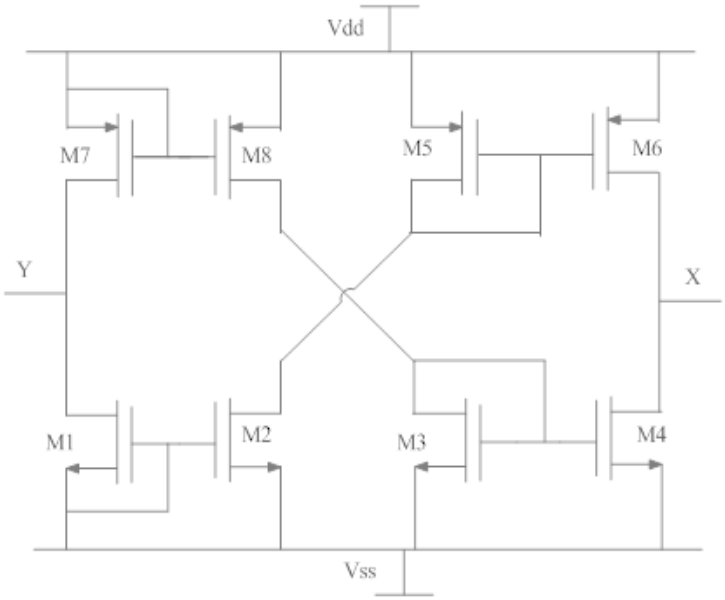
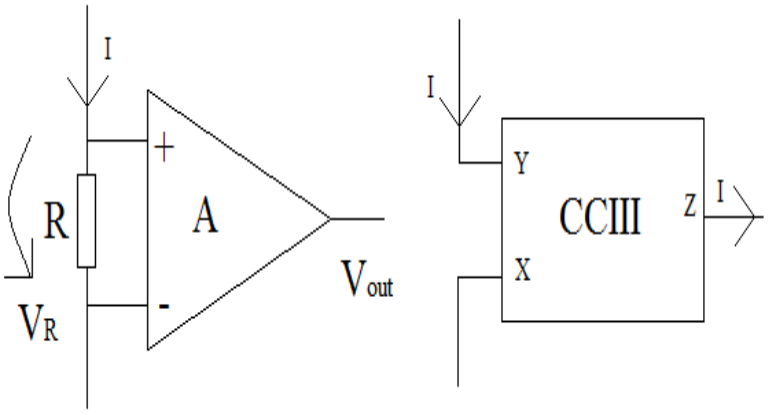


Figure 2.9 Inverting Class AB Current Follower [10].

2.3.3.1 APPLICATION OF THIRD GENERATION CURRENT CONVEYOR

There are so many application of CCIII such as filters, multifunction etc. Current measurement is the application of CCIII [13]. The current measurement with the shunt resistor and an OPAMP can be risky if the resistor should be low. In Figure 2.10 shows current measurement circuit with a voltage amplifier and with a CCIII.



(a) **(b)**

Figure 2.10 Current Measurements (a) with a Voltage Amplifier and (b) with a CCII.

2.4 SECOND GENERATION CURRENT CONTROLLED CONVEYOR (CCCII)

The basic circuit of Second Generation Current Controlled Conveyor (CCCII) is shown in Figure 2.11 [14-18]. The CCCII assures two functionalities between its terminals X, Y and Z. To achieve ideal transfers, a CCCII should be characterized by high impedance at terminals Y and Z and low impedance at terminal X. The architecture is considered to be symmetrical and it can operate for ± signal swing. By applying ±VBIAS, biasing of the CCCII is done and a proper design ensures symmetrical operation. Using MOSFET operating in sub-threshold region, translinear principle can be applied; therefore, the architecture is suitable for Low-Power/Low-Voltage (LP/LV) applications. Translinear circuits are highly reliable for application with non-tolerance of device mismatch such as biological operations, since translinear principle is based on current mode, therefore, this structure can provide benefits from CM.

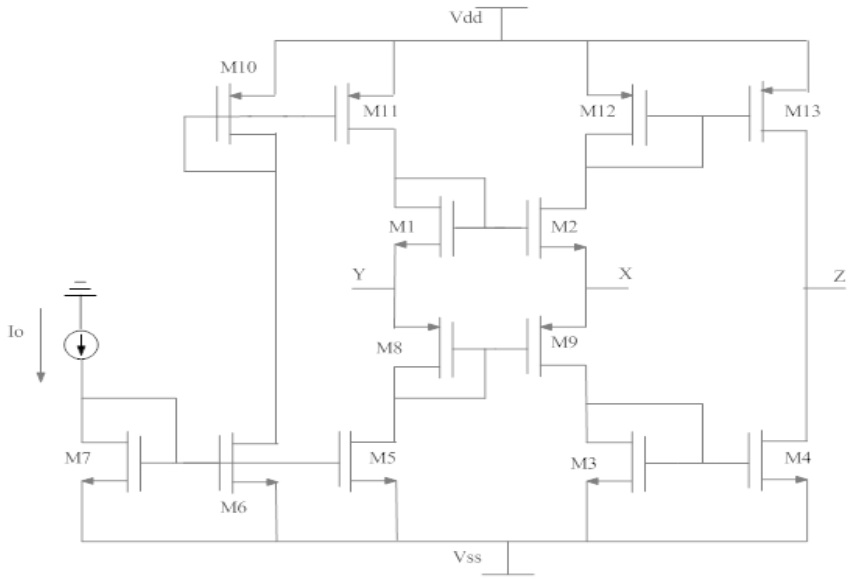


Figure 2.11 Basic Circuit of CCCII [8].

Temperature, circuit and process parameter dependent aberrations are balanced by this architecture and therefore, it is performance is free of several errors.

CHAPTER 3

LITERATURE REVIEW

3.1 INTRODUCTION

The current-mode circuits are used in high frequency circuits design applications such as active filters, function generator and oscillator, whereas for signal processing applications, the most widely used block is the Second Generation Current Controlled Conveyor (CCCII). The CCCII circuits based on the Translinear loop have excellent wide range of current and voltage transfer characteristics and also have excellent high frequency response with unity gain and wide bandwidth. Translinear loop based CCCII have excellent wideband current and voltage behavior as compare to the differential pair based CCCII circuits. This chapter is organized as follows: Section 3.2 explained different topologies of CCII. In section 3.3, comparison between Translinear loop based CCCII and Differential pair based CCCII have been discussed.

3.2 DIFFERENT TOPOLOGIES OF SECOND GENERATION CURRENT CONVEYORS

Researchers have classified basic current conveyors into two different topologies. This section is organized as follows: In section 3.2.1, Translinear loops based Second Generation Current Conveyor (CCII) is discussed and also compares variants parameter of translinear loop based CCCII's available in literature. Section 3.2.2 explained differential pair based second generation current conveyors and also compares variants parameter of differential pair based CCCII's available in literature.

3.2.1 TRANSLINEAR LOOP BASED SECOND GENERATION CURRENT CONVEYOR

CMOS current conveyor suggested by Samir Ben Salem *et al*. [19] is shown in Figure 3.1. The circuit between point Y and allows the function of voltage follower and between point X and Z allows the function of current follower. The transistors M1-M4 and M7-M8

are used to form translinear loop and current mirror, respectively. At node X, the two currents namely bias current (I_0) and input current (I_X) are injecting at node X and is entering into transistor M4 with current $I_0 + I_X$. The transistorsM9-M13are used for proper biasing. At nodeZ, I_0 is out-going current and $I_0 + I_X$ is incoming current. On applying KCL at node Z, the current I_Z is equal to I_X.

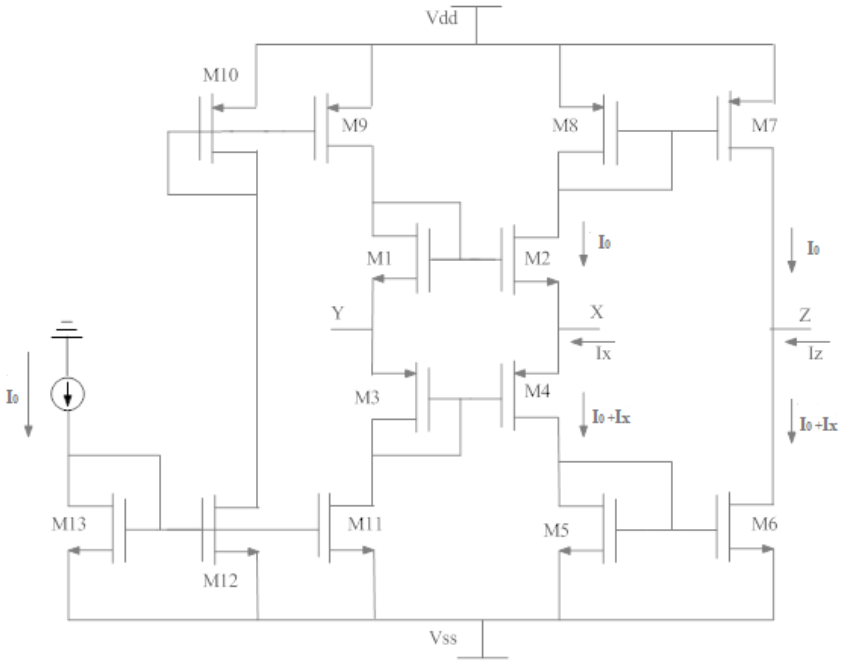


Figure 3.1 Translinear loop based CCII.

Salem *et al*. [20] have suggested CCII based on translinear loop configuration. Heuristic algorithm is used for optimal sizing regarding static and dynamic performances. In order to reduce its input parasitic resistance, an improved CCII configuration is considered.

A modified CCCII has been suggested by Hassen *et al*. [21. These circuits are operated at low supply voltage and allow the design of many electronic functions as well as the voltage mode instead of the current mode.

The value of input parasitic resistance of conventional CCCII is approximately $\approx 1k\Omega$ but this value may reduce the performance of oscillator and filters. Samir *et al*. [20] have presented a new improved CCII structure with low parasitic resistance at port X for RF design's implementation such as oscillator and filters.

3.2.2 DIFFERENTIAL PAIR BASED SECOND GENERATION CURRENT CONVEYOR

G. Ferri *et al*. [7] has presented differential pair based current conveyor, which is shown in figure 3.2.The circuit between ports Y and X allows the function of voltage follower and between ports X and Z allows the function of current follower.

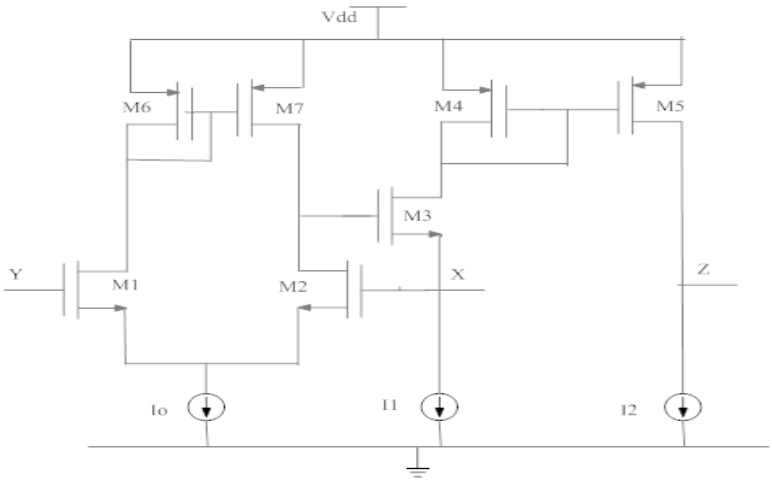


Figure 3.2 Differential Pair Based CCII.

In the circuit, transistors M1-M2 form a differential pair. The current mirror formed by transistors M6-M7 is used to sense the current flowing from X node and copies it to the high impedance Z node.

Hassanein *et al*. [22] have proposed a new high accuracy Class A CMOS CCII. The circuit exhibits voltage transfer gain of almost unity, voltage offset in the order of microvolt as well as very low input resistance in the order of milliohms, the highest voltage tracking accuracy and offset cancellation which is independent on the input current.

CMOS Class AB CCII has been proposed by Martin *et al*. [23].Class AB operation has been achieved without extra supply voltage requirements or power consumption using quasi-floating gate techniques. The CCII has very low input resistance at input terminal and low power consumption. Due to its power efficiency, it can find widespread use in low power applications like wireless transceivers and biomedical sensor interfaces.

Psychalinos *et al*. [24] have proposed CCCII topology, which offers the advantage of low voltage operation capability. The realization of input resistance in the CCCIIs is

achieved by a translinear loop constructed from two pairs of NMOS and PMOS, which is a disadvantage due to the fact that, in a typical Si or SiGe process, PMOS transistors offer reduced performance compared with that achieved by NMOS transistors. Due to the absence of P-MOS transistors for handling ac signal, performance of CCCII in terms of maximum frequency of operation is improved. Improved performances have been achieved without any loss of the performance in terms of current conveying accuracy.

A CMOS low-voltage and low-power CCII+ is suggested in [25]**,** which uses two n-channel differential pairs; i.e. (n-channel and p-channel), to realize the input stage. Therefore, the number of current mirrors needed in the input stage is less as compared to the complementary differential pair. These structures aimed at improving the voltage and the current transfer accuracy, increasing the output current capabilities, while reducing the offset using several compensation techniques and capable of operating under a minimum supply voltage at the input stage and at the output stage.

Farshidi et al. [26] have proposed CCCII which has the advantages of electronic adjustability over the CCII. In CCCII the input resistance can be varied by the current bias which is useful for application such as filters, to change its cut- off frequency or quality factor. CCCII works with low supply potentials while showing low power consumption and high dynamic range.

A CMOS Differential Voltage Current Control Conveyor (DVCCCII) cell has been suggested in [27], which is constructed from the CCCII to overcome the CCCII limitation. The circuit has the capability for working in a low-voltage power supply and also offers resistor less filter realizations. The main attractive offered benefit is that the handling of AC signals is exclusively performed by NMOS transistors. DVCCCII provides more design flexibility than CCCII. The maximum frequency of operation has been increased in comparison with the DVCCCII realized through the utilization of a conventional subtraction stage.

LP/LV Multi-Function Second Generation Current Controlled Conveyor (MFCCCII) has been presented by Ercan *et al*. [28]. Simulated Inductance and current mode band pass filter have been used to demonstrate as the application of the MFCCCII, which is able to achieve CCCII with both negative intrinsic resistance and positive resistance with small connection variation in the circuit. Tunable behavior of MFCCCII circuit is rather

convenient for low voltage IC realizations, which result in decreasing of threshold voltage. The MFCCCII could be operated even at lower supplies if the threshold voltage would be reduced.

3.3 COMPARISION BETWEEN TRANSLINEAR LOOP BASED CCCIIs AND DIFFERENTIAL PAIR BASED CCCIIs

Comparison has been made between translinear loop and differential pair based CCCII based CCCII whose main concluded factors are as follows:

- Translinear loop based CCCII provides a wide bandwidth as compared to differential pair based CCCII but it is not suitable for low voltage application.
- Translinear loop based CCCII is also not suitable for low power application too, because of its impedance levels and a very low X node impedance can be obtained only with biasing current that affect the overall power consumption in a dramatic way.
- In differential pair based CCCII noise cancellation is more when compared to translinear loop based CCCII and power consumption is very less in differential pair based CCCII when compared to translinear loop CCCII.
- In differential pair based CCCII dynamic range is unstable. Therefore, to overcome these problem Rail to Rail current conveyor is used.

3.4 FEATURE OF SECOND GENERATION CURRENT CONTROLLED CONVEYORS

The salient features of Second Generation Current Controlled Conveyor (CCCII) are as follows:

- **CURRENT MIRROR:** Since current mirror is a basic constituent of CCCII, Therefore, complexity of CCCII is lesser than OPAMP's complexity.
- **INTERCHANGEABLE OPERATION MODE:** To fulfill the need that the system reaming comparatively simpler, use of CCCII can be adopted in both voltage-mode and current-mode application.

- **LOW GAIN:** Since high gain is not required in CCCII, therefore, high performance amplifiers can be omitted and hence can be considered as a device with simple design and use.
- **SIMPLICITY OF DESIGN:** High precision components are not required to design CCCII. CCCII usually prefers comparative biasing signal levels.
- **APPLICATION SIMPLICITY:** CCCII is much simpler when viewed from application point. It is capable of realizing a negative resistance with uttermost simplicity when compared to OPAMP. The current conveyors provide a board spectrum of applications such as filters, oscillators, switched current circuits, converters, amplifiers, negative impedance realization etc.
- **SLEW RATE:** Current-Mode circuits also show higher slew rates. This is because usually the output transistor of a current mirror remains in the saturation region, due to which charging and discharging is dependent on current strength and hence current-mode circuits possess higher slew rates.
- **PROPAGATION DELAY:** A parameter that determines the execution of response is referred as propagation delay and is consider as performance index in digital circuits. In current-mode circuits, swing of voltage of a node with capacitance is given as

  $$C_n(\Delta V_n) = I_{avg}\Delta t = \Delta \int_0^t i(t)dt \qquad (3.1)$$

  On comparison node voltage should be very large than noise voltage of the node. Hence, to reduce delay either C_n or swing decreases or I_{avg} increases.
- **BANDWIDTH:** Due to no global feedback, current conveyor possesses high bandwidth. Since feedback is usually of local nature, hence, this leads to the increase in bandwidth.
- **INOUT AND OUTPUT IMPEDANCE:** $R_0 = \infty, R_x = 0\ and\ R_0 = \infty$are the characteristics of an ideal CCCII which helps to reduce the loading effects when the device is driving or being driven by other stages.

CHAPTER 4

DESIGN OF SECOND GENERATION CURRENT CONTROLLEDCONVEYOR CIRCUITS

4.1 INRODUCTION

In this chapter, design of proposed second generation current controlled conveyor (CCCII) with low input parasitic resistance (R_X) and programmable gain is presented. The chapter is organized as follows. Section 4.2 presents the proposed second generation current controlled conveyor (CCCII). The operation of current mirror with adjustable gain has been discussed in section 4.3. Section 4.4 proposes Multi-Output Second Generation Current Controlled Conveyor (MOCCCII). In section 4.5, applications of proposed multi-output second generation current controlled conveyor are presented.

4.2 PROPOSED SECOND GENERATION CURRENT CONTROLLED CONVEYOR CIRCUIT

In conventional circuit shown in Figure 2.18 (Chapter 2), value of input parasitic resistance at port X (R_x) is approximately $\approx 1k\Omega$ [29, 30] but this value may reduce the performance of high frequency application such as oscillators and filters, which are designed using basic Second Generation Current Controlled Conveyor (CCCII) and the current transfer gain is also found to be uncontrollable for basic CCCII [31-33]. To overcome these problems, a new Second Generation Current Controlled Conveyor (CCCII) with low input parasitic resistance and programmable gain shown in Figure 4.1 is proposed.

The proposed circuit guarantees two functionalities between its terminals X, Y and Z, a current follower and a voltage follower. To achieve ideal transfers, a CCCII should be characterized by high impedance at terminals Y and Z and low impedance at terminal X.

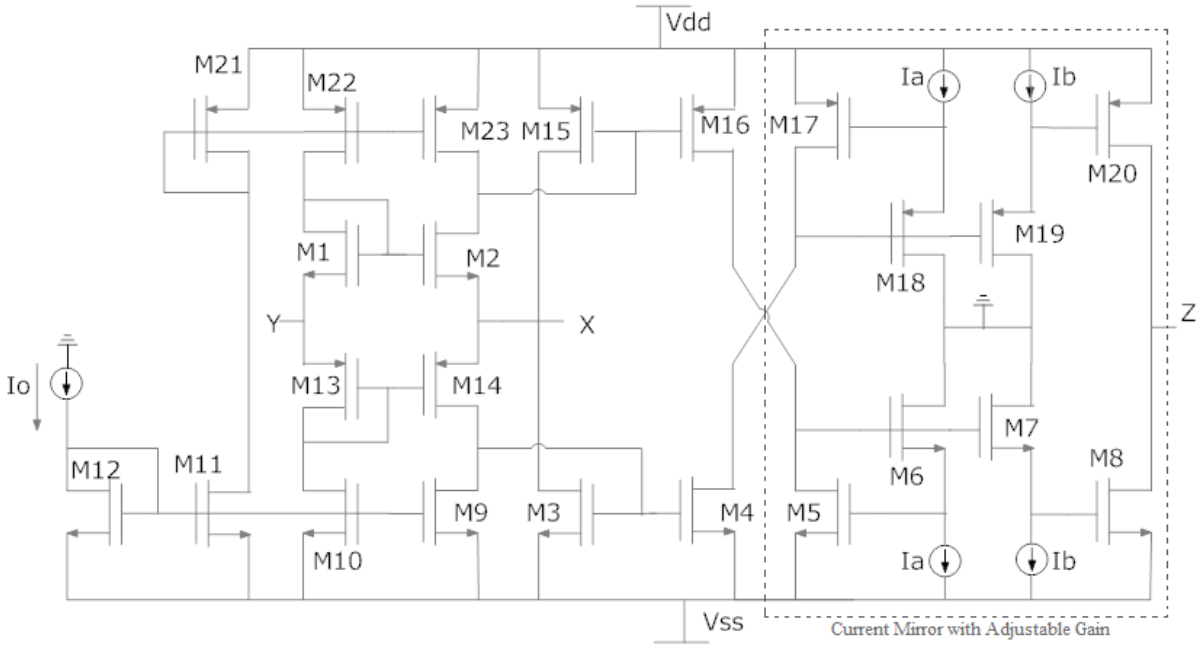


Figure 4.1 Proposed CCCII with Programmable Gain.

The CCCII current conveyor path is separated from the signal conveying path by making a new signal path for the current transfer between port X and Z, maintaining low impedance on port X. The parasitic impedance R_x lying in between ports X and Z and the parasitic resistance R_Y lying on terminal Y are given as:

$$R_X \cong \frac{1}{g_{M15}(1+g_{M2}r_{02})} \| \frac{1}{g_{M5}(1+g_{M14}r_{14})} \tag{4.1}$$

$$R_Y \cong \left(\frac{1}{g_{M1}} + r_{21}\right) \| \left(\frac{1}{g_{M13}} + r_{10}\right) \tag{4.2}$$

From the above equation, it can be observed that the value of parasitic resistances affected by bias current I_O.

By using small signal analysis the expression of current transfer function I_{OUT}/I_{In} is expressed as

$$\frac{I_{OUT}}{I_{IN}} = \left[\frac{g_{M8}\left[\frac{(g_{M2}+sC_5)(g_{M6}+sC_{11})}{sC_5\left(g_{M5}g_{M6}+sC_{10}(g_{M6}+sC_{11})\right)}\right] - g_{M20}g_{M4}\left[\frac{(g_{M14}+sC_6)(g_{M18}+sC_2)}{sC_6\left(g_{M17}g_{M18}+sC_9(g_{M18}+sC_{11})\right)}\right]}{s(C_5+2C_6+C_7+C_8)+2g_{M14}+g_{M12}-\frac{g_{M2}+sC_5}{sC_5}}\right] \tag{4.3}$$

where $C_2, C_5, C_6, C_7, C_8, C_9$ and C_{11} are expressed as

$$C_2 = C_{gs21} + C_{gs22} + C_{gs23} \quad (4.4)$$

$$C_5 = C_{gs1} + C_{gs2} \quad (4.5)$$

$$C_6 = C_{gs13} + C_{gs14} \quad (4.6)$$

$$C_7 = C_{gs3} + C_{gs4} \quad (4.7)$$

$$C_8 = C_{gs15} + C_{gs16} \quad (4.8)$$

$$C_9 = C_{gs17} \quad (4.9)$$

$$C_{11} = C_{gs6} \quad (4.10)$$

where $g_M \; and \; C_{gs}$ are the transconductance and gate to source capacitance of MOSFET, respectively.

4.3 CURRENT MIRRORS WITH ADJUSTABLE GAIN

The negative and positive types current mirrors with adjustable gain are shown in Figures 4.2 and 4.3, respectively. The transistors M1 & M2 and M3 & M4 are perfectly matched i.e. $(V_{t1} = V_{t2}, V_{t3} = V_{t4}, K_1 = K_2, \; K_3 = K_4)$, where V_{t1}, V_{t2}, V_{t3} and V_{t4} are the threshold voltages of transistors M1, M2, M3 and M4, respectively, and K_1, K_2, K_3 and K_4 are the trascunductance parameter of transistors M1, M2, M3 and M4, respectively.

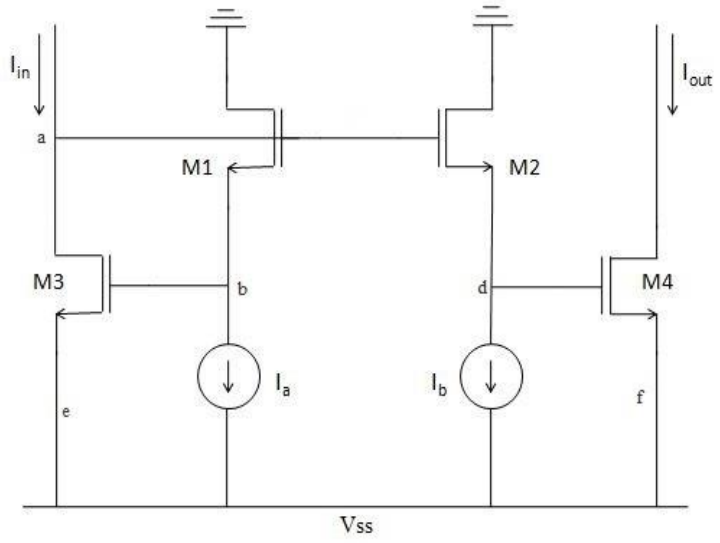


Figure 4.2 Negative Type Current Mirror with Adjustable Gain.

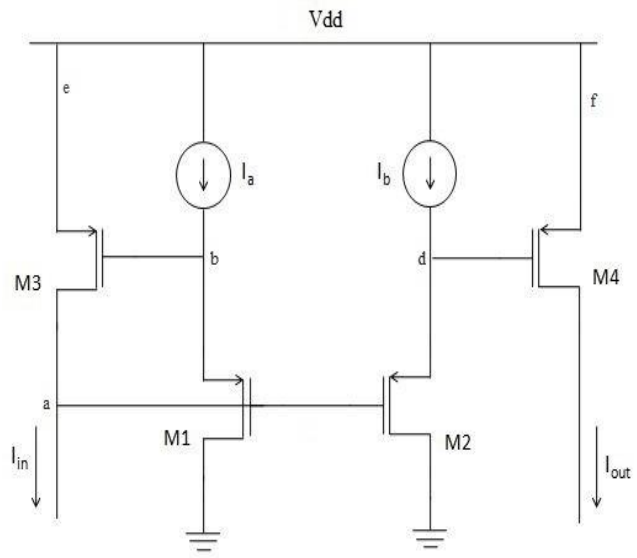


Figure 4.3 Positive Type Current Mirror with Adjustable Gain.

In Figure 4.2, the current gain 'k' of the translinear based CCCII can be expressed as:

$$k = \frac{I_a}{I_b} \tag{4.11}$$

The value of k is chosen as $k = 1$, then equation (4.2) is modified as

$$I_a = I_b \tag{4.12}$$

In Figure 4.3, the voltage across current sources I_a and I_b are $V1$ and $V2$, respectively. Applying KVL in loop abda

$$V_{gs1} + V1 - V2 - V_{gs2} = 0 \tag{4.13}$$

By choosing $V1 = V2$, the equation (4.13) reduced to,

$$V_{gs1} = V_{gs2} \tag{4.14}$$

From equation (4.14), since, $V_{gs1}$is equal to V_{gs2}, the voltage at node A (V_B)should be equal to the voltage at node B (V_B). Therefore, V_{gs3} is equal to V_{gs4}. Input current I_{in} and output current I_{out} of current mirror are expressed as

$$I_{in} = K_3(V_{gs3} - V_{t3})^2 \tag{4.15}$$

$$I_{out} = K_4(V_{gs4} - V_{t4})^2 \tag{4.16}$$

Using equations (4.14), (4.15) and (4.16), it is observed that I_{in} is equal to $I_{out.}$

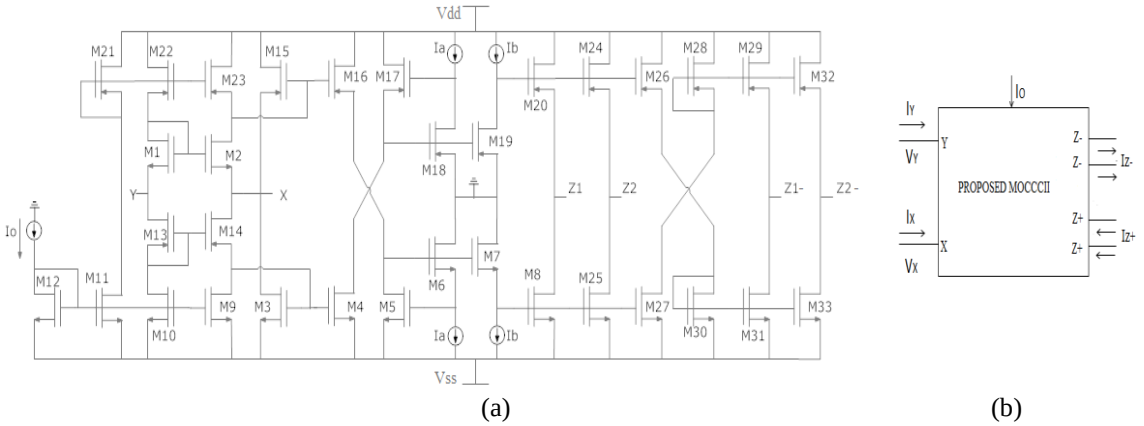
By using small signal analysis the expression of I_{out}/I_{in} is expressed as,

$$\frac{I_{out}}{I_{in}} = \frac{g_{M2}g_{M4}\,(g_{M1}k+\frac{1}{r_{01}})}{kg_{M1}g_{M3}\,(g_{M2}+\frac{1}{r_{02}})} \tag{4.17}$$

where $g_{M1,}\, g_{M2,}\, g_{M3}\, and\, g_{M4}$ are the transconductances of transistors M1, M2, M3 and M4, respectively and r_{01} and r_{02} are the output resistances of transistors M1 and M2, respectively. From equation (4.17), it can be observed that the programmable gain depends on the value of *k*. Therefore, the current mirror with adjustable gain can amplify the signal by the factor *k* as this factor *k* is controlled by choosing the appropriate value of $I_a\ /\ I_b$.

4.4 PROPOSED MULTI-OUTPUT SECOND GENERATION CURRENT CONTROLLED CONVEYOR CIRCUIT

Since there is a requirement of positive as well as negative current therefore, Multi-Output Second Generation Current Controlled Conveyor (MOCCCII) is developed from the basic Second Generation Current Controlled Conveyor shown in Figure 4.4(a). The circuit is developed using cross-coupled current mirrors. The symbol of proposed MOCCCII is shown in Figure 4.4(b).



(a) (b)

Figure 4.4 Proposed MOCCCII (a) Circuit of MOCCCII with Programmable Gain (b) Symbol of MOCCCII.

In Figure 4.4 (a), the transistors M9, M10, M11, M12, M21, M22 and M23 allow the mixed loop to be DC biased, transistors M1, M2, M13 and M14 form the translinear loop to provide equal voltage in both X and Y ports. Transistors M5, M6, M7, M8 & M25 and M17, M18, M19, M20 & M25 form NMOS and PMOS current mirrors, respectively. Transistors M16 & M17, M4 & M5, M27 & M30 and M26 & M28 form the cross coupled structures to convey the same current but in inverting mode to the output ports Z1- and Z2-.

4.5 APPLICATIONS OF MULTI-OUTPUT SECOND GENERATION CURRENT CONTROLLED CONVEYOR

The Multi-Output Second Generation Current Controlled Conveyor (MOCCCII) is widely used in high frequency applications [34-37]. Some of the applications such as sinusoidal oscillator, voltage-mode band-pass filter, current-mode band-pass filter and differentiator have been proposed in this section.

4.5.1 SINUSOIDAL OSCILATOR

The sinusoidal oscillator circuit based on proposed MOCCCII has been presented shown in Figure 4.5. The proposed oscillator has been developed using two MOCCCII blocks and two grounded capacitors.

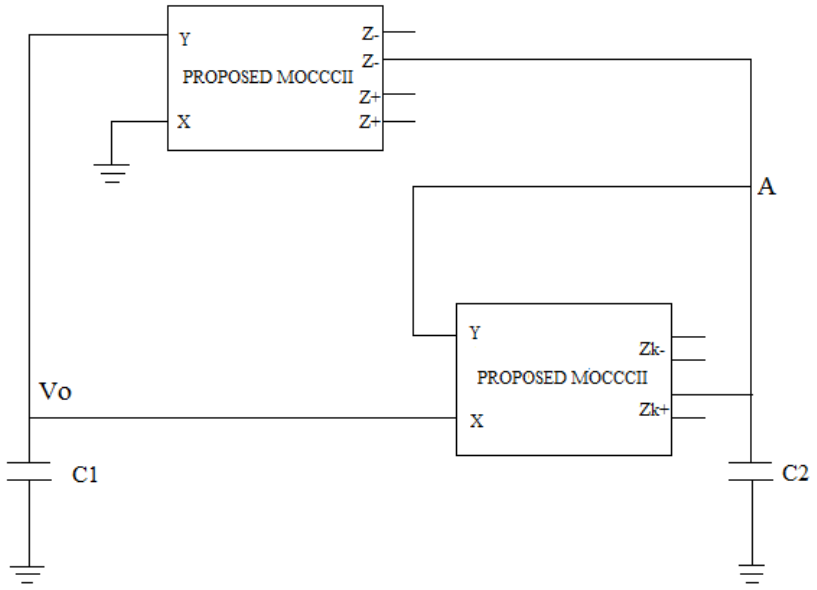


Figure 4.5 Proposed MOCCCII Based Sinusoidal Oscillator.

The characteristic equation of sinusoidal oscillator [33, 38] can be expressed as:

$$s^2 C_1 C_2 R_{X1} R_{X2} + sR_{X1}(C_2 - \alpha_2\beta_2 k_1 C_1) + \alpha_1\beta_1\beta_2 = 0 \quad (4.18)$$

The oscillation condition and the oscillation frequency of proposed sinusoidal oscillator can be written as:

$$C_2 = \alpha_2\beta_2 k_1 C_1 \quad (4.19)$$

$$w_o = \sqrt{\frac{\alpha_1\beta_1\beta_2}{C_1 C_2 R_{X1} R_{X2}}} \quad (4.20)$$

where R_{X1} and R_{X2} are the intrinsic resistance of the MOCCCII and also α and β are the voltage transfer function and current transfer function, respectively.

4.5.2 VOLTAGE-MODE BAND-PASS FILTER

The proposed voltage-mode band-pass filter shown in Figure 4.6 has been developed using MOCCCII.

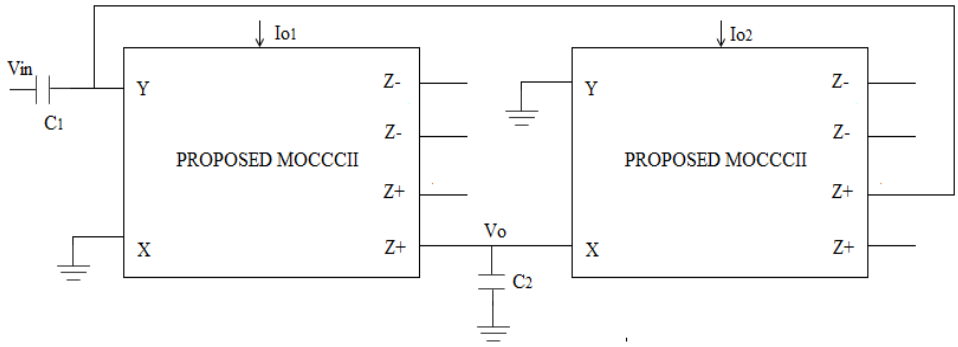


Figure 4.6 Proposed MOCCCII Based Voltage-Mode Band-Pass Filter.

From Figure 4.6 it can be seen that the voltage-mode band-pass filter is developed using two MOCCCII and two capacitors. The characteristics equation of band-pass filter [41] can be expressed as:

$$\frac{v_o}{v_{in}} = \frac{\frac{s}{C_2 R_X}}{s^2 + \frac{s}{C_2 R_X} + \frac{1}{C_1 C_2 R_X^2}} \quad (4.21)$$

From equation (4.21), its characteristic parameters central frequency and quality factor are given as:

$$w_0 = \frac{1}{R_X \sqrt{C_1 C_2}} \tag{4.22}$$

$$Q = \sqrt{\frac{C_2}{C_1}} \tag{4.23}$$

From the equations (4.22) and (4.23), it can be seen that central frequency w_o and quality factor Q are independent if the ratio of C_2 and C_1 remains constant.

The main advantage of the proposed filter is that the center frequency can be controlled with the help of bias current I_o.

4.5.3 CURRENT-MODE BAND-PASS FILTER

To transfer the voltage-mode filter to current-mode filter, a current-to-voltage converter is connected at the input stage and a voltage-to-current converter is connected at the output stage. Figures 4.7 and 4.8 show the current-to-voltage and voltage-to-current convertors, respectively.

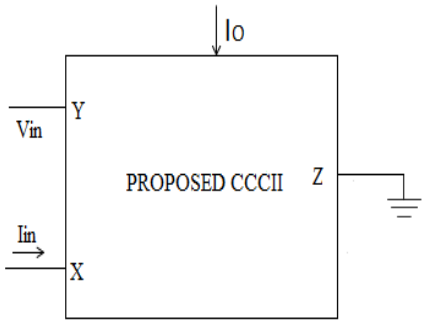


Figure 4.7 Current-to-Voltage Convertor Using Proposed CCCII.

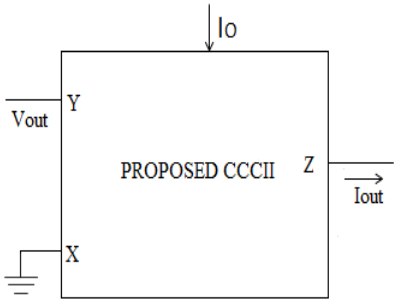


Figure 4.8 Voltage-to-Current Convertor Using Proposed CCCII.

The voltage-mode filter is converted to current mode filter to present the importance of current-mode filter. The high quality factor has been obtained in current-mode filter.

The current-mode band-pass filter based on MOCCCII is presented in Figure 4.9. The filter has been developed using four MOCCCII blocks and two capacitors.

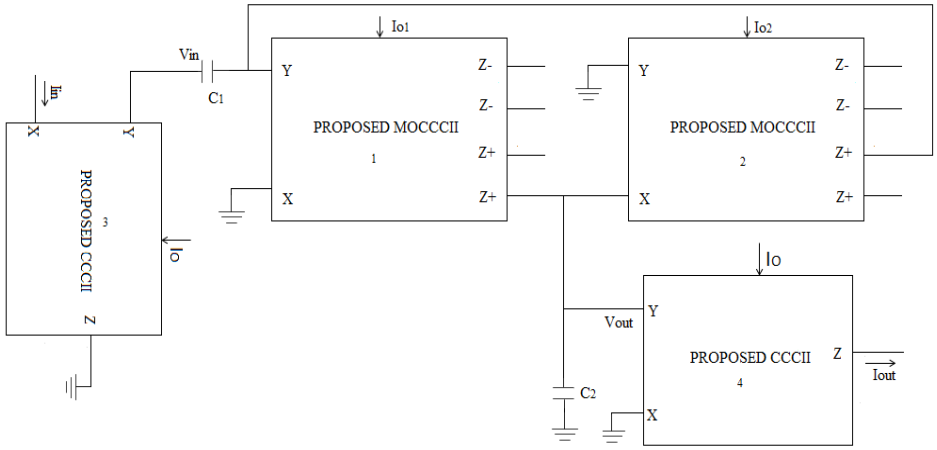


Figure 4.9 Proposed MOCCCII Based Current-Mode Band-Pass Filter.

4.5.4 DIFFERENTIATOR

The proposed current differentiator shown in Figure 4.10 is developed using MOCCCII, fixed grounded resistor and grounded capacitor.

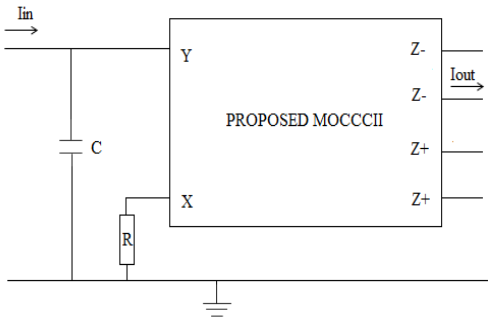


Figure 4.10 Proposed MOCCCII Based Differentiator.

The expressions of voltage at node Y and current at node X are expressed as:

$$V_Y = \frac{I_{in}}{sC} \tag{4.24}$$

$$I_X = \frac{V_X}{R} \tag{4.25}$$

From the Figure 4.11, it is observed that,

$$I_X = I_Z = I_{out} \tag{4.26}$$

Using equations (4.24), (4.25) and (4.26) the expression of output current of differentiator is given as:

$$I_{out} = \frac{I_{in}}{sCR} \tag{4.27}$$

From equation (4.27) it can be seen that the circuit behavior as a differentiator.

4.5.5 INTEGRATOR

The proposed current integrator shown in Figure 4.11 is developed using MOCCCII, fixed grounded resistor and grounded capacitor.

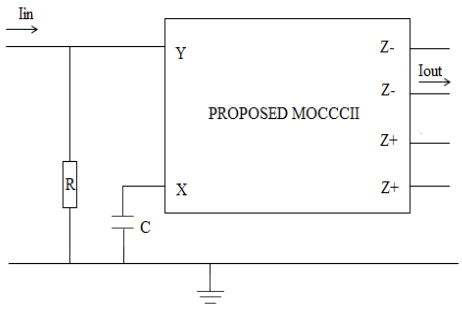


Figure 4.11 Proposed MOCCCII Based Integrator.

The expressions of voltage at node Y and current at node X are,

$$V_Y = RI_{in} \tag{4.28}$$

$$I_X = sCV_X \tag{4.29}$$

From the Figure 4.12, it is observed that,

$$I_X = I_Z = I_{out} \tag{4.30}$$

Using equations (4.28), (4.29) and (4.30) the expression of output current of differentiator is given as:

$$I_{out} = sCRI_{in} \tag{4.31}$$

From equation (4.31) it can be seen that the circuit behavior as a integrator.

CHAPTER 5

SIMULATION RESULTS

5.1 INTRODUCTION

The chapter addresses the simulation results of proposed Multi-Output Second Generation Current Controlled Conveyor (MOCCCII). The MOCCCII has been simulated using TSMC 0.18µm CMOS technology parameters. This chapter is organized as follow. In section 5.2, DC and AC analysis of proposed MOCCCII is presented. Section 5.3 presents the simulation results of sinusoidal oscillator. The simulation results of voltage-mode band-pass filter is presented in section 5.4. Section 5.5 presents the simulation results of current-mode band-pass filter and section 5.6 presents the simulation results of differentiator.

5.2 SIMULATION RESULTS OF MULTI-OUTPUT SECOND GENERATION CURRENT CONTROLLED CONVEYOR

The proposed Multi-Output Second Generation Current Controlled Conveyor (MOCCCII) has been simulated by performing DC and AC analysis in order to obtain desired parameters using TSMC 0.18µm CMOS technology. The MOCCCII operates at supply voltage of ± 0.85V and bias current of 50µA.

5.2.1 DC ANALYSIS

The DC characteristics of the proposed MOCCCII, such as plot of I_{Z+} against I_X, plot of I_{Z-} against I_X, plot of V_X against V_Y, plot of DC voltage error and plot of input resistance R_x against control current I_0 have been presented.

Figures 5.1 and 5.2 show the current transfer characteristics of the proposed MOCCCII+ and MOCCCII-, respectively, and plot the input current versus output current in the range of 0 to 100µA which indicate the linearity of the output current with respect to input current. For current transfer characteristics, a varying current source is applied at port X and corresponding output taken at port Z.

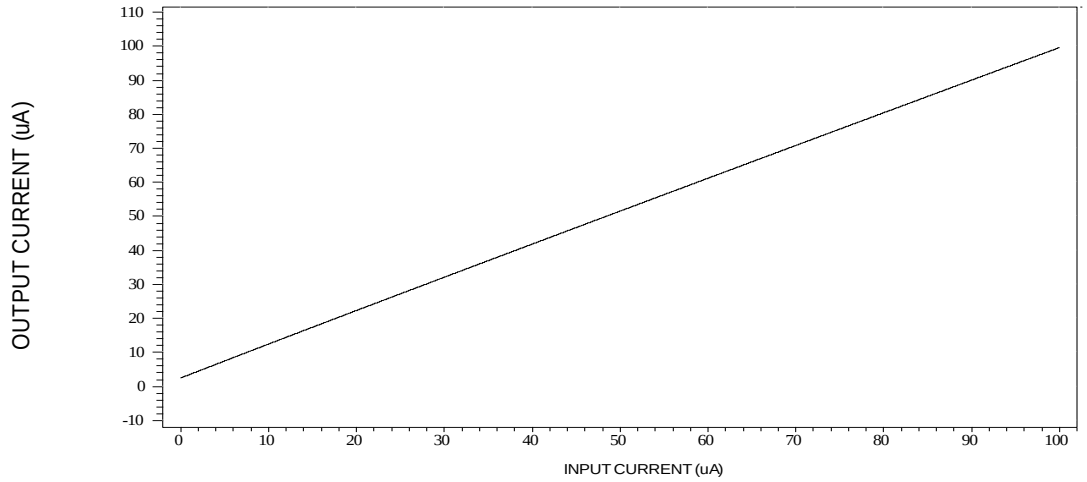


Figure 5.1 Variation of Output Current over Input Current at Port Z+.

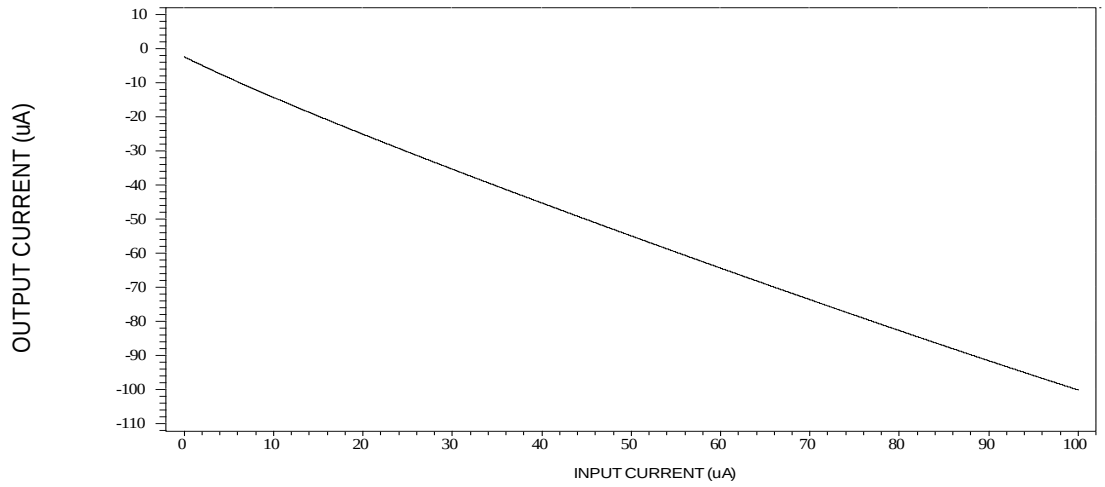


Figure 5.2 Variation Output Current over Input Current at Port Z-.

During the analysis, the port Y was grounded. From Figures 5.1 and 5.2, it can be seen that the input currents are varied along the X axis and outputs follow the input for a range of 0μA to 100μA properly and for MOCCCII+ an offset is found to be 2.46μA between input and output.

Figure 5.3 shows the voltage transfer characteristics between port Y and port X. A varying voltage source is applied at port Y and varied in the range of -1V to +1V. From the Figure 5.3 it is observed that the output is linear within the range -200 to +200mV.

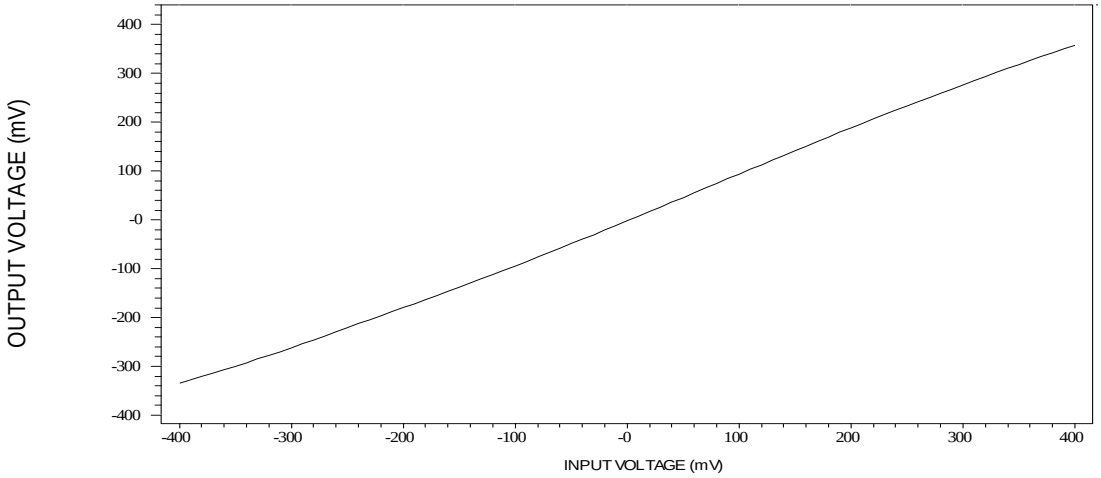


Figure 5.3 Variation Output Voltage over Input Voltage.

Figure 5.4 shows the DC voltage error and from the Figure, it can be seen that the input voltage is varied along the X axis and DC voltage error for a range of -200mv to +200mv is 1.87%.

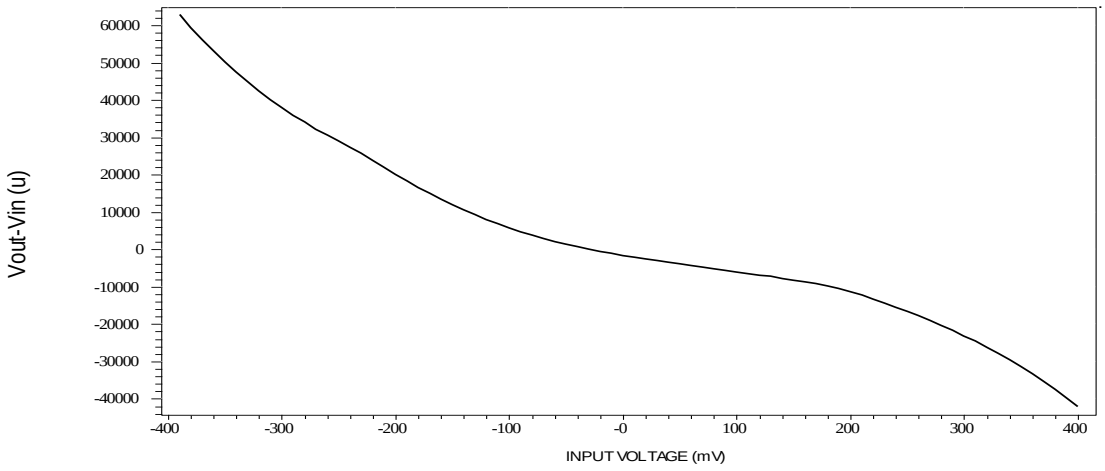


Figure 5.4 DC Voltage Error as a Function of Input Current.

The DC power dissipation of the proposed MOCCCII is obtained as 79.39µw for input current of 90µA.

The input resistance (R_X) as a function of control current I_O is shown in Figure 5.5. Resistance R_X can be controlled between 29.12Ω and 297.71Ω by varying the bias current in the range of $10\mu A\ to\ 300\mu A$ and is shown in Figure 5.5.

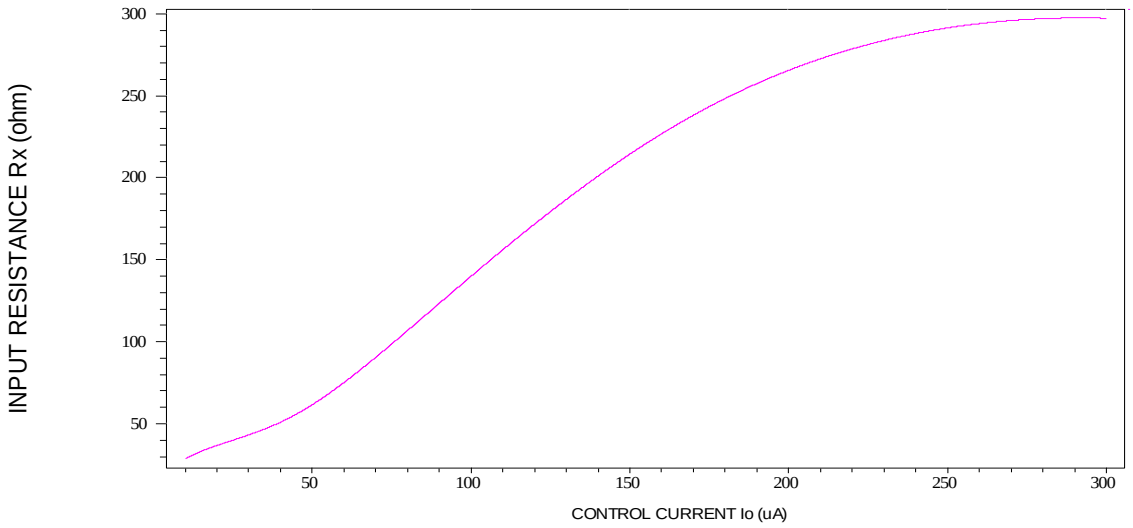


Figure 5.5 Input Parasitic Resistance Rx Versus Control Current $I_{0.}$

From Figure 5.5, it is observed that the various values of input resistance (R_X) for different bias current are listed in Table 5.1.

Table 5.1 Change in input resistance R_X as a function of bias current I_0.

BIAS CURRENT I_0 (µA)	**INPUT RESISTANCE R_X (Ω)**
25	39.90
50	62.30
75	98.91
125	180.05
175	243.46
225	281.45
275	296.55
300	297.24

5.2.2 AC ANALYSIS

Figures 5.8 and 5.9 show the frequency responses of proposed MOCCCII+ and MOCCCII- at port Z+ and port Z-, respectively, and values of current gains at both the output ports Z+ and Z- have been found to be closer to unity.

From Figure 5.6, it is observed that the bandwidth of proposed MOCCCII+ at output port Z+ is 103.70MHz. The Current gain of the MOCCCII+ is 0.9994.

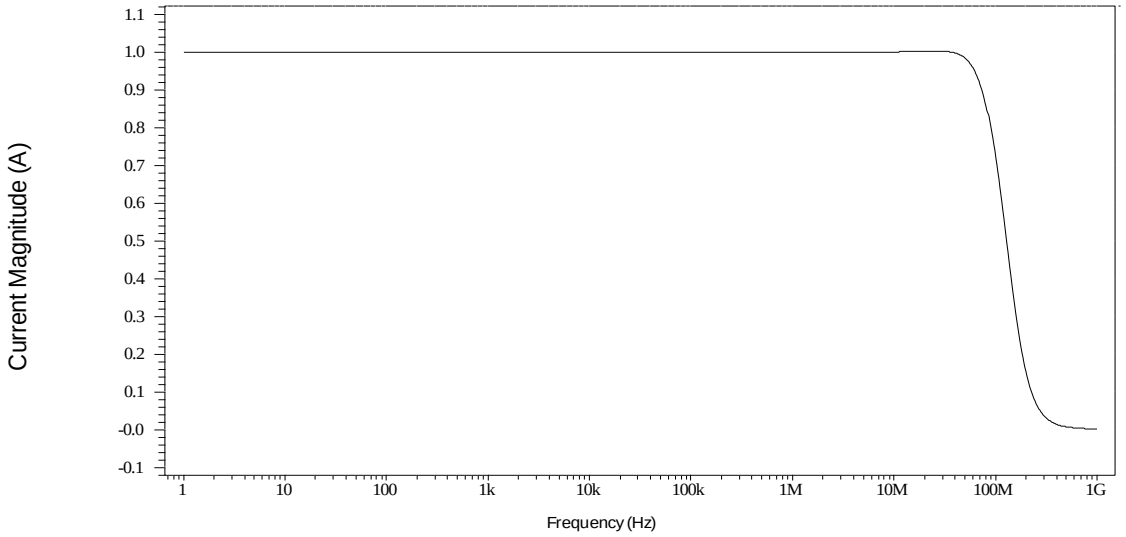


Figure 5.6 Current Gain as a Function of Frequency for CCCII+.

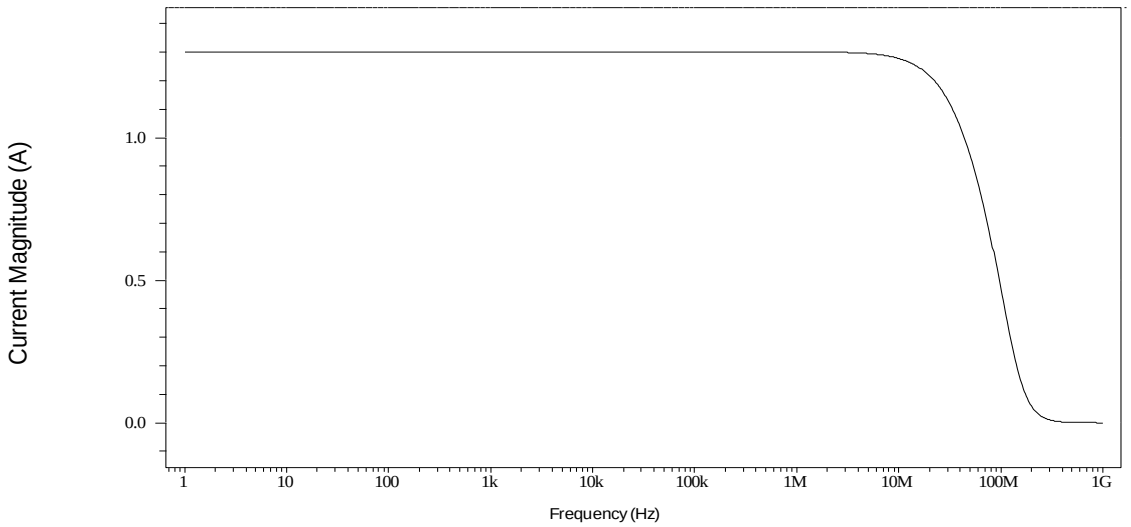


Figure 5.7 Current Gain as a Function of Frequency for CCCII-.

From Figure 5.7, it is observed that the bandwidth of proposed MOCCCII- at output port Z- is 94.70MHz. The Current gain of the MOCCCII- is 1.3.

Figure 5.8 shows the frequency response of proposed MOCCCII at port X. From Figure 5.8, it is observed that the voltage gain and -3dB bandwidth of the MOCCCII are 0.951 and 204.34MHz, respectively.

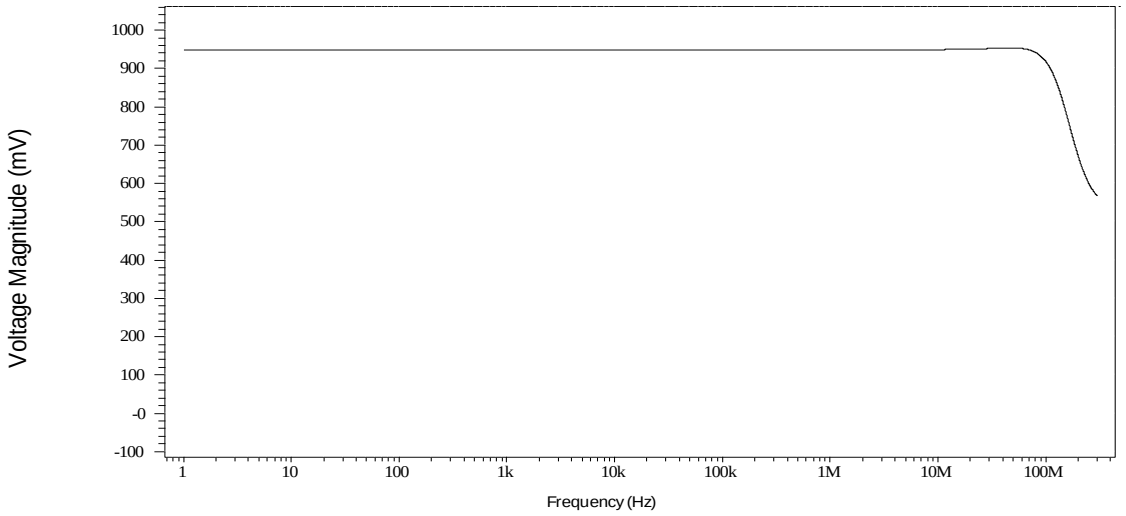


Figure 5.8 Voltage Gain as a Function of Frequency.

5.3 SIMULATION RESULTS OF SINUSOIDAL OSCILLATOR

The sinusoidal oscillator is simulated using TSMC $0.18\,\mu m$ CMOS technology parameters. The various parameter are chosen as $V_{DD} = |V_{SS}| = \pm 0.85V$, $C_1 = C_2 = 10nF$ and current I_{a1}=66µA, I_{b1}=60µA. The sinusoidal output waveform of the oscillator for $I_{o1} = I_{o2} = 50\mu A$ is shown in Figure 5.9. The oscillation frequency of the oscillator is 500kHz, which is shown in Figure 5.9.

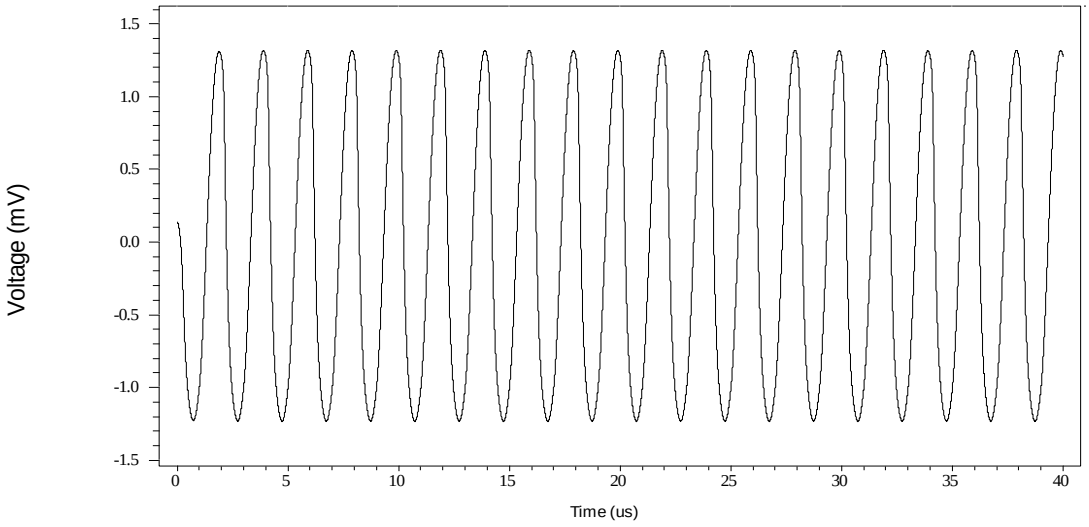


Figure 5.9 Simulated Output Waveform of Oscillator

5.4 SIMULTAION RESULTS OF VOLTAGE-MODE BAND-PASS FILTER

The voltage-mode band-pass filter is simulated using TSMC 0.18 μm CMOS technology parameters. The frequency response of the voltage-mode band-pass filter is shown in Figure 5.10. From the figure, it is observed that the resonate frequency is $f_0 = 9.02\text{MHz}$.

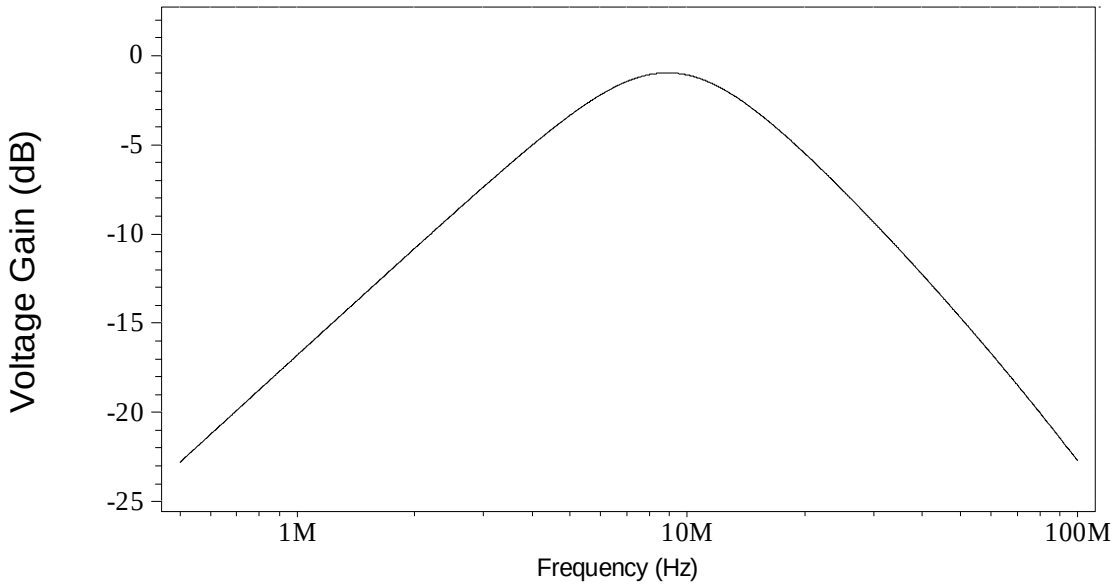


Figure 5.10 Frequency Response of Voltage-Mode Band-Pass Filter.

5.5 SIMULATION RESULTS OF CURRENT-MODE BAND-PASS FILTER

The current-mode band-pass filter is simulated using TSMC 0.18 μm CMOS technology parameters. The frequency response of the current-mode band-pass filter is shown in Figure 5.11. The various parameters are chosen as $V_{DD} = |V_{SS}| = \pm 0.85\text{V}$, $C_1 = C_2 = 200\text{pf}$. From Figure 5.11, it is observed that the high quality factor (Q) of the current-mode band-pass filter is 9.

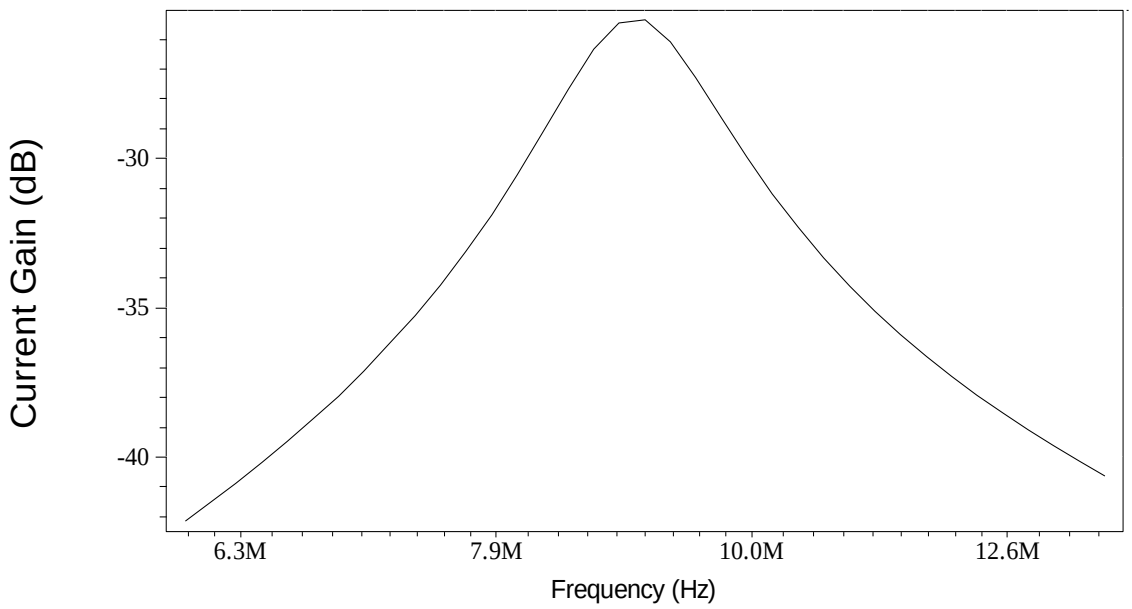


Figure 5.11 Frequency Response of the Current-Mode Band-Pass Filter.

5.6 SIMULATION RESULTS OF DIFFERENTIATOR

The differentiator is simulated using TSMC 0.18 μm CMOS technology parameters and the simulation results are shown in Figure 5.12.

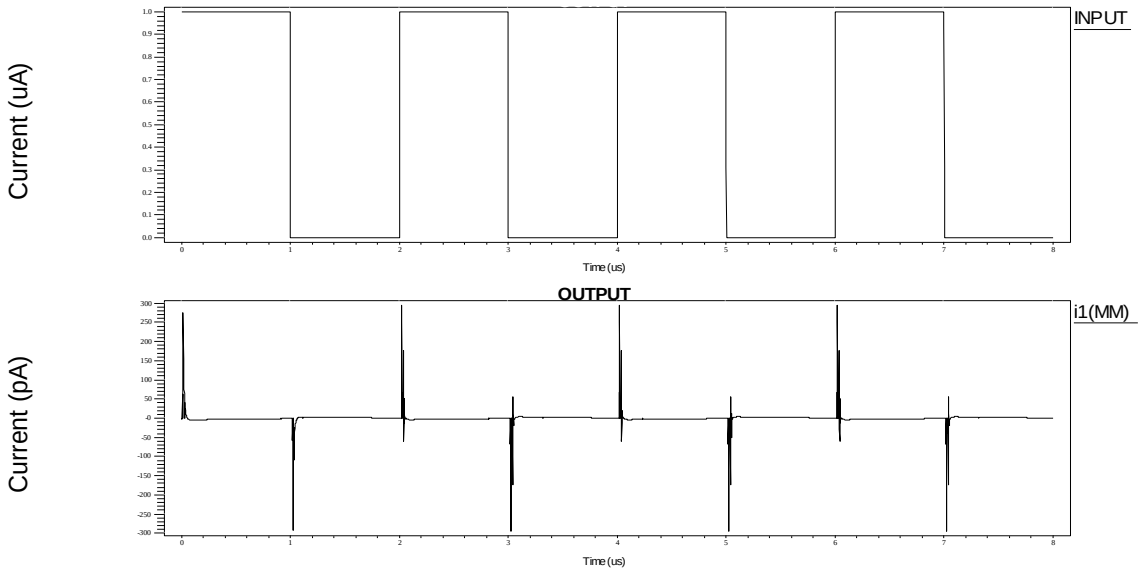


Figure 5.12 Input and Output Waveforms of Proposed Differentiator.

A pulse signal is applied to the differentiator and the impulse signal is obtained at the output which is shown in Figure 5.12.

Table 5.2 Comparison of proposed MOCCCII with CCCII available in literature [23-27].

Circuit Parameters	**Ref.[21] in 2011**	**Ref.[22] in 2014**	**Ref.[23] in 2012**	**Ref.[24] in 2007**	**Proposed MOCCCII**
Technology	0.18µm TSMC	0.18µm TSMC	0.18µm TSMC	0.35µm TSMC	0.18µm TSMC
Bias voltage	2V	±0.5V	±0.8V	5V	±0.85V
Voltage gain	0.94	0.989	0.94	0.9	0.951
Current gain	1	0.985	0.93	1.045	0.9994
Bandwidth	3.34GHz	70MHz	1.0GHz	1.4MHz	204.34MHz
Bandwidth current	4.37GHz	130MHz		1.17MHz	103.70MHz
DC error voltage(%)	1.5	-	-	-	1.83
DC error current (%)	0.8	-	-	-	0.068
Input resistance	169.32Ω	3.8kΩ	300Ω	540Ω	65.80Ω
Input impedance	5.67kΩ	-	-	-	144.9kΩ
Output impedance	6.81kΩ	4.28MΩ	-	-	35.08kΩ
DC power dissipation(µW)	-	126	3000	-	79.39
DC current offset	-	-	-	-	24.6µA
DC voltage offset	-	-	-	-	1.65mV

The comparison between proposed MOCCCII and CCCIIs available in literature is shown in Table 5.2. From the Table, it is observed that proposed MOCCCII has lower DC current error, lower DC power dissipation, lower input impedance, higher output impedance, and wider range of input current than the CCCII reported in literature.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In the work, MOCCCII has been proposed with adjustable gain and reduced input parasitic resistance. The inherent advantages of the proposed MOCCCII are low supply voltage requirement and low power dissipation. The DC current error of the proposed MOCCCII is 0.068% and DC voltage error is 1.83%. Some of the applications of proposed MOCCCII circuit such as sinusoidal oscillator, voltage-mode band-pass filter, current-mode band-pass filter, differentiator and integrator have also been addressed. The simulation results validate the effectiveness of the proposed circuits and these circuits are expected to be useful in high frequency applications such as multi-phase sinusoidal oscillators, multifunction filters and high frequency high-Q all pass filters etc.

6.2 FUTURE SCOPE

Some suggestions and ideas for future work are as follows

1. The MOCCCII and CCCII block based all pass filter and multifunction generator can be investigated.
2. By selecting low biasing currents, the static power dissipation of the CCCII can be reduced.
3. Simulations outcomes demonstrate that the current transfer bandwidth of proposed MOCCCII can be further expanded by using the bandwidth enhancement techniques.

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APPENDIX I

The TSMC 0.18µm CMOS technology model file is listed below:

```
.MODEL NMOS NMOS (LEVEL   = 53
+VERSION = 3.1          TNOM    = 27          TOX     = 4.1E-9
+XJ      = 1E-7         NCH     = 2.3549E17   VTH0    = 0.3725327
+K1      = 0.5933684    K2      = 2.050755E-3 K3      = 1E-3
+K3B     = 4.5116437    W0      = 1E-7        NLX     = 1.870758E-7
+DVT0W   = 0            DVT1W   = 0           DVT2W   = 0
+DVT0    = 1.3621338    DVT1    = 0.3845146   DVT2    = 0.0577255
+U0      = 259.5304169  UA      = -1.413292E-9 UB     = 2.229959E-18
+UC      = 4.525942E-11 VSAT    = 9.411671E4  A0      = 1.7572867
+AGS     = 0.3740333    B0      = -7.087476E-9 B1     = -1E-7
+KETA    = -4.331915E-3 A1      = 0           A2      = 1
+RDSW    = 111.886044   PRWG    = 0.5         PRWB    = -0.2
+WR      = 1            WINT    = 0           LINT    = 1.701524E-8
+XL      = 0            XW      = -1E-8       DWG     = -1.365589E-8
+DWB     = 1.045599E-8  VOFF    = -0.0927546  NFACTOR = 2.4494296
+CIT     = 0            CDSC    = 2.4E-4      CDSCD   = 0
+CDSCB   = 0            ETA0    = 3.175457E-3 ETAB    = 3.494694E-5
+DSUB    = 0.0175288    PCLM    = 0.7273497   PDIBLC1 = 0.1886574
+PDIBLC2 = 2.617136E-3  PDIBLCB = -0.1        DROUT   = 0.7779462
+PSCBE1 = 3.488238E10   PSCBE2 = 6.841553E-10 PVAG    = 0.0162206
+DELTA   = 0.01         RSH     = 6.5         MOBMOD = 1
+PRT     = 0            UTE     = -1.5        KT1     = -0.11
+KT1L    = 0            KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18    UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0            WLN     = 1           WW      = 0
+WWN     = 1            WWL     = 0           LL      = 0
+LLN     = 1            LW      = 0           LWN     = 1
+LWL     = 0            CAPMOD = 2          XPART   = 0.5
+CGDO    = 8.53E-10     CGSO    = 8.53E-10    CGBO    = 1E-12
+CJ      = 9.513993E-4  PB      = 0.8         MJ      = 0.3773625
+CJSW    = 2.600853E-10 PBSW    = 0.8157101   MJSW    = 0.1004233
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+CJSWG   = 3.3E-10       PBSWG   = 0.8157101     MJSWG   = 0.1004233
+CF      = 0             PVTH0   = -8.863347E-4  PRDSW   = -3.6877287
+PK2     = 3.730349E-4   WKETA   = 6.284186E-3   LKETA   = -0.0106193
+PU0     = 16.6114107    PUA     = 6.572846E-11  PUB     = 0
+PVSAT   = 1.112243E3    PETA0   = 1.002968E-4   PKETA   = -2.906037E-3   )
*
.MODEL PMOS PMOS ( LEVEL   = 53
+VERSION = 3.1           TNOM    = 27            TOX     = 4.1E-9
+XJ      = 1E-7          NCH     = 4.1589E17     VTH0    = -0.3948389
+K1      = 0.5763529     K2      = 0.0289236     K3      = 0
+K3B     = 13.8420955    W0      = 1E-6          NLX     = 1.337719E-7
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 0.5281977     DVT1    = 0.2185978     DVT2    = 0.1
+U0      = 109.9762536   UA      = 1.325075E-9   UB      = 1.577494E-21
+UC      = -1E-10        VSAT    = 1.910164E5    A0      = 1.7233027
+AGS     = 0.3631032     B0      = 2.336565E-7   B1      = 5.517259E-7
+KETA    = 0.0217218     A1      = 0.3935816     A2      = 0.401311
+RDSW    = 252.7123939   PRWG    = 0.5           PRWB    = 0.0158894
+WR      = 1             WINT    = 0             LINT    = 2.718137E-8
+XL      = 0             XW      = -1E-8         DWG     = -4.363993E-8
+DWB     = 8.876273E-10  VOFF    = -0.0942201    NFACTOR = 2
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.2091053     ETAB    = -0.1097233
+DSUB    = 1.2513945     PCLM    = 2.1999615     PDIBLC1 = 1.238047E-3
+PDIBLC2 = 0.0402861     PDIBLCB = -1E-3         DROUT   = 0
+PSCBE1 = 1.034924E10    PSCBE2 = 2.991339E-9    PVAG    = 15
+DELTA   = 0.01          RSH     = 7.5           MOBMOD = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD = 2              XPART   = 0.5
```

```
+CGDO    = 6.28E-10      CGSO    = 6.28E-10      CGBO    = 1E-12
+CJ      = 1.160855E-3   PB      = 0.8484374     MJ      = 0.4079216
+CJSW    = 2.306564E-10  PBSW    = 0.842712      MJSW    = 0.3673317
+CJSWG   = 4.22E-10      PBSWG   = 0.842712      MJSWG   = 0.3673317
+CF      = 0             PVTH0   = 2.619929E-3   PRDSW   = 1.0634509
+PK2     = 1.940657E-3   WKETA   = 0.0355444     LKETA   = -3.037019E-3
+PU0     = -1.0227548    PUA     = -4.36707E-11  PUB     = 1E-21
+PVSAT   = -50           PETA0   = 1E-4          PKETA   = -5.167295E-3   )
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.END
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LIST OF PUBLICATIONS

A. Kumar, R. Pandey, A Novel Multi-Output Second Generation Current Controlled Conveyor and its High Frequency Applications, International Journal of Circuit Theory and Applications, -*Communicated*, 2015. *(SCI Indexed)*