

COMPARATIVE STUDY OF CMOS INPUT & OUTPUT AMPLIFIERS

A Thesis

Submitted in partial fulfillment of the requirement for the award of the degree of

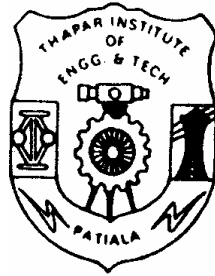
MASTER OF TECHNOLOGY

in

VLSI DESIGN & CAD

to

Thapar Institute of Engineering & Technology, Patiala



Submitted By

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CERTIFICATE

I, Anjali Arora, hereby certify that the work which is being presented in this thesis entitled “**Comparative Study of CMOS Input & Output Amplifiers**” by me in partial fulfillment of the requirements for the award of degree of Master of Technology in VLSI design & CAD from Thapar Institute of Engineering and Technology (Deemed University), Patiala, is an authentic record of my own work carried out under the supervision of Mrs. Alpana Agarwal and Mrs. Manu Bansal.

The matter presented in this thesis has not been submitted in any other University / Institute for the award of Master of Technology.

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At this occasion, I would not like to miss the opportunity to show my gratitude to **Dr D S Bawa**, Dean of Academic Affairs (TIET, Patiala) for his kind support and inspiration time to time through out my course.

I am deeply indebted to my parents for their inspiration and ever-encouraging moral support, which enabled me to pursue my studies. They inculcated in me the morale of their life "Simple living and High Thinking". I do not find enough words with which I can express my feelings of thanks to my dear friends for their help, inspiration and moral support, which went a long way in successful completion of the present study.

(Anjali Arora)

Date: June, 2005

Place: T.I.E.T., Patiala

Abstract

It is inconceivable to implement any analog circuit without the use of amplifiers in one form or another. The amplifiers are the essential part of the analog designs. Amplifiers consists of input amplifiers to primarily provide the gain and output amplifiers are used to provide sufficient power to the output load and to drive a speaker or other power device. Another important purpose of output stage is the input-output matching of devices with which it is cascaded. An output stage plays a crucial role in the circuit design. The output stage with minimum distortion, low output impedance, high bandwidth, and high efficiency is desired.

In this project, some amplifiers to be used as output amplifiers are designed to drive the RC load with $R_L=2K$ and $C_L=10$ pF.

Here, I have studied performance parameters like Total Harmonic Distortion, efficiency, Bandwidth, output voltage swing, dc gain, output resistance, temperature effects for class A current source load class A sinking amplifiers(without and with feedback), push-pull class B and AB output amplifiers (without and with feedback) and cascode amplifiers. The results for the same are tabulated in the concluding chapter, which would facilitate the design engineer to make a choice between the various modalities for a specific application.

Source degeneration technique to reduce the total harmonic distortion and error amplifier to reduce the output resistance are also presented in this project.

Differential amplifiers are also studied and two topologies i.e. resistive load differential amplifier, and current mirror load differential amplifier is designed to be used as input amplifiers.

The layouts of class A common source sinking amplifier, class B push-pull amplifier without feedback and differential amplifier is also presented.

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Chapter 1

Introduction

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integrated technologies and very large scale CMOS design. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at a very fast pace in digital as well as analog domains.

In analog domain, amplifier forms an essential component of every electronic circuits and is functionally important constituent of the signal processing circuits and systems.

We are available with many types of input and output stages, working in particular class of operation with particular architecture. The class of operation for output stage is determined by the biasing point. A particular circuit topology achieves some good parameters, while trading the other. Though some literature is available on this topic, but the detailed data for parameters achievable by a particular topology of amplifiers is not available for decision making to the choice of a specific circuit for desired use. Thereby need for comparative study of the useful parameters of different topologies to be used as output stage with different class of operation is of paramount importance.

The Class A, Class B, Class AB output stages, with and without feedback to drive $2k\Omega$, $10pf$, RC load was designed and performance parameters like the Total Harmonic distortion at different frequencies, voltage swing, Bandwidth, temperature effects, are studied and tabulated for different architectures used as output stage. The trade-offs to achieve best performance with one architecture is also discussed.

In input stages, differential amplifiers with resistive load and with current mirror load was designed.

This work has been made possible through the benign guidance in using the Tanner Tool facility (1.25 um Technology) for simulations, available at T.I.E.T, Patiala. The work has been done at the level of simulations using T-Spice and layouts are made in L-Edit.

The detailed design has been accomplished in the chapters to follow. However, brief introduction, chapter wise is presented hereby. The final results are tabulated at the end.

Precisely, this work in hand takes up the objective “It is necessary to examine closely the design process of analog circuits and to identify those principles that will increase design productivity & the designer’s chances for success”.

1.2. Organization of Thesis Work:

In Chapter 1, is given the brief introduction about the topic and chapterwise organization of the work.

In chapter 2, introduction to types of amplifiers is presented, that include input and output amplifiers and operational amplifier, which are commonly used for amplification in analog circuits. The various parameters which decide the performance of the amplifiers i.e. distortion, output voltage swing, -3dB Bandwidth, input and output resistances, efficiency, gain, noise, effect of temperature are also briefly discussed.

In chapter 3, the output amplifiers are discussed that are classified as Class A, Class B and Class AB amplifiers based on their operating point biasing. The two topologies of output amplifiers include output amplifiers without feedback and with feedback. Output amplifiers without feedback including Class A, Class AB and Class B are designed for driving a load of $R = 2K$ and $C = 10$ pF and their performances calculated in terms of Total Harmonic Distortion, DC Gain, Bandwidth, Output Resistance, Power Dissipation and Efficiency are discussed. Simulations are made in Tanner-Tool with 1.25um Technology is also presented in this chapter.

In chapter 4, the output amplifier with feedback, including class A, class AB, Class B amplifiers, are designed and the same parameters as mentioned in chapter 2 are calculated. The practical implementation of Class B output amplifier with floating batteries is discussed.

In chapter 5, differential amplifiers with different loads to be used as input amplifiers in analog circuits, is discussed. The trade-offs between these topologies are discussed. Two differential amplifiers i.e. Differential Amplifiers with resistive load and differential amplifier with current-mirror load is designed and their simulation results are also provided in this chapter.

In chapter 6, the analog layouts are made for common- source Class A, Class B and for current mirror load differential amplifier designed in previous chapters.

In chapter 7 the comparison of all the output amplifiers designed in previous chapters to drive the RC load is given in table 5. Then, which output amplifier is best suited to which application is discussed.

Appendix I – Model file

Appendix II – Net-list

References

Chapter 2

Classification of Amplifiers

Amplification is an essential function in most analog and many digital circuits. Amplification is done because the signal may be too small to drive a load, or to overcome the noise of a subsequent stage or to provide logical levels to a digital circuit. The performance parameters of the amplifiers are dc gain, supply voltage, linearity, power dissipation, noise and maximum voltage swings. The input and output impedances of the amplifier determines how the circuit interacts with preceding and subsequent stages. Most of these parameters trade with each other, making the design a multi-dimensional optimization problem.

2.1. Types of Amplifiers

The basic types of amplifiers [1] are shown as follows:

- MOS Inverting Amplifiers
- Differential Amplifiers
- Output amplifiers
- Operational Amplifiers

2.1.1. MOS Inverting Amplifiers

The inverter is widely used in both analog and digital circuits. In digital circuits, inverter accomplishes the Boolean operation of negation. In analog circuits, the inverter is used to achieve amplification. The inverting amplifier is primary gain stage of analog amplifiers. The objective of inverting amplifiers used in analog circuits is to provide an inverting, small signal voltage gain greater than 1. The inverter produces output that is inverted w.r.t input.

An inverting amplifier, in its simple form, consists of two blocks, voltage controlled current sink/ source and the load.

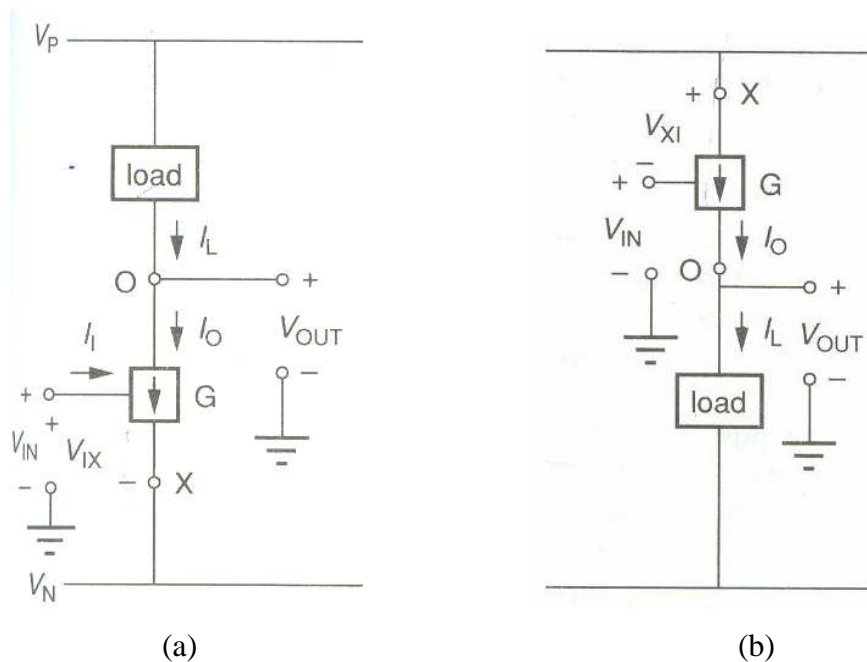
Basic Inverter Architectures

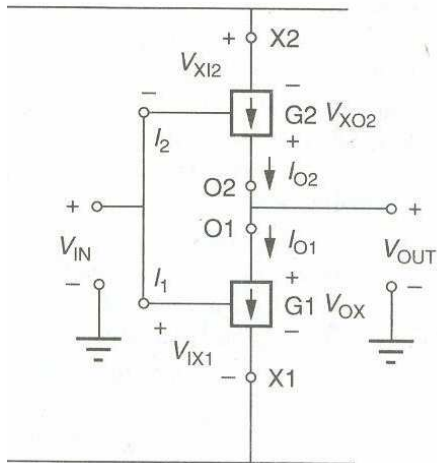
The voltage controlled current sink/ source are combined with two terminal loads to implement the three basic types of inverter architectures:

- Sinking Inverter
- Sourcing Inverter
- Push-Pull Inverter

In sinking inverter as shown in Fig. 2.1.(a), there is a voltage controlled current source and the load. The inverter is called sinking inverter because the transistor sinks the current through load whereas the sourcing inverter is called so because it sources the current in the load, as shown in Fig. 2.1.(b)

In push-pull inverters, as shown in Fig. 2.1.(b), there is a voltage controlled current source and a voltage controlled current sink. The use of dc current sources or sinks to realize the load will lead to high values of small signal voltage gain A_v .

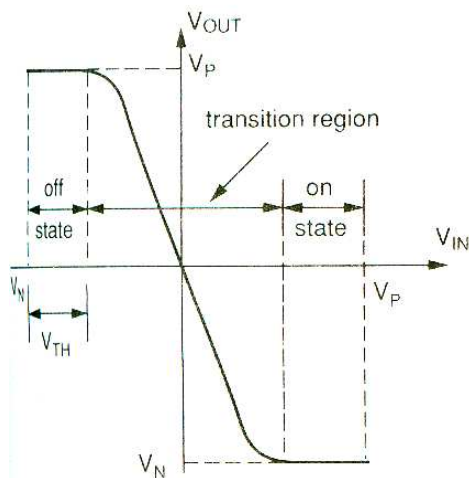




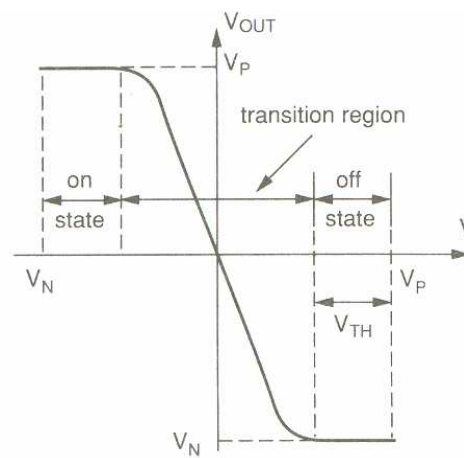
(c)

Fig .2.1. Inverter Architectures: (a) Sinking Inverter (b) Sourcing Inverter, (c) Push- pull Inverter.

The general voltage transfer representations for sinking inverter, sourcing inverter and Push-Pull inverter are shown in Fig 2.2.(a), 2.2.(b), 2.2.(c) respectively. In these voltage transfer curves, on and off state of transistor, transition region between switching on and off of transistor is shown, which tells about working of that architecture.



(a)



(b)

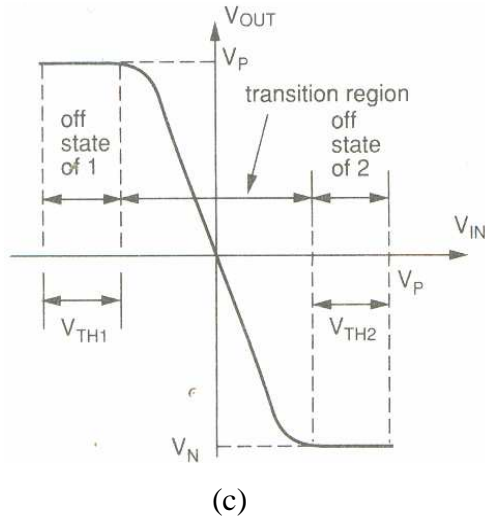


Fig.2.2. Typical voltage transfer functions for the inverters (a) Sinking Inverter (b) Sourcing Inverter, (c) Push-pull Inverter

The small signal ac performance of sinking and sourcing inverters can be calculated with the help of small signal model. It is seen that ac gain, input resistance, and the output resistance are as follows:

$$A_v = v_{out}/v_{in} = -g_m/(g_0 + g_1) = -g_m \cdot R_{out}$$

$$R_{in} = r_i = 1/g_i$$

$$R_{out} = r_o \cdot r_1 / (r_o + r_1) = 1/(g_0 + g_1)$$

In Push-Pull amplifier, the ac gain, the input resistance, and the output resistance seen with the help of small signal model are as follows:

$$A_v = v_{out}/v_{in} = -(g_{m1} + g_{m2}) / (g_{o1} + g_{o2}) = -(g_{m1} + g_{m2}) \cdot R_{out}$$

$$R_{in} = r_{i1} \cdot r_{i2} / (r_{i1} + r_{i2}) = 1 / (g_{i1} + g_{i2})$$

$$R_{out} = r_{o1} \cdot r_{o2} / (r_{o1} + r_{o2}) = 1 / (g_{o1} + g_{o2})$$

The possible MOS implementations of the sinking inverter architecture are shown in Fig.2.3. Each of the lower block is a realization of the voltage controlled current sink using an n-channel transistor and each of the upper block represents a realization of the load connected between the output of the voltage-controlled current-sink and V_{dd}.

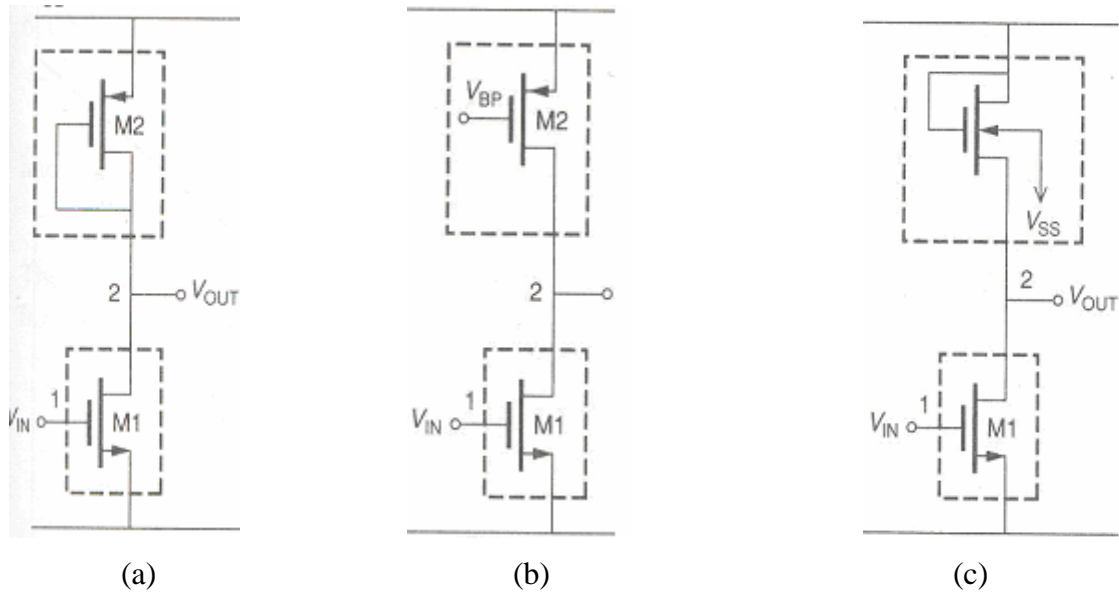


Fig.2.3. Possible realizations of Sinking Inverter with (a) Active p-channel load, (b) Current source load, (c) Active n-channel load.

The performance of the inverter varies with the different load used. The Table.1 shows theoretical values of ac voltage gain, ac output resistance and bandwidth.

The performance of the inverting amplifier can be improved by use of additional devices, like cascode amplifiers. The improvements are not only in the area of performance but also in the area of design freedom.

2.1.2. Differential Amplifiers

The differential amplifier is among the most important circuit in analog design. It is very useful to use as an input stage and is highly compatible with IC technology. The differential amplifier has two inputs. It amplifies the difference of input and gives single ended or differential output. The differential amplifiers should have higher output swings and high rejection of supply noise.

The differential-mode input voltage, V_{id} , of differential amplifier is defined as the difference between vin_1 and vin_2 . This voltage is defined between two terminals, neither of which is ground. The common mode input voltage V_{ic} is the average value of vin_1 and vin_2 .

$$V_{id} = vin_1 - vin_2$$

$$V_{ic} = (V_{in1} + V_{in2})/2$$

$$V_{in1} = V_{ic} + V_{id}/2$$

$$V_{in2} = V_{ic} - V_{id}/2$$

The output voltage of differential amplifiers is expressed as:

$$V_{out} = A_{vd} V_{id} + A_{vc} (v_{in1} + v_{in2})/2$$

The differential amplifier can be implemented with two transistors in differential arrangement and with different loads, like resistive load, cascode load and mirror load etc.

2.1.3 Output amplifiers

This amplifier is necessary to interface the output of an amplifier to a low resistance or low-capacitance load. Normally amplifiers are incapable of driving a low resistance/ high capacitance load. [2] Shows one technique for CMOS buffer amplifiers to derive low resistive loads. The output amplifier is difficult to design since it requires large, linear output swings across low resistive load[3].

The output load of the circuit can significantly influence the performance of the circuit. The output load generally consists of a load resistor R_L , in parallel with a load capacitor C_L . The objective of an output amplifier is to provide large output voltage swing across the load. The requirements of output amplifier can be divided into 'static and dynamic' requirements. The static requirement can be stated as the ability to maintain a dc voltage somewhere between the power supply limits across a specified load resistor. Therefore the output stage should have a low thevenin output resistance and should be efficient to avoid large power dissipation in the amplifier. The dynamic requirement is the ability to charge or discharge a large capacitance at a specified voltage rate. This requirement is often associated with slew rate or maximum output voltage rate of an analog circuit.

The maximum source/ sink output currents and the ac output resistance characterize the static performance of the output amplifier. The quiescent bias current of the amplifier relates these two measures.

Under dynamic conditions, the output sinking/ sourcing current needed to charge or discharge C_L may be greater than that required to maintain given dc voltage across R_L . It is assumed that the output voltage is in the range where both transistors are in saturation. The current required to charge a capacitor C_L at slew rate is given by:

$$\begin{aligned} |I_{out}| &= C_L [dV_{out}/ dt] \\ &= C_L \cdot \text{Slew rate.} \quad \dots\dots\dots(1) \end{aligned}$$

As the output voltage deviates from 0 V, the current available for charging C_L is reduced by the current necessary to sustain a non-zero value of V_{out} across R_L .

2.1.4. Operational Amplifiers

For analog circuits, the operational amplifier is one of the most useful blocks. The opamp is usually made up of two gain stages, namely, the differential input stage and the output stage.

Operational Amplifier, unlike the transconductance amplifier, includes an output stage capable of driving off-chip low load resistances. Drive capability, linearity, and output swing are mainly (or almost completely) set by the output stage [4, 5, 6] which is the most critical block in the design of low-voltage opamps.

The focus of inverting and differential amplifier is on the small signal performance. This includes the ac gain, input and output resistances, bandwidth and noise. These amplifiers are typically used as input or interstage amplifiers and do not have large signal swing requirements. The focus of output amplifiers is on large signal analysis. The key performance aspects include large signal swing, linearity, efficiency, and low output impedance. In operational amplifier, the emphasis includes both small signal & large signal considerations.

2.2. Performance factors of Amplifiers:

- **Distortion**

If the output signal is not like the input signal in shape or frequency, the signal is said to be distorted. Distortion is any undesired change in a signal from input to output.

An amplifier distortion can be characterized by the influence of the amplifier upon a pure sinusoidal signal[8]. Distortion is caused by the non-linearity of the transfer curve of the amplifier. If pure sinusoid is given as

$$V_{in}(\omega) = V_p \sin(\omega t)$$

is applied to the input, the output of amplifier with distortion will be

$$V_{out}(\omega) = a_1 V_p \sin(\omega t) + a_2 V_p \sin(2\omega t) + \dots + a_n V_p \sin(n\omega t)$$

Harmonic Distortion (HD) : for the *i*th harmonic can be defined as the ratio of magnitude of the *i*th harmonic to the magnitude of the fundamental.

$$HD_2 = a_2 / a_1$$

$$HD_3 = a_3 / a_1$$

Total harmonic Distortion (THD): is defined as the square root of the ratio of the sum of all of the second and higher harmonics to the magnitude of the first or fundamental harmonic. Thus THD can be expressed as

$$THD = [a_2^2 + a_3^2 + a_4^2 + \dots + a_n^2]^{1/2} / a_1$$

- **Efficiency**

The efficiency of an amplifier refers to the amount of power delivered to the output compared to the power supplied to the circuit.

$$\text{Efficiency} = P_{RL} / P_{supply}$$

- **Power Dissipation**

The power dissipated in load and dissipated by source is calculated with the help of .power command which is used alongwith .tran command.

The average power, the instantaneous minimum power and the instantaneous minimum power (in Watts) and the time of maximum and minimum power consumption (in seconds) are reported.

The instantaneous power P_t dissipated by voltage source at time t is the current through the source multiplied by the voltage drop across the source. The average power P for time interval (t_1, t_2) is computed using the trapezoidal approximation to evaluate the integral:

$$\bar{P}(t_1, t_2) = \frac{1}{t_2 - t_1} \int_{t_1}^{t_2} P(\tau) d\tau \dots\dots\dots(2)$$

- **Output Voltage Swing**

Output voltage swing is the range over which the output voltage can vary without excessive distortion. Infact the output voltage swing gives the value of the maximum positive and negative voltages over which transistor will be out of saturation. The output swing can be noted from the plot showing variation in output with the variation in input signal.

- **Bandwidth**

In the frequency domain, $A_v(\omega)$ of the ideal inverter should have a magnitude, A_{v0} , independent of frequency and a phase shift of ± 180 degree. At some frequency, the magnitude of $A_v(\omega)$ of the practical inverter will decrease. The frequency at which the magnitude of $A_v(\omega)$ is equal to $A_{v0}/ 2$ is called the -3dB frequency. The gain of integrated circuit inverters is A_{v0} for all frequencies sufficiently below $\omega_{-3\text{dB}}$. Thus the bandwidth of the inverter is -3dB frequency.

- **Output Resistance**

Output resistance affects the speed with which the amplifier can charge a capacitor connected to its output, and hence the highest signal frequency. Output resistance r_{out} for different topologies using small signal model, are evaluated.

For sinking and push-pull inverter, $r_{\text{out}} = 1 / (g_{\text{ds1}} + g_{\text{ds2}})$

For cascode architecture, $r_{\text{out}} = r_{\text{ds1}} \cdot g_{\text{m2}} \cdot r_{\text{ds2}} \parallel r_{\text{ds3}}$

The AC gain, Output resistance and Bandwidth of sinking inverter with n-channel active load, with p-channel active load and with current source load and push pull inverter with different type of loads are shown in Table.1.

Table1 : The AC gain, output resistance and bandwidth of sinking inverter and push pull inverter.

Inverter	AC voltage Gain	AC output resistance	Bandwidth (Cgb=0)
n-channel active load sinking inverter	$-g_{m1}/(g_{m2}+g_{mb2})$	$1/(g_{m2}+g_{mb2})$	$(g_{m2} + g_{mb2}) / (C_{bd1} + C_{gd1} + C_{gs2} + C_{bd2})$
p-channel active load sinking inverter	$-g_{m1}/g_{m2}$	$1/g_{m2}$	$(g_{m2} + g_{mb2}) / (C_{bd1} + C_{gd1} + C_{gs2} + C_{bd2})$
Current source load sinking inverter	$-g_{m1} / (g_{ds1} + g_{ds2})$	$1/(g_{ds1} + g_{ds2})$	$(g_{ds1} + g_{ds2}) / (C_{bd1} + C_{gd1} + C_{gd2} + C_{bd2})$
Push-pull inverter	$-(g_{m1} + g_{m2}) / (g_{ds1} + g_{ds2})$	$1 / (g_{ds1} + g_{ds2})$	$(g_{ds1} + g_{ds2}) / (C_{bd1} + C_{gd1} + C_{gd2} + C_{bd2})$

Chapter 3

Output Amplifiers without Feedback

The output stages primarily provide sufficient power to the output load to drive a speaker or other power device.

One method to characterize amplifiers is by class of operation. Basically, amplifier classes represent the amount the output signal varies over one cycle of operation for a full cycle of input signal. A brief description of amplifier classes is as follows:

Class A: The output signal varies for a full 360 degree of cycle. The Q-point of Class A amplifier is such biased that at least half the signal swing of the output may vary up and down without going to a high enough voltage to be limited by the supply voltage level, or too low to approach the lower supply level.

Class B: A class B circuit provides an output signal varying over one half the input-cycle, or for 180 degree of signal. The class B operation is set by selecting proper operating point of transistor. For Class B amplifiers to be used in amplification applications, push-pull architecture is used.

Class AB: For Class AB operation, the output signal swing occurs between 180 deg & 360 degree and is neither Class A nor Class B operation. This amplifier Q-point is biased at a dc level between the Q-point of Class A and Class B Q-point.

Class C: The output of a class C amplifier is biased for operation at less than 180 degree of the cycle and will operate only with a tuned (resonant) circuit which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.

Class D: This class is a form of amplifier operation using pulse signals which are on for a short interval and off for a long interval. Using digital techniques makes it possible to

obtain a signal that varies over the full cycle to recreate the output from many pieces of input signal.

There are two distinct approaches to implementing output stages:

- Output amplifier without feedback
- Output amplifier with feedback

A conservative approach to characterize the output signal swing of MOS amplifiers is to assume that all devices must be in saturation. This constrains the operation to the transition region of the voltage transfer function of the amplifier. The resulting output range is not as large as that which could be achieved if some of the devices are allowed to operate in the active or ohmic region.

3.1 Class A Common Source Output Amplifier

The MOS current source load inverting amplifier has a higher ac gain than the active p-channel and active n-channel load.

Consider the circuit of current source load (sometimes called a “pull-up”) class A sinking amplifier as shown in Fig. 3.1. It will be assumed that the current flows in both output devices during the entire swing of the output voltage (Class A operation)

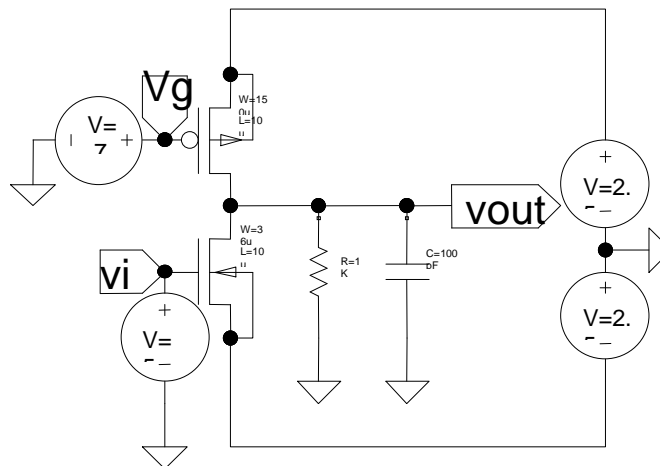


Fig.3.1. Schematic of Class A Common Source Output Amplifier

The maximum source current, I_{out}^+ , that can be obtained from the circuit of fig.1 occurs when M_1 (lower transistor) is off and M_2 (upper transistor) is saturated, is given as

$$I_{out}^+ = K_p' W_2 [V_{dd} - V_g - |V_{tp}|]^2 / 2L_2 \dots\dots\dots(3)$$

It is important to note that as long as M_2 is saturated, this current always flows in M_2 regardless of the value of V_{in} . The maximum sinking current, I_{out}^- , for Fig.1 occurs when M_1 is saturated and $V_{in} = V_{dd}$ and is given as

$$I_{out}^- = K_n' \cdot W_1 (V_{dd} - V_{ss} - V_{tn})^2 / 2L_1 - I_{out}^+ \dots\dots\dots (4)$$

Here, I_{out}^- must also include I_{out}^+ because of Class A nature of biasing. The current-sinking capability of M_1 can easily exceed I_{out}^+ because the gate-source voltage of M_1 can be very large.

If V_{out} approaches V_{ss} , then M_1 will pass from the saturation to ohmic region where $V_{ds1} < V_{gs1} - V_t$. If a load resistance R_L is connected to the output, V_{ds1} is small, and $V_{in} = V_{dd}$, Then eq. (4) for ohmic region becomes

$$I_{d1} \approx K_n' \cdot W_1 (V_{dd} - V_{ss} - V_{tn})(-I_{out}^- \cdot R_L - V_{ss}) / L_1 \dots\dots\dots (5)$$

Since I_{d1} is sum of I_{out}^+ and I_{out}^- , solving for I_{out}^- as

$$I_{out}^- \approx [K_n' \cdot W_1 (V_{dd} - V_{ss} - V_{tn}) \cdot V_{ss} / L_1 - I_{out}^+] / [1 + K_n' (W_1 / L_1) \cdot (V_{dd} - V_{ss} - V_{tn}) \cdot R_L] \dots\dots\dots(6)$$

When V_{out} approaches V_{dd} , I_{out}^+ will become dependent on R_L and have a smaller value than that of Eq.(3).

3.1.1 Designing of Class A Output Amplifier:

Specifications:

$R_L = 2K\Omega$, $C_L = 10pF$,

Slew rate = 5V/us, voltage swing = +-2V,

$$V_{dd} = -|V_{ss}| = 2.5V.$$

Design Steps:

Step 1. Calculate the bias current using eq. (1)

$$I_{bias} = C_L * \text{Slew rate.}$$

$$I_{out}^+ \text{ (Sourcing current)} = 1.05 \text{ mA}$$

Step 2. Find the bias voltage for upper transistor (M_2), so that it remains in saturation.

$$V_g = 0.74V$$

Step 3. Calculate aspect ratio of M_1 using eq. (3)

$$(W/L)_p = 125\mu/2\mu,$$

Step 4. Calculate aspect ratio of M_2 using eq. (4)

$$\text{And, } I_{out}^- \text{ (Sinking current)} = 10.5 \text{ mA}$$

$$(W/L)_n = 38\mu/2\mu,$$

The sinking current is approximately 10 times sourcing current. The sourcing current can be increased by decreasing the gate voltage on M_2 (upper transistor) or increasing (W_2/L_2) . In either case, the bias current that flow would increase, causing the power dissipation in the inverter to increase.

The small circuit resistance of the inverting voltage amplifier is a measure of how the AC gain will be influenced by the presence of a small load resistance.

Using eq $r_{out} = 1 / (g_{ds1} + g_{ds2})$, r_{out} is calculated.

$$\text{Using eq } A_v = -g_{m1} / (g_{ds1} + g_{ds2}) = [2K_n' (W_1/L_1)]^{1/2} / (\lambda_n + \lambda_p)(I)^{1/2}$$

The gain A_v for Class A amplifier, assuming that R_L is infinite.

When loaded with R_L , new gain A_v' was calculated, as

$$A_v' = A_v [R_L / (R_L + r_{out})] \dots\dots\dots(7)$$

$$= -g_{m1} / (g_{ds1} + g_{ds2} + G_L).$$

The Class A output amplifier has a zero at $z = g_{m1}/C_{gd1}$

$$\text{and a pole at } p = -(g_{ds1} + g_{ds2} + G_L) / (C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L) \dots\dots\dots(8)$$

The new value of gain A_v' for finite R_L is reduced from the value that obtained with infinite R_L .

Another desirable characteristic of an output amplifier is to have small value of r_{out} , so that small signal voltage gain by eq. (7) is not reduced.

The Total harmonic distortion in output for small value of input is less than the distortion for higher value of input. The THD measured for $V_{in} = 0.2$ is 1.76 whereas THD for $V_{in} = 0.5$ is 3.157, which is higher than that for $V_{in} = 0.2$, as shown in Appendix II. The THD also varies with change in frequency. The variation of THD in this output Stage, for $v_{in} = 0.5$ with variation in frequency is shown in Fig.3.5.

The efficiency of this amplifier is: 6.9 %

$$\text{Efficiency} = P_{RL} / P_{\text{supply}} = [v_{out}(\text{Peak})^2 / 2 RL] / (V_{dd} - V_{ss}) I_q$$

We know that, $I_q = (V_{dd} - V_{ss}) / 2RL$.

$$\text{Therefore, Efficiency} = (v_{out}(\text{Peak}) / (V_{dd} - V_{ss}))^2$$

The maximum efficiency of the Class A output stage occurs when $V_{out}(\text{peak})$ is $0.5(V_{dd} - V_{ss})$, which is 25%

3.1.2 Simulation Results:

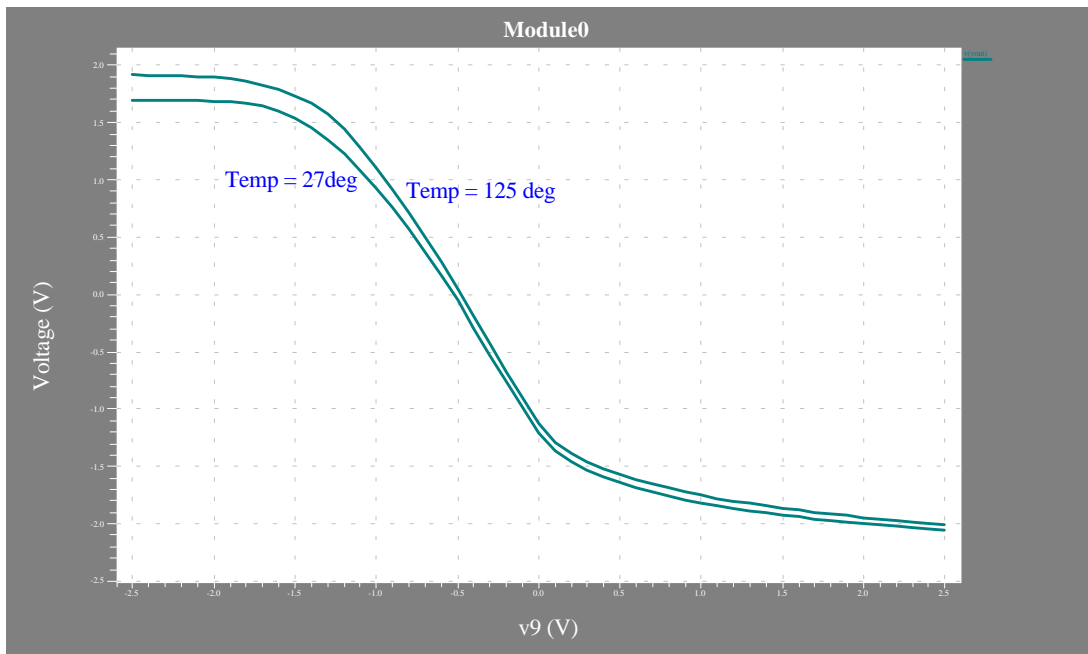


Fig.3.2. Plot of the output voltage of the circuit of Fig.3.1. as a function of 2KΩ load resistor.

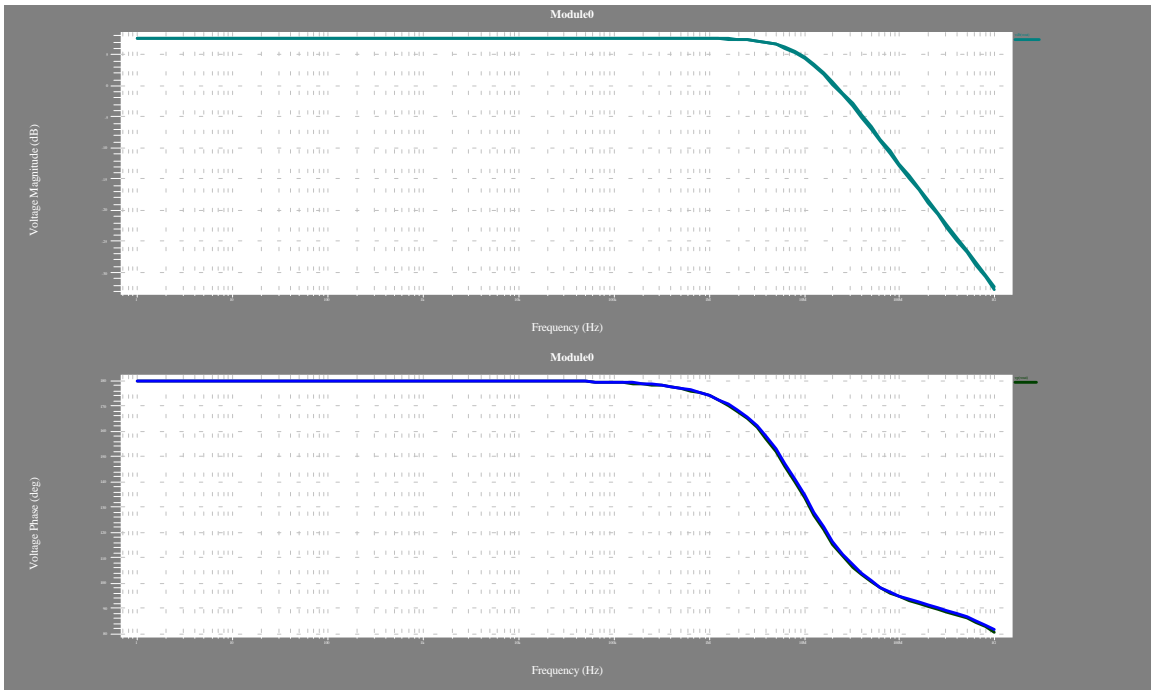


Fig.3.3. AC Analysis of Class A Output Amplifier.

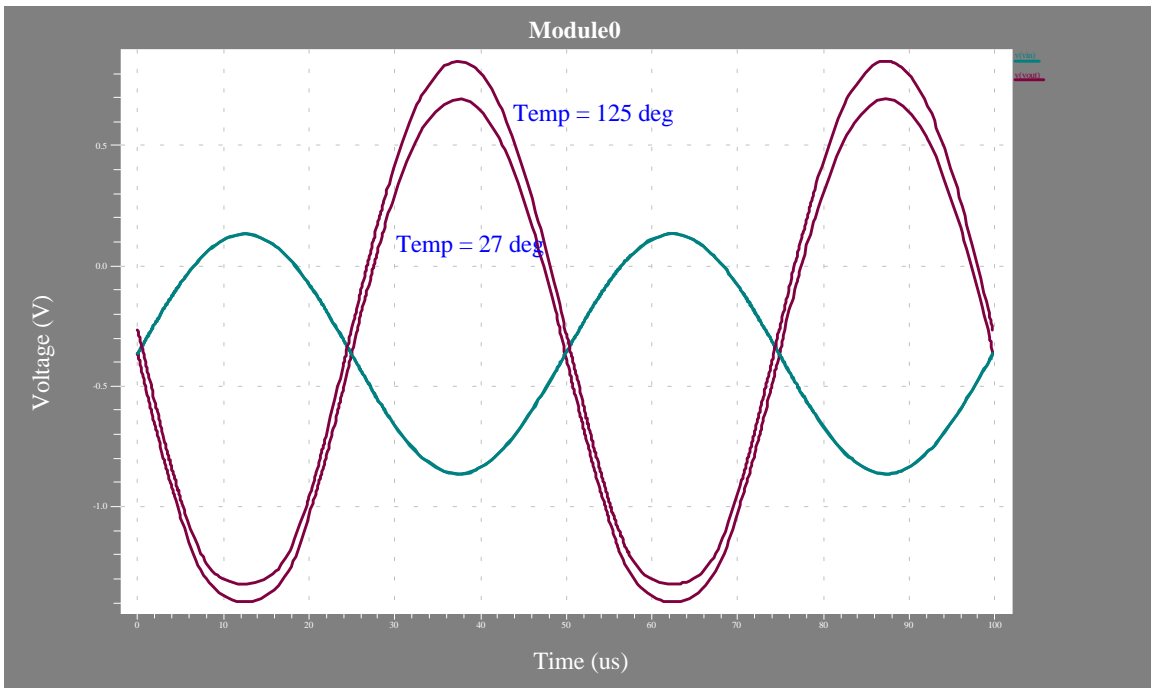


Fig.3.4. Plot of sinusoidal input ($V_{\text{peak}} = 0.5$) and output voltage for Fig.3.1.

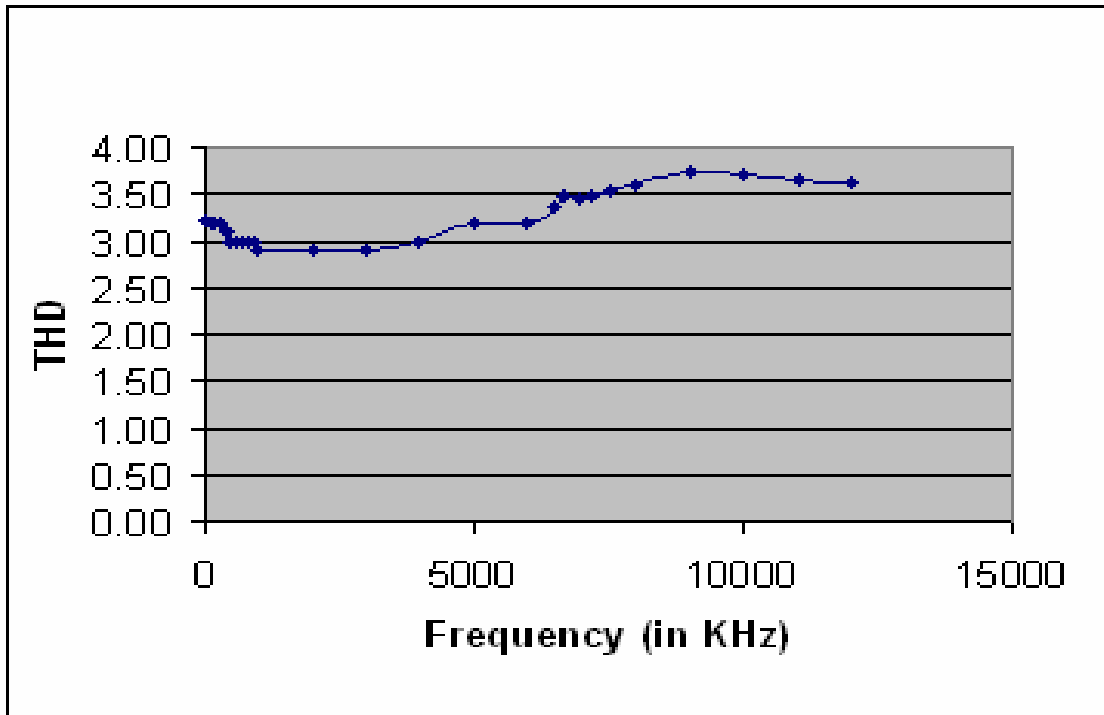


Fig.3.5. The variation of THD with frequency for Class A Output Amplifier.

The power results are shown in Appendix II.

Efficiency = 6.9 %

3.2. Class AB Amplifier Without Feedback

A second method of implementing an output amplifier without feedback in MOS Technology is the common-source Class B or Class AB amplifiers. V_b is a floating battery used to establish the proper bias of the devices. The sinking/sourcing output current capability of such amplifiers is very large and is limited primarily by the power dissipation capability of the devices.

The circuit diagram of push-pull architecture operating in Class AB output stage is shown below:

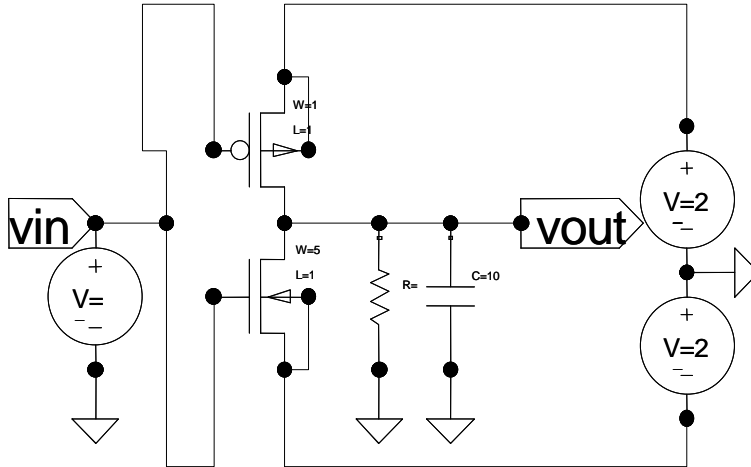


Fig.3.6. Class AB Output Amplifier without Feedback

Specifications:

$$R_L = 2K\Omega, C_L = 10pF,$$

$$\text{Slew rate} = 5V/\mu s, \text{ voltage swing} = \pm 2V,$$

$$V_{dd} = -|V_{ss}| = 2.5V$$

3.2.1. Designing Of Class AB Output Amplifier:

Step 1 : Slew Rate = $5V/V$,

$$I_{bias} = C_L * \text{Slew Rate} = 1.05mA$$

Step 2 : Calculate $(W/L)_n$ by the above eq.

$$I_{d1} \approx K_n' \cdot W_n (V_{dd} - V_{ss} - V_{tn}) (-I_{out} - R_L - V_{ss}) / L_n$$

$$(W/L)_n = 38/4$$

Step 3: Calculate $(W/L)_p$ by eq..

$$(W/L)_p = (W/L)_n * K_n' / K_p$$

$$(W/L)_p = 91/4$$

The two high-efficiency output stages providing rail-to rail output swing and high output current are the symmetric class-AB output stage[9], and the asymmetric class-AB output stage [7] are discussed in [10]. The symmetric class-AB output stage is based on a novel solution, which provides the drive capability of a simple inverter stage (i.e., with the same peak-to-peak output swing and an overdrive limited by only two saturation

voltages), and uses a simple and accurate current control. High linearity for low input level is also achieved. The asymmetric class-AB output stage is simpler than the previous one, but, due to its asymmetric topology, we expect a lower linearity performance.

The simulation Results are shown in section.3.2.2. In Fig.3.7, as both transistors, M1 and M2 are conducting in the region around $V_{in} = 0$, this amplifier is called Class AB.

Harmonic distortion in class-AB circuits can be evaluated with the approach suggested in [11 , 12]. The method gives the second and third-order harmonic distortions as a function of the small-signal voltage gain a_1 , as well as the output derivative at the highest and lowest extreme of the input variation a^+ and a^- respectively. The following harmonic distortion terms results in

$$HD2 = (a^+ - a^-) / 8a_1$$

$$HD3 = (a^+ - a^- - 2a_1) / 24a_1$$

The THD at frequency 20,000 Hz for this amplifier is 6.081%

Power consumed results are shown in Appendix II.

Efficiency = 12.2 %

3.2.2. Simulation Results:

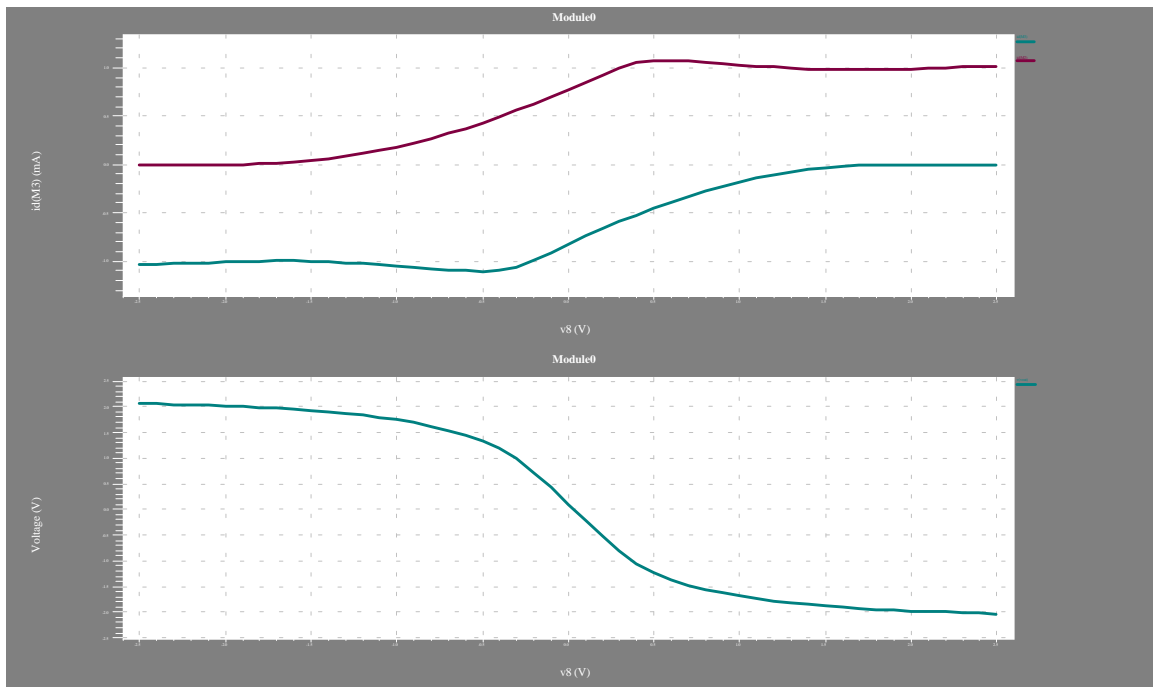


Fig. 3.7. Plot of the output voltage and drain current in M1 & M2 of Fig.3.6.

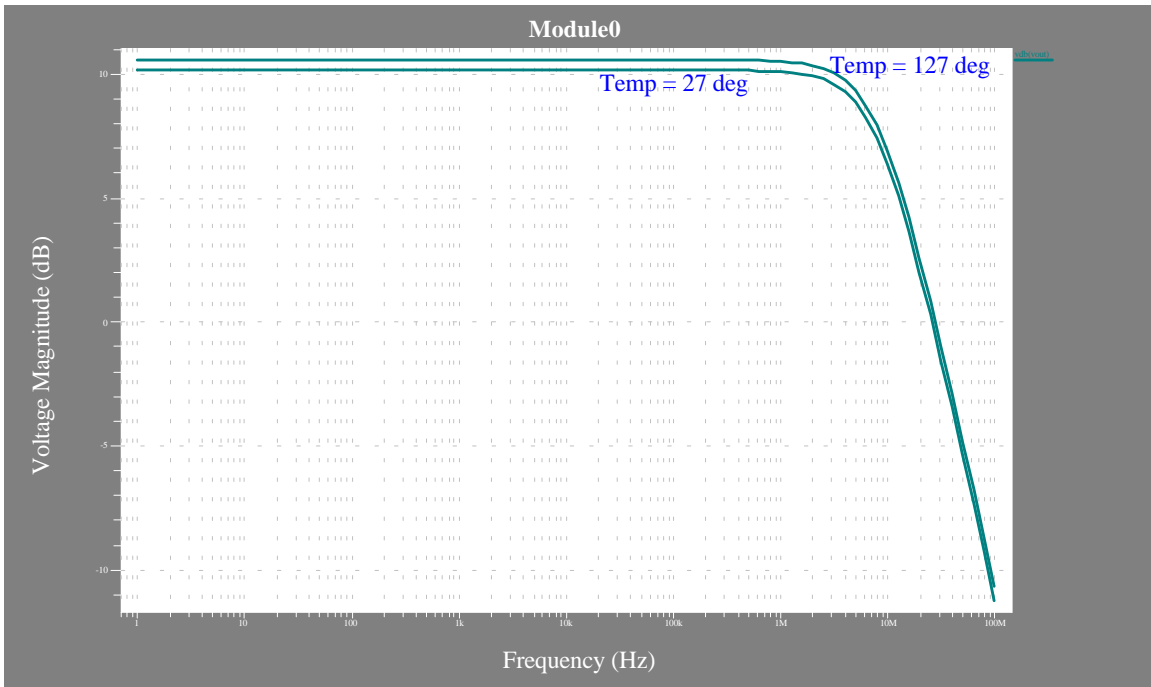


Fig.3.8. AC Analysis of class AB Output Amplifier

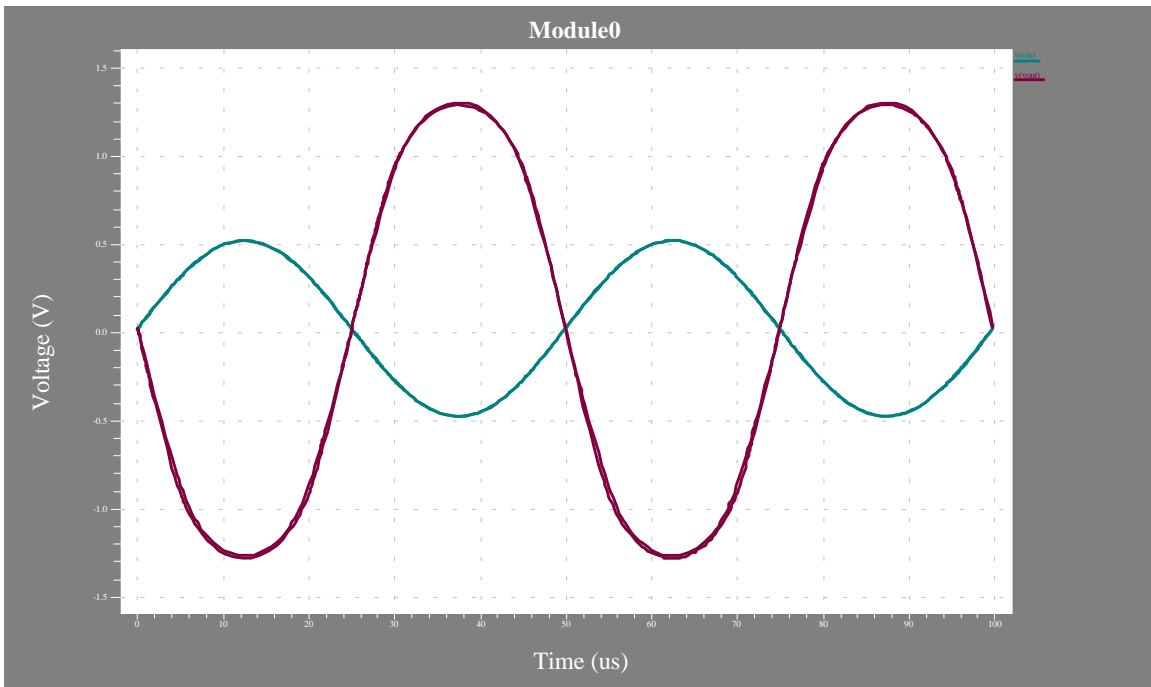


Fig. 3.9. Sinusoidal output for 0.5 V (p-p) sinusoidal input.

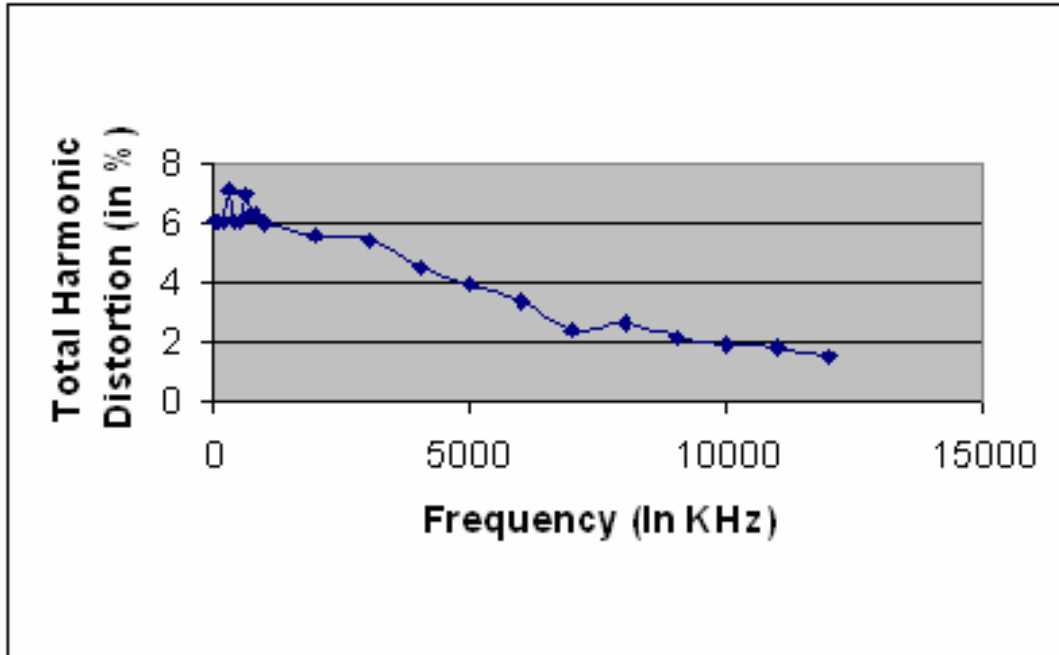


Fig. 3.10. The variation of THD with frequency for Class AB Output Amplifier

3.3. Class B Output Amplifier without feedback

In Fig. 3.11, the transistors are biased so that no drain current flows when V_{in} is zero, the stage is termed Class B. When V_{in} is positive, the lower device is on and the upper device is off. When V_{in} is negative, the lower device is off and the upper device is on. The maximum possible efficiency of the Class B amplifier for a sinusoidal Output signal is 78.5%.

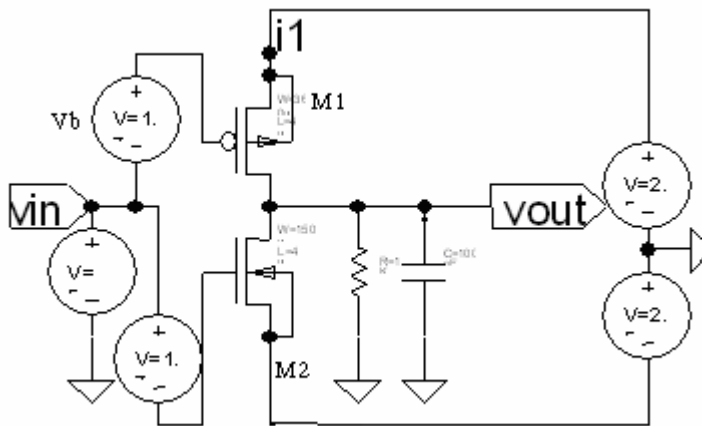


Fig. 3.11. Class B Output Amplifier without Feedback

Here, $I_{d1} = I_{out}$

$$\text{So, } I_{d1} \approx K_n' \cdot W_1 (V_{dd} - V_{ss} - V_{tn})(-I_{out} - R_1 - V_{ss}) / L_1 \dots\dots\dots(9)$$

In order to balance the ability of the amplifier to source/sink current,

$$(W/L)_2 = (K_n/K_p)(W_1/L_1) \dots\dots\dots(10)$$

3.3.1. Designing Of Class B Output Amplifier:

Specifications

Output swing = +-2V, $V_{dd} = |-V_{ss}| = 2.5 \text{ V}$

$I_{out} = 1.05 \text{ mA}$

Design Procedure:

Step 1: (W_1/L_1) is calculated from following eq. (9)

$$(W_1/L_1) = 38 \mu / 4 \mu.$$

Step 2: (W_2/L_2) is calculated from eq. (10)

$$(W_2/L_2) = 91 \mu / 4 \mu.$$

We can see from fig.3.7. that to operate in class B , $V_b = 1.81 \text{ V}$

This circuit has a maximum sink/source current of 1. 4mA, resulting in a $\pm 1.4 \text{ V}$ output signal swing.

Here $V_b = 1.81$, and the amplifier is operating in Class B mode. Fig.7 shows a simulation corresponding to that of fig.7 for $V_b = 1.81 \text{ V}$. Several things should be noted. The first is that M1 is off when. M2 is on and vice versa. The second is that V_b has caused the maximum source and sink currents to be reduced from 1.05 mA to 0.9mA. Also note that the transfer function is nonlinear about $V_{in} = 0$. This nonlinearity will introduce distortion in the output signal. A good compromise for this amplifier would be to go back to Class AB operation by choosing appropriate V_b .

$$\text{Efficiency} = P_{RL} / P_{supply} = [v_{out}(\text{peak})^2 / 2RL] / [(V_{dd} - V_{ss})(V_{out}(\text{peak})) / \pi RL]$$

The term $V_{out}(\text{peak}) / \pi RL$ in the denominator represents the average current flow for a half wave rectified sinusoid. The maximum efficiency occurs when $V_{out}(\text{peak})$ is the largest, i.e. $0.5(V_{dd} - V_{ss})$, and is 78.5%.

$$\text{Efficiency} = 7.2 \%$$

The primary advantage of the implementations of Class B / AB is that the, maximum sourcing/sinking current is not limited by the bias current. This allows, output amplifiers to have I_{out}^+ limitations similar to the I_{out}^+ levels of the Class A output amplifiers.

The variation of THD with change in frequency is shown in Fig. 3.15.

3.3.2. Simulation Results:

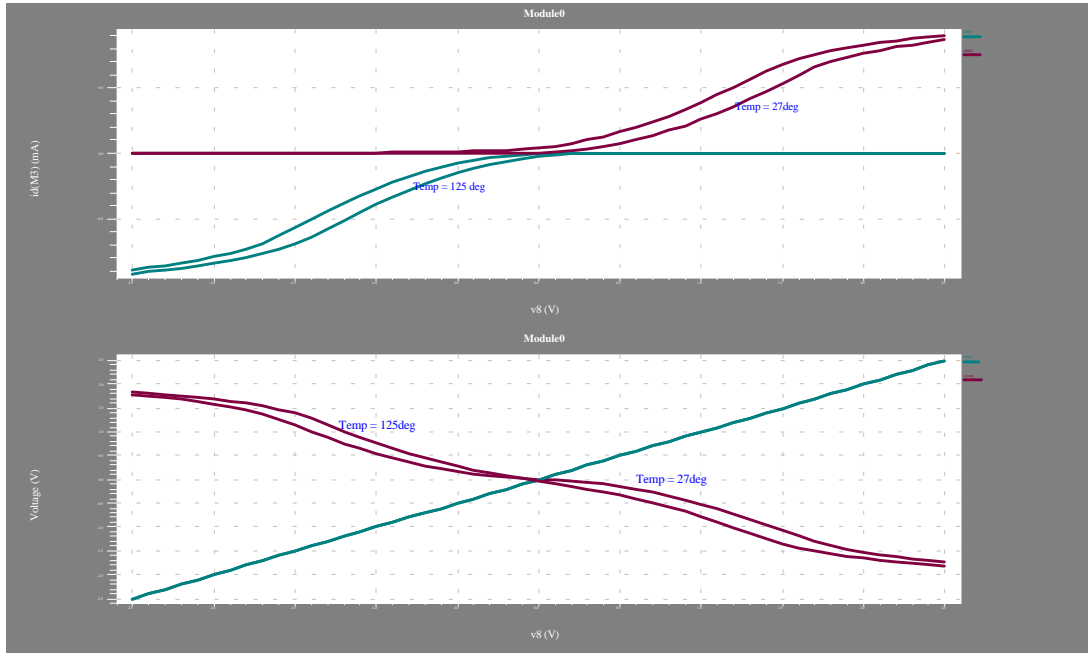


Fig..3.12. Output voltage and Class B Output Amplifier

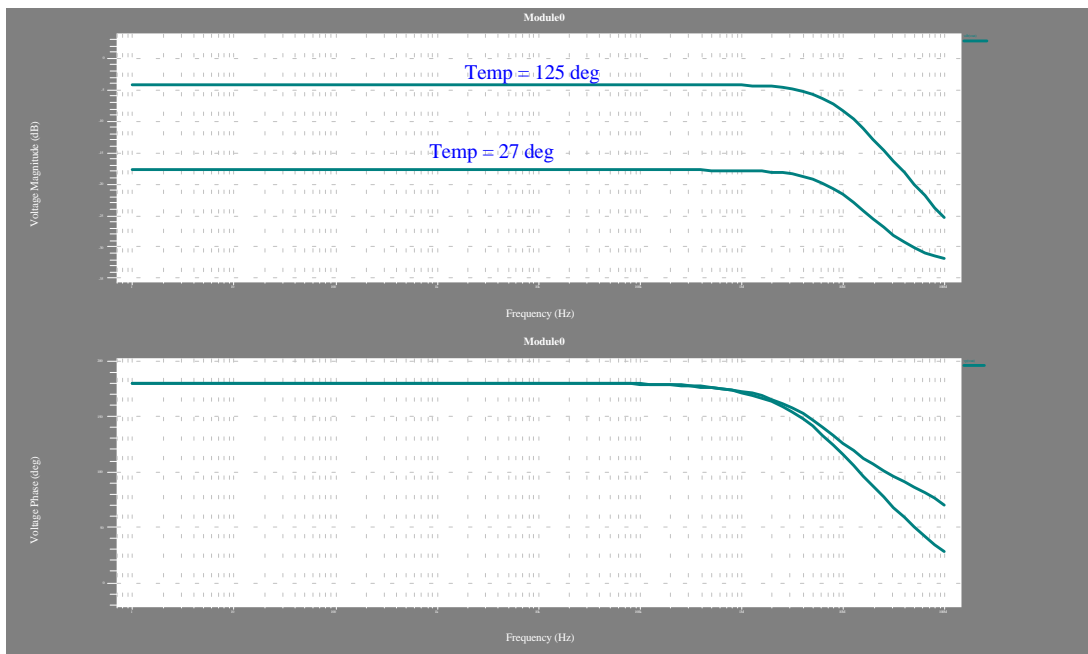


Fig. 3.13. AC Analysis of Class B Output Amplifier.

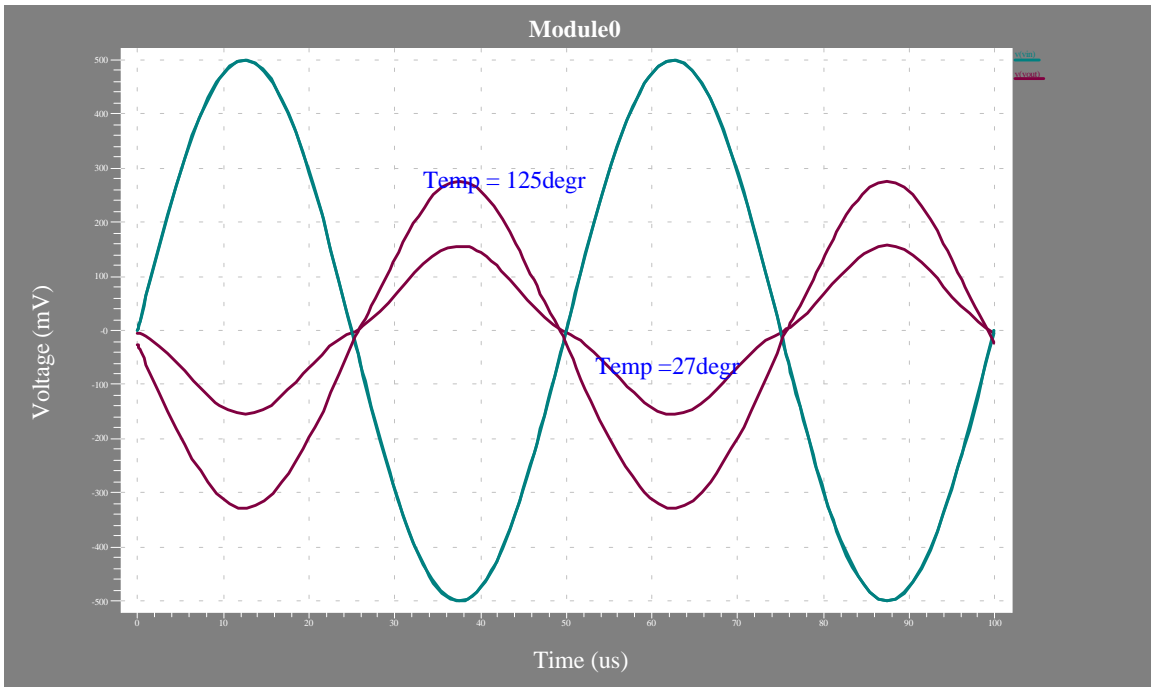


Fig.3.14. Sinusoidal Analysis of Class B output stage.

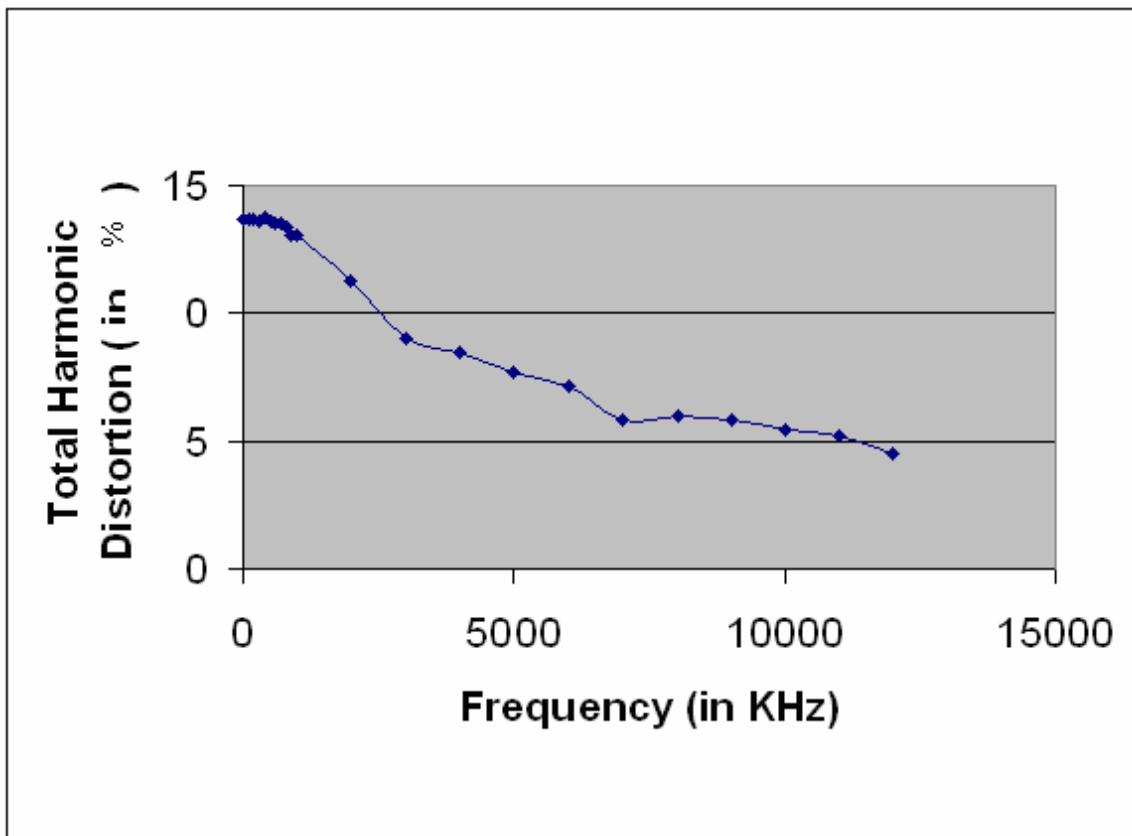


Fig. 3.15. Variation of THD of Class B with variation in Frequency

3.3.3. Floating Battery implementation for common source class B/ AB Push-Pull amplifier:

Class B/AB represents a good solution to the output amplifier, except for the implementation of floating battery, V_b . Figure below shows the cross-coupling of four devices that allow the design of Class AB or B operation. The operation is determined by the voltages V_{gg4} and V_{gg5} used to establish the bias current in the output devices M1 and M2. When input is taken positive, the current in M8 increases, and the current in M7

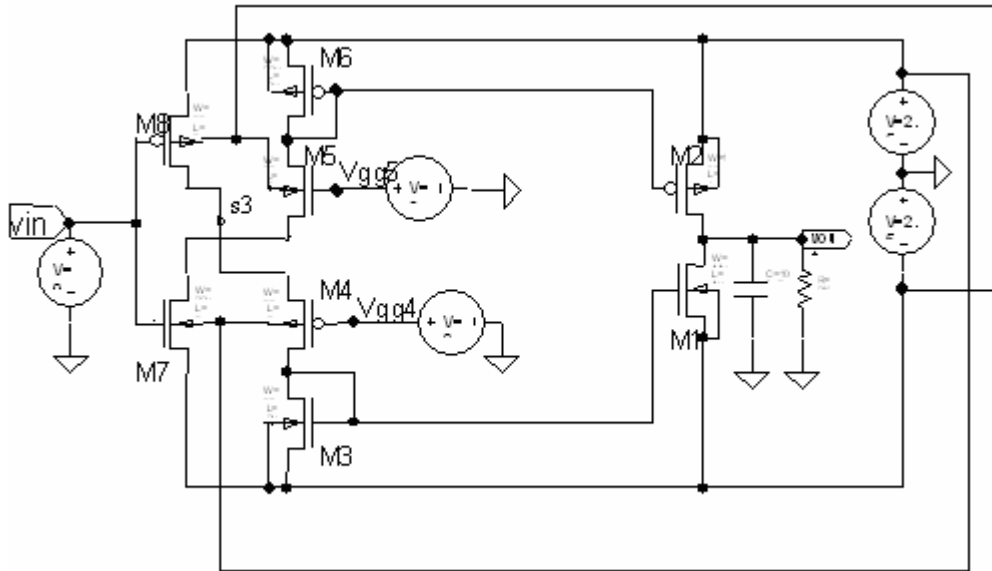


Fig. 3.16. Floating Battery implementation of class B/AB Amplifier

decreases. If the operation is Class B, then M7 turns off. As the current in M8 increases, it is mirrored as an increasing current in M1, which provides the sinking capability, for the output current. When v_{in} is decreased, M2 can source output current.

Using eq.(11), we can find the value of V_{gg4} and aspect ratio of M8, M4, M3.

$$I_1 = U_n C_{ox} (W/L)_8 (V_{in} - V_{s3} - V_{tn})^2 = U_n C_{ox} (W/L)_4 (V_{gg4} - V_{s3} - V_{tp})^2 = U_n C_{ox} (W/L)_3 (V_{s2} - V_{ss} - V_{tn})^2 \dots\dots\dots(11)$$

Similarly, V_{gg5} can also be calculated.

$$V_{gg4} = V_{gg5} = 2.5V$$

$$(W/L)_8 = (W/L)_5 = (W/L)_3 = 16/4 \text{ and } (W/L)_7 = (W/L)_6 = (W/L)_4 = 40/4.$$

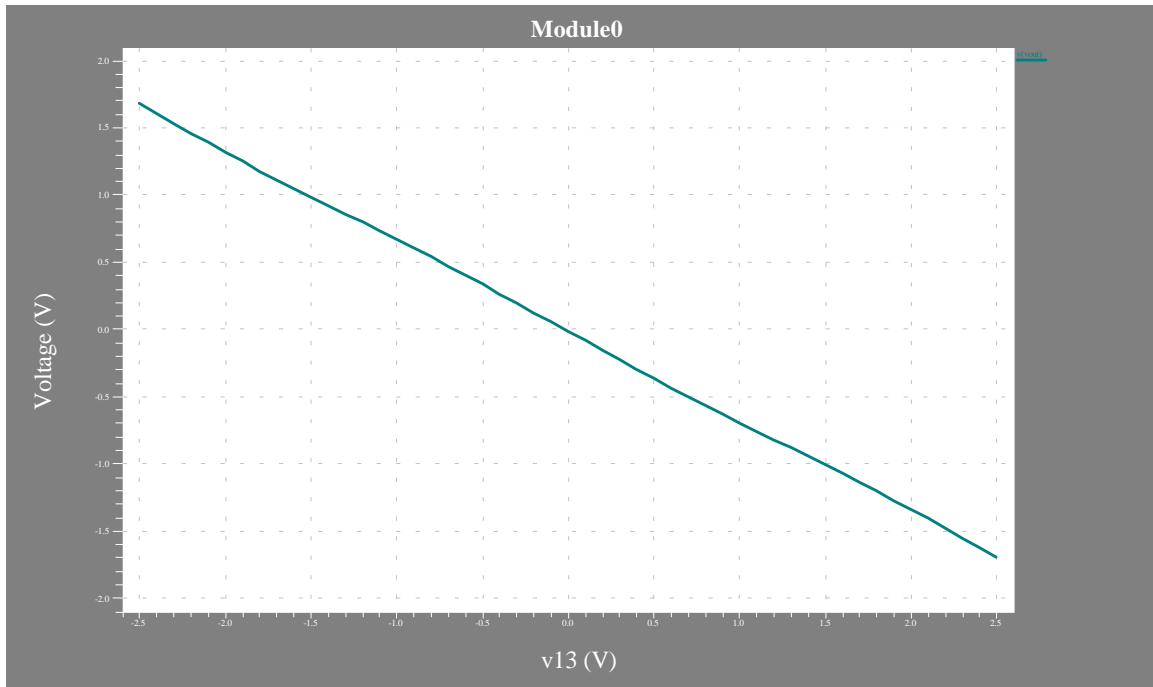


Fig. 3.17. Plot showing output swing for circuit of Fig. 3.16.

3.4. Cascode Amplifier

The cascode amplifier has two advantages over the inverting amplifiers. It provides a higher output impedance and it also reduces the effect of the Miller Capacitance on the input of the amplifier, which will be very important in designing the frequency behaviour of op-amp.

The input signal of a common gate stage may be a current. Also transistor in common-source arrangement converts a voltage signal to a current signal. The cascode of a CS stage and a CG stage is called a ‘cascode’ topology. Cascading can be extended to three or more stacked devices to achieve higher output impedance, but the required additional voltage headroom makes such configuration less attractive. For example, the minimum output voltage of a triple cascode is equal to the sum of three overdrive voltage.

Gm bear trade off with the bias current and device capacitances, it is desirable to increase the voltage gain by maximizing r_{out} .

The voltage gain is roughly equal to the square of intrinsic gain of the transistors.

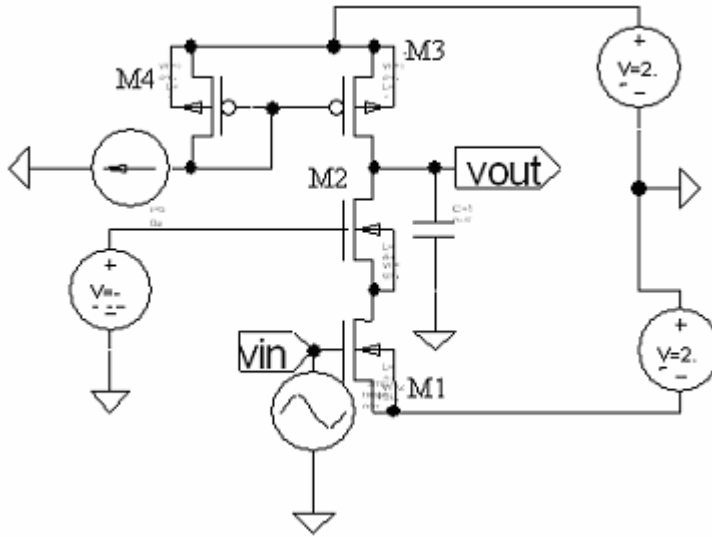


Fig 3.17. Schematic of Cascode Amplifier.

3.4.1. Design Procedure:

Specifications:

Slew rate = 5v/us,

$C_L = 10\text{pF}$,

$A_v = -50 \text{ V/V}$

Output voltage = $\pm 2\text{V}$

Design Steps:

Step 1: Calculate I_{bias} as

$$I_{\text{bias}} = C_L * \text{Slew Rate}$$

$$I_{\text{bias}} = I = 50\mu\text{A}$$

Step2: Calculate aspect ratio of M3 and M4 using eq.

$$(W/L)_3 = 2I / K_p' [V_{\text{dd}} - V_{\text{out(max)}}]^2$$

$$(W/L)_3 = 38.02 \cong \mathbf{152/4}$$

Step 3: $(W/L)_4 = I_{\text{bias}}(W/L)_3 / I$,

$$(W/L)_4 = \mathbf{152/4}$$

Step 4: Calculate aspect ratio of M1 using eq.

$$(W/L)_1 = (A_v \lambda)^2 I / 2 K_n'$$

$$(W/L)_1 = 61.70 \cong \mathbf{247/4}$$

Step 5 : Calculate aspect ratio of M2 using eq.

$$V_{out(min)} = V_{ds1(sat)} + V_{ds2(sat)}$$

$$= \{2I / K_n (W/L)1\}^{1/2} + \{2I / K_n (W/L)2\}^{1/2}$$

To calculate M2, $V_{d_{sat}2}$ is needed , and to calculate $V_{d_{sat}2}$ we need $V_{d_{sat}1}$.

$$V_{ds2(sat)} = \{2I / K_n (W/L)1\}^{1/2} = 0.160 \text{ V}$$

$$V_{d2(sat)} = V_{out(min)} - V_{ds1(sat)} = -1.66 \text{ V}$$

$$\text{Also, } V_{dd2(sat)} = \{2I / K_n (W/L)2\}^{1/2}$$

Therefore $(W/L)2 = 92/4$

Step 6 : Calculate V_{gg2} using eq.

$$V_{gg2} = V_{ds1(sat)} + V_{gs2}$$

$$V_{gg2} = -0.87$$

3.4.2. Simulation Results:

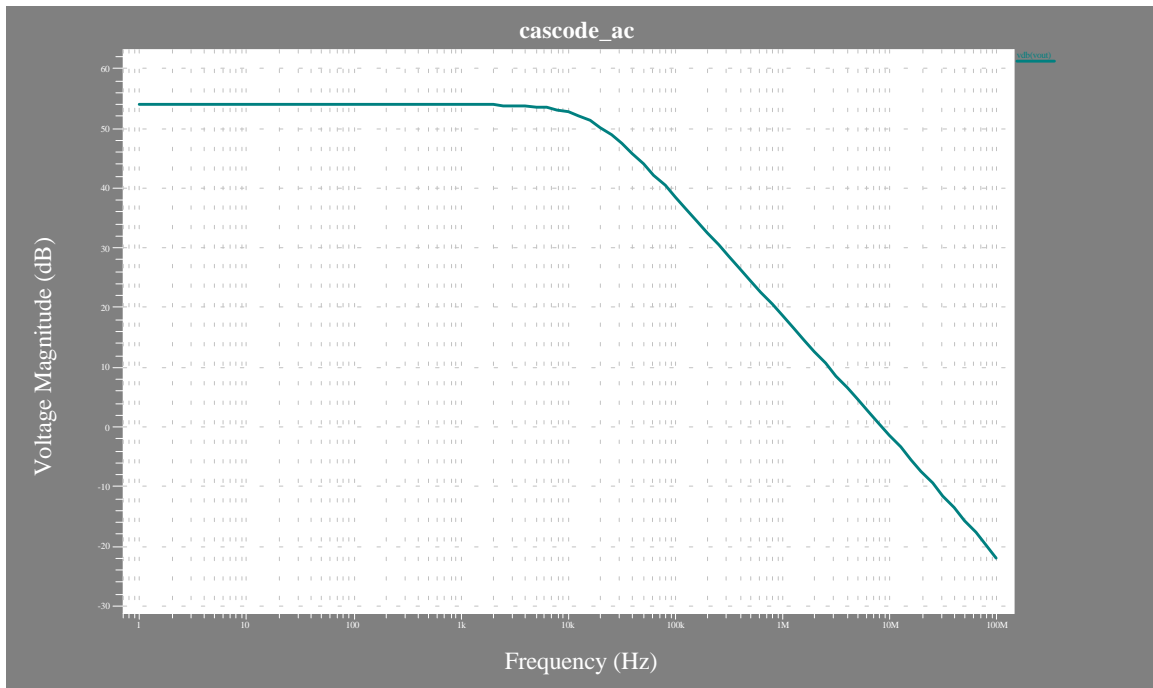


Fig. 3.18. Dc Analysis of Cascode Amplifier:

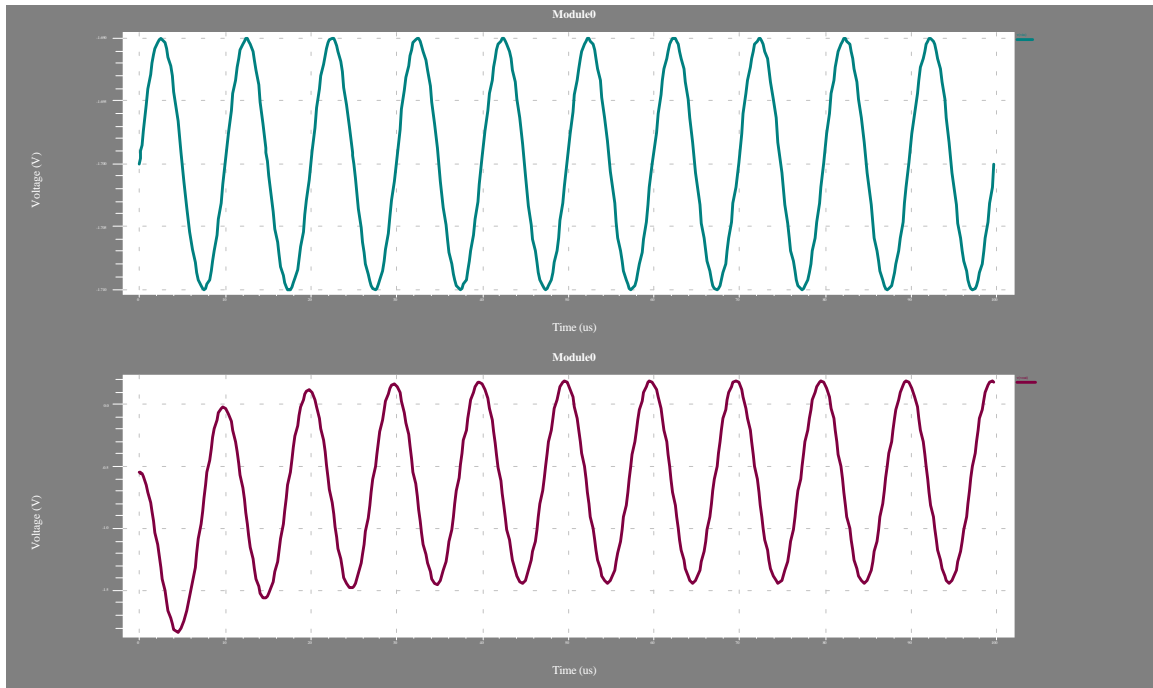


Fig. 3.19. Sinusoidal input and output for Fig.3.18.

3.5. Error Amplifier

Fig.3.20. shows an implementation of the use of negative feedback with error amp to obtain an improved common source push-pull output amplifier. Since the inverter can have reasonable gain, it is possible to use resistive feedback to replace the more complex error amplifier. The resistance R_2 should be twice R_1 so that the input signal does not have to be capable of maintaining the output signal. The resistors do not have to be carefully matched and could be polysilicon, diffusion, n- or p- well, or even transistors in the case of the MOS version. Assuming that $R_2 = 2 R_1$, the loop gain of negative feedback loop would be

$$LG \cong gm RL/ 3$$

Where gm is transconductance of M_1 or M_2 . Thus the output resistance of shunt feedback circuit is expressed as

$$R_{out}' = r_{out}/(1+ gm RL/3)$$

Where r_{out} is the resistance of output amplifier with the open loop.

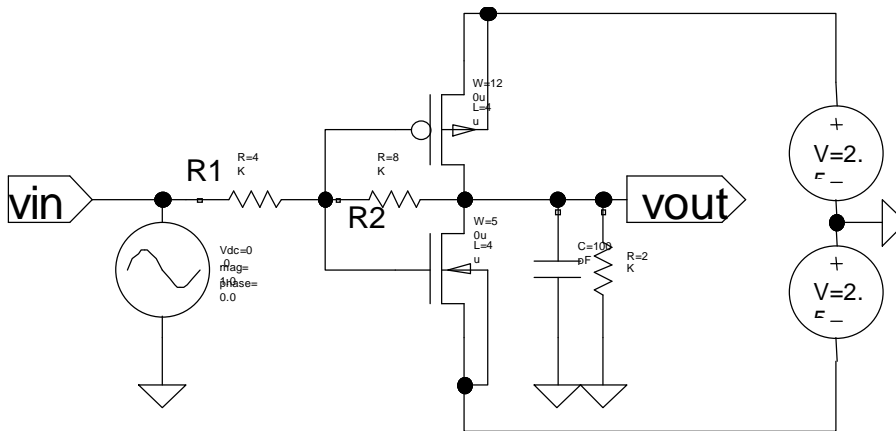


Fig. 3.20. Use of negative feedback to reduce the output resistance of the fig.3.6.

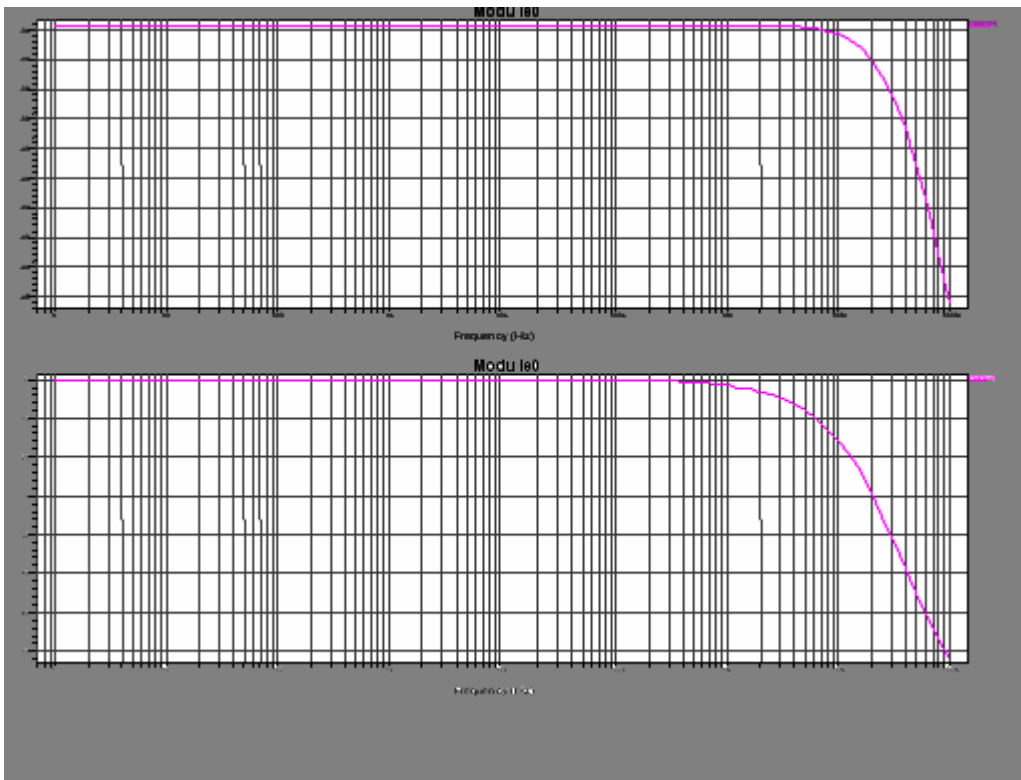


Fig.3.21. Frequency response of Error Amplifier

Taking different values of R_1 and R_2 satisfying $R_2 = 2 R_1$, we observe the gain bandwidth trade-off. Increasing the value of R_1 , the gain increases while the bandwidth decreases.

Table 2: Trade-off between dc gain and bandwidth for Fig. 3.21 with $R_2 = 2 R_1$.

R_1	R_2	Bandwidth	DC Gain
50	100	36.7 M Hz	-36 db
2K	4K	2.39M Hz	-0.7 db
4K	8K	2.2M Hz	0.27 db
10K	20K	2M Hz	1 db
20K	40K	2M Hz	1 db

3.6. Linearization Technique

In the large signal analysis of single stage and differential amplifiers, circuits usually exhibit a non-linear input/output characteristic.

In a common source, the output variation becomes heavily nonlinear as the input level increases i.e. for small input swing, the output is reasonable replica of the input but for large swings, the output exhibits saturated levels[13].

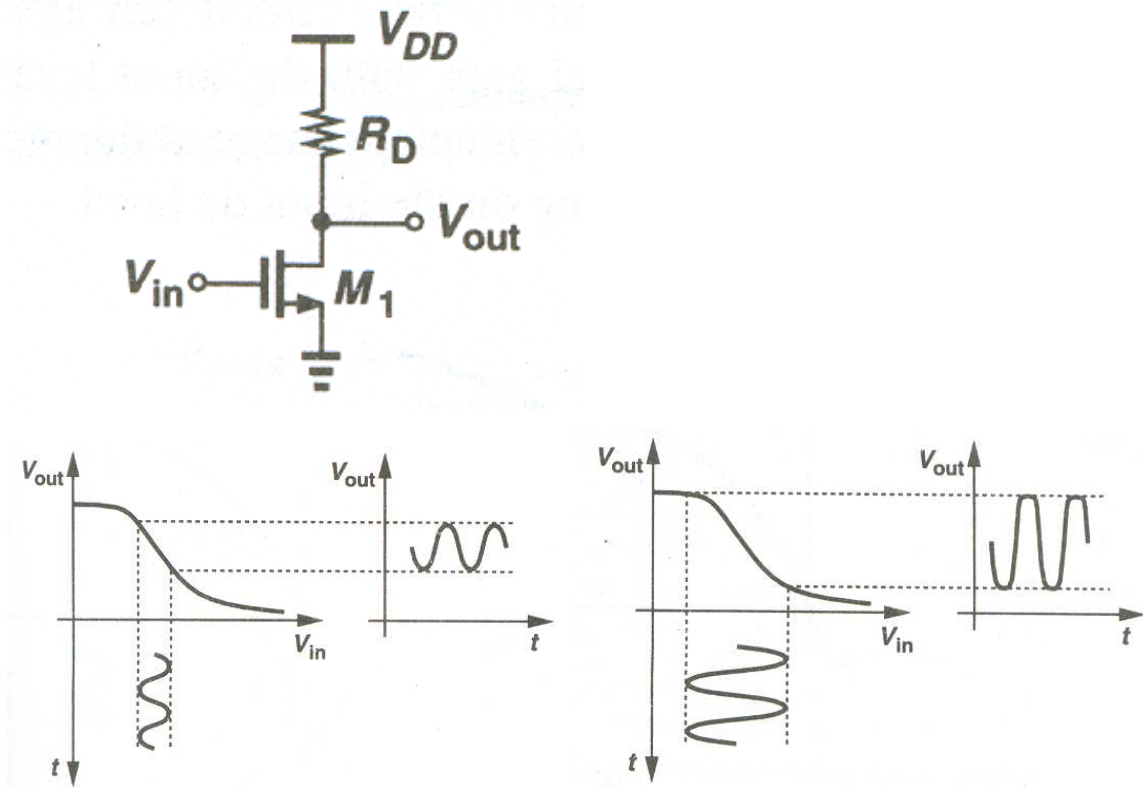


Fig.3.22. Distortion in common source stage.

While amplifiers using “global” feedback circuits can achieve a high linearity, stability and settling issues of feedback circuits limit their usage in high- speed applications. For this reason, many other techniques have been invented to linearize amplifiers with less compromise in speed.

The principle behind linearization is to reduce the dependence of the gain of the circuit upon the input level. This usually translates into making the gain relatively independent of the transistor bias currents.

The simplest linearization method is source degeneration by means of a linear resistor. For a common source stage, and revealed by the observations in the previous section, degeneration thereby reduces the signal swing applied between the gate and the source of the transistor, making the input output characteristics more linear.

From other point of view neglecting body effect, we can write the overall transconductance of the stage as,

$$G_m = g_m / (1 + g_m R_s)$$

For large $g_m R_s$, $G_m = 1/R_s$

Note that the amount of linearization depends on $g_m R_s$ rather on R_s alone. With a relatively constant G_m , $G_m R_d$ is also relatively independent of the input and amplifier is linearized.

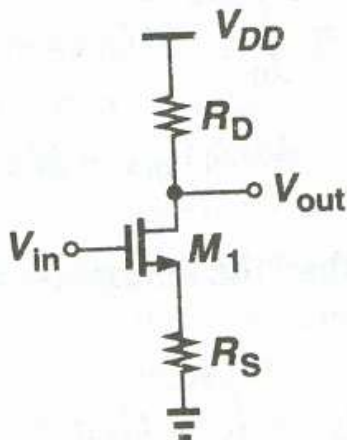


Fig. 3.23. Common source stage with degeneration

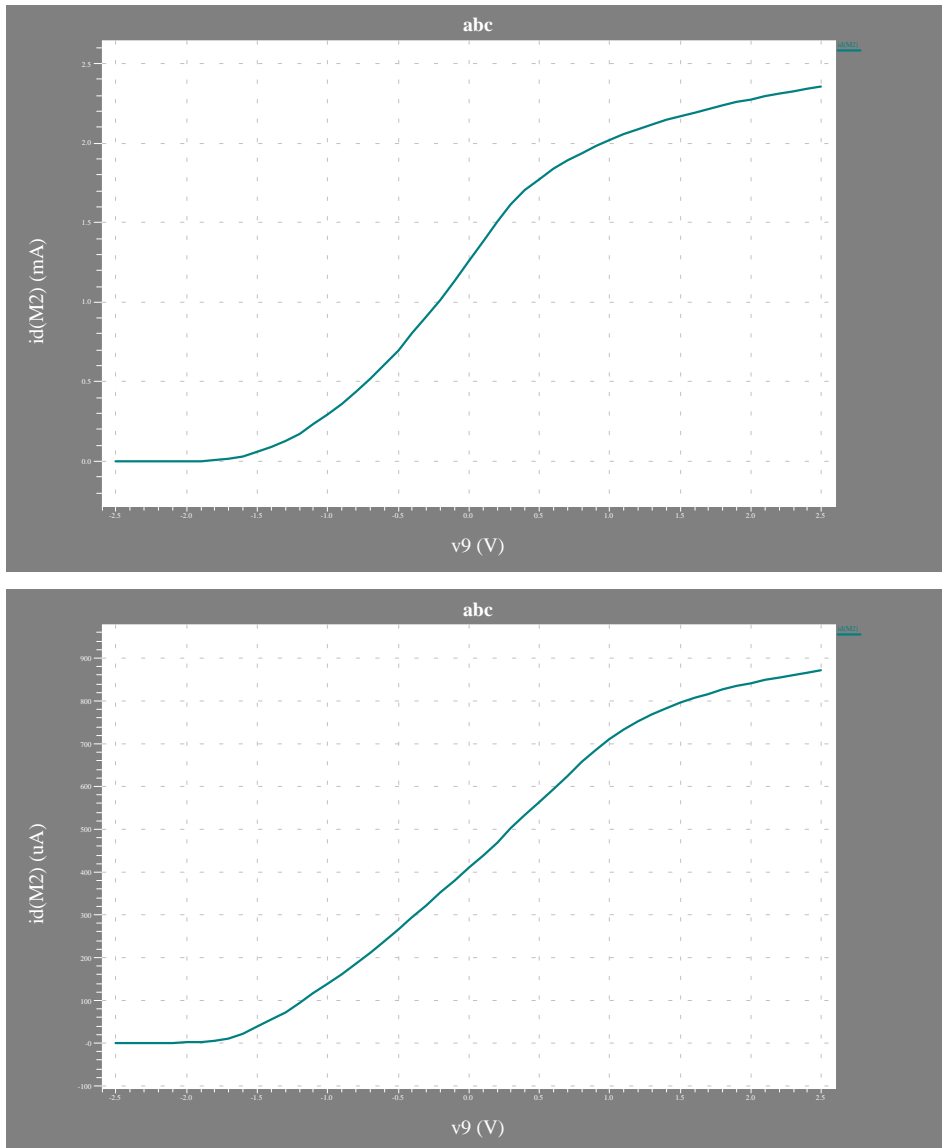


Fig.3.24: DC results of fig. 3.23, **(a)** For $R_s = 0$, $I_d(\max) = 2.5$ mA, **(b)** For $R_s = 2k$, $I_d(\max) = 840 \mu A$.

Resistive degeneration presents trade-offs between linearity, gain, noise and power dissipation. For reasonable input voltage swings, it may be quite difficult to achieve even a voltage gain of 2 in a common source stage if non-linearity is to remain below 1%.

CMOS current amplifiers with improved linearity performance of output stages and a high-drive capability are discussed in [14]

Chapter 4

Output Amplifier with Feedback

The feedback is generally employed in circuits, to stabilize the system. However, not all types of feedback has this property. There are two types of feedback: positive and negative. Negative feedback stabilizes, while the positive feedback has opposite effect.

The Feedback Equation

$$A_{CL} = A_{OL} / 1 + A_{OL} \beta \quad \dots\dots\dots(11)$$

Where, frequency dependence of A_{OL} is not shown.

A_{CL} : Closed loop gain

A_{OL} : Open loop gain

β : Feedback gain

$A_{OL}\beta$: loop gain

Note the dependence of A_{CL} on the value of A_{OL} . The value of A_{OL} becomes large (A_{OL} becomes infinity), then the value of A_{CL} approaches $1/\beta$. This illustrates the need for having a high-gain amplifier. If A_{OL} is large, then the closed loop gain becomes highly dependent on the feedback components.

4.1. Properties of negative feedback in Amplifier Design:

- Gain desensitivity
- Bandwidth extension
- Reduction in nonlinear distortion.
- Reducing the effect of noise.
- Input and output impedance control.

Gain desensitivity

Since the value of open loop gain is large, its value may change significantly with temperature, mismatch of devices, and other parameter variations. However, negative feedback desensitizes the closed loop gain from changes in open-loop.

Bandwidth Extension

Negative feedback also increases the usable bandwidth of an amplifier. Assume that an amplifier has the frequency response given by

$$A_{OLH}(s) = A_{OL} \omega_H / (s + \omega_H) \dots\dots\dots(12)$$

$A_{OLH}(s)$ is simply the high-frequency dependent version of A_{OL} and is approximated using a first-order pole at ω_H . Plugging Eq. (11) into eq.(12) yields

$$A_{CLH}(s) = A_{OLH}(s) / (1 + A_{OLH}(s) \beta) = [A_{OL} / (1 + \beta A_{OL})] / [1 + s / (1 + \beta A_{OL}) \omega_H] \dots\dots(13)$$

The eq.(13) is composed of two parts. The numerator is simply the closed-loop gain at low frequencies and the denominator reveals a pole at $(1 + \beta A_{OL}) \omega_H$. Thus, -3dB bandwidth has increased by a factor of $(1 + \beta A_{OL})$, at the cost of a proportional reduction in the gain. Figure 4.1 illustrates the bandwidth extension from using negative feedback. The original open-loop frequency response is drawn in the solid line, while the closed-loop frequency response is illustrated in the dashed line. The closed-loop response shows the decrease in the gain and at the same time an increase in bandwidth[15].

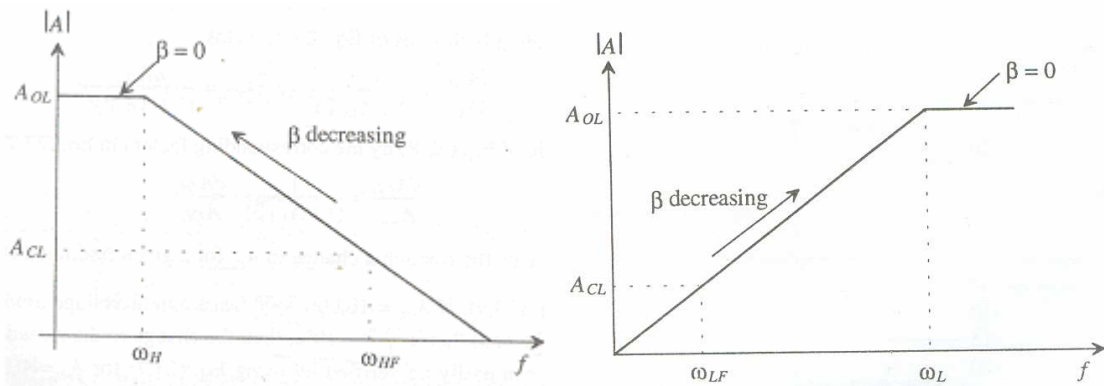


Fig. 4.1. Extension of the bandwidth (a) high-frequency pole, (b) Low frequency as a result of feedback.

Effect of negative feedback on Nonlinearity:

We know that negative feedback makes the closed-loop gain relatively independent of the open loop gain. Since nonlinearity can be viewed as the variation of small signal gain

with input level [20], we expect that negative feedback suppresses this variation as well, yielding higher linearity for the closed loop system.

A feedback circuit employing a feedforward amplifier with a finite gain suffers from gain error.

4.2. Source Followers:

Source followers are occasionally employed as level shifters or buffers, impacting the overall frequency response.

The follower configuration has both high current gain and low output resistance. Unfortunately, since the source is the output node, the MOS device is dependent on the body effect. The body effect causes the value of V_t to increase as the output voltage is increased. This creates the situation where the maximum output voltage of the n-channel source follower is considerably lower than $V_{dd} - V_t$.

One advantage of the source follower is a low small signal output resistance. This low resistance causes the ac voltage gain (and frequency response) to be less dependent on R_L .

4.3. Class A Source Follower

Fig. 4.2 Shows that, when V_{in} approaches V_{ss} , the source follower must sink external load current and $v_{out}(\min)$ will be greater than V_{ss} . The maximum value of V_{out} is given as

$$V_{out}(\max) = V_{dd} - V_{t1} - V_{on1} \cong V_{dd} - V_{t1}.$$

Assuming that V_{in} can be taken to V_{dd} ,

$$V_{t1} = V_{t0} + \gamma (V_{sb})^{1/2}$$

$$V_{out}(\max) \cong V_{dd} - \gamma_1^2/2 - V_{t01} - \gamma_1^2/2 (\gamma_1^2 + 4(V_{dd} - V_{ss} - V_{t01}))^{1/2}$$

The maximum output current sinking is determined by M_2 and maximum current sourcing is determined by M_1 and V_{in} .

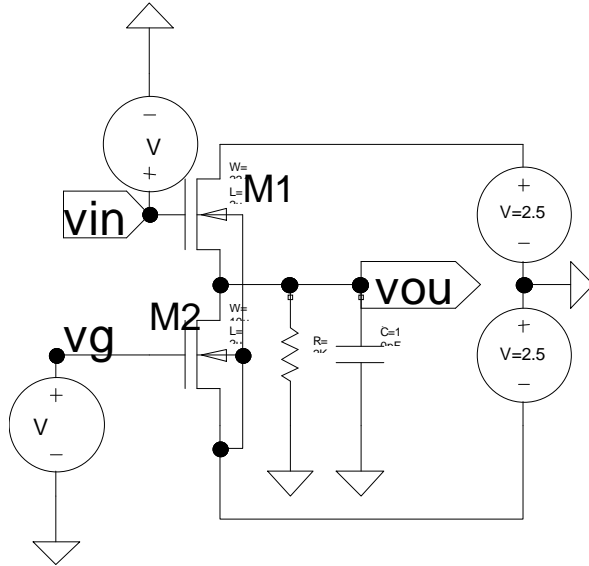


Fig. 4.2. Schematic of Class A Source Follower

4.3.1. Design Procedure:

Specifications:

Output voltage swing = ± 2 V

$V_{dd} = |V_{ss}| = 2.5$, $R_L = 2K$, $C_L = 10$ pF.

$V_g = 1$ V.

Step 1: $I = C_L * \text{Slew Rate} = 1.05$ mA.

Step 2: The aspect ratio of M2 can be found from equation given below

$$I_{out}^- = \frac{K_2 W_2}{2L_2} (V_g - V_{ss} - V_{t2})^2$$

$$(W_2/L_2) = 16 / 2$$

Step 2: The aspect ratio of M1 can be found from following equation, taking $V_{t1} = V_{t0}$.

$$I_{out}^+ = \frac{K_1 W_1}{2L_1} [V_{dd} - V_{out} - V_{t1}]^2 - I_{D2}$$

$$(W/L)_1 = 58/2$$

Step 3: Iterate again for the value of V_{t1} with eq. given below:

$$V_{t1} = V_{t0} + \gamma (V_{sb} + |2\phi|)^{1/2} - |2\phi|^{1/2}$$

4.3.2. Simulation Results

The simulation results of Class A source follower are given as:

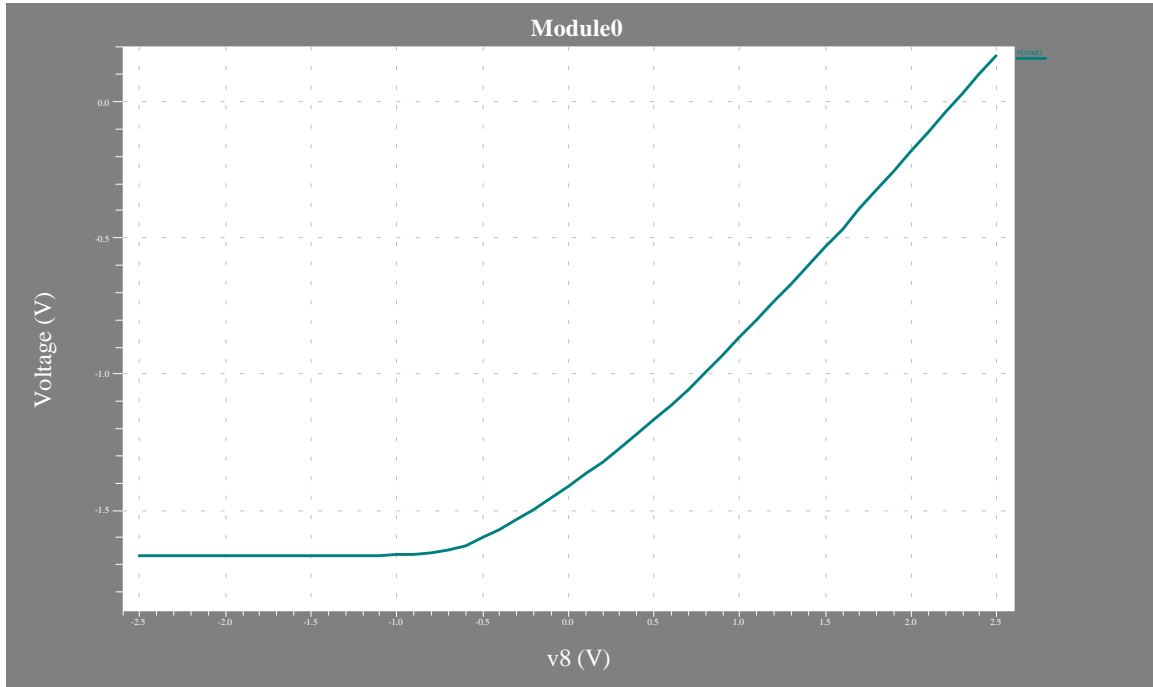


Fig. 4.3. Output voltage of fig 4.2. for variation in input.

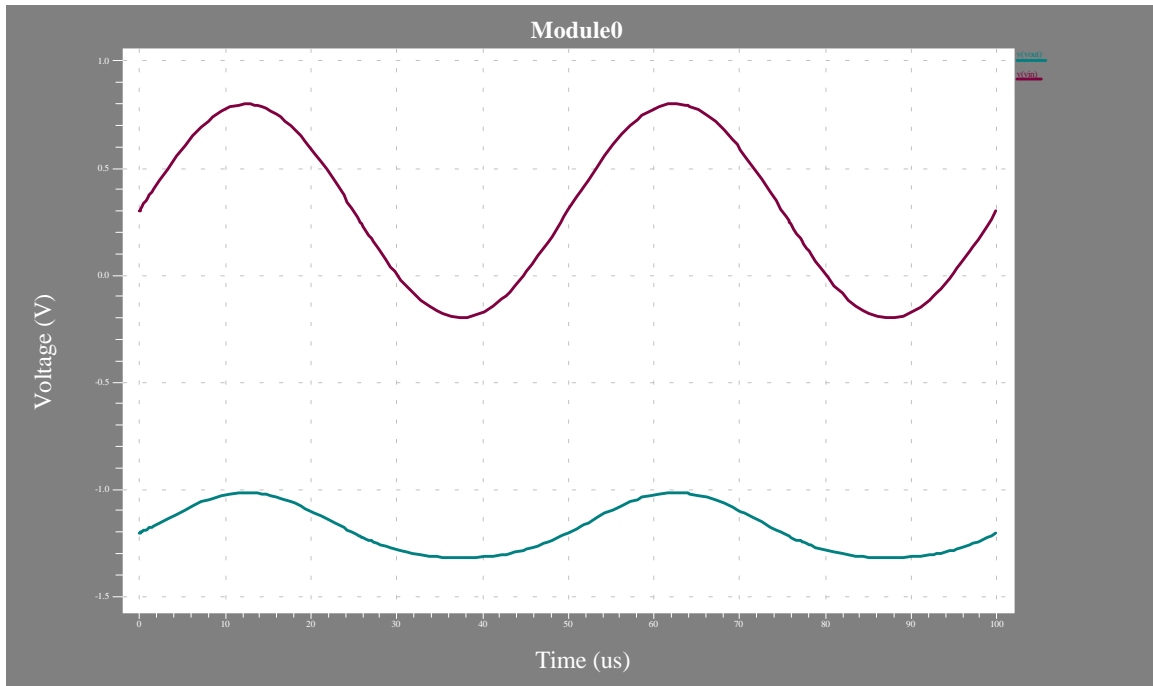


Fig. 4.4. Sinusoidal input and output for fig. 4.2.

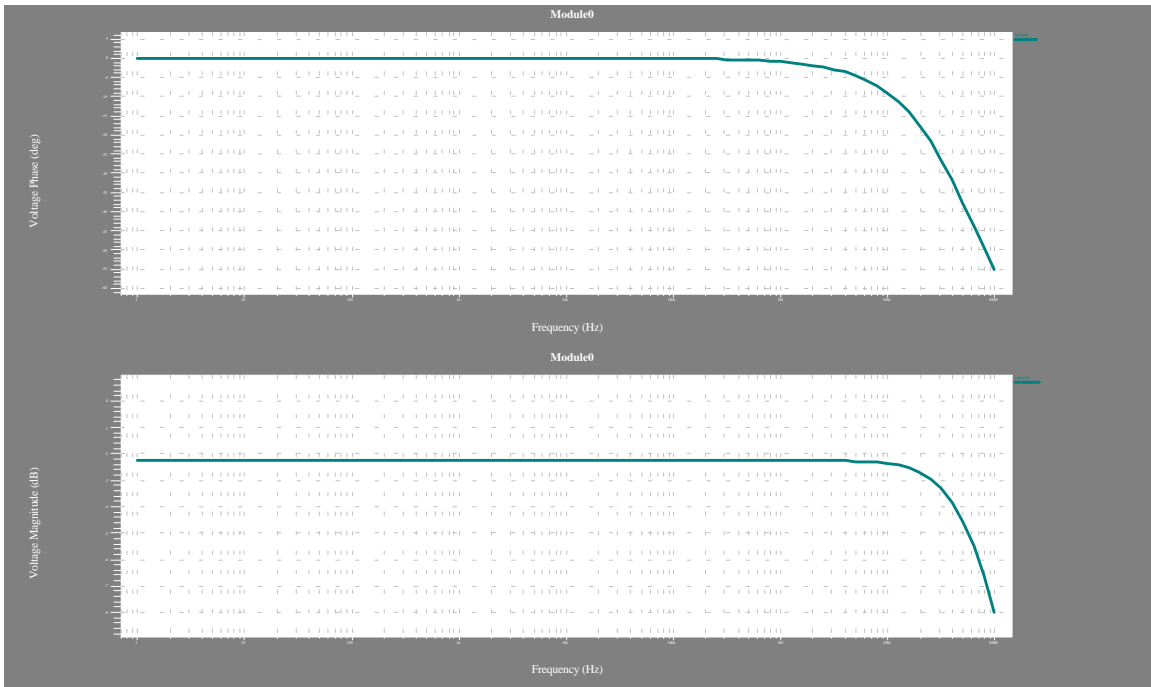


Fig. 4.5. AC Analysis of fig. 4.2.

THD = 2.92 %

Efficiency = 8.6%

4.3. Class AB source follower

The schematic of Class AB source follower is shown in fig. below.

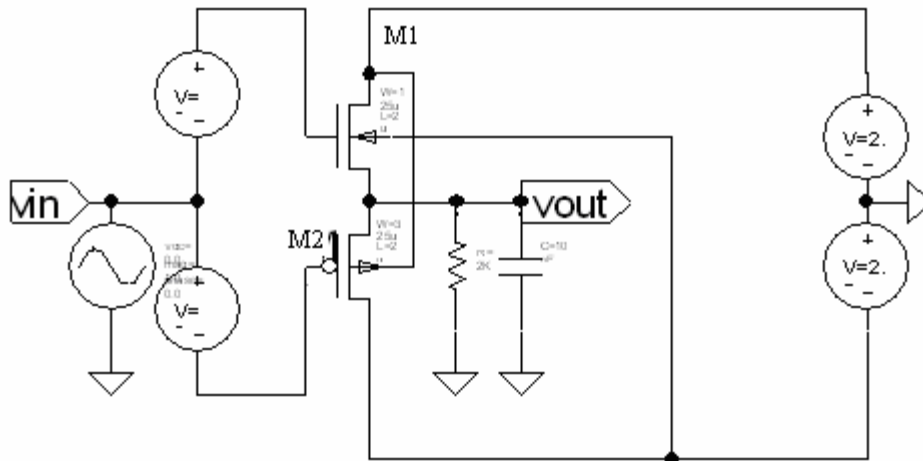


Fig. 4.6. Schematic of Class AB source follower

Here the battery $V_b = 2.5$ V and the circuit is operating in Class AB.

4.3.1. Design Procedure:

Specifications:

Output voltage swing = ± 2 V

$V_{dd} = |V_{ss}| = 2.5$, $R_L = 2K$, $C_L = 10$ pF.

Step 1: The aspect ratio of M1 is calculated with eq. given below:

$$I_{bias} = u_n C_{ox} (W/L)_1 (V_{dd} + V_b - V_{out} - V_t)^2 / 2$$

Initially assume, $V_t = V_{t0}$, $(W/L)_1 = 20/4$,

Step 2: The aspect ratio of M2 is calculated with eq. below:

$$(W/L)_1 = u_p / u_n (W/L)_2,$$

$$(W/L)_2 = 48 / 4$$

Step 3: Apply iterations for V_t with the eq. given below:

$$V_t = V_{t0} - \gamma ((\phi - V_{sb})^{1/2} - \phi^{1/2})$$

4.3.2. Simulation Results:

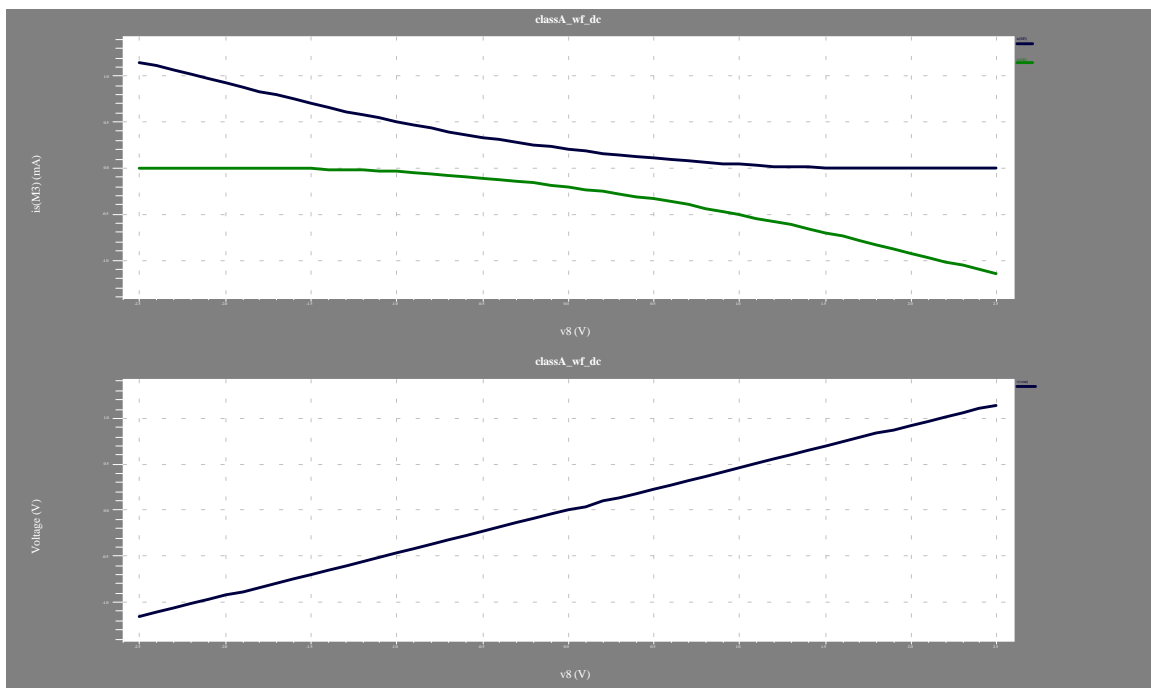


Fig.4.7. Output voltage and current characteristics for the push-pull Class AB Source Follower.

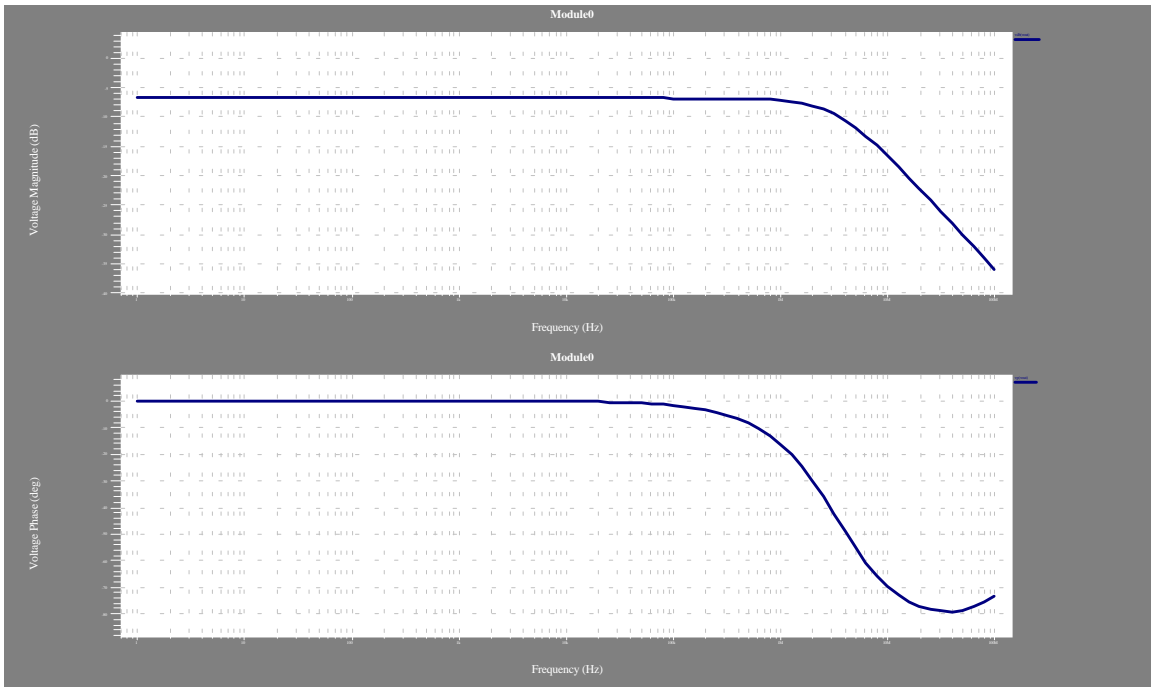


Fig. 4.8. AC Analysis of Class AB Source AB follower Stage

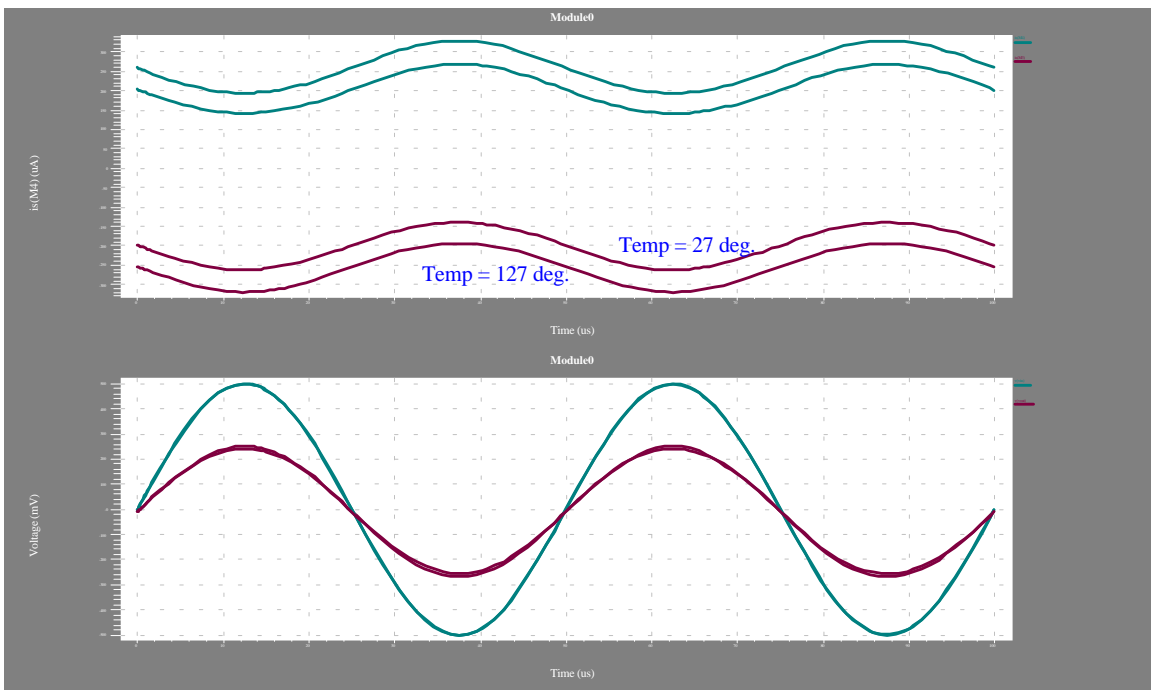


Fig. 4.9. Sinusoidal Analysis of Class AB Source Follower Stage

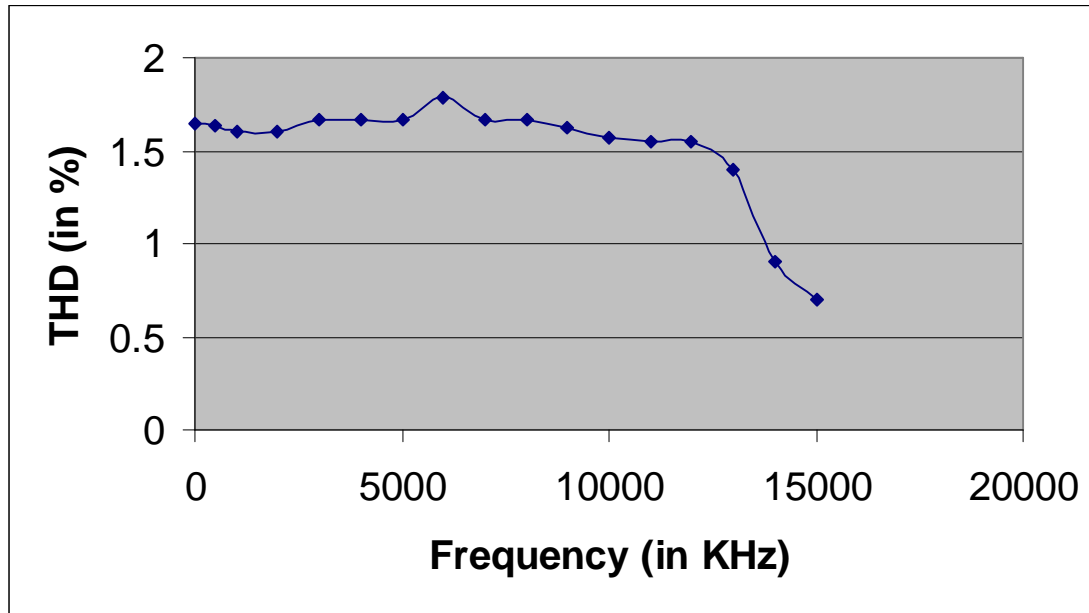


Fig. 4.10. THD variation of Class AB Source Follower with change in frequency.

Efficiency = 1.59%

The asymmetric class-AB output stage [7] is simpler than the asymmetric class AB output stage, but, due to its asymmetric topology, a lower linearity performance is expected. The THD in the symmetric class AB output stage is better than the THD of the asymmetric class AB output stage[10].

4.4. Class B Source Follower

The circuit for Class B source follower is shown in fig. 4.11.

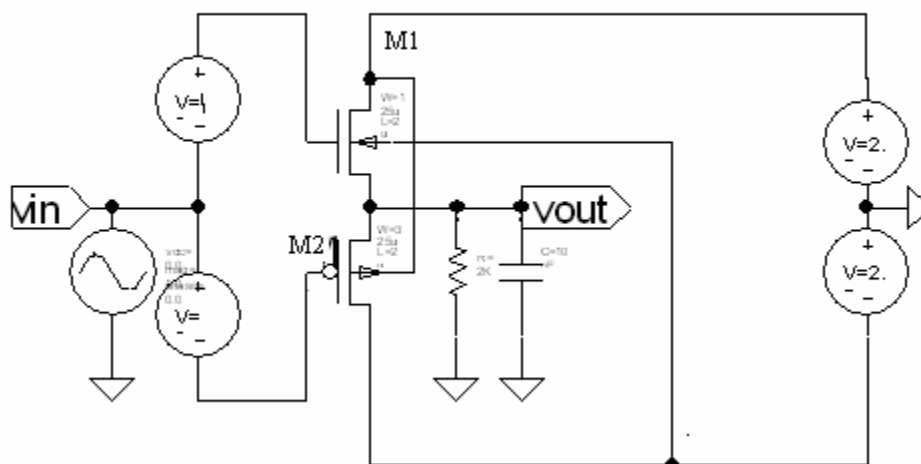


Fig.4.11. Schematic of Class B source follower.

4.4.1. Design Procedure:

Specifications:

Output voltage swing = ± 2 V

$V_{dd} = |V_{ss}| = 2.5$, $R_L = 2K$, $C_L = 10$ pF.

Step 1: The aspect ratio of M1 is calculated with eq. given below:

$$I_{bias} = u_n C_{ox} (W/L)_1 (V_{dd} + V_b - V_{out} - V_t)^2 / 2$$

Initially assume, $V_t = V_{t0}$, $(W/L)_1 = 20/4$,

Step 2: The aspect ratio of M2 is calculated with eq. below:

$$(W/L)_1 = u_p / u_n (W/L)_2,$$

$$(W/L)_2 = 48/4$$

Step 3: Apply iterations for V_t with the eq. given below:

$$V_t = V_{t0} - \gamma ((\phi - V_{sb})^{1/2} - \phi^{1/2})$$

4.4.2. Simulation Results:

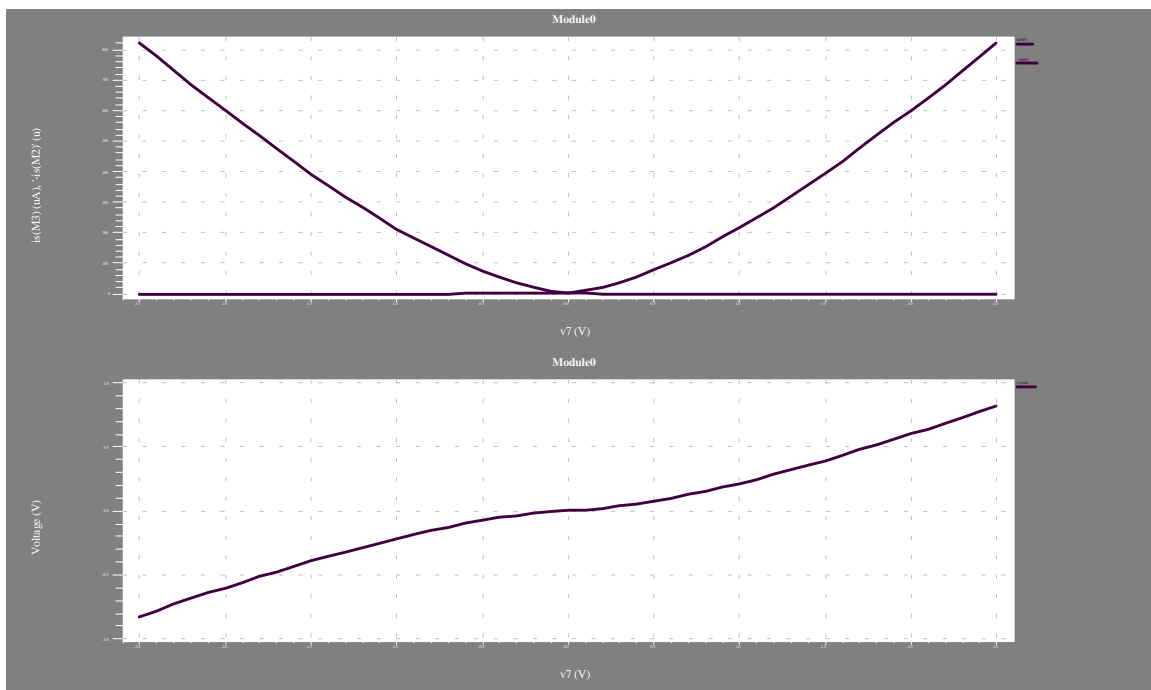


Fig.4.12. Output voltage and current characteristics for the Source follower Class B amplifier.

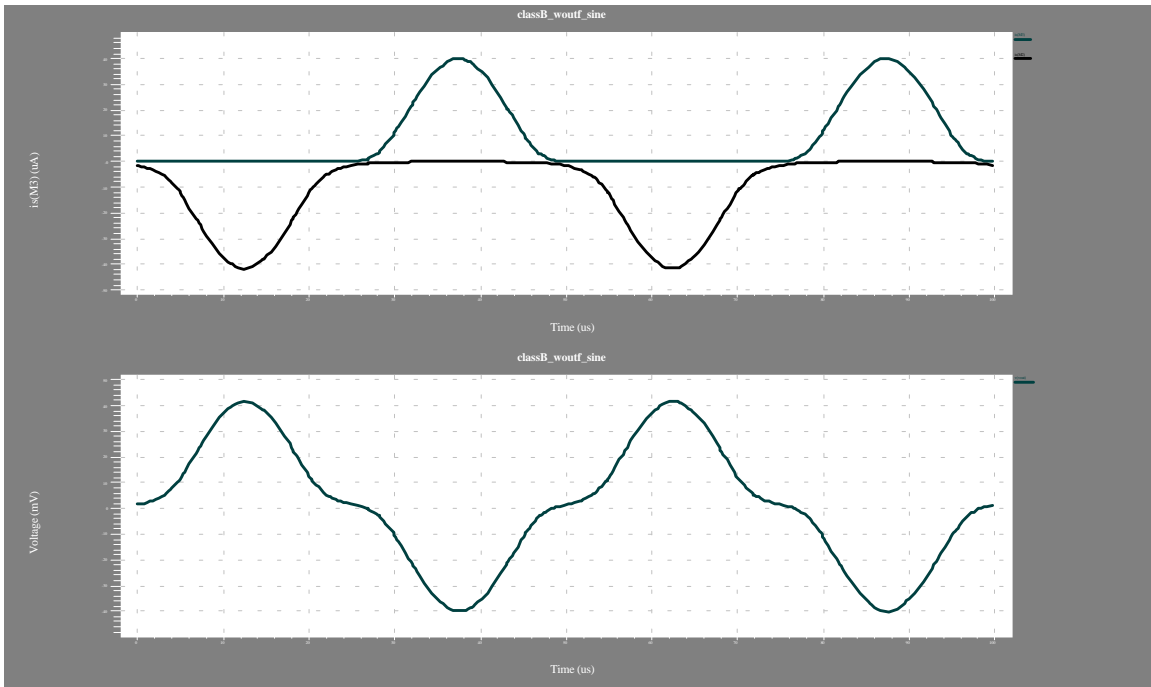


Fig.4.13. Sinusoidal Input and output voltage for fig. 4.11.

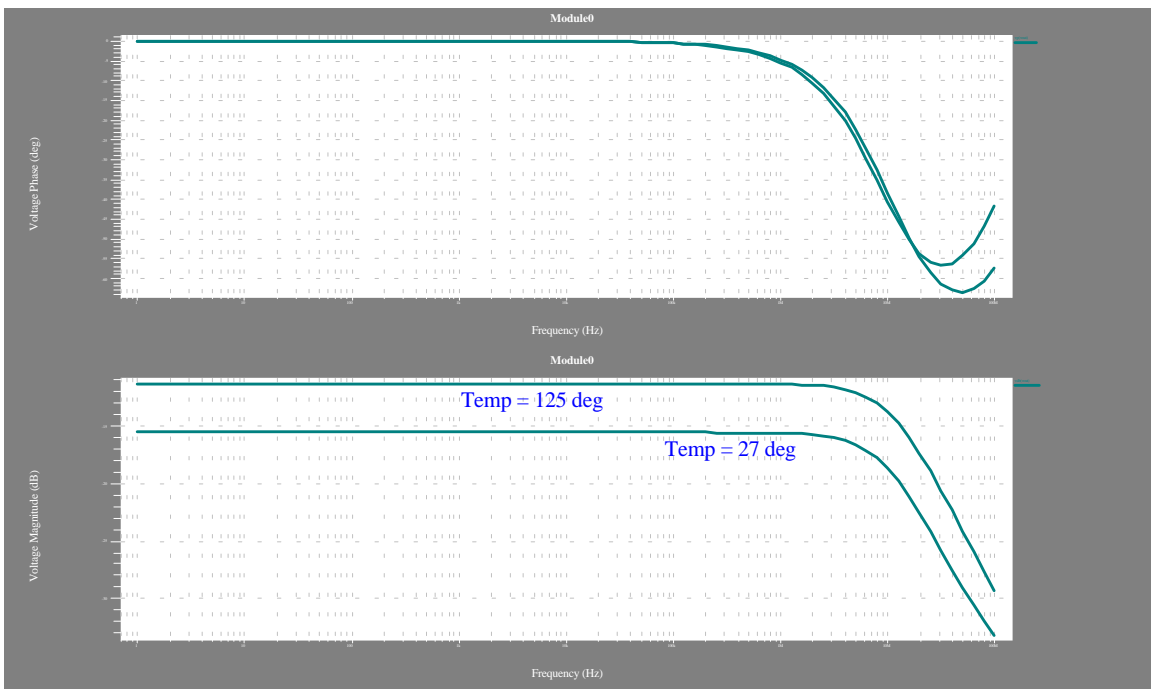


Fig.4.14. AC Analysis of fig. 4.11.

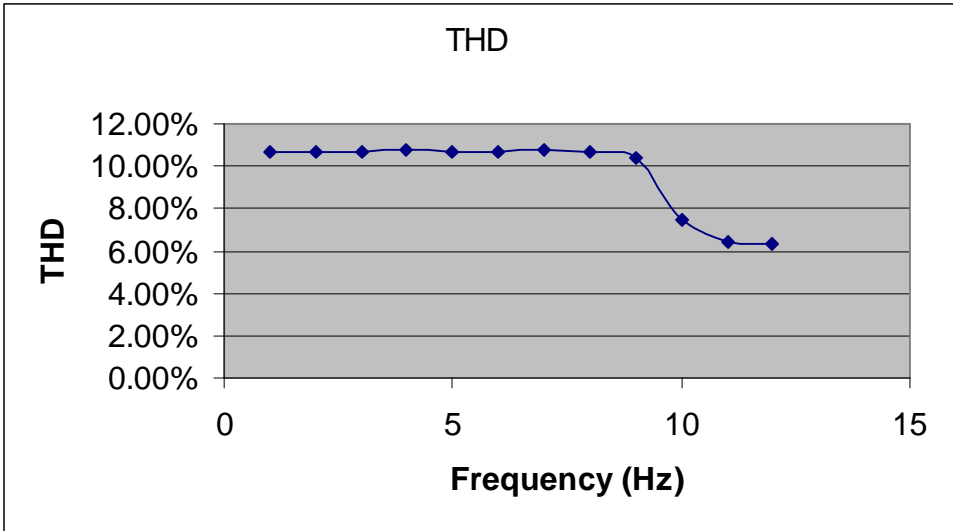


Fig.4.15. THD variation with variation in frequency for $v_{in} = 0.5$

Chapter 5

Differential Amplifiers

The differential amplifier is one of the more versatile circuits in analog circuit design. It serves as input stage to most op-amps. The differential amplifiers should have high output swings and high rejection of supply noise.

The differential-mode input voltage, V_{id} , of differential amplifier is defined as the difference between v_{in1} and v_{in2} . This voltage is defined between two terminals, neither of which is ground. The common mode input voltage V_{ic} is the average value of v_{in1} and v_{in2} .

The output voltage of differential amplifiers is expressed as:

$$\mathbf{V_{out} = A_{vd} V_{id} + A_{vc} (v_{in1} + v_{in2})/2}$$

Differential in single ended output Transconductance can be shown as

$$g_m = \delta I_d / \delta v_{id} |_{v_{id}=0} = (K' I_{d1} W_1 / 2L_1)^{1/2}$$

$$\begin{aligned} \text{Differential Out Transconductance } g_{ds} &= \delta I_{od} / \delta v_{id} |_{v_{id}=0} \\ &= (2K' I_{d1} W_1 / 2L_1)^{1/2} \end{aligned}$$

The output voltage of the differential amplifier depends on how the active loads are implemented.

$$\text{Gain of a differential Stage} = \text{Output Swing} / V_{id} = g_m / g_{ds} = g_m * R_{out}$$

5.1. Differential Amplifier With Resistive Load:

Fig. 5.1. displays a resistor-loaded, differential amplifier used in high speed applications. The resistors are often realized within a reasonably small area using unsilicided polysilicon, and introduce less capacitance than other loads such as triode PMOS devices or diode-connected NMOS devices. Further increases in bandwidth can be achieved at the expense of chip area by introducing inductors into the loads [2].

The maximum and minimum output levels in this case are V_{dd} and $V_{dd} - R_d \cdot I_{ss}$ resp. independent of the input CM level.

The small signal gain is maximum for $v_{in1} = v_{in2}$, gradually falling to zero as $|v_{in1} - v_{in2}|$ increases i.e. the circuit becomes more non-linear as the input voltage swing increases.

V_{CM} is bounded as follows:

$$V_{gs1} + (V_{gs3} - V_{th3}) \leq V_{in, CM} \leq \min [(V_{dd} - R_d \cdot I_{ss} / 2 + V_{th}), V_{dd}]$$

$$V_{out1} - V_{out2} = R_d \cdot \Delta I$$

i.e. $A_v = -G_m \cdot R_d$

$$|A_v| = g_m \left(R \parallel \frac{1}{g_{ds}} \right) \Rightarrow g_m = |A_v| / R + |A_v| g_{ds}$$

Under equilibrium condition, $|A_v| = (\beta I_{ss})^{1/2} \cdot R_d$

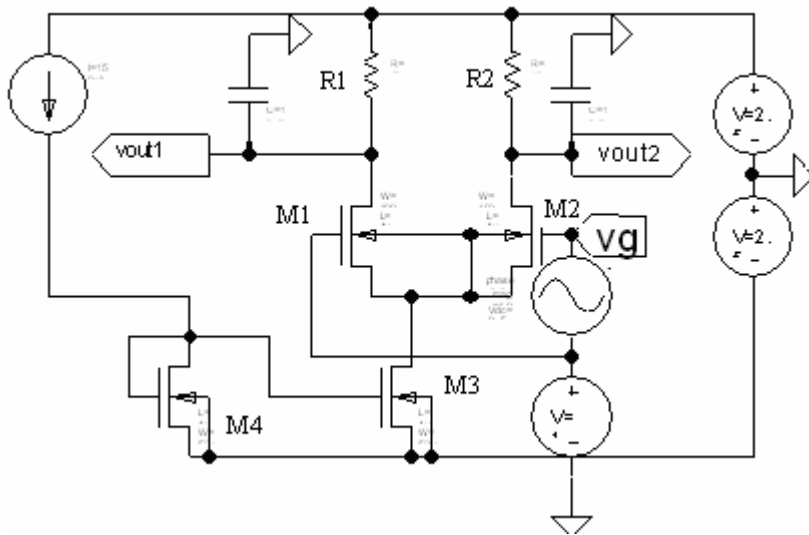


Fig. 5.1. Schematic of differential amplifier with resistive load

The aspect ratios of the transistors are as follows:

$$(W/L)_1 = (W/L)_2 = 52/4$$

$$(W/L)_4 = (W/L)_3 = 100/4$$

$$R1 = R2 = 10K\Omega$$

$$C1 = C2 = 10 \text{ pF}$$

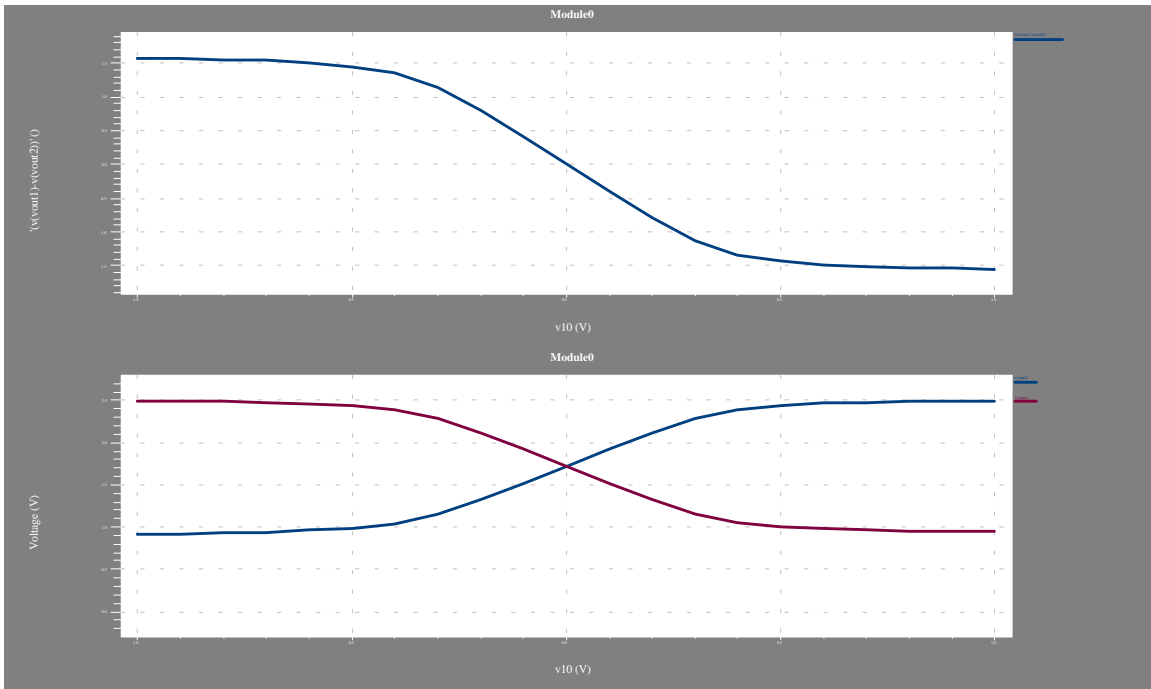


Fig. 5.2. Plot showing variations of (a) Drain currents in M1 and M2, (b) $(v_{out1} - v_{out2})$ as a function of $(V_{in1} - V_{in2})$

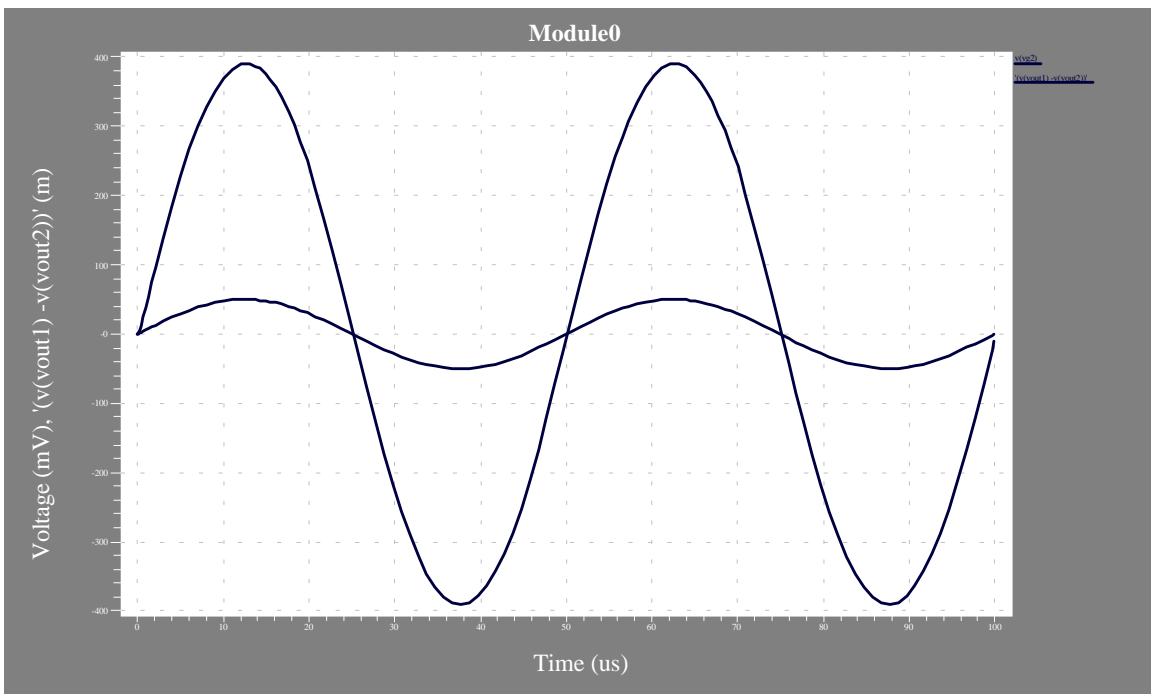


Fig. 5.3. Sinusoidal input and output voltage for Fig. 5.1.

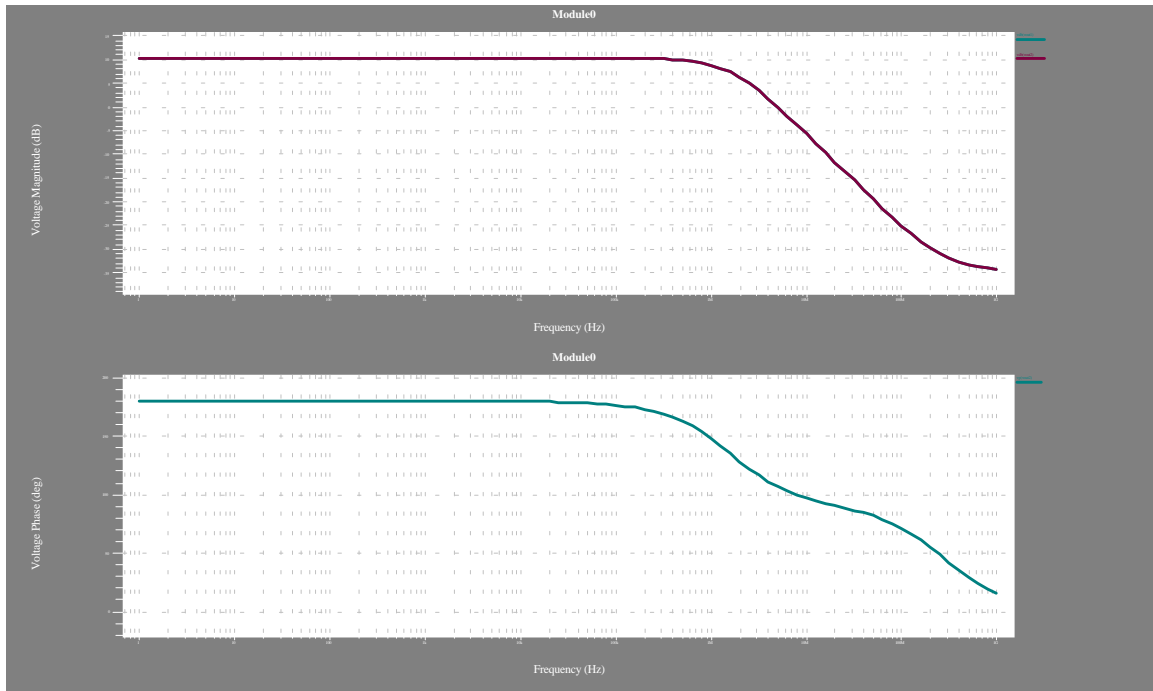


Fig. 5.4. AC Analysis of Fig. 5.1.

5.2. Differential Amplifier with Current-Mirror Load

The advantage of this configuration is that the differential output signal is converted to a single ended output signal with no extra component required. In this circuit, the output voltage or current is taken from the drains of M2 or M4.

Operation:

If a differential voltage V_{id} , is applied between the gates ($V_{id}/2$), then the half is applied to the gate-source of M1 and half to the gate source of M2. The result is to increase I_{d1} & decrease I_{d2} by equal increments ΔI . The ΔI increase I_{d1} is mirrored through M3- M4 as an increase in I_{d4} of ΔI . As a consequence of the ΔI increase in I_{d4} and ΔI decrease in I_{d2} , the output must sink a current of $2 \cdot \Delta I$. Therefore the transconductance of this circuit is equal to the single transistor. The small signal analysis of this is as follows :

The differential- in- differential-out gain =

$$A_{vdd} = \frac{1}{2} * (g_{m1} + g_{m1} \cdot g_{m4} / (g_{ds1} + g_{m3} + g_{ds3})) (1 / (g_{ds2} + g_{ds4}))$$

If M3 and M4 are matched then $g_{m3} = g_{m4}$, since $g_{m3} \gg$ either g_{ds1} or g_{ds3}

Therefore $A_{vdd} \approx g_{m1} / (g_{ds2} + g_{ds4})$

$$= 2(K' W_1) / (\lambda_2 + \lambda_4) (I_{ss}, L_1).$$

$$R_{out} = 1 / (g_{ds2} + g_{ds4}) = 1 / (\lambda_2 + \lambda_4) I_{ss} \approx 1 / \lambda I_{ss}.$$

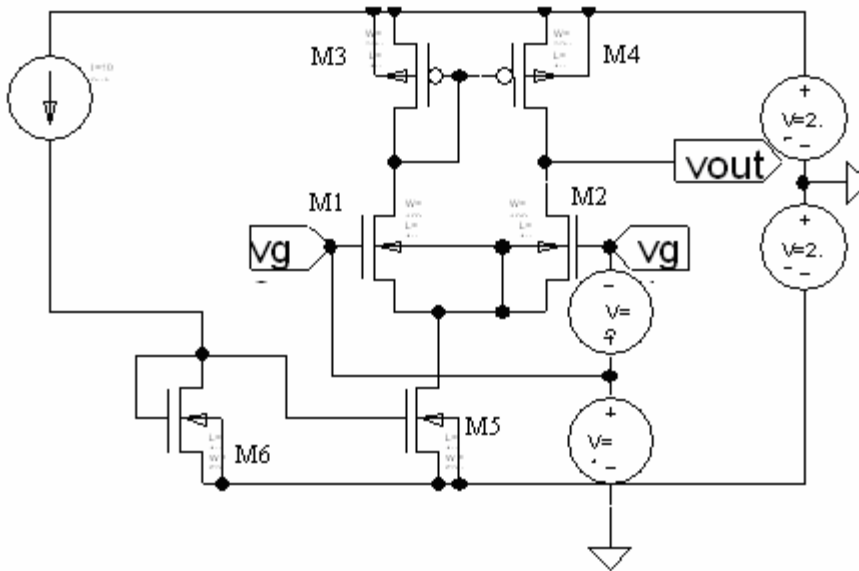


Fig. 5.5. Differential Amplifier with current source load.

The schematic of differential amplifier with current mirror load is shown in Fig. 5.4. The specifications and design equation for this amplifier is given in section 5.2.1.

5.2.1. Design Procedure:

Specifications:

Slew Rate ≥ 10 v/us, -3db Bandwidth ≥ 100 KHz,

$A_v = 100$ db ,

ICMR ≤ 2 V and ICMR ≥ -1.5 V,

$P_{diss} \leq 1$ mW.

Equations Used:

$$V_{ic}(\max) = V_{g1}(\max) = V_{dd} - V_{sg3} + V_{tn,1} \dots\dots\dots(1)$$

$$V_{ic}(\min) = V_{ss} + V_{ds5}(\text{sat}) + V_{gs2} \dots\dots\dots(2)$$

$$SR = I_5 / C_L \dots\dots\dots(3)$$

$$A_v = g_{m1} \cdot R_{out} \dots\dots\dots(4)$$

$$R_{out} = 1 / (g_{ds2} + g_{ds4})$$

$$A_v = V_{out} / V_{idd} = g_{md} / (g_{ds2} + g_{ds4}) = 2 * (K_1 * W_1)^{1/2} / (\Delta 2 + \Delta 4) * (I_{ss} \cdot L_1)^{1/2}$$

$$P_{diss} = (V_{dd} + |V_{ss}|) * I_5 \dots\dots\dots(5)$$

$$W_{-3db} = 1 / R_{out} \cdot C_L \dots\dots\dots(6)$$

Calculation Of Aspect Ratios:

Step 1: Using eq. (3) , $I_5 \geq 100\mu A$ and with eq (5), $I_5 \leq 200\mu A$.

Step 2: Using eq (6), $R_{out} \leq 159 K$ and $(W/L)_1 = (W/L)_2 = 25$.

Step 3: Using eq. (1), $(W/L)_3 = (W/L)_4 = 9.5$

Step 4: Using eq (2), V_{ds5} is calculated and then using current Equation of M_5 , $(W/L)_5 = 30$ is calculated.

Step 5: Iterate accordingly.

5.2.2. Simulation Results:

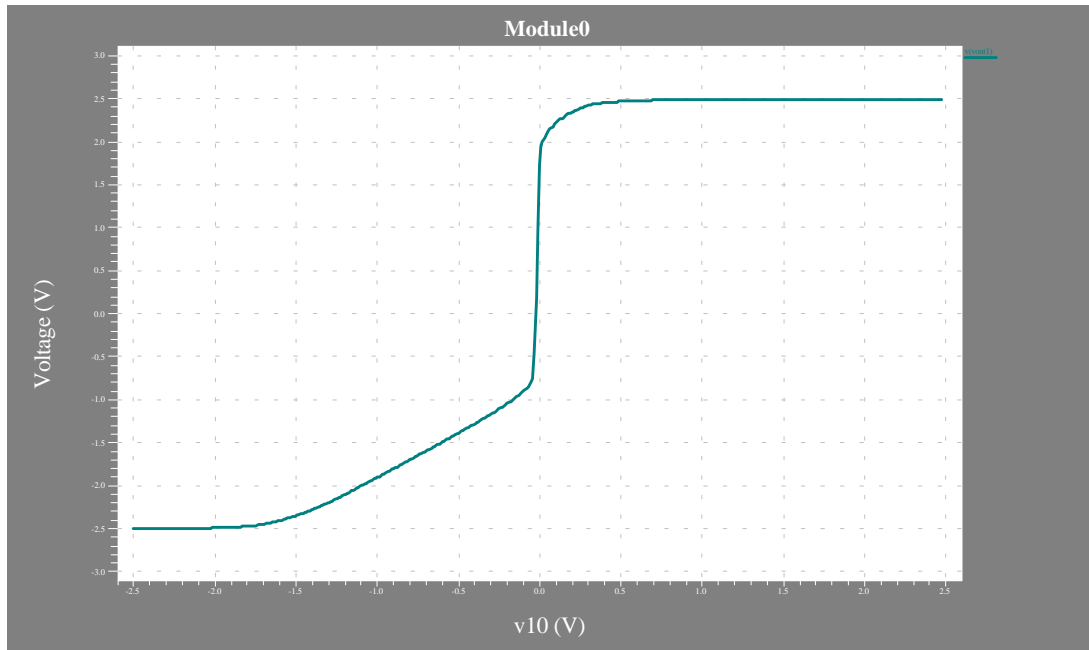


Fig. 5.6. Output Voltage Vs Differential Input Voltage

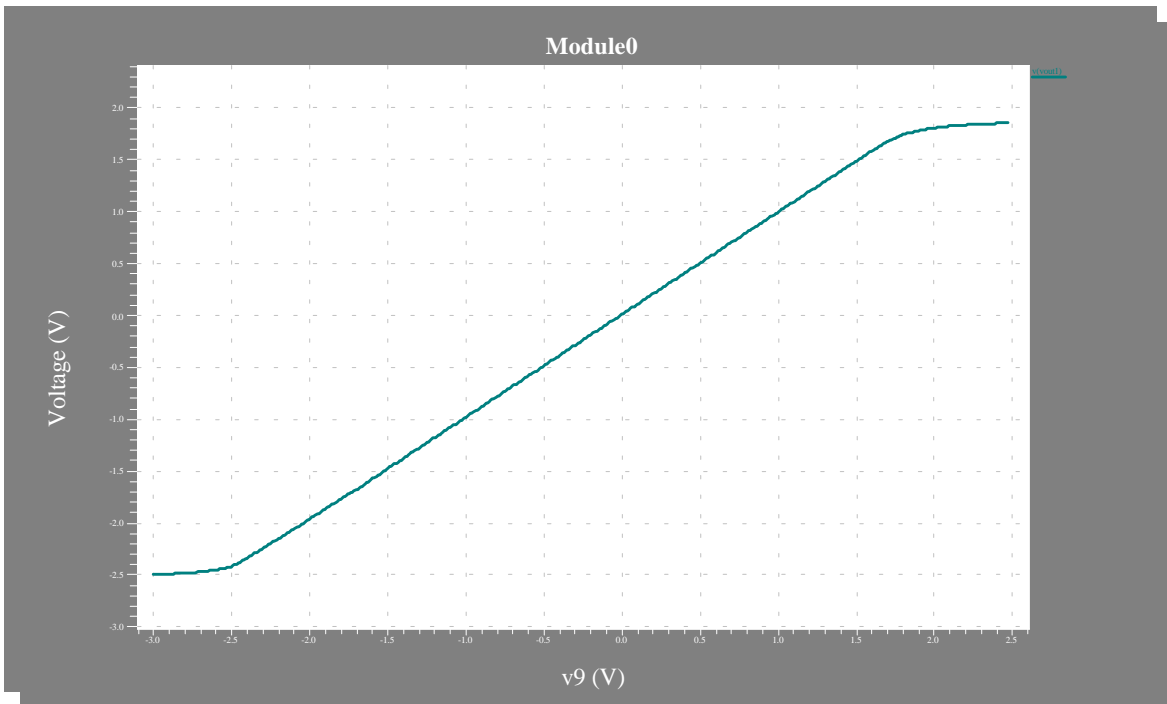


Fig. 5.7. Plot for Of CMIR

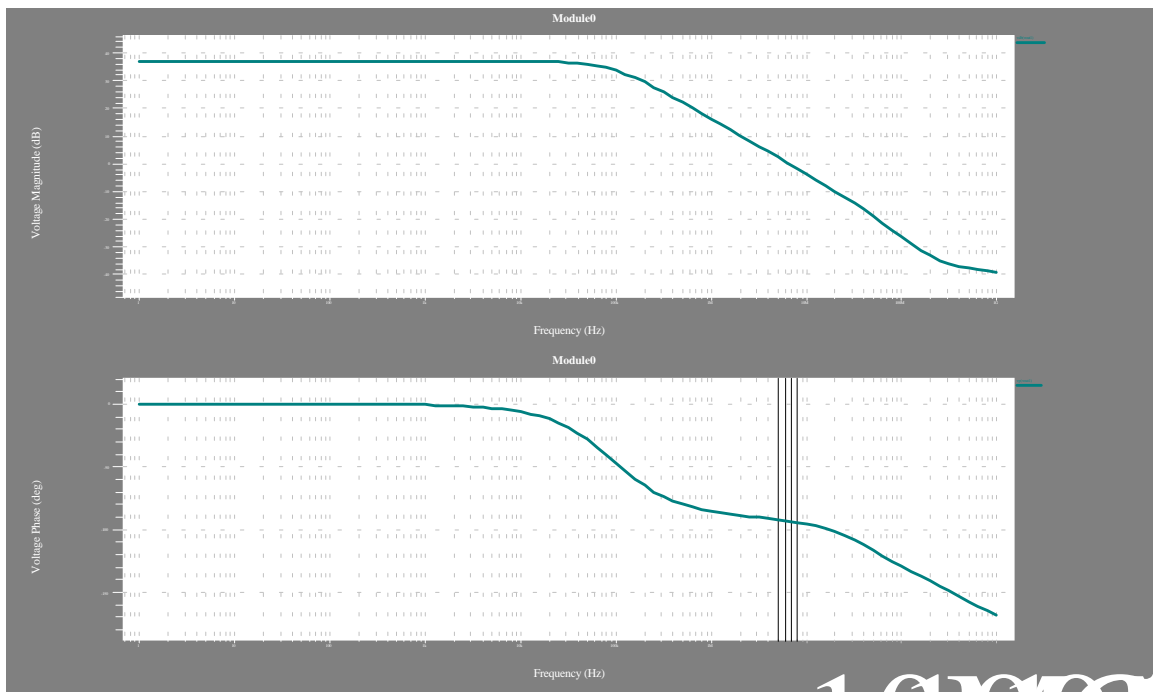


Fig. 5.8. Gain vs Frequency and phase vs Frequency plot

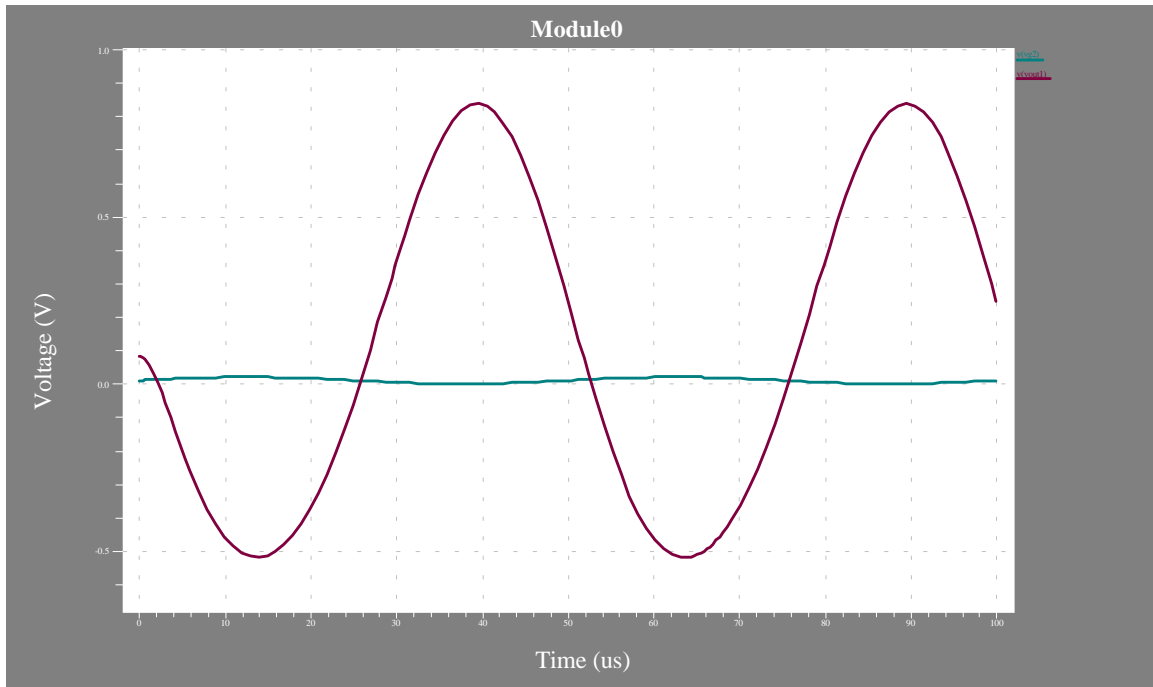


Fig. 5.9 Sinusoidal input and output plot for Fig. 5.5.

Results:

For VCC =2.5,

DC Gain =37db

CMRR = -2.3 to 1.7

BW =100k

PM = Phase Margin=90

Output Swing =-2.5 to 2.5

5.3. Differential Amp with NMOS enhancement Load:

The single ended output voltages V_{d1} and V_{d2} are given as

$$V_{d1} = V_{dd} - V_{t1} - (2 I_{d1} / (K_3 \beta_3))^{1/2} \quad V_{d1} = V_{dd} - V_{t4} - (2 I_{d2} / (K_4 \beta_4))^{1/2}$$

$$\text{Differential in single ended output gain} = -1/2 * (\beta_1 / \beta_3)^{1/2}$$

$$\text{Differential voltage gain } (A_{vdd}) = -g_{m1} / g_{m3} .$$

$$R_{id} = \text{Infinite}$$

$$\text{The single-ended output resistance } (R_{out1}) = 1 / (g_{m3} + g_{ds1} + g_{ds3}) \approx 1/g_{m3}$$

$$\text{And } Rout2 = 1 / (g_{m4} + g_{ds2} + g_{ds4}) \approx 1/g_{m4}$$

Differential output resistance $R_{od} = R_{out1} + R_{out2} \approx 1/g_{m3} + 1/g_{m4} \approx 2/g_{m3}$

The voltage gain of the enhancement Nmos load differential amplifier can be increased using current source loads.

5.4. Differential Amplifier With Current Source Load

This configuration has advantage of a larger input common mode range voltage because M3 is no longer in diode configuration. The differential in differential out ($v_{out1}-v_{out2}$) small signal voltage gain is the same as that of differential amplifier with current mirror load. If the voltage is taken at with current mirror load. If the voltage is taken at with current mirror load. If the voltage is taken at v_3 or v_4 , the small signal voltage gain is half that of differential amplifier with current mirror load.

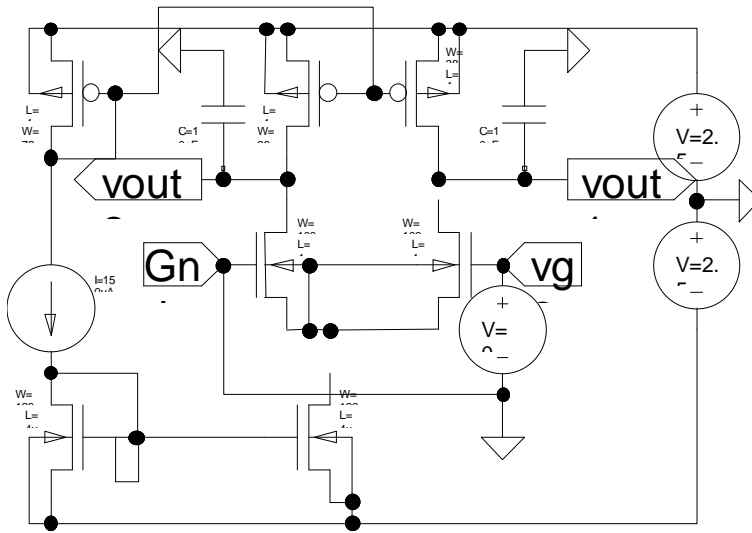


Fig. 5.9. Differential amplifier with current source load.

The I_{bias} defines the currents in M3 and M4, as well as the current in M5. It is likely that these currents will not be exactly equal. If a dc current flows through both PMOS and a NMOS transistors, the transistor with a larger dc current will become active. The only way to match these currents. The only way to do this is to leave the saturation region. So, if I_3 is greater than I_1 , then M1 is saturated & M3 is active and vice-versa

When the currents are not balanced, the outputs of the differential amplifier will decrease or increase. Therefore if a common-mode feedback scheme, we will be able to stabilize the common mode output voltages of the differential amplifier while allowing the differential mode output voltage to be determined by differential input to the amplifier.

The single ended gain A_{vds1} , A_{vds2} and differential gain A_{vdd} are summarized as follows.

$$A_{vds1} = A_{v1} = V_{d1} / V_{id} = -g_{m1} / 2(g_{ds1} + g_{ds3})$$

$$A_{vds2} = A_{v2} = V_{d2} / V_{id} = g_{m1} / 2 (g_{ds2} + g_{ds4})$$

$$A_{vdd} = V_{od} / V_{id} = -g_{m1} / 2(g_{ds1} + g_{ds3}) = -g_{m2} / 2(g_{ds2} + g_{ds4})$$

$$R_{out1} = 1 / (g_{ds1} + g_{ds3})$$

$$R_{out2} = 1 / (g_{ds2} + g_{ds4})$$

$$\text{and } R_{od} \approx 2 / (g_{ds1} + g_{ds3})$$

5.5. Nonlinearity Of Differential Circuits:

Differential circuits exhibits an “odd-symmetric” input/output characteristic, i.e. $f(-x) = -f(x)$.

Therefore, it can be shown that,

$$Y(t) = \alpha_1 x(t) + \alpha_3 x(t)^3 + \alpha_5 x(t)^5 + \dots$$

This indicates that a differential signal produces no even harmonics.

From large signal analysis, we can find that,

For single ended common source amplifier,

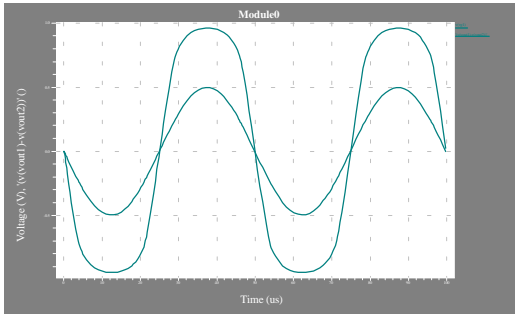
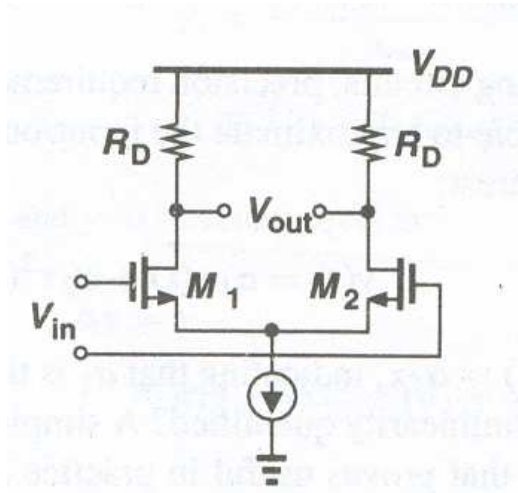
$$A_{HD2} / A_F = V_m / 4(V_{gs} - V_{th}) \dots\dots\dots(1)$$

For differential amplifier,

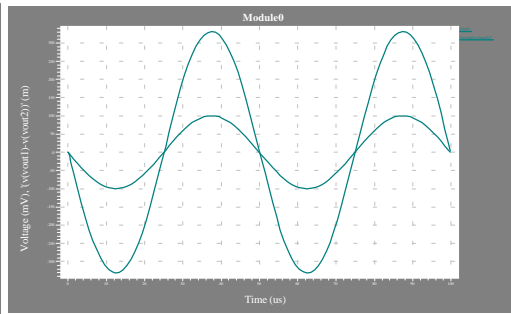
$$A_{HD3} / A_F = V_m / 32(V_{gs} - V_{th})^2 \dots\dots\dots(2)$$

Comparison of (1) and (2) indicates that the differential circuit exhibits much less distortion than its single ended counterpart while providing the same voltage gain and output swing.

While achieving a lower distortion, the differential pair consumes twice as much power than CS stage because $I_{SS} = 2I$.



THD = 15.2 %



THD = 1.85 %

Fig. 5.10. Distortion in a differential pair with (a) $v_{in} = 0.5$, (b) $v_{in} = 0.2$

The non-linearity of the circuit can be characterized by applying a sinusoid at the input and measuring the harmonic content of the output.

Putting in eq. (1), $x(t) = A \cos \omega t$

$$Y(t) = \alpha_1 A \cos \omega t + \alpha_2 A \cos^2 \omega t + \alpha_3 A \cos^3 \omega t + \dots$$

$$= \alpha_1 A \cos \omega t + \alpha_2 A^2 [1 + \cos(2\omega t)]/2 + \alpha_3 A^2 [3 \cos \omega t + \cos(3\omega t)]/4 + \dots$$

The higher order terms yield higher harmonics. In particular, even order terms and odd-order terms result in even and odd harmonics, respectively. The magnitude of the n th harmonic grows roughly in proportion to the n th power to the input amplitude. The “Harmonic Distortion” is usually quantified by summing the power of all of the

harmonics (except that of fundamental) and normalizing the result to the power of the fundamental.

$$\text{THD} = [(\alpha_2 A^2/2)^2 + (\alpha_3 A^3/4)^2] / (\alpha_1 A + 3\alpha_3 A^3/4)^2$$

Harmonic Distortion is undesirable in most signal processing applications, including audio and video systems.

Linearization Technique:

A differential pair can be degenerated as shown in 5.11.(a) and (b).

In Fig. 5.11(a), I_{SS} flows through the degeneration resistors, thereby consuming a voltage headroom of $I_{SS}R_S/2$. The circuit of Fig. 5.11(b), on the other hand does not involve this issue, but it suffers from a slightly higher noise (and offset voltage) because the two tail current sources introduce some differential error. If the output noise current of each current is equal to I_{n2} , then the input referred noise voltage of the circuit of Fig.5.11.(b) is higher than that of Fig.5.11.(a) by $2 I_{n2} R_{S2}$.

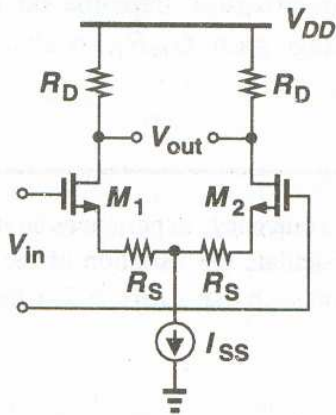


Fig. 5.11. Source degeneration applied to a differential pair

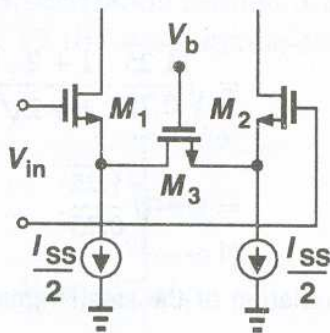


Fig.5.12. Differential pair generated by a MOSFET

Resistive degeneration requires high- quality resistors, which is difficult to fabricate. The resistor can be replaced by a MOSFET operating in deep triode region. However for large swings, M3 may not remain in deep-triode region, thereby experiencing substantial change in its on-resistance. Furthermore, V_b must track the input common mode level, so that R_{on} can be defined accurately.

Chapter 6

Analog Layouts

Device scaling has enhanced the raw speed of transistors, unwanted interaction between different sections of integrated circuits as well as non-idealities in the layout and packaging increasingly limit both the speed and the precision of such system. Analog circuit design is heavily influenced by layout and packaging.

The width and length of each transistor is determined by circuit design, most of the other dimensions in a layout are dictated by “Design rules”. These design rules are set of set of rules that guarantees proper transistor and interconnect fabrication despite various tolerances in each step of processing. These rules include Minimum widths of geometries defined on a mask, minimum spacing between masks, minimum enclosure and minimum extension of transistors in a well that must exceed a minimum value imposed by both lithography and processing capabilities of the technology.

After simulations in S-edit, layouts are made in L-edit.

6.1. Analog Layout Techniques:

Analog systems demand many layout precautions so as to minimize undesired effects such as crosstalk, mismatches, noise etc.

Multifinger Transistors:

Wide transistors are usually “folded” so as to reduce both the source/ drain junction area and gate resistance. A simple folded structure may prove inadequate for very wide devices, necessitating the use of “Multiple fingers”. As a rule of thumb, the width of each finger is chosen such that the resistance of the finger is less than the inverse of transconductance associated with the finger.

The gate resistance can be reduced by decomposing the transistor into more parallel fingers. But the capacitance associated with the perimeter of the source/ Drain area increases.

Symmetry:

The asymmetries in the fully differential circuit introduce input-referred offsets, thus limiting the min. signal level that can be detected. Inadequate attention to symmetry in the layout may result in large offsets. Symmetry also suppresses the effect of common-mode noise and even-order non-linearity. The symmetry must be applied to both the devices of interest and their surrounding environment.

The asymmetry can ameliorate by adding “dummy transistors” to the two sides of the transistors to provide same environment. The same environment must be provided on the two sides of the axis of symmetry.

Symmetry becomes more difficult to establish for large transistors. For example, in the differential pair layout, having a large width to achieve a small input offset voltage, but the gradients along the x-axis give rise to appreciable mismatches. To reduce the error, a “common-centroid” configuration may be used such that the effect of first-order gradients along both axis is cancelled. Each transistor is decomposed into two halves that are placed diagonally opposite to each other and connected in parallel.

6.2. Layouts of Amplifier:

6.2.1. Class A Amplifier layout:

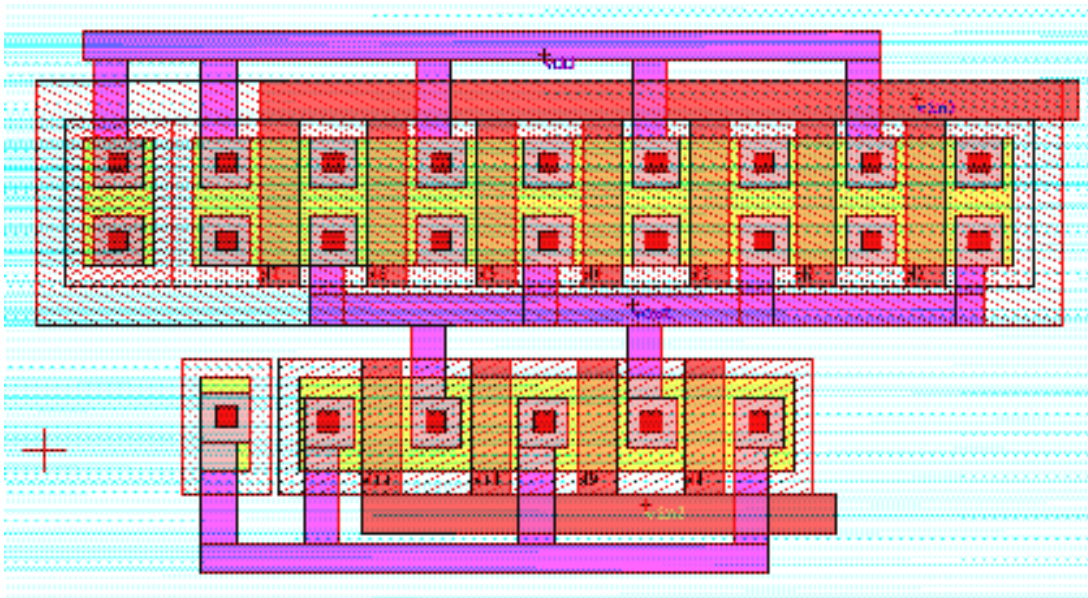


Fig. 6.1. Analog layout of fig. 3.1.

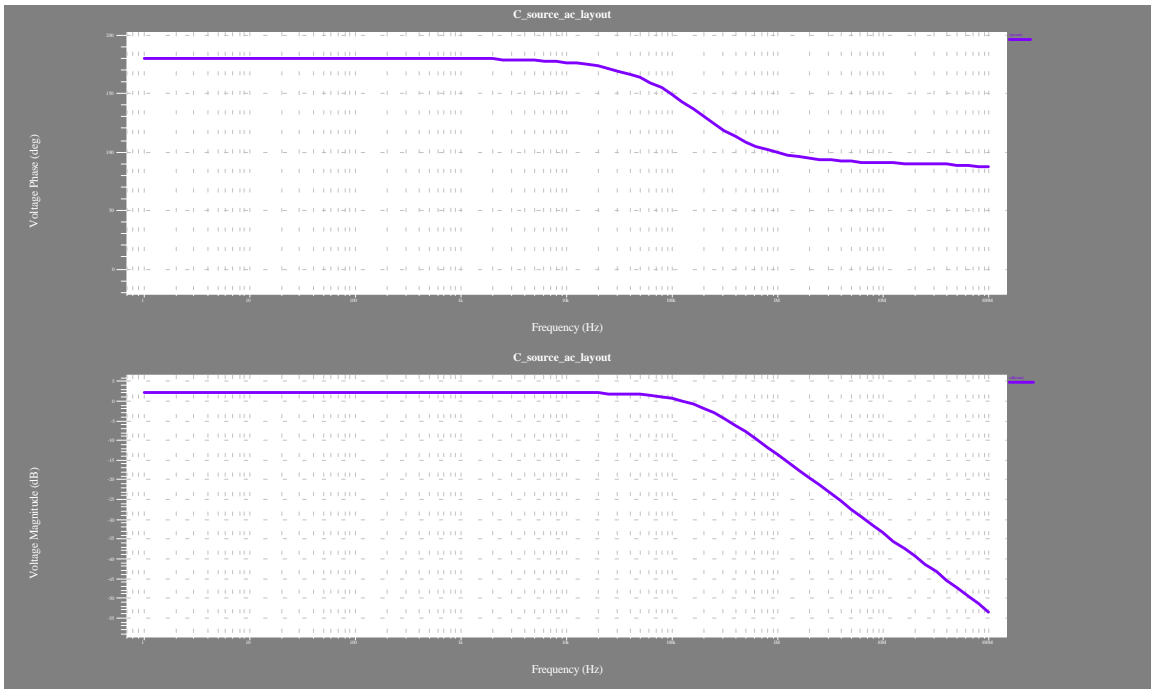


Fig. 6.2. DC Analysis of fig 6.1

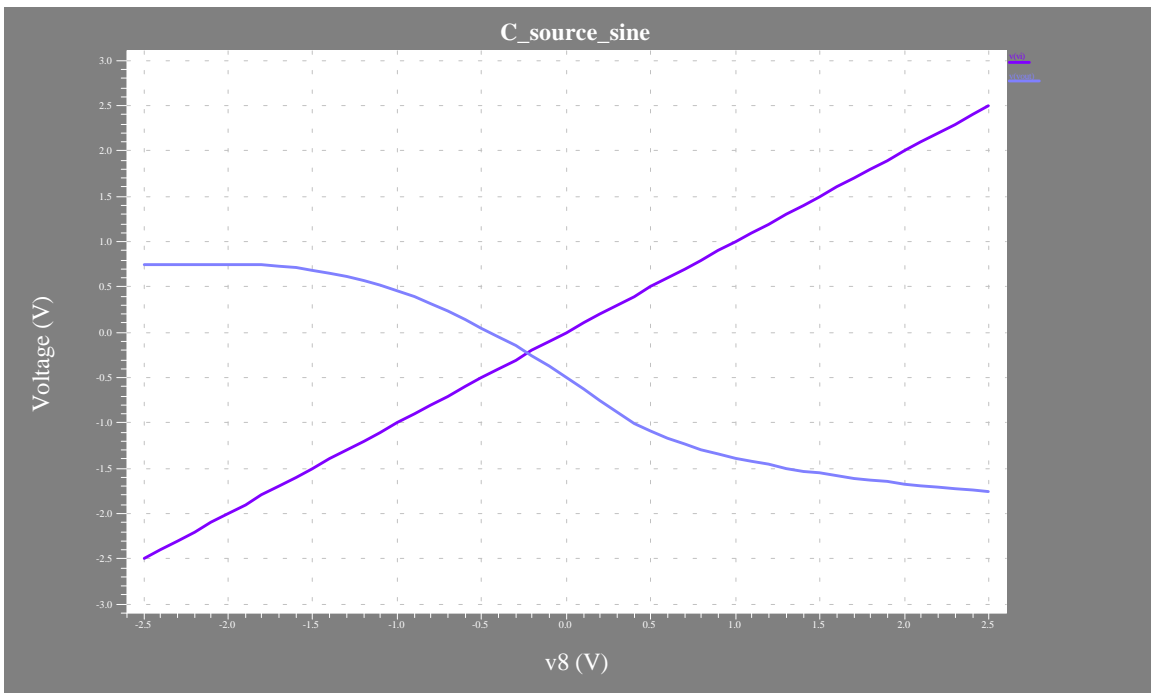


Fig. 6.3. DC analysis of fig 6.1.

6.2.2. Class B Amplifier:

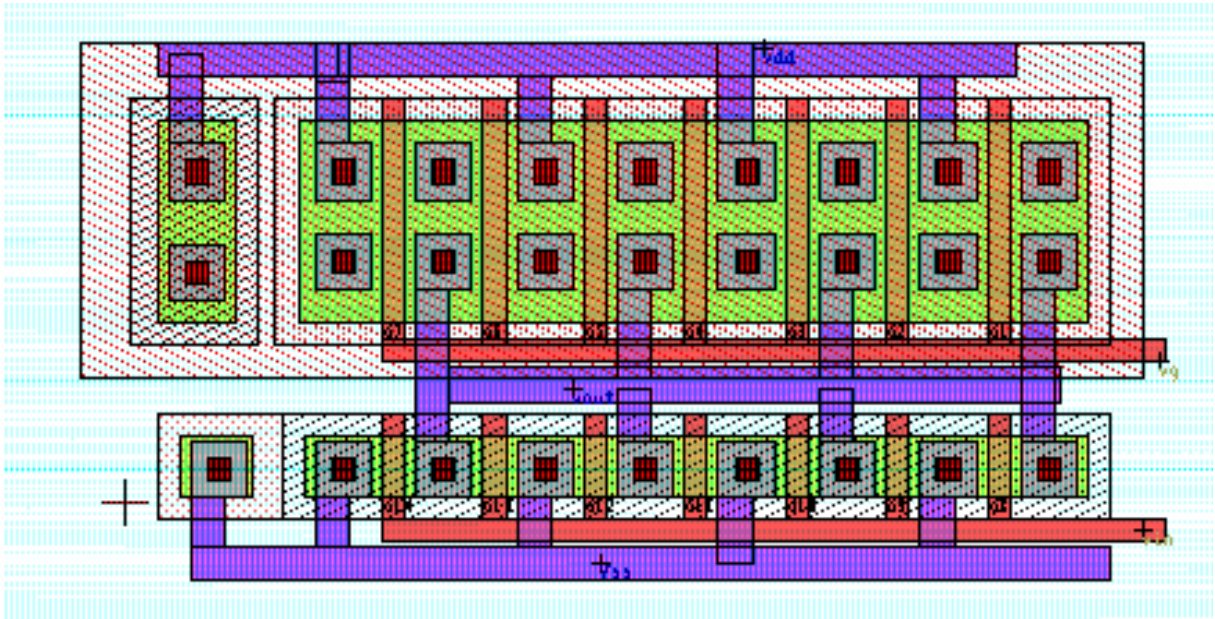


Fig.6.4. Analog Layout of fig. 3.11.

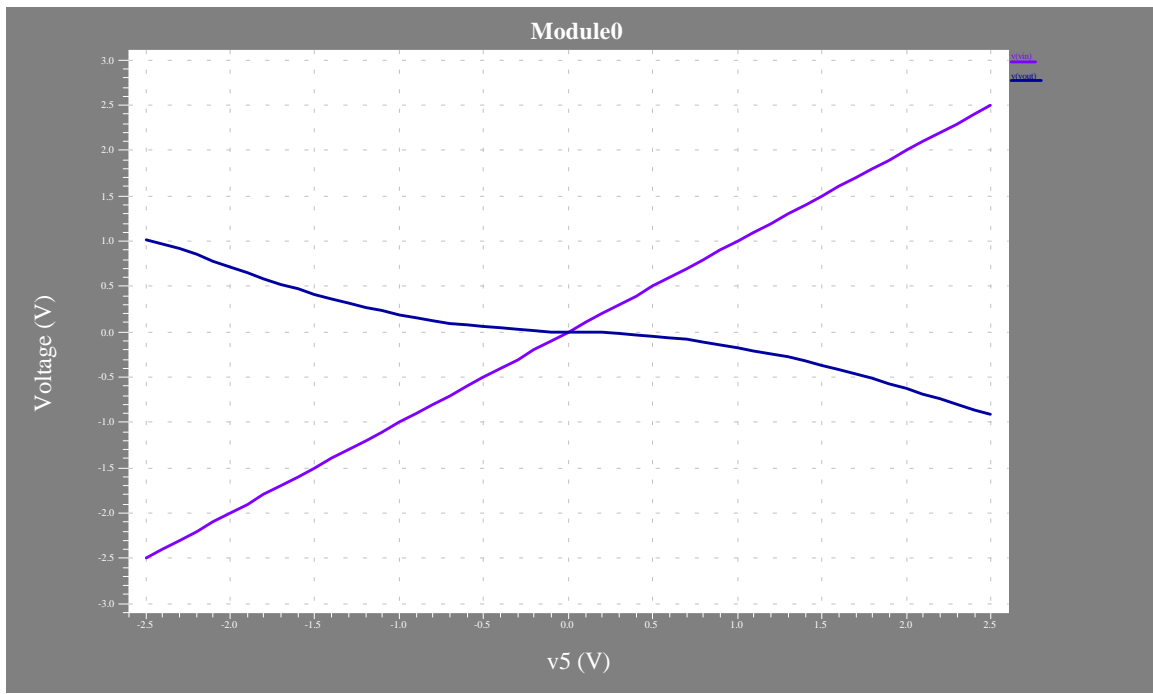


Fig. 6.5. DC Analysis of fig 6.4

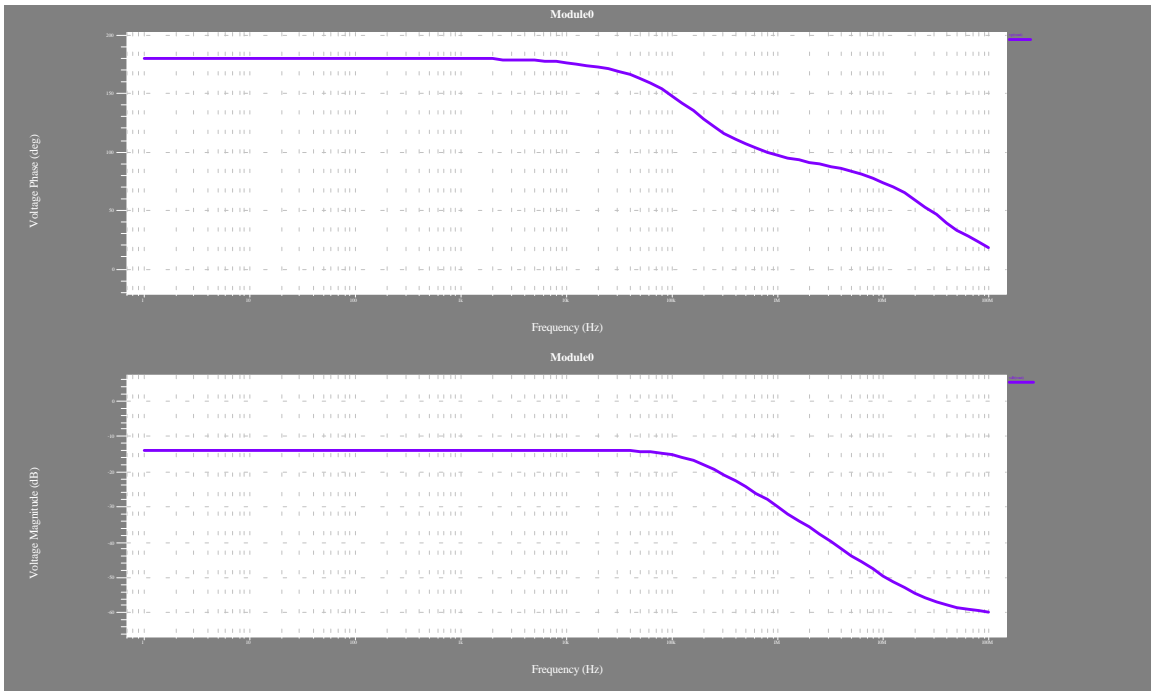


Fig. 6.6. AC Analysis of fig 6.4

Differential Amplifier with current Mirror Load:

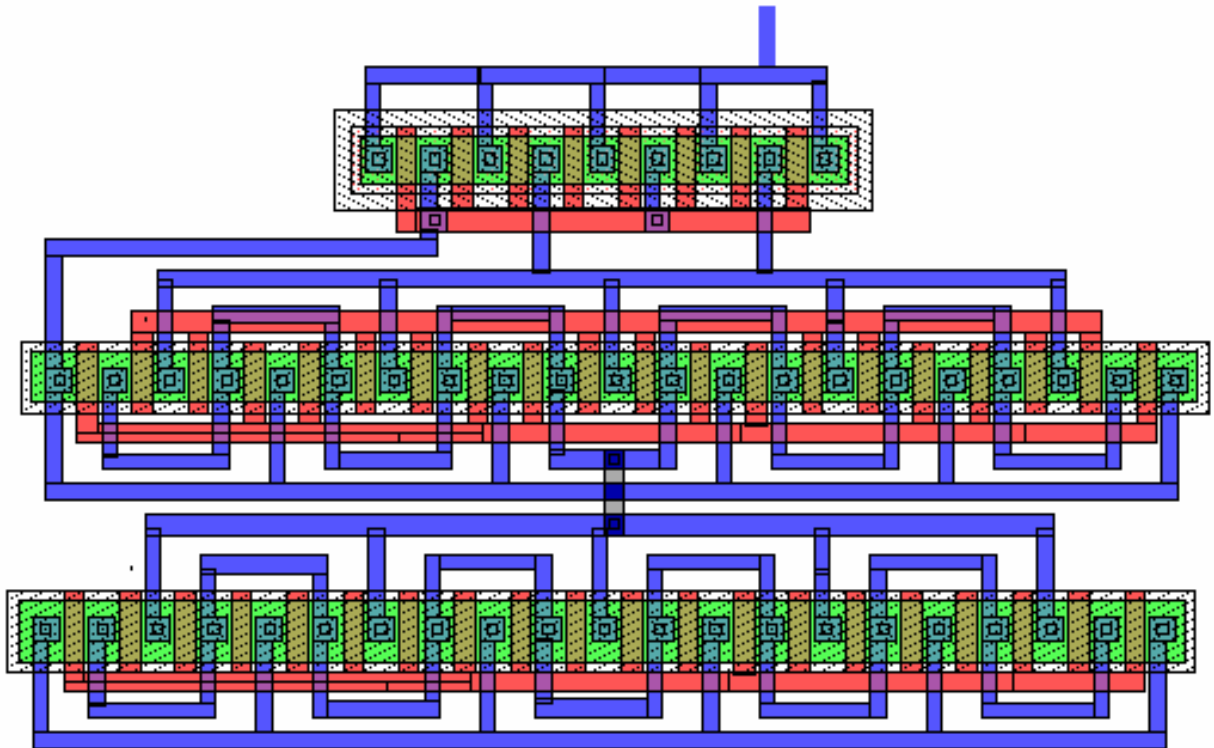


Fig. 6.7. Analog layout of fig 5.9

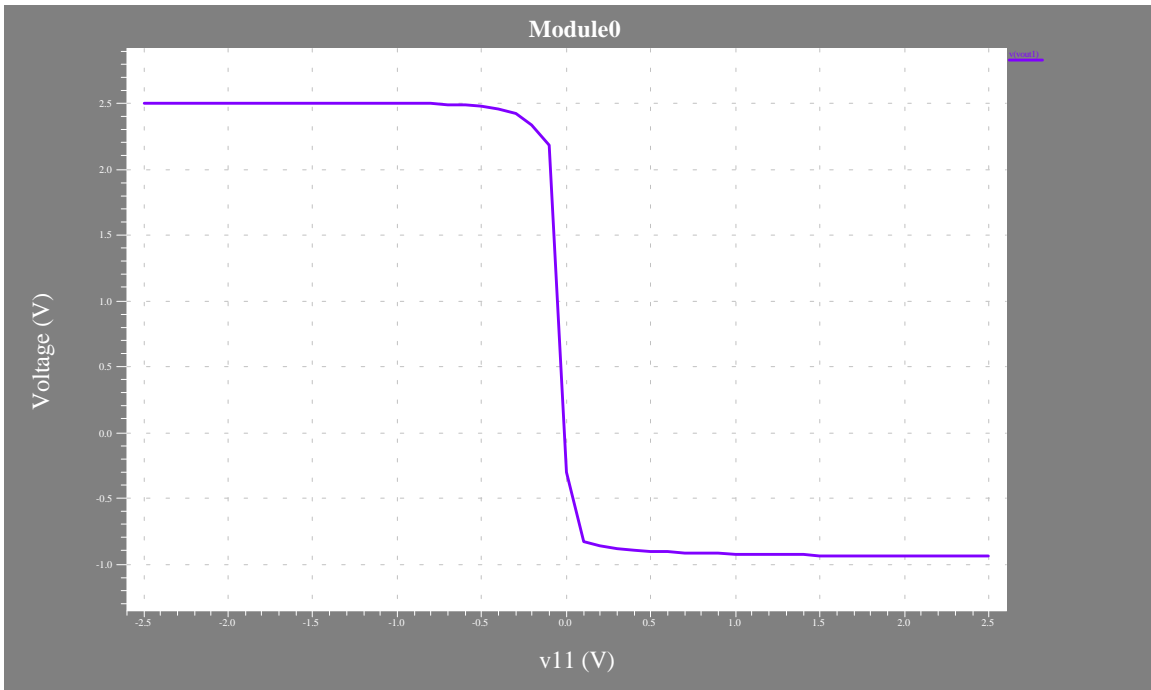


Fig. 6.8. DC Analysis of fig 6.7

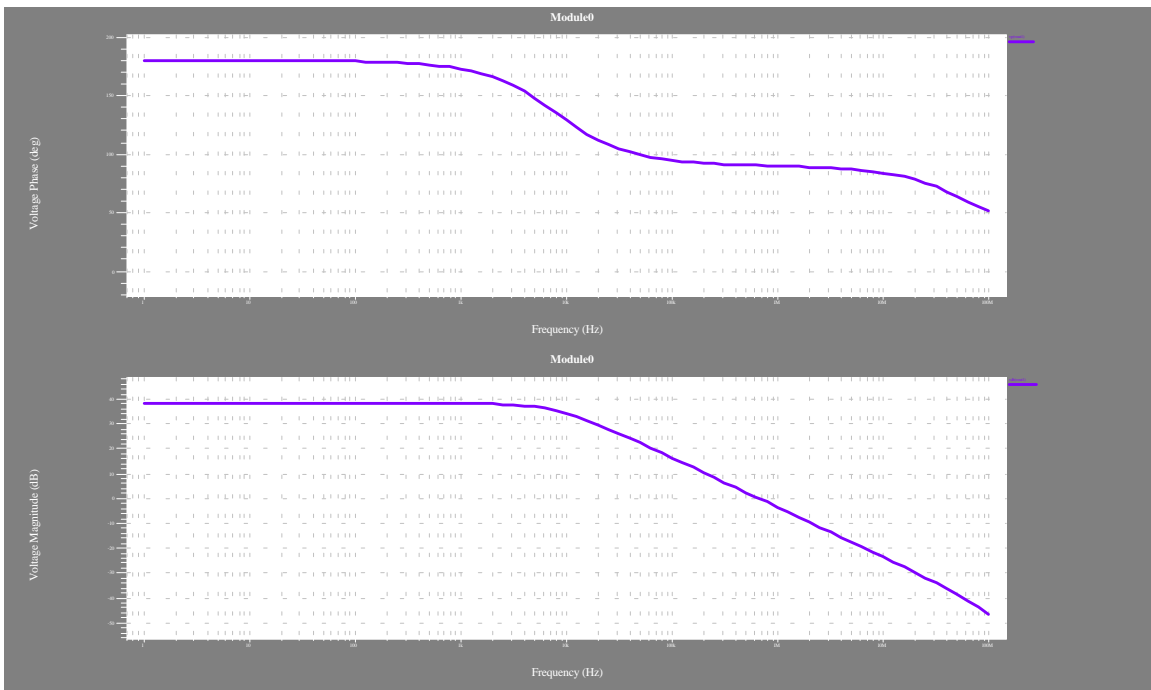


Fig. 6.9. DC Analysis of fig 6.7.

Chapter 7

Conclusion

Output Amplifier	I_{out+}	I_{out-}	R_{out}	THD	Voltage swing	-3dB BW	Efficiency	DC gain
Class A MOS common source	I _{bias}	>>I _{bias}	10.1KΩ	3.16%	1.7to – 2.1	9.3M	<25%	7.7dB
Class AB MOS Amplifier	High for large W/L	High for large W/L	25.3KΩ	6.081%	±2.06V	8.2Mega	<50%	10.5dB
Class B MOS Amplifier	High for large W/L	High for large W/L	1MegaΩ	14.08%	±1.4V	8 M	<75%	-18dB
Class A MOS source follower	High for large W/L	I _{bias}	694Ω	2.92%	-1.7 to +0.2	25M	<25%	-6dB
Class AB Inverter with negative feedback	High for large W/L	High for large W/L	650Ω	1.678%	±1.9%	17M	<75%	5.5dB
Class B MOS source Follower	High for large W/L	High for large W/L	600Ω	10.4%	±1.2	10M	<75%	-40dB

Cascode Amplifier	I_{bias}	V_{bias}	1.2 Mega	2.2%	± 2.4	10K	--	54 dB
------------------------------	------------	------------	-------------	------	-----------	-----	----	-------

The comparison performance parameters of Class A, Class B and Class AB(with and without feedback) is given in Table 3.

When high current is demanded by the resistive nature of the load, the emphasis is on the output stage. In class A output stages, the maximum current is equal to the bias current. One of the disadvantages of Class A inverting amplifiers is that considerable quiescent power is dissipated. The maximum efficiency of Class A power amplifier is 25% for a sinusoidal signal. One advantage of the Class A inverting amplifier is low distortion. This is a result of operating both MOS transistors in the saturation region over most of the output voltage swing.

Class B output stages combine high output current capability with very low quiescent current but introduce crossover distortion. The common-source class AB stage, presents a good trade-off between distortion and quiescent dissipation. The output transistors are biased with a small quiescent current compared to the maximum output current, which reduces crossover distortion in comparison with class B output stage.

Current source differential amp has performance that is identical to the current- source load sinking inverter

The Class A source follower has very low output resistance, poor signal swing, and low efficiency. The maximum source and sink currents depend on both the supply voltage and the dimensions of the transistors.

Class AB arrangements are probably the most commonly employed system for power amplifier output sections, although ‘Pure’ Class A is often used for low current/voltage applications where the poor power efficiency isn’t a problem. That *Class A* amplifiers employ a high *Quiescent Current* (sometimes called bias current or standing current)

large enough that the transistor currents are large even when the output signal level is small. It should be clear that the power efficiency of Class A amplifiers is therefore poor, but they can offer good signal performance due to avoiding problems with effects due to low-current level nonlinearities causing *Distortion*.

Class AB amplifiers have better efficiency and poorer fidelity than class A amplifiers. They are used when the output signal need not be a complete reproduction of the input signal, but both positive and negative portions of the input signal must be available at the output.

Future Scope:

The layouts study is done for just 3 configurations. Layout results can be compared with the schematic simulation results of all input and output stages.

Only two types of differential amplifiers are designed here. The study can be extended for many input stages, considering analysis of all types of differential amplifiers.

Appendix I

MODEL FILE

** MCNC 1.25um CMOS Process

** Nominal Level 2 MOSFET Parameters

** 2/26/87

.model nmos nmos

+	Level=2	Ld=0.0u	Tox=225.00E-10
+	Nsub=1.066E+16	Vto=0.622490	Kp=6.326640E-05
+	Gamma=.639243	Phi=0.31	Uo=1215.74
+	Uexp=4.612355E-2	Ucrit=174667	Delta=0.0
+	Vmax=177269	Xj=.9u	Lambda=0.0
+	Nfs=4.55168E+12	Neff=4.68830	Nss=3.00E+10
+	Tpg=1.000	Rsh=60	Cgso=2.89E-10
+	Cgdo=2.89E-10	Cj=3.27E-04	Mj=1.067
+	Cjsw=1.74E-10	Mjsw=0.195	

.model pmos pmos

+	Level=2	Ld=.03000u	Tox=225.000E-10
+	Nsub=6.575441E+16	Vto=-0.63025	Kp=2.635440E-05
+	Gamma=0.618101	Phi=.541111	Uo=361.941
+	Uexp=8.886957E-02	Ucrit=637449	Delta=0.0

+	Vmax=63253.3	Xj=0.112799u	Lambda=0.0
+	Nfs=1.668437E+11	Neff=0.64354	Nss=3.00E+10
+	Tpg=-1.00	Rsh=150	Cgso=3.35E-10
+	Cgdo=3.35E-10	Cj=4.75E-04	Mj=.341
+	Cjsw=2.23E-10	Mjsw=0.307	

Appendix II

SAMPLE NET-LIST

Simulations Results for Class A Output Stage With Current Source Load

```
* SPICE netlist written by S-Edit Win32 7.00
* Main circuit: Module0
.dc lin source v8 -2.5 2.5 .1
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.print dc v(vout) v(vin) id(M2) id(M3)
C1 vout Gnd 10pF
M2 vout vin N1 N1 NMOS L=2u W=38u AD=66p PD=24u AS=66p PS=24u
M3 vout vg N3 N3 PMOS L=2u W=125u AD=66p PD=24u AS=66p PS=24u
R4 vout Gnd 2K TC=0.0, 0.0
v5 N3 Gnd 2.5
v6 Gnd N1 2.5
v7 vg Gnd 0.74
v8 vin Gnd 2.5
* End of main circuit: Module0
```

Class AB without feedback:

```
* Main circuit: Module0
.dc lin source v7 -2.5 2.5 .1
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.print dc v(vout) v(vin) id(M2) id(M3)
C1 vout Gnd 10pF
M2 vout vin N3 N3 NMOS L=4u W=36u AD=66p PD=24u AS=66p PS=24u
M3 vout vin N2 N2 PMOS L=4u W=88u AD=66p PD=24u AS=66p PS=24u
R4 vout Gnd 2K TC=0.0, 0.0
v5 N2 Gnd 2.5
v6 Gnd N3 2.5
v7 vin Gnd 0.0
* End of main circuit: Module0
```

Class B without feedback:

```
* Main circuit: Module0
.dc lin source v8 -2.5 2.5 .1
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.print dc v(vout) v(vin) id(M2) id(M3)
C1 vout Gnd 10pF
```

```

M2 vout N1 N3 N3 NMOS L=4u W=38u AD=66p PD=24u AS=66p PS=24u
M3 vout N7 N5 N5 PMOS L=4u W=91u AD=66p PD=24u AS=66p PS=24u
R4 vout Gnd 2K TC=0.0, 0.0
v5 N2 N6 0.023 AC 1.0 0.0
v6 N5 Gnd 2.5
v7 Gnd N3 2.5
v8 vin Gnd 0
v9 N7 vin 1.81
v10 vin N1 1.81
* End of main circuit: Module0

```

Floating Battery implementation for common source class B/ AB

```

* Main circuit: Module0
.dc lin source v13 -2.5 2.5 .1
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.print dc v(vout) id(M6) id(M2)
C1 vout Gnd 100pF
M2 vout s2 N3 N3 NMOS L=4u W=44u AD=66p PD=24u AS=66p PS=24u
M3 s1 Vgg5 N2 N2 NMOS L=4u W=16u AD=66p PD=24u AS=66p PS=24u
M4 N4 vin N5 N5 NMOS L=4u W=16u AD=66p PD=24u AS=66p PS=24u
M5 s2 s2 N3 N3 NMOS L=4u W=16u AD=66p PD=24u AS=66p PS=24u
M6 vout s1 N4 N4 PMOS L=4u W=106u AD=66p PD=24u AS=66p PS=24u
M7 s1 s1 N4 N4 PMOS L=4u W=44u AD=66p PD=24u AS=66p PS=24u
M8 N3 vin N2 N2 PMOS L=4u W=44u AD=66p PD=24u AS=66p PS=24u
M9 s2 Vgg4 N5 N5 PMOS L=4u W=44u AD=66p PD=24u AS=66p PS=24u
R10 vout Gnd 2K TC=0.0, 0.0
v11 Gnd N3 2.5
v12 N4 Gnd 2.5
v13 vin Gnd 0
v14 Vgg5 Gnd 2
v15 Gnd Vgg4 2
End of main circuit: Module0

```

Cascode Amplifier:

```

* Main circuit: Module0
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.tran/op 1u 100u method=bdf
.print tran v(vout) v(vin)
C1 vout Gnd 10pF
M2 N1 N6 vout N1 NMOS L=4u W=92u AD=66p PD=24u AS=66p PS=24u
M3 N3 vin N1 N3 NMOS L=4u W=247u AD=66p PD=24u AS=66p PS=24u
M4 N7 N7 N5 N5 PMOS L=4u W=152u AD=66p PD=24u AS=66p PS=24u
M5 vout N7 N5 N5 PMOS L=4u W=152u AD=66p PD=24u AS=66p PS=24u
i6 N7 Gnd 50uA
v8 N6 Gnd -0.87
v10 N5 Gnd 2.5
v11 Gnd N3 2.5
v12 vin Gnd 0

```

Error Amplifier

```

Main circuit: Module0
.ac dec 10 1 100mega
.include "D:\tanner\S-Edit\tutorial\schematic\ml2_125.md"
.print ac vp(vout) vdb(vout)
.op

```

```

C1 vout Gnd 100pF
M2 vout N1 N2 N2 NMOS L=4u W=50u AD=66p PD=24u AS=66p PS=24u
M3 vout N1 N3 N3 PMOS L=4u W=120u AD=66p PD=24u AS=66p PS=24u
R4 vout Gnd 50 TC=0.0, 0.0
R5 N1 vout 100 TC=0.0, 0.0
R6 vin N1 2K TC=0.0, 0.0
v7 vin Gnd 0.0 AC 1.0 0.0
v8 N3 Gnd 2.5
v9 Gnd N2 2.5
End of main circuit: Module0

```

Differential Amplifier with Resistive load

```

* Main circuit: Module0
.dc lin source v10 -1 1 .1
.include "C:\Tanner\TSpice70\models\ml2_125.md"
.print dc v(vout1) v(vout2) '(v(vout1)-v(vout2))'

```

```

C1 vout2 Gnd 10pF
C2 vout1 Gnd 10pF
M3 N4 N1 N6 N4 NMOS L=4u W=52u AD=66p PD=310u AS=66p PS=24u
M4 vout1 N5 N6 N6 NMOS L=4u W=100u AD=66p PD=24u AS=66p PS=24u
M5 vout2 vg1 N6 N6 NMOS L=4u W=100u AD=66p PD=24u AS=66p PS=24u
M6 N4 N1 N1 N4 NMOS L=4u W=52u AD=66p PD=24u AS=66p PS=24u
R7 N3 vout1 10K TC=0.0, 0.0
R8 N3 vout2 10K TC=0.0, 0.0
i9 N3 N1 150uA
v10 N5 vg1 0
v11 N3 Gnd 2.5
v12 Gnd N4 2.5
v13 N5 Gnd 1
* End of main circuit: Module0

```

Differential with Current mirror load:

```

Main circuit: Module0
.dc lin source v9 -1 1 .01
.include "C:\Tanner\S-Edit\tutorial\schematic\ml2_125.md"
.print dc 'v(vout1)-v(vout2)' id(M4) id(M5) id(M1)
M1 N1 N3 N4 N4 NMOS L=4u W=52u AD=66p PD=24u AS=66p PS=24u
M2 vout2 vg1 N1 N4 NMOS L=4u W=100u AD=66p PD=24u AS=66p PS=24u
M3 vout1 vg2 N1 N4 NMOS L=4u W=100u AD=66p PD=24u AS=66p PS=24u
M4 N3 N3 N4 N4 NMOS L=4u W=52u AD=66p PD=24u AS=66p PS=24u
M5 vout1 vout2 N2 N2 PMOS L=4u W=32u AD=66p PD=24u AS=66p PS=24u
M6 N2 vout2 vout2 N2 PMOS L=4u W=32u AD=66p PD=24u AS=66p PS=24u
i7 N2 N3 100uA
v8 N2 Gnd 2.5
v9 vg1 vg2 0
v10 Gnd N4 2.5
v11 vg2 Gnd 1.5
End of main circuit: Module0

```

Class A Distortion Analysis:

The distortion was calculated for $v_{in} = 0.5$ and $v_{in} = 0.2$
For $v_{in}=0.5$
FOURIER ANALYSIS RESULTS

Fourier components of transient response v(vout)

DC component = 3.7061e-001

Harmonic no	Frequency<Hz>	Fourier comp	Normalized FC	Phase<deg>	Normalized phase
1	2.0000e+004	1.0782e+000	1.0000e+000	-1.7834e+002	0.0000e+000
2	4.0000e+004	1.4386e-002	1.3343e-002	-1.4521e+001	1.6382e+002
3	6.0000e+004	2.5358e-002	2.3520e-002	-1.7645e+002	1.8920e+000
4	8.0000e+004	1.3339e-002	1.2372e-002	6.3744e+001	2.4208e+002
5	1.0000e+005	1.0050e-002	9.3211e-003	5.2687e+000	1.8361e+002
6	1.2000e+005	4.3762e-003	4.0589e-003	-2.4690e+001	1.5365e+002
7	1.4000e+005	8.3822e-004	7.7744e-004	1.1206e+001	1.8954e+002
8	1.6000e+005	3.1011e-003	2.8763e-003	-8.9317e+000	1.6941e+002
9	1.8000e+005	3.0420e-004	2.8214e-004	1.2117e+002	2.9951e+002

Total harmonic distortion = 3.157 percent

For Vin=0.2

FOURIER ANALYSIS RESULTS

Fourier components of transient response v(vout)

DC component = 3.7013e-001

Harmonic no	Frequency<Hz>	Fourier comp	Normalized FC	Phase<deg>	Normalized phase
1	2.0000e+004	4.6104e-001	1.0000e+000	-1.7833e+002	0.0000e+000
2	4.0000e+004	7.0565e-003	1.5306e-002	3.4472e+001	2.1281e+002
3	6.0000e+004	1.0076e-003	2.1855e-003	-1.7305e+002	5.2868e+000
4	8.0000e+004	2.6295e-003	5.7034e-003	1.5600e+001	1.9393e+002
5	1.0000e+005	4.8597e-004	1.0541e-003	5.9869e+000	1.8432e+002
6	1.2000e+005	1.8519e-003	4.0168e-003	-9.7929e+000	1.6854e+002
7	1.4000e+005	9.9905e-004	2.1670e-003	1.4440e+001	1.9277e+002
8	1.6000e+005	1.4140e-003	3.0670e-003	-8.9884e+000	1.6935e+002
9	1.8000e+005	1.1930e-003	2.5877e-003	1.7252e+001	1.9559e+002

Total harmonic distortion = 1.76 percent

Efficiency and Power Calculations Power Results

v6 from time 0 to 0.1

Average power consumed -> 2.854781e-006 watts

Max power 4.235445e-003 at time 6.26814e-005

Min power 1.419001e-003 at time 3.74009e-005

v5 from time 0 to 0.1

Average power consumed -> 2.391479e-006 watts

Max power 2.486739e-003 at time 6.26814e-005

Min power 2.284143e-003 at time 3.74009e-005

R4 from time 0 to 0.1

Average power consumed -> 3.628325e-007 watts

Max power 9.785920e-004 at time 6.26814e-005

Min power 2.759044e-009 at time 7.76315e-005

Latout of Class A source follower:

* NODE NAME ALIASES

* 1 = Vss (42.5,-5.5)

* 2 = vout (40,10)

* 3 = vdd (57,40.5)

* 4 = vg (92.5,12.5)

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*      5 = vin (91,-2.5)
M1 vout vin Vss Vss NMOS L=2E-006 W=5.5E-006 AD=3.85E-011 PD=2.5E-005 AS=1.925E-011
PS=1.25E-005
* M1 DRAIN GATE SOURCE BULK (77 0.5 79 6)
M2 Vss vin vout Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=1.925E-011
PS=1.25E-005
* M2 DRAIN GATE SOURCE BULK (68 0.5 70 6)
M3 vout vin Vss Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=1.925E-011
PS=1.25E-005
* M3 DRAIN GATE SOURCE BULK (59 0.5 61 6)
M4 Vss vin vout Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=1.925E-011
PS=1.25E-005
* M4 DRAIN GATE SOURCE BULK (50 0.5 52 6)
M5 vout vin Vss Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=1.925E-011
PS=1.25E-005
* M5 DRAIN GATE SOURCE BULK (41 0.5 43 6)
M6 Vss vin vout Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=1.925E-011
PS=1.25E-005
* M6 DRAIN GATE SOURCE BULK (32 0.5 34 6)
M14 vout vin Vss Vss NMOS L=2E-006 W=5.5E-006 AD=1.925E-011 PD=1.25E-005 AS=3.85E-011
PS=2.5E-005
* M14 DRAIN GATE SOURCE BULK (23 0.5 25 6)
M7 vout vg vdd vdd PMOS L=2E-006 W=1.8E-005 AD=1.26E-010 PD=5E-005 AS=6.3E-011 PS=2.5E-
005
* M7 DRAIN GATE SOURCE BULK (77 16 79 34)
M8 vdd vg vout vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=6.3E-011 PS=2.5E-
005
* M8 DRAIN GATE SOURCE BULK (68 16 70 34)
M9 vout vg vdd vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=6.3E-011 PS=2.5E-
005
* M9 DRAIN GATE SOURCE BULK (59 16 61 34)
M10 vdd vg vout vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=6.3E-011 PS=2.5E-
005
* M10 DRAIN GATE SOURCE BULK (50 16 52 34)
M11 vout vg vdd vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=6.3E-011 PS=2.5E-
005
* M11 DRAIN GATE SOURCE BULK (41 16 43 34)
M12 vdd vg vout vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=6.3E-011 PS=2.5E-
005
* M12 DRAIN GATE SOURCE BULK (32 16 34 34)
M13 vout vg vdd vdd PMOS L=2E-006 W=1.8E-005 AD=6.3E-011 PD=2.5E-005 AS=1.35E-010
PS=5.1E-005
* M13 DRAIN GATE SOURCE BULK (23 16 25 34)
.END

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Layout of class B source follower:

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* NODE NAME ALIASES
*      2 = vout (60,15)
*      3 = vdd (51,40.5)
*      4 = vin2 (61.5,-5.5)
M1 vout 5 vdd vdd PMOS L=4E-006 W=1.3E-005 AD=9.1E-011 PD=4E-005 AS=4.55E-011 PS=2E-005
* M1 DRAIN GATE SOURCE BULK (88 19 92 32)
M2 vdd 5 vout vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=4.55E-011 PS=2E-005
* M2 DRAIN GATE SOURCE BULK (77 19 81 32)
M3 vout 5 vdd vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=4.55E-011 PS=2E-005
* M3 DRAIN GATE SOURCE BULK (66 19 70 32)

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M4 vdd 5 vout vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=4.55E-011 PS=2E-005
* M4 DRAIN GATE SOURCE BULK (55 19 59 32)
M5 vout 5 vdd vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=4.55E-011 PS=2E-005
* M5 DRAIN GATE SOURCE BULK (44 19 48 32)
M6 vdd 5 vout vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=4.55E-011 PS=2E-005
* M6 DRAIN GATE SOURCE BULK (33 19 37 32)
M7 vout 5 vdd vdd PMOS L=4E-006 W=1.3E-005 AD=4.55E-011 PD=2E-005 AS=9.1E-011 PS=4E-005
* M7 DRAIN GATE SOURCE BULK (22 19 26 32)
M8 1 vin2 vout 1 NMOS L=4E-006 W=9.5E-006 AD=6.65E-011 PD=3.3E-005 AS=3.325E-011
PS=1.65E-005
* M8 DRAIN GATE SOURCE BULK (65.5 -2 69.5 7.5)
M9 vout vin2 1 1 NMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011
PS=1.65E-005
* M9 DRAIN GATE SOURCE BULK (54.5 -2 58.5 7.5)
M10 1 vin2 vout 1 NMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011
PS=1.65E-005
* M10 DRAIN GATE SOURCE BULK (43.5 -2 47.5 7.5)
M11 vout vin2 1 1 NMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=6.175E-011
PS=3.2E-005
* M11 DRAIN GATE SOURCE BULK (32.5 -2 36.5 7.5)
.END

Layout of differential Amplifier:

* NODE NAME ALIASES
* 1 = vdd (160,70)
* 4 = Gnd (37.5,-62)
M1 vdd 5 6 2 PMOS L=4E-006 W=9.5E-006 AD=7.6E-011 PD=3.5E-005 AS=3.325E-011 PS=1.65E-005
* M1 DRAIN GATE SOURCE BULK (164 41 168 50.5)
M2 6 5 vdd 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M2 DRAIN GATE SOURCE BULK (153 41 157 50.5)
M3 vdd 5 5 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M3 DRAIN GATE SOURCE BULK (142 41 146 50.5)
M4 5 5 vdd 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M4 DRAIN GATE SOURCE BULK (131 41 135 50.5)
M5 vdd 5 6 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M5 DRAIN GATE SOURCE BULK (120 41 124 50.5)
M6 vdd 5 6 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M6 DRAIN GATE SOURCE BULK (109 41 113 50.5)
M7 vdd 5 5 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=3.325E-011 PS=1.65E-005
* M7 DRAIN GATE SOURCE BULK (98 41 102 50.5)
M8 5 5 vdd 2 PMOS L=4E-006 W=9.5E-006 AD=3.325E-011 PD=1.65E-005 AS=6.65E-011 PS=3.3E-005
* M8 DRAIN GATE SOURCE BULK (87 41 91 50.5)
M9 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=9.6E-011 PD=4E-005 AS=4.2E-011 PS=1.9E-005
* M9 DRAIN GATE SOURCE BULK (230.5 -53 234.5 -41)
M10 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M10 DRAIN GATE SOURCE BULK (219.5 -53 223.5 -41)
M11 7 9 6 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M11 DRAIN GATE SOURCE BULK (222 -2 226 8)

M12 6 9 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M12 DRAIN GATE SOURCE BULK (211 -2 215 8)
M13 5 8 7 10 NMOS L=4E-006 W=1E-005 AD=8E-011 PD=3.6E-005 AS=3.5E-011 PS=1.7E-005
* M13 DRAIN GATE SOURCE BULK (233 -2 237 8)
M14 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M14 DRAIN GATE SOURCE BULK (208.5 -53 212.5 -41)
M15 Gnd 11 3 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M15 DRAIN GATE SOURCE BULK (197.5 -53 201.5 -41)
M16 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M16 DRAIN GATE SOURCE BULK (186.5 -53 190.5 -41)
M17 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M17 DRAIN GATE SOURCE BULK (175.5 -53 179.5 -41)
M18 7 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M18 DRAIN GATE SOURCE BULK (164.5 -53 168.5 -41)
M19 Gnd 11 3 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M19 DRAIN GATE SOURCE BULK (153.5 -53 157.5 -41)
M20 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M20 DRAIN GATE SOURCE BULK (142.5 -53 146.5 -41)
M21 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M21 DRAIN GATE SOURCE BULK (131.5 -53 135.5 -41)
M22 7 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M22 DRAIN GATE SOURCE BULK (120.5 -53 124.5 -41)
M23 7 9 6 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M23 DRAIN GATE SOURCE BULK (178 -2 182 8)
M24 6 9 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M24 DRAIN GATE SOURCE BULK (167 -2 171 8)
M25 7 9 6 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M25 DRAIN GATE SOURCE BULK (134 -2 138 8)
M26 6 9 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M26 DRAIN GATE SOURCE BULK (123 -2 127 8)
M27 7 8 5 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M27 DRAIN GATE SOURCE BULK (200 -2 204 8)
M28 5 8 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M28 DRAIN GATE SOURCE BULK (189 -2 193 8)
M29 7 8 5 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M29 DRAIN GATE SOURCE BULK (156 -2 160 8)
M30 5 8 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M30 DRAIN GATE SOURCE BULK (145 -2 149 8)
M31 7 8 5 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M31 DRAIN GATE SOURCE BULK (112 -2 116 8)
M32 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M32 DRAIN GATE SOURCE BULK (109.5 -53 113.5 -41)
M33 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M33 DRAIN GATE SOURCE BULK (98.5 -53 102.5 -41)

M34 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M34 DRAIN GATE SOURCE BULK (87.5 -53 91.5 -41)
M35 7 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M35 DRAIN GATE SOURCE BULK (76.5 -53 80.5 -41)
M36 Gnd 11 3 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M36 DRAIN GATE SOURCE BULK (65.5 -53 69.5 -41)
M37 3 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M37 DRAIN GATE SOURCE BULK (54.5 -53 58.5 -41)
M38 Gnd 11 7 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M38 DRAIN GATE SOURCE BULK (43.5 -53 47.5 -41)
M39 7 11 Gnd 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=4.2E-011 PS=1.9E-005
* M39 DRAIN GATE SOURCE BULK (32.5 -53 36.5 -41)
M40 Gnd 11 3 10 NMOS L=4E-006 W=1.2E-005 AD=4.2E-011 PD=1.9E-005 AS=1.08E-010 PS=4.2E-005
* M40 DRAIN GATE SOURCE BULK (21.5 -53 25.5 -41)
M41 7 9 6 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M41 DRAIN GATE SOURCE BULK (90 -2 94 8)
M42 6 9 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M42 DRAIN GATE SOURCE BULK (79 -2 83 8)
M43 7 9 6 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M43 DRAIN GATE SOURCE BULK (46 -2 50 8)
M44 6 9 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M44 DRAIN GATE SOURCE BULK (35 -2 39 8)
M45 5 8 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M45 DRAIN GATE SOURCE BULK (101 -2 105 8)
M46 7 8 5 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M46 DRAIN GATE SOURCE BULK (68 -2 72 8)
M47 5 8 7 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=3.5E-011 PS=1.7E-005
* M47 DRAIN GATE SOURCE BULK (57 -2 61 8)
M48 7 8 5 10 NMOS L=4E-006 W=1E-005 AD=3.5E-011 PD=1.7E-005 AS=9E-011 PS=3.8E-005
* M48 DRAIN GATE SOURCE BULK (24 -2 28 8)
.END

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