MODIFIED 10 CODED TEST DATA COMPRESSION TECHNIQUE FOR SYSTEM ON CHIP

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Submitted by

APOORVA

Roll No: 601562003

Under the Guidance of

Ms. Harpreet Vohra

Assistant Professor, ECED

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

THAPAR UNIVERSITY, PATIALA (PUNJAB) 147004

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DECLARATION

I, Apoorva hereby declare that the work presented in this thesis entitled **"Modified 10 coded test data compression technique for system on chip"** in partial fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under the supervision of **Ms. Harpreet Vohra,** Assistant Professor, ECED, Thapar University from January 2016 to June 2017. The matter presented in this thesis has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 14/9/17

APOORVA

Roll no: 601562003

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Ms. Harpreet Vohra
Assistant Professor
ECED, Thapar University

Date 14/9/17

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My most sincere thanks to my parents, who have always been a pillar of strength in my life.

ABSTRACT

SoC testing has become increasingly complex nowadays. With the application of large test data, there is an increase in test time. The testing cost of a SoC is directly proportional to test data volume. Large test data volume also leads to increased automatic test equipment (ATE) memory requirements. International Technology Roadmap for Semiconductors (ITRS) represents that there will be a need of hundreds of sub-processors for the future generation of SOC designs which will further increase the test cost. Testing involves a large amount of power dissipation. Dynamic power dissipation is the major source of power dissipation due to increased switching activity.

Many techniques have been proposed till date to lessen test data volume and test power consumption during testing of an SoC. But till date, there has always been a tradeoff between power consumption and compression in test data volume. The objective of this work is to compress the test data by modifying the 10C coding scheme. In this thesis report, modified compression technique is proposed for testing different SoC's while taking test power into consideration. This problem can be optimized by first double reordering based on hamming distance. Secondly, apply modified 10C compression scheme on the reordered test set taking into account the maximum probability of frequency of occurrence of combinations. Testing of compression mechanism has been carried out on ISCAS's benchmark circuits with achieved compression efficiency up to 49.18% and power consumption reduced by 72.34%.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Nowadays core based design methodology is employed on a vast scale for designing system on chips, commonly referred to as System on Chip (SoC). An SoC is a system on an IC that integrates software and hardware Intellectual Property (IP) blocks using more than one design methodology for the purpose of defining the functionality and behavior of the required system by the user.

A typical SoC comprises of many intellectual property (IP) cores each core of which is assigned a particular task. And the amalgamation of such cores on a single chip gives rise to what is nowadays termed as SoC. In today's rapidly growing technology, the time to market is a very important term in electronic design business. It is always required for a manufacturer to come up with new product in the market at the earliest. To reuse the existing verified designs in the new product is a key to save design time.

The primary design methods used today can be divided into three segments depending on the linchpin technologies used, the design capacity, and the level of and investment in design reuse.There are designs being implemented at three levels as shown in fig.1.1.Application specific integrated circuits are being implemented as single logic blocks then followed by amalgamation of logic along with processor and memory. An SoC can be divided into many sub-categories depending on the type of cores being used during its designing, some can be firm cores or hard cores. In these, modification cannot be done at the gate level and hence, we opt for soft cores in which the circuit designer has the full right to make changes at the gate level. In soft cores, the entire implementation can be re-design and make sufficient changes at the basic level. Hence reusability comes at the expense in making the modifications at the circuit level.

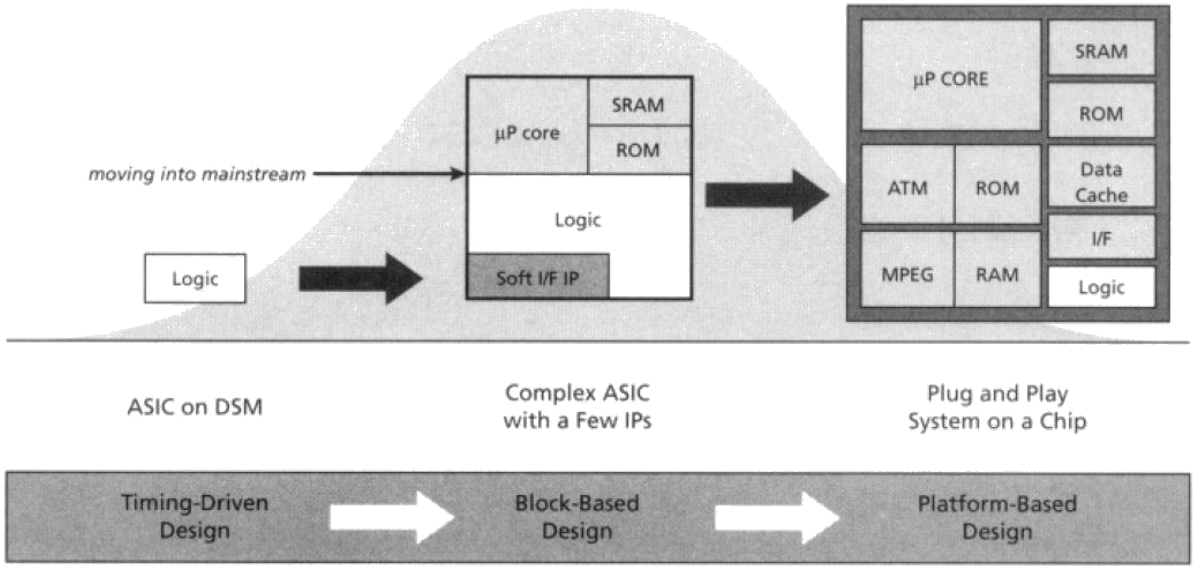

Fig 1.1: Design Methodologies

As can be seen from Fig 1.2, for every new core being designed there is anincrease in the number of resources being used. To minimize the number of resources, design reuse concept has been introduced. Also, there is less time to market by using multiple reusescheme.

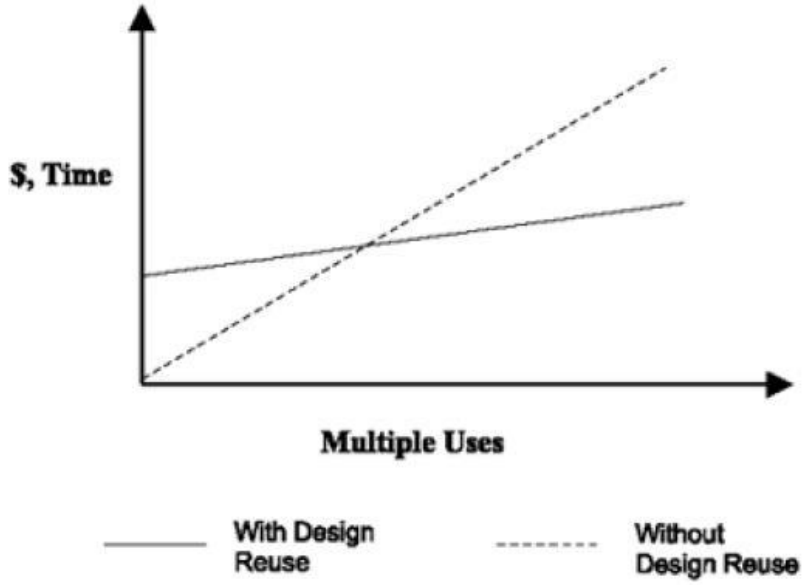

Fig. 1.2: Resources vs. no of uses plot

The testing time of an SoC depends on the test data volume, the time required to transfer the data to the cores and the rate of transferring the test data. This total testing time can be

reduced bycompressing the test data volume. Test data compression techniques can be applied on all types of cores whether hard, soft or firm whereas scan chains reorganization can only be applied to soft and firm cores. Hence, we go for test data compression.

There are mainly two sources of power which are taken into consideration at this juncture: Peak Power and Average power. Average power is the sum total of all the power distributed over a given time interval. This average power overall leads to generation of enormous amount of heat in SoC.This heat then further causes early dying out of SoC,decrease in overall performance,occurrence of faults at a rapid rate thereby having serious reliability concerns.

The above mentioned effects due to increase in average power also cause changes such as thermal runway and variation in current flow. These temperature alterations lead to delay. Besides to these variations, the excessive heat as a result of increased switching activity plays a heavy toll on the test cost.

Peak power, defined as the maximum power at any given time interval leads to noise at the power supply level due to an increased stipulation of instantaneous current. There are also enhanced chances of test failure occurring at the initial level.Hence, average and peak power dissipation has a vital role to play during the testing of any SoC.

For a CMOS circuit comprising of NMOS and PMOS, power consumption [12] can be classified in two types static and dynamic. Short circuit power consumes when there is a direct current path from V_{dd} to GND while PMOS and NMOS are ON simultaneously for a short period. Dynamic power consumption arises due to the switching activity that arises due to the transition from 0 to 1 or vice versa. Dynamic power is the major cause of power consumption since energy in CMOS circuits is mainly dissipated due to signal transition. In our test data, there are a large number of don't cares. Test power can be reduced by two mechanisms either by scheduling of the cores which are to be tested simultaneously or by minimizing the number of transitions in the test data. Power consumption can be minimized by appropriately assigning binary values to the don't care bits in test data using appropriate reorder schemes.[17]. Reordering can be based on hamming distance and then applying minimum transition filling or bit stuffing technique to fill X's.

The compression of the input test data occurs as a result of compression scheme,thereby reducing the test data volume. Compression schemes can only increase the compression ratio without taking into account high amounts of power dissipated during the testing process.

In this thesis, a double reordering scheme based on minimizing the hamming distance which allows for assigning don't care along with reduction in hamming distance thereby leading to a significant decrease in the average and peak power dissipation. After analyzing various ISCAS 89 circuits with test set, we can say that first reordering the original uncompact test set with don't care bits and then don't care bits are filled using minimum transition filling approach and then again it is reordered and at last difference vector is taken before being compressed by multi-code compression coding scheme. The major contribution of this work has been carried out on the below mentioned platform:

- Double reordering scheme has been carried out on MATLAB (R2012).
- A decoder has been designed for 10C compression scheme.
- Designing of decoder has been synthesized using XILINX.

1.2 Thesis Organization:

The rest of the report is organized as follows:

Chapter 1: Introduces the motivation for this proposed work,problem outline and gives contributions of work.

Chapter 2: briefly compares various reordering techniques. Along with an analysis with and without don't care filling followed by a comparison of all the schemes and discussion of compression techniques in detail along with their advantages and disadvantages.

Chapter 3: describes the proposed reordering scheme and difference test vectors to calculate peak power and average power which is a major component during testing,presents don't care bits filling techniques so as to minimize hamming distance. Reordering scheme has been implemented in MATLAB R2009 and R2012 for four benchmark circuits with test data set. Also presents the compression scheme applied on the reordered test set data implemented in MATLAB.

Chapter 4:gives the results for compression have been shown along with the decoder design in Xilinx. The experimental results and comparison with other code based test data compression techniques are shown.

Chapter 5: concludes the report along with the future outline in which further advancements can be done.

CHAPTER 2

LITERATURE REVIEW

Huge amounts of test data with ever increasing complexity of SoC's is a major hurdle during testing of anSoC. Testing has to be such that no faults should be left in an SoC.In this chapter, the analysis of the previous work in test data compression and test power domain is briefly discussed.

2.1 MINIMIZATION OF TEST DATA VOLUME:

The analysis of test data volume takes place through various means such as run length based codes,statistical codes or constructive codes. One of the run length based codes is presented in [16] involving storage of the test data in compressed form in tester memory. Herein, statistical coding has been used in which a unique code word is assigned to the possible recurring combinations. To provide the shortest code word possible, we have implemented Hamming Distance mechanism. Huffman code infers from the Huffman tree wherein the path distance from the topmost node i.e. root to each leaf determine the code word for each possible combination. Also in [7] run length encoding is performed for fixed as well as variable length blocks. It provides maximum compression[2] but on the other hand requires a complex decoder. There is no reduction in the power consumption while testing the SoC Static compaction techniques proposed by [5] to control power dissipation during scanning of test vectors. Due to increased number of transitions while scanning the test vectors, there is increase in dynamic power consumption with increase in switching activity. Average power and peak power reduces to a great extent by employing these techniques but on the other hand integration density and clock frequency increases abruptly. Hence, we need to take both factors into consideration test data volume as well as test power consumption. There cannot be a tradeoff in only one of the factors mentioned above.

There has also been a consideration of dictionary based compression put by [9] in which unique code words are obtained for each character. Its limited to only text based compression. There is also high space complexity associated with dictionary based compression.in this string of characters is replaced by a single character thereby reducing the effective length of text data. Then we proceed to compression via cyclical scan chains and its application to

testing core based design introduced by [14]. Here an internal xor operation is performed on the input scan vectors thereby leading to a decrease in the overall test data volume. But it has been able to achieve compression ratio up to 15.9% and also significant increase in test application time.

Alt-FDR scheme[13] proposed a mechanism in which alternating run lengths of 0's and 1's are considered for successive compression. First an entire run length is taken for all 0's consecutively followed by all 1's which happens only in certain benchmark circuits and hence the achieved average compression ratio achieved is up to 15.9% with no reduction in test power. Overall, there is an increase in test application time. On applying weighted reordering once again put up by Usha Mehta [12] we are able to achieve low scan power with no extra area overhead.

Reordering mechanism has been explained in detail in chapter 3 wherein we have performed double reordering. Reordering is performed on the basis of ascending order of hamming distance between successive test vectors. There hasn't been any compression achieved in this mechanism thereby still high test application time.

On applying FDR code as proposed by [15], a new class of variable-to-variable-length compression codes that are designed using the distributions of the runs of 0's in typical test sequences. An FDR code is a variable-to-variable-length code which maps variable-length runs of 0's to code words of variable length. It can be used to compress both the difference vector sequence Tdiffand the test set Td. But it hasn't taken into account the frequency of occurrence of continuous run lengths of 0's and 1's. Hence, it achieves a remarkable compression ratio at the cost of increasing area overhead and no variation in test power consumption.

On the other hand, on implementing selective Huffman coding as in [16], there is 10% area increase as compared to FDR with no appreciable increase in compression ratio even less than 0.2% in some of the cases. And in analyzing tradeoffs in scan power and test data compression for a SoC as proposed by [17]there is 55% compression achieved at the expense of test power. It is shown how combining a recently proposed symmetric coding scheme and a new weighted scan latch reordering (W-SLR) algorithm, leads to efficient exploration in the scan power and test data compression solution space. This is achieved by reducing and, at the same time, balancing the transition activity in scan-in and scan-out sequences. This put an impact, on the one hand, the test data compression which depends only on the scan-in

sequence, and, on the other hand, the overall scan power dissipation which depends on both the scan-in and the scan-out sequences.

There has been a change in frequency directed codes by employing Alternating Frequency directed run length code which exploits the the typical properties of deterministic test sets to achieve upto 88% compression ratio as proposed in [18] .

In optimal selective compression [1], a very efficient technique which works by overcoming the obstacles of 9C coding technique of the unique code words. OSCCPRL techniques works on the principle of achieving maximum compression by opting either inter or intra block merging on the basis of the compression achieved by both. Since unique combination takes more number of bits for encoding, the main emphasis is laid on unique code words only. A little increase in area overhead in decoder has been compensated for achieving 80% compression ratio. But there hasn't been any decrease in test power consumption.

Among the many other block code techniques, Block merging-8C also plays a significant role in achieving test data compression up to 68.14%. This technique primarily focuses on the block size of 8 bits at a time and determining the compatibility between them based on the assigned code words. This technique is limited on fixed block size and hence only efficient for some of the test data and not of varying block sizes. Golomb coding and Huffman techniques have also been implemented for recurring patterns in the entire test set data. Also, due to an increase in unique set of test patterns it becomes challenging to keep a track of each one of the patterns.

2.2 Minimizing the Test Power Consumption:

Decreasing the switching activity is one of the major contributors to reducing the power consumption during testing. Hamming Distance i.e. the calculation of test vectors such that their bits are incompatible ignoring the don't cares minimization between successive test vectors needs to be minimized for decreasing power consumption [19]. In general, the total switching power in the whole circuit is proportional to the hamming distance of input test vectors. Hence we perform double reordering before applying any suitable test data compression technique to the test data.

Scan in power is influenced by the manner in which the don't cares in the original test set data Td are mapped to binary values. While Pavg and Ppeak can be minimized by choosing an appropriate mapping, such a mapping is not guaranteed to provide high test data

compression as well as reduced transitions during scan in [20]. Even though we do not directly address scan out power, our experiments with benchmark circuits show that this approach reduces the number of transitions and the resulting WTM during scan out. This is an added advantage of using encoded test sets for scan testing. Scan out vectors are dependent on the scan in vectors and the relationship between the two depends on the function implemented by the circuit under test (CUT). Determining the effect of filling don't cares cubes on the scan out vectors require circuit simulation.

There are various techniques for filling don't cares. Zero fill is mainly effective when we employ golomb code for test data compression. Random fill introduces negative compression [22] as it increases the number of bits in the encoded test set data. Column wise bit stuffing [21] is an approach which when used with difference vector increases the compression ratio to a greater extent compared to other X's filling approaches discussed earlier for most of the circuits. MT-Fill introduces the concept of minimum transition filling where the previous bit value is compared with successive bit and then decision is taken to assign an appropriate value to don't care.

Each of the above mentioned techniques has its own disadvantages and advantages. Depending on the benchmark circuit and the technology available, there has to be a suitable decision to be taken for achieving optimum compression of test data along with minimum power consumption.

CHAPTER 3

DOUBLE REORDERING SCHEME AND 10C ENCODING MECHANISM ON THE REORDERED TEST DATA

This chapter focuses on the proposed scheme for test data compression and test power minimization. As can be seen from Fig 3.1, select the test vector size according to the benchmark circuit. Then, assign the test vector into respective block sizes of 8. On applying 10C Coding scheme, we get encoded test set data of 72 bits i.e. 18.18% compression ratio. On applying 9C coding scheme, we get encoded test set data of 85 bits i.e. 0.68% and if we apply 9C on some circuits and 10c on others, in that case decoder design circuitry would be highly complex thereby leading to an increase in decoder area. On comparing with variable 9C results, we infer that optimum compression has been achieved for smaller values of K say for 8, 12,16. For higher values of K, there is a noticeable drip in compression ratio. There has also been an experimental study carried out with different value of L's along with Variable K. But tuning for each test pattern posed challenge for extreme values of L. Moreover, there has been a drip in compression ratio as well. Hence, increasing the on chip decoder area wasn't worthwhile. Figure 3.2 shows a brief outline of the proposed scheme.

Apply hamming distance based reordering scheme on the test data to get the reordered test set. Calculate average and peak power using the given formulae. Then, applying modified 10-C coding on the reordered test set by first checking for the count of no. of zeroes and ones. If count of zeroes >8, then assign detect bit equal to 1 else detect bit is equal to 0. Then,performrun-length encoding with necessary modifications in run lengths of 0's and 1's on the test data according to Table 3.2. Repeat the above steps for run length of ones. Finally, scan in the data through the decoder to get the final result.

Flow-Chart

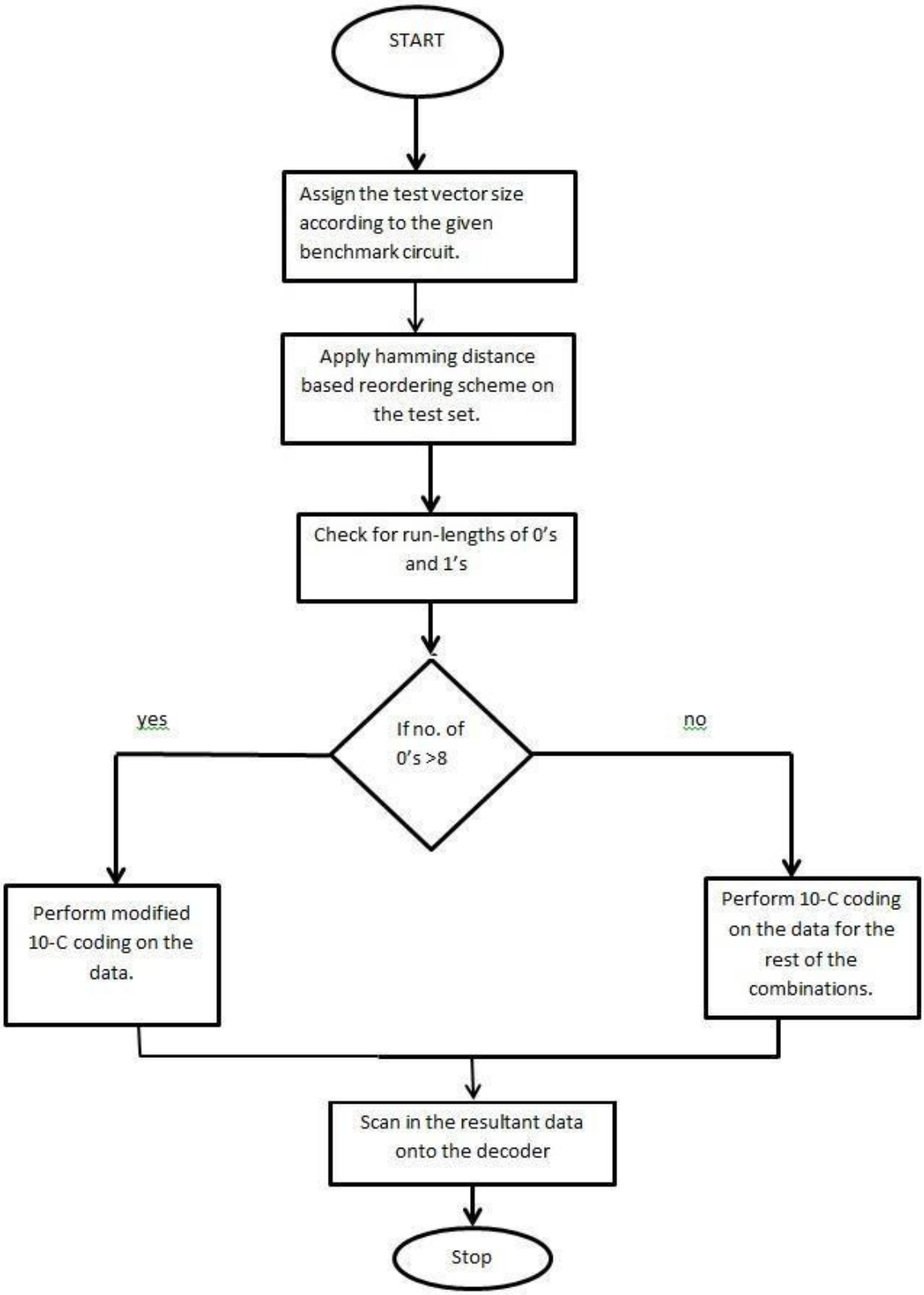

Fig 3.1: Flow chart of the proposed technique

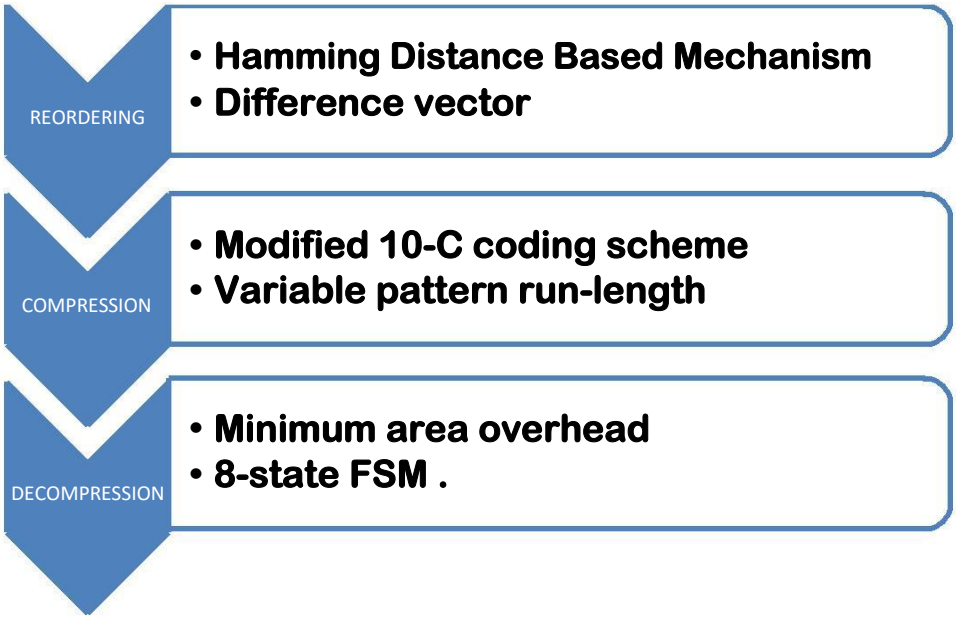

Fig: 3.2 Proposed Scheme Model

3.1 Test data Analysis

We have minimized the total hamming distance here as shown in fig 3.2 Total hamming distance is defined as the Sum of hamming distance between successive test vectors in the sequence. Let hamming distance d [ti,tj] be the total number of changes between ith and jth test vector. Total hamming distance can be calculated by the following formula:

$THD = \sum_{i}^{n-1} d[tj,t_{j+1}]$

Assume we have the following test data of 56 bits as shown in Fig. 3.3.

10XX10110XXX11001XX0X101X01
1XXXXX001110111XX00001111XX
XX

Fig 3.3 Original Test data

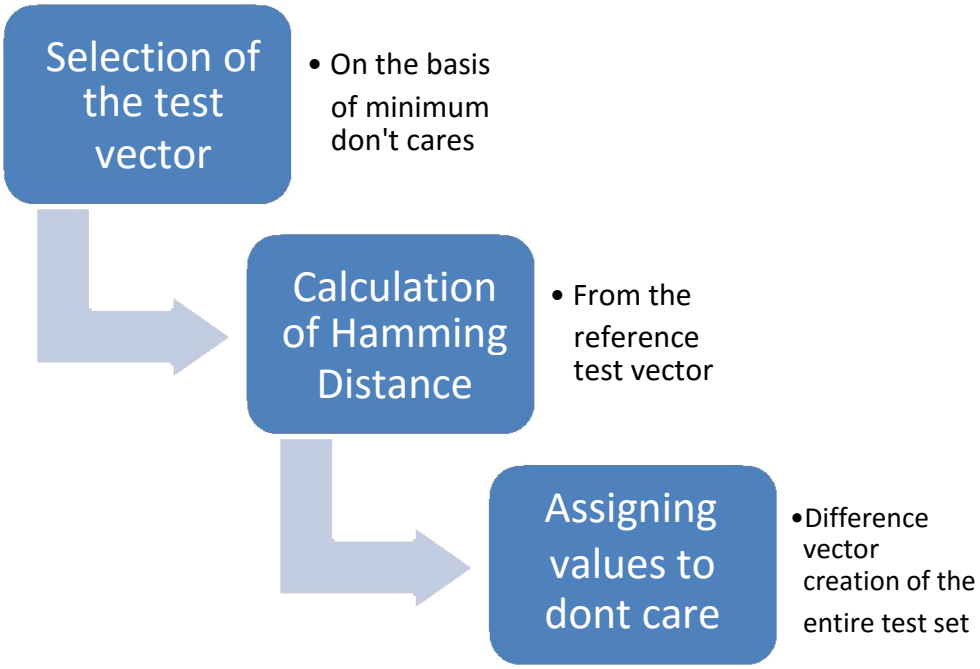

Fig. 3.4 Reordering Mechanism

This can be divided into 7 vectors of 8 bits each as depicted in fig 3.5.

T1: 10XX1011
T2: 0XXX1100
T3: 1XX0X101
T4:X011XXXX
T5: X0011101
T6: 11XX0000
T7: 1111XXXX

Fig.3.5 Rearranged test vectors

Here we have calculated the hamming distance wrt. T1. Hamming distance basically compares each consecutive bit in both the test vectors ignoring the don’t cares. Then, we add them each bit by bit.

Hamming distance calculations show that we have varying distances in terms of don't cares as shown in table 3.1.

T1 (10XX1011)	T2 (0XXX1100)	4
T1 (10XX1011)	T3 (1XX0X101)	2
T1 (10XX1011)	T4 (X011XXXX)	0
T1 (10XX1011)	T5 (X0011101)	2
T1 (10XX1011)	T6 (11XX0000)	4
T1 (10XX1011)	T7 (1111XXXX)	1

Table 3.1: Hamming Distance

Rearranging the test vectors in their ascending hamming distance we get Fig 3.6.

T1: 10XX1011
T4: X011XXXX
T7: 1111XXXX
T3: 1XX0X101
T5: X0011101
T2: 0XXX1100
T6: 11XX0000

Fig 3.6 Reordered test vectors

Filling first test vector according to minimum transition,

T1: 10001011

And the rest of the test vectors according to T1, we get

T4: 10111011

T7: 11111011

T3: 11101101

T5: 10011101

T2: 00011100

T6: 11010000

Hence, this technique leads to minimum hamming distance based reordering technique [23]. Minimum transition between the test vectors leads to reduced switching and hence reduced dynamic power, which is the major source of power consumption.

Also, such a reordered test set data also leads to increased compression efficiency when applied with a suitable run-length code.

3.3 COMPRESSION SCHEME ON REORDERED TEST DATA

3.3.1 Comparison of the various run length based codes:

On applying the various run length based codes on the example mentioned above, negative compression ratio has been observed. There have been a dramatic increase in the compression ratio of few ISCAS's Benchmark circuits which have a large run's of 0's and 1's. However, same scheme applied on other circuits' yields negative compression[24] which is undesirable. Exampleshown below shows the no. of bits after compression. Hence, on comparing various compression schemes, 10 C coding scheme looks more suitable.

In 10C coding scheme, input block of 8 bits(K = 8) each has been taken. For each unique case there is a unique symbol assigned to it for example – 10, 01, UU…etc. Next column starts with the prefix bit which is 1 bit long [26]. For cases other than UU,UU',UV prefix bit is assigned the value 0.For rest of the other cases, tail bit is also assigned since it consumes less test data. Moreover the three aforesaid test cases already consume more no. of bits in total code word.Instead of the sub-prefix bit, we have the tail bit (3 bits) assigned to them. Then the final decoder input is combination of prefix, sub-prefix (if applicable) and tail bit. There is a marked decrease in the no. of bits for decoder input when 10C is applied as compared to 9C [26] especially for unique cases whose probability of occurrence is also higher thereby improved compression ratio.

On the other hand, one of the major drawbacks of 10C encoding scheme is that the no. of bits in code word for test cases 00 and 11 are invariably larger as compared to 9C. Moreover, there is a high rate of occurrence of large runs of 0's and 1's. But 9C poses the hindrance as it uses large amount of bits for unique cases even more than the no. of bits in the test case i.e. 12 bits for 8 bit test data. So, overall either one of the two cannot be applied on all the circuits.

Here, modified 10C is incorporated in such a way as shown in fig 3.5 that variable block size is considered for the test data.

Combinations	Detect bit	Block size	Codeword	Length
All 0’s	0	8	00	3
	1	9	0000	4
	1	10	0001	4
	1	11	0010	4
	1	12	0011	4
	1	13	0100	4
	1	14	0101	4
	1	15	0110	4
	1	16	0111	4
All 1’s	0	8	11	3
	1	9	1000	4
	1	10	1001	4
	1	11	1010	4
	1	12	1011	4
	1	13	1100	4
	1	14	1101	4
	1	15	1110	4
	1	16	1111	4
01	0	8	01	3
10	0	8	10	3
1U	0	8	100UUUU	7
U1	0	8	101UUUU	7
0U	0	8	110UUUU	7
U0	0	8	111UUUU	7
UU	0	8	010UUUUUUUU	11

Table 3.2 Modified 10-C coding implementation

In the table 3.2, length of the code word is reduced to a maximal extent as compared to previous techniques. There are unique code words assigned for each and every possible combination in the test data set as can be inferred from column 4. A detect bit is used to

justify the choice of pattern length for block size greater than 8 such that for number of zeroes greater than 8 modified 10C coding can be employed. Then the final compressed test data is scanned onto the decoder. Decoder is composed of various blocks in such a manner so as to scan in the test vectors onto the scan chains in the best way possible.

Assume the reordered test data in fig 3.8

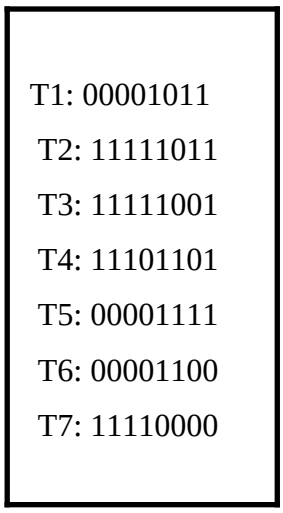

Fig 3.8: Reordered test data for compression

After applying Modified 10C coding scheme:

Compressed test data:

00101101101101100011110100110100110010 0

Considering the example, the total test data has been reduced to 39 bits from 56 bits. Hence achieving 30.35% compression ratio.

Decoder Architecture:

The design for the basic architecture of the decoder has been depicted in fig 3.7, where the benchmark circuit after compression provides the input data. The data is scanned in bit by bit via an input port during testing. Decoder has been designed in CADENCE and Xilinx and area calculations have been done accordingly using the report area command.

The decoder consists of four counters namely one for counting the no. of times run length of zeroes and ones has been considered with each unique pattern length. There is a separate

counter to keep track of no. of times the pattern length is taken as 8. And first counter is meant to utilize the eight states of FSM which have been formed as a result of eight code words C0- C8. And for pattern length greater than 8,we have a separate counter keeping track of the occurrences namely C9-C15.

It also comprises of p multiplexers to select the final decoder output. The inputs to the multiplexer are the input bit and the detect bit. If the pattern length is 8, then our detect bit is 0 else 1. For detect bit =1,there are separate eight code words for run lengths of 0's and 1's. The Decoder Area Overhead (DAO) calculation has been carried out by the formula as given by eq. 3.3.

DAO = (Area of Decompressor/Area of Benchmark Circuit) X 100 % (3.3)

Overall, there has been a significant improvement in reducing the number of transitions between successive bits. This has resulted in dynamic power reduction which mainly depends on switching activity in the input data stream. Test data compression is also considerably achieved on applying the above mentioned compression scheme since number of consecutive 1's and 0's are inevitably larger in number as compared to the rest of the combinations.

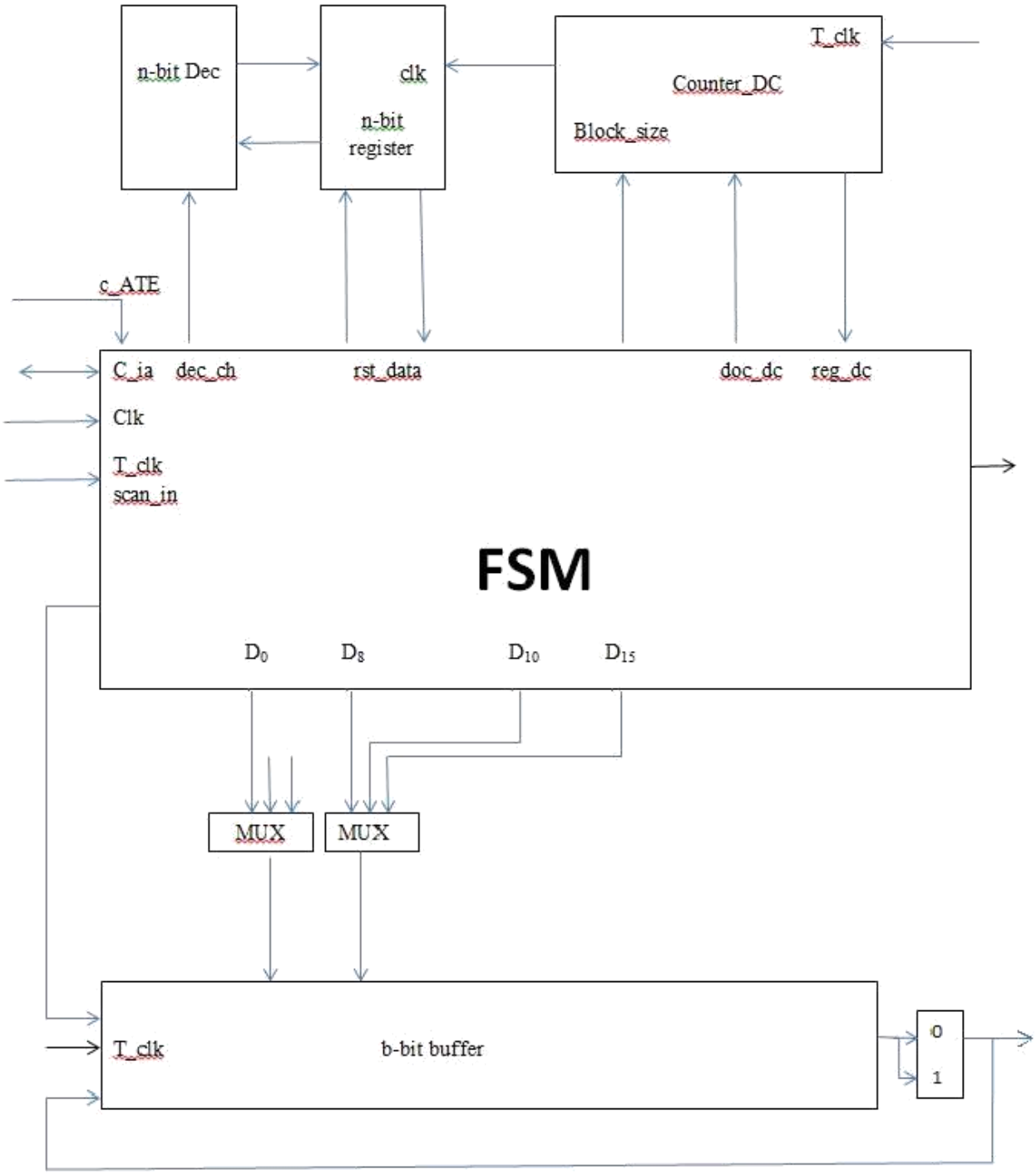

Fig. 3.7 Block Diagram of Decoder

CHAPTER 4

RESULTS AND ANALYSIS

The tests were performed on the test data of five benchmark circuits. First of all, reordering had been performed for reduced Hamming Distance, thereby saving the test power. For incorporating variable length 10-C coding on the test data, first it needs to be verified that till how much block length should be considered for efficient compression to be achieved also taking into account area overhead. Hence, a careful comparative study has been carried out for all the circuits counting their 0's and 1's for block length 8,12,16,24 and 32.

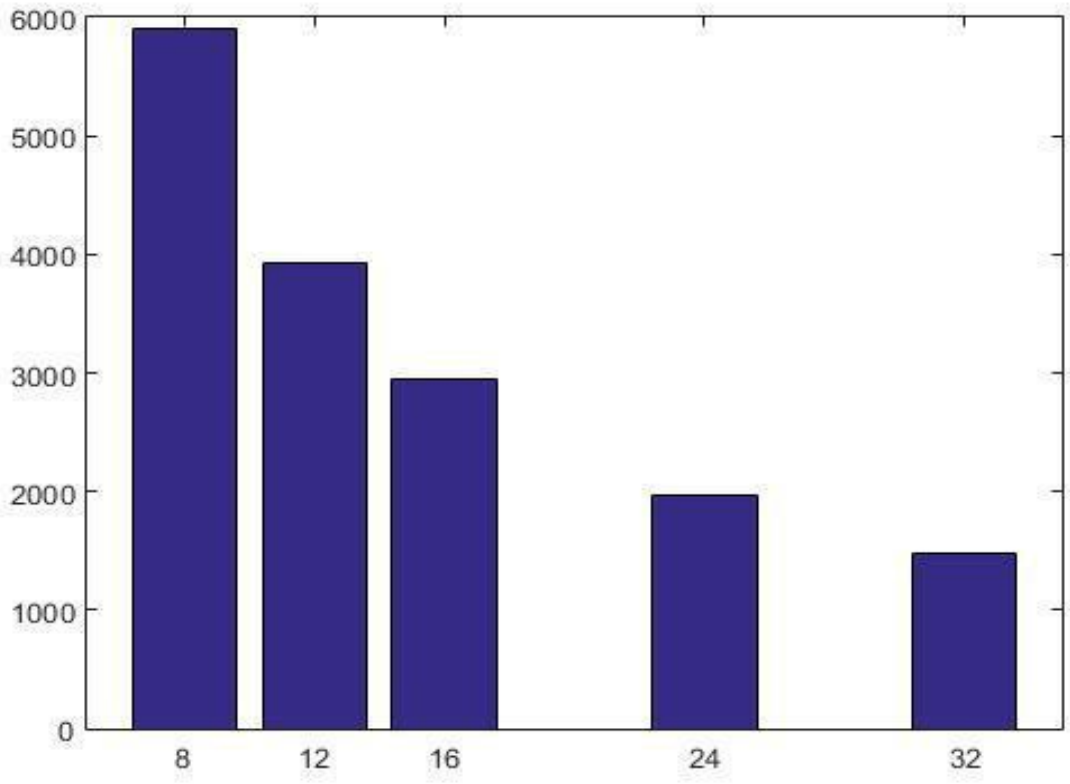

Fig. 4.1(a): Number of 1's for circuit s15850

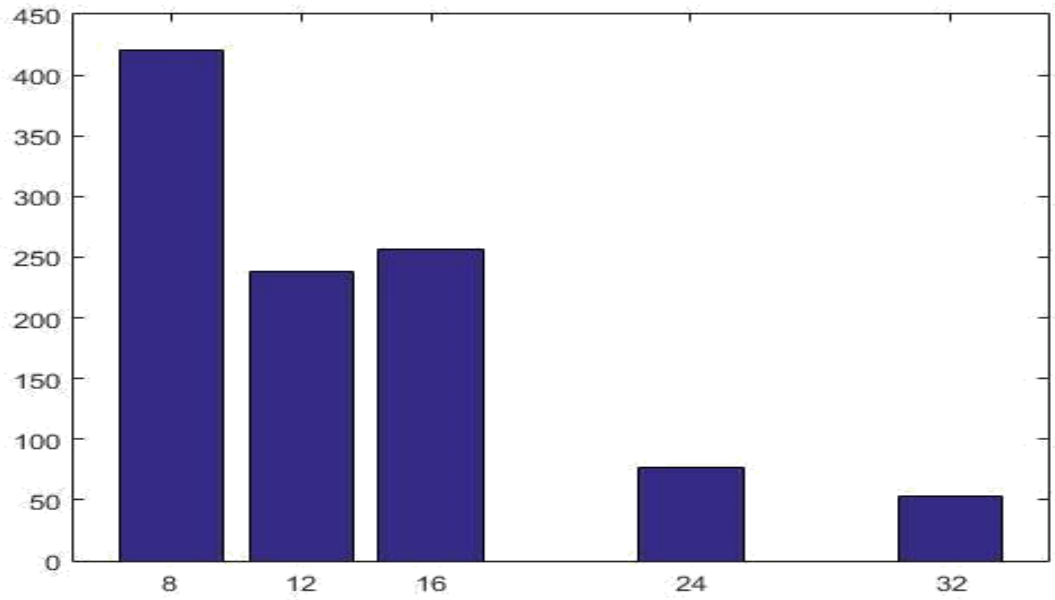

Fig. 4.1(b): Number of 0's for circuit s15850

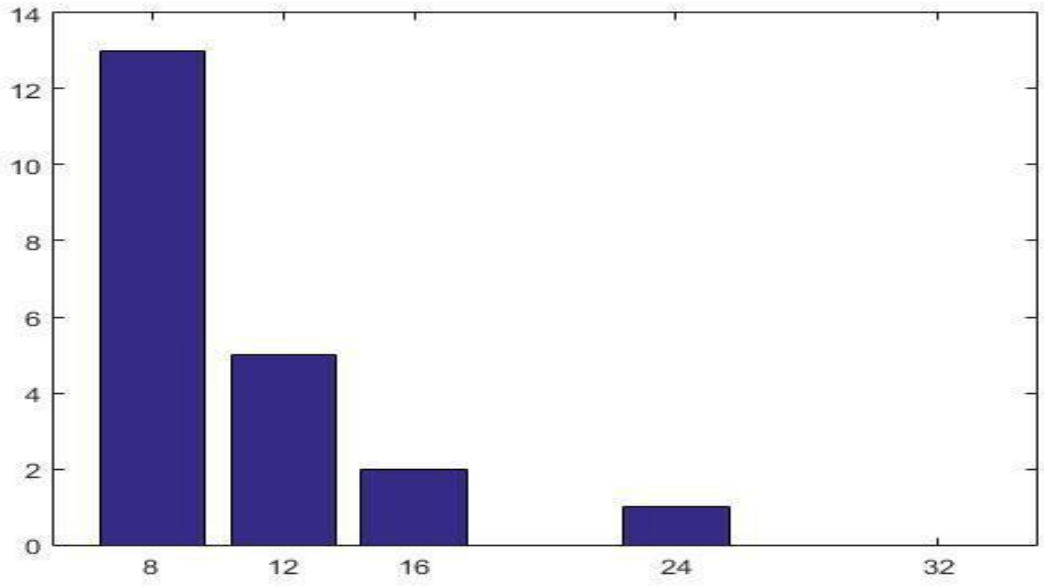

Fig. 4.2(a): Number of 1's for circuit s9234

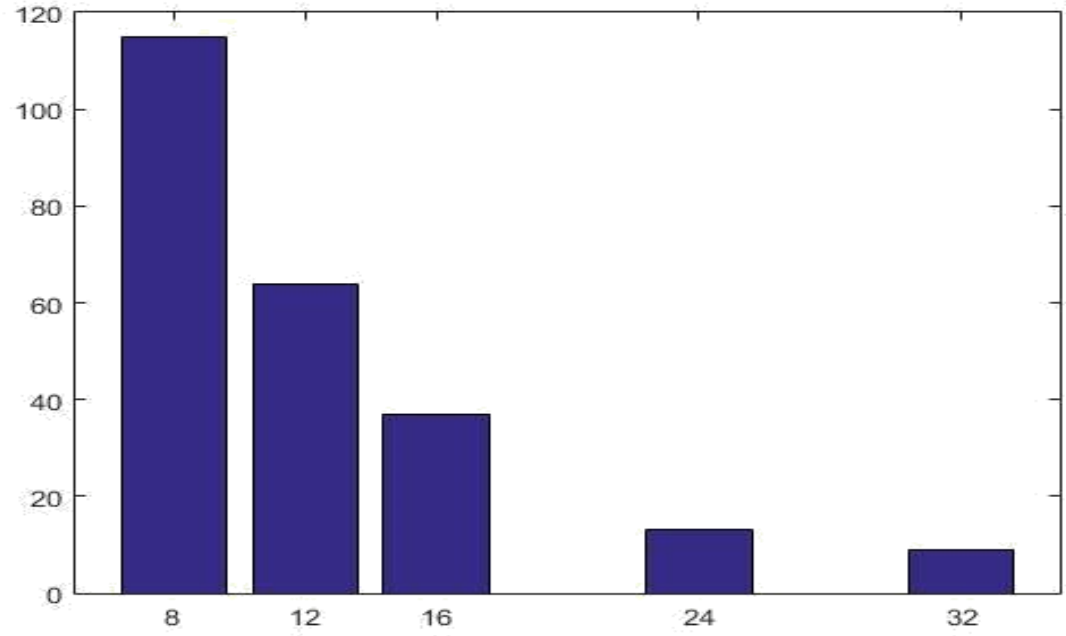

Fig. 4.2(b): Number of 0's for circuit s9234

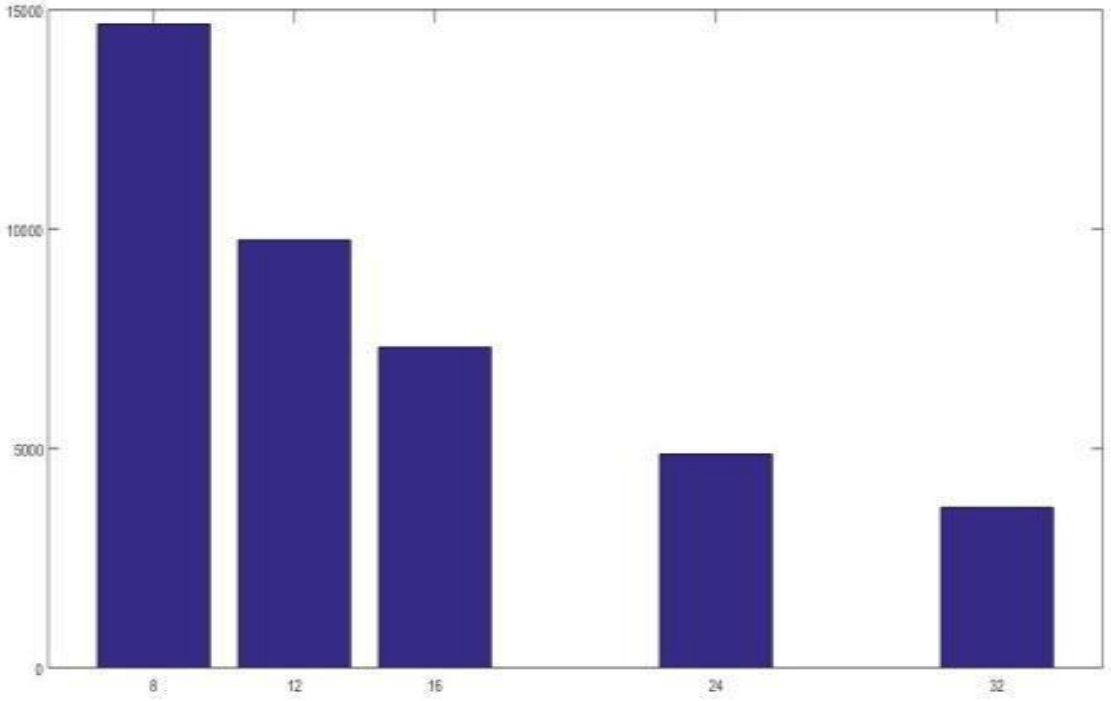

Fig. 4.3(a): Number of 1's for circuit s38584

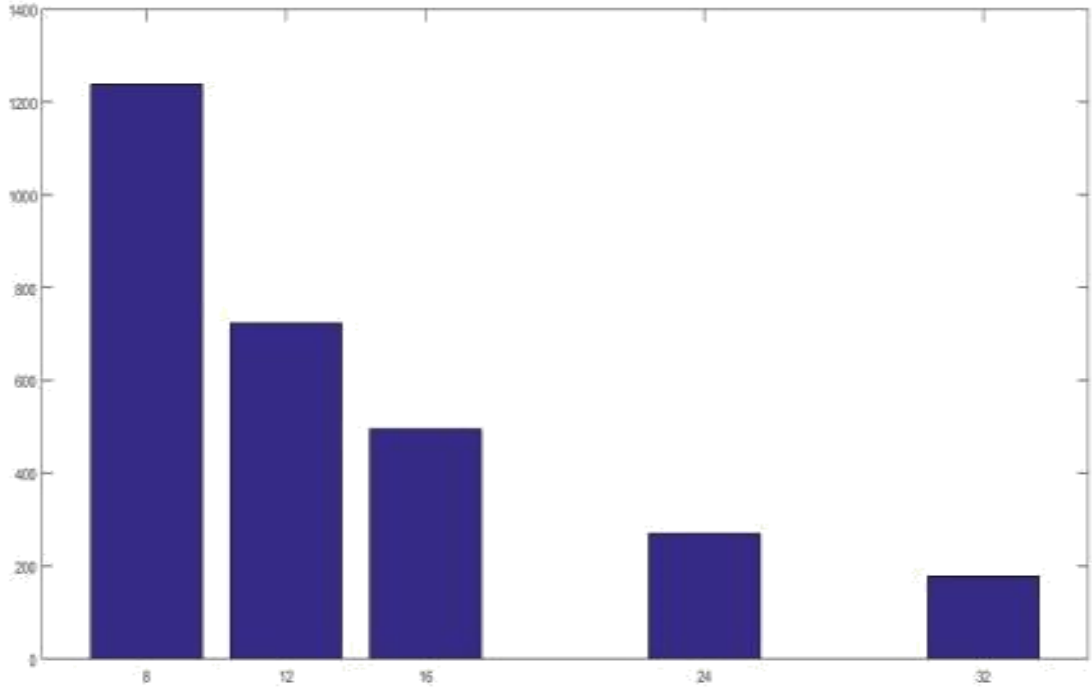

Fig. 4.3(b): Number of 0's for circuit s38584

Based on the observations from the occurrences of 0's and 1's as shown in Fig 4.1,4.2 and 4.3 for different benchmark circuits, it has been inferred that there has been frequent run lengths of 0's and 1's up to block length 16. That's why variable pattern has been taken maximum upto 16 only, thereby reducing the extra area overhead in accounting for more block length. Upto block size 8, there hasn't been a considerable variation but, above 8 we have considered the run length of consecutive zeroes and ones.

On applying the below mentioned formulae for Peak and Average power [25] given in eq. 4.1 and 4.2, Matlab results for ISCAS 89 Benchmark circuits are given in table 1.2.

$$P_{peak} = \frac{max.}{j \in \{1,2....n\}} . \{\sum_{i=1}^{l-1} (l-i)(t*j, i \otimes t*j, i+1)\} \quad (4.1)$$

$$P_{avg} = \frac{\sum_{j=1}^{n} \sum_{i=1}^{l-1} (l-i)(t*j,i \otimes t*j,i+1)}{n} \quad (4.2)$$

Where, *n* stands for the number of test vectors.

l and *i* are the positions associated with each vector.

Inferring from the above statistics, there has been a considerable reduction in peak power and average power consumption while testing the SoC as shown in table 4.1.

Circuit	Average Power(%) [17]	Peak Power
S5378	37.2%	82%
S13207	34.8%	78.3%
S15850	45.2%	73.5%
S35930	35.2%	76.4%
S38417	47.6%	79.2%

Table 4.1: Results for average and scan power

Table 4.1 shows that there has been a significant decrease in the overall power consumption in terms of both average and peak power. There has been quite a significant change in peak power due to focusing on the fixed block size of 8 bits at a time according to the benchmark circuit.

Comparison of Test application time achieved for modified 10C coding scheme with other compression techniques in terms of the average and peak power have been tabulated below as under in Table 4.1 and fig 4.2. As can be seen from the table 4.2, there has been an appreciable decrease in the average power consumption while applying double reordering technique. There hasn't been any change while applying Zero filling and then Xoring the bits as compared to Run- based bit fill technique. Column wise bit stuffing filling mechanism somewhat gives an improved result compared to the previous two techniques. Minimum transition fill has been employed in double reordering but, it also takes into account the additional hamming distance thereby leading to significant improvement in average power consumption.

ISCAS circuit	MT-Fill	Zero fill +xor	Run based bit fill	HDR CBF DV	**Double reordering**
S5378	3433	3526	3526	4589	**3102**
S9234	3958	4022	4022	5322	**3462**
S13207	7735	7887	7887	8213	**7004**
S15850	13514	13659	13659	14542	**12985**
S38417	117540	118080	118080	127582	**110283**

Table 4.2: Comparison of results for Average Power.

Circuit	MT-Fill	Zero fill +xor	Run based bit fill	HDR CBF DV	**Double reordering**
S5378	11519	12085	12085	13327	**10894**
S9234	14092	15395	15395	17828	**13752**
S13207	94879	110129	110129	128638	**92421**
S15850	70875	84360	84360	96084	**68955**
S38417	437884	514716	514716	644262	**426588**

Table 4.3: Comparison of results for Peak Power

As can be seen from the table 4.3 given above, there has been an appreciable decrease in the peak power consumption while applying double reordering technique. There hasn't been any change while applying Zero filling and then xoring the bits as compared to Run- based bit fill technique. Column wise bit stuffing filling mechanism somewhat gives an improved result compared to the previous two techniques. Minimum transition fill has been employed in double reordering but, it also takes into account the additional hamming distance thereby leading to significant improvement in peak power consumption.

In order to validate the efficiency of the proposed modified 10C technique, diverse experiments on the five large full scanned ISCAS'89 benchmark circuits have been accomplished. Test sets generated by Mintest [11] ATPG with dynamic compaction are applied for test data compression and the results have been compiled in table 4.4.

Circuit	Test data	Block size= 8	12	16	24	32	**Variable 10C**
S5378	122532	105674	119754	117896	121890	121657	**113728**
S9234	139283	116573	123765	126594	107389	114787	**128675**
S13207	1165200	989533	749032	1102782	1108743	1146341	**121595**
S15850	176993	141790	154524	136582	128986	149654	**130592**
S38417	183462	163673	157842	148599	174511	170782	**159405**

Table 4.4: Compression results of variable 10-C coding

From the above table, it can be seen that there is a marked decrease in the number of bits as we go on increasing the block size subsequently at each level. Column 8 depicts that with variable size of the blocks, there has been a significant decrease in the number of bits with much less complexity associated with the decompressor circuit. Moreover, in the previous columns, there has been a fixed block size in which case many of the repetitive code words get neglected leading to reduced compression ratio being achieved in the previous techniques.

Circuit	Total area	Extra area
s5378	125675	0.069727472
s9234	152144	5.759675045
s13207	310428	2.822876802
s15850	335076	2.61522759
s38584	438320	1.999224311

Table 4.5: Decoder area calculations

Table 4.5 draws the fact that with a little increase in the area overhead associated with the decoder circuit, there is significant test data volume reduction along with test power consumption. The average increase in the area overhead is about 2.6531%.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE:

5.1 CONCLUSION:

The results of the calculations based on the proposed technique using two-step process of first double reordering followed by modified 10C coding scheme for compression have been presented in Chapter 3. The total power consumption has been reduced significantly with the average power being reduced to 38.6% and peak power to 80.82%.

Since it has been assigned the don't cares possible values according to the reordering being performed as a result on applying modified 10C coding scheme we achieve the average compression ratio as 49.18%. Hence, we have achieved a balance between the two main primary concerns i.e. the test data volume and the test power consumption associated while testing of SoC. Although, there is somewhat extra cost incurred associated with area overhead in implementation of the decoder to achieve high compression ratio and low test power.

5.2 FUTURE SCOPE:

The research work proposed in this thesis presents a modified 10C coding compression scheme which shows better comparable results to the existing techniques. It has tendency to reduce the compression as well as the test power along with easy implementation of the decoder. Its implementation to large benchmark circuits efficiently proves its niche. Along with applications in the field of testing, it can be applied in domains having large amount of test data. The future advances in this field can optimize testing of complex circuits at a reasonably easy level without having to compensate on the huge test power or area overhead.

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