A

Thesis Report

On

"DESIGN AND IMPLEMENTATION OF ALL DIGITAL PHASE LOCKED LOOP"

Submitted towards the partial fulfilment of requirement for the award of degree of

Master of Technology

In

VLSI DESIGN

Submitted By:

Prince Prabhakar

Roll No: 601562018

Under Supervision of:

Dr. Alpana Agarwal

Associate Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

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DECLARATION

I, Prince Prabhakar hereby declare that the work presented in this thesis entitled "DESIGN AND IMPLEMENTATION OF ALL DIGITAL PHASE LOCKED LOOP" in partial fulfillment of the requirement for the award of degree of Master of Technology in VLSI DESIGN submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of Dr. Alpana Agarwal (Associate Professor, ECED, Thapar University) from 2015 to 2017. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Prince Prabhakar
601562018

Date: 11/8/17
Place: TU, Patiala.

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Dr. Alpana Agarwal
Associate Professor, ECED
Thapar University, Patiala

Date: 11/8/17
Place: TU, Patiala

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The study has indeed helped me to explore knowledge and avenues related to my topic and I am sure it will help me in my future.

ABSTRACT

Phase Locked Loops (PLLs) are widely used in clock recovery and frequency synthesis. Fully Digital PLLs are more suitable for the monolithic implementation with other circuits compared to the traditional implementations of the PLLs. The All Digital PLLs are also independent of process variations and can be easily ported to different technologies.

This thesis presents the design of an All-Digital Phase Locked Loop (ADPLL) using a twin Vernier delay line based time to digital converter and an All-Digital Lock Detection and Control Unit (ADLDC). General design criteria are summarized for the all-digital implementation in comparison to the traditional approaches and analog implementations. The design has been implemented using $0.18\mu m$ CMOS technology. The ADPLL can operate in the frequency range between 230 MHz and 1.118 GHz the ADPLL has a lock time of $1.768\mu s$. The simulation results of the ADPLL are also presented to verify its operation.

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LIST OF GLOSSARY

APLL	*Analog Phase Locked Loop*
ADPFD	*All Digital Phase Frequency Detector*
ADPLL	*All Digital Phase Locked Loop*
APR	*Automatic Place and Route*
ASIC	*Application Specific Integrated Circuit*
CCO	*Current Controlled Oscillator*
CLK	*Clock*
CMOS	*Complementary Metal Oxide Semiconductor*
CPPLL	*Charge Pump Phase Locked Loop*
CU	*Control U nit*
DAC	*Digital to Analog Converter*
DCD	*Duty Cycle Distortion*
DCO	*Digitally Controlled Oscillator*
DCPLL	*Digitally Controlled Phase Locked Loop*
DDFS	*Direct Digital Frequency Synthesizer*
DDS	*Direct Digital Synthesis*
DPLL	*Digital Phase Locked Loop*
OUT	*Device Under Test*
EXOR	*Exclusive OR*
FF	*Flip Flop*
FIFO	*First In First Out*
FTW	*Frequency Tuning Word*
IC	*Integrated Circuit*
ID	*Increment Decrement*
LPF	*Low Pass Filter*
LPLL	*Linear Phase Locked Loop*
LSB	*Least Significant Bit*
MSB	*Most Significant Bit*
NCO	*Numerically Controlled Oscillator*
NMOS	*N Type Metal Oxide Semiconductor*
NRPD	*Nyquist Rate Phase Detector*
PA	*Phase Accumulator*
PADDFS	*Phase Accumulator DDFS*
PO	*Phase Detector*
PFD	*Phase Frequency Detector*
PLL	*Phase Locked Loop*
PMOS	*P Type Metal Oxide Semiconductor*
ROM	*Read only Memory*
RST	*Reset*
RTL	*Register Transfer Level*
SPLL	*Software Phase Locked Loop*
SRFF	*Set Reset Flip Flop*
STC	*Single Time Constant*
SYNC	*Synchronization*
VCO	*Voltage Controlled Oscillator*
VLSI	*Very Large Scale Integration*

CHAPTER 1 INTRODUCTION AND OVERVIEW

1.1 INTRODUCTION

Phase Locked Loops (PLLs) [1] are feedback systems that generate signals that are phase locked with external input signals. PLLs are used to generate an output signal whose frequency is a programmable, rational multiples of a fixed input frequency. In other words, PLLs are used to lock or track input signals in frequency and phase. When the phase and frequency of the input signals are synchronized, the PLL is said to be in the locked condition. The phase difference between the output signal and the reference is a known value when the loop is locked.

Phase Locked Loops are used for applications such as clock recovery, motor speed control and frequency control of communications equipment. PLLs are widely used in modern communication systems and high performance microprocessors because of their remarkable versatility. PLLs are also used in frequency modulation, demodulation as well as to regenerate the carrier from an input signal in which the carrier has been suppressed [2]. In communication applications, PLLs are used to make local clocks synchronous with other signals.

Consider a scenario in which two systems with no external handshaking signals are synchronized to the same clock [3]. The two systems may be out of synchronization if the local clocks deviate from each other. Figure 1.1 shows two systems, System A and System B synchronized to a global timing reference f_{osc}.

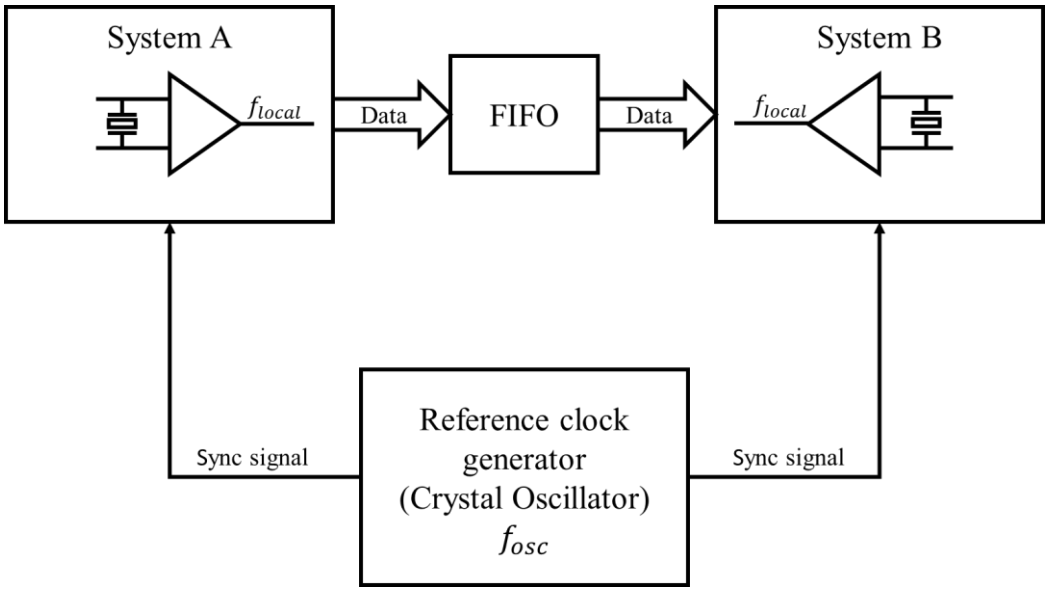


Figure 1.1 Two Systems Synchronized to the same clock

The jitter between the two systems A and B operating at the frequency, f_{local} makes the First in First out (FIFO) buffer fluctuate when transmitting data between the two systems.

Therefore in a complex system made up of many synchronous devices, it is often necessary to distribute the clock to one or more devices. This leads to problems such as clock jitter, synchronization and clock skew. It is probable that the individual devices also

operate at different clock frequencies. Thus the Phase Locked Loops find a variety of applications including clock skew/jitter suppression, clock distribution and clock synchronization.

1.2 MOTIVATION

The conventional PLLs use analog techniques and the classical digital PLLs use a combination of analog and digital techniques to achieve robust operation. However, integrating an analog PLL in a digital noisy environment is difficult. The digital switching noise coupled through the power supply and substrate causes considerable noise in the noise-sensitive analog circuits. The Analog PLL (APLL) is also sensitive to process variations and must be redesigned for each new process. Advances in all digital implementations of the phase locked loops [4] offer enhanced functionality and flexibility.

The All Digital Phase Locked Loop (ADPLL) has better portability and can be used in system on a chip applications and is independent of process variations. It also minimizes the design cost and time. Further, with the use of this new architecture based on twin VDL based time to digital converter, the output frequency, phase and amplitude can be precisely manipulated under digital processor control.

This thesis will focus on the design of a PLL using digital methodologies. As the feature size of the VLSI technology continues to shrink, fully integrated digital techniques will be more scalable and portable in many applications than their analog counterparts.

1.3 SCOPE OF THESIS

1.3.1 ADPLL Requirements

The purpose of this work is to design an All-Digital PLL that replaces the blocks of previous ADPLL's by new digital blocks that can achieve faster lock time and operate at frequencies between 200 MHz to 1 GHz.

1.3.2 Literature Review

An extensive literature search has been performed for papers dealing with the design of Phase Locked Loops.

R.*C.* Den Dulk *et al.* (1988) [5] a simple DLD circuit was used in the direction to differentiate the unlock state of a PLL. A sequential phase detector was used in this, such as the three-state phase-and-frequency detector or the phase detector for S/R flip-flop. In support of normally worn benchmark PLL IC 4046, the proposed path could the same as the sense unbolt in the case of via the previous (multiplying) XOR-PD, since incident of sequence slips was used as a description of phase lock and this was mainly in the main probably helpful description of phase lock because cycle-slipping positively intimates that the PLL was at times out-of-lock and certainly allowed a circumstances during which the well-known linear approximated PLL model was not applicable.

Shi Hao and Yan Puqiang *et al.* (1991) [6] in this paper a novel type of DPLL was offered, which reposed a frequency multiplier, a personalized 9-gate phase detector as well as a loop Blter-all executed in DH devoid of any analog module. Main recompenses of the future DPLL were i) For time ramp input signals no steady-state frequency tracking error , ii) high lock-in speed, and iii) simplicity of organism integrated into a particular chip**.**

Seog-Jun Lee *et al*. (1997) [7] Abundant MPLLFS path executed in a criterion 0.8-µm CMOS expertise was described. Every ambit in the synthesizer employs discrepancy methods through the digital sections considered by static logic so that system would be noise immune. New VCO has an inside frequency of 800 MHz in addition to a tuning range of ±25%.The frequency range of completion of measured frequency synthesizer was 700 MHz to one GHz with −80 dBc/Hz phase noise at a 100 KHz carrier offset. The test chip expends 125 mW at highest frequency from a 5 V supply with an active area of 0.34 mm^2. Provided DCC plus a PF were the only external components.

Tzi-Dar Chiueh *et al. (*2001) [8] this paper had described how a novel FS based scheduled combined the ADPLL and the analog PLL. High frequency resolution, high switching speed, broad frequency range, and low supply voltage were achieved by the frequency synthesizer. Both the digital control word and the control voltage of the analog PLL were used to control oscillator. Using a symmetric load differential inverting buffers array oscillators were implemented which gives improved denunciation to supply noise and fabrication variance. To improve the separator resolution without inducing jitter, FND and DI methods were engaged. To uncover appropriate digital frequency control word a BSA was pre-owned, which be able to store for afterwards pre-owned plus significantly speed up the frequency switching procedure. They had also created a 0.6-µm SPTM CMOS technique, in which the synthesizer accomplished a recurrence scope of 54–154 MHz with a recurrence mistake under 1 ppm and a recurrence exchanging time under 10 µs. Approximately no power and draws 47 mW from a 2-V supply voltage was consumed by chip.

Shinwoong Kim *et al.* (2016) [9] in this paper a synthesized 2 GHz fractional-NADPLL with a dual-referenced interpolating time-to-digital converter (TDC) was presented. By referencing adjacent two integer phases the proposed TDC measures fractional phase achieved and without any calibration scheme achieves gain matching. Improvement in linearity with little sensitivity to process, temperature variations and voltage by averaging nonlinearity errors of differing polarities was achieved. Apart from digitally controlled oscillator (DCO), PLL was intended only by RTL-level behavioural descriptions and synthesized with a standard cell library. PLL was executed in 65 nm CMOS with an active area of *0.*047 m^{m^2} plus achieved a stable in-band phase noise of lower than −100 dB*c/*Hz in a extensive collection of supply voltage from 1 to 1.4 V.

Kwang-Hee Choi *et al. (*2009) [10] by utilizing the interpolation scheme at both the coarse and fine delay blocks of the DCO, a carefully controlled oscillator DCO a digitally controlled oscillator (DCO) for the all-digital phase-locked loop (ADPLL) and the high frequency was proposed. Two ladder-shaped coarse delay chains were present in the coarse block. First's delay was an odd multiple of an inverter delay and the

second's was an even multiple. At the second coarse defer chain an introduction method was performed, which successfully reduced both the delay range of the fine block to half and the resolution of the coarse delay block. By this output frequency of the DCO increased the maximum. The ADPLL with the future DCO was invented in a 0.18 µm CMOS prepared with the dynamic region of 0.32 mm2. Output frequency of the ADPLL were in the range from 33 to 1040 MHz at the supply of 1.8 V. Measured rms and peak-to-peak jitters were 13.8 ps and 86.7 ps, correspondingly, at the output frequency of 950 MHz. 15.7 Mw power was consumed.

Won Namgoong *et al.* (2010) [11] in this paper, to utilize the growing transistor speediness of recent procedure skill, a DPLL had been refined. With applying a DCO and a TDC, the LF of a DPLL alter to all-digital. Alternatively scheming of the LF with digitizing a CTLR since had been normally ended, additional complicated organize methods could be engaged. It planned to intend the FL in the time-domain through initial modelling the DCO and TDC as a strident "plant" in state-space form. Seeing the Kalman observation of the "plant," the future moved towards after that generates OCS that precisely report intended for the preservative blare in addition to the TD inside the digital feedback system. Future OCLF will achieve quick transient response time as well as appreciably diminishes the SSPNJ related to the conventional DPLL. Moreover, the future loom enable modelling of previous noise sources such as appropriate to oscillator pulling, which was a general trouble in numerous modern transceivers. With using the OCLF, the outcome of oscillator pulling was able to successfully separate devoid of corrupting taken as a whole phase noise recital.

Chia-Tsun Wu *et al.* (2010) [12] in this paper a FEA for an (ADPLL) as a substitute of the BSA algorithm was presented. Depending on a new fast-lock scheme and the future FEA, a fast-lock engine was intended to advance the lock-in time of an ADPLL intend with two referenced clock cycles. Execution of the future ADPLL intend was reels in by exertion UMC 0.18-μm1P6M CMOS equipment with a core area of 300 × 250 μm2, reposing of an adequate input reference clock ranging from 220 kHz to 8 MHz. Frequency collection is 28–446 MHz for ADPLL design with an 8.8-ps DCO declaration. The peak-to-peak jitter of the ADPLL was achieved 70 ps, correspondingly.

Kai-Hui Zeng *et al.* (2015) [13] in this**,** the ADPLL devoid of a key separator was locked using sub-harmonically injection was offered. It achieves not just low phase noise, even though too low power in excess of the procedure, voltage and temperature (PVT) changes and this ADPLL uses merely a easy BBPD devoid of TDC when evenly frequency in addition to phase locking. Moreover, the insertion pulse would be self-adjusted to most favourable time in excess of the PVT changes devoid of supplementary calibration loop. This ADPLL was fictitious in a 40-nm CMOS procedures, it took 3.04mW under a criterion provider of 1.1V exclusive of output buffers. The calculated phase noise of the future ADPLL was -121.4dBc/Hz at 1MHz offset. The integrated rms jitter was 109.6 fs for the offset frequency from 1kHz to 100MHz. Figure-of-merit was equal to –254.39 dB.

Young-Ho Choi *et al. (*2017) [14] in this paper, a PIFC was used to reduce the power expenditure by changing TDC in a ring-oscillator-based digital fractional-N PLL. The calculation of the integer and fractional parts of the frequency-division-ratio a predicted-phase-interpolation method was used and to discover two exclamation clocks; the prophecy means provide a considerable power diminution in the future PIFC by enabling the employ of low-frequency clocks intended for phase exclamation. Future PLL chip in a 65-nm CMOS employed 0.173 mm^2 in addition to devour mW at 6 GHz and 1.2 V; the PIFC devour fewer than 20% of the TDC power. The integrated rms jitter was 1.75 ps and a FoM value of −223.2 dB was successfully achieved.

Samira Bashiri *et al.* (2015) [15] All-digital bang-bang PLL suffered by unnecessary productivity spurs owing to their non-linear behaviour. The phase detector hysteresis was explored as a source intended for supplementary recital dilapidation in this work. In the presence of hysteresis the jitter dependency on the loop parameters were analyzed, on condition that a novel nearby to be measured when scheming meant for least jitter. An innovative representation used for the BBPLL was too showed to revolve the non-idealist nature of the PD and its consequence on the loop. To assess recital, a time-amplifier was worn to recover the declaration of the PD. A loop amid a standard PD is then compared with those of Jitter in addition to counterfeit quality of the BBPLL with TA assisted PD. Final output shows to facilitate the TAPD boosts the realization with a feature of three. Intend and simulations had been completed in a 32-nm CMOS expertise.

Helmuth Brugel and Peter F. Driessen *et al.* (1994) [16] this paper proposed a digital PLL bit synchronizer with inconsistent loop bandwidth intended for quick acquirement in addition high-quality tracking recital and its recital evaluated using Markov chain methods. Results were accessible intended for the sharing of achievement time with time to initial bit slip in conditions of state transition possibility. Proposed for explode mode statistics, result meant for the timing error and bit error rate as an occupation of the prelude bit number were obtained. Results were estimated with frequent matrix products plus established with imitation. Evaluation of the changeable bandwidth DPLL towards a permanent bandwidth DPLL shows considerably quicker attainment designed for a specified tracking presentation.

C.W. Chang *et al.* (2016) [17] close-threshold ADPLL through a PMU was used to built the future ADPLL employment dependably diagonally variations as well as power expenditure. While operated below close-threshold situation starting from 0.52 to 0.58 V VDD, the gated digitally COF collection was beginning 90.8 to 245.7 MHz. A confine time of 9.5μs at 100 MHz output clock frequency was deliberate through an rms period jitter of 0.17% UI, while the ADPLL was operated at 0.52 V VDD. ADPLL power diminution at 130 MHz output frequency is 39% by PMU plus the buck converter power expenditure is almost 30 μW. As a result, the future ADPLL by PMU was appropriate to event driven or low-voltage applications.

Pei-Ying Chao *et al.* (2013) [18] the frequency collection spotted is repeatedly segmented meant for an ADPLL, and this can grounds important jitter when the operational circumstance revisions. Towards concentrate on this matter, it present a method, called even code-jumping, that can sew up mutually the SFP of a DCO into a

permanent collection, moreover thus diminish the jitter considerably. This method blended a novel mirror-DCO-based calibration method lying on the road to obtain into narrative procedure variations. This method with test chips in 0.18-μm CMOS expertise. Capacity results demonstrate to, while functioning at 1 GHz, the RMS jitter was 4.3ps (0.43%UI) and the peak-to-peak jitter was 35.6 ps (3.56%UI), correspondingly.

Jian Chen et al. (2012) [19] this paper presented an enhanced construction of polar TX. This future architecture was digitally-intensive and primarily unruffled of a 1-bit low-pass delta sigma ΔΣ modulator intended for envelop modulation, an all-digital PLL (ADPLL) intended for phase modulation plus a H-bridge class-D power amplifier (PA) for differential signalling. Using the phase modulated RF carrier the ΔΣ modulator was clocked to guarantee phase synchronization among the amplitude and phase path, as well as to assurance PA was interchanging on zero crossings of the output current. An on-chip pre-filter was worn to diminish the PC on or after packages at the exchange stage output. The on-chip filter as well acts while discrepancy to single-ended alteration and impedance matching .The deliberate digital transmitter expends 58 mW from a 1-V supply at 6.8 dBm output power.

Kuo-Hsing Cheng *et al.* (2012) [20] in this paper a technique called ultra-low-voltage ADPLL through a DSR was presented. The DSR preserves an RMS jitter intended for a 280-MHz output signal of a smaller amount than 0.55% while a 100-kHz to 100-MHz supply noise was formed resting on a DCO. The DCO uses the stage timing declaration of a DCV towards attain the elevated timing declaration. The future DLF could diminish the area cost plus critical path by means of the DET method. Intended for a small supply voltage, the DCO plus the TDC employ bulk-controlled method to amplify the maximum operational frequency in addition to timing declaration, in that order. While the ADPLL output is 800 MHz at 0.6 V, the power expenditure as well as core area are 656 μW and 0.02 mm^2, correspondingly, in a 90-nm CMOS procedure.

Ching-Che Chung Chiun-Yao Ko *et al*. (2012*)* [21] this paper shows a PLL designed for analog video RGB signal, attainment boundary needed accurate clock creation starting from a extremely noisy and low-frequency HSYNC. The frequency reproduction percentage was forever tubby than 800 and can be up to in excess of 2600 in such applications. For HSYNC the production pixel clock had to be phase associated. If not, the displayed illustration will turn into indistinct. ADPLL intended for video pixel clock creation in a 65 nm CMOS expertise were offered in the paper. The DLF reduced the orientation clock jitter belongings in the proposed ADPLL and afterwards the period jitter of the yield pixel clock can be determined. To perform the fast phase tracking a TDC plus a DSM were worn, and the tracking jitter were guarded at smaller amount than 1/3 of the production pixel clock period. The future ADPLL does not involve an additional exterior oscillator to conquer the reference clock jitter belongings as compared to prior studies. Therefore, it had diminutive chip region plus little power expenditure, and is complementary to VPC invention applications in 65 nm CMOS procedure.

Wei Deng *et al.* (2015) [22] this paper presented a completely synthesizable PLL depends on insertion locking, through an interpolative PCO, (a present output DAC), plus a well pledge digital varactors. Every circuit so as to formulate up the PLL are premeditated as well as executed by DSC devoid of some alteration, with repeatedly P&R through a DDF devoid of several manual placements. Executed in a 65 nm digital CMOS procedure, this effort employs simply 110 μm × 60 μm layout district, which was the fewest PLL described consequently distant to the most excellent information of the authors. The dimension results demonstrate to facilitate this exertion attains a 1.7 ps RMS jitter on the output frequency of 900 MHz even as overwhelming 780 μW DC power.

Jim Dunning *et al.* (1995) [23] in this paper for frequency-synthesizing, a ADPLL was completely incorporated through a CMOS microprocessor. The ADPLL had a 50-cycle phase lock, have a expand machinery sovereign of procedure, voltage, and temperature, along with the resistant to input jitter. A DCO design the center of the ADPLL plus compels as of 50 to 550 MHz, consecutively at 4x the RCF. DCO have 16 b of binary weight control plus had achieved LSB declaration below 500 fs.

Ahmed Elkholy *et al.* (2016) [24] Phase noise performance of ring oscillator depends on digital FNPLLs was brutally compromised via incompatible bandwidth desires towards concurrently contain oscillator phase plus quantization noise imported through the TDC, $\Delta\sum$ fractional divider, DAC and while a significance, their FoMJ that quantify the power–jitter tradeoffs was at slightest 25 dB inferior than their LC-oscillator-dependent FNPLL supplements. This paper explores to shut this recital breach through unrolling PLL bandwidth by QNCT and with applying a dual-path DLF to repress the damaging collision of DAC quantization noise. Fictitious in 65 nm CMOS procedure was the planned FNPLL worked in excess of an extensive frequency series of 2.0–5.5 GHz by a customized comprehensive variety multi-modulus partition through flawless interchanging. The future FNPLL achieves extensive BW awake to 6 MHz using a 50 MHz orientation plus its FoMJ was −228.5 dB, which was the most brilliant between every single reported ring-based FNPLLs.

Mark A. Ferriss and Michael P. Flynn *et al.* (2008) [25] this paper described an all-digital PD for a fractional- PLL. PD dwells of an only FF, which acted since in excess of sampled one bit phase quantizes. A method that enables FSKM charge greatly well-built than the loop BM was established, called digital sampling composing lying on the frequency accurateness of the output signal. A prototype 2.2 GHz fractional- N synthesizer associates the digital PD and sampling method was offered as evidence of impression. Though the loop BM was merely 142 kHz, an FSKM charge of 927.5 kbs was achieved. The 0.7 mm^2 prototype is executed in 0.13 m CMOS consumes 14 mW as of a 1.4 V supply.

1.4 CONTRIBUTIONS OF CURRENT WORK

This research concentrated on designing an All-Digital Phase Locked Loop with a twin Vernier delay line based time to digital converter. The goal of this work was to design a PLL to eliminate the use of analog components and fully digitize its components. The PLL also aims at achieving a faster lock time. After simulation is performed, conclusions will be arrived at to determine the performance of the ADPLL and to determine what changes and improvements could be made for performance enhancement. This thesis provides a good starting point for a designer who aims at fully digitizing the components of a PLL using Time to digital converters as digital phase detectors.

The design was simulated at the behavioral level for testing the functionality of the design. The design was synthesized to obtain the gate-level equivalent that was simulated for testing the timing constraints. Finally, the transistor-level design was obtained for transient response. The design was synthesized for the 180nm CMOS technology.

1.5 ORGANIZATION OF THESIS

Chapter 2 presents a review of the Phase Locked Loop fundamentals. An overview of the basic building blocks of a Linear PLL is presented. A second order model of a Linear PLL is also presented. Existing approaches such as conventional Charge Pump PLLs and Digitally Controlled Oscillator based approaches are also discussed.

Chapter 3 presents an in-depth look at the architecture, design and implementation of the current research on implementing a fully digital PLL with the use of new architecture based on VDL based time to digital converter.

Chapter 4 presents the simulation and measured results of the All-Digital Phase Locked Loop that verify some of the robust features of the fully digital implementation.

Chapter 5 presents a summary of the contributions of the research and the conclusions for this work. The objectives accomplished in this thesis will be reviewed and suggestions for future work are also investigated in this chapter.

CHAPTER 2 PHASE LOCKED LOOP BACKGROUND

2.1 INTRODUCTION

This Chapter presents a review of the fundamental concepts of Phase Locked Loops (PLLs) and an overview of the All-Digital Phase Locked Loops (ADPLLs). Section 2.2 discusses the implementation techniques of the different building blocks of Linear PLLs (LPLLs). Section 2.3 presents the system analysis of a second-order PLL. Section 2.4 presents a brief description of Digital Phase Locked Loops (DPLLs). Section 2.5 presents an overview of All Digital PLLs (ADPLLs) and concludes with a discussion on the implementation methods currently used for the realization of ADPLLs.

Figure 2.1 shows the block diagram of a basic Phase Locked Loop (PLL). The complex nonlinear PLL feedback system is made up of the following blocks: Phase Detector (PD), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO). A Divide by N Counter is inserted between the VCO and the PD in frequency synthesis applications. When the counter is used, the VCO generates a frequency that is N times the reference frequency.

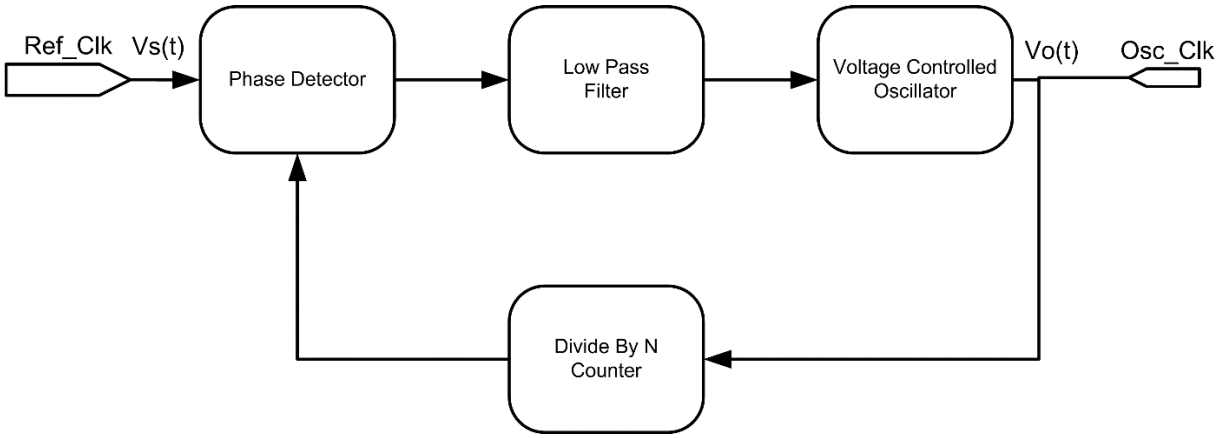


Figure 2.1 Block diagram of a basic Phase Locked Loop (PLL)

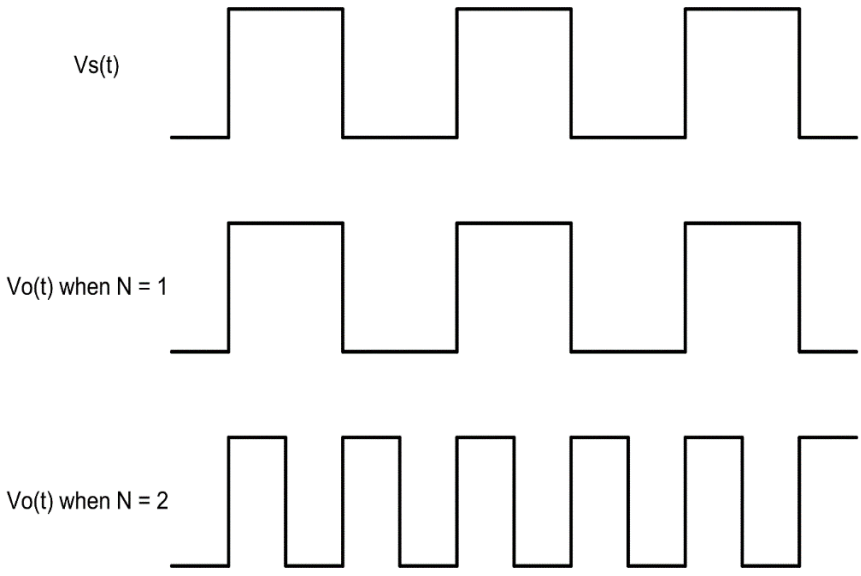


Figure 2.2 PLL in locked state.

Figure 2.2 shows the input and output waveforms when the PLL is locked with zero phase error in the absence of a frequency divider (N=1). Figure 2.2 also shows the waveforms in the presence of a Divide by 2 Counter in the feedback loop (N = 2). In this case, the frequency of the PLL output $(v_0(t))$ is twice that of the input signal $(v_s(t))$.

The working of a basic PLL can be summarized as follows; the Phase Detector (PD) compares the phases of the input signal $(v_s(t))$ and the output of the Voltage Controlled Oscillator (VCO) $(v_0(t))$. The PD generates an error signal that is proportional to the phase difference between the two signals. The Low Pass Filter (LPF) is used to suppress the sum or the high-frequency component of the error signal. The VCO is a free-running multi-vibrator and operates at a frequency called the free running frequency (f_0). It can be shifted to either side by applying a dc control voltage to the VCO. The low-frequency component from the LPF is applied as the control signal to the VCO. The VCO generates an output signal whose frequency is a linear function of the control voltage. This signal is then fed back to the Phase Detector to achieve zero or constant phase difference between the input signal and the output of the VCO. Once locked, the PLL tracks the frequency changes of the input signal. Some of the commonly used terminologies in a PLL are

- The **Hold range** is defined as the range of frequencies over which the PLL can maintain lock with the input signal.
- The **Pull-in range** or **Capture range** of a PLL is the range of frequencies over which the PLL can acquire lock with the input signal.
- **Pull-in time** or **Lock time** is the total time taken by the PLL to establish the lock.

2.2 BUILDING BLOCKS OF PLL

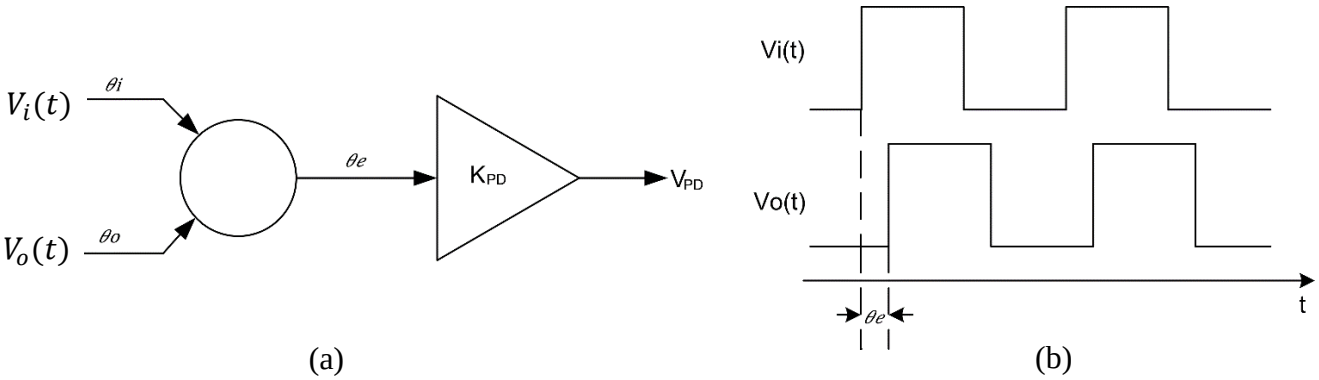
The basic PLL negative feedback system has three blocks, namely Phase Detector, Low Pass Filter and Voltage Controlled Oscillator. The features and implementation methods of these blocks are investigated in this section.

2.2.1 Phase Detector

Phase Detectors fall into two broad categories: The first category consists of detectors that are memoryless; their outputs are independent of the previous inputs. These detectors are based on multiplier circuits such as Exclusive OR gate and the Diode Ring Mixer. The second category consists of detectors that require memory because the output is determined using the previous inputs. These detectors are based on sequential circuits constructed from flip-flops and logic gates. The sequential phase detector provides many advantages over the memoryless detectors:

- Extended Phase Detector range.
- Improved frequency acquisition.
- Insensitivity to input signal levels.

A simple model of a Phase Detector (PD) is shown in Figure 2.3 (a). The PD converts the difference between the phase of the input (θ_i) and the phase of the VCO output (B0) into a voltage (V_{PD}) with a gain factor (K_{PD}). Let θ_e represent the difference between the input phase and the VCO phase as illustrated in Figure 2.3 (b). The PD produces an output voltage (V_{PD}) that is proportional to the phase error (θ_e).



(a) (b)

Figure 2.3 Phase Detector (a) Model (b) Waveform

Equation 2.1 gives the phase difference between the input and output.

$$\theta_e = \theta_i - \theta_o \tag{2.1}$$

In the linear region, the PD can be modeled by Equation 2.2.

$$V_{PD} = K_{PD} * \theta_e \tag{2.2}$$

The range of values of θ_e for which the linear model is valid is called the Range of the PD. The phase detectors can be analog or digital.

2.2.1.1 Four Quadrant Multiplier Phase Detector

Figure 2.4 shows the block diagram of a Four Quadrant Multiplier PD. The Four Quad rant Multiplier performs the multiplication of the input signal by the output of the VCO. Let the input signal be given by

$$v_s = V_s \sin(\omega_s t) \tag{2.3}$$

And the VCO signal be

$$v_O = V_O \sin(\omega_o t + \theta_e) \tag{2.4}$$

The output of the multiplier is

$$\overline{v_e} = K_M v_s v_o = K_M V_s V_O \sin(\omega_s t) \sin(\omega_o t + \theta_e) \tag{2.5}$$

Where K_M is the multiplier constant or the PD-gain and θ_e is the phase shift between the input signal and the output of the VCO.

Equation (2.5) can be simplified to,

$$\bar{v_e} = 0.5\, K_M V_S V_0[\cos(\omega_s t - \omega_0 t - \theta_e) - \cos(\omega_s t + \omega_o t + \theta_e)] \quad (2.6)$$

When PLL is in locked condition $\omega_0 = \omega_s$.

Thus,

$$\bar{v_e} = 0.5\, K_M V_S V_0[\cos(-\theta_e) - \cos(2\omega_o t + \theta_e)] \quad (2.7)$$

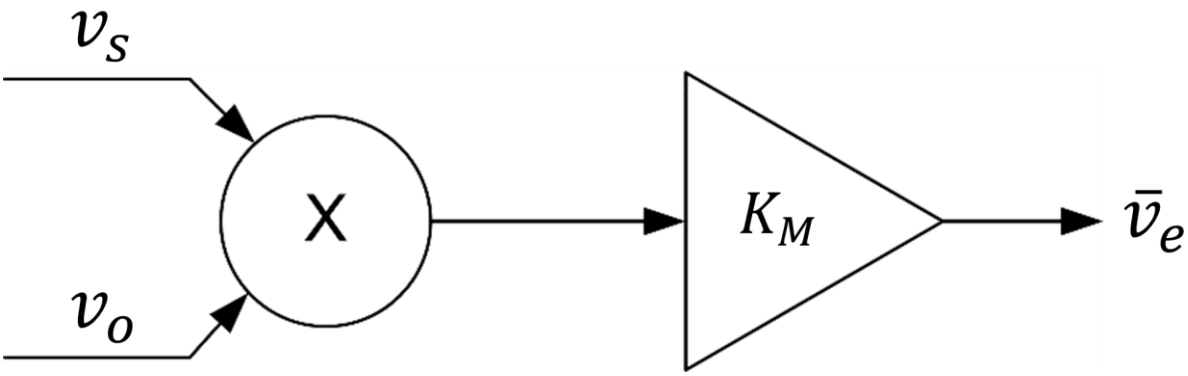


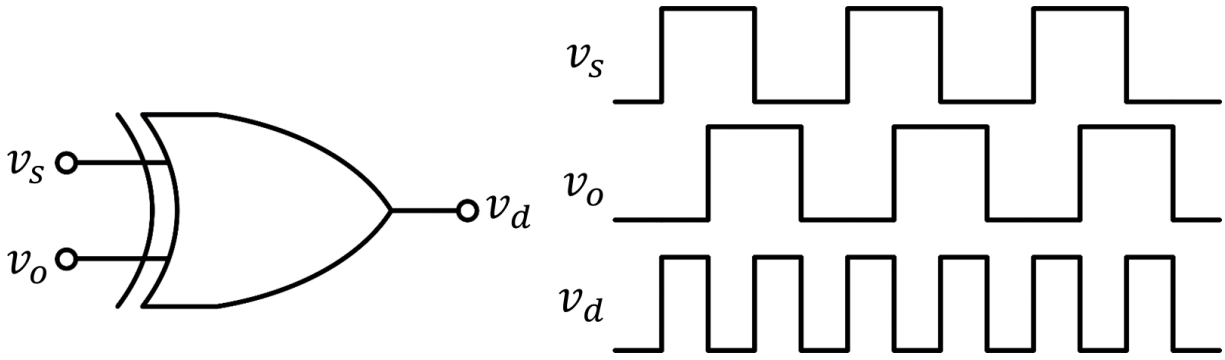
Figure 2.4 Block diagram of a Four Quadrant Multiplier PD

The phase comparator output contains a dc term ($0.5KV_sV_0$) and a double frequency term. The second term is filtered using a low pass filter and the dc term is applied as the control input to the VCO. Thus in the locked state ($\omega_s = \omega_0$), the phase difference between the input signal and the VCO output should be 90° ($\theta_e = 90°$). Equation 2.8 shows that the PD gain for small values of θ_e is

$$K_{PD} = 0.5\, K_M V_S V_0 \theta_e \quad (2.8)$$

2.2.1.2 Exclusive OR Phase Detector

Figure 2.5(a) shows the symbol of the Exclusive OR (EXOR) Phase Detector. The EXOR PD is the simplest type of phase detector that uses digital input waveforms. The output of the gate is logic high only when one input goes high and is low for all other inputs. When the input signals are out of phase by exactly 90°, the phase error is zero. When the input signals are symmetrical square waves, the output is a square wave with 50% duty cycle. This condition is depicted in Figure 2.5(b).



(a) (b)

Figure 2.5 EXOR PD (a) Symbol (b) Waveform when e = 0

The output of the Four Quadrant Multiplier varies with the sine of the phase error; the average output of the EXOR is a triangular function of the phase error as shown in Figure 2.6. When $-\pi/2 < \theta_e < \pi/2$, the average output signal is given by Equation 2.9,

$$\overline{v_d} = K_{PD}\theta_e \tag{2.9}$$

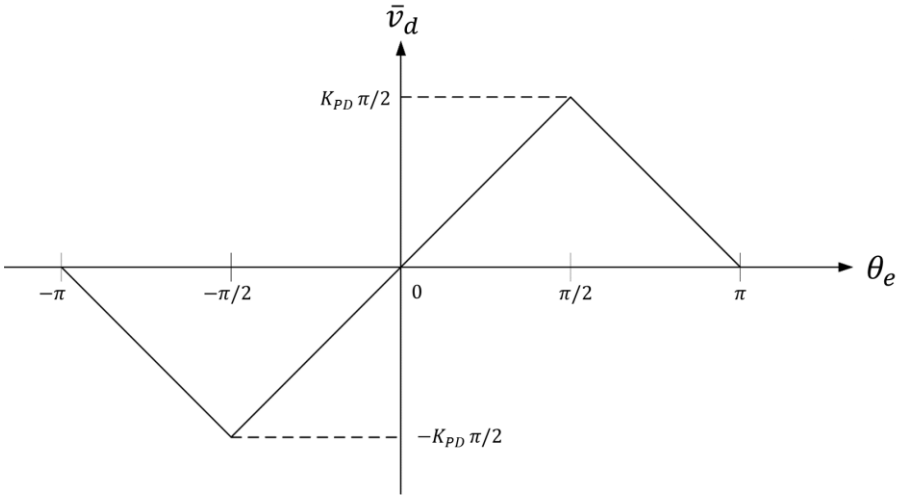


Figure 2.6 Characteristics of EXOR PD

When the high and low logic levels are V_{DD} and 0, the phase detector gain (K_{PD}) is given by,

$$K_{PD} = \frac{VDD}{\pi} \tag{2.10}$$

2.2.1.3 Phase Frequency Detector (PFD)

The Phase Frequency Detectors (PFDs) can be used for both phase and frequency detection. Figure 2.7 shows the schematic of a PFD constructed using two D-Flip Flops (FFs) and an AND gate. Table 2.1 shows the state assignment of the PFD. Figure 2.8 shows the state diagram of the PFD.

Table 2.1 State assignment of the PFD

UP	DOWN	STATE
0	0	S_0
0	1	S_1
1	0	S_2

The outputs of the PFD are designated as Up and Down. The PFD can be in one of the four states, Up = 0, Down = 0; Up = 1 ; Down = 0; Up = 0, Down = 1 ; Up = 1 , Down = 1. However, the fourth state is prevented using an AND gate which resets the flip-flops. Thus the three allowed states of the PFD are designated as S_O, S_1, and S_2.

Upon Reset, the PFD enters state S_0 . The state of the PFD is determined by the positive transitions of the input signals ($v_s \; and \; v_0$). The PFD generates the appropriate Up/Down signals depending on the current and the previous states. The Up/Down pulses are generated proportional to the phase error when the input leads/lags the output. If the loop is in lock, short pulses are generated on the

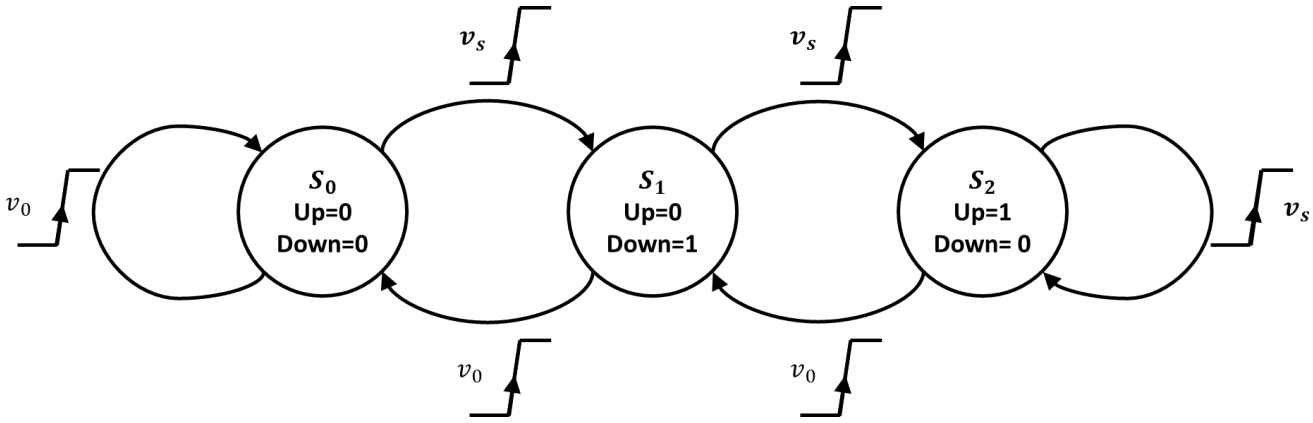


Figure 2.7 State diagram of the PFD

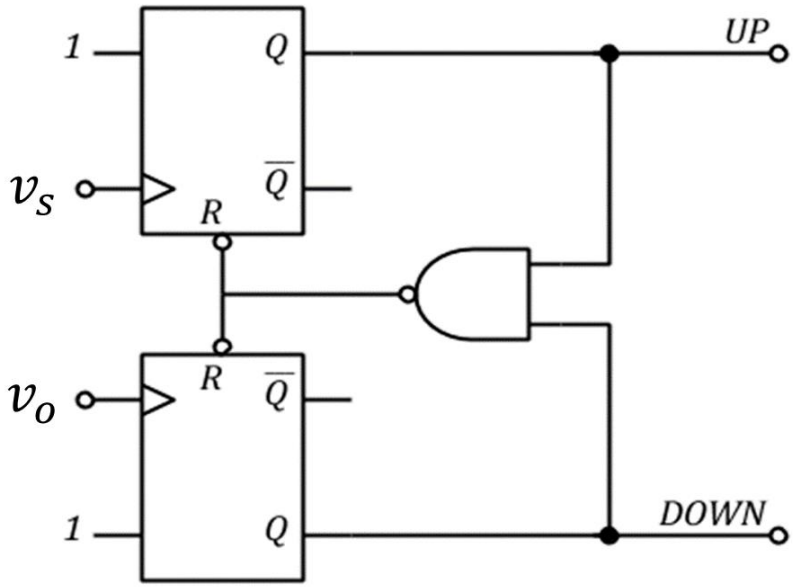


Figure 2.8 Block Diagram of PFD

Up/Down outputs. The PFD also functions as a frequency detector. Depending on the frequencies of the input and the output, more pulses are generated on the Up/Down outputs. When $-2\pi < \theta_e < 2\pi$, the average output signal is given by Equation 2.11,

$$v_d = K_{PD}\theta_e \tag{2.11}$$

When the high and low logic levels are V_{DD} and 0, the Phase Detector gain (K_{PD}) is given by,

$$K_{PD} = \frac{V_{DD}}{4\pi} \tag{2.12}$$

The characteristics of different phase detectors are investigated and compared in the following section. In an EXOR Phase Detector, the output is averaged or integrated, hence it has good noise rejection. However a drawback of the EXOR Phase Detector is that it may lock to a multiple of the clock frequency. An EXOR DPLL locks on harmonics of the input. If any of the clock inputs is replaced with twice or one half of the frequency, the average of the waveforms will still remain the same. Thus, the EXOR PD declares a "false lock". This restricts the operating frequency of the VCO between $2f_s$ and $f_s/2$ where f_s is the frequency of the reference or the input signal.

The other phase detector discussed was the Phase Frequency Detector (PFD). The PFD overcomes the problem of locking on a harmonic of the data encountered in EXOR PDs. However, the PFD has poor noise rejection. Also, the outputs of the PFD namely Up and Down have to be converted to a single output which drives the loop filter. Figure 2.9 shows the two ways this can be achieved. Figure 2.9(a) uses

the tristate output and the configuration in Figure 2.9(b) is called the Charge Pump. The latter is preferred over the former configuration due to its better immunity to power supply variations. When the signals, Up and Down are low, the transistors M1 and M2 are off and the output is in the high impedance state. If Down signal is high, the output is pulled low through M2. If Up signal is high, the output is pulled to VDD as M1 is on.

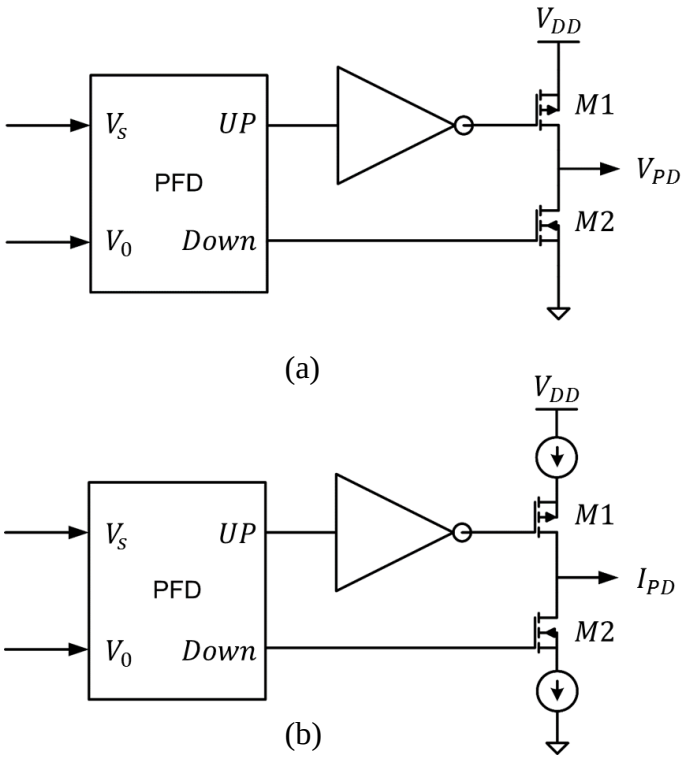


Figure 2.9 PFD (a) Tri-State Configuration and (b) Charge Pump Configuration

In this configuration, the power supply variations can adversely affect the output voltage when M1 is on and thus modulating the VCO control voltage. This can be overcome by using current sources in series with M1 and M2 and making them insensitive to power supply variations [26].

Table 2.2 characteristics of different phase detectors.

Characteristic	Multiplier	XOR	PFD
Phase Detection	Yes	Yes	Yes
Frequency Detection	No	No	Yes
Sequential (With Memory)	No	No	Yes
Detection Range	Small	TC	4rc
Sensitivity to missing edges	No	No	Yes
Locking Phase	RC/2	RC/2	0
Duty Cycle Sensitive	Yes	Yes	No

Multiplier type Phase detectors have an advantage when it comes to the frequency of operation. These phase detectors provide good performance when the applied signals are noisy. On the other hand, Sequential Phase detectors are used when the input signals are free from noise and have well-defined level transitions. The PFD will not lock on a harmonic of the clock frequency. Hence the VCO clock duty cycle is irrelevant with the PFD as the PFD performs edge-triggered comparison. However, in communication applications, an EXOR PD might be used due to its good noise rejection.

2.2.2 Loop Filter

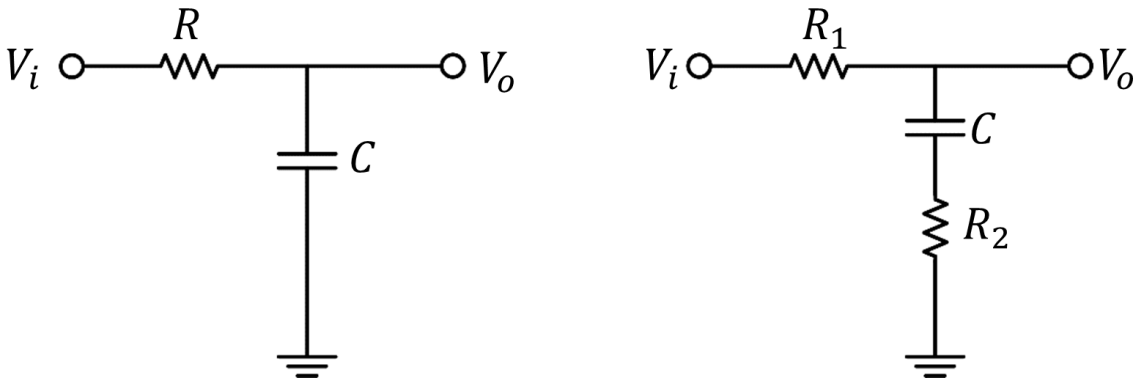
The higher-order frequencies out of the Phase Detector must be filtered out, so the Loop Filter must be of low-pass type. The Loop Filters can be of active type based on operational amplifier technology or passive type using resistor-capacitor networks.

2.2.2.1 Passive Lag Lead Loop Filter

The simplest Low Pass Filter (LPF) can be constructed using RC Single Time Constant network (STC) as shown in Figure 2.10(a). The RC filter has the transfer function of the form,

$$F(s) = \frac{1}{1+s\tau} \tag{2.13}$$

Where, $\tau = RC$.



(a) (b)

Figure 2.10 Passive Loop Filter (a) First Order RC LPF (b) Lag Filter with a zero

A Passive Lag Lead Loop Filter with another resistor R2 in series with the capacitor C can be constructed as shown in Figure 2.10(b). This filter has one pole and one zero and does not have an integrating function. The filter has a low gain since it is made up of passive elements. The transfer function $F(s)$ of the Passive Loop Filter is given by,

$$F(s) = \frac{1 + s\tau}{1 + s(\tau_1 + \tau_2)} \tag{2.14}$$

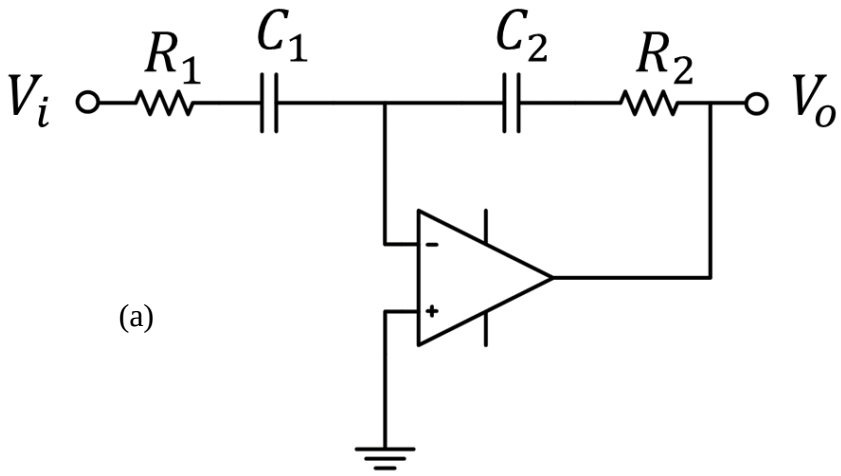
Where, $\tau_1 = R_1C_1$ and $\tau_2 = R_2C_2$.

2.2.2.2 Active Lag Lead Loop Filter

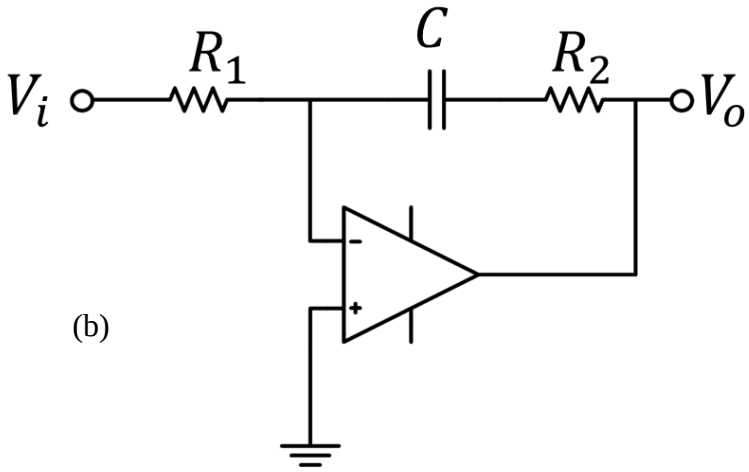
The Active Filters are made using passive elements as part of the feedback network for a high-gain amplifier. Figure 2.11(a) shows an Active Lag Lead filter. Its transfer function contains a gain term K_a . The transfer function $F(s)$ of this filter is given by

$$F(s) = K_a \frac{1+s\tau_2}{1+s\tau_1} \tag{2.15}$$

Where, $\tau_1 = R_1C_1$, $\tau_2 = R_2C_2$ and $K_a = -C_1/C_1$



(a)



(b)

Figure 2.11 Active Loop Filter (a) Active Lag Filter (b) Active PI Filter

Figure 2.11(b) shows an active "PI" low pass filter. Equation 2.16 gives the transfer function of the active "PI" filter.

$$F(s) = \frac{1+s\tau_2}{s\tau_1} \tag{2.16}$$

Where, $\tau_1 = R_1C$ and $\tau_2 = R_2C$.

The PI filter has a pole at s = 0 and behaves like an integrator at low frequencies.

2.2.3 Voltage Controlled Oscillator (VCO)

VCOs are electronically tunable oscillators in which the output frequency is dependent on the control voltage. A Voltage Controlled Oscillator uses a voltage input to control its frequency in contrast to a Current Controlled Oscillator (CCO) that uses a current input to control its frequency. The choice of a VCO circuit configuration depends on the application. If the VCO frequency (ω_2), is a linear function of the control voltage $(v_c(t))$, it can be given by

$$\omega_2(t) = \omega_0 + \Delta\omega_2(t) = \omega_0 + K_V v_c(t) \tag{2.17}$$

Where ω_0 is the free running frequency of the VCO. K_V is the gain factor of the VCO. Figure 2.12 illustrates the frequency versus control voltage characteristics of the VCO. The VCO is the critical component of a conventional PLL that affects the jitter and phase noise performance. A resonant VCO circuit with an LC tank as the resonant element is known to have excellent jitter performance. However this type of VCO configuration is not suitable for monolithic implementations and requires some off-chip components. On-chip implementations of inductors have been reported in [27] but these have a low quality factor (Q) and are bulky. Ring oscillators are attractive from integration and cost point of view and are being used in jitter sensitive applications [27] [28] [29].

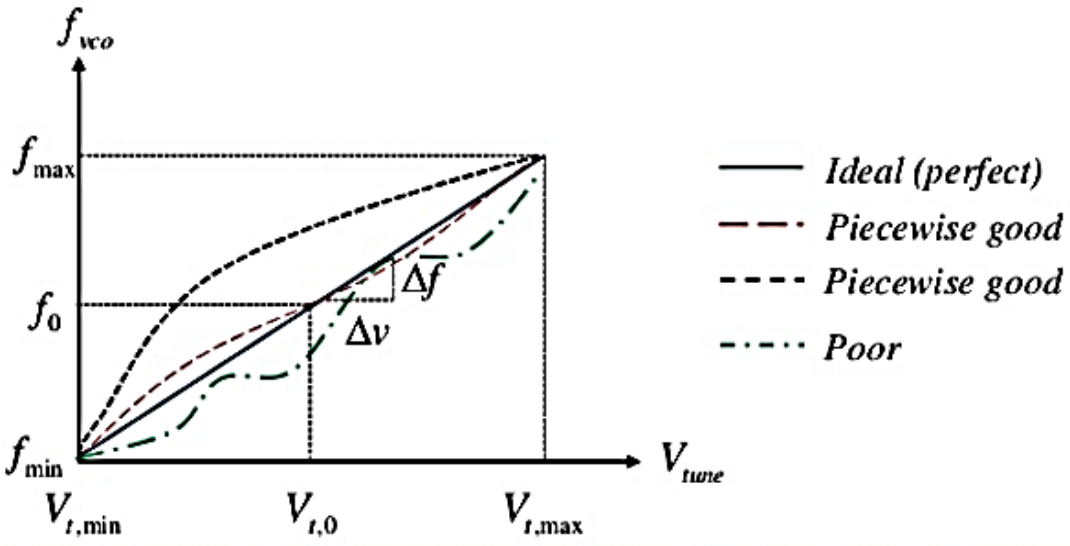


Figure 2.12 Characteristics of the VCO

A Ring Oscillator is made up of a number of delay stages. If a cascade of N gain stages with an odd number of inversions is placed in a feedback loop, the circuit oscillates with a period equal to $2N\,T_d$ where T_d is the delay for each stage with unit fan-out. The schematic of a Ring Oscillator is shown in Figure 2.13. Equation 2.18 gives the frequency of oscillation.

$$f_{osc} = \frac{1}{2NT_d} \tag{2.18}$$

The factor of 2 in the above equation is due to both rising and falling edges of each delay stage contributing to f_{osc}. The above equation suggests that there are two ways to change the frequency of oscillation:

- By varying the number of delay stages N.
- By varying the delay per stage T_d.

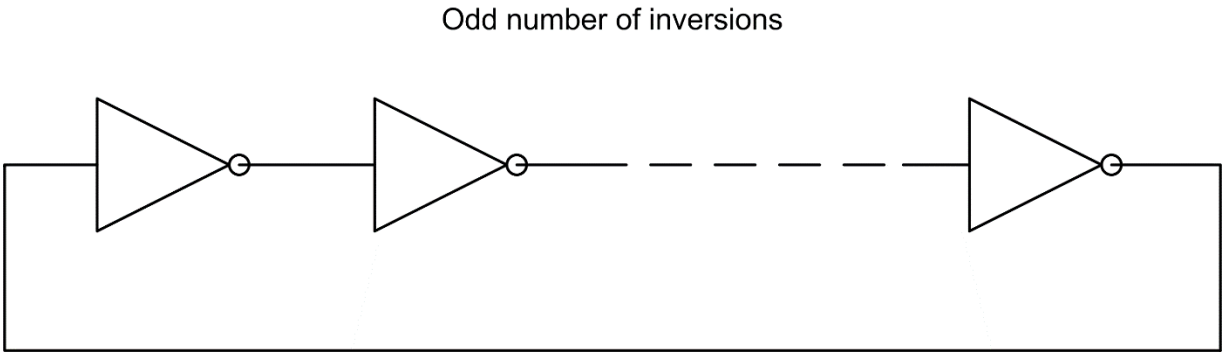


Figure 2.13 Ring Oscillator General Schematic

A Conventional Voltage Controlled Ring Oscillator and its delay approximation are shown in Figure 2.14 [30]. Here, N is an odd number of inversions. Assume that the gate to source parasitic capacitances, CG of the $NMOS$ and $PMOS$ transistors are equal. The frequency of oscillation is given by

$$f_{osc} = \frac{1}{2N\,\tau} \tag{2.19}$$

Where τ is the delay of one inverter stage. The oscillation amplitude of each inverter stage is given by Equation 2.20,

$$\tau = \frac{V_{osc}C_G}{I_{ctrl}} \tag{2.21}$$

Where V_{osc} is the oscillation amplitude.

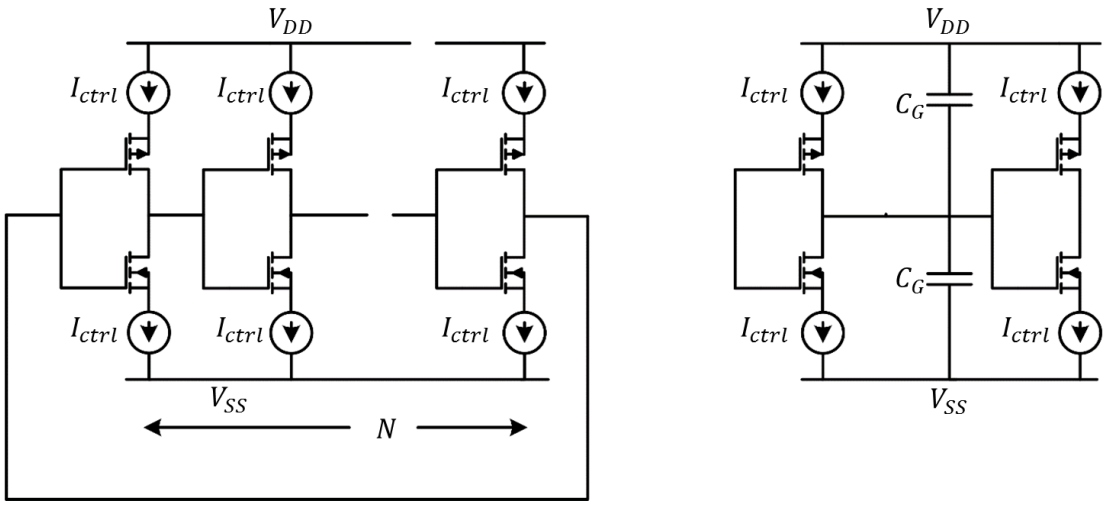


Figure 2.14 A Conventional Voltage Controlled Ring Oscillator

The expression for oscillation frequency, f_{osc} can now be given by:

$$f_{osc} = \frac{I_{ctrl}}{2N\, V_{osc} C_G} \tag{2.22}$$

The oscillation frequency depends on the current I_{ctrl}. The number of stages (N), the parasitic capacitance C_G and the oscillation amplitude. Thus, the oscillation frequency can be varied by varying control current or amplitude, as C_G is a fixed parameter. The current is usually the controlling factor. The oscillation frequency can be tuned for a wide range, by changing the value of control current. However, it is difficult to keep the matching between the upper and lower control currents for very small currents.

A modified Voltage Controlled Oscillator topology with wide tuning range and fast voltage swing is reported in [30]. The design implements a low frequency ring oscillator with relatively smaller devices and fewer stages.

2.3 SYSTEM ANALYSIS OF SECOND-ORDER PLL

The three building blocks namely the Phase Detector, Low Pass Filter and VCO can be put together and a linear mathematical model for the system can be developed. The mathematical model will be used to derive the phase transfer function $H(s)$ which relates the phase of the input signal θ_1 to the phase of the output signal θ_2:

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{KF(s)}{s+KF(s)} \tag{2.23}$$

Where $\theta_1(s)$ and $\theta_2(s)$ are the Laplace Transforms of the phases of the output and the input respectively. $F(s)$ is the transfer function of the Loop Filter. K is the loop gain of the PLL and is given by $K = K_{PD}\, K_v$. Figure 2.15 shows the linear model of the PLL. The output signal from the Four Quadrant Multiplier Phase Detector is given by:

$$v_e(t) = K_{PD} sin\, \theta_e \tag{2.24}$$

When the phase error is small,

$$v_e(t) \cong K_{PD}\theta_e \tag{2.25}$$

K_{PD} represents the Phase Detector gain. Equation 2.25 represents the linear model of the Phase Detector. Thus a Four Quadrant Multiplier used in a Linear PLL, which is in the locked state, represents a zero-order block of gain K_{PD}. Laplace Transform of Equation 2.25 yields,

$$V_e(s) = K_{PD}\theta_e(s) \tag{2.26}$$

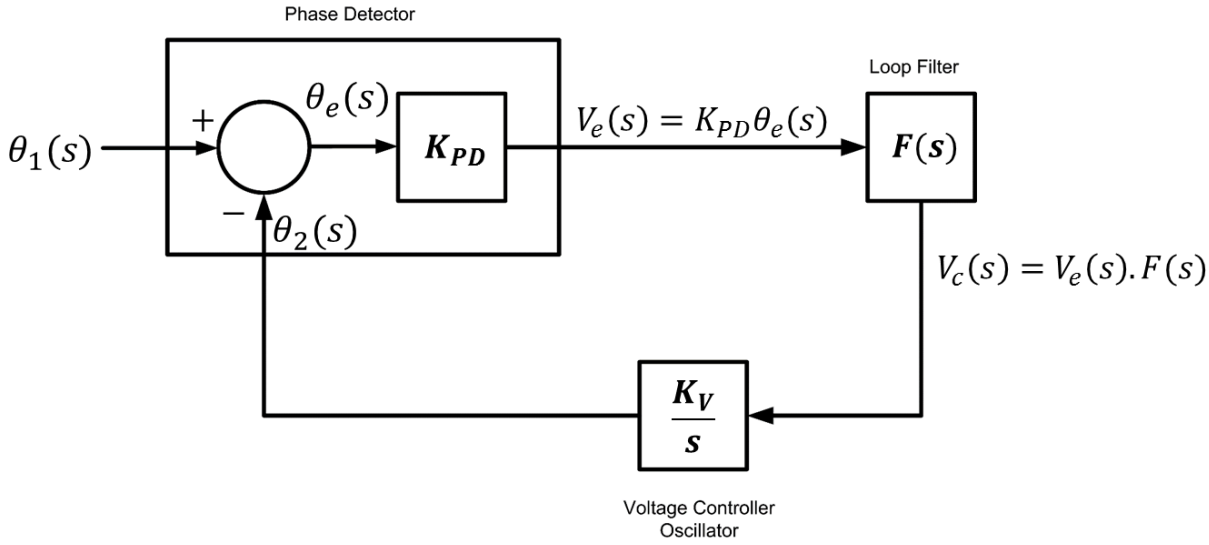


Figure 2.15 Linear model of the Phase Locked Loop

Table 2.3 presents a summary of the Transfer Functions, $F(s)$ for the different loop filters discussed in Section 2.2.2.

The output of the Low Pass Filter is applied as the control input to the VCO. The control voltage, $v_c(t)$ shifts the VCO frequency from its free running frequency, ω_0 to a frequency ω_2 given by,

$$\omega_2(t) = \omega_0 + \Delta\omega_2(t) = \omega_0 + K_v v_c(t) \tag{2.27}$$

The phase of the VCO, θ_2 is given by the integral over the frequency variation, $\Delta\omega_2(t)$ as shown in Equation 2.28,

$$\theta_2(t) = \int \Delta\omega_2(t)dt = K_v \int v_c(t)dt \tag{2.28}$$

Table 2.13 Summary of the Transfer Functions of the Loop Filters

Type of Loop Filter	**Transfer function, $F(s)$**
Passive Lag filter	$F(s) = \frac{1}{1+s\tau}, \tau = RC$
Passive Lag Filter with a zero	$F(s) = \frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}, \tau_1 = R_1C \text{ and } \tau_2 = R_2C$
Active Lag Lead Filter	$F(s) = K_a\frac{1+s\tau_2}{1+s\tau_1}, \tau_1 = R_1C_1, \tau_2 = R_2C_2 \text{ and } K_a = -\frac{C_1}{C_2}$
Active PI Filter	$F(s) = \frac{1+s\tau_2}{s\tau_1}, \tau_1 = R_1C \text{ and } \tau_2 = R_2C$

Laplace Transform of an integral over time is same as division by s, so the Laplace transform of Equation 2.28 yields

$$\theta_2(s) = \frac{K_v}{s} V_c(s) \tag{2.29}$$

The Transfer Function of the VCO is given by Equation 2.30.

$$\frac{\theta_2(s)}{V_c(s)} = \frac{K_v}{s} \tag{2.30}$$

The Laplace Transform of the error signal, $\theta_e(s)$is given by Equation 2.31.

$$\theta_e(s) = \theta_1(s) - \theta_2(s) \tag{2.31}$$

The Phase Transfer Function, $H(s)$ is given by:

$$H(s) = \frac{\theta_2(s)}{\theta_1(s)} = \frac{\theta_2(s)}{V_c(s)} * \frac{V_c(s)}{V_e(s)} * \frac{V_e(s)}{\theta_e(s)} * \frac{\theta_e(s)}{\theta_1(s)} \tag{2.32}$$

The Phase Transfer Function can therefore be expressed as:

$$H(s) = \frac{K_v K_{PD} F(s)}{s + K_v K_{PD} F(s)} \tag{2.33}$$

In addition to the Phase Transfer Function, an Error Transfer Function, $H_e(s)$ can also be defined which is given by:

$$H_e(s) = \frac{\theta_e(s)}{\theta_1(s)} = \frac{s}{s + K_v K_{PD} F(s)} \tag{2.34}$$

2.4 Digital Phase Locked Loop (DPLL)

The block diagram of a DPLL is shown in Figure 2.16. The difference between the DPLL and APLL lies in the implementation of the Phase Detector. The Phase Detector in a DPLL can be implemented using the Digital Phase Detectors namely the EXOR gate, J K Flip Flop or using a Phase Frequency Detector (PFD).

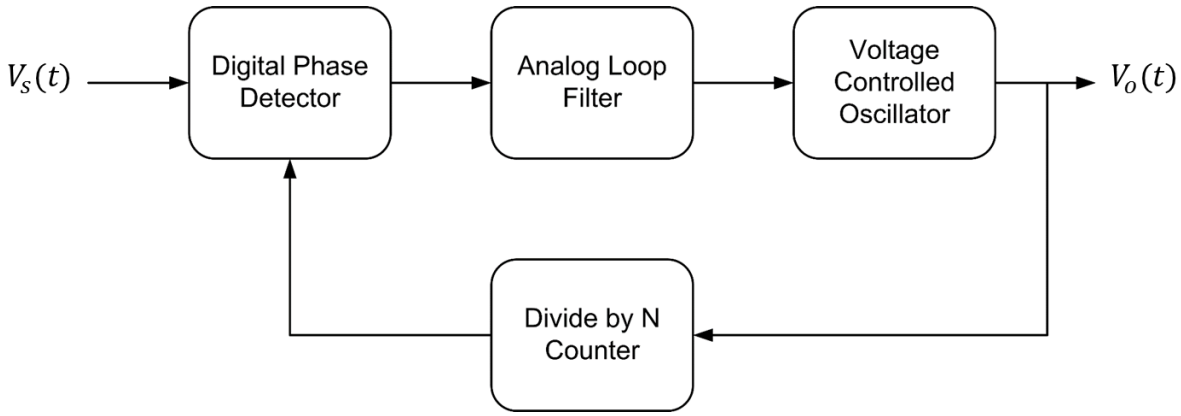


Figure 2.16 Block Diagram of a Digital Phase Locked Loop (DPLL)

2.5 All Digital Phase Locked Loops

2.5.1 Introduction

The All Digital Phase Locked Loop (ADPLL) aims at eliminating all the analog circuitry. In contrast to the Digital Phase Locked Loop (DPLL), it is "fully digital". The all-digital phase locked loops offer better scalability and portability. Existing standard cell implementations can be used for the all-digital PLL blocks. The term "digital" in an ADPLL signifies two things: Firstly, the components of an ADPLL are entirely digital.

Secondly, the signals associated with the different blocks are also digital and could be binary or bit signals or word signals such as the digital code word output of a data register or n-bit output word of a counter [1].

ADPLLs offer some advantages compared to Analog or Charge Pump Phase Locked Loops with respect to simplicity and flexibility of the design. But these loops also have some limitations when it comes to characteristics such as jitter performance or locking range. The goal of this work was to design a fully Digital Phase Locked Loop that can match or exceed the performance of the Analog PLLs. Some ADPLLs may also use a Digitally Controlled Oscillator (DCO) in contrast to its analog counterpart: the Voltage Controlled Oscillator (VCO). The following section explores some of the possible digitized phase detectors, loop filters and DCO implementations used in ADP LLs.

2.5.2 Basic Building Blocks of an ADPLL

2.5.2.1 Digital Phase Detector

The Digital Phase Detectors discussed in Section 2.2.1 can also be extended for ADPLLs when digital word signals instead of bit signals are used. A Flip Flop (FF) counter based PFD uses an edge triggered SR Flip Flop in combination with a counter [1]. The output of the FF is used to gate the high frequency clock signal into the counter. The content of the counter is proportional to the phase error (Be). Another phase detector is the Nyquist Rate Phase Detector (NRPD), which is used if the input is an analog signal [1]. The analog signal is converted into a digital

signal using an Analog to Digital Converter (ADC) sampled at a rate greater than the Nyquist rate. The name stems from the Nyquist theorem, which states that a sampled signal can be reconstructed only when the sampling rate is more than twice the highest frequency component of the signal. Other kinds of PD include the Hilbert Transform Phase Detector and the Digital Averaging Phase Detector discussed in [1]. These are suitable for Software PLL (SPLL) implementations.

2.5.2.2 Digital Loop Filter

The all-digital implementations of the loop filter do not have passive elements such as resistors or capacitors. The UP/DOWN Counter is the simplest type of loop filter, which is used in conjunction with the Phase Frequency Detector (PFD) [1]. The PFD delivers Up/Down pulses based on the comparison between frequencies of the input and the output. These pulses are used to increment or decrement a counter. The Up/Down pulses do not contain information about the magnitude of the phase error. The Up/Down pulses are a result of the relative comparison of the two signals.

A K-Counter Loop filter [1] [31] used in 74HC297 uses two counters, U P and DOWN Counters to generate Carry and Borrow Signals. The Up I Down signal controls the operation of the two counters. If the Up I Down signal is active "high", the DOWN counter is active and if the signal is active "low", the U P counter is active.

Another digital loop filter is the N-before-M counter [1]. It operates in conjunction with a Phase Detector generating Up/Down pulses such as a Phase Frequency Detector. The N-before-M counter uses two counters, the ÷M counter and the ÷N counter. The Carry pulse is generated when a majority of N pulses have been Up pulses. Similarly, the Borrow pulse is generated when a majority of N pulses have been Down pulses. (M > N always).

2.5.2.3 Digitally Controlled Oscillator (DCO)

The DCO is the digital counterpart of the Voltage Controlled Oscillator (VCO) in fully Digital Phase Locked Loops. The N-Counter is used to scale down the signal generated by a fixed high frequency oscillator (f_{REF}). The N-bit output of the Digital Loop filter controls the operation of the DCO. The output of the DCO is given by Equation 2.35.

$$f_{DCO} = \frac{f_{REF}}{N} \tag{2.35}$$

Another popular DCO mechanism called the Increment-Decrement (ID) counter DCO is proposed in [31] which is a modified form of the DCO used in 74HC97 ADPLL. The DCO works in conjunction with a K-Counter Loop Filter or an N-before-M filter that generates the Carry or Borrow signals.

Several DCO approaches have also been proposed in [32] [33] [34]. The first type of DCO is the "Path Delay Oscillator". The Path Delay Oscillator proposed in [32] contains logic gates to form a closed ring oscillator with an odd number of

inversions. The PLL achieves lock by using two tuning mechanisms namely the Coarse and the Fine-Tuning mechanisms. The Coarse Tuning mechanism operates by activating paths such that the frequency of the DCO just exceeds the frequency of the reference clock. When this occurs, the Fine-Tuning mechanism takes control of the lock process to achieve fine resolution. However, the frequency of the Path Delay Oscillator is very limited and is not suitable for high frequency requirements.

The second type of the DCO is the "Schmitt-Trigger Based Current-Driven Oscillator" [33]. A Schmitt-Trigger inverter together with a big capacitor is used to realize the oscillator. The capacitor is usually connected off-chip due to its large value. The external capacitance may make the system complicated and degrade the performance.

The third category is the "Current-Starved Ring Oscillator" to design the DCO [34]. This DCO has good linearity and implemented by using different MOS switches to get different frequencies. However, the DCO is large and needs a lot of hardware. Another approach similar to the current starved technique has been proposed in [35] that uses less hardware and saves half the layout area of the conventional DCO in [34].

2.5.3 Design Criteria

Using more bits for the DCO provides a wider range; however this comes at the cost of increased area, more power dissipation. The lock time of the ADPLLs depends on the implementation. Full Custom design is not required for the ADPLLs. The synthesis tools can be used to simplify the design process. The Integrated Circuit (IC) layout and simulation are also simpler compared to Analog Loops. The design details of the ADPLL using the new techniques will be discussed in detail in the following chapter.

CHAPTER 3 ALL DIGITAL PHASE LOCKED LOOPS

3.1 INTRODUCTION

All Digital Phase Locked Loops (ADPLLs) are more attractive than the Analog PLLs since they offer better flexibility and portability. For portable or mobile applications, lock time is very important since the PLL must support fast exit and entry from power management techniques. The ADPLLs have the characteristic of fast frequency locking, full digitization and good stability. Chapter 2 discussed some of the implementations of the ADPLLs reported in [30] [34] [36] [37] using Digitally Controlled Oscillator (DCO) techniques. This chapter describes an All-Digital Phase Locked Loop using a twin Vernier delay line Time to digital converter (TDC) based PD. Section 3.2 presents the building blocks of the ADPLL. Some target specifications for this ADPLL include:

- Fast Lock Time
- Phase Locking and Wide Operating Range
- Reduced Silicon Area

3.2 BUILDING BLOCKS OF ADPLL

Figure 3. 1 depicts the block diagram of an All-Digital Phase Locked Loop. The ADPLL consists of the following blocks:

- Phase Detector (PD)
- Lock Detection And Control (LDC)
- Digitally Controlled Oscillator (DCO)

The PFD compares the phases of the reference signal (Ref_clk) and the feedback signal ($feedback\_clk$). The Phase Detector uses two TDC's to calculate the phase difference between the reference signal and the feedback signal. A thermometer code representing the timing difference between the reference and the feedback signal is asserted after each phase comparison. The Lock Detection and Control Unit detects the locking and changes the Frequency Tuning Code (FTC) based on the output of the PFD.

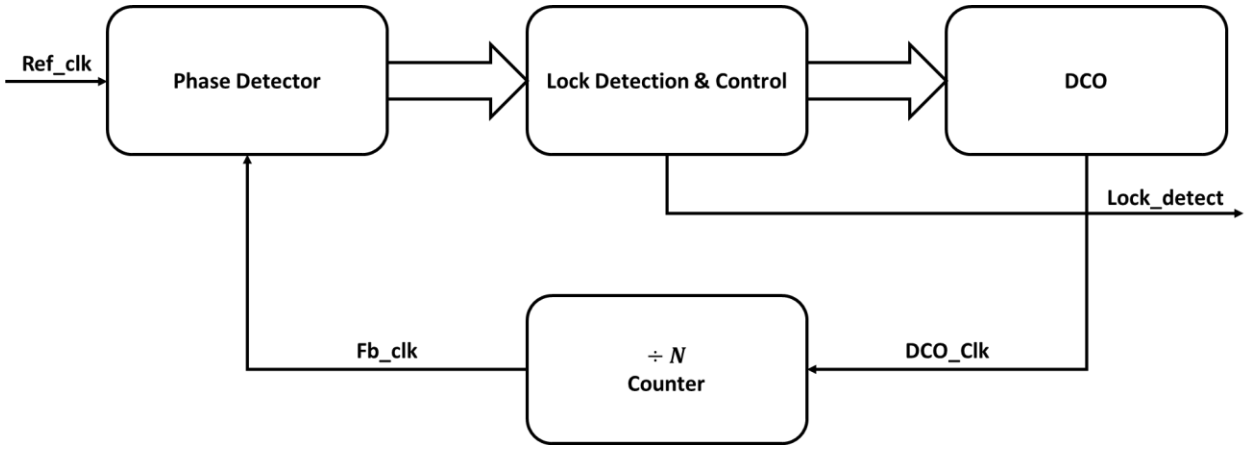


Figure 3.1 Block Diagram of an All-Digital Phase Locked Loop (ADPLL)

The clock output from the Digitally Controlled Oscillator (DCO) forms the core of the ADPLL. The output frequency of the DCO depends on the Frequency Tuning Code. When the REF_Clk and Fb_Clk signals are locked, the Lock Detection Control Unit asserts the Lock_detect signal High. The output of the Phase Detector determines whether the Frequency Tuning Code has to be incremented or decremented. Arithmetically incrementing or decrementing the Tuning Word modulates the DCO Frequency. The DCO_Clk is then fed to digital counter that divides the DCO clock frequency by N and produces a feedback clock Fb_Clk whose frequency is comparable to that of the reference clock Ref_Clk which is fed back to the phase detector block of ADPLL.

3.2.1 All Digital Phase Detector

The main components of the all-digital phase detector are as follows:

- VDL based Time to Digital converter.
- Nand gate.

3.2.1.1 VDL Based Time to Digital Converter

Vernier TDC allows to overcome the technology limitation on time resolution. In a Vernier TDC two delay lines are used to delay both input signals, as depicted in Figure 3.2.

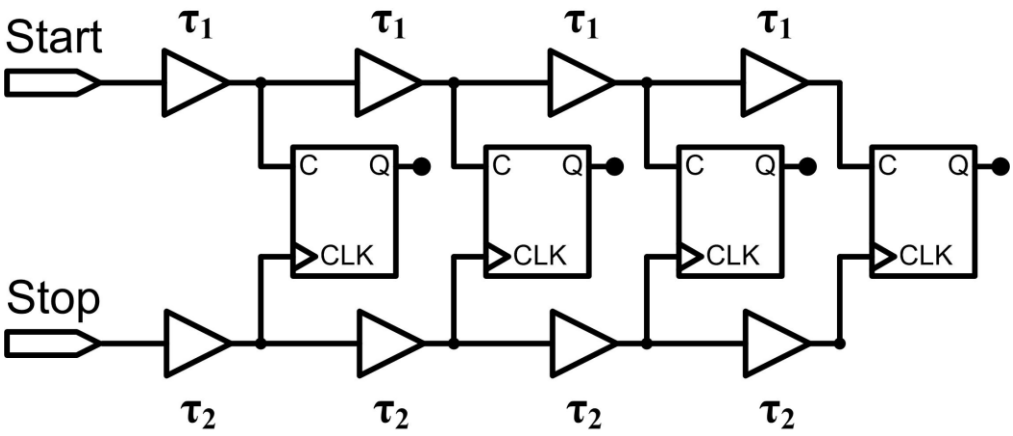


Figure 3.2 Vernier TDC schematic

In a Vernier scale (Figure 3.3), a differential delay Δ between two corresponding taps of the lines is accumulated after each stage so that a signal edge, which lags a reference edge by $n.\Delta$ at the input of the Vernier, will be lined up with it after n stages.

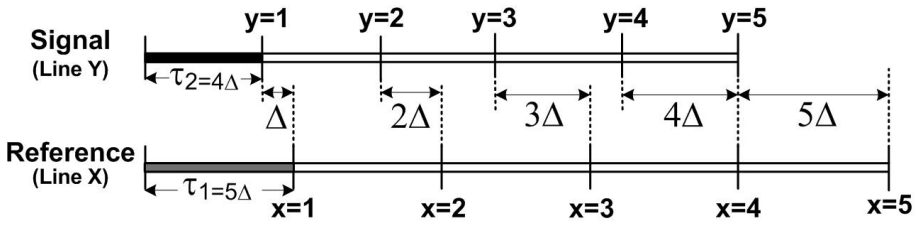


Figure 3.3 Vernier Scale

Since the reference scale is made of relative delays, the TDC time resolution is not technology limited by the smallest reliable delay available in the technology. The TDC time resolution is limited only by the accuracy of the delay element, which can be arbitrarily enhanced at cost of area and power.

The All Digital Phase Detector (ADPD) compares the phases of the REF_Clk and Fb_Clk respectively. The block diagram of the Phase Frequency Detector is shown in Figure 3.4.

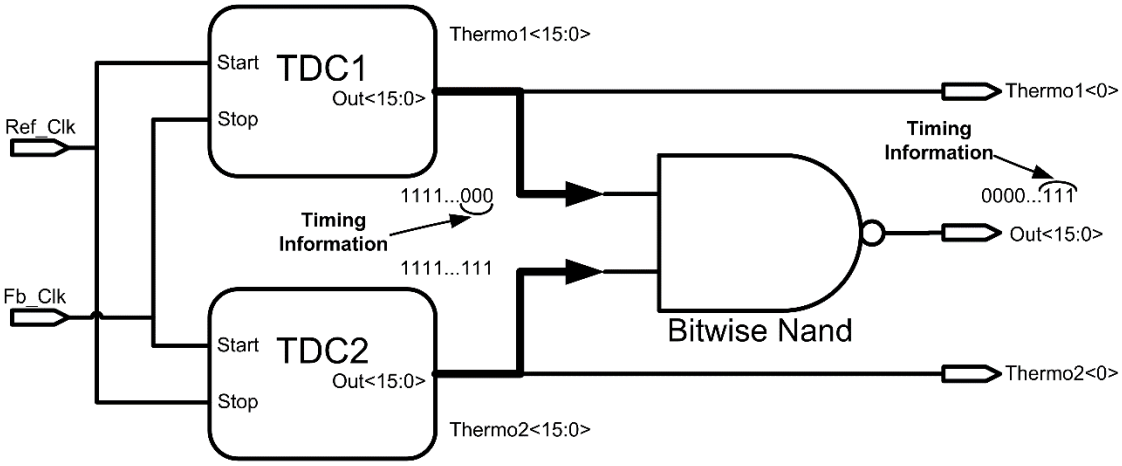


Figure 3.4 Schematic of Phase Detector

The ADPD consist of two VDL-TDC's. TDC1 converts the delay between the Ref_Clk and the Fb_Clk into an N-bit digital thermometer code in which the number of zeroes represent the delay between the Ref_Clk and the Fb_Clk. TDC2 converts the delay between the Fb_Clk and the Ref_Clk into an N-bit digital thermometer code in which the number of zeroes represent the delay between the Fb_Clk and the Ref_Clk.

Clearly we can see that only one of the TDC's will get the timing information while the other TDC will have no timing information and the output of that TDC will have all the bits in High state ie.,'1'. These two thermometer codes are then fed to an N-bit Nand gate which performs a bitwise Nand operation on both and provides an N-bit output in which the number of bits in high state represent the timing information as shown in Figure 3.4.

3.2.2 Lock Detection And Control

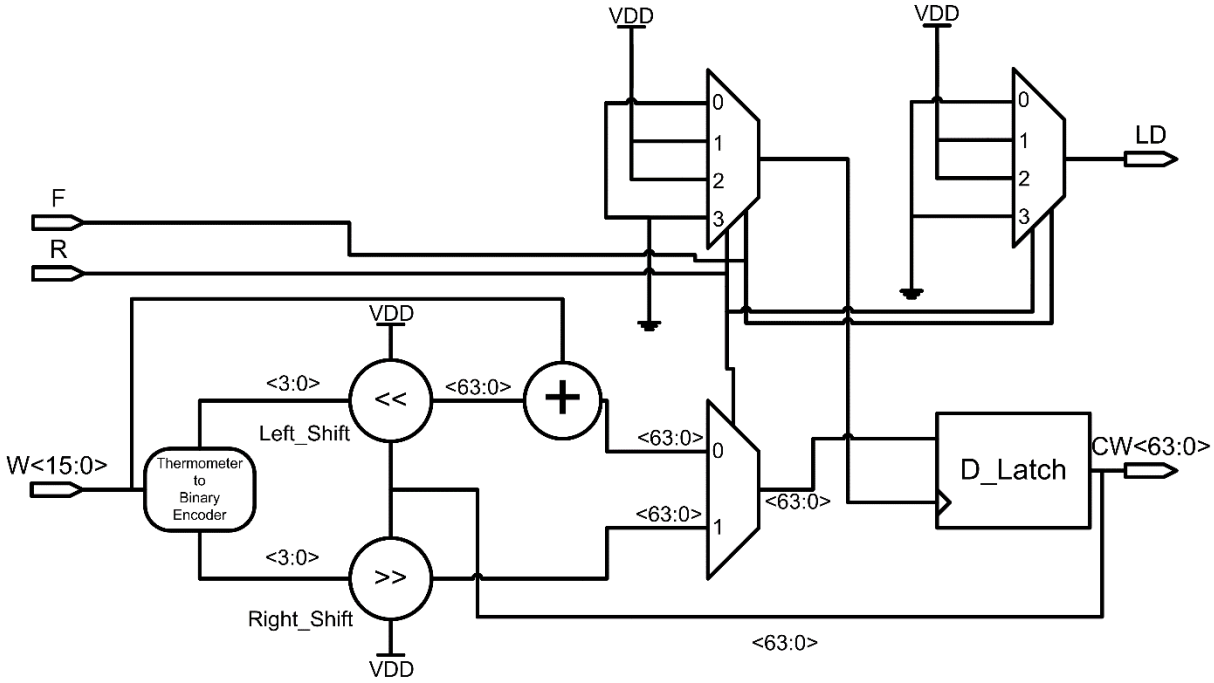


Figure 3.5 Lock detection and control Unit

Figure 3.5 shows the Lock Detection and Control block. The Lock detection and control block detects the Locking of the PLL and also asserts the Frequency tuning code for controlling the DCO frequency. It consists of three input signals F, R and W and two output signals CW and LD. First, it checks the value of the F and R bits. If {F,R} = 00 then this block performs no operation and asserts the previous value of the CW and then makes the LD pin Low. If the {FR} = 01 then this means that the Ref_Clk is leading than Fb_Clk so we have to increase the frequency of the Fb_Clk. Hence, we left shift the CW by the number of high bits present in the input thermometer code. If the {FR} = 10 then this means that the Ref_Clk is lagging than Fb_Clk so we have to decrease the frequency of the Fb_Clk. Hence, we right shift the CW by the number of high bits present in the input thermometer code. The behavioral code of the operation explained above is written in Verilog language and it is provided at the end of the thesis.

Table 3.1 Different Cases for F and R

F	R	Inference of the LDC Block
0	0	Invalid, Perform no operation
0	1	Ref_Clk is leading, Increase Fb_Clk Frequency
1	0	Ref_Clk is lagging, Decrease Fb_Clk Frequency
1	1	Ref_Clk is in phase with Fb_Clk, Make LD = 1

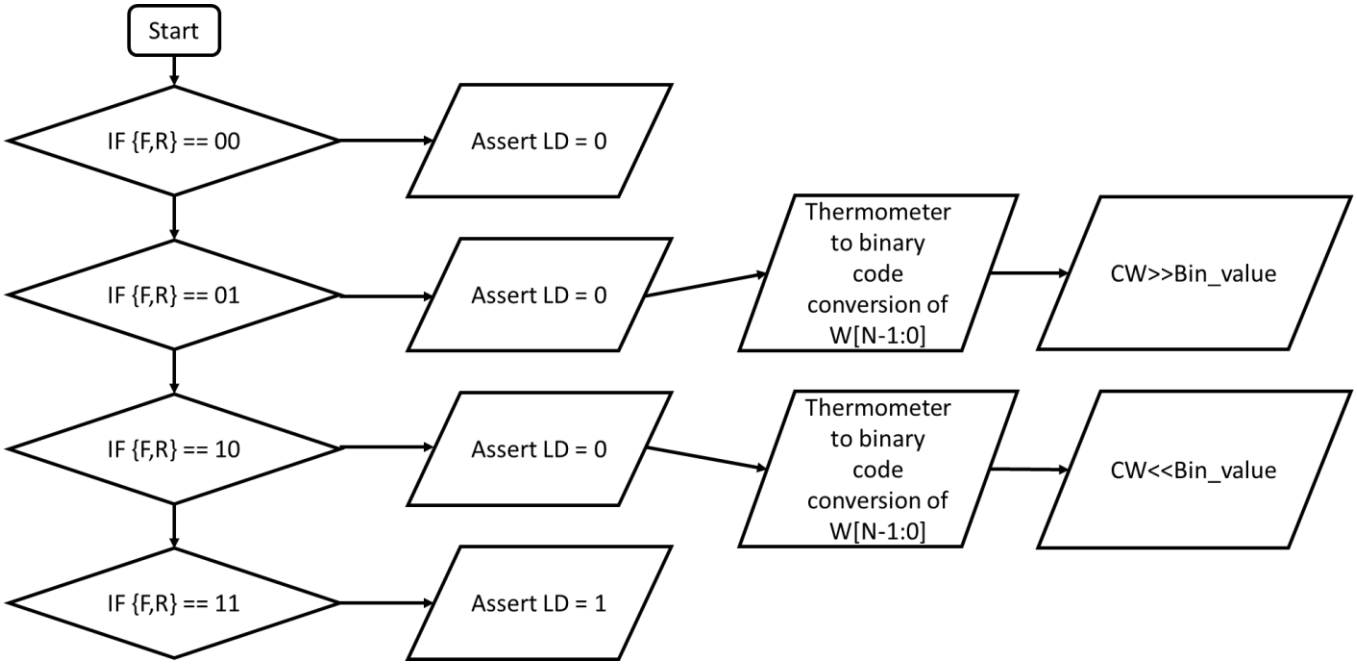


Figure 3.6 Flow chart of LDC Block

3.2.3 Digitally Controlled Oscillator (DCO)

The DCO is a key component in an ADPLL, which is a replacement of the conventional voltage or current controlled oscillator is shown in Figure 3.7. They are more exible and usually more robust than the conventional VCO.

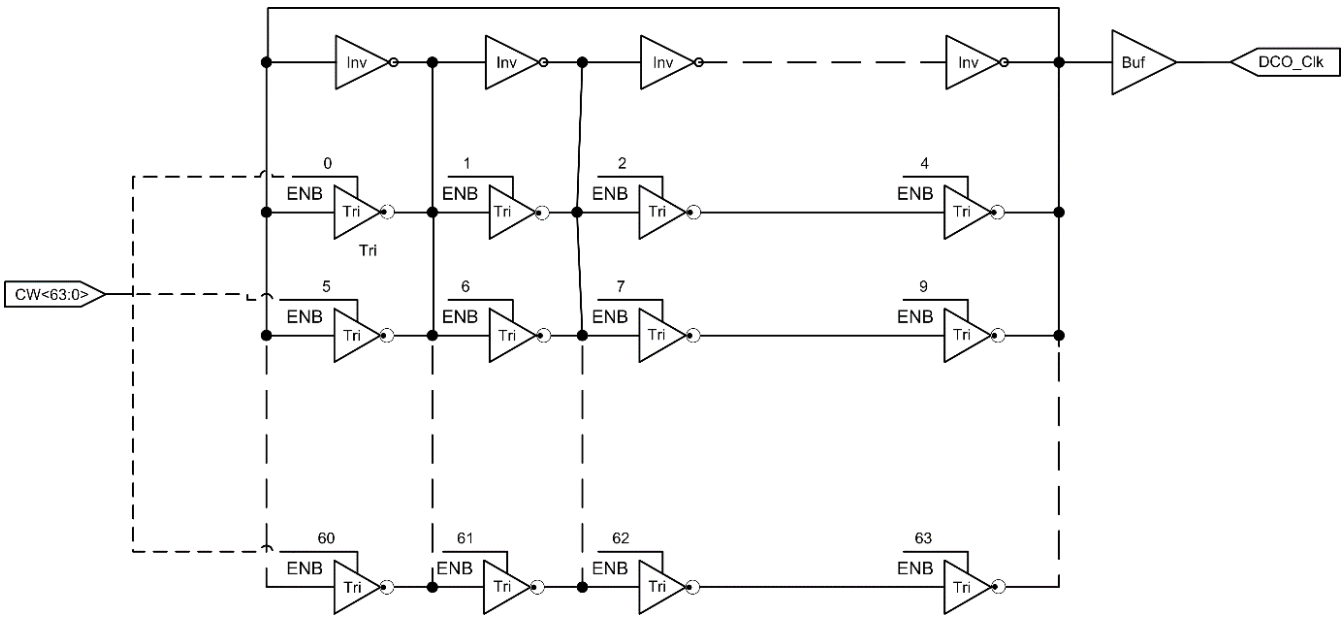


Figure 3.7 DCO Circuit Schematic

DCOs are distinguished from one another by the actual oscillators, which are usually LC tank based or ring-based. The LC-tank oscillator is based on resonance between L and C components in the circuit. In LC tank based RO's, the oscillating frequency changes with digital control word because different number of capacitors are active in the capacitor bank corresponds to different control word to resonate with the inductor

during circuit operation. On the other hand, the ring-based topology is based on the resonance of odd number of inverting gates tied in a loop fashion. Control words are applied to adjust the number of inverting gates in the ring or the delay of each inverting gate to manipulate the frequency of oscillation. Even though LC-tank based oscillators have good inherent phase noise performances, ring-based DCOs are chosen for the purpose of this work because they are more digital intensive in nature and easier to integrate.

3.2.3.1 DCO Design Metrics

Frequency tuning range, tuning linearity and tuning resolution are three major design metrics of DCOs. Frequency tuning range is defined as the frequency span from the minimum to the maximum control words.

$$\Delta f = f_{MAX} - f_{MIN} \tag{3.1}$$

Frequency resolution is the maximum frequency tuning step the DCO takes when the control word is being adjusted by 1 least significant bit (LSB) throughout the whole sweeping range, which is always in the unit of Hz/LSB. Frequency tuning linearity is evaluated by whether the output frequency of oscillation changes linearly with the change of control word, i.e. whether the frequency resolution remains constant throughout the whole span of control words. DCOs could have drastically different frequency tuning linearity's, but generally speaking, the better frequency tuning linearity the DCO is, the better it is. In addition, as with PLLs and delay-locked loops (DLLs), phase jitter, the amount of phase fluctuation of the output clock signal, is also a very important metric to evaluate a DCO.

Linear frequency tuning of the DCO is commonly required when the DCO is used in the ADPLL. Because it guarantees low hardware complexity in the control circuit to calculate the control word corresponding to a certain oscillating frequency.

CHAPTER 4 Results And Discussion

4.1 INTRODUCTION

Previous chapter discussed the different blocks of the ADPLL and the implementation details. This chapter is divided into two sections: Section 4.1.1 presents the Simulation Results of different blocks of ADPLL. Section 4.1.2 presents the Simulation Results of the ADPLL. The Register Transfer Level (RTL) Verilog codes and the test benches are included in the Appendix A.

4.1.1 Simulation Results for different blocks of ADPLL

4.1.1.1 Time to digital converter

Figure 4.1 shows the schematic capture view of the Vernier delay line based time to digital converter when Ref_Clk period = 40ns and the Fb_Clk period = 42ns. The Ref_Clk is connected to the Start pin of the VDL-TDC and the Fb_Clk is connected to the Stop pin of the VDL-TDC and the output is generated, which is a thermometer code containing the timing information in the form of number of zeroes in the thermometer code.

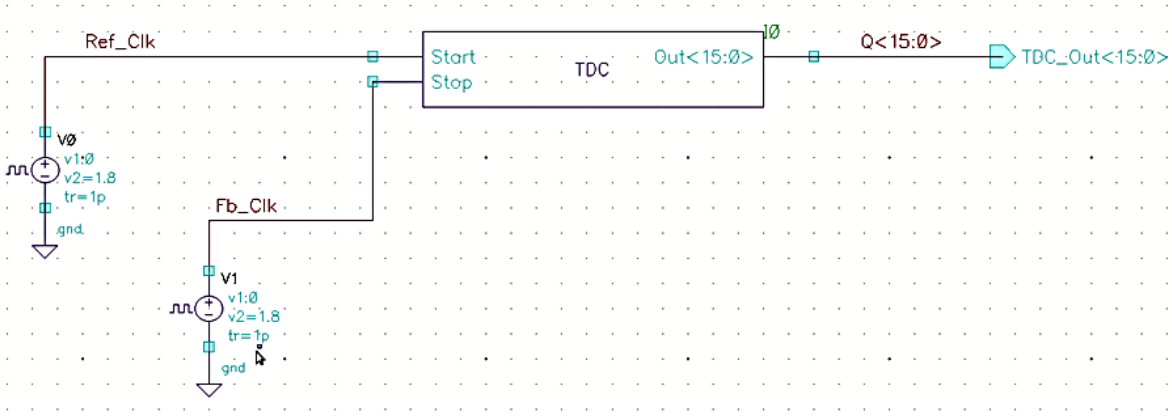


Figure 4.1 Schematic of Time to digital converter

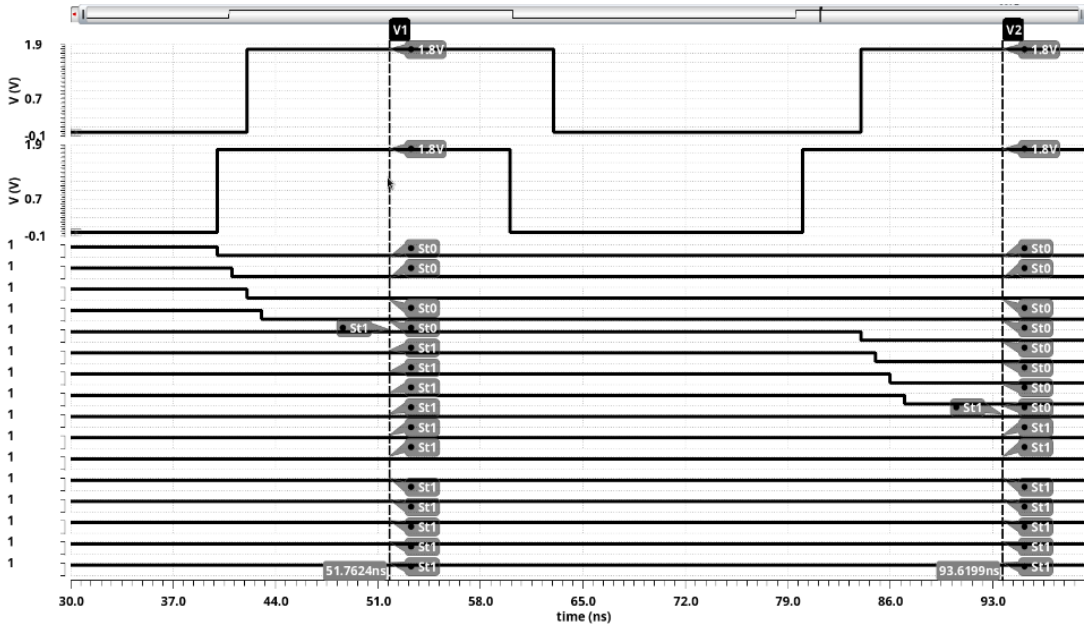


Figure 4.2 Simulation Results of TDC

In Figure 4.2 the simulation results of the circuit shown in Figure 4.1 is shown. We can see that the difference in the phase of the Ref_Clk and the Fb_Clk is 2ns. The output of the TDC i.e. Q [15:0] = 1111111111110000. The difference in the buffer chain of start and stop side is 0.5ns i.e. $\Delta = 0.5ns$. So according to the theory discussed in Section 3.2.1.1, the delay between the Ref_Clk and the Fb_Clk is $n.\Delta$ where n is the number of zeroes in the output of the TDC i.e. n=4. Hence the theoretical delay is $4 \times 0.5 = 2\,ns$, which matches with the actual simulation results.

4.1.1.2 Proposed Phase detector

Figure 4.3 shows the schematic capture view of the Proposed Digital Phase Detector. The Ref_Clk is provided with the clock signal of a period of $40ns$ and the Fb_Clk is provided with the clock signal of period of $42ns$. The Ref_Clk signal is connected to the start pin of the TDC1 and stop pin of the TDC2 and the Fb_Clk is connected to the stop pin of the TDC1 and start pin of the TDC2 as shown in the Schematic.

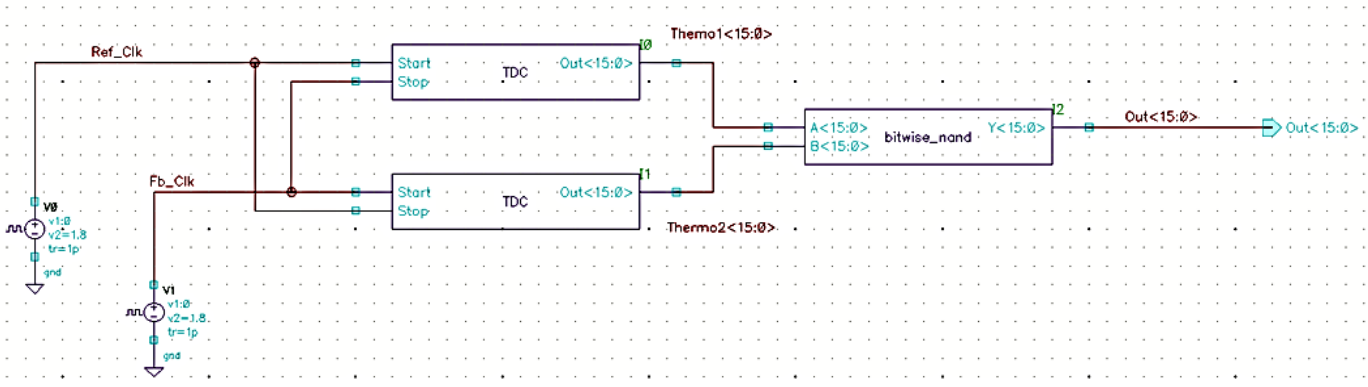


Figure 4.3 Phase Detector schematic

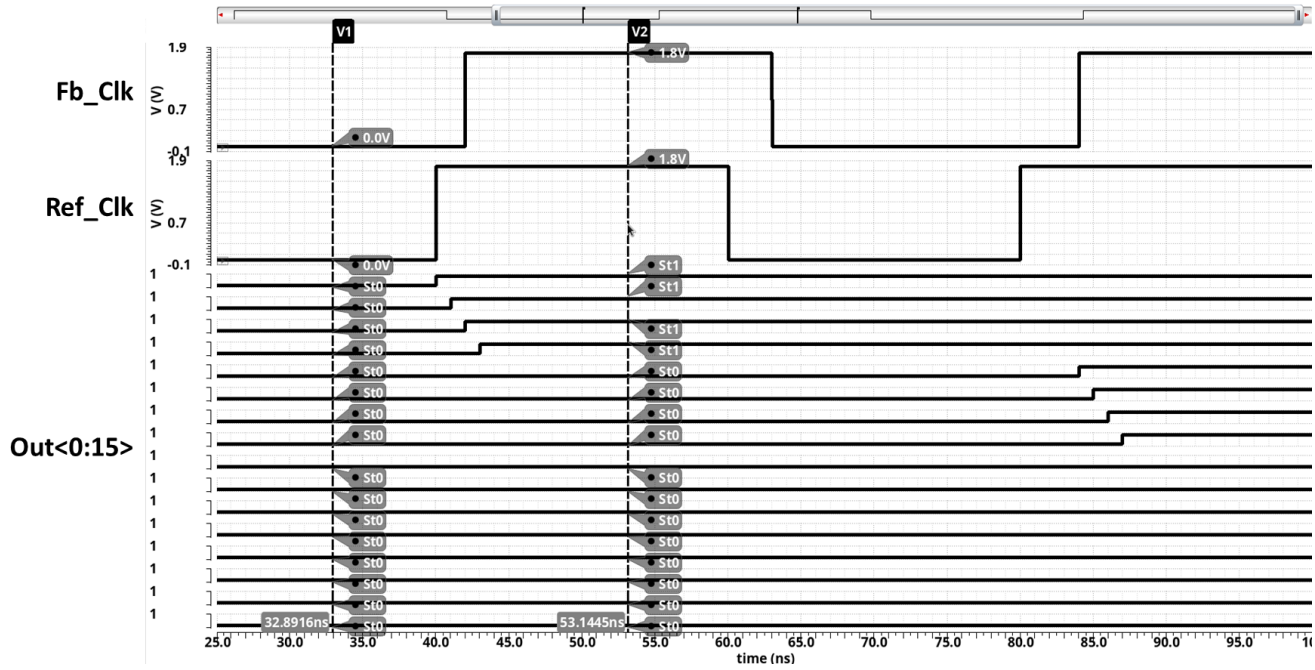


Figure 4.4 Phase Detector simulation

As we can see in the simulation results of the previous TDC structure with same inputs, the output of that same TDC will be same. Hence, the output of the TDC1 i.e. Thermo1 [15:0] = 1111111111110000. But, the inputs in the TDC2 block are inverted i.e. the Ref_Clk in connected to the Stop pin and the Fb_Clk is connected to the start pin of the TDC2. Hence, the output of the TDC2 will contain all 1's as its output because the delay between the two signals will keep on increasing i.e Thermo2 [15:0] = 1111111111111111. These two thermometer codes are then passed through Nand gates which performs the bitwise Nand operation on these two thermometer signals. And hence, we get our final thermometer code word i.e. Out [15:0] = 0000000000001111.

4.1.1.3 Proposed Lock Detection and control

Figure 4.5 shows the schematic capture view of the proposed Lock detection and control unit. The output of the all-digital phase detector goes as an input to the Lock detection and control unit.

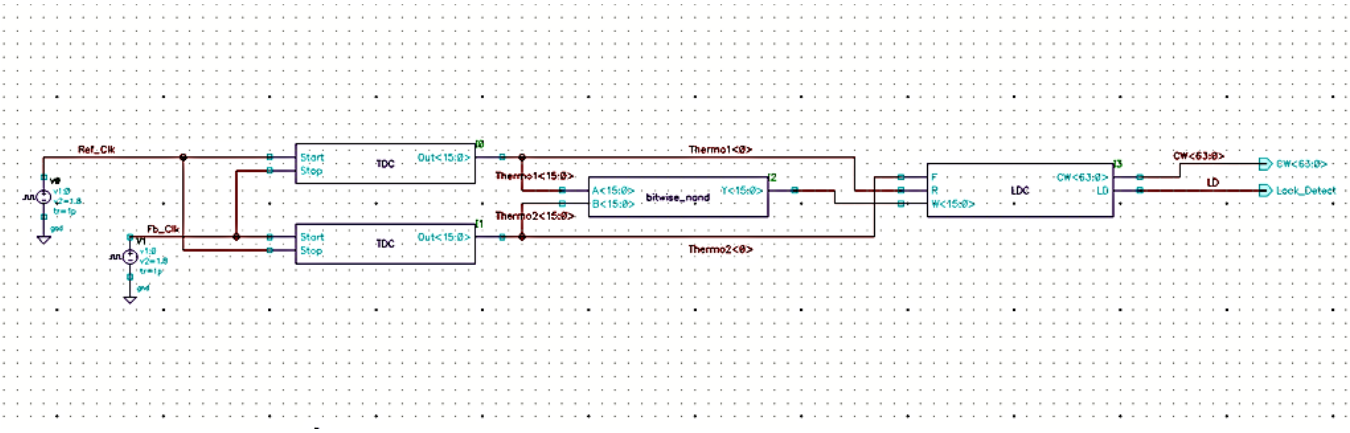


Figure 4.5 Lock Detection and Control (LDC) with ADPD Schematic

[35]

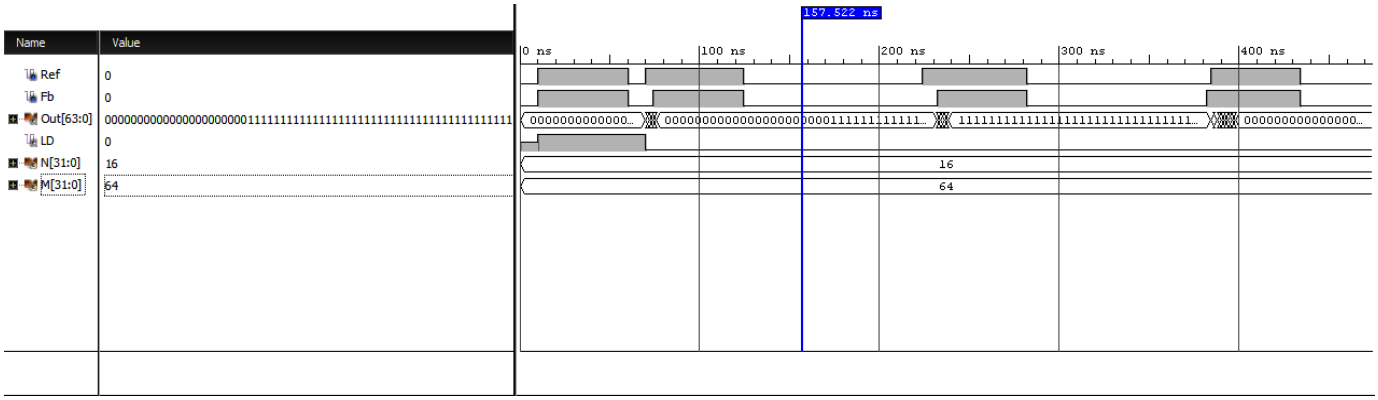


Figure 4.6 Vivado simulation of Lock Detection and Control Unit

Figure 4.6 Shows the Simulation Results of the Lock detection and control Unit. It shows that as the difference in clock pulses of Ref_Clk and Fb_Clk increases the output control word CW [63:0] increases or decreases depending upon the leading and lagging of the Ref_Clk with respect to Fb_Clk.

4.1.1.4 Digitally Controlled Oscillator

Figure 4.7 shows the schematic circuit of the digitally controlled oscillator. There are 5 number of inverter stages used in this design and a 5 by 13 matrix of tristate inverters.

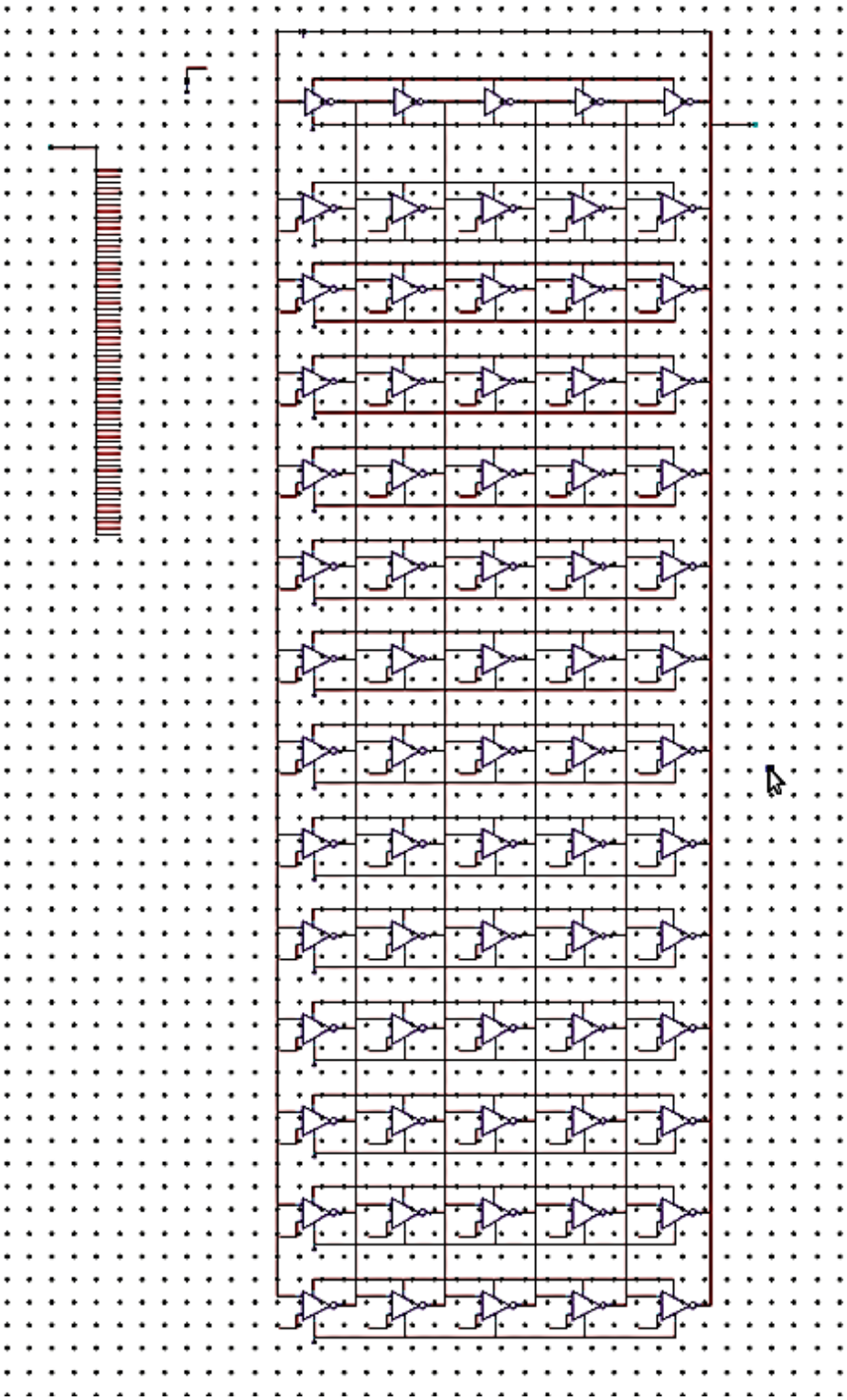


Figure 4.7 DCO Schematic Circuit

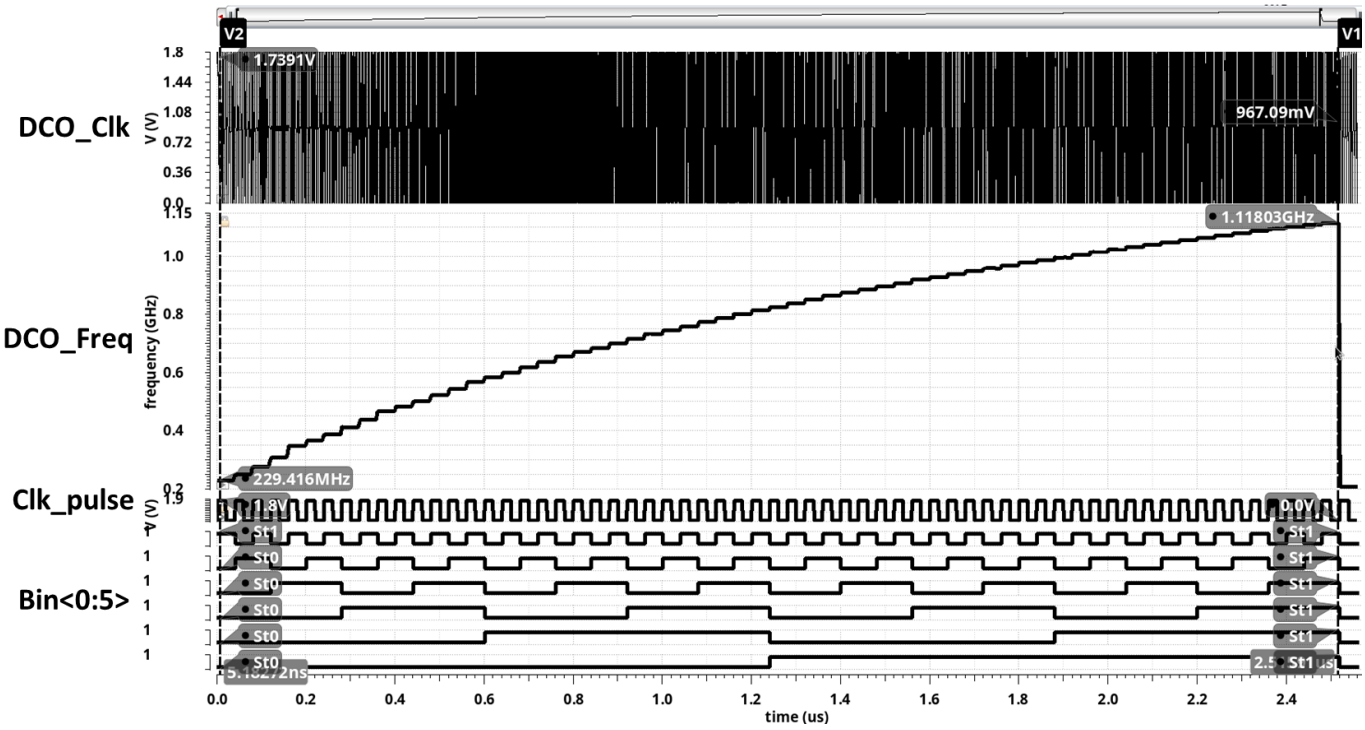


Figure 4.8 DCO Simulation Results

Figure 4.8 shows the simulation results of the DCO. To obtain these results, a binary counter and a binary to thermometer code converter is used. A clock pulse is fed to binary counter block which increments the binary code which is fed to the binary to thermometer code converter, and a thermometer code is generated, which is fed as an input to the DCO block. As the value of the thermometer code increases after every clock cycle, the frequency of the DCO clock signal also increases monotonically.

Table 4.1 DCO Parameters

Parameters	Value (MHz)
Minimum Frequency	229.416
Maximum Frequency	1118.03
Centre Frequency	828.575
Dynamic Range	870.579

Table 4.1 shows various DCO design parameters that are calculated after designing the DCO. We can see that the minimum frequency produced by the DCO is 229.421 MHz. The Maximum Frequency produced by the DCO is 1.11786 GHz. Its Center frequency is 828.575 MHz.

4.1.2 ADPLL Simulation Results

The test bench for the top module of the ADPLL instantiates the device under test (DUT), creates the required clock signals and inputs the test vectors into the device. Figure 4.9 shows the input, output and intermediate ports of the different blocks of the ADPLL and the top-level signals of the ADPLL.

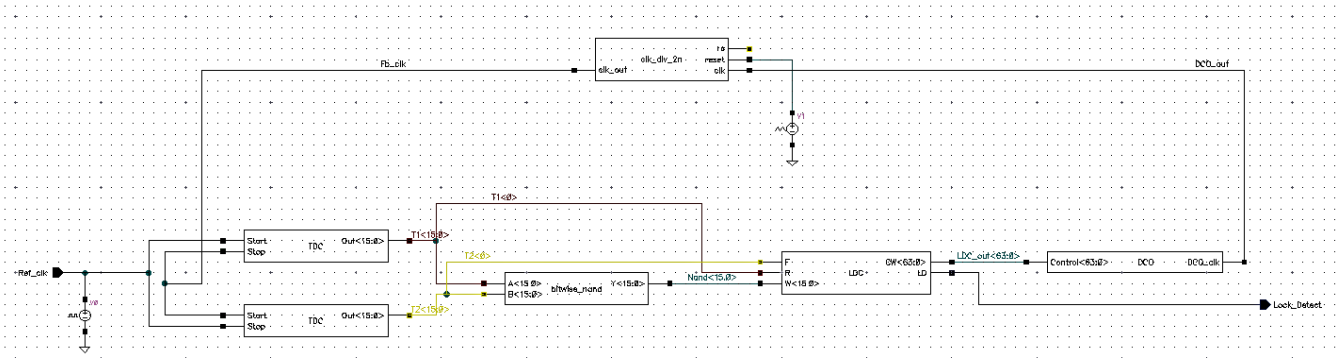


Figure 4.9 ADPLL Schematic view

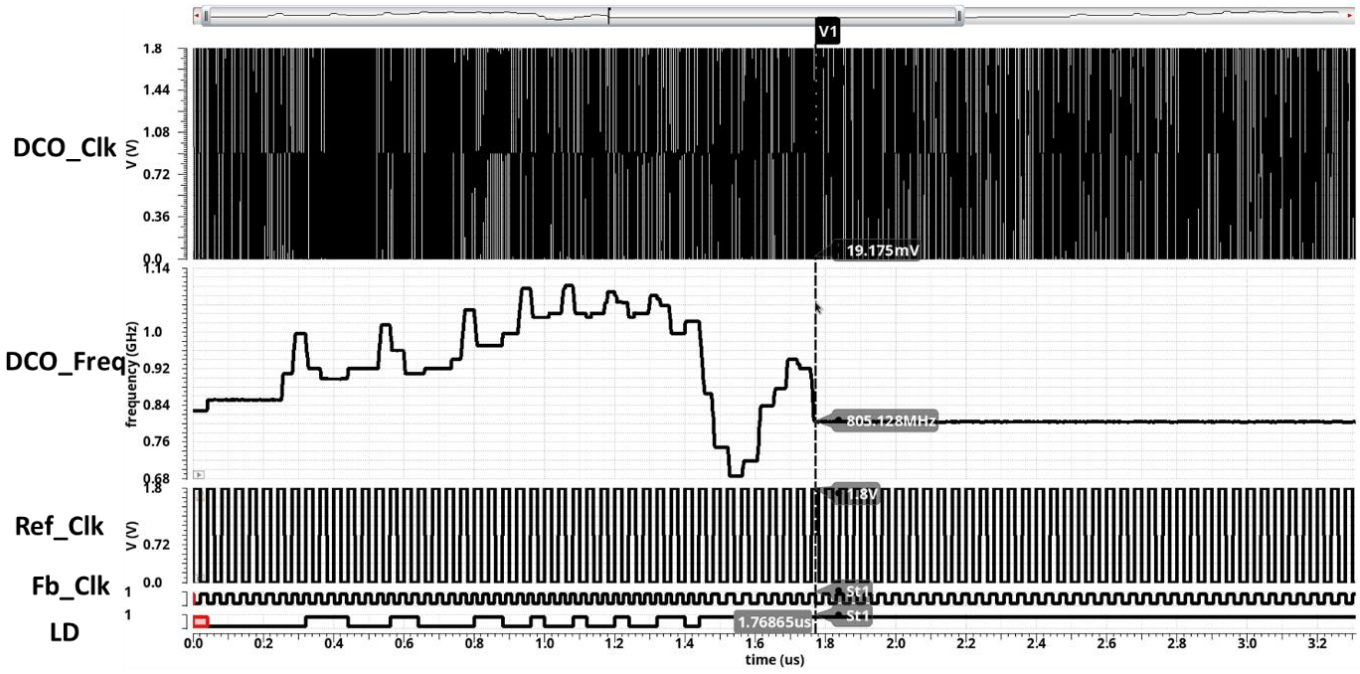


Figure 4.10 ADPLL Simulation Results

Figure 4.10 shows the Simulation Results of the ADPLL. We can see that the Locking time of the ADPLL is 1.7687μs and it takes around 45 clock cycles of the Ref_Clk to Lock the DCO's Clock with the Ref_Clk. The rms-jitter of the ADPLL is also calculated and is reported to be equal to 7.875ps. The total Area of the core of the ADPLL is calculated to be equal to 30.958 μm^2 after implementation. The total power consumption of the ADPLL is calculated to be equal to 11.606mW.

Table 4.2 Comparison table for different chahrachteristics of ADPLL

Parameter	**This Work**	[38]	[39]	[40]	[41]	[42]	[43]	[44]	[45]
Type	**ADPLL**	ADPLL	ADPLL	DPLL	ADPLL	ADPLL	ADPLL	ADPLL	ADPLL
CMOS Process(nm)	**180nm**	180nm	130nm	180nm	130nm	22nm	180nm	22nm	28nm
Supply	**1.8**	1.8	1.2	1.8	NA	0.5-1.0	1.8	1	1
Oscillator	**Ring Osc.**	Ring Osc.	Ring Osc.	LC Osc.	Ring Osc.	Ring Osc.	Ring Osc.	Ring Osc.	Ring Osc.
Freq Range	**0.23 - 1.118 GHz**	0.2539-1.367 GHz	0.3-1.4 GHz	9.75-10.17 GHz	0.6-2 GHZ	0.3-3.2 GHz	NA	0.6-3.6 GHz	0.083-2 GHz
Locking Time	**1.76us**	2.9184 us	7.5u	6.89u	4	2.31	22.5	<12	<1
Locking Time (cycles)	**~45 cycles**	57	375	276	800	231	879	NA	<50
Power(mW)	**11.6m W**	35mW	16.5m W	7.1mW	15.7 @ 1.6 GHz	3.4 @ 3.2 GHz	9 @ 1.25 GHz	18.4	0.64
Area(mm2)	**0.031**	0.7735	0.2	0.352	0.27	0.017	0.348	0.0296	0.00234
RMS jitter	**7.875ps**	3.7ps	3.7 @ 1.35 GHz	0.9ps @ 9.9 GHz	13.1 @ 1.6 GHz	6 @ 3.2 GHz	5.8907 @ 1.25 GHz	10	31
Divide ratio	**32**	13-70	27	248		30	32	NA	40

CHAPTER 5 CONCLUSION

5.1 SUMMARY

This thesis discussed the basic techniques used for the design of All Digital Phase Locked Loops. A modified ADPD has been proposed along with Lock detection and control circuit that reduces the locking time and has less jitter over some of the existing published work. The design was implemented using $0.18\ \mu m$ CMOS technology. The contributions of this work include:

- Designing of an All-Digital Phase Locked Loop (ADPLL) using a Vernier delay line based time to digital converter an All-Digital Phase Detector (ADPD) with a faster locking time.
- Designing of an All-Digital Phase Locked Loop (ADPLL) using digital components so as to make the design scalable and portable.

5.2 FUTURE WORK

Although the design has been verified at all levels and satisfactory results were obtained, a great deal of improvement could be made to enhance the performance of the existing design.

Firstly, the design of an All-Digital PLL that presents a better jitter performance could be considered which is extremely critical in some applications.

Also, in some applications it might be necessary to convert the square wave digital output to a sine wave output. Hence it might be necessary to use a Digital to Analog Converter (DAC) to support such applications.

As the feature size of the CMOS technology shrinks down and the clock frequency is increased, these techniques have to be pursued to achieve robust performance over process, supply voltage and temperature variations.

In addition to the design concepts of the ALL Digital Phase Locked Loops, this thesis also presents an insight into the comparison between the different implementations: Analog, Digital and All Digital PLLs which provides leads to further research and development in these areas.

CHAPTER 6 LIST OF PUBLICATIONS

1 J.Kaur, P.Prabhakar, A.Singh and A.Agarwal, "A novel fast digital foreground gain error calibration for pipelined ADC" *IET Circuits, Devices & Systems journal*.(communicated)

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APPENDICES

APPENDIX-A: VERILOG RTL CODES

ADPLL: Top Level Module

```
module ADPLL(
   input Ref_Clk,
   output PLL_Clk,
   output LD
   );

   wire [63:0] A;
   wire Fb_Clk;
   wire PLL_Clk1;
   PFALD P1 (.Ref(Ref_Clk),.Fb(Fb_Clk),.CW(A),.LD(LD));
   DCO D1 (.CW(A),.DCO_out(PLL_Clk1));
   clk_div N1 (.clk(PLL_Clk1),.clk_out(Fb_Clk));
   assign PLL_Clk = PLL_Clk1;

endmodule
```

PFALD: Sub-module ADPLL

```
module PFALD #(parameter N= 16, M=64) (Ref,Fb,CW,LD);
   input Ref,Fb;
   output [M-1:0] CW;
   output LD;

   wire [N-1:0] W1,W2,W3;

   TDC #(.N(N)) TDC1 (.Start(Ref),.Stop(Fb),.Out(W1));
   TDC #(.N(N)) TDC2 (.Start(Fb),.Stop(Ref),.Out(W2));
   bitwise_nand#(.N(N)) G1 (.Y(W3),.A(W1),.B(W2));
   LDC#(.N(N),.M(M)) B1 (.R(W1[0]),.F(W2[0]),.W(W3),.CW(CW),.LD(LD));
endmodule
```

VDL-TDC: Sub-module PFALD

```
`timescale 1ns / 1ps
module TDC
   #(parameter N = 16)
   (Start,Stop,Out);
   input Start,Stop;
   output [N-1:0] Out;
   supply0 GND;
```

```
    supply1 VDD;
    wire [N-2:0] A,B;

    buffer1 A1 (A[0], Start);                                    // 1 Buffer
    DFF FF1 (.clk(Start),.D(Stop),.rst(GND),.Q(Out[0]));                    // 1 DFF
    buffer B1 (B[0],Stop);                                    // 1 Buffer
    DFF FFL (.clk(A[N-2]),.D(B[N-2]),.rst(GND),.Q(Out[N-1]));                    //
1 DFF

    buffer1 A2[N-3:0] (A[N-2:1], A[N-3:0]);                          // N-3 Buffers
    DFF    FF[N-3:0]    (.clk(A[N-3:0]),.D(B[N-3:0]),.rst(GND),.Q(Out[N-2:1]));
// N-3 D Flip Flpos
    buffer B2[N-3:0] (B[N-2:1],B[N-3:0]);                          // N-3 Buffers
endmodule
```

Buffer1: Sub-module TDC

```
module buffer1(Y,A);
    input A;
    output Y;

    assign #1 Y = A;
endmodule
```

Buffer: Sub-module TDC

```
module buffer(Y,A);
    input A;
    output Y;

    assign #0.5 Y = A;
endmodule
```

DFF: Sub-module TDC

```
`timescale 1ns / 1ps
module DFF( D, clk, rst, Q, Q_bar );
    input D,clk,rst;
    output Q,Q_bar;

    reg temp;

    always@(posedge clk)
        begin
            if(rst)
                temp = 0;
```

```
            else
                temp = D;
        end

    assign Q = temp;
    assign Q_bar = ~temp;

endmodule
```

Bitwise_nand: Sub-module PFALD

```
module bitwise_nand
    #(parameter N = 16)
    (Y,A,B);
    input [N-1:0] A,B;
    output [N-1:0] Y;

    assign Y = ~ (A & B);

endmodule
```

LDC: Sub-module PFALD

```
`timescale 1ns / 1ps
module LDC
    #(parameter N = 16, M = 64)
    (R,F,W,CW,LD);
    input R,F;
    input [N-1:0] W;
    output [M-1:0] CW;
    output reg LD;

    reg [M-1:0] temp_out = {(M/2){1'b1}};
    reg [N-1:0] count = 0;
    reg [M-2:0] P;
    integer i,j;
//    genvar i,j;

    always@(R,F,W)
        begin
            case({R,F})
                0:
                    begin
                    temp_out = temp_out;
                    LD = 0;
                    end
                1:
```

```
                begin
                    LD = 0;
                    count                                                    =
W[0]+W[1]+W[2]+W[3]+W[4]+W[5]+W[6]+W[7]+W[8]+W[9]+
                          W[10]+W[11]+W[12]+W[13]+W[14]+W[15];
                    temp_out = temp_out<<count;
                    temp_out = temp_out + W;
                end
            2:
                begin
                    LD = 0;
                    count                                                    =
W[0]+W[1]+W[2]+W[3]+W[4]+W[5]+W[6]+W[7]+W[8]+W[9]+
                       W[10]+W[11]+W[12]+W[13]+W[14]+W[15];
                    temp_out = temp_out>>count;
                end
            3:
                begin
                    LD = 1;
                    temp_out = temp_out;
                end
            default:
                begin
                    temp_out = temp_out;
                    LD = 0;
                end
        endcase
    end

    assign CW = temp_out;

endmodule
```

DCO: Sub-module ADPLL

```
module DCO(
    input [63:0] CW,
    output DCO_out
    );
    wire a,b,c,d,e;

    not (b,a);
    not (c,b);
    not (d,c);
    not (e,d);
    not (a,e);
```

```
   notif1 (b,a,CW[0]); notif1 (c,b,CW[1]); notif1(d,c,CW[2]);
notif1(e,d,CW[3]);notif1(a,e,CW[4]);
   notif1 (b,a,CW[5]); notif1 (c,b,CW[6]); notif1(d,c,CW[7]);
notif1(e,d,CW[8]);notif1(a,e,CW[9]);
   notif1 (b,a,CW[10]); notif1 (c,b,CW[11]); notif1(d,c,CW[12]);
notif1(e,d,CW[13]);notif1(a,e,CW[14]);
   notif1 (b,a,CW[15]); notif1 (c,b,CW[16]); notif1(d,c,CW[17]);
notif1(e,d,CW[18]);notif1(a,e,CW[19]);
   notif1 (b,a,CW[20]); notif1 (c,b,CW[21]); notif1(d,c,CW[22]);
notif1(e,d,CW[23]);notif1(a,e,CW[24]);
   notif1 (b,a,CW[25]); notif1 (c,b,CW[26]); notif1(d,c,CW[27]);
notif1(e,d,CW[28]);notif1(a,e,CW[29]);
   notif1 (b,a,CW[30]); notif1 (c,b,CW[31]); notif1(d,c,CW[32]);
notif1(e,d,CW[33]);notif1(a,e,CW[34]);
   notif1 (b,a,CW[35]); notif1 (c,b,CW[36]); notif1(d,c,CW[37]);
notif1(e,d,CW[38]);notif1(a,e,CW[39]);
   notif1 (b,a,CW[40]); notif1 (c,b,CW[41]); notif1(d,c,CW[42]);
notif1(e,d,CW[43]);notif1(a,e,CW[44]);
   notif1 (b,a,CW[45]); notif1 (c,b,CW[46]); notif1(d,c,CW[47]);
notif1(e,d,CW[48]);notif1(a,e,CW[49]);
   notif1 (b,a,CW[50]); notif1 (c,b,CW[51]); notif1(d,c,CW[52]);
notif1(e,d,CW[53]);notif1(a,e,CW[54]);
   notif1 (b,a,CW[55]); notif1 (c,b,CW[56]); notif1(d,c,CW[57]);
notif1(e,d,CW[58]);notif1(a,e,CW[59]);
   notif1 (b,a,CW[60]); notif1 (c,b,CW[61]); notif1(d,c,CW[62]);
notif1(e,d,CW[63]);notif1(a,e,CW[63]);

   buf (DCO_out,a);
endmodule
```

Clk_div: Sub-module ADPLL

```
module clk_div
#(
parameter WIDTH = 16, // Width of the register required
parameter N = 16// We will divide by 32 for example in this case
)
(clk,reset, clk_out);
input clk;
input reset;
output clk_out;
reg [WIDTH-1:0] r_reg;
wire [WIDTH-1:0] r_nxt;
reg clk_track;
always @(posedge clk or posedge reset)
begin
  if (reset)
```

```
    begin
       r_reg <= 0;
    clk_track <= 1'b0;
    end
  else if (r_nxt == N)
       begin
         r_reg <= 0;
         clk_track <= ~clk_track;
       end
  else
     r_reg <= r_nxt;
end
 assign r_nxt = r_reg+1;
 assign clk_out = clk_track;
endmodule
```

APPENCDIX-B

SYNOPSIS DESIGN TOOL REPORTS

Dc-Compiler: Area Report

```
****************************************
Report : area
Design : ADPLL_1
Version: L-2016.03
Date   : Wed Jul 12 18:53:44 2017
****************************************

Library(s) Used:

    tsl18fs120_scl_ff (File:
/cad/cad_FDK/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_scl
_ff.db)

Number of ports:                         1103
Number of nets:                          2380
Number of cells:                         1526
Number of combinational cells:           1238
Number of sequential cells:               185
Number of macros/black boxes:               0
Number of buf/inv:                        305
Number of references:                       3

Combinational area:              24426.490103
Buf/Inv area:                     2113.179991
Noncombinational area:            7303.350208
Macro/Black Box area:                0.000000
Net Interconnect area:            1260.846807

Total cell area:                 31729.840311
Total area:                      32990.687118

Hierarchical area distribution
------------------------------

                                  Global cell area            Local
cell area
                                  ------------------  -------------
----------------
Hierarchical cell                 Absolute    Percent  Combi-
Noncombi-  Black-
                                  Total       Total    national
national   boxes   Design
-------------------------------- ----------  -------  ----------  -
--------  ------  ----------------------
ADPLL_1                           31729.8403    100.0      0.0000
0.0000  0.0000  ADPLL_1
D1                                 1966.0600      6.2    498.4900
1467.5700  0.0000  DCO
N1                                 1815.8800      5.7    175.6300
1119.6200  0.0000  clk_div
```

```
N1/add_35                              520.6300      1.6    520.6300
0.0000  0.0000  clk_div_DW01_inc_0
P1                                   27947.9003     88.1      0.0000
0.0000  0.0000  PFALD
P1/B1                                25038.1402     78.9   3170.6000
2809.6001  0.0000  LDC_N16_M64
P1/B1/add_30                          3182.9801     10.0   3182.9801
0.0000  0.0000  LDC_N16_M64_DW01_add_0
P1/B1/sll_29                          7771.5801     24.5   7771.5801
0.0000  0.0000  LDC_N16_M64_DW01_ash_0
P1/B1/srl_37                          8103.3800     25.5   8103.3800
0.0000  0.0000  LDC_N16_M64_DW_rash_0
P1/G1                                  200.6400      0.6    200.6400
0.0000  0.0000  bitwise_nand_N16
P1/TDC1                              1354.5600      4.3      0.0000
0.0000  0.0000  TDC_N16_0
P1/TDC1/A1                              0.0000      0.0      0.0000
0.0000  0.0000  buffer1_0
P1/TDC1/A2[0]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_29
P1/TDC1/A2[10]                          0.0000      0.0      0.0000
0.0000  0.0000  buffer1_19
P1/TDC1/A2[11]                          0.0000      0.0      0.0000
0.0000  0.0000  buffer1_18
P1/TDC1/A2[12]                          0.0000      0.0      0.0000
0.0000  0.0000  buffer1_17
P1/TDC1/A2[13]                          0.0000      0.0      0.0000
0.0000  0.0000  buffer1_16
P1/TDC1/A2[1]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_28
P1/TDC1/A2[2]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_27
P1/TDC1/A2[3]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_26
P1/TDC1/A2[4]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_25
P1/TDC1/A2[5]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_24
P1/TDC1/A2[6]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_23
P1/TDC1/A2[7]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_22
P1/TDC1/A2[8]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_21
P1/TDC1/A2[9]                           0.0000      0.0      0.0000
0.0000  0.0000  buffer1_20
P1/TDC1/B1                              0.0000      0.0      0.0000
0.0000  0.0000  buffer_0
--------------------------------  ----------  -------  ----------  -
--------  ------  ----------------------
Total
24426.4901  7303.3502  0.0000
```

Dc-Compiler: Power Report

```
****************************************
Report : power
        -hier
        -analysis_effort low
Design : ADPLL_1
Version: L-2016.03
Date   : Wed Jul 12 18:56:59 2017
****************************************


Library(s) Used:

    tsl18fs120_scl_ff
(File:/cad/cad_FDK/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18
fs120_scl_ff.db)


Operating Conditions: tsl18fs120_scl_ff
Library:tsl18fs120_scl_ff
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
ADPLL_1                35000             tsl18fs120_scl_ff


Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------
-------------
                                       Switch   Int      Leak
Total
Hierarchy                              Power    Power    Power
Power    %
--------------------------------------------------------------------
--------------
ADPLL_1                                   9.769   11.193 4.32e+04
20.963 100.0
  N1 (clk_div)                            0.183    2.685 2.81e+03
2.867  13.7
    add_35 (clk_div_DW01_inc_0)        6.03e-02 7.37e-02  795.230
0.134   0.6
  D1 (DCO)                                8.131    6.651 2.76e+03
14.783  70.5
  P1 (PFALD)                              1.455    1.858 3.77e+04
3.313  15.8
    B1 (LDC_N16_M64)                      1.349    1.552 3.31e+04
2.901  13.8
```

```
      sll_29 (LDC_N16_M64_DW01_ash_0)     0.334    0.524 1.27e+04
0.858   4.1
      add_30 (LDC_N16_M64_DW01_add_0)  6.91e-02    0.157 4.47e+03
0.226   1.1
      srl_37 (LDC_N16_M64_DW_rash_0)      0.450    0.397 7.10e+03
0.847   4.0
    G1 (bitwise_nand_N16)              3.57e-02 3.58e-03  110.640
3.93e-02   0.2
    TDC2 (TDC_N16_1)                   3.69e-02    0.146 2.22e+03
0.183   0.9
      FF[13] (DFF_1)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[12] (DFF_2)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[11] (DFF_3)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[10] (DFF_4)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[9] (DFF_5)                    2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[8] (DFF_6)                    2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[7] (DFF_7)                    2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[6] (DFF_8)                    2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[5] (DFF_9)                    2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[4] (DFF_10)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[3] (DFF_11)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[2] (DFF_12)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[1] (DFF_13)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF[0] (DFF_14)                   2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FFL (DFF_15)                     2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      FF1 (DFF_16)                     2.31e-03 9.14e-03  138.870
1.14e-02   0.1
      A1 (buffer1_15)                     0.000    0.000    0.000
0.000   0.0
    TDC1 (TDC_N16_0)                   3.36e-02    0.155 2.22e+03
0.189   0.9
      FF[13] (DFF_17)                  2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[12] (DFF_18)                  2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[11] (DFF_19)                  2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[10] (DFF_20)                  2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[9] (DFF_21)                   2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[8] (DFF_22)                   2.06e-03 9.71e-03  138.870
1.18e-02   0.1
```

```
      FF[7] (DFF_23)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[6] (DFF_24)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[5] (DFF_25)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[4] (DFF_26)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[3] (DFF_27)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[2] (DFF_28)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[1] (DFF_29)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FF[0] (DFF_30)                    2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      FFL (DFF_31)                      2.06e-03 9.71e-03  138.870
1.18e-02   0.1
      B1 (buffer_0)                        0.000    0.000    0.000
0.000   0.0
      FF1 (DFF_0)                       2.73e-03 9.69e-03  138.870
1.24e-02   0.1
      A1 (buffer1_0)                       0.000    0.000    0.000
0.000   0.0
```

IC-Compiler: Area Report

```
****************************************
Report : area
Design : ADPLL_1
Version: L-2016.03-SP5-1
Date   : Wed Jul 12 21:28:15 2017
****************************************

Library(s) Used:

    tsl18fs120_scl_ff (File:
/cad/cad_FDK/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_
scl_ff.db)

Number of ports:                          3
Number of nets:                          71
Number of cells:                          3
Number of combinational cells:            0
Number of sequential cells:               0
Number of macros/black boxes:             0
Number of buf/inv:                        0
Number of references:                     3

Combinational area:              24021.980103
Buf/Inv area:                     1824.699995
Noncombinational area:            6936.490192
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)
```

```
Total cell area:                30958.470295
Total area:                 undefined

Hierarchical area distribution
------------------------------

                                    Global cell area
Local cell area
                                    -------------------  ----------
------------------
Hierarchical cell                   Absolute    Percent  Combi-
Noncombi-  Black-
                                    Total       Total    national
national   boxes   Design
-------------------------------  ----------  -------  ----------
---------  ------  ----------------------
ADPLL_1                          30958.4703    100.0      0.0000
0.0000  0.0000  ADPLL_1
D1                                1589.7900      5.1    489.0800
1100.7100  0.0000  DCO
N1                                1800.2000      5.8    159.9500
1119.6200  0.0000  clk_div
N1/add_35                          520.6300      1.7    520.6300
0.0000  0.0000  clk_div_DW01_inc_0
P1                               27568.4803     89.0      0.0000
0.0000  0.0000  PFALD
P1/B1                            24846.8202     80.3   3057.7000
2809.6001  0.0000  LDC_N16_M64
P1/B1/add_30                      3182.9801     10.3   3182.9801
0.0000  0.0000  LDC_N16_M64_DW01_add_0
P1/B1/sll_29                      7821.7501     25.3   7821.7501
0.0000  0.0000  LDC_N16_M64_DW01_ash_0
P1/B1/srl_37                      7974.7900     25.8   7974.7900
0.0000  0.0000  LDC_N16_M64_DW_rash_0
P1/G1                              200.6400      0.6    200.6400
0.0000  0.0000  bitwise_nand_N16
P1/TDC1                           1260.5100      4.1      6.2700
0.0000  0.0000  buffer1_20
P1/TDC1/FF1                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_0
P1/TDC1/FFL                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_31
P1/TDC1/FF[0]                       78.3900      0.3     18.8100
59.5800  0.0000  DFF_30
P1/TDC1/FF[10]                      78.3900      0.3     18.8100
59.5800  0.0000  DFF_20
P1/TDC1/FF[11]                      78.3900      0.3     18.8100
59.5800  0.0000  DFF_19
P1/TDC1/FF[12]                      78.3900      0.3     18.8100
59.5800  0.0000  DFF_18
P1/TDC1/FF[13]                      78.3900      0.3     18.8100
59.5800  0.0000  DFF_17
P1/TDC1/FF[1]                       78.3900      0.3     18.8100
59.5800  0.0000  DFF_29
P1/TDC1/FF[2]                       78.3900      0.3     18.8100
59.5800  0.0000  DFF_28
P1/TDC1/FF[3]                       78.3900      0.3     18.8100
59.5800  0.0000  DFF_27
```

```
P1/TDC1/FF[4]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_26
P1/TDC1/FF[5]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_25
P1/TDC1/FF[6]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_24
P1/TDC1/FF[7]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_23
P1/TDC1/FF[8]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_22
P1/TDC1/FF[9]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_21
P1/TDC2                              1260.5100      4.1      6.2700
0.0000  0.0000  TDC_N16_1
P1/TDC2/FF1                            78.3900      0.3     18.8100
59.5800  0.0000  DFF_16
P1/TDC2/FFL                            78.3900      0.3     18.8100
59.5800  0.0000  DFF_15
P1/TDC2/FF[0]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_14
P1/TDC2/FF[10]                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_4
P1/TDC2/FF[11]                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_3
P1/TDC2/FF[12]                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_2
P1/TDC2/FF[13]                         78.3900      0.3     18.8100
59.5800  0.0000  DFF_1
P1/TDC2/FF[1]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_13
P1/TDC2/FF[2]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_12
P1/TDC2/FF[3]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_11
P1/TDC2/FF[4]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_10
P1/TDC2/FF[5]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_9
P1/TDC2/FF[6]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_8
P1/TDC2/FF[7]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_7
P1/TDC2/FF[8]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_6
P1/TDC2/FF[9]                          78.3900      0.3     18.8100
59.5800  0.0000  DFF_5
--------------------------------  ----------  -------  ----------
---------  ------  ----------------------
   Total
   24021.9801  6936.4902  0.0000
```

IC-Compiler: Power Report

```
****************************************
Report : power
        -hier
        -analysis_effort low
Design : ADPLL_1
Version: L-2016.03-SP5-1
Date   : Wed Jul 12 21:30:07 2017
****************************************


Library(s) Used:

    tsl18fs120_scl_ff (File:
/cad/cad_FDK/scl_pdk/stdlib/fs120/liberty/lib_flow_ff/tsl18fs120_
scl_ff.db)


Operating Conditions: tsl18fs120_scl_ff   Library:
tsl18fs120_scl_ff
Wire Load Model Mode: top


Global Operating Voltage = 1.98
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


--------------------------------------------------------------------
--------------
                                        Switch   Int      Leak
Total
Hierarchy                               Power    Power    Power
Power    %
--------------------------------------------------------------------
--------------
ADPLL_1                                    3.510    8.096 4.18e+04
11.606 100.0
  P1 (PFALD)                               0.413    0.920 3.70e+04
1.333  11.5
    TDC1 (TDC_N16_0)                    2.19e-02    0.167 2.07e+03
0.189   1.6
      A2[1] (buffer1_28)                   0.000    0.000    0.000
0.000   0.0
      A2[0] (buffer1_29)                   0.000    0.000    0.000
0.000   0.0
      FFL (DFF_31)                      6.32e-04 1.05e-02  128.800
1.11e-02   0.1
      FF1 (DFF_0)                       1.26e-03 1.04e-02  128.800
1.17e-02   0.1
      A1 (buffer1_0)                       0.000    0.000    0.000
0.000   0.0
```

```
      A2[9] (buffer1_20)                    0.000    0.000    0.000
0.000   0.0
      A2[8] (buffer1_21)                    0.000    0.000    0.000
0.000   0.0
      A2[7] (buffer1_22)                    0.000    0.000    0.000
0.000   0.0
      A2[6] (buffer1_23)                    0.000    0.000    0.000
0.000   0.0
      A2[5] (buffer1_24)                    0.000    0.000    0.000
0.000   0.0
      A2[4] (buffer1_25)                    0.000    0.000    0.000
0.000   0.0
      A2[3] (buffer1_26)                    0.000    0.000    0.000
0.000   0.0
      A2[2] (buffer1_27)                    0.000    0.000    0.000
0.000   0.0
      FF[3] (DFF_27)                    7.12e-04 1.05e-02  128.800
1.12e-02   0.1
      FF[2] (DFF_28)                    7.45e-04 1.05e-02  128.800
1.12e-02   0.1
      FF[1] (DFF_29)                    7.56e-04 1.05e-02  128.800
1.12e-02   0.1
      FF[0] (DFF_30)                    8.66e-04 1.04e-02  128.800
1.13e-02   0.1
      A2[13] (buffer1_16)                   0.000    0.000    0.000
0.000   0.0
      A2[12] (buffer1_17)                   0.000    0.000    0.000
0.000   0.0
      A2[11] (buffer1_18)                   0.000    0.000    0.000
0.000   0.0
      A2[10] (buffer1_19)                   0.000    0.000    0.000
0.000   0.0
      FF[11] (DFF_19)                   7.50e-04 1.05e-02  128.800
1.12e-02   0.1
      FF[10] (DFF_20)                   9.53e-04 1.04e-02  128.800
1.14e-02   0.1
      FF[9] (DFF_21)                    8.26e-04 1.05e-02  128.800
1.13e-02   0.1
      FF[8] (DFF_22)                    7.68e-04 1.05e-02  128.800
1.12e-02   0.1
      FF[7] (DFF_23)                    7.75e-04 1.04e-02  128.800
1.12e-02   0.1
      FF[6] (DFF_24)                    6.29e-04 1.05e-02  128.800
1.11e-02   0.1
      FF[5] (DFF_25)                    8.05e-04 1.04e-02  128.800
1.12e-02   0.1
      FF[4] (DFF_26)                    6.63e-04 1.05e-02  128.800
1.11e-02   0.1
      FF[13] (DFF_17)                   8.09e-04 1.04e-02  128.800
1.13e-02   0.1
      FF[12] (DFF_18)                   7.32e-04 1.05e-02  128.800
1.12e-02   0.1
    TDC2 (TDC_N16_1)                    2.65e-02    0.173 2.07e+03
0.199   1.7
      FFL (DFF_15)                      5.54e-04 1.08e-02  128.800
1.14e-02   0.1
      FF1 (DFF_16)                      8.41e-04 1.08e-02  128.800
1.16e-02   0.1
```

```
      FF[3] (DFF_11)                    5.81e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[2] (DFF_12)                    8.06e-04 1.08e-02  128.800
1.16e-02   0.1
      FF[1] (DFF_13)                    6.82e-04 1.08e-02  128.800
1.15e-02   0.1
      FF[0] (DFF_14)                    7.70e-04 1.08e-02  128.800
1.16e-02   0.1
      FF[11] (DFF_3)                    5.96e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[10] (DFF_4)                    5.80e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[9] (DFF_5)                     8.63e-04 1.08e-02  128.800
1.16e-02   0.1
      FF[8] (DFF_6)                     6.99e-04 1.08e-02  128.800
1.15e-02   0.1
      FF[7] (DFF_7)                     6.18e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[6] (DFF_8)                     6.22e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[5] (DFF_9)                     7.62e-04 1.08e-02  128.800
1.16e-02   0.1
      FF[4] (DFF_10)                    5.55e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[13] (DFF_1)                    5.93e-04 1.08e-02  128.800
1.14e-02   0.1
      FF[12] (DFF_2)                    6.88e-04 1.08e-02  128.800
1.15e-02   0.1
    G1 (bitwise_nand_N16)               3.13e-02 3.62e-03  110.640
3.49e-02   0.3
    B1 (LDC_N16_M64)                       0.333    0.576 3.27e+04
0.910   7.8
      srl_37 (LDC_N16_M64_DW_rash_0)    8.74e-02    0.115 6.92e+03
0.203   1.7
      add_30 (LDC_N16_M64_DW01_add_0)   3.57e-02 5.64e-02 4.47e+03
9.21e-02   0.8
      sll_29 (LDC_N16_M64_DW01_ash_0)   8.89e-02    0.132 1.28e+04
0.220   1.9
  D1 (DCO)                                 2.997    4.744 2.01e+03
7.741  66.7
  N1 (clk_div)                             0.101    2.431 2.78e+03
2.532  21.8
    add_35 (clk_div_DW01_inc_0)         4.61e-02 7.43e-02  795.230
0.120   1.0
```