Simulation Study of Hybrid MOSFET Device Architecture

A thesis submitted in partial fulfillment of the

requirement for the award of degree of

Master of Technology
in
VLSI Design & CAD

Submitted by

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CERTIFICATE

This is to certify that the thesis report entitled, **"Simulation Study of Hybrid MOSFET Device Architecture"** is being submitted by **Pardeep Kumar** in the partial fulfillment of the degree of **Master of Technology in VLSI Design & CAD** of Thapar University, Patiala, embodies work under my supervision at **Department of Electrical Engineering, IIT Bombay, Mumbai** during the training period from January 2012 to June 2012.

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DECLARATION

I hereby declare that the thesis work which is being presented in the report entitled, **"Simulation Study of Hybrid MOSFET Device Architecture"** in the partial fulfillment of the award of the degree of M.Tech.(VLSI Design & CAD) at ECE Department of Thapar University, Patiala, is an authentic record of my own work carried out under the supervision of **Prof. V. Ramgopal Rao**, Institute Chair Professor, Department of Electrical Engineering, IIT Bombay, Mumbai and **Mr. Arun Kumar Chatterjee**, Assistant Professor, ECED Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any degree.

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It is certified that the above statement is correct to the best of my knowledge and belief.

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ABSTRACT

This work presents the simulation study of tunnel FET and hybrid MOSFET device architecture. As the device dimensions are shrinking and lower supply voltage is becoming the prime requirement for today's integrated circuits, the leakage current is increasing and it leads to standing power dissipation in MOSFET devices. For digital application low subthreshold swing and high I_{on}/I_{off} is a major requirement. MOSFET based devices have a fundamental lower limit of 60 mV/decade on subthreshold swing and the leakage current is also increases with the scaling of channel length. The Double Gate MOSFET, Fin-FET, Tri-Gate MOSFET have a better control over the leakage current but the minimum limit on subthreshold swing is still a problem.

Tunnel FET based devices have a different operating principle and have no lower limit of 60 mV/decade on subthreshold swing. Tunnel FET devices operate on the principle of tunneling for creating the conducting channel. In tunnel FET both the source and drain junctions are reversed biased, so the leakage current is less. The supply voltage requirement for tunnel FET is also low and it leads to lower power dissipation. The low subthreshold swing is an attracting feature for the switching kind of applications.

Although the tunnel FETs have low leakage current and lower subthreshold swing, but it also have the lower value of I_{on} current and is not a symmetric device like MOSFET. Tunnel FET have ambipolar behaviour and have fabrication issues for complex device architectures. Today's high performance devices need high I_{on}/I_{off} ratio and lower subthreshold swing value. Tunnel FETs are suitable only for low performance applications and for high performance applications there is strong requirement of new device architectures.

In hybrid MOSFET device architecture the tunnel FET and MOSFET are combined on the same device, so that both the high I_{on}/I_{off} ratio and lower value of subthreshold swing can be obtained. From simulation results of hybrid MOSFET device architecture, the I_{on}/I_{off} ratio of 4.19×10^7, and average subthreshold swing value of 48.9 mV/decade have been achieved.

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ABBREVIATIONS

Symbol	Quantity	Units
SS	Subthreshold Swing	mV/decade
I_{on}	Maximum ON State Current	A μm^{-1}
I_{off}	Minimum OFF State Current	A μm^{-1}
C_{gs}	Gate-source capacitance	fF μm^{-1}
C_{gd}	Gate-drain capacitance	fF μm^{-1}
g_m	Trans-conductance	AV^{-1} μm^{-1}
g_{ds}	Drain-source conductance	AV^{-1} μm^{-1}
I_d	Drain current	A μm^{-1}
f_T	Unity gain frequency	Hz

CHAPTER 1

INTRODUCTION AND MOTIVATION

1.1 Introduction

The CMOS (Complementary Metal Oxide Semiconductor) scaling in conventional bulk MOSFET (Metal Oxide Semiconductor Field Effect Transistor) structure usually requires complex doping profiles and channel engineering to control the leakage current and the short-channel effects (SCEs). With the downscaling of channel length, the static power consumption, and subthreshold slope degradation starts increasing in conventional bulk MOSFET. The leakage current and the short-channel effects are suppressed structurally in multi-gate devices, without the need of complex doping profiles and channel engineering. The multi-gate devices will extend the scaling limit of conventional bulk MOSFETs to 10 nm gate length and beyond [1]. But there is a fundamental lower limit of 60 mV/decade on subthreshold swing (SS) on multi-gate devices due to the thermionic dependency of MOSFET operation.

In digital applications, the MOSFET operation acts like a switch. The steep off-on transition (i.e. lower subthreshold swing value) and high I_{on}/I_{off} ratio are the prime requirement for a device to act like a switch. The steep off-on transition helps in improving the standby power dissipation and the high I_{on}/I_{off} ratio determines the performance level of the device. The multi-gate devices can provide high I_{on}/I_{off} ratio, but they cannot have the subthreshold swing below 60 mV/decade. It results in lower limit of threshold voltage and also limits the supply voltage scaling. The subthreshold swing problem can be resolved by using the tunnel FET (TFET) devices. Tunnel FET operates on different principle than MOSFET and its subthreshold swing value is not limited by 60 mV/decade. Tunnel FET can operates at lower supply voltage values, but the lower I_{on} current value as compared to MOSFET and the fabrication complexity are the major issues related to tunnel FET. The qualitative comparison of different kinds of bulk FET switch characteristics is shown in figure 1.1.

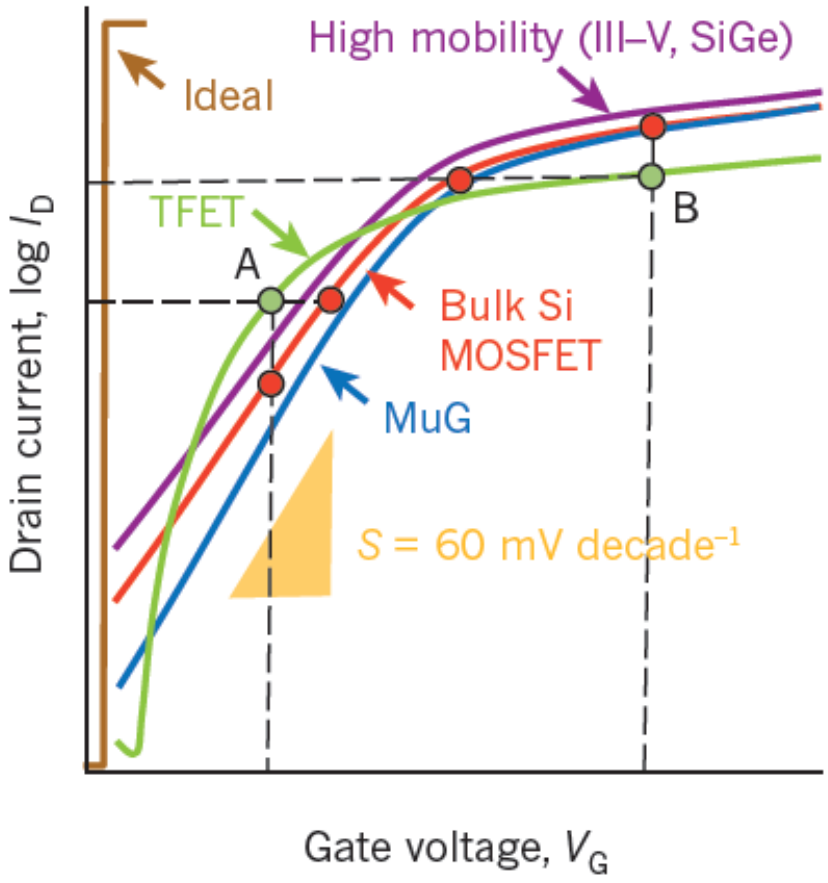


Figure 1.1 : Qualitative comparison of different bulk FET switches [2].

The qualitative comparison shows that multigate device (MuG) have better control over the off-state current (I_{off}) as compared to bulk silicon MOSFET. Tunnel FET have near ideal characteristics (i.e. steep off–on transition) for lower gate voltage values. The bulk MOSFET with SiGe have higher value of on-state current (I_{on}) but it also have larger I_{off} current value. The conventional bulk silicon MOSFET have better I_{on} current performance but the I_{off} current performance is poor.

1.2 Motivation

Tunnle FET and multi-gate MOSFET device architectures are seems to be future of digital integrated circuits. Figure 1.2 shows the qualitative comparison between switching energy and performance for a MOSFET and a TFET:

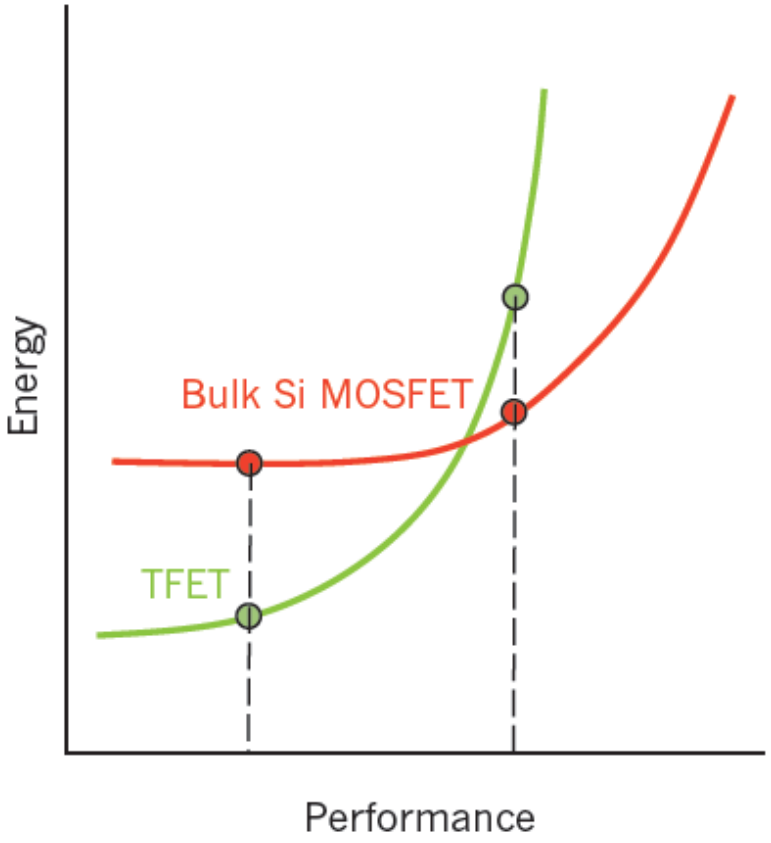


Figure 1.2 : Qualitative comparison between switching energy and performance for a MOSFET and a TFET [2].

The steep-swing TFET offers better energy efficiency at lower or moderate performance level and for higher performance, the MOSFET switch dominates over TFET switch. The use of both tunnel FET and MOSFET devices together in a digital integrated circuits doesn't seems a good solution due to the fabrication complexity and design issues.

The main source of motivation was to design a hybrid MOSFET device architecture that combines both the tunnel FET and MOSFET action on the same device so that, the new hybrid device can perform better than individual tunnel FET and MOSFET devices.

CHAPTER 2

LITERATURE SURVEY

This chapter undertakes a thorough review of previous literature with an aim to examine the challenges in CMOS technology for low power applications and possible solutions to overcome these challenges.

2.1 Challenges in CMOS Technology

Beyond 45 nm technology node the CMOS device scaling imposed different technology challenges. The increase in standby power dissipation is the most important challenges beyond 45 nm node [3]. Figure 2.1 elaborates the importance of static power consumption in the recent years.

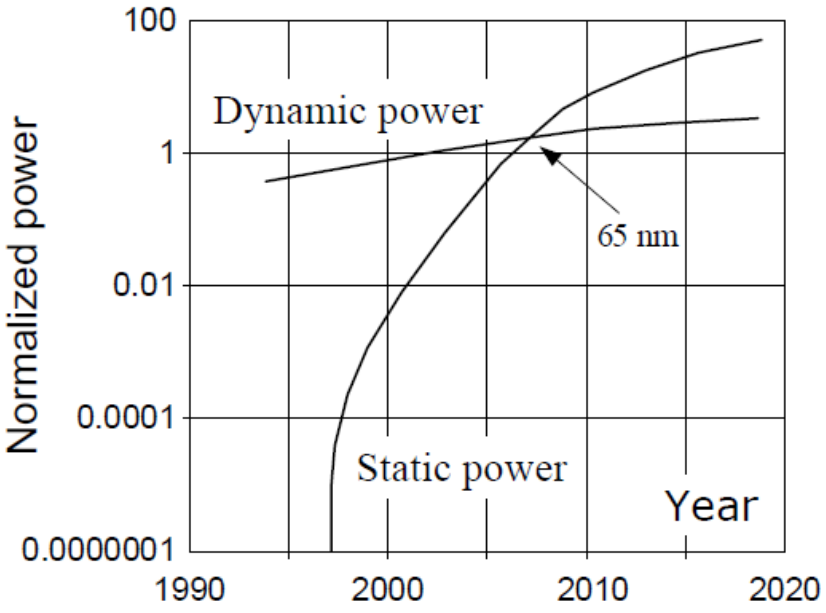


Figure 2.1 : Static power and dynamic power performance [4].

Static power consumption can be expressed as:

$P_{static} = I_{leak} V_{DD}$ (2.1)

where I_{leak} is the sum of the leakage currents in the device when the MOSFET is in the off state.

2.1.1 Subthreshold Swing

The subthreshold swing (SS), is defined as the change in gate bias required to change the subthreshold drain current by one decade. It is given by [5]:

$$SS = \left(\frac{\partial V_g}{\partial \log I_D} \right) \tag{2.2}$$

$$SS \cong \left(1 + \frac{C_d}{C_{ox}}\right) \ln 10 \, \frac{kT}{q} \cong 60 \text{ mV decade}^{-1} \text{ at } T = 300 \text{ K} \tag{2.3}$$

where kT/q is the thermal voltage, and C_d and C_{ox} are the depletion and the oxide capacitances, respectively. The thermionic dependency of injection of electrons in MOSFET sets a fundamental lower limit to the subthreshold swing and it is not scalable but has a minimum value of 60 mV per decade at room temperature [2]. The figure 2.3 shows the variation of subthreshold swing with the technology nodes :

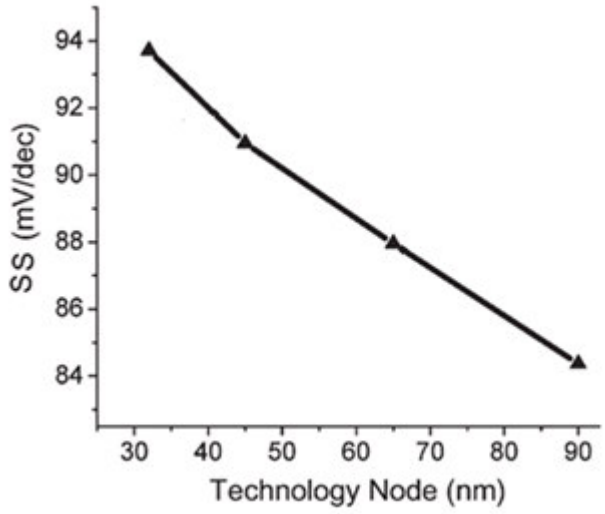


Figure 2.2 : Subthreshold swing vs technology node for nMOSFET [6].

2.1.2 I_{on}/I_{off} Ratio

For an n-channel MOSFET, I_{on} is maximum drain current at $V_G = V_D = V_{DD}$ and I_{off} is minimum drain current at $V_G = 0$ V and $V_D = V_{DD}$, where V_G, V_D, and V_{DD} are the gate voltage, drain voltage, and supply voltage respectively. I_{off} increases with the reduction in threshold voltage, V_{TH} and is given by [7]:

$$I_{off} = I_{DS}\left(10^{-\frac{V_{TH}}{SS}}\right) \tag{2.4}$$

where SS is the subthreshold swing.

I_{on} increase with the reduction in threshold voltage, V_{TH} as :

$$I_{on} \propto (V_{GS} - V_{TH}) \tag{2.5}$$

With technology node the threshold voltage is keep decreasing and it results in increase in the I_{off} current value. The effect of technology node on I_{on}/I_{off} ratio is shown in figure 2.3 and table 2.1:

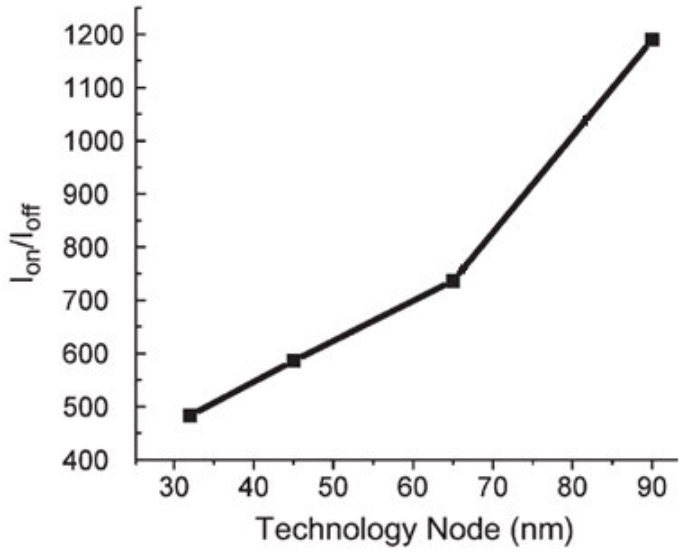


Figure 2.3 : I_{on}/I_{off} vs technology node for nMOSFET [6].

Table. 2.1 : Device features of CMOS technologies under nominal supply voltage [8]

Node (nm)	L_{eff} (nm)	T_{ox} (nm)	$V_{dd,nom}$ (V)	$V_{t,sat}$ (V)	$I_{off,nom}$ (nA/µm)	$I_{on,nom}$ (µA/µm)
250	120	4.0	2.5	0.63	0.002	820
180	70	2.3	1.8	0.49	0.11	840
130	49	1.6	1.3	0.36	4.5	890
90	35	1.4	1.2	0.32	19	1030
65	24.5	1.2	1.1	0.30	62	1150
45	17.5	1.1	1.0	0.27	200	1250
32	12.6	1.0	0.9	0.27	350	1290

2.2 Possible Solutions to CMOS Technology Challenges

Different device architectures like double gate MOSFET, tri Gate MOSFET, gate-all-around MOSFET, fin-shaped FET, impact-ionization MOSFET, MEMS/NEMS switches, tunnel FET, etc. have been demonstrated to minimize the short channel effect and to lower the source-drain leakage current.

2.2.1 Multi-Gate FET Devices

In May 2011, Intel announced its decision to use tri-gate FET devices for its 22-nm technology. This indicates that planar MOSFET scaling is reaching its limits. In multi-gate devices, the control of the channel by the gate is stronger than in planar single-gate MOSFETs. Due to better control of the channel, the short channel effects can be significantly reduced [9].

2.2.2 Impact-Ionization MOSFET

Impact-Ionization MOSFET (I-MOS) is a new kind of transistor that uses modulation of the breakdown voltage of a gated p-i-n structure in order to switch from the OFF to the ON state. The subthreshold slope is much lower than kT/q in I-MOS because the impact-ionization is an abrupt function of the electric field (or the carrier energy). The switching speed of I-MOS is comparable with CMOS and its basic concept is experimentally verified [10].

2.2.3 MEMS/NEMS Switches

MEMS/NEMS (Microelectromechanical Sensor/Nanoelectromechanical Sensor) switches are

controlled by electrostatic forces to mechanically deflect an active element into physical contact with an opposing electrode, thus changing the state of the device. MEMS/NEMS switches are also relatively insensitive to radiation, temperature and external electric fields, which makes it well suited for the harsh environments encountered in aerospace and military applications [11].

2.2.4 Tunnel FET

The tunnel FET is basically a gated p-i-n diode which works on the principle of band-to-band tunneling. Because of lower subthreshold-swing, tunnel field-effect transistors are potential successors of conventional bulk MOSFETs. Tunnel FET can operate on significantly reduced supply voltage and it seems a promising candidates for low-power operation [7].

CHAPTER 3

Theory of Tunnel FET

This Chapter explains the principle of operation of tunnel FET. It also includes the different types of architectures for tunnel FET and the advantages and disadvantages of tunnel FET devices.

3.1 Simple Tunnel FET Structure and Principle of Operation

A tunnel FET is basically a p-i-n diode geometry with a control gate terminal separated by an oxide layer, as shown in figure 3.1:

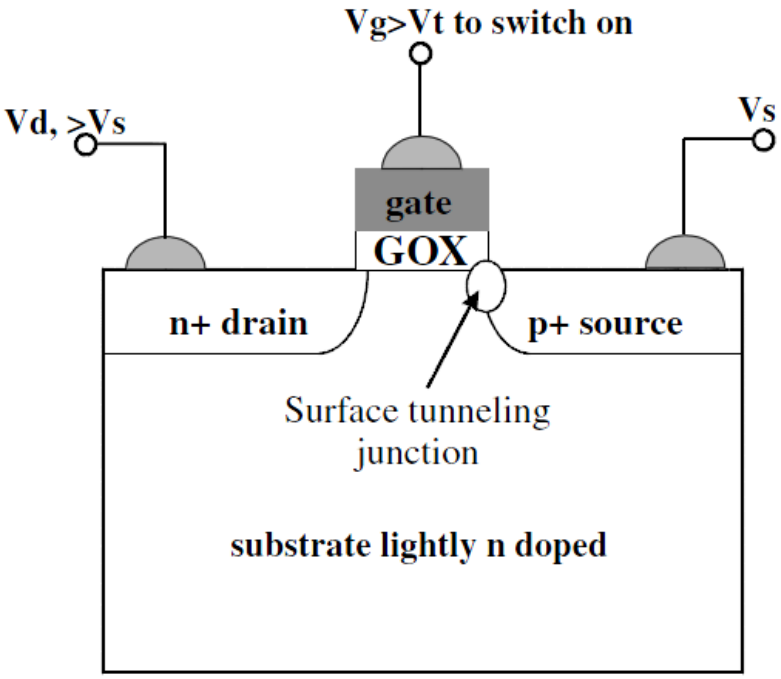


Figure 3.1: Planar n-channel TFET structure [12].

The potential to the gate terminal controls the flow of current. The tunneling side acts as source. The source and drain are separated by lightly doped channel region.

Depending upon the potential at gate terminal the operation of n-channel TFET can be divided into three parts.

i) $V_G = 0$ V

This is also called the off-state and there is no band bending for this state as shown in figure. 3.2 :

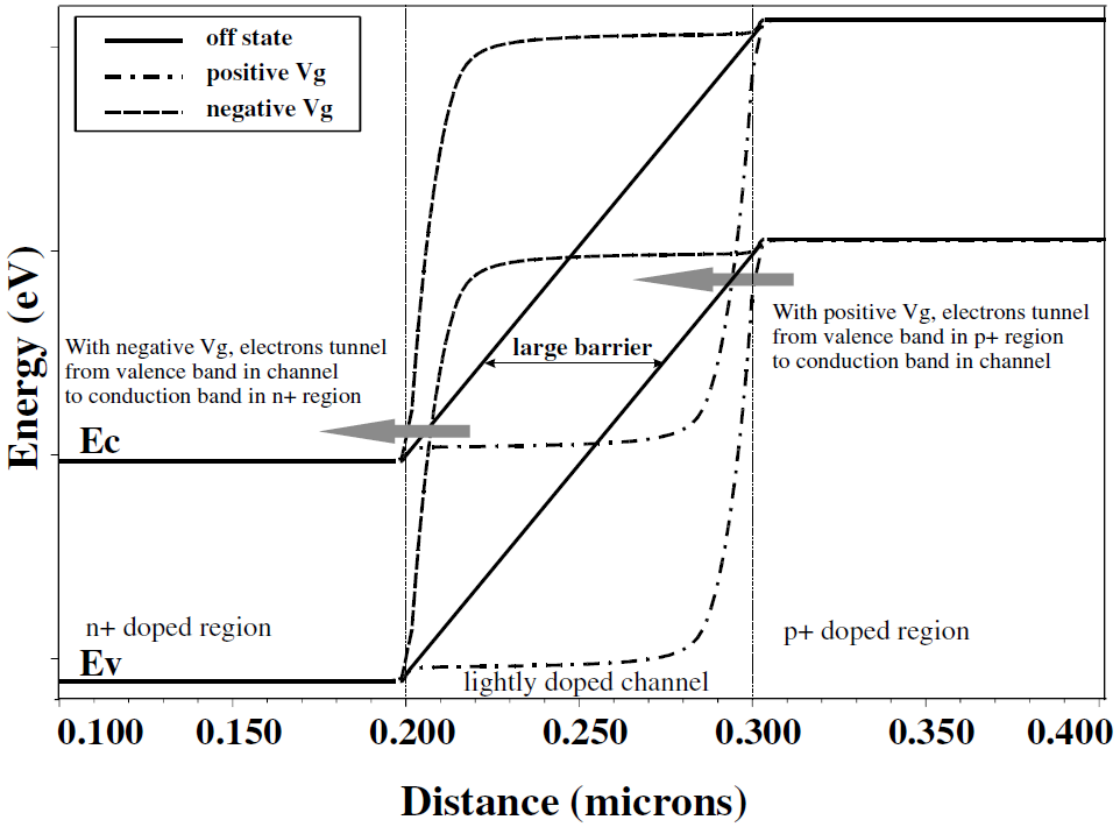


Figure 3.2: Band diagram for gate controlled band-to-band tunneling in TFET with 100 nm channel length [12].

The tunnelling barrier as well as the barrier for thermal emission of electrons from source to drain is larger and as a result there is no conduction current flow or very small leakage current flow during the off-state.

ii) $V_G > 0$ V

During this state there is band bending near the p+ region and channel region and electrons can now tunnel from valence band of p+ region to the conduction band of channel region. The band bending increases with the increase in positive gate voltage and as a result the tunnelling current will also increase with the positive gate voltage.

iii) $V_G < 0$ V

This state is also called ambipolar state. The TFET will now behave as p-channel TFET. In this state there is band bending near the n+ region and the channel region. The electrons can tunnel from the valence band of channel region to the conduction band of n+ region. The holes will now flow towards the p+ region. The transfer characteristics of TFET with n+ drain and p+ source regions is shown in figure 3.3 :

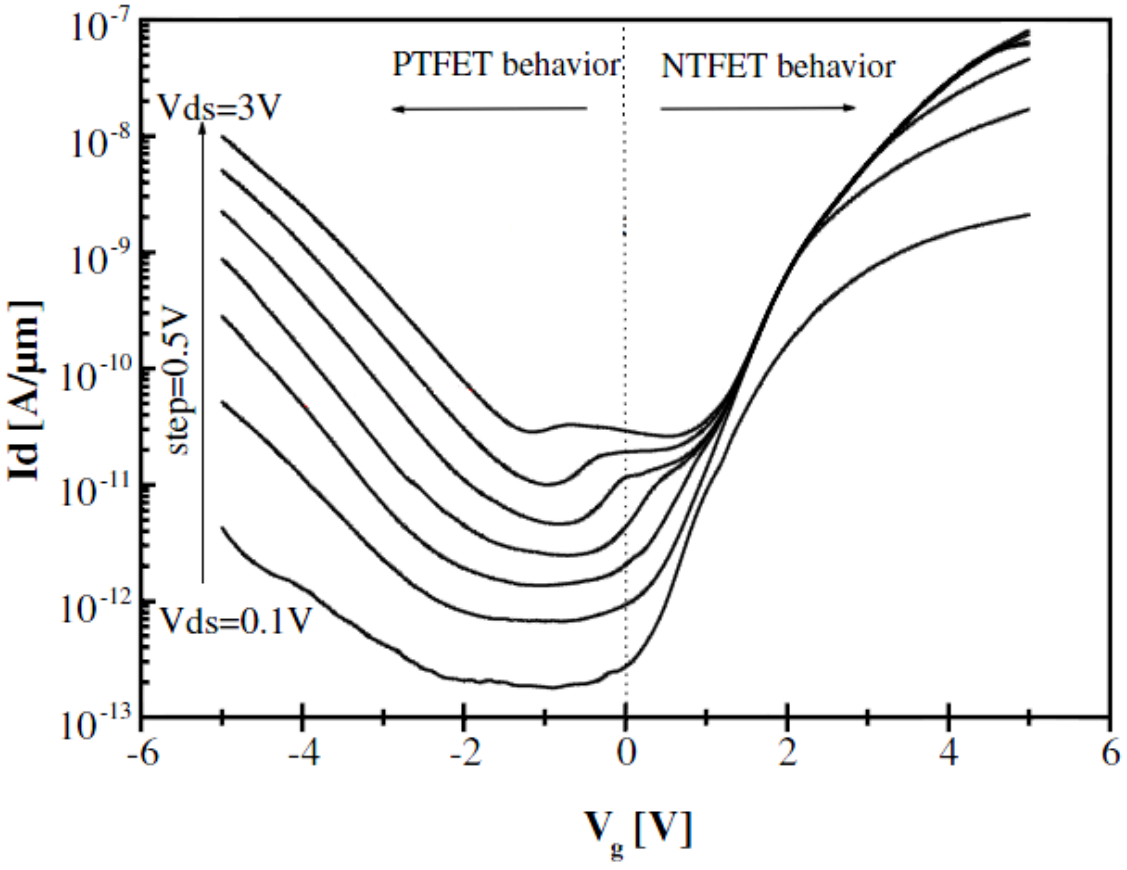


Figure 3.3: Transfer characteristics of TFET with n+ drain and p+ source regions [12].

3.2 Band to Band Tunneling

The band to band tunneling (or interband tunnelling) mechanism was first proposed by Zener in 1934. The band to band tunneling can be approximated by the triangular potential barrier and the transmission probability can be solved by Wentzel-Kramer-Brillouin approximation [2].

$$T_{WKB} \cong \exp\left(-\frac{4\lambda\sqrt{2m^{*}\,E_g{}^{3}}}{3q\hbar(E_g + \Delta\varphi)}\right) \tag{3.1}$$

where m* is the effective mass

E_g is the bandgap

$\Delta\varphi$ is E_C (source) - E_V (channel) i.e. energy range over which tunneling can occurs.

λ is screening tunneling length

and for single gate device its value can be given by [13]:

$$\lambda = \sqrt{\frac{\varepsilon_{Si} t_{Si} t_{ox}}{\varepsilon_{ox}}} \tag{3.2}$$

where ε_{Si} and ε_{ox} are the dielectric permittivity of the silicon and gate oxide, t_{Si} and t_{ox} are the thickness of silicon and gate oxide respectively.

The tunneling current depends both on the transmission probability as well as available states for tunneling. For lower bandgap materials the tunneling probability is more and the lower bandgap materials can be used at the source side to increase the tunneling current.

3.3 Threshold Voltage in Tunnel FET

The transfer characteristics of tunnel FET are non-linear and are different from conventional MOSFET. The threshold voltage in tunnel FET is a function of both gate and drain potential. So, for a tunnel FET there are two threshold voltages [14].

1.) Gate Threshold Voltage

The gate voltage for which the energy barrier narrowing starts to saturate and it reflects the gate voltage for which maximum point in transconductance derivative, dg_m/dV_G is achieved.

2.) Drain Threshold Voltage

The drain voltage for which the energy barrier narrowing starts to saturate and it reflects the drain voltage for which maximum point in dg_{ds}/dV_D is achieved.

3.4 Subthreshold Swing in Tunnel FET

In tunnel FET, the drain current depends on the tunneling-barrier width rather than the formation of an inversion layer and there are different expressions proposed to find out the subthreshold slope for Tunnel FET. Based on Hurkx's band-to-band tunneling model subthreshold slope can be given by [15]:

$$S_{TFET} = \frac{{V_{GS}}^2}{5.75(V_{GS} + \text{Const})} \quad [\text{mV dec}^{-1}] \tag{3.3}$$

where the value of Const is determined by device dimensions and material parameters.

The terms point subthreshold swing and average subthreshold swing are also used for tunnel FET. The minimum subthreshold swing value at any point in the transfer characteristics (i.e. I_d-V_g characteristics) is called the point subthreshold swing [15] and the average subthreshold swing value is measured from the threshold voltage value to the gate voltage value at which the current starts to increase. The subthreshold swing in tunnel FET is a function of gate voltage and does not restricted by the thermionic process.

3.5 Different Tunnel FET Device Architectures

Tunnel FET working depends upon band to band tunneling and this band to band tunneling is determined by the transmission probability as shown in Equation 3.1. There are different ways to increase the transmission probability and different device architectures are possible in tunnel FET. Some of these tunnel FET device architectures are : planar TFET, double gate TFET, vertical TFET, sandwich tunnel barrier FET (STBFET), TFET with raised Germanium source, halo layer TFET, compound-semiconductor TFET etc.

3.6 Advantages and Disadvantages of Tunnel FET

Table. 3.1 : Advantages and disadvantages of Tunnel FET

S. No.	Advantages	Disadvantages
1.	Lower subthreshold swing value.	Lower performance for silicon and higher band gap materials.
2.	Low leakage current or OFF state current.	Lower ON current values as compared to conventional bulk MOSFET.
3.	Less temperature dependent	Ambipolar in nature.
4.	Needs lower supply voltage, so power efficient.	Fabrication issues for complex device architecture.
5.	It supports the scaling.	Compact models are not available for circuit level simulations.

CHAPTER 4

Hybrid MOSFET Device Architectures

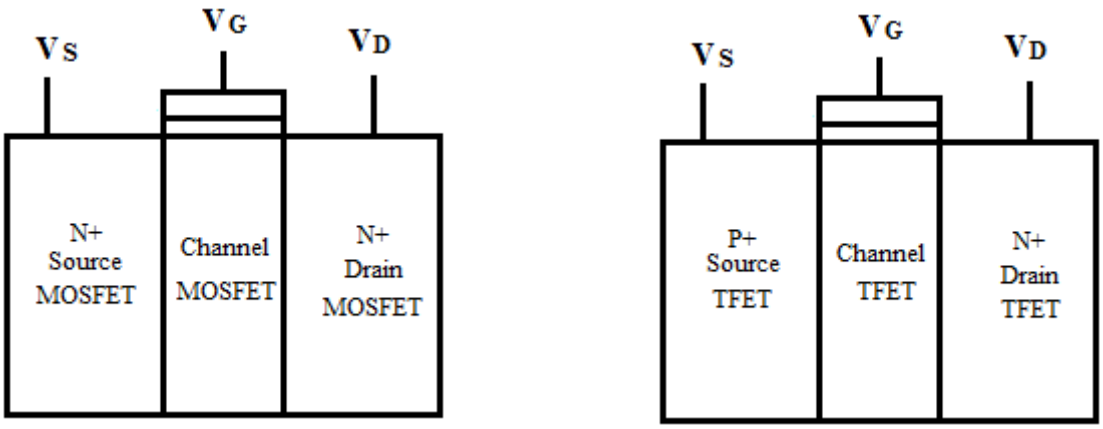
This chapter explains the need of hybrid MOSFET device architectures. It also includes the different types of planar and vertical hybrid MOSFET device architectures, and their principle of operation.

4.1 Need of Hybrid MOSFET Device Architecture

Conventional bulk MOSFET is facing different challenges like, standby power dissipation, short channel effects, higher subthreshold swing, etc. Short channel effects and standby power dissipation can be significantly reduced using multi-gate devices, but the subthreshold swing of MOSFET have a lower limit of 60 mV/decade. The I-MOS and MEMS/NMES switches have steep off-on characteristics but they operates at higher voltage values and have issues with integration with present CMOS technology. Tunnel FET seems to be the potential successors of conventional bulk MOSFETs for low power application due to their lower subthreshold swing value. Tunnel FET have lower I_{on} current value and cannot be used in high performance application. This leads to think of new device architectures that can combine both the key parameters of MOSFET and tunnel FET into a single hybrid device architecture.

4.2 Planar Hybrid MOSFET Device Architecture

Figure 4.1 shows the conventional bulk n-channel MOSFET and planar n-channel TFET device structure. The drain region of both bulk n-channel MOSFET and planar n-channel TFET is of N+ type and can be combined to form a planar hybrid n-channel MOSFET device architecture as shown in figure 4.2. For n-channel hybrid MOSFET device the source region is P+ type for tunnel FET and N+ type for MOSFET. The channel region for tunnel FET is lightly doped N type and channel region for MOSFET is P type.



(a) (b)

Figure 4.1: (a) Conventional bulk n-channel MOSFET structure, and (b) Planar n-channel TFET structure.

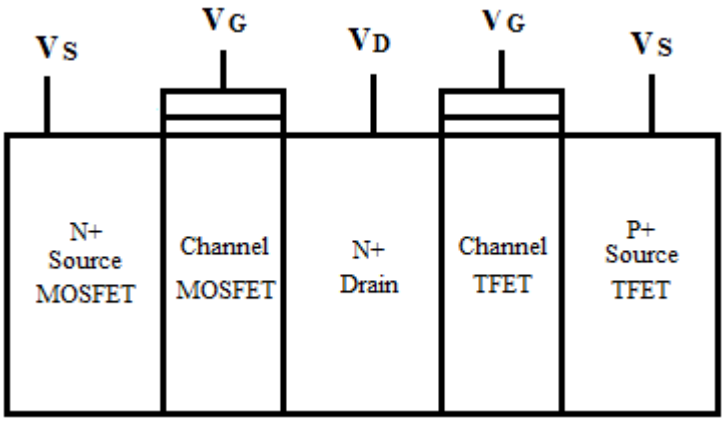


Figure 4.2: Planar hybrid n-channel device architecture.

The hybrid device have two gate terminals and they can be combined together. Since, tunnel FET can operate at lower supply voltage, so, for gate voltage values lower than MOSFET threshold voltage value, the tunnel FET action will dominate over the MOSFET action and will provide the lower subthreshold swing value. For gate voltage greater than threshold voltage value of MOFET, the MOSFET action will dominate over the tunnel FET and it will provide the larger I_{on} current values. The planar hybrid MOSFET device architecture combines the features of both tunnel FET and MOSFET and is CMOS compatible for fabrication process.

4.3 Vertical Hybrid MOSFET Device Architecture

The increase in layout area and short channel effects are the major problems with planar hybrid MOSFET device architecture. TFET and MOSFET can also be combined vertically with a bottom gate as shown in figure 4.3 :

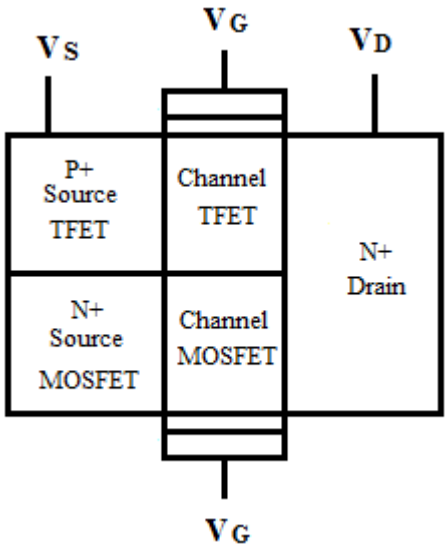


Figure 4.3: Vertical hybrid n-channel MOSFET device architecture.

Vertical hybrid n-channel MOSFET device architecture will reduce the layout area and will also reduce the short channel effects because of gate control from two sides. The operating principle of vertical hybrid n-channel is similar as that of planar hybrid n-channel MOSFET device architecture. The source terminal is kept at ground potential and drain terminal is kept at positive supply voltage vlaue. When positive potential at gate terminals starts increasing, the tunnel FET and MOSFET will operate in parallel and will result in higher I_{on} current value and steep off-on characteristics. The body thickness will decide the gate control over the channel region and will control the leakage current.

The leakage current problem with vertical hybrid MOSFET device architecture can be minmized by separating the source region of MOSFET and TFET by a low doped layer or by an oxide layer as shown in figure 4.4 :

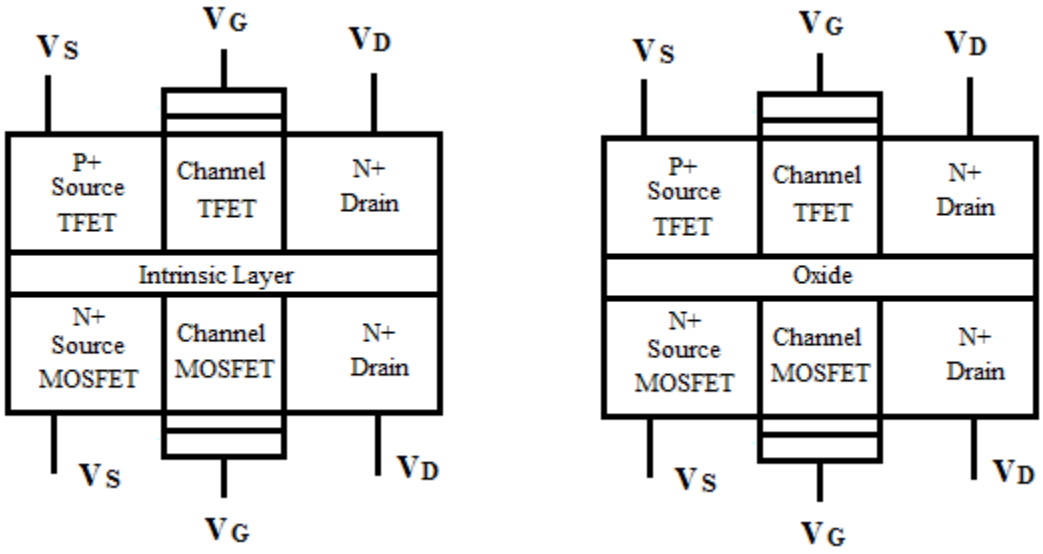


Figure 4.4: Vertical hybrid n-channel MOSFET device architecture (a) with intrinsic layer, (b) with oxide layer.

CHAPTER

5 Simulation Setup and Results

5.1 Simulation Setup

The Synopsis TCAD tool (SENTAURES) is used to carry out the 2-D device simulations for all the device architectures. Gaussian doping profile, with a peak concentration of 1×10^{20} atoms/cm^3 for source region and peak concentration of 1×10^{19} atoms/cm^3 for drain region of both tunnel FET and MOSFET with a lateral doping profile of 1 nm/dec, is assumed for all the device architectures. The channel doping is made moderately doped with 1×10^{16} atoms/cm^3. The source and drain contacts are assumed ohmic contacts and gate contact for n-channel device is made of a metal with the work function of 4.69 eV for MOSFET and the work function of 4.12 eV for tunnel FET in order to match the I_{off} current value with hybrid MOSFET device architecture. The equivalent oxide thickness (EOT) of 0.4 nm is used for all the device architectures. For tunnel FET devices, the nonlocal band to band tunneling (BTBT) model is used.

5.2 Different Device Structures

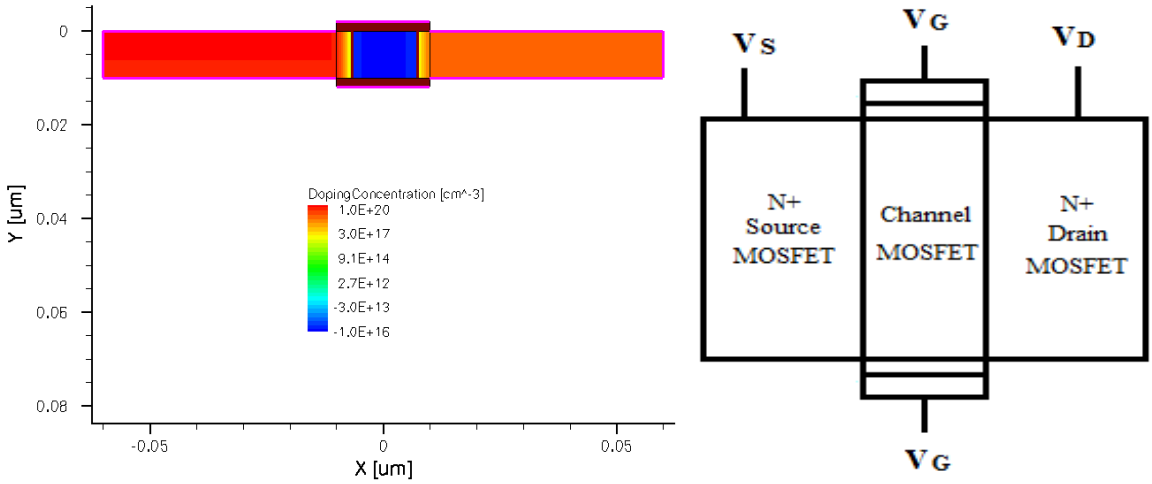


Figure 5.1 : Double gate MOSFET structure with simulator view and labeled view.

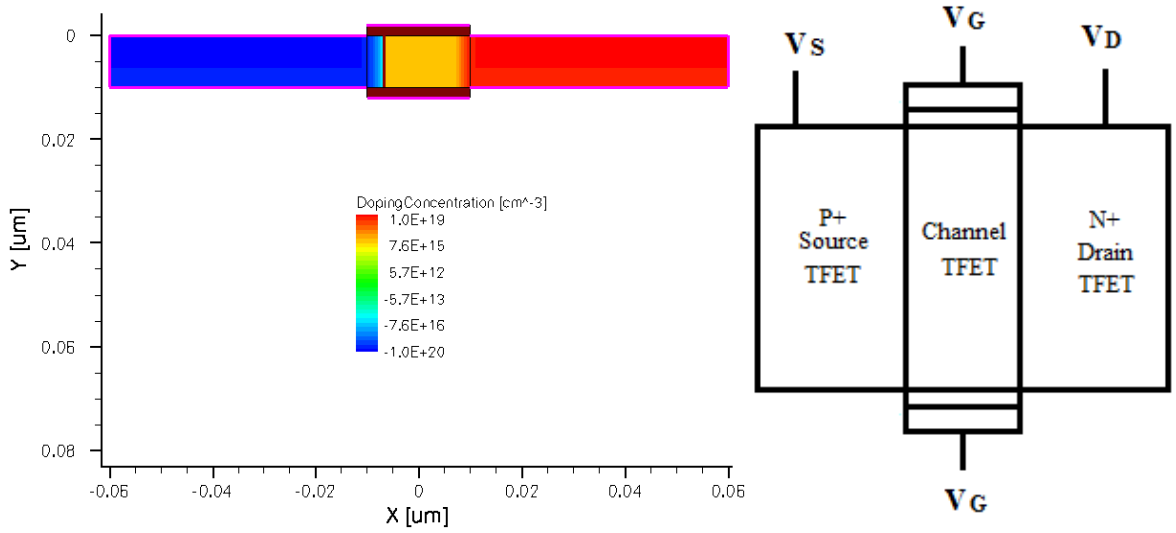


Figure 5.2 : Double gate tunnel FET structure with simulator view and labeled view.

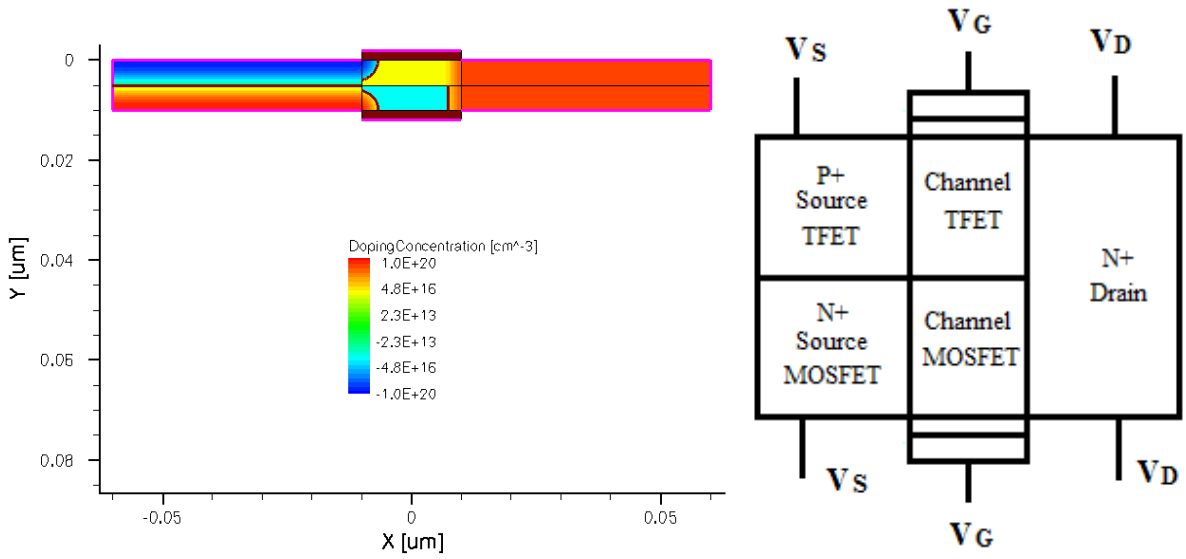


Figure 5.3 : Simple hybrid MOSFET (MOS_TFET) structure with simulator view and labeled view.

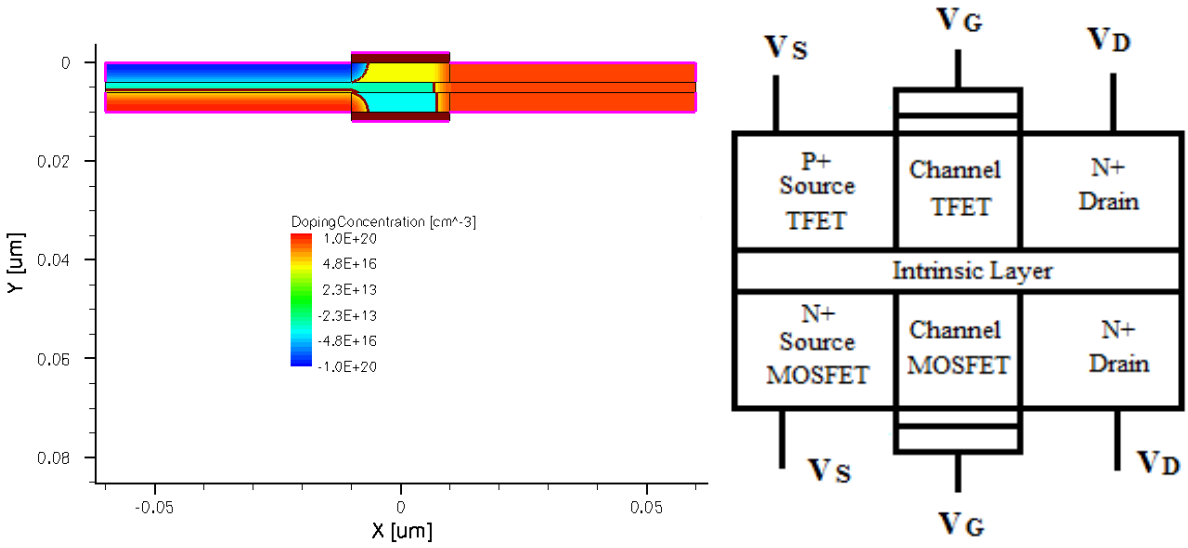


Figure 5.4 : Hybrid MOSFET with intrinsic layer (MOS_TFET with intrinsic layer) structure with simulator view and labeled view.

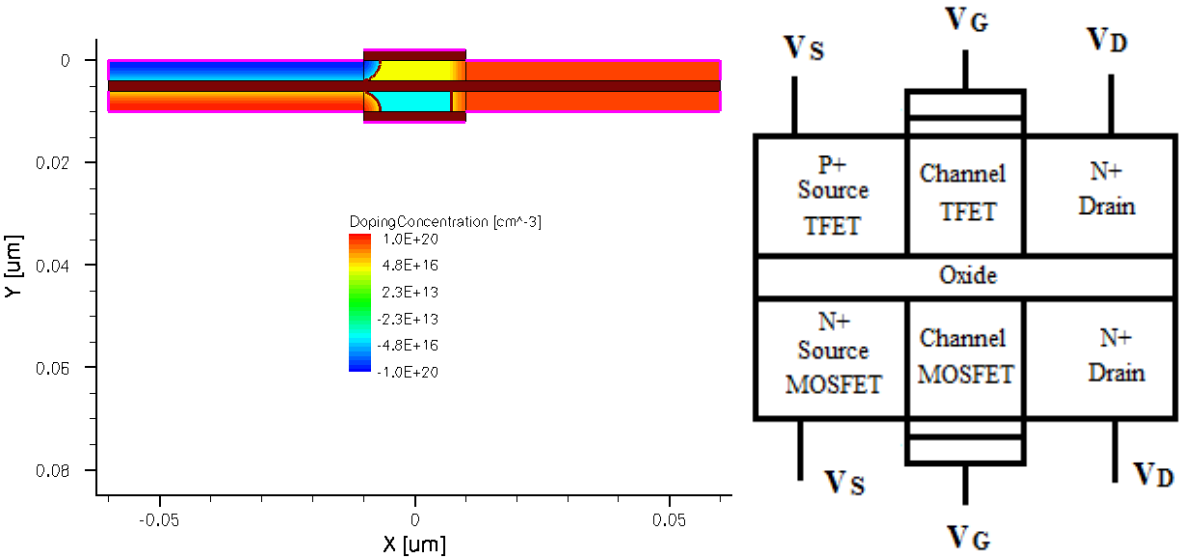
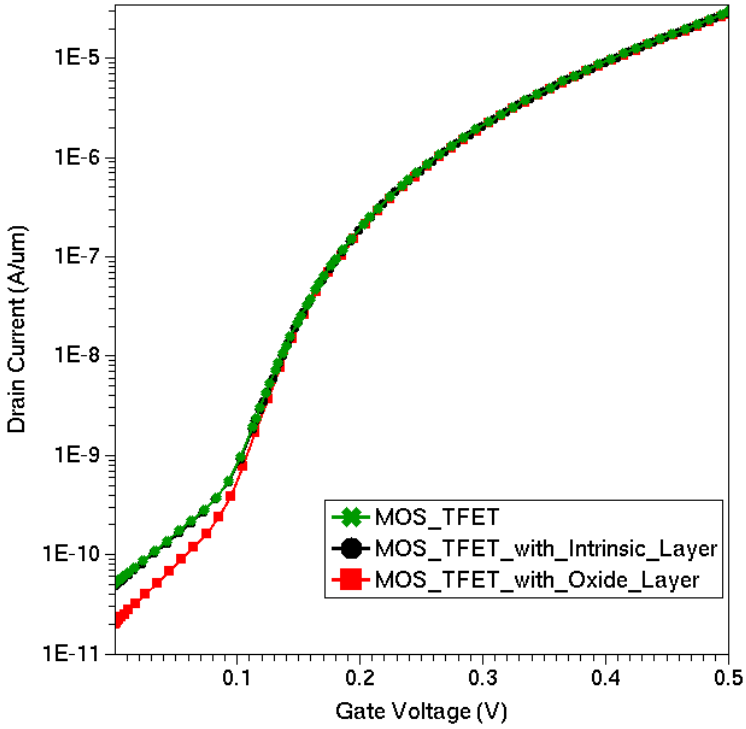
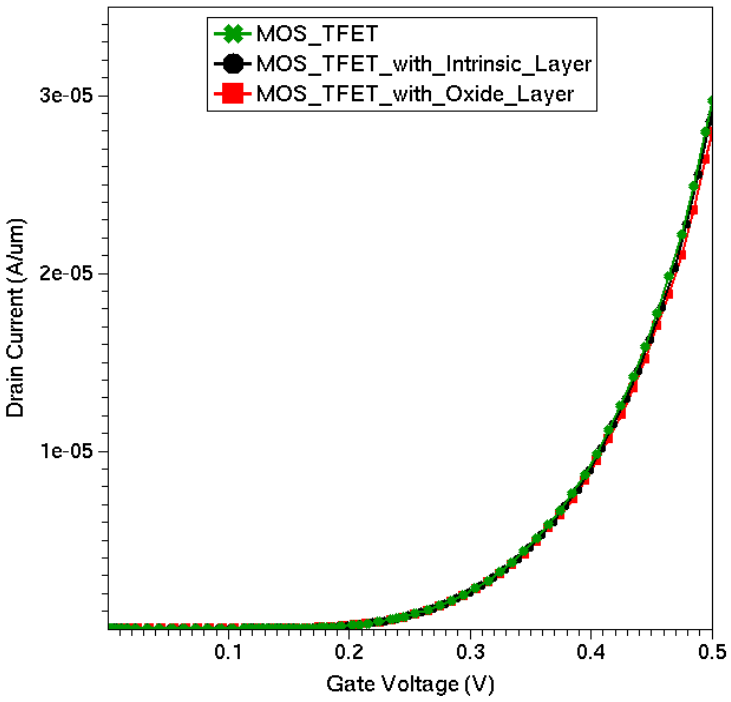


Figure 5.5 : Hybrid MOSFET with oxide layer (MOS_TFET with oxide layer) structure with simulator view and labeled view.

5.3 I_d vs V_g Characteristics

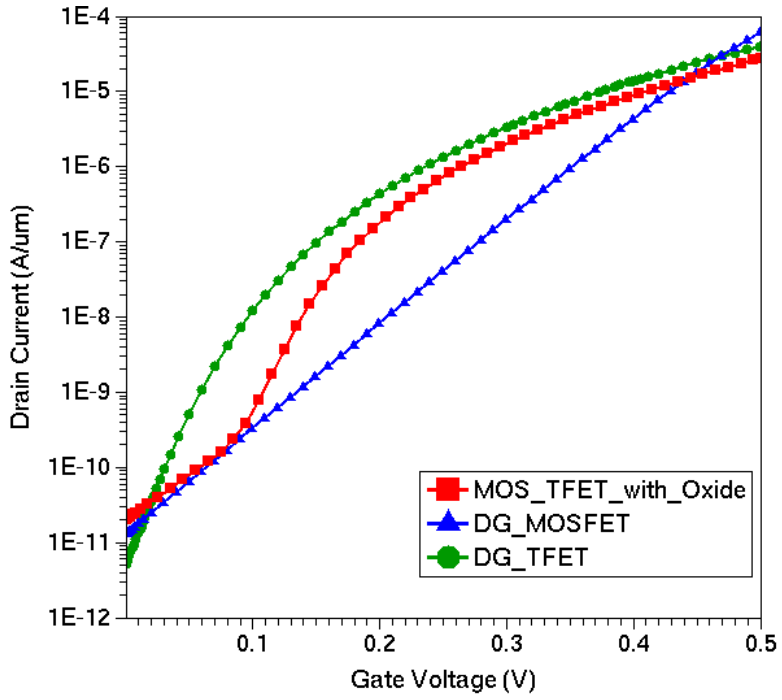


(a)

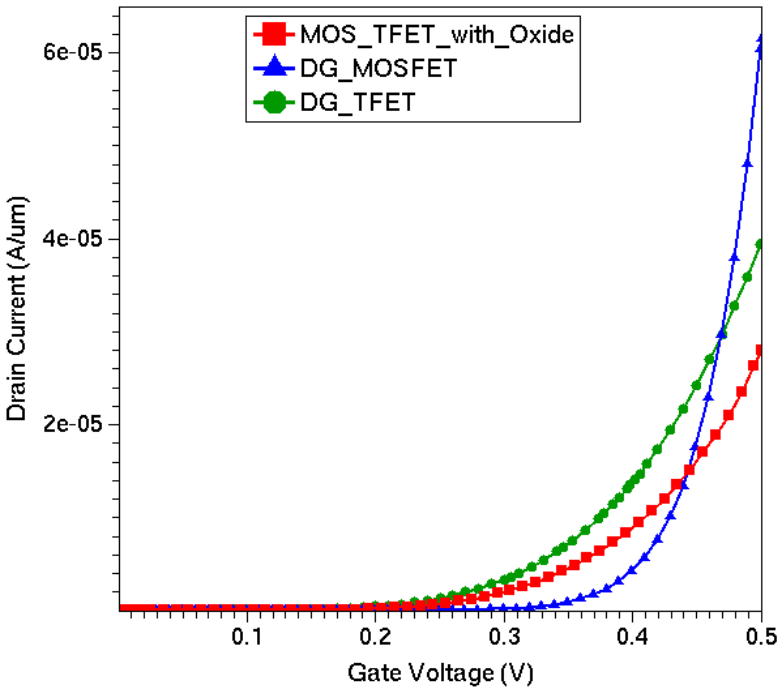


(b)

Figure 5.6 : I_d vs V_g characteristics of three hybrid MOSFET device architectures with drain voltage of 0.5 V and drain current on (a) log scale, and (b) linear scale.

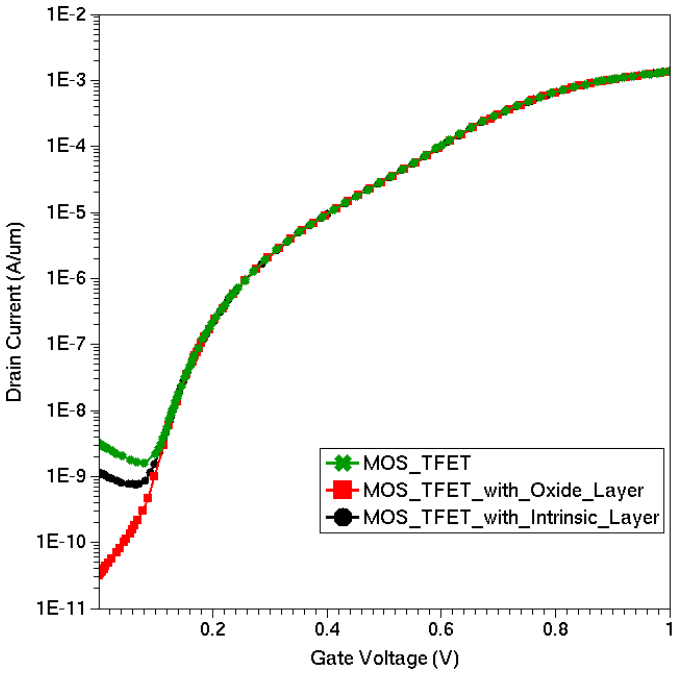


(a)

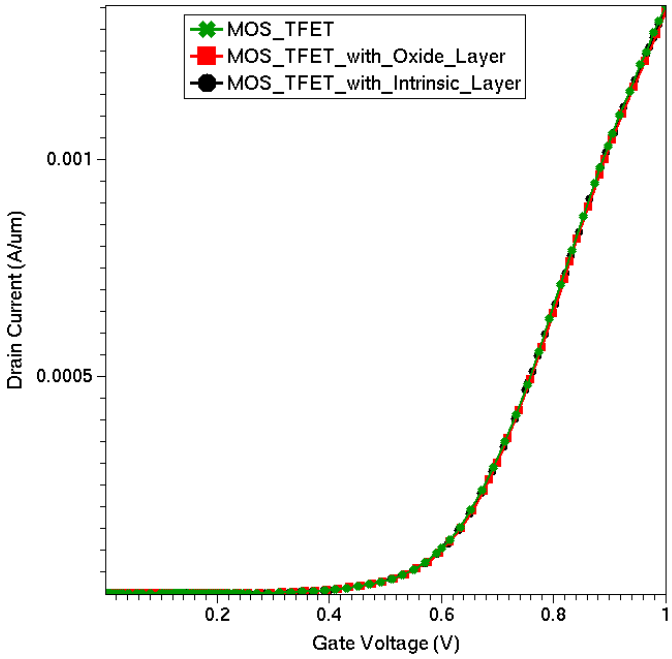


(b)

Figure 5.7 : I_d vs V_g characteristics of double gate MOSFET (DG_MOSFET), double gate tunnel FET (DG_TFET) and hybrid MOSFET (MOS_TFET_with_Oxide) with drain voltage of 0.5 V and drain current on (a) log scale, and (b) linear scale.

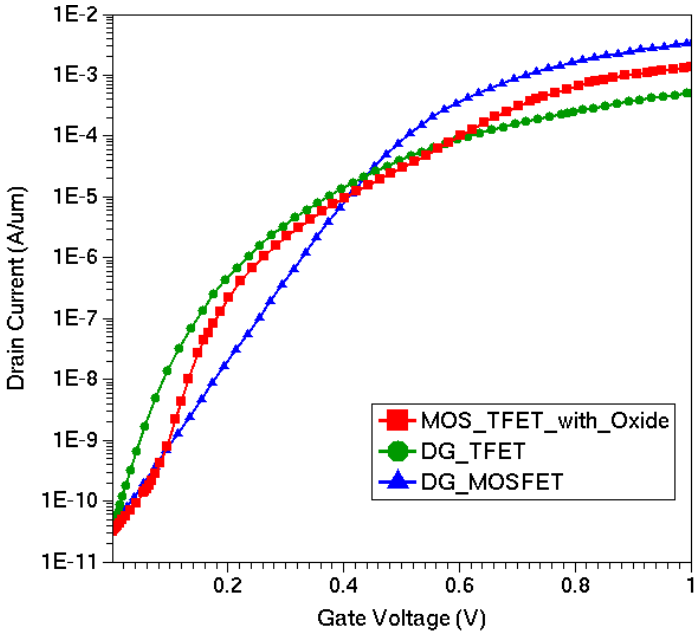


(a)

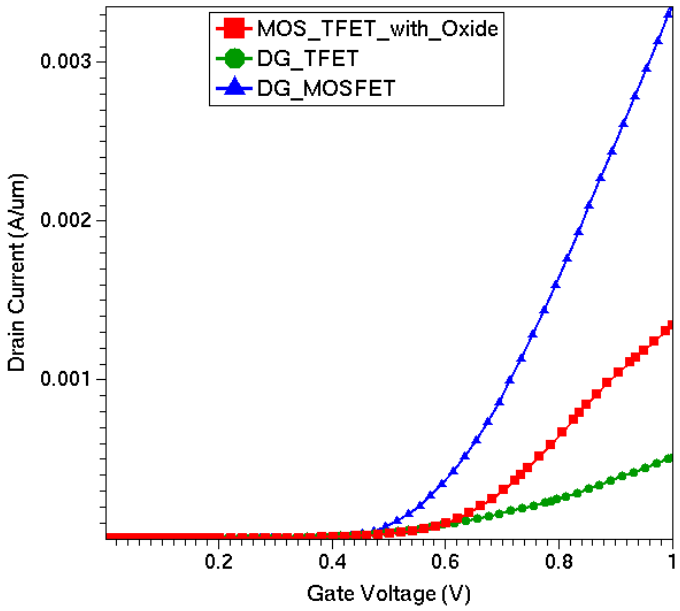


(b)

Figure 5.8 : I_d vs V_g characteristics of three hybrid MOSFET device architectures with drain voltage of 1.0 V and drain current on (a) log scale, and (b) linear scale.



(a)



(b)

Figure 5.9 : Id vs Vg characteristics of double gate MOSFET (DG_MOSFET), double gate tunnel FET (DG_TFET) and hybrid MOSFET (MOS_TFET_with_Oxide) with drain voltage of 1.0 V and drain current on (a) log scale, and (b) linear scale.

5.4 I_d vs V_d Characteristics

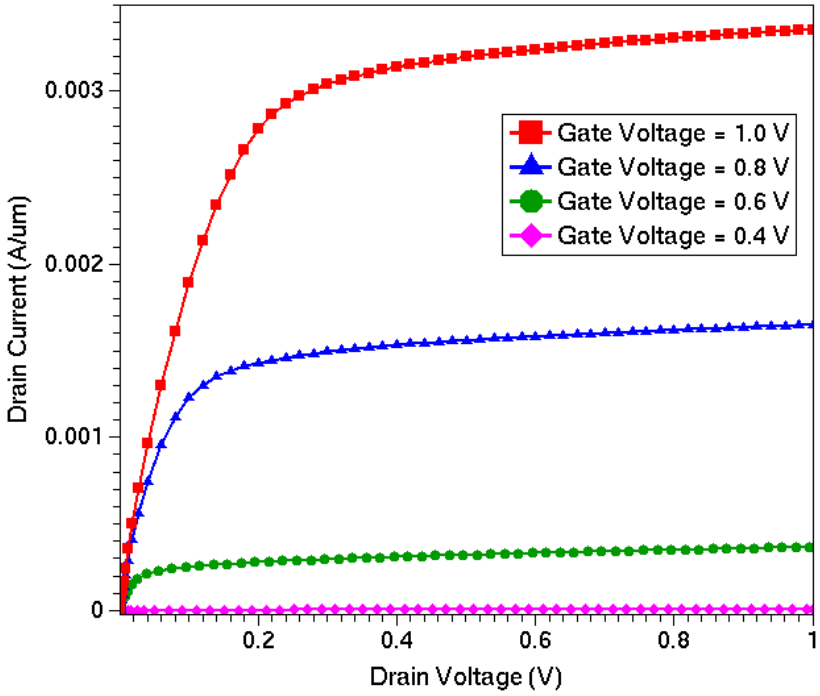


Figure 5.10 : I_d vs V_d characteristics of double gate MOSFET (DG_MOSFET).

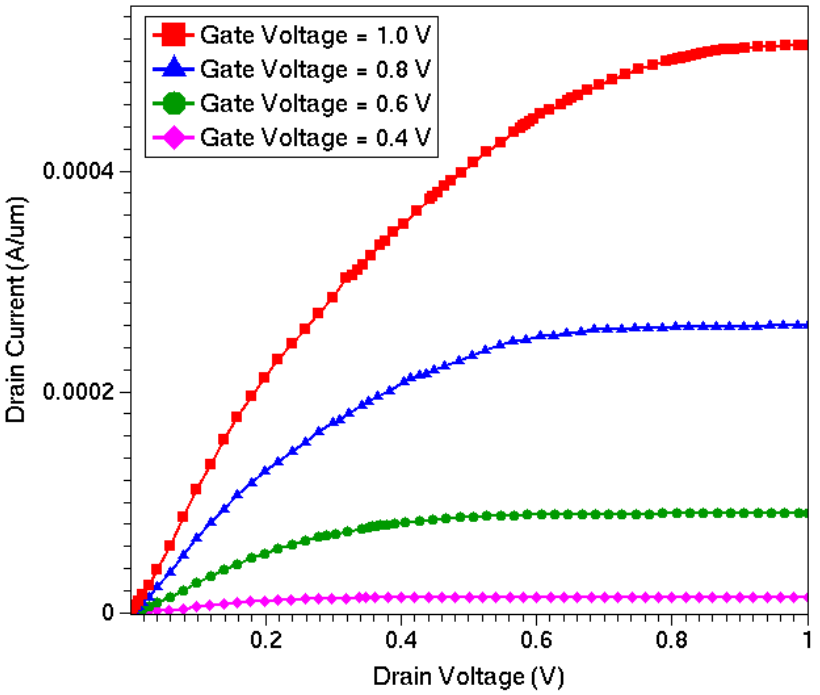


Figure 5.11 : I_d vs V_d characteristics of double gate TFET (DG_TFET).

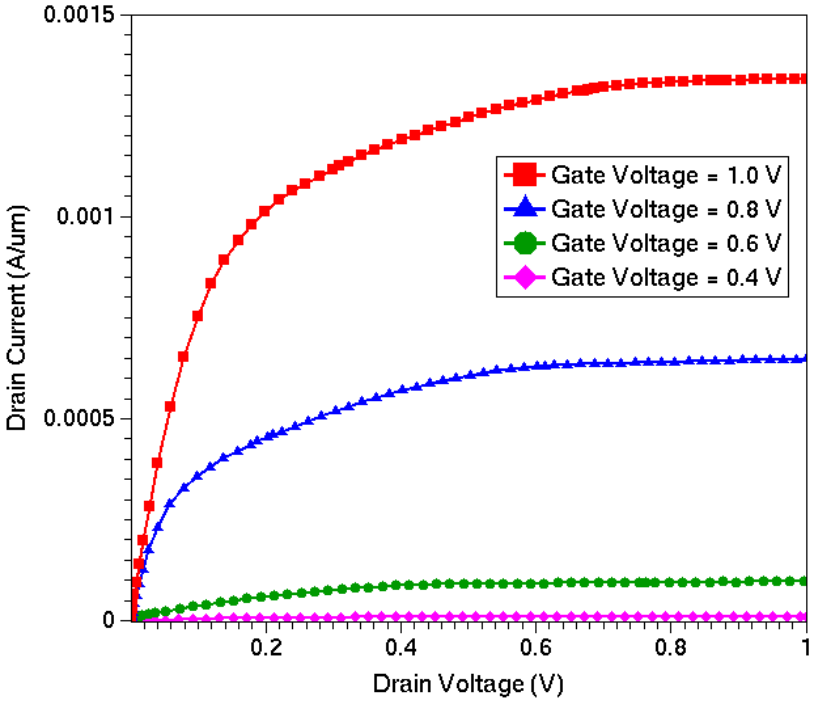
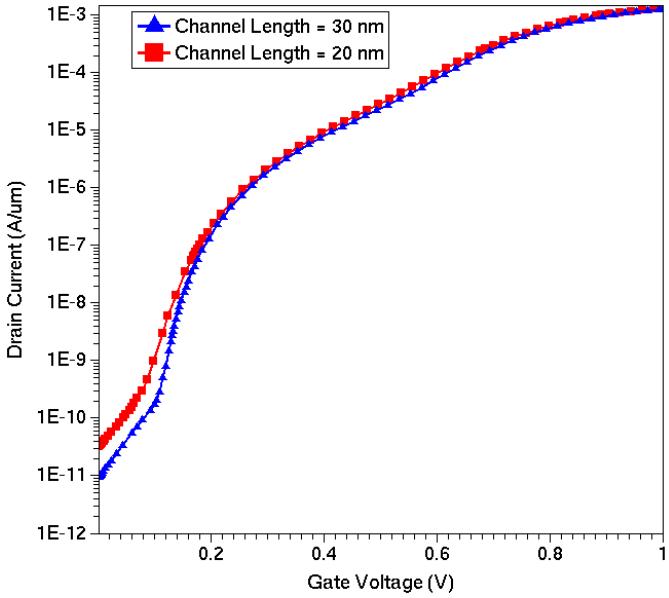
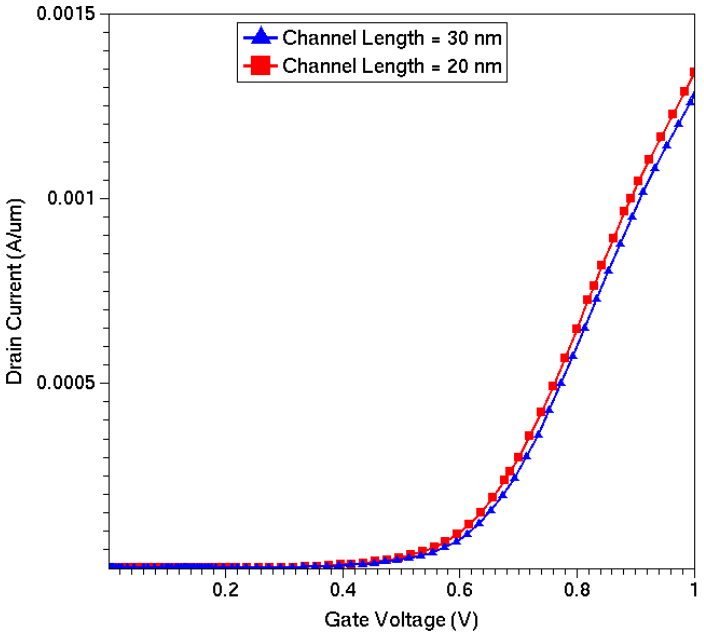


Figure 5.12 : I_d vs V_d characteristics of hybrid MOSFET with oxide layer (MOS_TFET_with_Oxide).

5.5 Effect of Channel Length on I_d vs V_g Characteristics



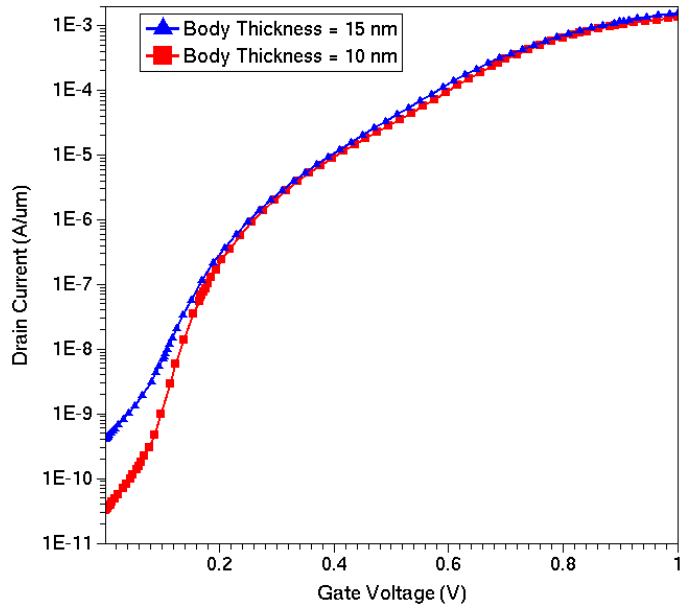
(a)



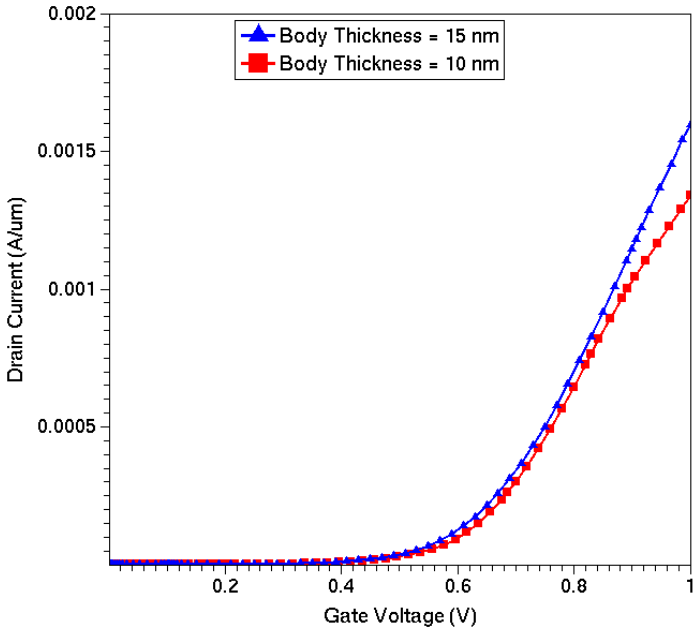
(b)

Figure 5.13 : Effect of channel length on I_d vs V_g characteristics of hybrid MOSFET (MOS_TFET_with_Oxide) with drain voltage of 1.0 V and drain current on (a) log scale, and (b) linear scale.

5.5 Effect of Body Thickness on I_d vs V_g Characteristics



(a)



(b)

Figure 5.14 : Effect of body thickness on I_d vs V_g characteristics of hybrid MOSFET (MOS_TFET_with_Oxide) with drain voltage of 1.0 V and drain current on (a) log scale, and (b) linear scale.

CHAPTER

6 CONCLUSION AND FUTURE WORK

CONCLUSION

In this thesis work, the 2-D device simulation of MOSFET, tunnel FET, and hybrid MOSFET device architectures, have been performed on the Synopsis TCAD (SENTAURES) tool. The thesis work can be divided into three major parts:

In first part, different types of silicon based tunnel FET structures with channel length of 20 nm were first being optimized for lower value of subthreshold swing and higher value of $I_{on}/I_{off.}$ From simulation results, it was found that tunnel FET can be optimized for lower subthreshold swing (< 60 mV/decade) and lower value of I_{off} current (< 10 pA) but the higher I_{on} current values (~ 1 mA/μm) is still a challenge for silicon based tunnel FET.

In the second part, silicon based MOSFET structures with channel length of 20 nm were being optimized for lower value of subthreshold swing and higher value of I_{on} / $I_{off.}$ From simulation results, it was found that silicon based MOSFET structures can be optimized for high I_{on} current values (~ 1 mA/μm) but have a fundamental lower limit on subthreshold swing value (i.e. SS > 60 mV/decade).

In the third part both the tunnel FET and MOSFET structures were being combined to form a hybrid MOSFET in different device architectures and then the large signal and small signal simulation results of the hybrid MOSFET structure were being compared with the individual tunnel FET and the individual MOSFET structures for same device dimensions and for same value of I_{off} current value. The large signal and small signal simulation results are listed in table 6.1, and table 6.2 respectively.

Table 6.1 : Comparison of Large Signal Simulation Results

	Double Gate MOSFET	**Double Gate TFET**	**Hybrid MOSFET (MOS_TFET with Oxide Layer**)
Threshold Voltage (mV) (V_{GS} Value at $I_D = 10^{-7}$ A/um)	271	155	186
I_{on} Current (A/um)	3.35×10^{-3}	0.51×10^{-3}	1.34×10^{-3}
I_{off} Current (A/um)	3.5×10^{-11}	3.3×10^{-11}	3.2×10^{-11}
I_{on} / I_{off}	9.57×10^{7}	1.55×10^{7}	4.19×10^{7}
Point Subthreshold Swing (mV/decade)	71.2	31.9	31.5
Average Subthreshold Swing (mV/decade)	71.3	40.8	48.9

Table 6.2 : Comparison of small signal parameters

Parameter	Device Type	Gate Voltage				
		0.2 V	**0.4 V**	**0.6 V**	**0.8 V**	**1.0 V**
C_{gs} (fF μm^{-1})	DG_MOSFET	0.337	0.414	1.008	1.778	1.973
	DG_TFET	0.329	0.350	0.420	0.545	0.569
	MOS_TFET with_Oxide	0.306	0.322	0.488	0.833	0.943
C_{gd} (fF μm^{-1})	DG_MOSFET	0.286	0.285	0.279	0.284	0.30
	DG_TFET	0.30	0.302	0.306	0.314	0.370
	MOS_TFET with_Oxide	0.305	0.305	0.305	0.306	0.318
g_m ($AV^{-1}\mu m^{-1}$)	DG_MOSFET	3.1×10^{-7}	2.0×10^{-4}	4.0×10^{-3}	8.0×10^{-3}	8.4×10^{-3}
	DG_TFET	2.1×10^{-5}	2.0×10^{-4}	7.0×10^{-4}	1.5×10^{-3}	1.6×10^{-3}
	MOS_TFET with_Oxide	2.9×10^{-6}	8.1×10^{-5}	1.1×10^{-3}	3.9×10^{-3}	3.1×10^{-3}
g_{ds} ($AV^{-1}\mu m^{-1}$)	DG_MOSFET	6.3×10^{-8}	2.3×10^{-4}	4.1×10^{-3}	8.2×10^{-3}	8.6×10^{-3}
	DG_TFET	2.2×10^{-5}	1.9×10^{-4}	6.9×10^{-4}	1.5×10^{-4}	1.6×10^{-3}
	MOS_TFET with_Oxide	4.8×10^{-6}	8.9×10^{-5}	1.1×10^{-3}	4.0×10^{-3}	3.2×10^{-3}
g_m / g_{ds}	DG_MOSFET	4.921	0.870	0.976	0.976	0.977
	DG_TFET	0.955	1.053	1.015	1.0	1.0
	MOS_TFET with_Oxide	0.604	0.910	1.0	0.975	0.969
f_T (Hz)	DG_MOSFET	7.92×10^{7}	4.55×10^{10}	4.95×10^{11}	6.17×10^{11}	5.88×10^{11}
	DG_TFET	5.31×10^{9}	4.88×10^{10}	1.53×10^{11}	2.78×10^{11}	2.71×10^{11}
	MOS_TFET with_Oxide	7.55×10^{8}	2.06×10^{10}	2.21×10^{11}	5.45×10^{11}	3.91×10^{11}

From simulation results, it was found that the hybrid MOSFET structure overcomes the fundamental lower limit of subthreshold swing of MOSFET and also overcomes the lower I_{on} current value of tunnel FET. The objective of this thesis work was to develop a new device architecture which can overcome the problems of both MOSFET and tunnel FET and can replace these devices. Both the large signal and the small signal simulation results indicates that the hybrid MOSFET device structure can replace both the tunnel FET and MOSFET for low power applications.

FUTURE WORK

In this thesis work only silicon based tunnel FET were included. The lower band gap materials and hetro-junctions can also be used for tunnel FET for higher I_{on} current values. Here, only the device level simulation is being performed for discrete MOSFET, tunnel FET, and hybrid MOSFET device architectures. In future there is target to develop the compact models for tunnel FET and hybrid MOSFET and then perform the circuit level simulation.

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