Implementation of All Optical Arithmetic and Logic Unit Based on Nonlinear Properties of Semiconductor Optical Amplifiers

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Certificate

I, **Sanmukh Kaur** hereby certify that the work which is being presented in this thesis entitled **"Implementation of All Optical Arithmetic and Logic Unit Based on Nonlinear Properties of Semiconductor Optical Amplifiers"** in partial fulfillment of requirements for the award of degree of the Doctor of Philosophy in Electronics and Communication Engineering from Thapar University, Patiala, is an authentic record of my own work carried under the supervision of **Dr. R. S. Kaler** and **Dr. T. S. Kamal**.

The matter presented in this thesis has not been submitted in any other University/ Institute for the award of any degree or diploma.

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Abstract

Optical communication systems operating at gigabits per second are commercially available and the data rates are achieved above 10 Tb/s in research laboratories. In order to achieve such data rates, all-optical computing should be realized using digital optical devices. These days, ultra-fast and all-optical processes are required in the high-capacity photonic networks to avoid optoelectronics conversions.

The key components for these all-optical networks amongst others are all-optical regenerators, wavelength converters, packet switches and all optical memory. All optical gates, optical arithmetic and logic circuits and flip-flops form important subsystems of these components. An all-optical arithmetic and logic unit is the integral part of optical computing and data processing. So, there is a need of all optical digital devices which provide better performance (in terms of simple structure, operation at multi Gbs^{-1} speeds, photonic integration etc.) for future all optical networks.

With the advances in the optical semiconductor device design and fabrication techniques, the semiconductor optical amplifiers (SOAs) have become a preferred choice for use in future optical communication networks for in line amplification and optical switching. This thesis mainly designs, characterizes and investigates all optical arithmetic and logical devices using on nonlinear properties of semiconductor optical amplifiers. The all optical digital devices are implemented considering various important design aspects such as data rate; simple structure; potential for integration etc.

Initially an optical gate architecture is proposed to perform AND, OR and NOT logic gates using a single SOA. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates. Maximum extinction ratio and contrast ratio achieved are 19dB and 17.2 dB respectively. Simple structure and potential for integration makes the proposed architecture an interesting approach in photonic computing and optical signal processing.

Next we investigated SOA-based all-optical flip flops, binary counter and registers. First, a simple and new scheme for all-optical SR and D flip-flop employing XGM effect in two wideband SOAs is proposed. The simulation results exhibit contrast ratio of 13 dB and an amplitude modulation of less than 2.5 dB. Flip-flop operation has been verified for several set-reset pulse signals confirming successful operation at 10Gb/s. Secondly, we investigated the operation of a circular shift register for a 10-bit input sequence at the sequence bit rate

f_b = 2.5 Gb/s and f_b = 10 Gb/s respectively. The all-optical circular shift register is realized using a fiber-loop based optical buffer (OB) and an optical AND gate. BER = 10^{-9} is achieved at an OSNR of 16dB at the output of the shift register. The dependence of the output quality factor (*Q*-factor) on SOA parameters is also investigated and discussed.

Finally, an all optical binary counter is presented employing two stages of optical T flip-flop and an optical NOT Gate. The TFF consists of a SOA based Mach–Zehnder interferometer and an external feedback loop. The proposed counter is implemented using the minimum number of active components and with only a single control signal as input. Principle of operation is numerically evaluated for the proposed counter at 5 GHz. The switching times are less than 80 ps. Simple structure implies low power consumption and reduced footprint making it ideal for photonic integration.

Further, by using nonlinear effects in a SOA, different functions of optical digital signal processing are realized. In particular the logic functions of integrated addition-subtraction, decoder, data comparator and demultiplexing are demonstrated. The all optical implementations are based on SOA-MZI based optical tree architecture (OTA). SOA-MZI based all optical demultiplexer operation has also been analyzed for demultiplexing of an optical time division multiplexing signal at data rates up to 160 Gb/s.

Therefore, this study establishes the designs and investigations of all optical arithmetic and logical devices, which are very essential in the high capacity core networks in order to avoid optoelectronics conversions and deal with the revolutionary growth of internet traffic for the future photonics networks.

List of Publications

The thesis includes following research papers:

[1] Sanmukh Kaur and R. S. Kaler, "Ultrahigh speed reconfigurable logic operations based on single semiconductor optical amplifier", **OSA**: Journal of the Optical Society of Korea, vol.16, no.1, pp. 13-16, March 2012.

[2] S. Kaur and R.S. Kaler, "All-optical circular shift register based on semiconductor optical amplifiers", **Springer**: Optical and Quantum Electronics, vol.46, no.8, pp. 991-998, 2014.

[3] S. Kaur and R.S. Kaler "5 GHz all-optical binary counter employing SOA-MZIs and an optical NOT gate", **IOP Publishing**: Journal of Optics, vol. 16, 4pp, Feb. 2014.

[4] S. Kaur and R.S. Kaler, "Performance of RZ and NRZ modulation—Format in 40–160 Gb/s OTDM system demultiplexing", **Elsevier**: Optik - International Journal of Light and Electron Optics, vol.124, no.12, pp.1100–1104, June 2013.

[5] S. Kaur, "All optical data comparator and decoder using SOA-based Mach–Zehnder interferometer", **Elsevier**: Optik - International Journal of Light and Electron Optics, vol.124, no.17, pp.2650– 2653, Sep. 2013.

[6] S. Kaur and R.S. Kaler, "All optical SR and D flip-flop employing XGM effect in semiconductor optical amplifiers", **Elsevier**: Optik - International Journal of Light and Electron Optics, vol.125, no.02, pp.865– 869, Jan.2014.

[7] Sanmukh Kaur and R.S.Kaler, "All optical integrated full adder-subtractor and demultiplexer using SOA-based Mach–Zehnder interferometer", International Journal of Engineering Science and Technology , vol.4, no.01, Jan. 2012.

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List of Acronyms

IP	Internet protocol
HPCM	High Performance Computing Machines
UNI	Ultrafast Nonlinear Interferometer
LCD	Liquid Crystal Display
DPSK	Differential Phase Shift Keying
SR	Set-Reset
RAM	Random Access Memory
OBF	Optical Band pass Filter
EDFA	Erbium Doped Fiber Amplifier
XPM	Cross Phase modulation
OTDM	Optical Time Division Multiplexing
SOA	Semiconductor Optical Amplifier
DWDM	Dense Wavelength Division Multiplexing
WDM	Wavelength Division Multiplexing
OTA	Optical Tree Architecture
MZI	Mach-Zehnder Interferometer
VOA	Variable optical attenuators
BCD	Binary Coded Decimal
TFF	T flip flop
O-E-O	Optical-Electrical-Optical
OAMPs	Optical amplifiers
AM	Amplitude Modulation
CR	Contrast Ratio
FF	Flip Flop
FWHM	Full Wave Half Maximum
SNR	Signal to Noise Ratio
CW	Continuous Wave
BPF	Band pass Filter
RZ	Return to Zero
NOLM	Nonlinear Optical Loop Mirror

ISI	Inter Symbol Interference
SLM	Spatial Light Modulators
OB	Optical Buffer
OSNR	Optical Signal to Noise Ratio
MSD	Modified Signed-Digit
TOAD	Terahertz Optical Asymmetric Demultiplexer
Q	Quality
PolSK	Polarization Shift Keying
BER	Bit Error Rate
SLALOM	Semiconductor Laser Amplifier in a Loop Mirror
UNI	Ultrafast Nonlinear Interferometer
TWA	Travelling Wave Amplifier
OFA	optical fiber amplifier
NRZ	Non Return to Zero
RZ	Return to Zero
TMM	Transfer Matrix Method
HNLF	Highly Nonlinear Fiber
ER	extinction ratio
XGM	Cross gain modulation
AR	Anti-Reflection
FF	flip flop
Ch	Channel
NRZ	Non Return to Zero
CP	Control pulse
PRBS	Pseudo- Random Bit Sequence
FWM	Four Wave Mixing
ASE	Amplified spontaneous emission
PPLN	Periodically poled lithium niobate
SPM	Self Phase Modulation

Chapter 1
Introduction

1.1 Introduction and Motivation

Optical fiber transmission using dense wavelength division multiplexing (DWDM) systems is used for transporting internet data between powerful electronic Internet protocol (IP) routers within today's Internetworks. Different wavelength division multiplexed fibers are connected to an IP router, where signals are transformed from the optical to the electronic domain at the input side and from electronic to optical domain at the output side. Routers are required to handle data with data rates of the order of Tbit/s for redirecting incoming Internet packets from maximum loaded wavelength division multiplexing fibers [1].

When comparing the increase of optical fibers capacity with the speed of electronic processor, it is observed that there is a difference in bandwidth handling capacity of electronic routers and optical fibers. This situation could become more complicated if in the future optical networks routers will have to handle thousands of optical wavelengths and there is a further increase in bit rates up to 40 Gbit/s or beyond. Electronic processing in this scenario would not be able to handle the routing of a massive number of packets per second, which could easily lead to router congestion. From an economic perspective, conversions between optical and electrical formats at the inputs and outputs of a router can grow to be half of the cost of a node.

The ultimate goal is to minimize the amount of complex electronics [2], [3] and hence the cost, by considering an all-optical network, where switching is carried out transparently in all optical form, with a minimum amount of electronic processing.

The interest in the field of optical digital signal processing has been growing in for a long time. Optical digital signal processing is promising for those applications in which fast computational speed is one of the essential requirements [4]. All optical short range interconnection networks are one of the examples. The congestion in the chip to chip or chip to memory communication interface hampers the improvement of present day high performance computing systems. The limitations are imposed by the density of the wiring, throughput and the more power consumption [5], [6]. In such types of optical networks, optical digital signal processing could become the most suitable and efficient

model for simple as well as ultrafast control and switching operations. For applying optical digital processing for the purpose of controlling the various network operations, complex functions are required.

There had been many approaches to realize optical logic function using nonlinear effects. Different approaches are based on nonlinear effects either in optical fiber or in semiconductor optical amplifier. In comparison to utilizing the nonlinear effect in optical fiber, SOA-based implementations have shown great potential with regard to the various performance parameters such as higher data rates, small footprint, less power consumption, and optical integration [7]. The fast non linear characteristics of semiconductor optical amplifiers are very attractive for applications in all optical digital processing such as all optical Gates, flip flop, counter, registers, square wave generation, adder, subtractor and comparator etc.

Optical logic gates with higher speeds are the main elements of the future generation optical networks as well as the computing systems. These are used to carry out all optical signal processing functions, such as binary addition, all-optical header recognition, label swapping, parity checking, and data encryption [8]. A gate used to modulate a continuous wave (CW) signal can function as a wavelength converter. A gate used to modulate a pulse train can act as a part of an optical regenerator. Gates can also be used for time demultiplexing of input optical signals. Optical gates such as AND and XOR are used in routing functions [9]. All-optical flip-flops have been widely investigated as they can be employed in large number of applications. The application areas include optical packet switches, in which routing, switching, and forwarding functions can be directly carried out in the optical domain utilizing these elements. All optical binary counters are also one of the key components to be utilized in photonics networks. These find applications in both areas of optical computing and communication. The device can be used in payload processing, header recognition and as a finite state machine in packet switching networks and optical computing [10].

Optical shift registers find applications in optical packet buffers, serial-to-parallel converters and synchronizers. They might also become essential building blocks for more complex subsystems. These devices have received considerable attention as they can play a significant role in signal processing techniques. Other applications include cyclic operations such as parity and cyclic redundancy checks that enable digital detection and correction of transmission errors. All optical combinatorial circuits are essential for management of contentions and controlling the switching operation in the nodes of an

optical packet switching network. Boolean numbers addition is a primary function to be performed in the header processing of packets.

So, there is a demand of all optical digital devices which provide better performance (in terms of data rate, simplicity for low power consumption and reduced footprint, potential for integration etc.) for future all optical networks. For achieving these objectives it is utmost important to design, characterize and investigate all optical digital devices such as optical Gates, optical arithmetic and logic circuits, flip-flops, counters and registers as these are integral components for optical computing and all optical processing in next generation optical networks [10].

1.2 Semiconductor Optical Amplifiers

1.2.1 The Role of Optical Amplifiers

Optical fiber communication networks have grown rapidly with respect to the deployment and capacity of the networks over the past few decades. There is a growing demand for the networks having large capacity and capability for transparent routing. Continuous up gradation and advances are required to be made in the signal amplification and other processing techniques. Optical amplifiers have made possible a number of significant advances in the optical networks. Light gets attenuated during propagation over long distances in optical fibers. Optical amplifiers are mainly utilized to amplify optical signals. Optical switching and wavelength conversion are also some of the important applications of these devices.

Optical amplifiers can be broadly classified into types: optical fiber amplifiers (OFAs) and semiconductor optical amplifiers (SOAs). Their comparison is given in Table 1.1.

The size of the SOA is small and it is electrically pumped. The SOAs differ from other doped fiber amplifiers in the way of achieving population inversion. The population in the SOA are carriers (i.e. electrons or holes) in a semiconductor material rather than ions in various energy states.

This device is less expensive than the Erbium Doped Fiber Amplifier (EDFA) and can be integrated with modulators, semiconductor lasers, etc. SOAs are sensitive to polarization. Waveguide structure and the gain material are some of the important factors responsible for this. In order to improve polarization sensitivity, waveguides with square-cross section and strained quantum-well material can be used [11].

Table 1.1: Comparison between OFAs and SOAs.

Feature	OFA	SOA
Maximum gain	30 - 50 (dB)	32 (dB)
Insertion loss	0.1 - 2 (dB)	5 - 10 (dB)
Polarisation sensitivity	No	(Less than 2 dB)
Pump	Optical source	Electrical source
3 dB gain bandwidth	30 (nm)	30 – 50 (nm)
Nonlinearities	Negligible	Present
Power output (Saturation)	10 - 15 (dBm)	5 - 18 (dBm)
Noise Figure	3 - 5	6 - 11 dBm
Integrated circuit compatibility	Not compatible	Compatible
Possibility of Functional device	No	Yes

Fiber amplifiers have been dominating the conventional applications in optical fiber communication systems [12]. One example is in-line amplification of the optical signals for compensation of fiber losses. The reason for this was mainly due to the fact that the fiber amplifiers, for example EDFA, provide higher internal gain. They are also not susceptible to internal noise which otherwise can cause the gain to vary dynamically as seen in SOA implementations [13], [14].

SOA is very promising for the use in evolving optical fiber communication networks. This is due to the advances in the device design and optical semiconductor fabrication techniques. SOA can be used for amplifying optical signals and also have many functional applications. These include wavelength conversion, an optical switching, regeneration, in line amplification and mid span spectral inversion. These are the main functions required in transparent optical networks. Transparent optical networks do not require any conversion of optical signals into the electrical domain and vice-versa.

Polarization independence compact size, low power consumption and high speed [15] are the salient features of the device.

1.2.2 Principle of Semiconductor Optical Amplifier

Figure 1.1 shows the schematic configuration of device. An electrical current drives the device. Input signal is imparted gain via stimulated emission by the active region in the

device. Noise accompanies the output signal. The added noise is produced due to amplified spontaneous emission (ASE) during the amplification process.

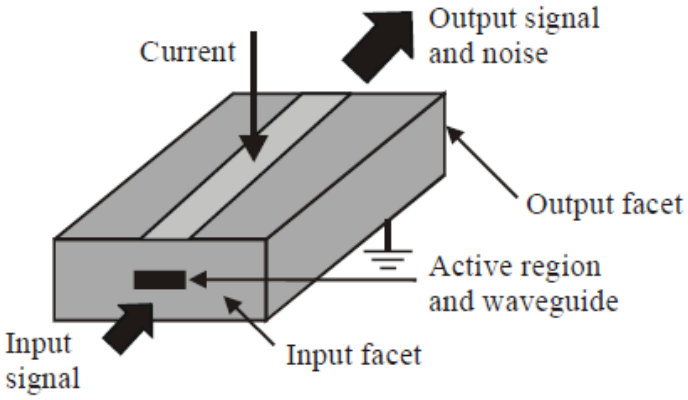


Figure 1.1: Schematic configuration of an SOA.

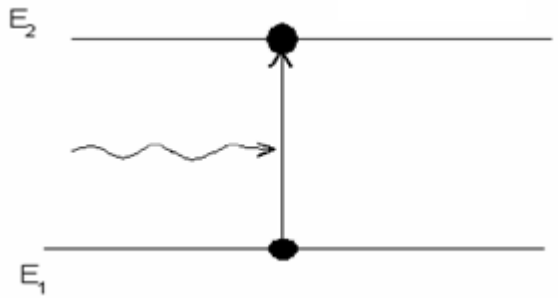
The input signal power along with internal noise generated during the amplification process influence the gain of a semiconductor optical amplifier. Gain decreases with the increase in the power of input signal. Carrier recombination lifetime (few hundred picoseconds) determines the gain dynamics of the device [13]. The amplifier gain responds quickly to the variations in the power of the input signal. Signal distortion may be caused by dynamic change in the gain of the amplifier. Signal distortion may become more severe if the bandwidth of modulated signal is further increased [13].

The SOA utilizes stimulated emission principle for amplifying an optical information signal. The optical input signal is applied to the active region of the device with the help of coupling [16]. The injection current delivers the external energy to pump the electrons to the conduction band. The input optical signal stimulates the transition of electrons in the downward direction to valence band. This results in emitting of photons with the same amount of energy and wavelength as of the input signal. An amplification of optical signal is achieved in this manner.

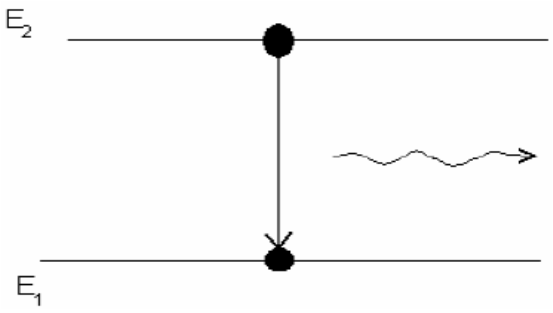
Atom exists only in certain discrete energy state. Absorption and emission of light cause them to make a transition from one discrete energy state to another state. The energy of the emitted light is related to difference between the two energy states. One of them is the higher energy level (E2) and the other is lower energy level (E1) as shown in Figure 1.2. When photon with associated energy E strikes an atom which is at lower energy level (E1), it may cause the atom to get excited to higher energy level (E2). This phenomenon is known as absorption as shown in Figure 1.2(a). As atom in energy state E2 does not

remain stable, the atom yield to lower energy state in arbitrary manner by generating output photon as shown in Figure 1.2(b). This mechanism is called spontaneous emission. Similar to the approach used in a laser, principle of stimulated emission is used in optical amplification [17]. When the incident photon with energy E = hc/ λ interacts with electron in the upper energy level, the stimulated emission takes place, causing the photon to return back into lower energy state with generation of second photon as shown in Figure 1.2(c), In this relation, h, c and λ are Plank's constant, velocity of light in vacuum and wavelength of light respectively [18]. The amplification of light takes place, when input as well as generated photons are in same phase and discharge two or more number of photons.

For achieving better optical amplification, the density at upper energy state should be larger than population at lower energy state i.e. $N_1 < N_2$, where N_1 and N_2 are population densities of lower energy level and upper energy level, respectively. This is phenomenon is known as population inversion. Population inversion could be achieved by using external source (called pump) which is responsible to excite the electron into higher energy level.



(a)



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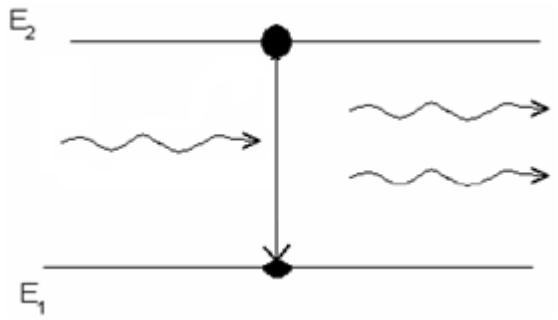


(c)

Figure 1.2: Different processes of optical amplification; (a) Absorption process, (b) Spontaneous emission process and (c) Stimulated emission process.

The stimulating emission process can be dominating only in the case if requirement of population inversion condition is fulfilled. For the case of SOA the requirement is satisfied by doping the n-type and p-type cladding layers to such a high level that the Fermi level separates the band gap in forward bias condition of p-n junction. The rates of three types of emission processes such as absorption, spontaneous emission and stimulated emission are given as

$$R_{spon} = AN_2$$

$$R_{stim} = BN_2\rho_{em}$$

$$R_{abs} = B'N_1\rho_{em} \quad (1.1)$$

Where A , B and B' are constants. ρ_{em} is the spectral density of the electromagnetic energy. Also, N_2 is the atomic density of excited state. In the condition of thermal equilibrium, the atomic densities at the two levels are distributed as per Boltzmann statistics [19], *i.e.*

$$\frac{N_2}{N_1} = \exp\left(\frac{-E}{K_B T}\right) \equiv \exp\left(\frac{-hf}{K_B T}\right) \quad (1.2)$$

Where K_B and T are the Boltzmann's constant and the absolute temperature respectively. As N_1 and N_2 will not change with respect to time in the condition of thermal equilibrium, the upward transition rate and the downward transition rate has to be kept same.

$$AN_2 + BN_2\rho_{em} = B'N_1\rho_{em} \quad (1.3)$$

By using equation (1.2) in (1.3), the spectral density ρ_{em} becomes [20]

$$\rho_{em} = \frac{A\ /B}{(B'/B)\exp\left(\frac{hf}{K_B T}\right) - 1} \quad (1.4)$$

The stimulated emission and absorption rates are achieved similarly and are given as follows

$$R_{stim}(\omega) = \int_{E_C}^{\infty} B(E_1, E_2) f_C(E_2)[1 - f_v(E_1)]\rho_{Cv}\,\rho_{em}\,\partial E_2 \quad (1.5)$$

$$R_{abs}(\omega) = \int_{E_C}^{\infty} B(E_1, E_2) f_v(E_1)[1 - f_c(E_2)]\rho_{Cv}\,\rho_{em}\,\partial E_2 \quad (1.6)$$

Where $f_C(E_2)$ are the occupation probability electrons of conduction band and $f_v(E_1)$ are the occupation probability electrons in valence band respectively. Also, $\rho_{em}(\omega)$ is the spectral density of photons, ρ_{Cv} is joint density of the states and E_C is the energy of conduction band.

When injection of carriers in active layer becomes larger than a certain value, which is known as transparency value, population inversion takes place and optical gain is exhibited by active region. The input optical signal propagating inside the active layer will then be amplified as $exp(gz)$, where g is defined as gain coefficient. In this g is proportional to $R_{stim} - R_{abs}$. Where g is the function of injected carrier density N, then peak value of gain g_p depends upon N which is given by empirical approach as

$$g_p(N) = a(N - N_t) \quad (1.7)$$

In this equation N_t represents the transparency value of the carrier density and the differential gain is represented by symbol a. Typical value of a for InGaAsP amplifiers is in the range $2 - 3 \times 10^{-16}$ cm^2. Typical value of N_t for InGaAsP amplifiers is in the range $1.0 - 1.5 \times 10^{18}$ cm^{-3} [21]. The small signal gain can be described by the following expression.

$$g_0 = (\Gamma\alpha/V)\left(I\tau/q - N_t\right) \quad (1.8)$$

In this equation Γ and α are defined as the confinement factor and the differential gain respectively. V is the active volume of the device. I, q and N_t are the bias current, charge of electron and transparency carrier density respectively. Also τ is carrier lifetime, which represents the total recombination time of charge carriers in absence of any stimulated recombination.

Carrier lifetime is defined as $R_{spon} + R_{nr} = N/\tau$, where N is carrier density and R_{nr} is nonradiative recombination rate. R_{spon} and R_{nr} increase nonlinearly with increase in N as given by the following equation

$$R_{spon} + R_{nr} = AN + BN^2 + CN^3$$

Where A represents nonradiative coefficient, which is due to recombination at defects or traps. B and C represent the spontaneous radiative recombination coefficient and Auger coefficient respectively. The carrier lifetime thus becomes dependent on N and it can be obtained by using expression $1/\tau = (A + BN + CN^2)$

1.3 Optical Arithmetic and Logic Unit

An all-optical arithmetic and logic unit is the integral part of optical computing and data processing. By means of an arithmetic and logic unit, so many binary logic operations such as AND, OR, NOT, NOR, flip-flop (used as memory unit for storage), data comparator, shifting, counting etc., as well as some arithmetic operations, such as addition, subtraction, etc., can be performed. An optical arithmetic and logic unit may be developed by exploiting nonlinear properties of an SOA. Basic building blocks required to implement such an optical logic processor are the optical logic Gates and SOA is found to be the very promising in this aspect.

1.3.1 Architectures for all-Optical Logic Gates

The use of optical fibre as well as semiconductor elements has facilitated the development of all-optical architectures for logic gates. Next, the most important all-optical configurations for implementing logic gates will be presented, describing their main advantages and disadvantages as well as their applications.

1.3.1.1 Sagnac Interferometers

The Sagnac interferometer consists of an optical ring cavity in which two light beams are propagating in opposite directions. These two beams interfere at a beam splitter and as the length of the optical path of the ring cavity is the same; both the clockwise and counter-clockwise beams interfere with the same phase. If, however, the interferometer is rotating, then the light that goes round in the direction of rotation will have a shorter distance (as the mirrors of the cavity are moving towards it) than the other light beam (which experiences the mirrors as receding), and the phase will be different.

Most common interferometric approach for optical signal processing is NOLM. Modifications of this have also been proposed to implement, for example, demultiplexers, switches and optical gates. This is the case of the TOAD, the SLALOM and the SOA-assisted SAGNAC interferometers.

A. NOLM

One of the first architectures used to implement logic functions in the optical domain was the nonlinear optical loop mirror. This configuration presents some drawbacks and limitations. For example, this configuration works properly only if there is no interaction between the signals counter-propagating inside the loop. This supposition is valid only if the pulse length is shorter enough in comparison with the fiber length. If this condition is not achieved, the influence between the two signals cannot be neglected, since there are crossed-interaction effects. One more limitation is derived from the fibre length to use in order to achieve a notable phase shift. The first NOLM that was used required a 2 km length fibre to achieve a complete demultiplexing and switching function. Later on, this length has been reduced to 10 m, but even so it still being very difficult to integrate. Moreover, the energy of the control pulse needed to achieve the nonlinear effect in the fibre is too large, in the order of tens of picojoules, which limits the performance in real systems.

On the other hand, the main advantage of this configuration is that, due to the fact that switching is based on a passive element, high bit rates operation is achievable. In addition, it does not require interferometric alignment, is robust, and is of simple construction. Using this configuration several functions may be implemented. It has been used to realize reconfigurable all-optical logic gates for ultra-fast applications [22].

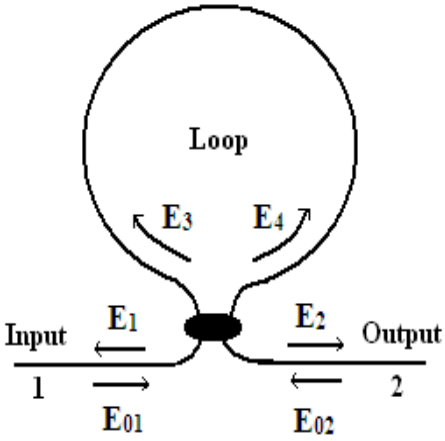


Figure 1.3: The original optical NOLM based on a fibre loop.

B. TOAD

The terahertz optical asymmetric demultiplexer consists of a nonlinear optical element asymmetrically placed within a short fibre loop and an intra-loop 2x2 coupler used to inject a control pulse. A signal pulse enters the loop through the main coupler and produces two pulses in the loop. As the pulses traverse the loop, the clockwise pulse and

the counterclockwise pulse are always located on opposite sides of the loop, equidistant from the midpoint. Each pulse passes through the nonlinear element once, and they return to the main coupler at the same time. Under these conditions, the pulses arrive at the output coupler synchronised and in-phase. Both pulses interfere as in an ordinary loop mirror and do not emerge from the output port.

If a control pulse is injected into the loop via the intra-loop 2x2 coupler just after one of the pulses passed through the nonlinear element and before the second one did it, the behaviour of the device changes. The control pulse passes once through the nonlinear element, modifies its optical properties and then passes out of the loop. When the second pulse reaches the nonlinear element, the conditions of the nonlinear element are not the same that those of the first pulse. As a result the destructive interference between the two pulses at the TOAD's output is incomplete, and a pulse is present at the output.

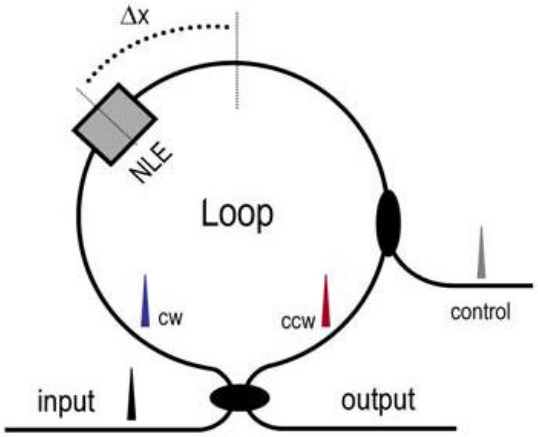


Figure 1.4: The terahertz optical asymmetrical demultiplexer.

Usually the nonlinear element used in the TOAD is an SOA. One limitation of the TOAD approach is the finite propagation time of the pulse across the SOA. If the offset of the SOA from the centre is decreased, the effective SOA length that the two counter-propagating pulses see is reduced. The decrease in effective SOA length leads to a reduction in the contrast ratio of the TOAD switching and thus, an excess power penalty. The effective length of the SOA required for producing the relative π phase shift places a practical limitation on the switching window size of the TOAD to be greater than the propagation time of the pulse through the SOA.

In cascaded configurations using TOADs certain stability to thermal effects is observed. This is because the counter-propagating pulses in each TOAD travel through the same span of fibre. The integration of the TOAD is currently a difficult problem yet to be solved.

C. SLALOM

This device is based on the Sagnac interferometer. However, its operation does not depend on the optical nonlinearity of the fibre but on the optical nonlinearity of a semiconductor laser amplifier (SLA) in the fibre loop.

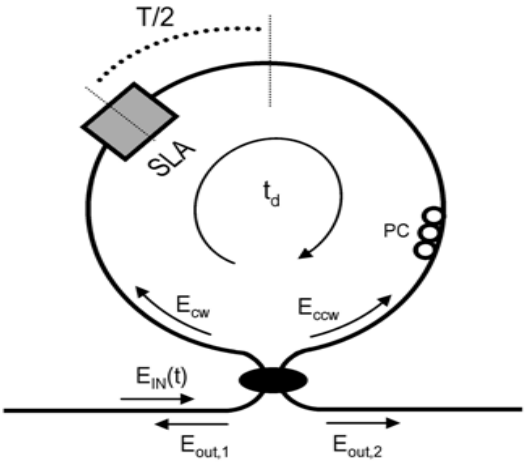


Figure 1.5: The SLALOM basic configuration.

As compared to the NOLM, the SLALOM has two advantages. Firstly, the device may be very compact so that integration on a chip is possible. Secondly, the required optical power is of the order of 1 mW. A disadvantage is that the operation speed is generally lower. It is of the order of a few GHz for most applications of the SLALOM except the applications as demultiplexer.

The SLALOM is a configuration that may be used as an all-optical header processor based on correlation pulses, an all optical NOT gate [23], an all-optical binary half-adder, a phase comparator in a clock recovery scheme and a number of applications on photonic systems, like pulse shaping, decoding, retiming and time-division demultiplexing.

1.3.1.2 UNI

The concept of operation of the ultrafast nonlinear interferometer gate relies on polarization rotation of the incoming signal to be switched in the presence of a switching pulse in a SOA.

This device shows two main drawbacks. On one hand, it is strongly polarization sensitive as its operation relies on optimum adjustment of the polarization of the incoming data signal. On the other hand, the recovery time of the SOAs is very slow, so the transit time from one pulse to the next it is not very short. This imposes a restriction in terms of maximum achievable bit rate operation. In this configuration, a filter is needed to eliminate the control signal, although several architectures have been proposed in which

the control signal counter-propagates the data signals, avoiding the use of a filter at the output. Furthermore, due to the use of fibre to cause the polarization rotation, this design shows many difficulties to be integrated.

Obviating the need of the output filter, cascaded configurations using UNIs are possible since the output of one device may be used as the signal or control to the subsequent device. This configuration has been used to successfully achieve switching, demultiplexing, optical regeneration, clock recovery, logic operations, such as XOR, NAND [24], AND and NOT functions and other signal processing functionalities.

1.3.2 Logic Gates based on Nonlinearities in Semiconductor Optical Amplifiers

Nonlinear effects make SOA a very interesting device for applications in optical networks. Semiconductor optical amplifier (SOA) exhibits various non-linear effects, which restrict it to use for various applications in optical communication systems [25]. These same nonlinearities can be used for ultra fast switching and gating applications. SOA nonlinearities are mainly caused by carrier density variations in the amplifier. Amplifier input signals are responsible for the carrier density changes [10]. There are four main types of nonlinearities: cross phase modulation (XPM), Cross gain modulation (XGM), self-phase modulation (SPM) and four-wave mixing (FWM).

1.3.2.1 Cross-Gain Modulation

The XGM effect results in the change of the semiconductor optical amplifier gain with the input signal power. The increase in the power of the input optical signal results in the decrease in the density of the carriers in the SOA. Due to this, the amplification gain of the SOA is also decreased. These dynamic processes taking place in the carrier density of the semiconductor optical amplifier are very fast (of the order of picoseconds). Thus it is possible to utilize this variation in the gain as per the bit to bit fluctuations of the input signal power. Figure 1.3 shows the operation principle of of a wavelength converter using XGM effect. There are two input data signals. One is low power continuous wave (CW) signal and the other is a pulsed signal. These two signals which are at different wavelengths are coupled to the SOA. When an input optical pulse appears on the pulsed signal, SOA gain decreases. This results in the continuous signal experiencing low amplification. On the other hand, if there is no light pulse on the pulsed input signal the gain of the device increases. This results in the CW signal experiencing high

amplification. Thus incoming pulsed signal at λ_s is wavelength converted to $\lambda=\lambda_p$. The signal is inverted at the output.

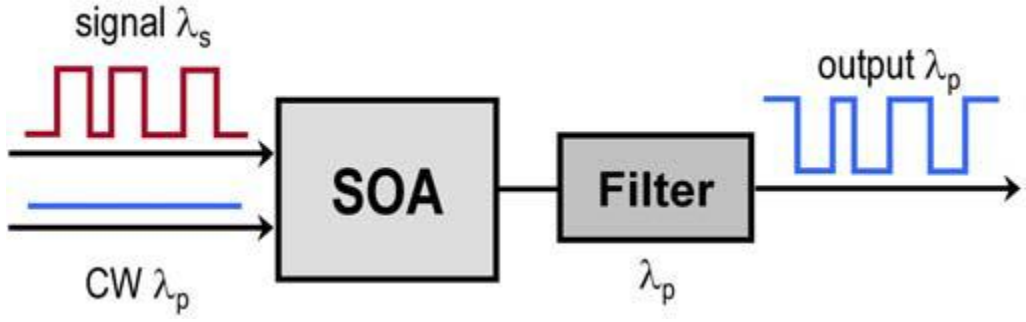


Figure 1.6: Simple wavelength converter using SOA –XGM.

Low extinction ratio (ER) is the main disadvantage of SOA-XGM based architectures. Lower value of the extinction ratio are possible (<10 dB) as the output signal in the lower state is not negligible. High input signal powers (0 dBm) are required to deplete the carriers and thereby saturate the device. Very good-shaped filters are required to filter the signal at the output of the device. As a result of the change of the carrier density, a change in the refraction index is also induced. This modulates the phase of the CW thus increasing the distortion of the output signal.

Many configurations are proposed in the literature utilizing this nonlinear effect. Several types of logic functions have been realized using cross gain modulation effect in the semiconductor optical amplifiers. These include AND, XOR and NAND Implementations [26].

1.3.2.2 Cross-Phase Modulation

The latter effect is the operation principle of XPM. The refractive index of the active region of semiconductor optical amplifier is not constant. It depends on the carrier density and hence the material gain. Thus phase and the gain changes of an optical signal travelling through the amplifier are coupled through the gain saturation. The amount of coupling depends upon the linewidth enhancement factor α.

When more than one signal is applied to an SOA, XPM will take place between the applied signals. Wavelength converters and other functional devices can be created using XPM. As the XPM causes only phase changes, the semiconductor optical amplifier has to be put up in an interferometric configuration so that phase variations in the signals can be converted to the intensity variations using constructive or destructive interference. SOA is placed in the interferometer consisting of two identical branches. Both the continuous

wave signal and the pulsed signal are coupled to both the branches. Symmetric optical couplers are considered having a coupling factor of α. In this way, the continuous wave signal is modulated in one side of the branch as a result of variations in the pulsed signal thereby achieving constructive or destructive interference at the output. Figure 1.4 depicts the principle of operation. Signals are counter-propagated in the interferometer. Phase information is converted into intensity information due to the interferometric arrangement. XPM based architectures generally use either a Mach-Zehnder or a Michelson interferometric structure.

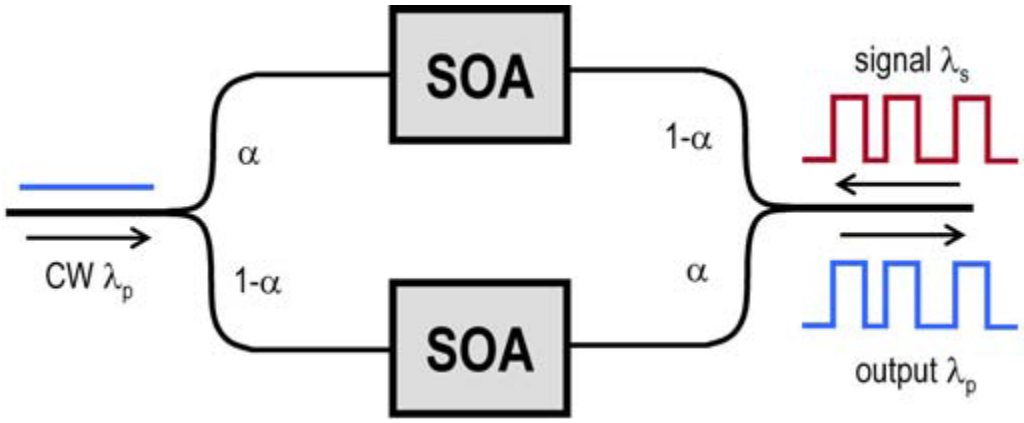


Figure 1.7: Wavelength converter using XPM in SOAs.

1.3.2.3 Four Wave Mixing

Four wave mixing is a nonlinear process, in which a new field gets created in a medium depending upon the product of three input electrical fields. In a semiconductor optical amplifier, gain and phase gratings are produced by beating of three input electric fields (at three different frequencies f_1, f_2 and f_3). This results in scattering the input fields thus generating upper and lower sidebands. This nonlinear effect takes place due to the refractive index dependence on the intensity of the input signal. This results in generation of new frequencies at the output of the device. $2f_1 - f_2$ and $f_1 + f_2 - f_3$ are the combinations which will be at higher level.

Four wave mixing effect is transparent to the data rate and the modulation format of the input optical signals. This is one of the main advantages of this nonlinear effect, as compared to XGM and XPM effects. At the other end, a filter is required for filtering out all the frequency components except the one of interest. The conversion efficiency becomes lower as the frequency difference between the input signals is increased. Thus high powers will be required at the input. FWM effect shows the polarization

dependence. This effect is shown in Figure 1.5. The figure shows one application of this nonlinear effect in the form of wavelength conversion.

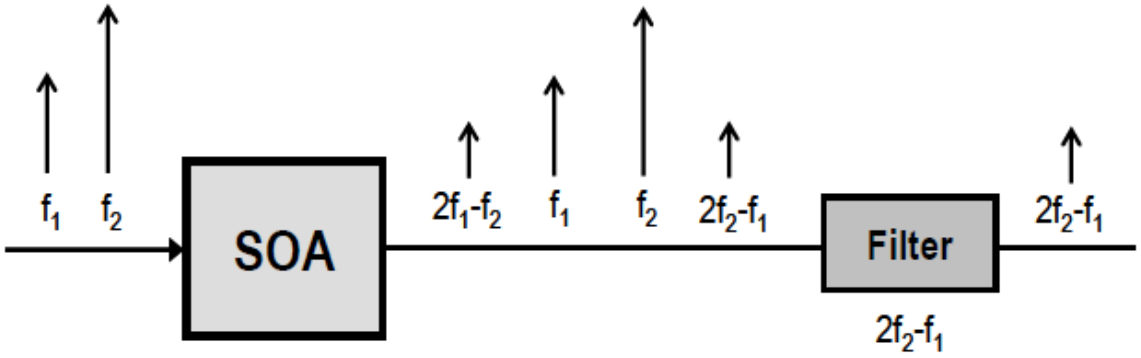


Figure 1.8: Application of FWM effect in SOA for wavelength conversion of input signal. Beating of more than one frequency in the SOA causes new frequencies to appear at the output. A filter is there for filtering all the frequencies at output except the one of interest. FWM effect in SOAs can be used for realization of optical AND Gate [10].

1.3.2.4 The SOA based MZI

One of the preferred architectures for performing logic operations is based on interferometric structures. These interferometric structures often incorporate a nonlinear element in one of its two branches or in both. This nonlinear element will adjust the phase of the signal passing through it to perform the logic operation. The preferred nonlinear element is the SOA, because with this element low power is needed in order to obtain phase shifts (the intensity dependent refractive index is orders of magnitude lager than that of a fibre).

Two input data signals which are at the wavelengths λ_1 and λ_2 respectively are coupled into ports 1 and 2 of the MZI. Continuous wave signal at wavelength λ_{cw} is coupled through port 3. Input data signals are applied to the two semiconductor optical amplifiers. They will modulate the carrier density and hence the refractive index in the two SOAs. This results in phase modulation of the continuous wave signal propagating in the semiconductor optical amplifiers. The phase modulation will be as per the bit pattern of the input data signals. The continuous wave light signals at the output of two SOAs interfere either constructively or destructively at the output of the interferometer. The constructive or destructive interference takes place depending on the cosine of the phase difference between the lights from the respective SOAs ($\cos(\varphi_1 - \varphi_2)$). This is controlled by the input data signals. Wavelength converted output signal appears at port 4 which corresponds to the XOR logic of the two input data signals.

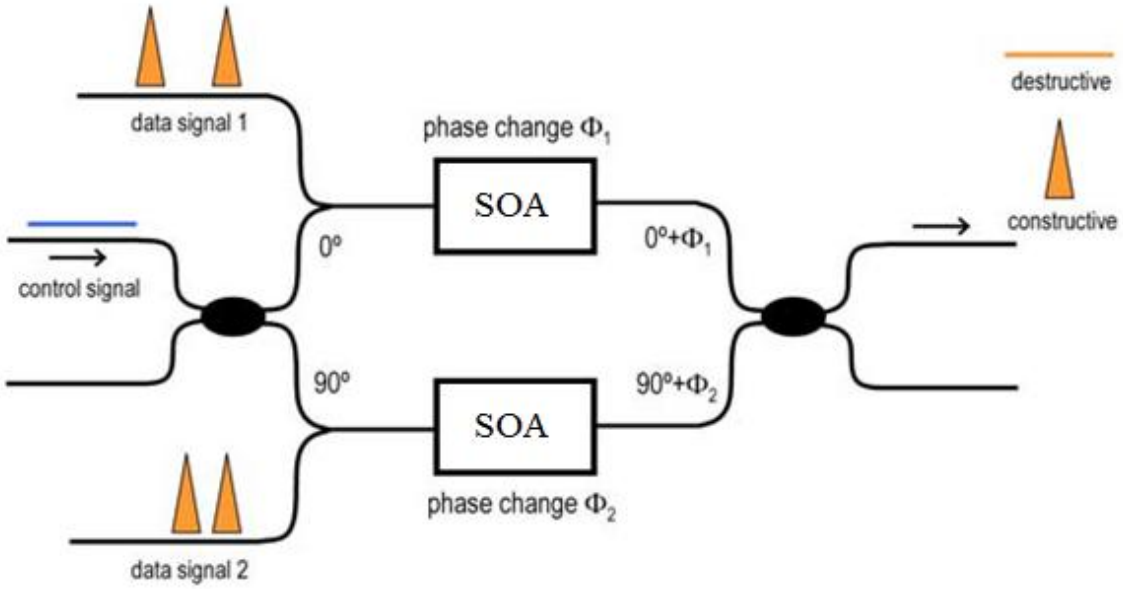


Figure 1.9: Principle of operation of the MZI.

With these structures co-propagation (control and data signals travel in the same direction) as well as counter-propagation (control and data signals travel in opposite directions) is allowed. In some cases, a pulsed signal is used instead of a CW signal. The phase change is induced by non-linear effects (typically XPM or XGM in SOAs). XOR, NOR, OR, NAND [27] and AND logic operations can be performed by using these configurations. SOA-based interferometric configurations have become a reference scheme for several applications, such as signal regeneration, wavelength conversion, demultiplexing, and the logic operations above mentioned.

1.4 Summary

The role and need of arithmetic and logic unit for optical computing and all optical processing in next generation optical networks is discussed. Semiconductor optical amplifiers are introduced and the basic principles of operation have been presented. Important all-optical configurations for implementing logic gates have been presented The fast non linear characteristics of semiconductor optical amplifiers are very attractive for applications in all optical digital processing such as optical Gates, flip flop, counter, registers square wave generation, adder, subtractor and comparator etc. As compared to the nonlinearity of optical fiber, implementations incorporating SOA have demonstrated great potential in terms of small footprint, high speed, optical integration and low power consumption.

Chapter 2

Literature Review and Outline

2.1 Introduction

There has been a growing interest in photonic digital processing for a long time. This is very promising in the application areas where fast computation speed is an important requirement. Short range optical interconnection networks represent one of these scenarios. The congestion in the chip to chip or memory to chip communication interface hampers the improvement of present day high performance computing systems. The limitations are imposed by the density of the wiring, throughput and the more power consumption. In these types of optical networks, optical digital signal processing could become the most suitable and efficient model for simple as well as ultrafast control and switching operations. This is due to the fact that it reduces the packet delay to the optical time of flight between the adjacent nodes. For applying optical digital processing for the purpose of controlling of various network operations, complex functions are required.

All optical combinational circuits are essential for management of contentions and controlling the switching operation in the nodes of an optical packed switching network [28]. Boolean numbers addition is a primary function to be performed in the header processing of packets. The other key components for these all-optical networks are all-optical regenerators, wavelength converters, all optical packet switches [29], and all-optical memory. All optical Gates, optical arithmetic and logic circuits and flip-flops form important subsystems of these components.

Optical logic gates with higher speeds are the main elements of the future generation optical networks as well as the computing systems. These are widely used to carry out all optical signal processing functions, such as binary addition, all-optical header recognition, parity checking, label swapping, and data encryption. A gate used to modulate a continuous wave (CW) signal can function as a wavelength converter. A gate used to modulate a pulse train can act as a part of an optical regenerator. Gates can also be used for time demultiplexing of input optical signals. Optical gates such as AND and XOR are used in routing functions.

All-optical flip-flops have got considerable attention as they can be employed in large number of applications. The application areas include optical packet switches [30], in which routing, switching and forwarding functions can be carried out directly in the

optical domain utilizing these elements. Optical packet switch examples utilizing a flip-flop are given in [29] and [31] respectively. Optical flip-flop is used for storing the switch control information and driving the switching operation in these applications.

All optical binary counters are the key components to be utilized in photonics networks. These find applications in both areas of communication and optical computing. The device can be used in payload processing, header recognition and as a finite state machine in optical computing and packet switching networks.

Optical shift registers find applications in serial-to-parallel converters, optical packet buffers, and synchronizers. They might also become essential building blocks for more complex subsystems. These devices have received considerable attention as they can play a significant role in signal processing techniques. Other applications include cyclic operations. Examples are cyclic redundancy checks and parity that enable digital correction and detection of errors occurring during transmission. All optical combinational circuits are essential for management of contentions and controlling the switching operation in the nodes of an optical packed switching network. Boolean numbers addition is a primary function to be performed in the header processing of packets [32].

SOA is very promising for the use in evolving optical fiber communication networks. This device exhibits various non-linear effects. Nonlinear effects make SOA a very interesting device for applications in optical networks.

These nonlinearities can be used for ultra fast switching and gating applications. Optical logic functions may be implemented by employing nonlinear effects either in optical fiber or in SOA. Implementations utilizing SOA have shown great potential as compared to fiber based implementations. High speed, small footprint, low power consumption and potential for optical integration are the salient features of the device.

As such, new ways to extend the data rates, simplify the structural configurations in order to improve the noise performance and potential for integration of present-day devices are constantly pursued. On the basis of above said issues the comprehensive literature review and gaps in present study are described in following Sections.

2.2 Literature Survey

2.2.1 All Optical Logic Gates

Various approaches have been proposed in the literature to implement different types of logic gates employing nonlinear properties of SOA. These nonlinear properties include

XGM, FWM, XPM and cross-absorption modulation in a semiconductor optical amplifier. A combination of these properties has also been utilized.

Kristian E. Stubkjaer reviewed the progress of logic gates. He reviewed the progress from simple logic gates utilizing XGM and FWM to the integrated interferometric gates using XPM effect [9].

Logic functions can be realized based on FWM in SOA. This is achieved by encoding information on the polarization of the input signals. By utilizing non return to zero PolSK signals, reconfigurable logic operations such as XNOR, XOR, NOR, AND can be obtained using four wave mixing effect at 10Gb/s. Zhihong Li et al. [33] demonstrated different logic operations including XNOR, XOR, NOR, AND utilizng 10Gb/s NRZ PolSK signals. In order to generate four wave mixing signals, input signals are combined in parallel or perpendicular before applying to the SOA. Pattern dependent degradation has been shown to be reduced as a result of constant intensity feature of the signal. Different logic functions were able to be generated by adjusting the polarization controllers at the input and output.

The SOA-MZI can perform different types of optical logic functions with high extinction ratio at the output. This device needs low switching energy for operation and have compactness and regenerative capability. Reis C et al. [34] experimentally demonstrated all optical XOR gates using SOA-MZI at 10 Gbit/s. NRZ modulated signals are used as input signals with co and counter propagation schemes. The extinction ratio showed high operation performance with low degradation.

Ali Rostami et al. [35] analyzed performance of an ultrafast all optical logic gate utilizing a quantum dot semiconductor optical amplifier. XGM effect is used for acceleration of the gain recovery process with the help of a control pulse. An optical XOR gate with a proper quality factor is demonstrated employing a Mach–Zehnder interferometer based structure at Tb/s operational speeds.

L. Li et al. demonstrated an all-optical reconfigurable logic gate utilizing FWM effect in a HNLF at 10 Gb/s. It utilized NRZ-PolSK signals. The input power to the highly nonlinear fiber is optimized to be as low as about 15.2 dBm. High Q factors above 8 dB are achieved for eye diagrams [36].

S.K.Garai et al. proposed a technique for optical realization of different logic operations based on frequency encoding method. Difference frequency generation and second harmonic methods are used in a nonlinear material [37].

Table 2.1: Optical Logic Gates using different nonlinear effects.

Author, Year	**Nonlinear Effect Used**	**Based On / Using**	**Speed**	**Advantages/ Issues**
Li et al. [2006] [33]	FWM in SOA	Based on polarization encoded signals	10 Gb/s	Pattern dependent degradations are reduced due to the constant intensity feature of the signal
Reis et al. [2009] [34]	XPM in SOA	XOR gate based on SOA-MZI	10 Gb/s	High ER (more than 10 dB for Counter propagation shceme), compact, requires low switching energies, have regenerative capability
Rostami et al. [2010] [35]	XGM and XPM in SOA	Based on QD-SOA with acceleration of the gain recovery process using a control pulse	2 Tb/s	With QD-SOA, negligible pattern effect, suitable for ultra-high-speed applications, Q factor - at 2.5 Tbps, Q:4.9, at 2 Tbps, Q: 8.8
Li et al. [2010] [36]	FWM in a HNLF	Using NRZ-PolSK Signals	10 Gb/s	The input power is optimized to be as low as about 15.2 dBm and high Q factor above 8 dB is achieved
Garai et al. [2010] [37]	Non-linear response / character of materials	Utilizing second harmonic and difference frequency generation methods	---	Problems related to Intensity loss dependence are negligible, The scheme is temperature and polarization sensitive due to the use of PPLN wave guide.
Singh et al. [2012][38]	XPM in SOA	Based on SOA-MZI	40 Gb/s and 120 Gb/s	The quality factor measured from the eye diagrams of proposed logic gates is more than 15 dB.

S. Singh et al. proposed all optical logic gates including AND, OR, XOR, and XNOR at ultrahigh speed by using SOA-MZI configuration. The simulations of optical logic gates are carried out at 40 and 120 Gb/s. Eye diagrams of proposed logic gates indicate a quality of more than 15 dB [38].

There have been many other approaches for realizing optical logic [39], [40]. These include implementations based on single-mode Fabry-Perot laser diode or FWM effect in highly nonlinear fiber. For better clarity optical logic gates implementations based on different nonlinear effects has been briefly described in Table 2.1.

2.2.2 All Optical Flip Flops

The interest in optical flip flop is decades old. Sengupta et al. [41] demonstrated a flip–flop in 1978. The flip flop was optically controlled and used liquid crystal spatial light modulators (SLMs).

Optical flip flops are the key components for applications like all optical packet switching [42]. These devices could be potential basics for certain optical digital computers, Requirements and issues have been different. Programmable optoelectronic types of flip-flops were developed. These were not fast but were able to provide greater flexibility. Flip–flop energy, orthogonal optical outputs, independence of the output wavelength, high-frequency operation and long term stability considerations are some of the aspects investigated in the past.

Later (from 2005), SOA-based [43]--[45] implementations have been playing a main role. SOA has been used extensively in different types of configurations such as ultrafast nonlinear interferometer, symmetric Mach Zehnder interferometer, and terahertz optical asymmetric de multiplexer (TOAD) [35]. Mach–Zehnder interferometers (MZIs) dominate these systems. Thereafter some emphasis was put on creation of very small devices. Waveguide based photonic integrated circuits [46] and ultra-small photonic crystal based optical circuits [47] are some of the examples. Some isolated works were reported thereafter. These are based on utilizing bistability of an injection locked Fabry–Perot laser diode [48], electric field nonlinearity of coherent laser amplifiers [49], and using nonlinear materials in the form of a switch. This enthusiasm continued with recent developments of fiber-based bi stable device [50], ring lasers [51], plasma photonic crystals [52].

A. K. Datta et al. [53] presented a novel schematic for implementing the flip-flop operation with an optical architecture which is hybrid and uses a single LCD panel. The

previous state is taken as the third input for the system. All the three inputs are superimposed and spatially coded. Operations of J–K, T, S–R and D flip-flops are decided by the modes of switching of the light sources in the array in a single architecture.

H. J. S. Dorren et al. [54] demonstrated an asynchronous optical flip flop solution. The flip flop utilized coupled ring lasers which offered a number of features. It was able to exhibit high value of contrast ratios between two states. Set and reset operations are symmetric. This occurs as there is no difference in the method of switching from one state to other and vice versa. A controllable switching threshold and large input light wavelength range are important features of this flip flop.

A. Malacarne et al. [50] presented all-optical flip-flops exploiting erbium-doped fiber properties. The implementation suffered from high set and reset powers at the input and slow switching times.

M. T. Hill et al. [55] proposed an integrated scheme. The scheme exhibited a very high contrast ratio. Transition times in the nanosecond range were reported. Thus for different flip-flop applications a tradeoff exists between edges speed and contrast ratio of the flip-flop.

A. Malacarne et al. [56] analyzed the above mentioned scheme [54] for investigating its drawbacks and finding out one of the possible solution to overcome its limitations. They experimentally measured transition times as 20ps with a contrast ratio 17.5dB. This scheme actually exploited two flip flops. Both the flip flops are based on two coupled semiconductor optical amplifier based ring lasers and two NOT logic gates. NOT gates exploit XGM and cross polarization rotation in a single SOA.

Among the various types of reported schemes of flip flop implementations, MZI configuration using SOAs is promising because of the low power operation and small-size of the device.

S. Shimizu and H. Uenohara [57] investigated an all optical T type flip-flop utilizing SOA for differential phase shift keying (DPSK) encoding. Their result revealed that the stable operation is possible at 10Gbps.

2.2.3 All optical binary counter

A small number of optical bit counters have been reported in the literature. These devices mainly rely on analogue time of flight designs with a limited potential for integration [58], [59]. In [58] an optical counter circuit using directional coupler switches, which are

polarization dependent was demonstrated. Optoelectronic conversion was required in this counter. In [59] a TOAD based switching is used to implement an all optical binary counter. This configuration requires an external clock signal and provides a serial output.
A true digital optical counter has been presented at speeds up to 120 kHz. It employs set reset optical flip flops utilizing coupled semiconductor optical amplifier based ring lasers [10]. In this proposed scheme, SR flip flops are utilized to perform latching functionality. These are assisted by auxiliary signals, which are generated by two AND gates in a feedback configuration. SR, D, T, and JK types of flip-flops, and an all-optical binary counter are implemented by adding one of the logic gates, or a combination of them, to the latch. The proposed counter provides a parallel output. The rise time and fall time are ≈1 μs and about 5ns respectively. As the scheme is SOA based, so high energy efficiency is possible with photonic integration. By cascading N number of counter stages, N-bit counting can be demonstrated counting from 0 to $2N$–1. The cascadability in this scheme is limited by the degradation of carry signals, and by the pedestal due to the amplified spontaneous emission noise generated by the SOAs.
In 2010 Aaron M .Kaplan et. al. [60] described generation of optical square-wave clock using an all-optical flip flop. This is achieved by switching on and switching off the bistable output power from a resonant type of SOA. Input of the SOA is modulated with its output via XGM effect in a traveling wave SOA**.** Frequency of the clock signal generated is 3.5 MHz and is limited by the time of flight between bulk optical components. Wavelength and clock frequency are selectable. Optical clocks thus generated may be used for providing timing and control signals in photonic integrated circuits. Table 2.2 briefly describes the specifications and issues involved with the major implementations of all optical binary counters.

2.2.4 Optical shift register

Optical shift registers find applications in optical packet buffers, serial-to-parallel converters and synchronizers [61], [62], [63]. They might also become essential building blocks for more complex subsystems. These devices have received considerable attention as they can play a significant role in signal processing techniques. Other applications include cyclic operations such as cyclic redundancy checks and parity that enable digital correction and detection of transmission errors.

Table 2.2: Progress of all optical Counters.

Author, Year	**Based On / Using**	**Specifications**	**Issues**
Feuerstein et al. [1991] [58]	Directional coupler switches and single-mode fibers	Speed: 100 MHz Integrable : Analogue time of flight design thus limited potential for integration	Optical to electrical conversion is required in the coupler switches
Poustie et al. [2000] [59]	TOAD	Speed : 3.4 MHz Integrable : No	Serial output is provided by this configuration, an external clock signal is required
Wang et al. [2010] [10]	SR latches and logic gates based on coupled Ring lasers using SOAs as active elements**.**	Speed: 40 - 120 kHz Integrable : yes Q:16.1,19.9 (depending upon the efficiency of the two latches) Switching energy: f j range (possible With integrated version)	Carry signals degradation limits the cascadability of the device, Additional combinatorial circuitry is needed for generation of auxiliary signals
A. M. Kaplan et. al. [2010] [60]	An optical flip flop employing a resonant type SOA	Speed: 3.5 MHz Wavelength as well as clock frequency can be selected	Clock frequency is limited by time of flight between bulk optical components

In most of the cases, shift registers are implemented using coupled flip flops. There has been a lack of stable all optical flip–flops which are easier to cascade. Therefore optical shift registers have been realized using alternative ways. Fiber Sagnac interferometer was used for demonstrating original recirculating shift register at 100MHz [61]. This configuration provided ultrafast operation. It was bulky and required high switching energies to operate due to the long fiber interaction lengths. Thereafter, recirculating shift registers were demonstrated with various semiconductor optical amplifier based schemes. One example is by using the ultrafast nonlinear interferometer (UNI) [64]. Other such

Table 2.3: Progress of all optical Shift Registers.

Author, Year	**Based On / Using**	**Features / Issues**
Whitaker et al. [1991][61]	Fiber Sagnac interferometer	Speed: 100 MHz Integrable : No Bulky configuration, high switching energy is required due to the long fiber interaction lengths.
Hall et al. [1997] [64]	Ultrafast nonlinear interferometer (UNI)	Speed: 40 Gb/s Integrable : Yes Requires low switching energy
Lee et al. [1999] [65]	SPM in SOA	Integrable : yes polarization independent operation, requires low switching energy
Xie et al. [2000] [66]	Fiber loop buffer, EDFA to amplify and feedback the output	Integrable : No Integration is inhibited by large physical size of the shift register, propagation time of the order of milliseconds
Manning et al. [2001] [67]	UNI, SOAs for switching and feedback	Speed: 40 GHz Time-of-flight of the switch is minimized, provide sufficient switching energy
Houbavlis et al. [2003] [68]	SOA-assisted Sagnac switch, SOA feedback	Speed: 10 GHz Time-of-flight of the switch is minimized, provide sufficient switching energy
Jhon et al. [2006] [69]	SOAs	Speed: 1 Gb/s Two SOAs are needed for a single stage, to obtain three-bit circular shifting, three stages (6 SOAs) are required
Zhang et al. [2005] [70]	Optical flip–flop memory (with active element as SOA) placed in series	Speed: 20KHz Switching speed of the flip-flop memory limits the operation speed , which is proportional to its cavity length
Lazzeri et al. [2011] [71]	Ring Buffer based on SOA and a BSC based on fiber Kerr nonlinearities	Input sequence bit rate : 236MHz Long fibers and hence high optical powers are necessary, amplification is needed before applying the buffer output to the BSC

scheme exploits semiconductor optical amplifier's XPM effect to achieve polarization independent operation [65]. This gives the device attractive features of low switching energy and integrability. The mentioned schemes store a sequence by alternating the circulation of the original and inverted version of the same signal in a loop. Fiber loop based optical buffers employing semiconductor optical amplifiers have been also proposed. Performance of these devices is optimized in terms of critical parameters of the SOAs' [66]. In these configurations, an EDFA amplifies the output signal, which is then fed back as the switching (control signal). Length of erbium doped fiber amplifiers may be many meters, resulting in two inevitable practical consequences. First is the large physical size of the shift register, which inhibits integration. Second is propagation times, which are of the order of milliseconds creating high latency. This is not desired in all optical feedback applications as the output signal will have a very large period and cannot be detected easily by the available electronic diagnostic instruments.

In order to avoid these problems feedback EDFA may be replaced by a SOA. This provides sufficient switching energy and minimizes the time of flight of the switch due to its large amplification capability and compact size.

This approach has been adopted in UNI and SOA-assisted Sagnac switch in [67] and [68], respectively.

In [69] Jhon et al. 2006, a circular shift register was presented utilizing three semiconductor optical amplifierss. Three bit shifting operation was carried out. This is achieved without considerably distorting the input sequence. Another solution comprising of two serial connected semiconductor optical amplifier based optical flip–flop memories has also been proposed. This configuration demonstrated two bit shifting [70]. For better clarity the progress of all optical shift registers in terms of speed, integrabilty and other design issues has been briefly described in Table 2.3.

2.2.5 All Optical Arithmetic and Logical Circuits

Optical logic functions may be implemented by employing nonlinear effects either in optical fiber or in SOA. Many approaches have been proposed based on these effects.

These include an ultra-fast nonlinear interferometers (UNIs), cross gain modulation and cross polarization rotation in a single semiconductor optical amplifier, SOA- assisted OBF, one level simplification method, SOA-based MZI and terahertz optical asymmetric demultiplexer (TOAD) [72], [73]. Considering various topologies, monolithically integrated Mach–Zehnder interferometer based switches represent one of the most

promising solutions due to their large potential for integration with different types of active and passive components, thermal stability, compact size, high operational speed and low power. Out of various configurations of MZI, the symmetric structure of the device provides shortest switching window and highest flexibility. SOA-based MZI switches can be used for successful implementation of various types of logical functions [20].

Optical interconnection systems are the primitives in digital optical computing. These systems constitute various optical architectures and algorithms. In this regard optical tree architecture also has an important role. OTA can be successfully designed using semiconductor optical amplifier based MZI switching system. Single architecture can be utilized for different purposes. This scheme can be easily extended. It can be implemented for any higher number of input digits. This is possible by proper arrangements of Mach–Zehnder interferometer based optical switches, by suitable branch selection and by horizontal and vertical extension of the tree [74].

J.N.Roy and D.K.Gayen [75], [76] proposed TOAD based tree architecture for realizing all-optical arithmetic unit and all-optical arithmetic and logic operations.

Dilip Kumar Gyan et al. [73] described TOAD based all optical BCD adder. Bit error rate, Contrast ratio, Extinction ratio and Amplitude modulation are reported to be 10^{-15} , 38.06 dB, 30.23 dB and 2.36 dB respectively.

J.N.Roy et.al [74] exploited the advantages of semiconductor optical amplifier based MZI switches and optical tree architecture by proposing SOA-MZI based OTA. This architecture is a new and alternative scheme for integrated all optical parallel arithmetic and logic operations.

According to Young. jin. jung et.al [72] a one level simplification method can be utilized for realization of all optical combinational logic circuits with resulting improvement in Q-factor. A one level method minimizes the accumulation of signal degradation. It also provides a systematic method for construction of higher level combinational optical logic circuits.

Micro. Scaffardi et al. [32] proposed a full adder and optical comparator. It is implemented by cascading a unique basic gate that exploits cross gain modulation and cross polarization rotation in a single semiconductor optical amplifier.

Abdallah k.Cherri et al. [77] utilized the powerful and attractive parallelism property of the modified signed digit number representation. Ultra fast all-optical switching property of the semiconductor optical amplifier based MZI is used for designing and

implementation of all-optical MSD adder/ subtracted circuits. As compared to the binary adder, modified signed digit adder optical circuits may be extended to n number of digits by including more stages without affecting the total time of addition.

A.S. Al-Zayed et al. [78] generated an improved version of all optical MSD adders [77] using SOA-MZI. It is more efficient as far as number of optical components and operational speed is concerned. A 50% reduction in the unit size and at least 50% increase in execution time are achieved. The proposed adders require lesser semiconductor optical amplifier based MZI switches, wavelength converters and optical amplifiers.

2.3 Gaps in Present Study

Optical logic gates with higher speeds are the main elements of the future generation optical networks as well as the computing systems. Depending on the transfer function of these gates, inverted or in-phase output signals are obtained. Modules are needed that are simple, polarization independent, reconfigurable and integrable. Moreover they should be able to work at low optical power levels. They should also be easily adjustable to the transmission protocol and system bit rate.

Computing machines with high performance are just entering the exaflop era. A balanced approach of system design needs similar advances in all its functional subsystems. Electronic RAM devices still suffer from long access times and limited bandwidth, thus imposing a major restriction in further enhancement of processing capabilities. In order to bridge the gap between memory and processor speeds, ultra fast optical memory based elements and latching devices should be developed. Such devices must be capable of performing switching and buffering functions in the optical domain at unprecedented data rates.

All optical binary counters can be used in header recognition, payload processing and as a finite state machine in optical computing and packet switching networks.

Minimizing the number of components required for implementing these devices reduces the complexity and power consumption requirements. Optical shift registers find applications in serial-to-parallel converters, optical packet buffers and synchronizers. They can be a basic building block for other applications such as optical memory and clock division. Enhancing the speed of operation and potential of integration, and minimizing the number of components required for their implementation are the major issues for these all optical devices.

SOA-based implementations have great potential in terms of small footprint, high speed, low power consumption and optical integration. SOA-MZI represents one of the most promising solutions for implementing all optical arithmetic and logical circuits.

In order to achieve these objectives, it is of utmost importance to propose and investigate all optical digital devices which provide better performance, can operate at high data rates, have simple structure and potential for integration in order to be used for future all optical networks. Based on the above discussion the gaps in present study are summarized as following:

1. Modules of all optical logic gates are needed that are simple, polarization independent, reconfigurable and integrable. Moreover they should be able to operate at low optical power levels and be easily adjustable to the system bit rate and transmission protocol.
2. Realization of different types of all optical flip flops using a single architecture is not readily available.
3. All optical circular shift register is yet to be investigated for different number of bit storage and Gb/s operational speed.
4. There is need to investigate all optical binary counter requiring minimum number of active components and operating at higher operational speeds (5 GHz).
5. Potential of SOA-MZI for realization of all optical arithmetic and logical circuits is an open area of research.

2.4 Objectives

Based on the initial studies, literature survey (as reported) and the understanding established the following objectives are proposed:

1. To realize all optical logic Gates based on nonlinear properties of SOA.
2. To investigate SOA-based SR Latches and flip flops as binary counters and registers.
3. To investigate and analyze SOA based all optical arithmetic and logical circuits such as Adder, Subtractor, Comparator, Demultiplexer, Decoder etc.

2.5 Basic Contribution of Thesis

A simple and new scheme is proposed for all-optical SR and D flip-flop employing XGM effect in two wideband semiconductor optical amplifiers. The proposed flip-flop has a fast response and its simple structure implies reduced footprint and low power consumption that makes it suitable for photonic integration. An optical gate architecture

is proposed to perform AND, OR and NOT logic gates using a single SOA. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates. Simple structure and potential for integration makes this architecture an interesting approach in photonic computing.

Another innovative result presented in this thesis is the investigation of a new and potentially integrable scheme to realize an all optical circulating shift register consisting of an optical AND as a bit selecting circuit. The operation of the shift register has been verified for a 10-bit input sequence at a sequence bit rate of 2.5 GHz and 10 GHz respectively. Further, we propose a digital two bit optical counter. The proposed counter has highest operational speed and lowest number of active components among the truly digital optical bit counting devices reported so far.

Finally we demonstrate the logic functions of integrated addition-subtraction, all optical decoder, data comparator and demultiplexing based on SOA-MZI based OTA. In general terms this thesis investigates all optical arithmetic logic devices from an application perspective. Specifically, the research performed in this thesis can be summarized as:

- Realization of simple, reconfigurable and polarization independent all-optical logic operations using single SOA at 40Gb/s.
- Implementation of all optical SR and D flip-flop employing XGM effect in semiconductor optical amplifiers.
- Investigation of all optical shift register and binary counter while acknowledging the limitations of existing devices.
- Realization of all optical arithmetic and logical circuits based on SOA-MZI based optical tree architecture (OTA)
- Use of SOA-MZI as a demultiplexing switch in demultiplexing of optical time division multiplxing channel at data rates up to 160 Gb/s.

2.6 Organization of Thesis

The thesis has been organized into six chapters. The content of each chapter is briefly described below.

Chapter 1 introduces the overview of optical amplifiers and fundamental concept of the operating principle of SOA. The different nonlinear effects that make SOA a very interesting device for applications in optical networks and different types of architectures to implement logic gates are also discussed.

Chapter 2 contains a comprehensive literature review of the concerned field. It also demonstrates the gaps in the literature survey and the objectives of research.

Chapter 3 deals with the first objective of the thesis which is to realize all optical logic Gates based on nonlinear properties of SOA. An optical gate architecture is proposed to perform AND, OR and NOT logic gates using a single SOA. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates.

Chapter 4 is based on the second objective of the thesis which is to investigate SOA-based SR Latches and flip flops as binary counters and registers. First, we propose a simple and new scheme for all-optical SR and D flip-flop employing XGM effect in two wideband semiconductor optical amplifiers. Flip-flop operation has been verified for several complementary and non complementary set-reset pulse signals confirming successful operation at 10Gbp/s. Secondly, the operation of circulating shift register is investigated for a 10-bit input sequence at the sequence bit rate f_b = 2.5 GHz and f_b = 10 GHz respectively. The dependence of the output *Q*-factor on SOA parameters is also investigated and discussed. Finally, we propose an all optical two bit binary counter. The counter uses two stages of optical TFF and an optical NOT Gate.

Chapter 5 pertains the study and realization of arithmetic and logical circuits which is related to the third objective of this thesis. The all-optical realizations of adder, subtractor, comparator, demultiplexer, decoder etc are based on SOA-MZI. Numerical Simulations confirming the described logic devices have been presented for different input combinations. Further, SOA-MZI based all optical demultiplexer operation has been analyzed in demultiplexing of an optical time division multiplexing channel at data rates up to 160 Gb/s.

Finally, chapter 6 covers the conclusions and recommendations on the basis of results obtained in chapters three to five.

Chapter 3

Realization of All optical Logic Gates based on Nonlinear Properties of SOA

3.1 Introduction

If the node functionalities are to be implemented using electronics, it will result in the bottleneck toward flexible and broadband optical networks. Optoelectronic conversions should be avoided in high capacity core networks. All-optical processing is mainly important in such type of networks. All optical processing is required in add–drop as well as cross–connect functions. Examples of some applications are clock recovery, add–drop multiplexing, wavelength conversion, simple bit-pattern recognition and regeneration. Logic gates capable of operating in the optical domain are being studied for many years because of the prospects of eliminating optical- electronic- optical conversions. These devices enable all-optical networks with above mentioned applications.

In this chapter, the first research objective, i.e. to realize all optical logic functions utilizing nonlinear properties of SOA, has been investigated.

In this work, an optical gate architecture is proposed to perform AND, OR and NOT logic functions using a single SOA. The all optical logic gates are implemented by FWM, cross gain modulation and XPM nonlinear effects in a semiconductor optical amplifier. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates. Simple structure and potential for integration makes the proposed architecture an interesting approach in optical signal processing and photonic computing.

3.2 Optical Logic Gates based on Semiconductor Optical Amplifier

All-optical logic functions are crucial elements in ultra-fast applications employing optical signal processing. Reconfigurable logic gates are mainly preferred as they are able to provide more flexible set of network functions. These functions include all-optical header recognition, label swapping, parity checking, binary addition, data encryption, time demultiplexing and routing functions [79].

There have been many approaches previously reported for realizing optical logic, see Section 2.2.1. Frequency encoding techniques using periodically poled lithium niobate

(PPLN) waveguides do not have any problems concerning intensity loss. However the use of periodically poled lithium niobate waveguides make these implementations polarization and temperature sensitive [37]. Proposals which are based on polarization based logic have certain disadvantages. The polarization state may change at the refracting and/or reflecting points along the propagation or transmission path length [36], [37]. As compared to the implementations utilizing optical fiber nonlinearity, the semiconductor optical amplifier based implementations demonstrate large potential as far as low power consumption, fast switching time, and optical integration is concerned [80]. Semiconductor optical amplifier is an attractive nonlinear device, but SOA based realizations using two or more devices arranged in the interferometric configurations need accurate control and stabilization schemes [81]. Logic gates employing FWM effect in semiconductor optical amplifiers suffer from polarization dependence and have low conversion efficiency [8]. In order to be competitive to their electronic counterparts, optical gates should operate at high bit rates. Operating speed of logic gates employing XGM and XPM is limited. This is due to the reason that semiconductor optical amplifier has intrinsic slow carrier recovery time. Higher operating speeds upto 40 Gb/s or even higher can be achieved with this device. This is possible with the help of using different interferometer structures or a continuous wave holding beam with high power. As a result of using these structures, the cost and complexity of the devices are increased. In this Section, an optical gate architecture is proposed to perform AND, OR and NOT logic functions using a single semiconductor optical amplifier. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed.

3.2.1 Principle of Operation

The all optical logic gates are implemented by FWM, XGM and XPM in semiconductor optical amplifier. Cross gain modulation is a non-linear effect that takes place in a semiconductor optical cavity for example SOA. This effect takes place when a high power input signal called Pump signal is injected into the semiconductor optical amplifier. This signal depletes maximum number of the carriers which are present in the active region of the device when it is amplified. If simultaneously a lower power signal for example Probe signal is injected into the SOA, it will suffer attenuation due to the absorption of the carriers. In four-wave mixing effect two or three waves, co-propagating in the nonlinear medium (SOA), interact with each other generating waves at new

frequencies as discussed in Section 1.3.2.3**.** The cross phase modulation results due to chirps and large phase variation in the semiconductor optical amplifier with the ultra short injection of the pulse.

When two modulated, optical RZ control signals, along with the probe signal which is a continuous wave, are applied to the semiconductor optical amplifier, rising and falling edges of the probe are shifted towards shorter and longer wavelengths respectively [7]. This occurs due to XGM and XPM effects in the SOA. These effects will result in the broadening of output optical spectrum of the probe signal as illustrated in Figure 3.1.

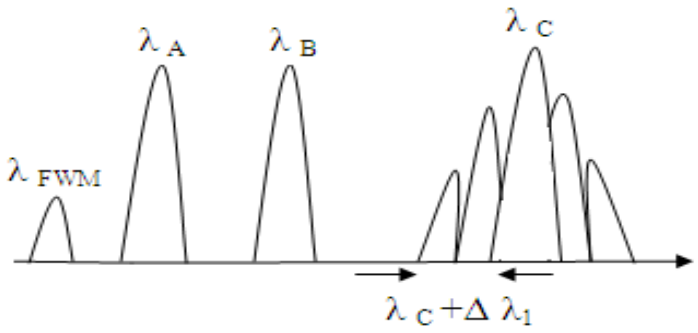


Figure 3.1: Conjugated light generated and broadened spectrum of the probe due to XGM, XPM and FWM respectively.

According to four wave mixing effect if f_1 is the frequency associated with the input signal and f_2 is the frequency of converted signal, the pump frequency is required to be chosen such that

$$\boldsymbol{f_p = (f_1 + f_2)/2} \qquad \textbf{3.1}$$

When two input data signals are applied to the semiconductor optical amplifier, the conjugated light is generated at the output as a result of four wave mixing effect as shown in Figure 3.1. This conjugated light generated is to be filtered out optically in order to generate AND logic. With the presence of data signals (*A* or *B)* or both, gain modulation of the probe signal takes place. This results in output which is polarity inverted, thus implementing a logic NOR operation. Thus NOR gate operation is obtained due to XGM in SOA. NOT gate operation can be obtained with the same filter detuning when only one data signal is present.

By shifting the optical bandpass filter's detuning by properly large value (i.e., $\lambda c + \Delta\lambda_1$), probe carrier may be rejected thus selecting the part of the spectrum which is shifted. Either data *A* or data *B* or both the data signals applied to the semiconductor optical amplifier will be inducing the shift in the spectrum. If both the data signals are absent,

there will not be any shifting of the spectrum. Thus the output will be logic OR gate. The truth table of the proposed logic gates is shown in Table 3.1.

Table 3.1: Truth Table for all optical Logic Gates.

data A	data B	AND	NOR	OR	NOT A
0	0	0	1	0	1
0	1	0	0	1	1
1	0	0	0	1	0
1	1	1	0	1	0

3.2.2 Numerical Simulation Setup

The system configuration is depicted in Figure 3.2. The wavelengths of two CW beams generated by Laser Diode1, Laser Diode2 are 1549.3 nm and 1550.7 nm respectively.

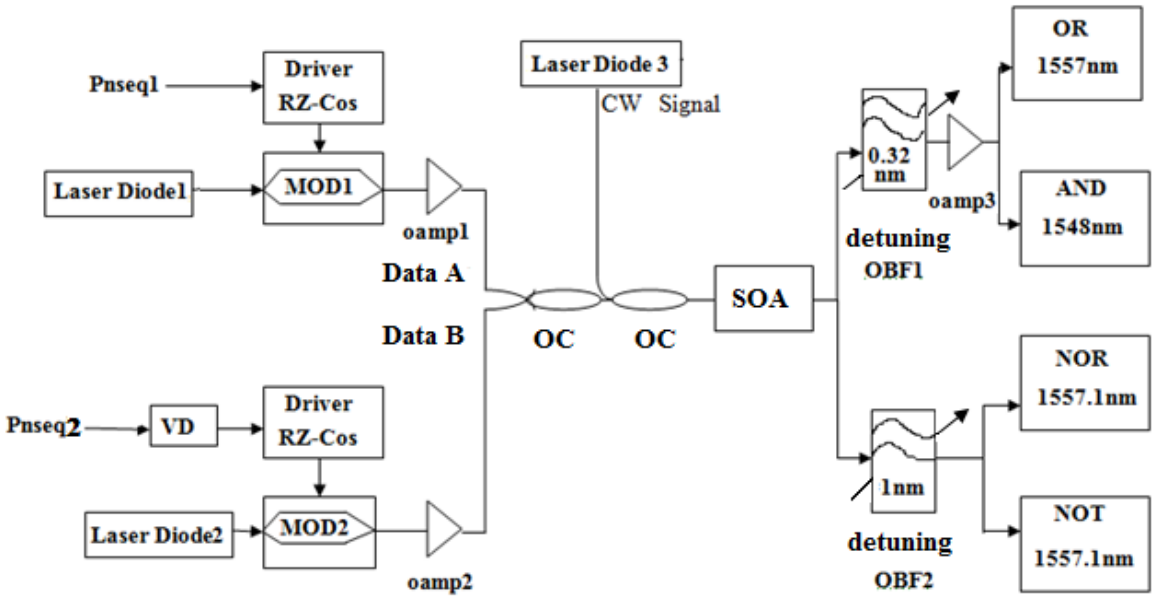


Figure 3.2: Schematic configuration of single SOA-based reconfigurable logic gates.

Lorentzian laser sources are used as Laser Diode1, Laser Diode2 with FWHM as10MHz and 10dBm power. Pnseq1 and pnseq2 generate PRBS with deterministic polynomial number 1 at high data rate. The data signals A and B are modulated at 40 Gb/s by two modulators to generate RZ pseudo random bit Sequence signals. These RZ pulses have

duty cycle of 33%. One of the data signal is delayed for several bits so that two data signals may be generated with different data patterns. Data signals A and B have the average power of 2dBm. Optical amplifiers oamp1 and oamp2 are used to amplify data signals.

Laser Diode 3 is generating the probe signal (CW) at 1557.3nm with full wave half maximum as 10MHz and 0dBm power. SOA is biased at 300mA with line width enhancement factor of 6. The standard travelling wave semiconductor optical amplifier is considered to be the amplifier model with relevant parameters as given in Table 3.2. A tunable gaussian narrow optical bandpass filter (OBF1) is used to filter the OR and AND logic. This filter has a bandwidth of 0.32 nm. For filtering out the probe signal with NOR/NOT output another gaussian tunable optical bandpass filter (OBF2) is used. This filter has a bandwidth of 1 nm.

In the system two optical bandpass filters having different bandwidths perform different functions. For achieving logic OR operation, the probe carrier is rejected using optical bandpass filter thus filtering out the sideband component. A narrow optical bandpass filter with 0.32 nm bandwidth is employed for this purpose as the frequency of the sideband is very close to the probe carrier frequency. The conjugated light signal frequency is close to the data signal frequency; thus an optical bandpass filters with narrow bandwidth is selected for the logic AND. For generation of logic NOT/NOR, OBF which is slightly detuned is required so that it should not suppress the probe carrier. Thus an ordinary optical bandpass filter with a bandwidth of 1 nm is used. Optical amplifier oamp3 is used to amplify AND output power.

3.2.3 Results and Discussion

The all optical logic functions are obtained by FWM, XGM and XPM in a SOA. Simulation for output wave form is performed using RZ modulated signals, at data rate 40 Gb/s utilizing the parameters of semiconductor optical amplifier (shown in Table 3.2). Through the proper adjustment of the power levels at the input and the centre wavelength of OBF, different logic functions are realized.

A. Logic OR

When two data signals which are modulated with optical return to zero (RZ) modulation format along with a continuous wave probe signal are applied to the SOA, as a result of XGM and XPM, the optical spectrum of the probe signal at the output becomes

broadened. A shifted spectrum is induced when either data signal *A* or data signal *B* or both the signals are applied to the SOA. In the absence of both the data signals, there will not be any shifted spectrum. OBF with properly large detuning select the shifted spectrum and rejects the probe carrier. Thus, logic OR gate is obtained at the output.

Table 3.2: SOA Parameters.

Parameters	**Value**
Bias Current	300mA
Amplifier Length	500µm
Active Layer Width	2µm
Active Layer thickness	0.15µm
Confinement Factor	0.35
Transparency carrier density	$1x10^{18}cm^{-3}$
Linewidth Enhancement Factor	$6cm^{-1}$
Material Loss	$10.5cm^{-1}$
Input/output insertion loss	3dB
Material gain constant	$3x10^{-16}cm^{2}$

Figure 3.3 (a) and (b) depict the input data signals *A* and *B* before applying to the SOA. Average of both the waveforms is 2.2 dBm. Power of the probe signal is 0 dBm. For achieving logic OR operation, a narrow (0.32nm) optical bandpass filter (OBF1) is used. OBF1 is detuned −0.3 nm from the probe carrier signal. The output signal depicts logic OR operation, although the noise in amplitude and pattern effects appear in the eye diagram [see Figure 3.3 (c)]. Optical bandpass filter (OBF1) has been detuned far from the probe carrier. As a result of this penalty, low power level output signal is obtained. Extinction ratio and contrast ratio measured for OR are 18.2dB and 17dB respectively.

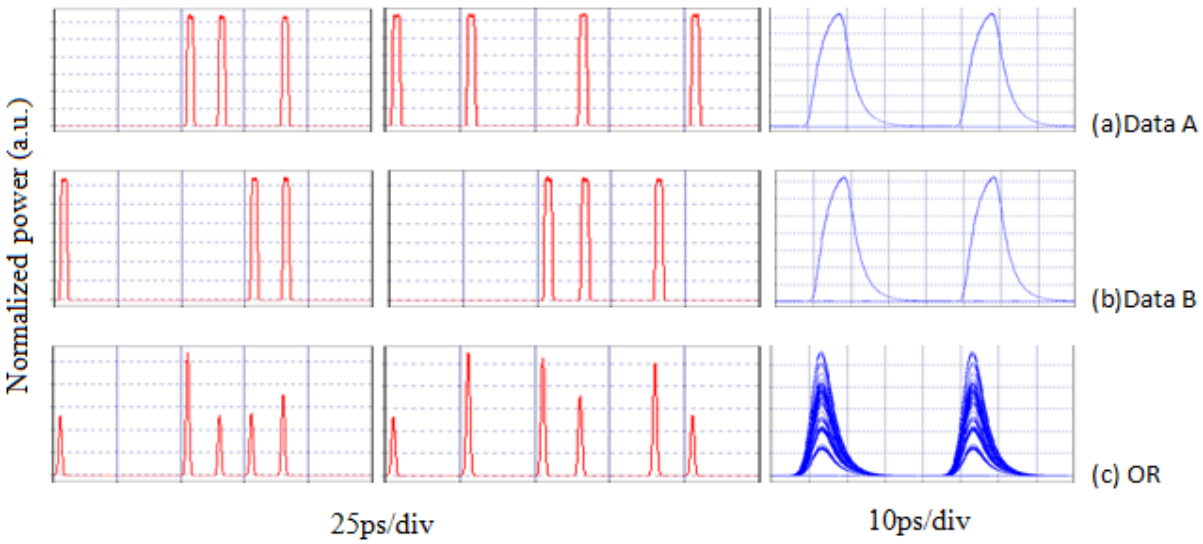


Figure 3.3: Output waveforms of OR logic gate (a) Data A (b) Data B (c) Logic OR.

B. Logic NOT

NOT gate operation is obtained due to XGM in SOA. When either data signal *A* or data signal *B* are present, the probe signal is gain-modulated. Thus a polarity-inverted output signal is obtained. This results in logic NOT output. For accelerating the recovery of the amplitude and removal of the pattern effects, OBF2 which is a slightly detuned to the probe carrier i.e -0.2nm is utilized. As cross gain modulation effect is limited with respect to the SOA gain recovery time so the outputs appear to be somewhat saturated in the case of NOT gate.

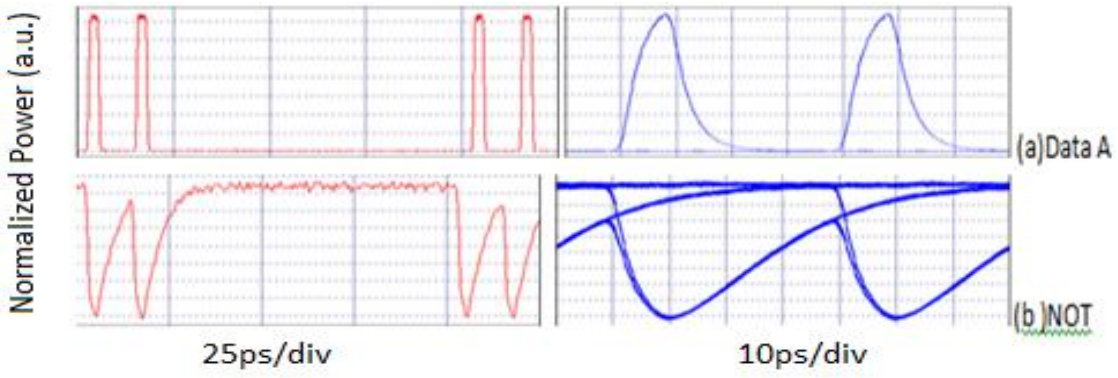
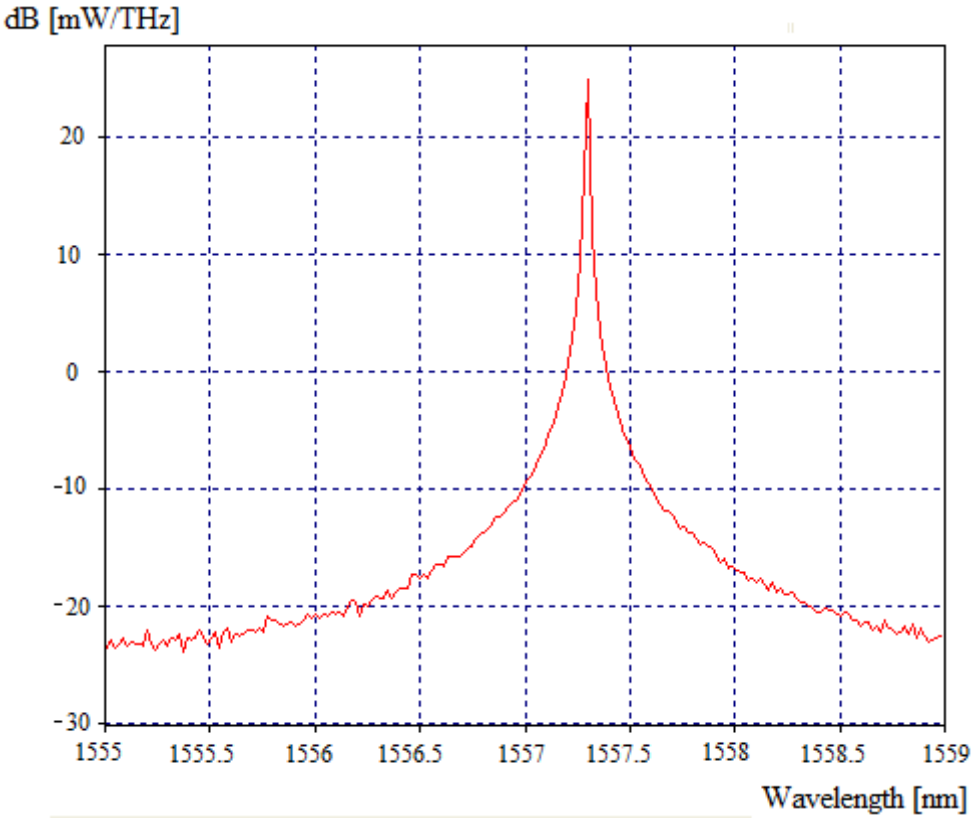
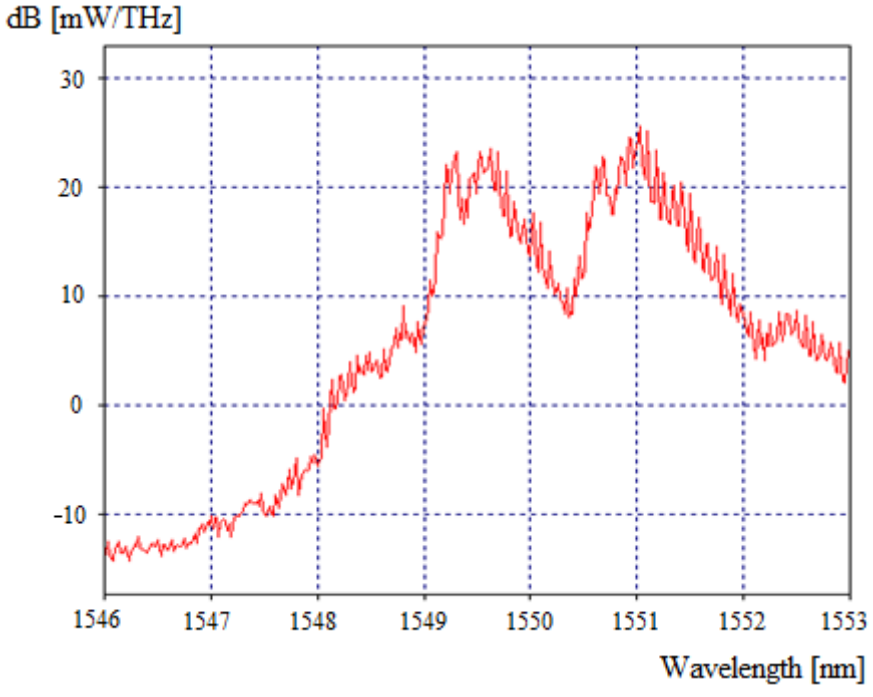


Figure 3.4: Output waveform of NOT logic gate (a) Input Data signal (b) Logic NOT.

Input signal waveform of data A with Laser Diode 2 turned off is shown in Figure 3.4 (a).Output waveform with good eye diagram can be seen in Figure 3.4 (b).



(a)



(b)

Figure 3.5: (a) Spectrum of the probe signal before SOA (b) SOA output.

C. Logic AND

The conjugated light is generated with the presence of both the data signals in the semiconductor optical amplifier. FWM effect results in the generation of the conjugated light, which is filtered out optically to realize AND logic operation. Optical spectrum of the continuous wave probe signal before applying to the semiconductor optical amplifier is depicted in Figure 3.5 (a). Figure 3.5 (b) shows the spectrum at SOA output. Conjugated light generated according to the four wave mixing effect at 1548 nm and is filtered out by OBF1.

The signal at the output of the AND logic gate has a low power level. It is therefore amplified by oamp3. This results because of the low conversion efficiency of four wave mixing effect. The output signal of AND logic with good eye diagram is depicted in Figure 3.6 for the two data inputs signals 3.6 (a) and 3.6 (b). Maximum extinction ratio and contrast ratio observed for AND logic are 19dB and 12dB respectively

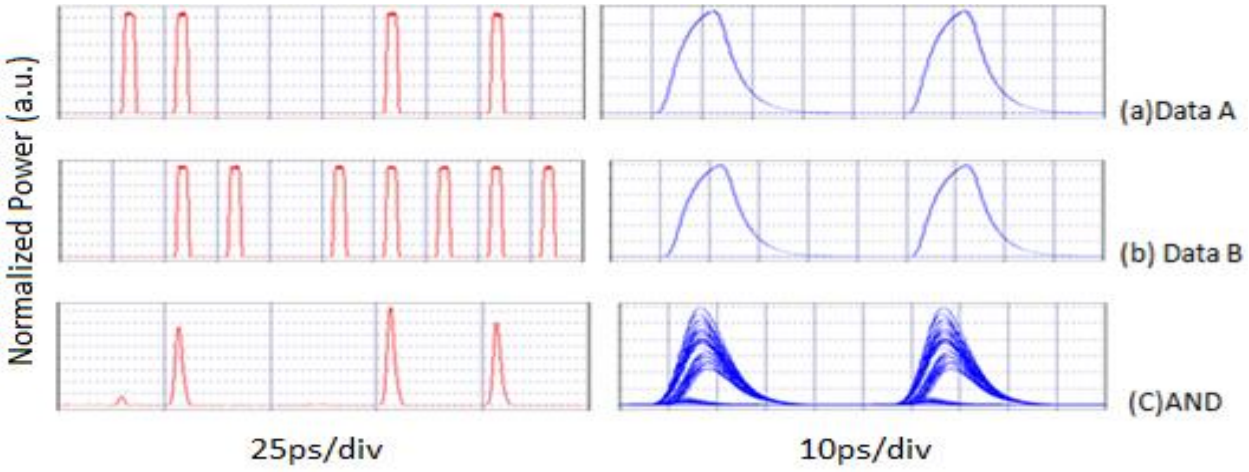
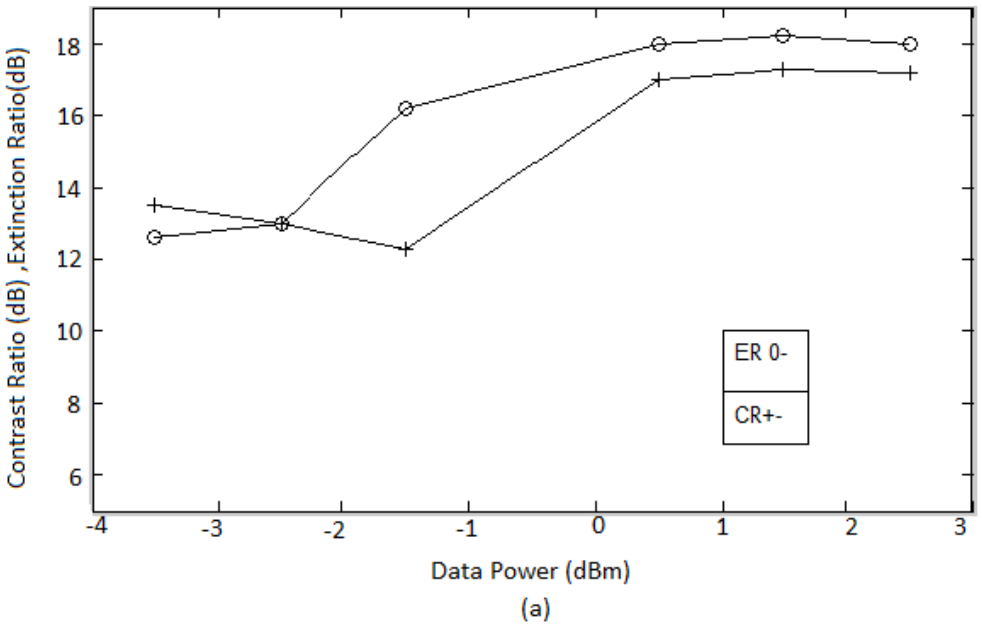
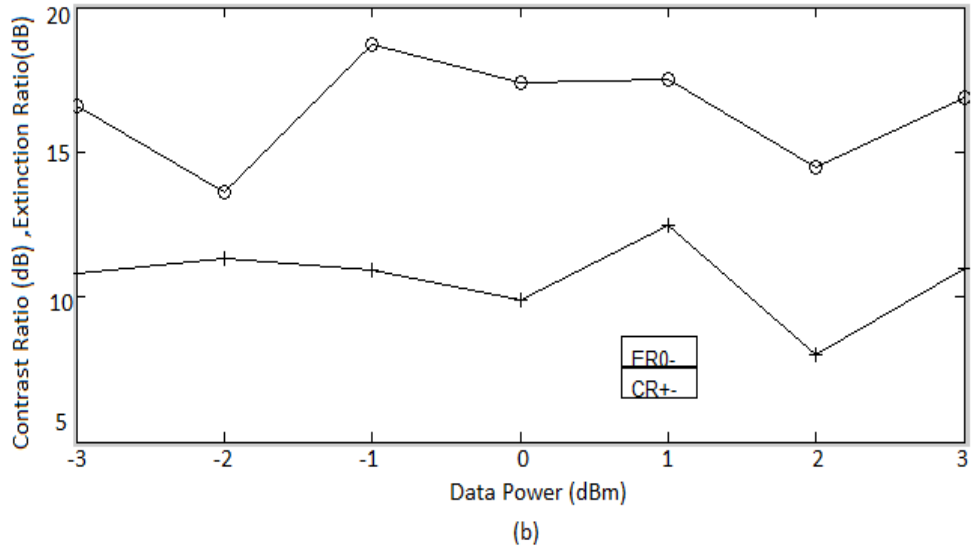


Figure 3.6: Output waveform of AND logic gate (a) Data A (b) Data B (c) Logic AND.

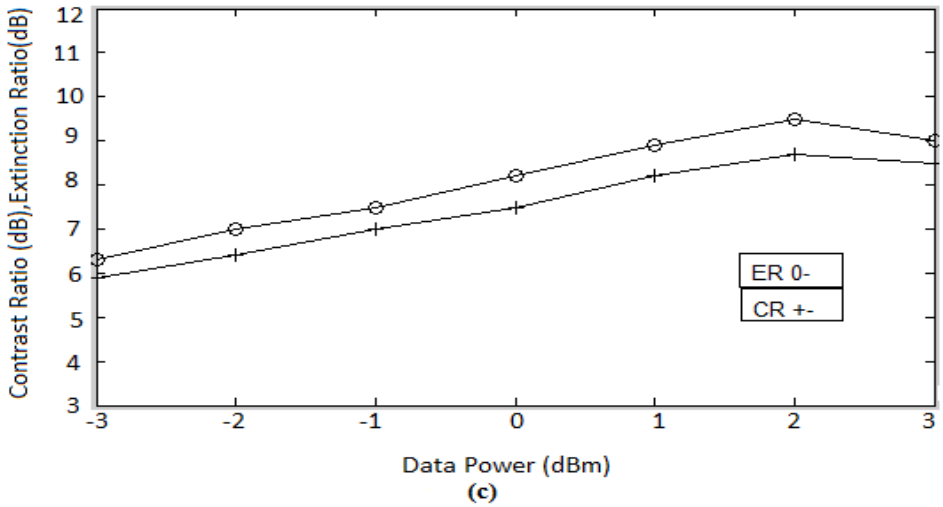
Output eye diagram of NOT gate is in the inverted return to zero format. This is also case with practical optical networks. Some small residual pulses are observed in the AND gate output where ideally they should not appear. By optimizing the filter transfer function, this could be improved. As a result of low conversion efficiency of the four wave mixing effect, the AND output has a low power level. The power level observed at the output of NOT gate is high. As NOT gate is based on XGM effect in SOA therefore observed extinction ratio is lesser as compared to those measured for the other gates [82].



(a)



(b)



(c)

Figure 3.7: Contrast ratio (C.R.) and Extinction ratio (E.R.) for different types of logic gates (a)-(c) Logic OR, AND and NOT respectively.

D. Performance Characteristics

Contrast ratio and extinction ratio is selected as the optimization criteria. For maximum gate performance, C.R. must be as high as possible. This will result in the largest fraction of input signal existing at the output. E.R. must be as high as possible. This is required so that the 'HIGH' (1) level can be distinguished from 'ZERO' (0). Figure 3.7 presents contrast ratio and extinction ratio variation with variation in the power levels of the input RZ data signals from -3 to +3 dBm, while at the same time maintaining the CW probe power 0 dBm. The graphs show that maximum E.R is obtained at input data power ~ 2.2dBm. Maximum extinction ratio obtained for OR, AND and NOT gates are 18.2dB, 19dB and 9.7dB respectively.

3.3 Conclusion

In this chapter, an optical gate architecture is proposed to perform AND, OR and NOT logic gates using a single semiconductor optical amplifier. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Numerical simulation confirming the described method are given in this chapter. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates. Maximum extinction ratio and contrast ratio achieved are 19dB and 17.2 dB respectively, which is more adequate for all optical logic based information processing. The proposed logic gates have a very simple structure and as they are based on the semiconductor technology allow for photonic integration.

Chapter 4

Investigation of SOA-based All optical Flip-Flops, Binary Counter and Register

4.1 Introduction

This Chapter deals with the second objective of this thesis work, which is to investigate SOA-based SR Latches and flip flops as binary counters and registers. This objective is achieved and presented in different Sections as follows: In Section 4.2, a simple and new scheme is proposed for all-optical SR and D flip-flop employing cross gain modulation effect in two wideband SOAs. Flip-flop operation has been verified for several non complementary and complementary set and reset pulse signals confirming successful operation at 10Gb/s. In Section 4.3 the operation of a circular optical shift register consisting of an optical AND gate and a fiber-loop based optical buffer is investigated for a 10-bit input sequence at the sequence bit rate f_b = 2.5 GHz and f_b = 10 GHz respectively. The OB is implemented using SOA as a nonlinear element. It is able to store a finite number of bits at a required bit rate. AND gate provides the consecutive bits at output at a lower clock rate. The dependence of the output quality factor (*Q*-factor) on SOA parameters is also investigated and discussed. Finally, a two bit optical binary counter is presented in Section 4.4. The optical counter consists of two stages of optical TFF and an optical NOT Gate.

4.2 All Optical SR and D Flip-Flop employing XGM effect in Semiconductor Optical Amplifiers

Several devices capable of exhibiting optical bistability and delivering switching and buffering functions have been reported so far. These devices were mainly based on two ring lasers which are coupled in a master–slave configuration [83] or utilizing the bistability between the lasing direction of a microdisk laser [84]. Other realizations utilize SOA-MZI [85] and semiconductor optical amplifiers used as frequency shifting threshold pairs [86]. In literature, various other methods are proposed, which are briefly described in Section 2.2.2.

Implementations of all-optical flip-flops utilizing erbium doped fiber properties [50] or discrete devices suffer from the requirement of high set and reset input powers and exhibit slow switching times. Several other solutions which are integrated or are

integrable [87], present small switching times (of the order of tens of ps) at the expenses of lower contrast ratios. In [55] an integrated scheme is reported with a contrast ratio which is high in value but with the transition times in ns range. Micro-resonators based bi-stable element [88] present high optical operating power, but with microsecond times of switching. All of above mentioned technologies for optical buffering utilize all-optical SR flip-flops. An all optical D-FF was demonstrated experimentally in [89]. This scheme required two coupled semiconductor optical amplifier based MZIs to achieve optical bistability. This increases the complexity of this scheme, making the scalability more difficult.

In this Section, a simple and new scheme is proposed for all optical SR and D flip-flop employing XGM effect in two wideband SOAs. Flip-flop operation is verified for several non complementary and complementary set and reset input pulse signals confirming successful operation at 10Gbp/s. Intra-FF coupling length and recovery time of the SOA are main factors in determining the speed-limit of the flip-flop. The simulation results exhibit a contrast ratio of 13 dB between two states with an AM of less than 2.5dB. The distinctive simplicity of the flip-flop results in reduced footprint and low power consumption thus making it suitable for photonic integration.

4.2.1 Operation Principle

Figure 4.1 depicts the system configuration of the proposed set-reset all optical flip-flop.

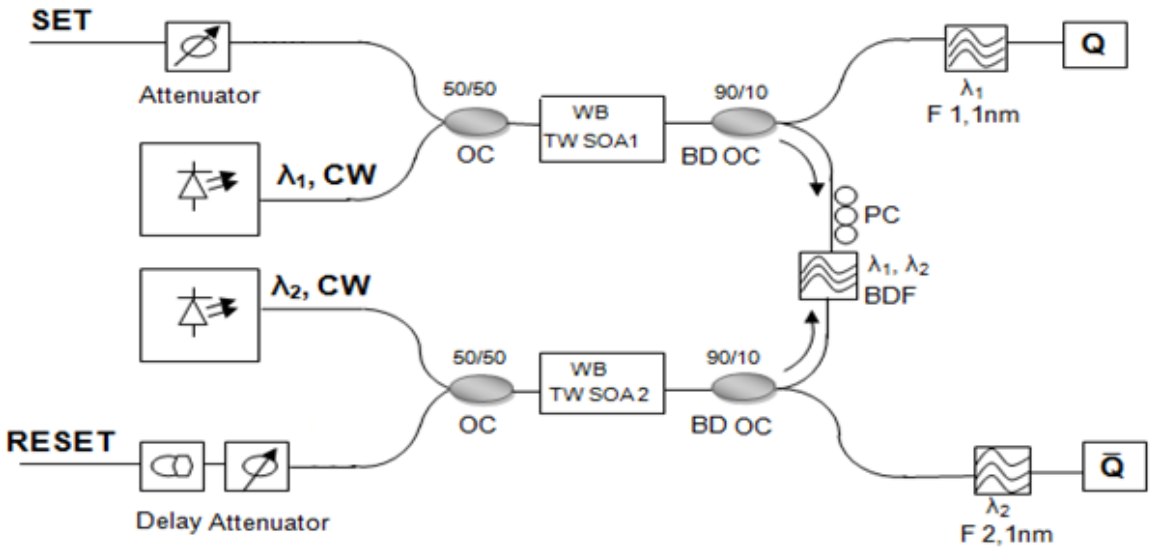


Figure 4.1: The schematic of proposed all-optical flip-flop.

The FF consists of two symmetrical arms. The right sides of these arms are coupled with the help of two 90/10 couplers. The other sides of the symmetrical arms are each coupled to two different branches through which external signals are introduced. Each SOA is powered at the left side through a 50/50 coupler by a weak CW input signal with FWHM as 10MHz at wavelength of 1550.3 nm (λ_2) and 1548.4 nm (λ_1) respectively. The other branches at the left side are used to input the Set and Reset input optical pulses. These pulses are the non return to zero (NRZ) modulated signals at a wavelength of 1555 nm (λ_3). The Set and Reset pulses are to be properly synchronized for generating equal propagation delays. An Optical Delay line has been used in the Reset branch for this purpose.

Gain recovery time may be shortened and the pattern effects may be restrained by adopting a long SOA. Two bidirectional and identical wideband travelling wave SOAs (SOA1 and SOA2) are chosen with 1600-μm length and less than 40ps recovery time. There are two bidirectional 90/10 couplers used at the coupled stage between the two semiconductor optical amplifiers. These couplers enable the free circulation of the semiconductor optical amplifier outputs at wavelengths of λ_1 and λ_2 respectively. Two outputs of the FF (Q and $\overline{Q}$) are also obtained through these couplers. A Bandpass Filter (BPF) centered at a wavelength of 1549.35 nm and with a bandwidth of 3-nm is interleaved between the two couplers. This is used for filtering out the amplified spontaneous emission noise and blocking the passage of Reset and Set pulses towards the upper and lower branch respectively. Two 1nm band pass filters (F1 and F2) are employed in the the Set and Reset branches to filter the Q and $\overline{Q}$ outputs at wavelengths λ_1 and λ_2 respectively. Polarization Controllers (PCs) are employed at different stages of the setup. These are used for adjustment of the polarization state and to compensate for any polarization dependencies of the SOAs. Power level of the signals may be adjusted by two variable optical attenuators (VOAs) employed in the setup.

The set-reset FF relies on the bistability between a slightly and a fully saturated condition of two wideband TW- SOAs. One of the SOA acts as master suppressing the other that acts as a slave. The role of slave and master can be interchanged due to symmetrical setup. A logical 1 indicates that SOA1 is dominant SOA and λ_1 signal is suppressing the output signal of SOA2. When SOA2 is dominating the set-reset flip-flop, a logical 0 state is achieved. Switching from one state to the other requires injection of proper reset or set pulses to the SOA that is dominating at that time.

When logical 1 level Set signal at wavelength λ_3 is applied to the SOA1 of logical 1 (dominating SOA), gain saturation of the SOA takes place. As a result of XGM effect, the transmission of continuous wave input signal at wavelength λ_1 is blocked. This results in gain recovery of SOA2 which will unblock the transmission of λ_2 continuous wave signal and switch the state of SR-FF to logical '0'. The high continuous wave signal at a wavelength λ_2, is now fed into SOA1. This will serve as the control signal which will suppress the gain of the SOA1 even after the end of the Set pulse. Due to this, SOA2 becomes master and it starts dominating over the SOA1. The flip-flop remains in this state. Now if a Reset pulse of wavelength λ_3 is fed into SOA2. It will saturate the gain of this SOA, thus unblocking the transmission of λ_1 continuous wave signal. Thus SR-FF will switch back to its initial logical 1 state.

4.2.2 Theoretical Analysis

The numerical evaluations are based on an experimentally validated wideband travelling wave SOA model [90]. The SOA model is based on the numerical solution of a set of coupled differential equations. These equations describe the interaction of the photon rates with carrier density. The traveling-wave equations for the signal fields are given as

$$\frac{dE_{sk}{}^{+}(\mathrm{z})}{dz} = \left(-j.\beta_k + \frac{1}{2}(\Gamma.g_m(v_k,\mathrm{n}) - \alpha(\mathrm{n}))\right).E_{sk}{}^{+}(\mathrm{z}) \tag{4.1}$$

$$\frac{dE_{sk}{}^{-}(\mathrm{z})}{dz} = \left(j.\beta_k - \frac{1}{2}\left(\Gamma.g_m(v_k,\mathrm{n}) - \alpha(\mathrm{n})\right)\right).E_{sk}{}^{-}(\mathrm{z}) \tag{4.2}$$

Where $E_{sk}{}^{-}$ and $E_{sk}{}^{+}$ are the complex traveling waves propagating in the negative and positive z direction respectively, α is the material loss coefficient, β_k is the propagation coefficient, Γ is the optical confinement factor, and $g_m(v_k,\mathrm{n})$ refers to the material gain coefficient.

Amount of spontaneously emitted noise from the amplifier also determines the signal amplification. Spontaneous emission may be expressed by the following travelling wave equations.

$$\frac{dN_j{}^{+}(\mathrm{z})}{dz} = (\Gamma.\mathrm{g}_m(v_j,\mathrm{n}) - \alpha(\mathrm{n})).N_j{}^{+}(\mathrm{z}) + R_{sp}(v_j,\mathrm{n}) \tag{4.3}$$

$$\frac{dN_j{}^{-}(\mathrm{z})}{dz} = -(\Gamma.\mathrm{g}_m(v_j,\mathrm{n}) - \alpha(\mathrm{n})).N_j{}^{-}(\mathrm{z}) + R_{sp}(v_j,\mathrm{n}) \tag{4.4}$$

Where N_j^- and N_j^+ represent the spontaneous emission rates of the photon traveling in the negative and positive z direction respectively. Emission noise coupled into N_j^+ and N_j^- is represented by R_{sp}.

The carrier density at z obeys the rate equation

$$\frac{d\mathrm{n(z)}}{dt} = \frac{I}{q.d.L.W} - R(\mathrm{n(z)}) - \frac{\Gamma}{d.W}.\left\{\sum_{k=1}^{N} \mathrm{g}_m(v_k, \mathrm{n(z)})\left(N_{sk}{}^+(\mathrm{z}) + N_{sk}{}^-(\mathrm{z})\right)\right\} - \left\{\sum_{j=1}^{\mathrm{N}_m-1} \mathrm{g}_m(v_j, \mathrm{n(z)}).\left(N_j{}^+(\mathrm{z}) + N_j{}^-(\mathrm{z})\right)\right\} \quad (4.5)$$

Where R is the recombination rate term, I the injected bias current, q the electronic charge, N_s the number of signals applied to the the SOA. $N_{sk}{}^+$ and $N_{sk}{}^-$ represent the photon rates of the waves in the corresponding direction respectively.

First, the amplifier is split into a number of sections and equations (4.1) to (4.5) are solved numerically by considering the steady state condition. The time domain representation of the carrier density rate then depends only upon bias level of the current and the input fluxes in all sections of the semiconductor optical amplifier.

The material gain coefficient is then described by.

$$\mathrm{g}_m = \frac{c^2}{4\sqrt{2}\,\pi^{3/2} n_a{}^2 \tau \nu^2}\left(\frac{2m_e\, m_{hh}}{\hbar(m_e + m_{hh})}\right)^{3/2} \times \sqrt{\nu - \frac{E_g}{h}}\,[f_c(\nu) - f_v(\nu)] \quad (4.6)$$

where n_a is the refractive index in the active region, c the speed of light in vacuum, τ the radiative recombination lifetime, $\hbar$ the Planck's constant divided by 2π, ν the optical frequency, E_g the bandgap energy, m_{hh} and m_e the valence band heavy hole and conduction band electron effective masses respectively and $f_v(\nu), f_c(\nu)$, the Fermi-Dirac distributions in the valence and conduction band respectively.

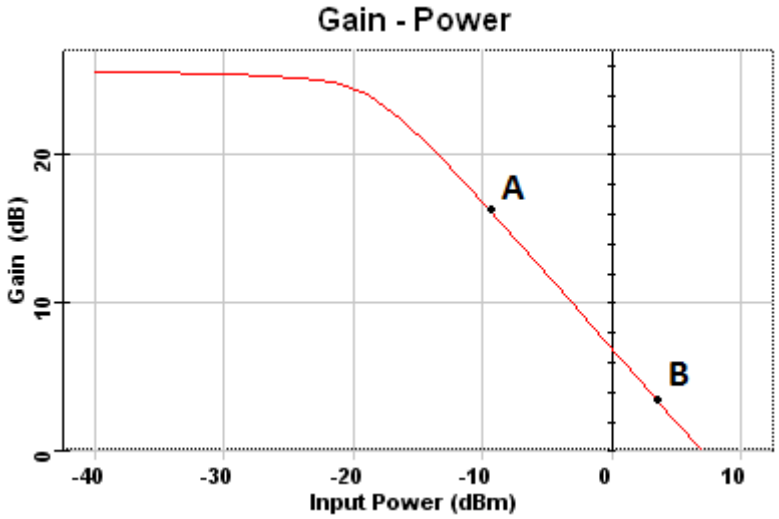


Figure 4.2: The gain profile of a semiconductor optical amplifier.

Table 4.1: Physical parameters.

Parameters	**Symbol**	**Value**
Injection current	I	300mA
Input & output facets reflectivity	R	0
SOA length	L	1600μm
Width of the active layer	W	1.1μm
Thickness of the active region	D	0.1 μm
Confinement factor	Γ	0.2
Linear recombination coefficient	c_1	$36.10^{7}s^{-1}$
Bimolecular recombination coefficient	c_2	$5.6.10^{-16}m^{3}/s$
Auger recombination coefficient	c_3	$80.10^{-41}m^{6}/s$
Group velocity	u_g	$8.5.10^{8}$ m/s
Carrier density at transparency	N	$1.4.10^{+24}$ m^{-3}
Linear radiative recombination coefficient	$Arad$	10^{7}
Bimolecular radiative recombination coefficient	$Brad$	5.10^{-16}
Active regions refrective index	n_a	3.22
Bandgap energy with no injected carriers	E_g	0.77725eV
CW average power	P_{CW}	200 μw
Control pulse peak power	P_{SR}	2mW

4.2.3 Result and Discussion

Operation of the flip-flop has been verified for several non complementary and complementary set and reset pulse input signals confirming successful operation at 10Gbp/s. Figure 4.2 shows the gain profile of the SOA. A and B points indicate the slightly and fully saturated conditions of SOA, whereas the remaining operational conditions are described in Table 4.1.

For assessing the performance of the optical circuit, we evaluated the following three performance parameters. First parameter is the contrast ratio (CR),

$$\mathrm{CR(dB)} = 10\log\left(\frac{{P_{Min}}^{1}}{{P_{Max}}^{0}}\right), \tag{4.7}$$

where ${P_{Max}}^{0}$ and ${P_{Min}}^{1}$ represent the maximum and minimum value of the peak power of 0 and 1, respectively. Next parameter is the amplitude modulation (AM),

$$\mathrm{AM(dB)} = 10\log\left(\frac{{P_{Max}}^{1}}{{P_{Min}}^{1}}\right), \tag{4.8}$$

where ${P_{Min}}^{1}$ and ${P_{Max}}^{1}$ are the minimum and maximum value of the peak power of 1, respectively. Finally, Extinction ratio (ER) parameter is given as,

$$\mathrm{ER(dB)} = 10\log\left(\frac{P_1}{P_2}\right), \tag{4.9}$$

where P_2 and P_1 are the optical power when the output is 0 and 1, respectively. For achieving optimum performance of the circuit following requirements should be satisfied.

- the contrast ratio should be as high as possible so that the largest fraction of the incoming signal exits at the output;
- the amplitude modulation should be low so that the output remains at the same level for logical 1; and
- the extinction ratio should be as high as possible so that logical 1 level can be distinguished clearly from the logical 0 level.

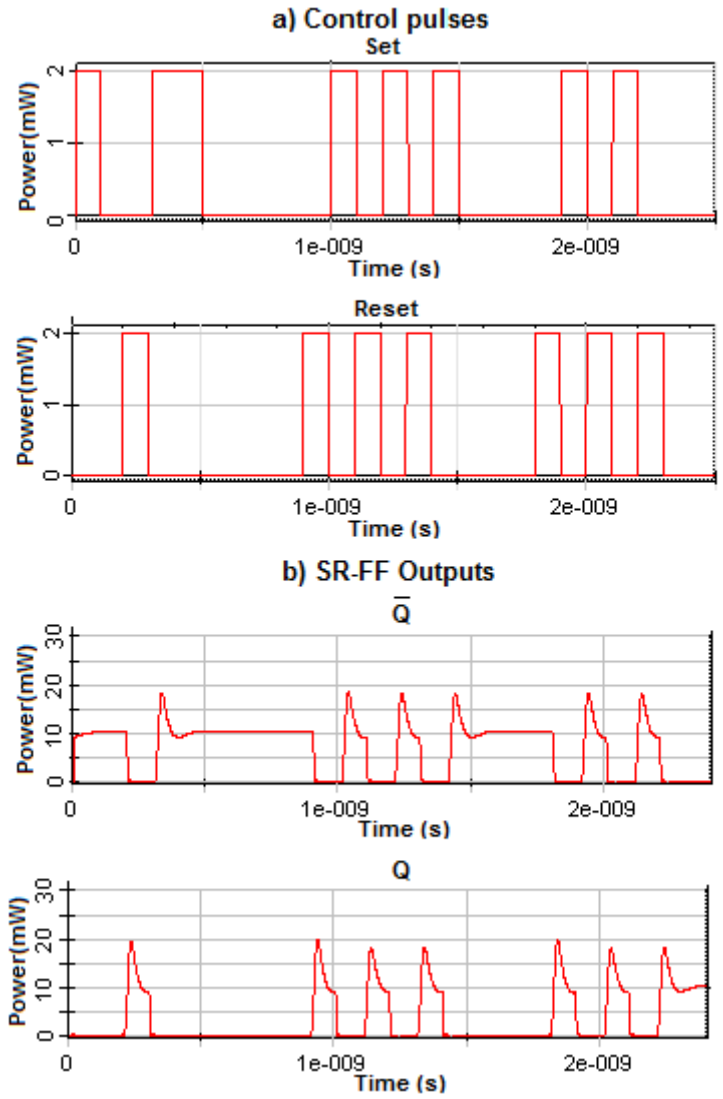


Figure 4.3: Output waveforms of the proposed SR-FF, (a) set and reset input pulses, (b) noninverting and inverting outputs observed at two output ports.

A. SR-FF operation

In Figure 4.3, Output waveforms of the proposed AOFF are depicted. Set and reset control pulses are shown in Figure 4.3 (a). Figure 4.3 (b) shows SR-FF noninverted (Q) and inverted ($\overline{Q}$) outputs. The Set and Reset signals at peak optical power of 2 mW along with CW beams of 200 μW are injected into SOA1 and SOA2 respectively. The signals are injected through the respective SOA branches.

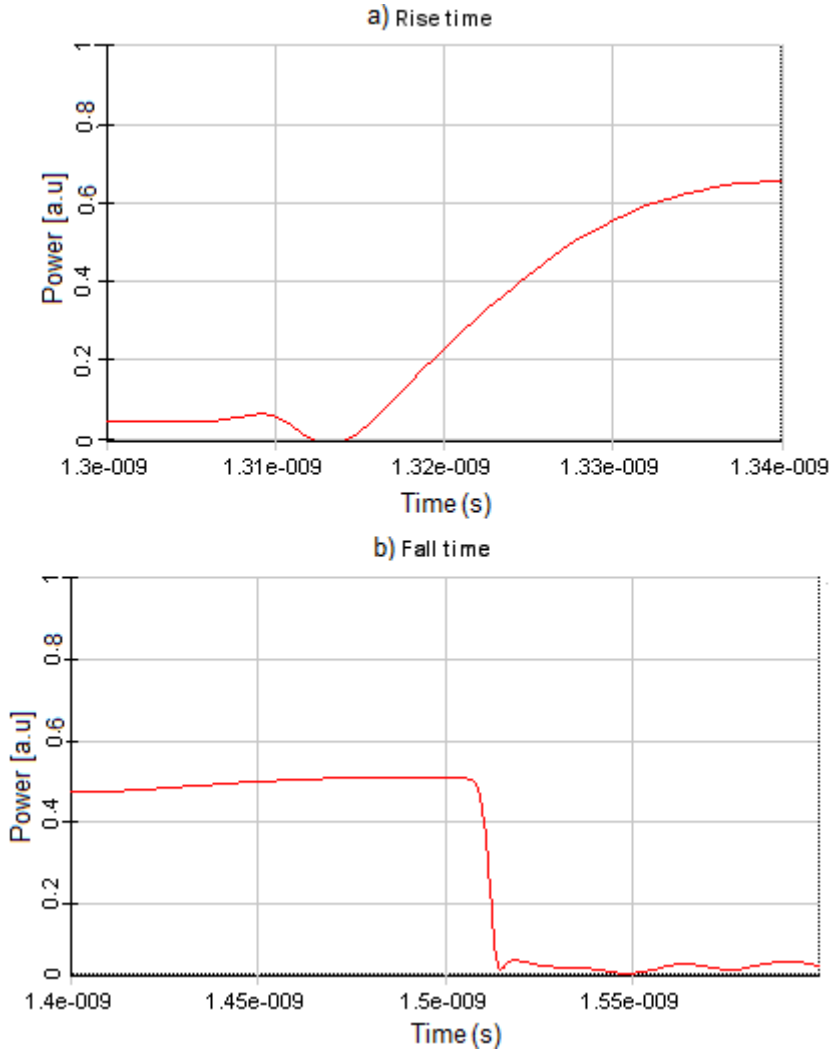


Figure 4.4: Transitions between two states, (a) rising time, (b) falling time.

On arrival of the set pulse, SOA1 gets blocked thus setting a '0' at Q. At the same time, SOA2 gets recovered to set a '1' at $\overline{Q}$. This results in the state of FF as logical '0'. Arrival of Reset pulse results in an assignment of '1' at Q and '0' at $\overline{Q}$. This is defined as the second state of the flip-flop. When Set or Rest pulses are zero simultaneously, slave SOA gain is suppressed by master SOA output and the flip-flop maintains its state. This is shown between 500-900 psec of the pulse traces.

The SR-FF has contrast ratio of 13 dB between two states. Results exhibit an amplitude modulation (AM) of 2.4 and average extinction ratio (ER) of 13 dB for both the FF outputs. Finally, 10%-to-90% rise and fall times have been measured at the outputs of the SR-FF. As shown in Figure 4.4 (a), the rise time is 18 ps. Fall time is less than 10 ps according to Figure 4.4 (b). Thus a RAM cell operation can be achieved at 10 Gb/s. This is faster than the access times of electronic Static RAM cells which is in ns range.

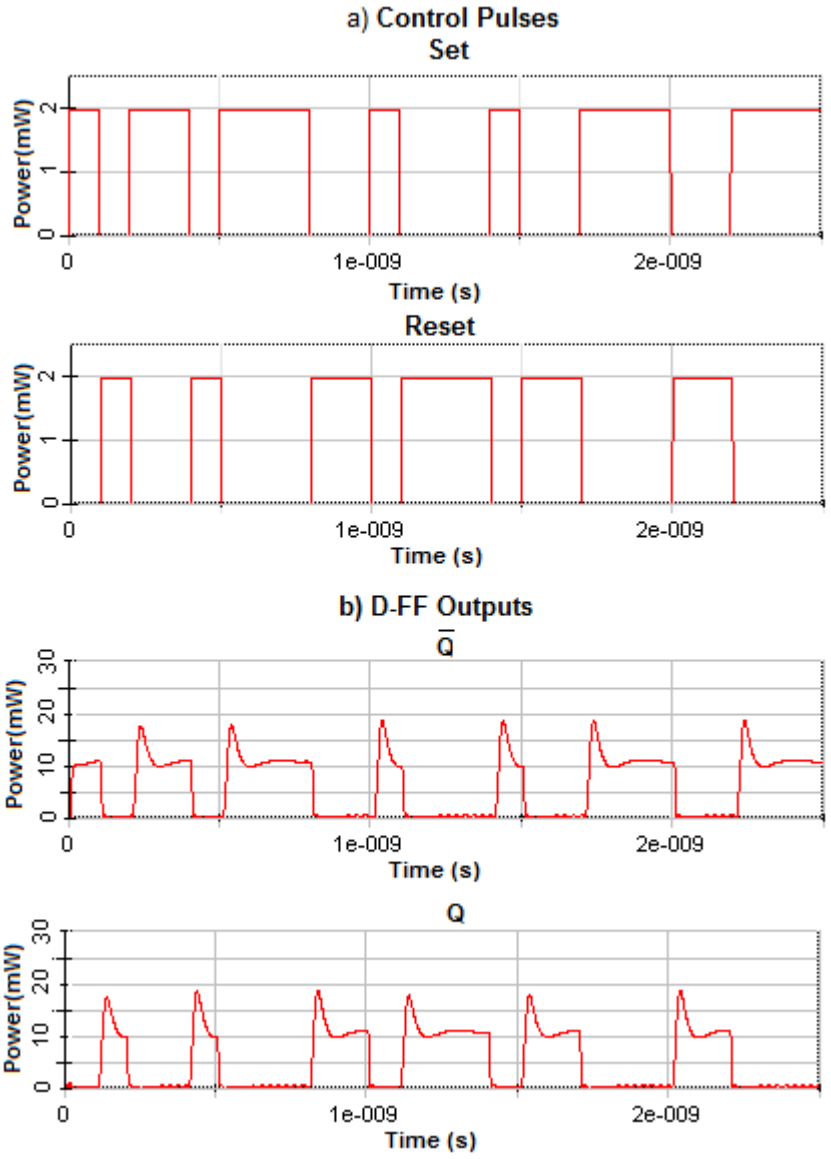


Figure 4.5 (a) Set and Reset control pulses (D-FF) and (b) the FF states observed at Q and $\overline{Q}$ outputs.

B. D-FF operation

For D-FF operation complementary control pulses are applied as Set and Reset inputs. Figure 4.5 (a) depicts the Set and Reset signals which drive the D flip-flop operation. The FF output results are illustrated in Figure 4.5 (b). Improved performance of 14dB ER, 13dB CR and 1.7dB amplitude modulation is observed in case of complementary Set and Reset input pulses. Flip-flop outputs exhibit a slight gain overshoot and some pattern effect when switching the state of the flip-flop. Full switching can be achieved at

operational speed of 10 Gb/s. Higher operational speeds up to 20 Gb/s can be achieved at the expense of higher amplitude modulation and lower contrast ratio values.

4.3 Investigation of All Optical Circular Shift Register based on SOAs

Demand of data communication for future photonics networks is ever- increasing. In order to fulfill this demand high speed processing of digital signals is required. Elaboration of photonics signal at the optical layer is attractive for performing different computational functionalities and overcoming all the limitations with respect to speed of electronics. The examples are packet buffering, header processing, bit-length conversions, switching, reshaping and retiming [91].

Optical shift registers find applications in serial-to-parallel converters, optical packet buffers, and synchronizers [61], [62], [63]. They might also become essential building blocks for more complex subsystems. These devices have received considerable attention as they can play a significant role in signal processing techniques. Other applications include cyclic operations. Examples are cyclic redundancy checks and parity that enable digital correction and detection of errors occurring during transmission. The circulating shift register can be a basic building block for other applications such as optical memory and clock division.

In the literature, different shift register schemes have been suggested as described in Section 2.2.4. In [71] a circular shift register comprising of an optical buffer and a bit selecting circuit based on fiber Kerr nonlinearities has been proposed. As a result of weak Kerr coefficient in fibers, high optical powers and long fiber lengths are necessary [38]. Therefore further amplification is needed before applying the buffer output to the bit selecting circuit. Optical logic functions may be implemented by employing nonlinear effects either in semiconductor optical amplifier or in optical fiber. Implementations utilizing SOA have shown great potential as compared to fiber based implementations. Low power consumption, high speed, potential for optical integration and small footprint are the salient features of the device [92].

In this Section, a new scheme is presented to realize all optical circular shift register consisting of a optical buffer and an optical AND gate. The OB is implemented by employing a fiber-loop and using SOA as a nonlinear element. It is capable for storing a finite number of bits at a required bit rate. AND gate provides the consecutive bits at output at a lower clock rate. The AND gate is realized by incorporating FWM effect in a SOA which gives a more compact, efficient and potentially integrable solution as

compared to fiber based implementation. Successful 10-bit shifting operation is presented at a sequence bit rate f_b = 2.5 GHz and f_b = 10 GHz respectively. The concept can be implemented for different number of bits for a given loop length delay time. Two important SOA parameters, confinement factor and SOA length are optimized to enhance the FWM effect and hence quality of the output signal.

4.3.1 System Setup and Operation Principle

Figure 4.6 shows the schematic of the circular optical shift register, which comprises of a semiconductor optical amplifier based optical buffer and an optical AND gate. The buffer is capable of storing a finite number of bits at high bit rate. AND gate is used to provide the consecutive bits at output at a lower clock rate.

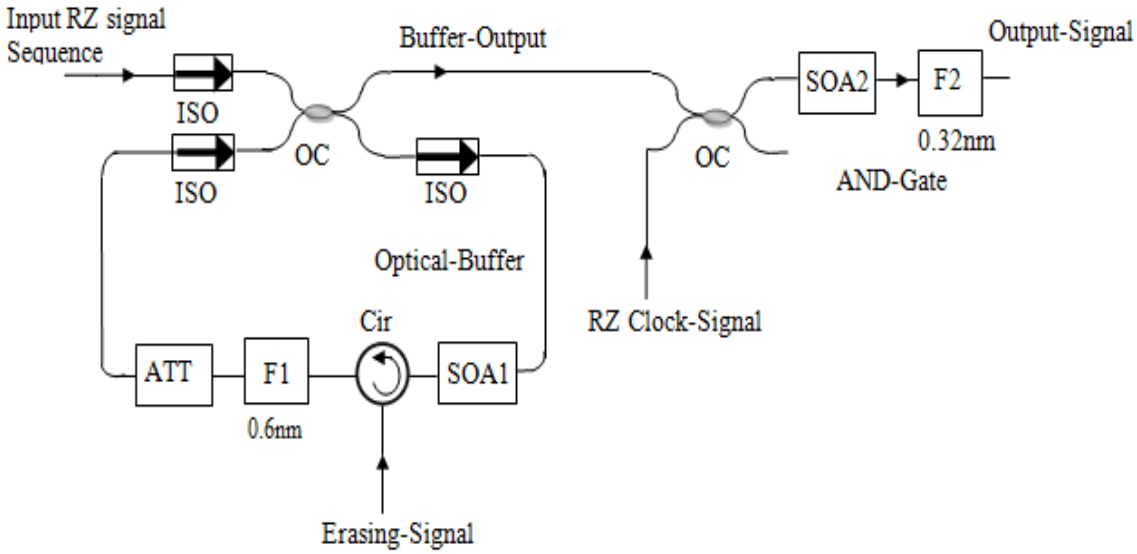


Figure 4.6: Schematic configuration of all optical circulating shift register.

The optical buffer consists of two isolators, an optical 3dB coupler, an optical band pass filter (OBF), an optical attenuator, a circulator and a semiconductor optical amplifier (SOA1). Optical coupler provides the access to the loop. The isolators were used to allow the light to propagate in only one direction thus reducing reflections.

Apart from acting as an amplifying medium, SOA1 enables the Erase operation of the shift register. Erasing signal is introduced through the circulator and a 0.6nm optical band pass filter (F1) has been used to suppress the amplified spontaneous emission noise inside the cavity.

Buffer output signal along with the RZ clock signal is applied to an optical AND gate. The AND gate is implemented by means of FWM effect in SOA2. When both the input signals, which are at different wavelengths, are applied to the semiconductor optical amplifier, the conjugated light is generated due to the four wave mixing effect. A tunable narrow optical bandpass filter (F2) with 0.32 nm bandwidth is utilized for filtering the AND logic.

Analogous to its electronic counterpart, three operations are performed with the circulating shift register. These are: Write Shift and Erase. The first operation is to write the n bit sequence in the shift register. When the write operation is over, n bit shifting is performed, one at each clock transition. After completion of the n shifts all the bits that were stored in the register are returned at the shift register output, one at each clock transition and in the same order of the original sequence. When the n shifts have been performed, the shift register is erased and a new sequence can be written into the register. Fig.2 shows the bit sequences associated with various signals depicted at different points in the schematic configuration for a 4 bit input sequence.

When the input signal sequence is applied to buffer which constitutes the write operation, the signal starts circulating the buffer. For a given length of the fiber $\boldsymbol{L}$, the maximum delay per loop traversal $\boldsymbol{T_{loop}}$ is given as

$$\boldsymbol{T_{loop}} = \frac{\boldsymbol{n_r L}}{\boldsymbol{c}}, \qquad (\mathbf{4.10})$$

Where $\boldsymbol{L}$, $\boldsymbol{n_r}$, is the length and refractive index of the fiber, respectively; $\boldsymbol{c}$ is the speed of light in the vacuum. The maximum number of bits $\boldsymbol{n}$ that can be stored for a given bit rate $\boldsymbol{B}$ is given as [93].

$$\boldsymbol{n} = \frac{\boldsymbol{n_r L}}{\boldsymbol{c}} \boldsymbol{B}. \qquad (\mathbf{4.11})$$

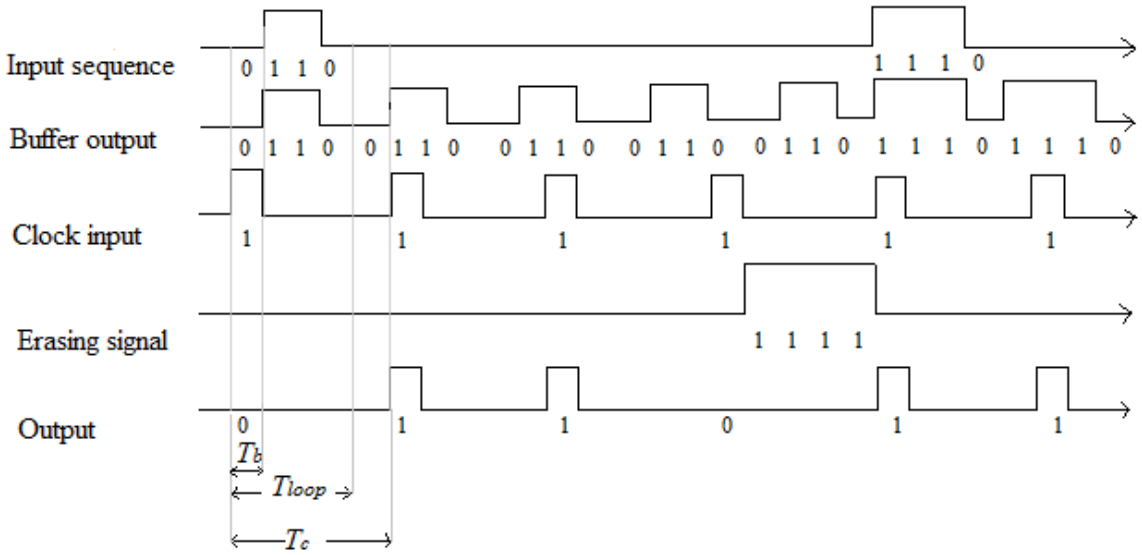


Figure 4.7: Bit sequences of the signals depicted at different points in the schematic configuration for 4 bit input sequence.

As seen in the Figure 4.7, the propagation time of the cavity $\boldsymbol{T_{loop}}$ is set to be equal to the $\boldsymbol{n}$ bit input sequence duration $\boldsymbol{nT_b}$, where $\boldsymbol{T_b}$=1/$\boldsymbol{f_b}$ is the bit interval. Therefore after each traversal a replicated signal appears at the buffer output.

Time reference for the register state is set by a return-to-zero (RZ) clock. When buffer output signal along with the RZ clock signal having time period $\boldsymbol{T_c = T_b(n+1)}$ is applied to SOA2, a conjugated light is generated due to FWM effect in SOA. The conjugated light is optically filtered out by OBF (F2) thus extracting the stored bit sequence. This is achieved by the selection of the first bit of the original input sequence, then the second bit of the first replicated sequence, the third bit of the next replicated sequence and so on.

In order to erase the bit pattern from the buffer an erasing signal with duration equal to $\boldsymbol{n}$ bit input sequence duration $\boldsymbol{nT_b}$ is fed to SOA1.This signal saturates SOA1 due to cross gain modulation effect and will cancel the existing bit pattern in the buffer. Thus a new $\boldsymbol{n}$ bit sequence can be stored in the shift register.

4.3.2 Results and Discussion

First, we investigate the operation of circulating shift register for a 10-bit input sequence at the sequence bit rate f_b =2.5 GHz and f_b =10 GHz respectively. Secondly, we examine the BER performance of the circular shift register in the case of f_b =10GHz. Finally, the effects of both confinement factor and length of SOA2 on quality of the output signal are highlighted.

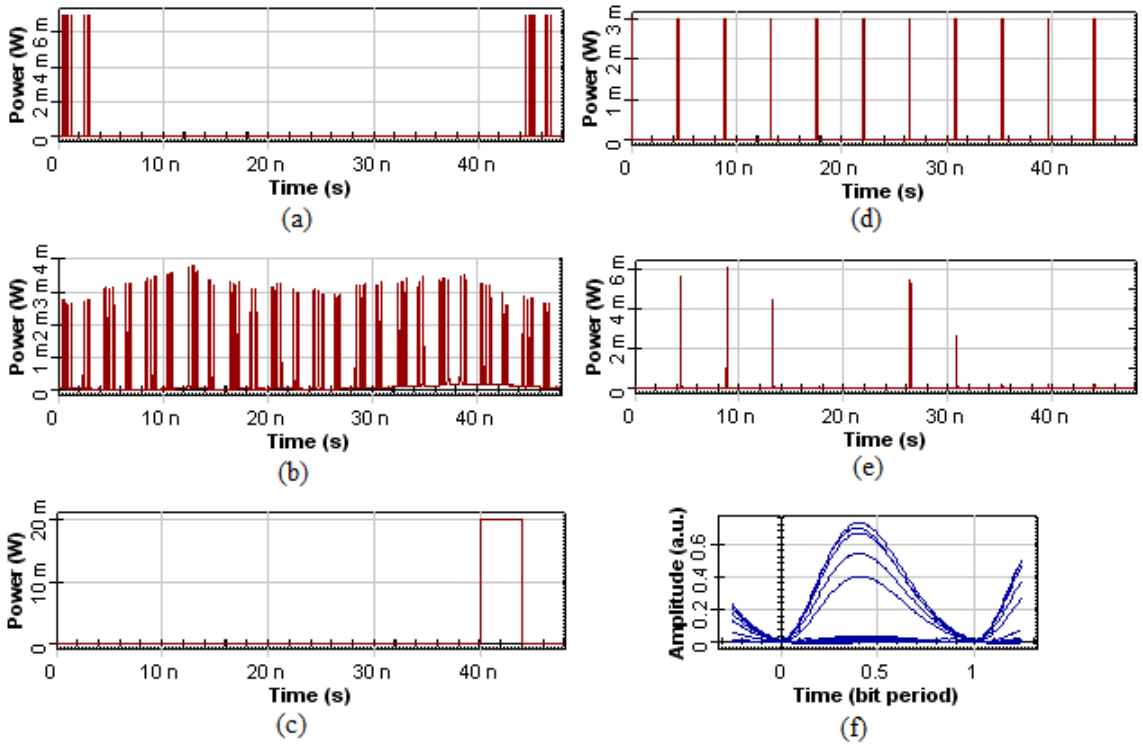


Figure 4.8: Results of shifting the format of 0111001100 in the case of f_b = 2.5 GHz. (a) Input signal (b) Buffer output (c) Erasing signal (d) Clock input. (e) and (f) show the output of the shift register and corresponding eye diagram.

Figure 4.8 shows how the information format of 0111001100 is shifted through the circulating shift register in the case of f_b =2.5 GHz. The corresponding T_b and T_c values comes out to be 0.4ns and 4.4ns respectively. The optical delay of the feedback loop (T_{loop}) was adjusted to 4ns. The input bit sequence is RZ coded with 33% duty cycle at a wavelength of 1553.3nm as shown in Figure 4.8 (a). Buffer output consisting of first initial sequence, ten replicated sequences and next initial sequence is shown in Figure 4.8 (b). Return-to-zero (RZ) pulsed signal was used as clock with 33% duty cycle at a wavelength of 1552.5nm [Figure 4.8 (d)]. RZ modulated signals are used as clock signal as it can tolerate more distortion and improves the tolerance of the device to chromatic dispersion and timing jitter. Spectrum at the SOA2 output is depicted in Figure 4.9.

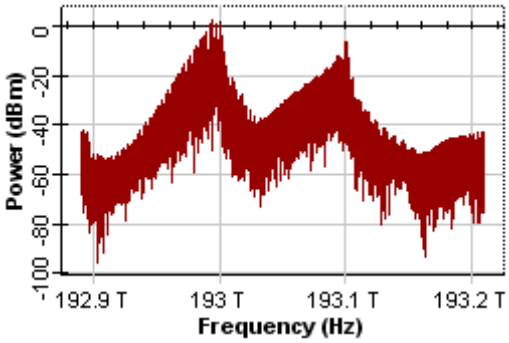


Figure 4.9: Spectrum at the SOA2 output.

Buffer output signal interacts with the RZ clock signal in SOA2, thus generating the power at new FWM frequencies at 192.9 THz and 193.2 THz respectively. The conjugated light generated at 193.2 THz (1551.72 nm) is filtered out by OBF (F2). As conjugated light is generated at a frequency which is close to the input clock signal frequency so, a narrow bandwidth OBF (0.32nm) is selected for this purpose. The output signal generated from the logic AND operation and its corresponding eye diagram are shown in Figure 4.8 (e) and (f) respectively.

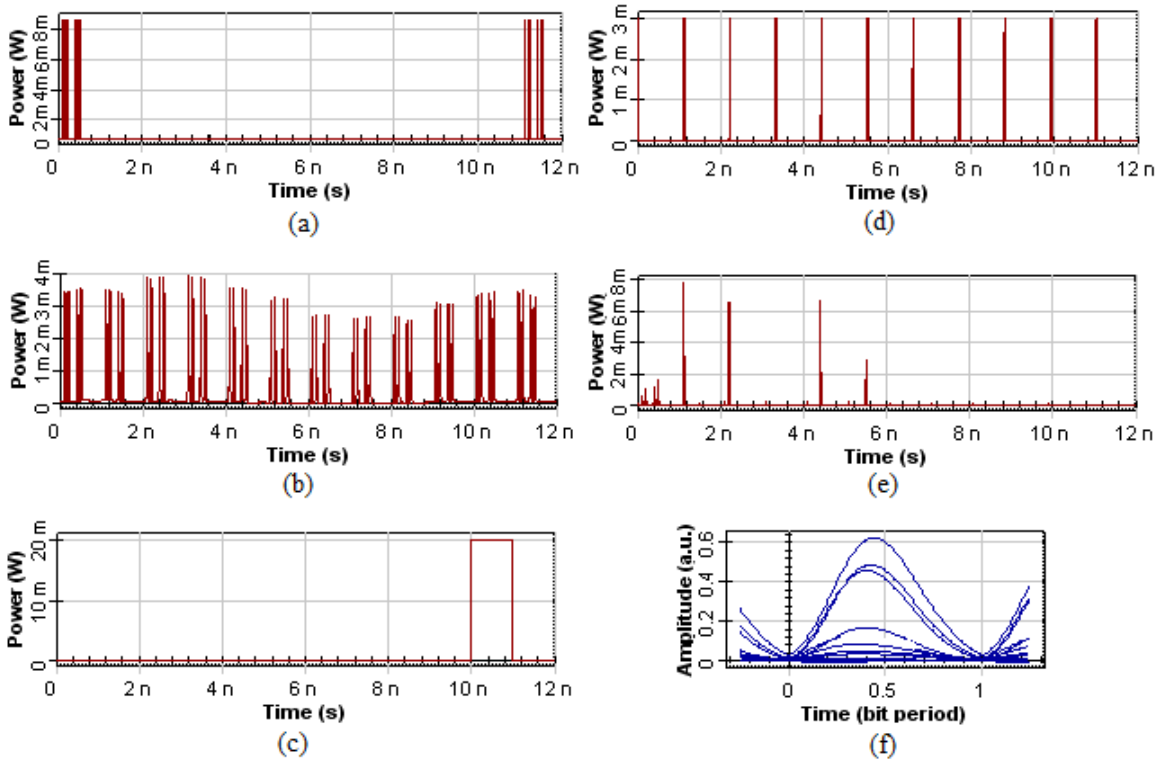


Figure 4.10: Results of shifting the format of 0110110000 in the case of f_b = 10 GHz. (a) Input signal (b) Buffer output (c) Erasing signal (d) Clock input. (e) and (f) show the output of the shift register and corresponding eye diagram.

Figure 4.10 shows the signals at the addressed points of Figure 4.6 for the case of f_b = 10 GHz. As a consequence of this choice, T_b and T_c were 0.1ns and 1.1ns respectively. T_{loop} was set to be 1ns corresponding to these values. Figure 4.10 (a) depicts the 10 bit input sequence 0110110000 applied as shift register input. Buffer output consisting of first and second initial sequences that do not circulate into the loop and ten replicated sequences of the first initial sequence is shown in Figure 4.10 (b).

After completion of the ten shifts, all the ten bits that were stored in the register are returned at the shift register output, one at each clock transition and in the same order of the original sequence. [Figure 4.10 (e)]. At the end of the tenth shift, shift register sequence is erased and thus a new cycle begins for storing the second initial sequence.

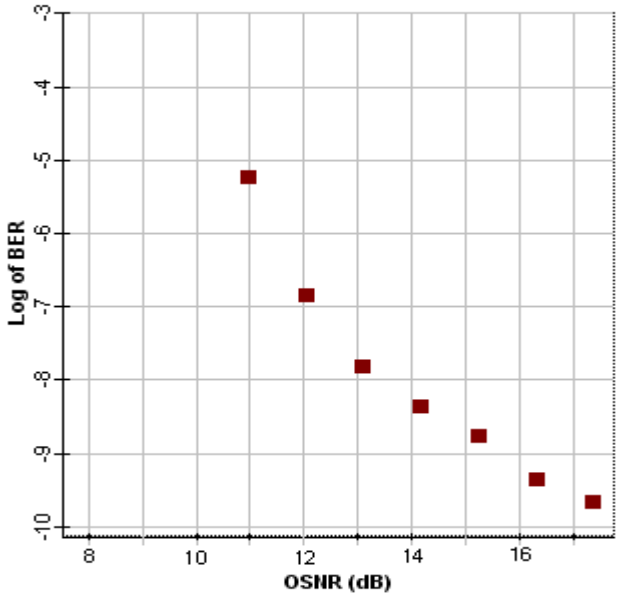


Figure 4.11: BER performance versus SNR at the output of circulating optical shift register for a 10 bit input sequence.

Figure 4.10 (f) and Figure 4.11 shows the output eye diagram and BER performance of the circulating shift register for the case of f_b =10GHz. BER=10^{-9} is achieved at OSNR of 16 dB at the output of the shift register. The impairments arise from the ASE noise introduced by SOAs and FWM effect in SOA2.

We further investigated the effects of confinement factor and length of SOA2 on quality of the output signal. The above two parameters are varied in order to enhance the four wave mixing effect and thus maximize the Q factor response at the shift register output.

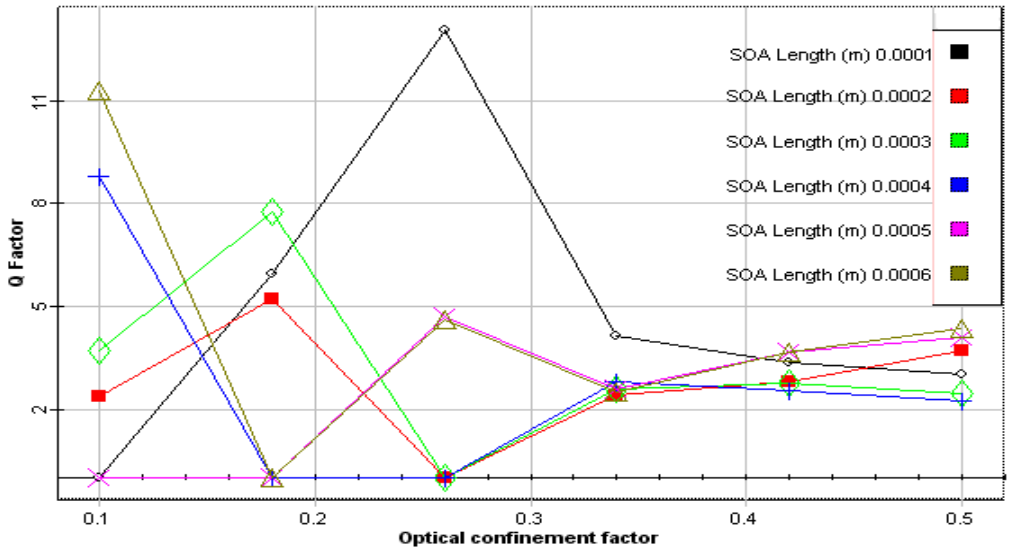


Figure 4.12: Q factor variation with optical confinement factor for different SOA Lengths.

In Figure 4.12 the maximum Q factor is represented with respect to confinement factor for different values of length of SOA2. For a fixed gain compression, the increase in the length of SOA corresponds to the increase in the input power energy [94]. The gain recovery time on the other hand is inversely proportional to the confinement factor. Thus higher values of confinement factor and lower values of SOA length are desirable. As seen in the Figure 4.12, the Q factor remains less than 6 for the values of confinement factor exceeding 0.34. For the value of confinement factor = 0.1, the higher Q values are possible for the increased values of the SOA length. The maximum Q is achieved at the values of confinement factor and SOA length as 0.26 and 0.0001m respectively.

4.4 5-GHz All-Optical Binary Counter Employing SOA-MZIs and an Optical NOT Gate

Computing Machines with high performance (HPCM) are just entering the exaflop era. For a balanced system design approach similar advances are required in all its functional subsystems. Electronic RAM devices still suffer from long access times and limited bandwidth. This imposes a major bottleneck in further enhancement of processing capabilities [95].

For reducing the gap between throughput of the processor and speed of the memory, focus of the research has shifted on development of ultrafast all optical latching devices

and flip-flops. A number of optical flip-flops based on different technologies have already been proposed in the literature [84], [89].

All optical binary counters are the key components to be utilized in photonics networks. These find applications in areas of communication as well as optical computing. The device can be used in packet switching networks, payload processing, header recognition and as a finite state machine in optical computing.

A small number of devices capable of performing optical bit counting functions have been reported so far [10], [58], [59]. Most of these devices rely on analog time-of-flight designs and there is a limited potential for integration [58], [59]. An optical counter using directional coupler switches has been demonstrated in [58]. The switches are polarization-dependent. Optoelectronic conversion is one of the requirements in this counter. In [59] an all-optical binary counting is carried out using a TOAD based switching gate. This configuration requires an external clock signal and provides a serial output.

A true digital optical counter has been proposed and demonstrated at 120 kHz data rates. It uses SR optical flip-flops and employs coupled semiconductor optical amplifiers based ring lasers [10]. SR FFs are utilized to provide latching functionality in this scheme. Flip-flops are assisted by auxiliary signals which are generated by two AND gates arranged in a feedback configuration.

In this Section, an all optical binary counter is presented employing two stages of optical TFF and an optical NOT Gate. The TFF consists of a SOA based MZI and an external feedback loop. The proposed counter is implemented using the minimum number of active components and with only a single control signal as input. Principle of operation is numerically evaluated for the proposed counter at 5 GHz. The switching times exhibited by the counter are less than 80 ps. Simple structure implies low power consumption and reduced footprint making it suitable for photonic integration.

A single control signal is required at the input of the proposed counter architecture. This relaxes the need for generation of auxiliary signals by additional combinatorial circuitry. In this way, it provides a successful counting operation by utilizing the minimum number of components that have been reported so far. It reduces the power consumption and complexity requirements. Further, it retains all speed advantages of optical interferometric switching gates as compared to coupled-laser based digital counter counterparts that usually require significantly higher time constants. Thus length of the feedback loop is the main factor determining the speed of proposed counter circuit in the practical implementation.

Table 4.2: Truth Table of the 2-bit binary optical counter.

Optical clock pulses	Inputs T	Outputs Q_1	Q_0
0	1	0	0
1	1	0	1
2	1	1	0
3	1	1	1
4	1	0	0

4.4.1 System Setup and Operating Principle

Truth table of the optical 2-bit binary counter is given in Table 4.2. From the truth table it is observed that the counting operation is achieved whenever a clock pulse arrives at the input of the counter. Figure 4.13 depicts a conventional counter layout of the proposed optical binary counter. It comprises of two stages of T FFs and a logical NOT gate. The input optical pulse sequence to be counted (CLK_0) is applied to the 1st stage of optical T-FF (T-FF0). The T-FF0 switches its state upon the arrival of every new clock pulse. This provides the one-bit counting operation at its Q_0 output. Q_0 signal thus generated is applied to a logical NOT gate which generates a $\overline{Q_0}$ signal at the output. $\overline{Q_0}$ signal acts as a clock input CLK_1 for the second stage. This signal is applied to the 2nd stage of optical T-FF (T-FF1), where the second bit counting function is performed thus generating Q_1 signal at the output.

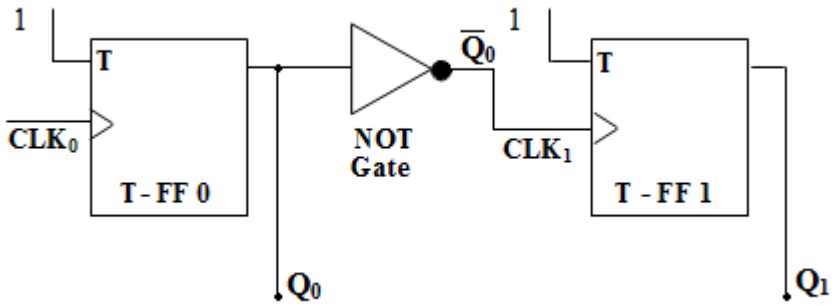


Figure 4.13: conventional counter layout of the proposed optical binary counter.

Figure 4.14 depicts the architecture of the proposed optical counter. Ld1, Ld2, Ld3 and Ld4 generate continuous wave (CW) beams at wavelengths 1555 nm (λ_1), 1550 nm (λ_2), 1550 nm (λ_3), and 1555nm (λ_4) respectively. CW input signal at wavelength λ_1 acts as input signal to the 1st stage of T-flip-flop (T-FF0). NRZ pulse sequence (CLK_0) is applied

as a control signal in SOA2. A 2 × 2 coupler is used to interconnect output port (#1) to the upper branch of the MZI through a feedback loop. The power at the output of the flip-flop can be properly adjusted by modifying the coupling factor of feedback loop. To remove the external clock signal before applying the feedback signal as a control signal to SOA1, a 0.6 nm OBF1 centered at a wavelength 1555 nm is utilized. For adjusting the power level of the signals, variable optical attenuators (VOAs) and optical amplifiers (OAMPs) have been used at different stages of the setup.

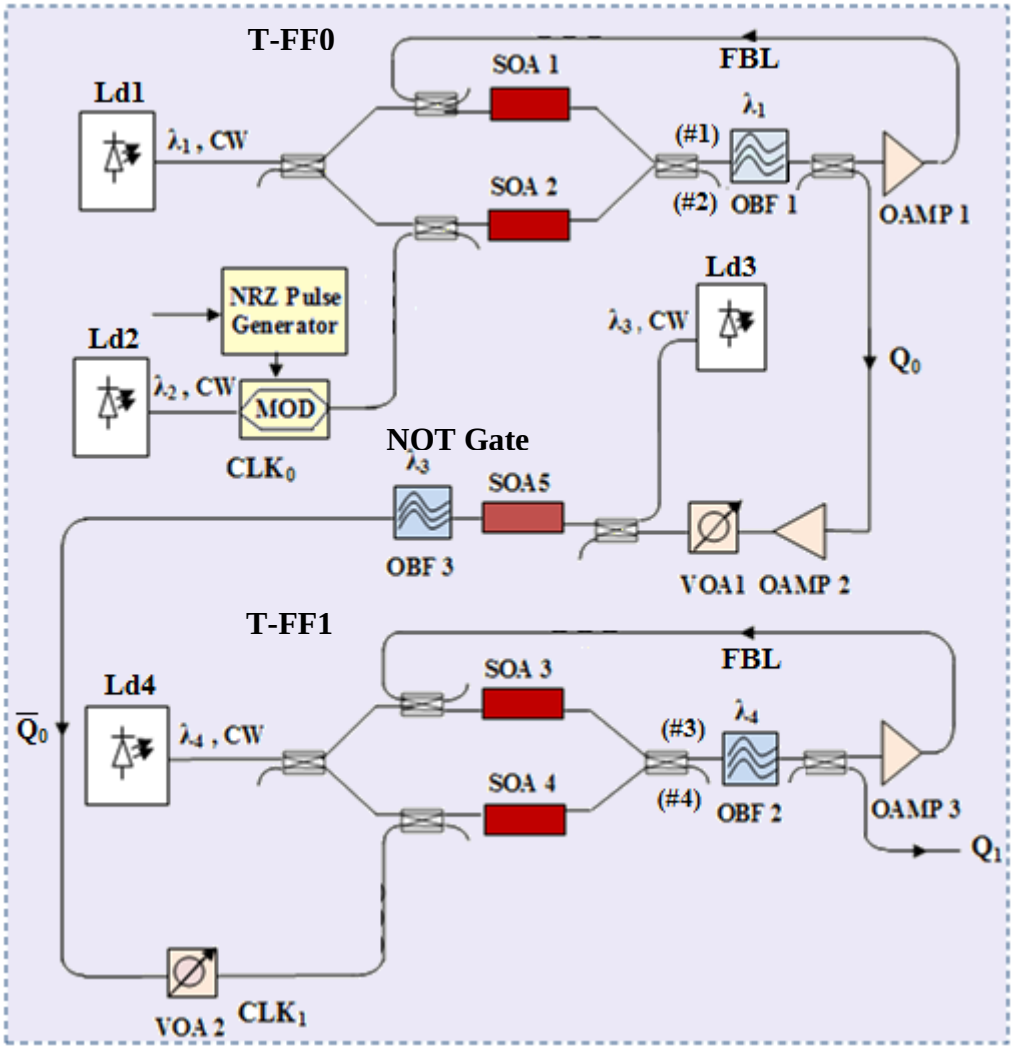


Figure 4.14: The proposed all-optical 2-bit binary counter.

π/2 phase shift is provided between both SOA-MZI arms by the input and output couplers. Thus, when there is no control signal, no output signal is received at the MZI port (#1). This results due to destructive interference taking place at the output coupler. On injection of first optical input pulse into the counter, differential gain and carrier density of SOA2 decreases. This causes the continuous wave input signal to be switched

to and appear at the Port (#1). Delay time caused by the length of the loop is chosen to be equal to the input optical pulse duration. Therefore entire loop will be filled with the switched continuous wave signal. Due to this, even after the end of the original optical pulse, switching operation of the SOA-MZI is sustained. On arrival of the next optical pulse in sequence, MZI performs a logical exclusive or operation. This results due to the simultaneous presence of two control pulses in the respective semiconductor optical amplifiers. This will force the continuous wave signal to exit from the Port (#2). Thus feedback-loop will be emptied from continuous wave light signal and the flip-flop output will switch to a logical '0' state. In this way, first stage of optical T-flip-flop switches its output state on arrival of the each new optical input pulse.

XGM effect in SOA5 has been used for realization of the NOT gate. NOT logic is filtered using OBF 3. The Q_0 output signal of the 1st stage of T-flip-flop (T-FF0) acts as control signal to this SOA. Continuous wave signal at λ_3 wavelength serve as input signal in the SOA5. The generated $\overline{Q_0}$ signal is applied to the second stage of T-FF (T-FF1). Both the flip-flop stages are identical except for the difference in the delay times of the loop length, which is double for the case of 2nd stage.

4.4.2 Results and Discussion

An experimentally validated simulation model is used for the numerical evaluations of the principle of operation. It confirms that an escalation of the speed at multi-Gb/s levels is feasible. The time domain simulation model is based on the transfer matrix method (TMM) [96], [97]. The carrier density (N_i) is described by a well known rate equation:

$$\frac{\partial N_i}{\partial t} = \frac{J}{ed} - N_i\left(c_1 + c_2 N_i + c_3 {N_i}^2\right) - \sum_{u=1,2,3} u_g \Gamma \, {g_m}^{(u,i)} s^{(u,i)} \qquad (4.12)$$

Where d is the thickness of an active region, J is the total injection current density, c_3, c_2 and c_1 are the recombination constants associated with auger recombination, radiative recombination and current leakage respectively, e is the electron charge, u_g is the group velocity, the index "u" refers to the amplified spontaneous emission and external photon streams, and $s^{(u,i)}$ and ${g_m}^{(u,i)}$ are the photon density and material gain coefficient in the ith section for the light designated by "u", respectively.

To describe the material gain coefficient, a wideband steady state numerical model is used [90].

$$g_m = \frac{c^2}{4\sqrt{2}\,\pi^{3/2} n_a{}^2 \tau \nu^2} + \left(\frac{2m_e\, m_{hh}}{\hbar(2m_e + m_{hh})}\right)^{3/2} \times \sqrt{\nu - \frac{E_g}{h}}\,[f_c(\nu) - f_\nu(\nu)] \qquad (4.13)$$

where n_a is the refractive index of the active region, τ the radiative recombination lifetime, c the velocity of light in vacuum, $\hbar$ the Planck's constant divided by 2π, ν the optical frequency, E_g the bandgap energy, m_{hh} and m_e the valence band heavy hole and conduction band electron effective masses respectively and $f_v(\nu)$ $f_c(\nu)$, the Fermi-Dirac distributions in the valence and conduction band respectively.

Each semiconductor optical amplifier is identical and is characterized by an active layer thickness of 0.1μm, a length of 900 μm, an active layer width of 1.2 μm, a bias current of 300 mA, a confinement factor of 0.2, carrier lifetime of 40 ps, a cladding's refractive index of 3.0 and an active region's refractive index of 3.2. To our knowledge, neglecting polarization issues is the only assumption that has been made. As it is well-known, in order to achieve optimum performance the states of polarization of optical signals at the inputs of a MZI have to be controlled carefully. In a practical setup, even a slight deviation of the optimum polarization states of the input signals may result in the reduction of the output power and efficiency or performance of the device. There may not be any influence on the counter operation.

Figure 4.15 shows the timing diagram of the optical binary counter. The input optical pulses at a clock rate of 5GHz are depicted in Figure 4.15 (a). Q_0 and $\overline{Q}_0$ outputs of all optical counter are depicted in Figure 4.15 (b) and (c) respectively. This reveals the successful operation of the circuit. NRZ modulated optical input pulses, having a peak power of 1.8mW, are injected to the first stage of optical T-FF (T-FF0). For a continuous wave input signal of 0.8 mW, the coupling factor is adjusted to obtain maximum output power. The optical delay for the feedback loop (marked in Figure 4.14 as FBL) is adjusted to 200 ps. This corresponds to a waveguide length of about 40 mm. The Q_0 signal thus generated complements with each input count pulse.

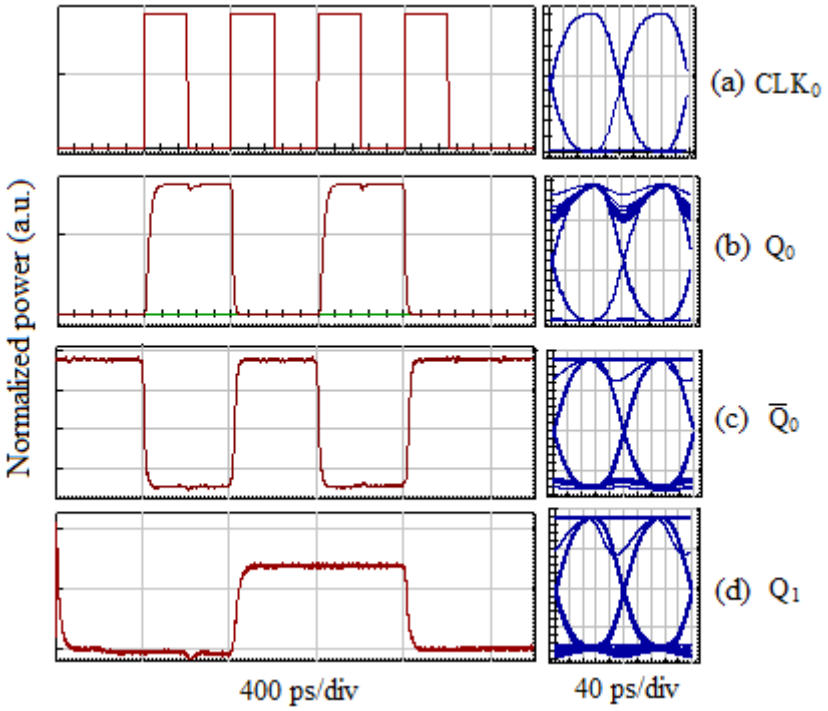


Figure 4.15: (a) Input optical pulses to be counted, (b) the T-FF0 output (Q_0), (c) NOT gate output ($\overline{Q}_0$), (d) the T-FF1 output (Q_1).

Q_0 signal exhibit a high extinction ratio (higher than 11.5 dB) as shown in the simulation results of Figure 4.15 (b). The main reason for this high performance is that the "zero/off" level is almost perfect. This is due to the destructive interference of the bias power and the two control pulses in their respective semiconductor optical amplifiers at the output of the MZI during the period of occurrence of 2^{nd} and 4^{th} input optical pulse. Pulse sequence observed at the output of the NOT gate is illustrated in Figure 4.15 (c). Logical NOT operation is obtained through cross gain modulation effect in semiconductor optical amplifier. As a result of non ideal logical NOT operation, the $\overline{Q}_0$ signal exhibits lower extinction ratio.

The $\overline{Q}_0$ signal at the output of the NOT gate acts as the input clock signal for the next stage of optical T-FF (T-FF1). T-FF1 output is shown in Figure 4.15 (d). Figure depicts that the Q_1 switches to a logical high state on arrival of the second pulse of original optical pulse sequence and remains at this level until the fourth pulse arrival. This indicates the successful second digit counting operation. The extinction ratio of the T-FF2 output signal was found to be 9.7dB. The reason for the lower performance of the signal

at the output of the second stage was the accumulation of noise and lower extinction ratio of the pulses used for switching T- FF2.

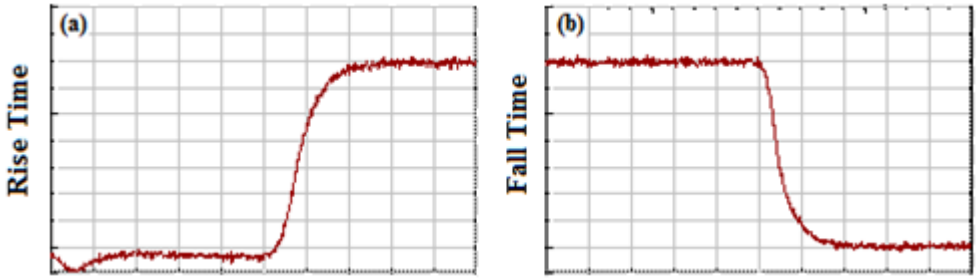


Figure 4.16: (a) Rise time and (b) fall time of the output pulse at Q_1.
Time scale: 80 ps/div.

Figure 4.16 depicts the transition times of rising and falling edges between two states for the Q_1 output pulse. Rise and fall times are illustrated in Figure 4.16 (a) and (b) respectively with 10% to 90% values being lower than 80 ps. The rise and fall times of the output optical pulses directly depend on the speed of the semiconductor optical amplifier and the rise time of the input clock pulses.

4.5 Conclusion

In this chapter, SOA-based all optical flip-flops, binary counter and shift register have been investigated. First, a simple and new scheme is proposed for all-optical SR and D flip-flop employing XGM effect in two wideband semiconductor optical amplifiers. Flip-flop operation is verified for several non complementary and complementary set and reset pulse signals confirming successful operation at 10Gbp/s. SR-FF results exhibit an ER, CR and AM of 13dB, 13dB and 2.4dB respectively. Improved performance of 14dB extinction ratio, 13dB contrast ratio and 1.7dB amplitude modulation is demonstrated in case of D-FF with complementary Set and Reset input pulses. Although both flip-flop outputs experience a slight gain overshoot when switching state and some pattern effect, it has been clearly shown that full switching can be achieved at a operational speed of 10 Gb/s. Semiconductor optical amplifier recovery time and intra-FF coupling length are main factors in determining the speed-limit of the flip-flop. Multi-Gb/s operational speeds are feasible if photonic integration is employed to allow for ultra-short coupling lengths between the two semiconductor optical amplifiers.

Secondly, the performance of an all optical circulating shift register consisting of a semiconductor optical amplifier based optical buffer and an optical AND gate is numerically investigated. The shift register is designed to store an n-bit sequence and to return its bits one by one at a lower clock rate. The increase in the number of bits to be stored does not increase the complexity of the scheme. The operation of the circulating shift register has been verified for a 10-bit input sequence at sequence bit rate of 2.5 GHz and 10 GHz respectively with the speed being mainly determined by the fiber-based feedback loop implementation, so that multi-Gb/s operation should be considered feasible by deploying it as an integrated device. The dependence of the output *Q*-factor on SOA parameters is also investigated and discussed. The circulating shift register can be a basic building block for other applications such as optical memory and clock division.

Finally, an all optical binary counter is presented employing two stages of optical TFF and an optical NOT Gate. The TFF consists of a SOA based MZI and an external feedback loop. The proposed counter is implemented using the minimum number of active components among the digital optical bit counting devices reported so far. It requires only a single control signal as input. Principle of operation is numerically evaluated for the proposed counter at 5 GHz. The switching times exhibited by the counter are less than 80 ps. Feedback loop length is the main factor determining the speed of proposed counter circuit in the practical implementation. Simple structure implies low power consumption and reduced footprint making it suitable for photonic integration.

Chapter 5

All Optical Arithmetic and Logical Circuits based on Semiconductor Optical Amplifiers

5.1 Introduction

This Chapter deals with the study and realization of arithmetic and logical circuits, which is related to the third objective of this thesis. Different functions of optical digital signal processing are realized by employing nonlinear effects in a SOA. The all-optical realizations of adder, subtractor, comparator, demultiplexer, decoder etc are based on SOA-MZI. Numerical Simulations confirming the described logic devices have been presented for different input combinations. Further, SOA-MZI based all optical demultiplexer operation has been analyzed in demultiplexing of an optical time division multiplexing channel at data rates up to 160 Gb/s.

5.2 All Optical Arithmetic and Logical Circuits using SOA-MZI

Different types of ultra fast optical switches have received considerable attention all over the world to realize all optical algebraic and logic processors. Some of them are TOAD, Sagnac switch, UNI and the SOA-MZI [98], [99], [100].

Interferometric gates employing Mach-Zehender Interferometer and using SOA as the nonlinear element have gained lot of attention. This is due to their high operational speed, low power consumption, high stability and large potential for integration with a variety of passive and active components [78].

There are different kinds of topologies available. Among them, monolithically integrated Mach-Zehender Interferometer switches are one of the most promising solutions. This is as a result of their thermal stability, low power operation and compact size. Symmetric Mach-Zehender Interferometer structures provide the shortest switching window and highest flexibility [101].

Optical interconnection systems are the primitives in digital optical computing. These constitute various optical architectures and algorithms. OTA also takes an important role in this regard [102]. In the following section, advantages of semiconductor optical amplifier based MZI switch are extended by including optical tree architecture for the realization of all optical arithmetic and logical circuits.

5.2.1 SOA-MZI Switch

A Mach-Zehender Interferometer switch is shown in Figure 5.1. This is a powerful technique to implement ultra fast switching.

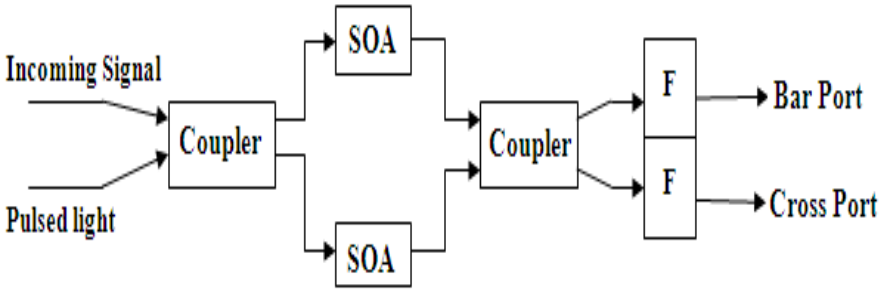


Figure 5.1: SOA–MZI based optical switch.

SOA is inserted in both arms of the Mach-Zehender Interferometer switch. Two couplers are used [20]. At the first coupler, the pulsed signal which is at the wavelength λ_1 is split in a way that more power passes through one arm of the MZI. At the same time, the continuous wave signal at the wavelength λ_2 propagates simultaneously in the two arms as it is split equally by this coupler. The continuous wave signal exits from the lower port known as cross port of SOA-MZI, in the absence of the λ_1 beam. However, in the presence of both the signals, all one bits are directed towards the upper port of the device known as bar port due to the change of the refractive-index caused by the λ_1 input signal. Cross phase modulation (XPM) is the physical mechanism behind this behavior. Carrier density inside one semiconductor optical amplifier is reduced due to saturation of gain induced by the λ_1 beam. This results in the increase of the refractive index only in the branch through which the signal passes. Thus, an additional phase shift is introduced to the continuous wave signal as a result of cross phase modulation effect. During each one bit, the wave is directed towards the bar port. For blocking the original λ_1 signal, optical filters are used in front of the output ports.

Thus, it is clear that the incoming continuous wave signal exits from the lower channel (cross port) of switch in the absence of input control signal (λ_1). No light appears in the upper channel (bar port) in this case. When the control signal is present, the incoming signal exits from the bar port of the device. In this case no light appears at the cross port

of the MZI. When there is no incoming signal present at the input, the filter will block the control signal. Thus no light will be present at cross port and bar port of the device.

5.2.2 Integrated Full Adder - Subtractor

Schematic diagram of all optical integrated full adder -subtractor is shown in Figure 5.2.

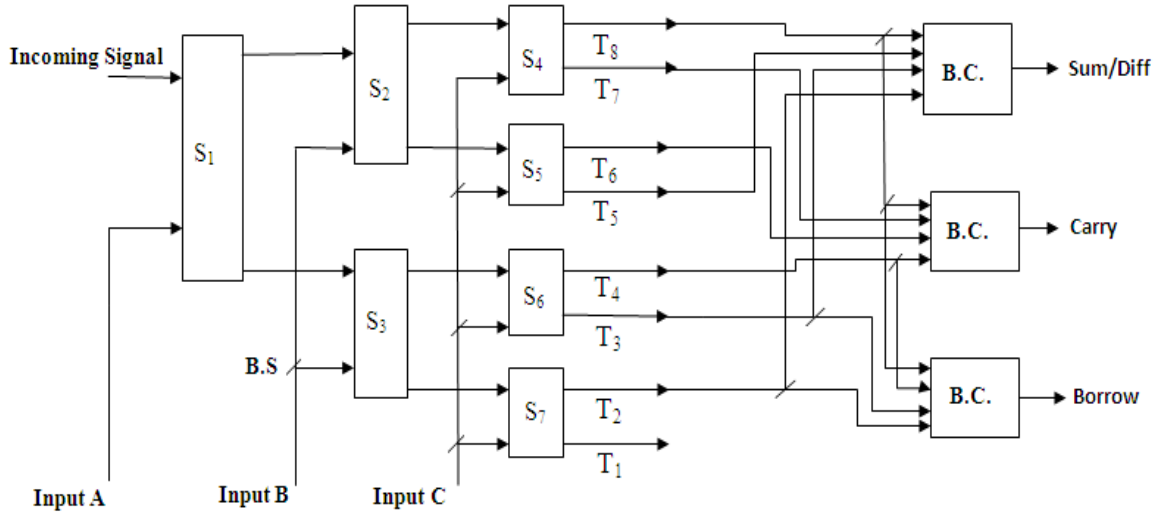
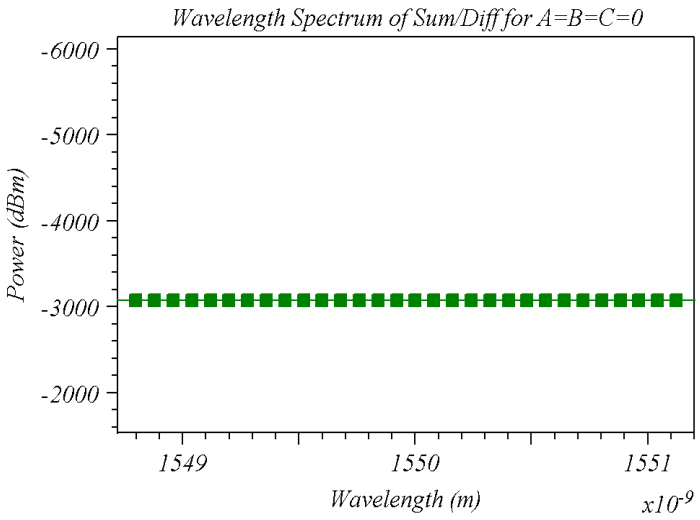


Figure 5.2 Schematic diagram of full adder-subtractor using SOA based MZI switches (BC: Beam combiner, BS: Beam splitter).

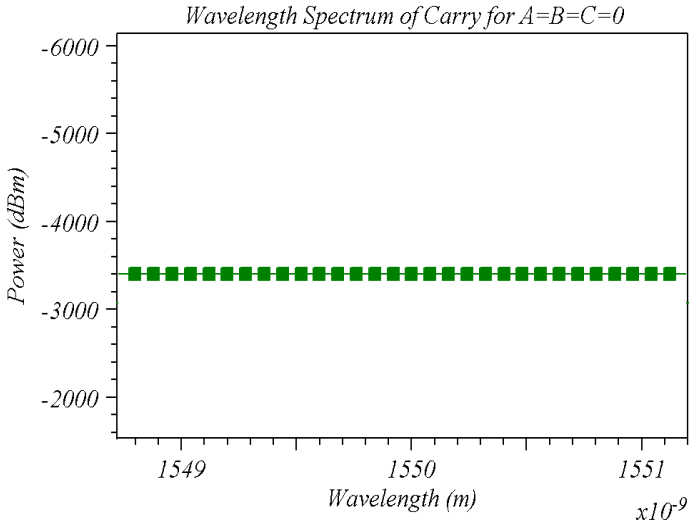
Four signal generators having a frequency of 40 GHz act as electrical sources for incoming signal and for three inputs of the integrated full-adder and subtractor. Direct modulated semiconductor lasers are directly modulated with the electrical signals. In the considered model lasers having wavelength of 1550 nm and 1500 nm act as incoming signal and control signal respectively. Lasers have 0 dBm of continuous wave power, 10 FWHM line width, ideal laser noise bandwidth, and laser random phase. A single MZI switch is formed by an input coupler followed by two semiconductor optical amplifiers and an output coupler and filters [Figure 5.1]. Outputs of the coupler are fed to input couplers of the MZI switches. The couplers have two output ports named as cross port and bar port respectively. Parameters of the coupling matrix and coupling coefficient α are optimized to obtain switching of the MZI. Both arms of the coupler are fed to the SOAs. Semiconductor optical amplifier is modeled as a travelling wave amplifier. Time dependent phase change caused by the coupling of the gain and index and the time dependence of the gain due to saturation effect is taken into consideration by SOA. The SOA is polarization independent with noise figure of 6dB, confinement factor of 0.15, 200mA of pump current, fast transient time and high nonlinearity.

Finally, outputs of the SOAs are fed to other optical couplers. The gaussian type filter with a bandwidth of 1e-10m is used for blocking the control signal at wavelength 1500 nm. Total seven switches are used, one in first stage, two in the second stage and four in the third stage. There are four MZI switches in third stage. Final outputs of these switches are applied to spectrum analyzers. These represent terminals T_1 through T_8.

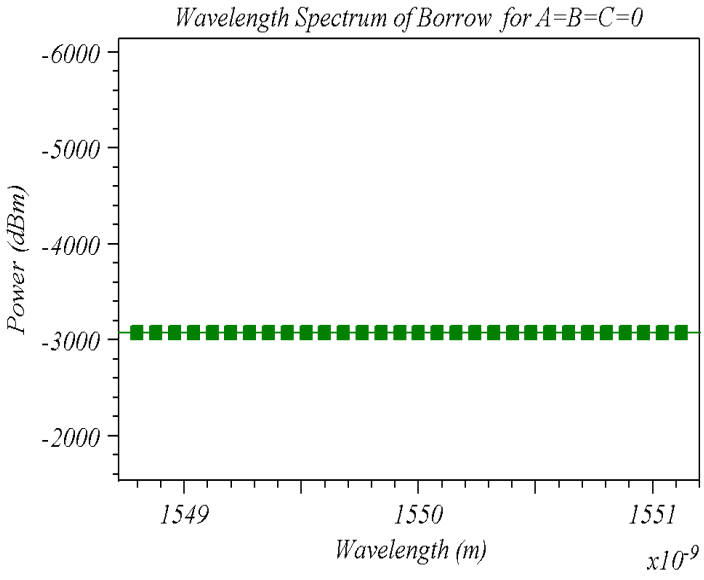
As per the switching operation of SOA-MZI switch, when A=B=C=0, incoming signal light is obtained at terminal T_1 and all other terminals are in off state. Thus T_1 represents logic $\bar{A}\bar{B}\bar{C}$. Similarly terminals T_2–T_8 give the logical operations of $\bar{A}\bar{B}C, \bar{A}B\bar{C}, \bar{A}BC, A\bar{B}\bar{C}, A\bar{B}C, ABC$ and ABC, respectively. As "sum'' as well as "difference" takes the expression $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$, therefore outputs of terminals T_8, T_5, T_3 and T_2 are combined to obtain the result. Combination of results at output of terminals T_8, T_7, T_6 and T_4 gives the result of ''carry''($\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$) in case of full-adder. Whereas the combination of terminals T_2, T_3, T_4 and T_8 gives the result of ''borrow'' ($\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$) in the full-subtraction case. There are eight different cases depending upon eight different input combinations.



(a)



(b)



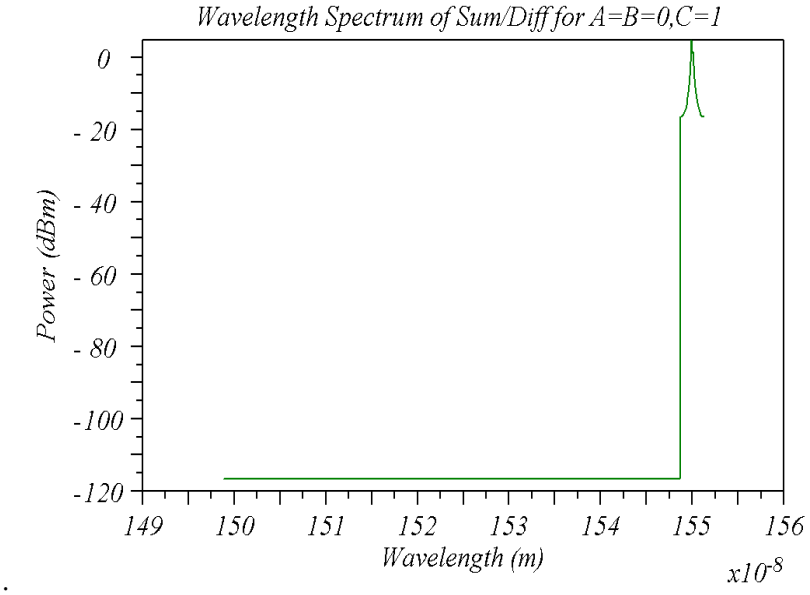
(c)

Figure 5.3: Wavelength spectrum for logic A=B=C=0 (a) "sum" and "Difference" (b) "carry" (c) "borrow".

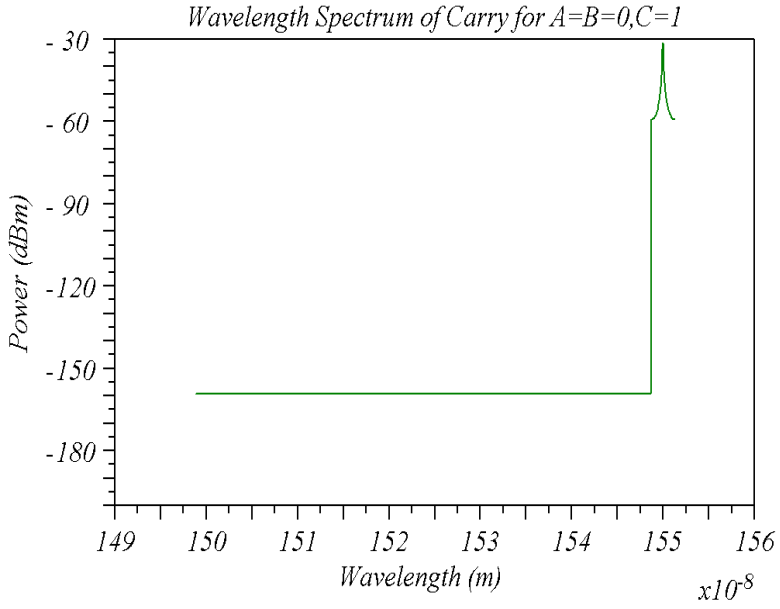
When A=B=C=0, output is high at T_1 but this output is not connected to "sum" ("difference"), "carry" and "borrow" so all three outputs give very low power (i.e. gives the 0 output) [Figure 5.3].

When A=0,B=0,C=1, light reaches at output terminal T_2, which contributes to the "sum" ("difference ") and "borrow" output but is not connected to "carry". Positive and negative output powers in the wavelength spectrum are considered as high and low respectively. Figure 5.4, shows the resulting spectrum for output of "sum" ("difference") and "borrow"

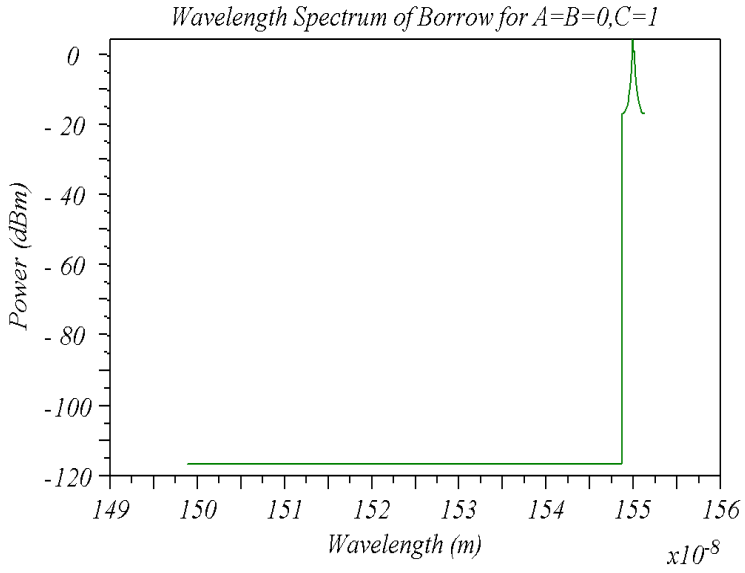
is high and for “carry” is low. Similarly, the three outputs are verified for other input combinations.



(a)



(b)



(c)

Figure 5.4: Wavelength spectrum for logic A=0, B=0, C=1. (a) "sum" and "difference".(b) "carry" (c) "borrow".

5.2.3 System Description of all optical decoder

A decoder is a type of combinational circuit. It converts binary information from n number of input terminals to 2^n unique output terminals. A 2 to 4 decoder is realized using three MZI switches. Figure 5.5 shows the schematic diagram of the device.

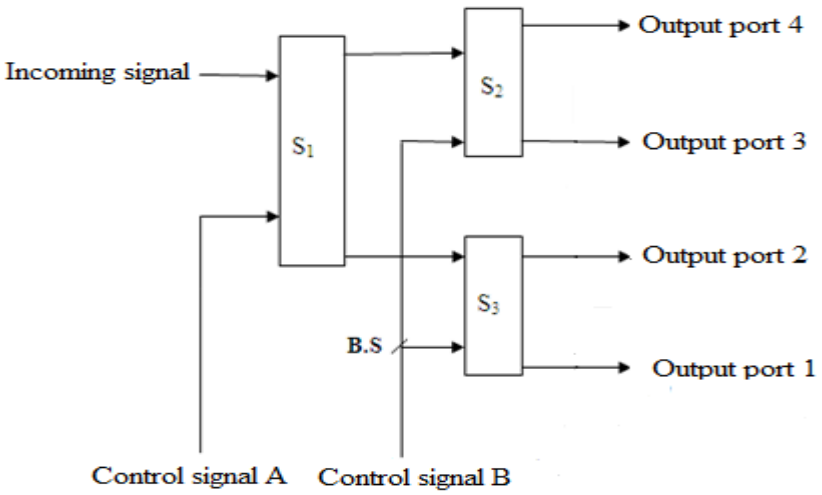
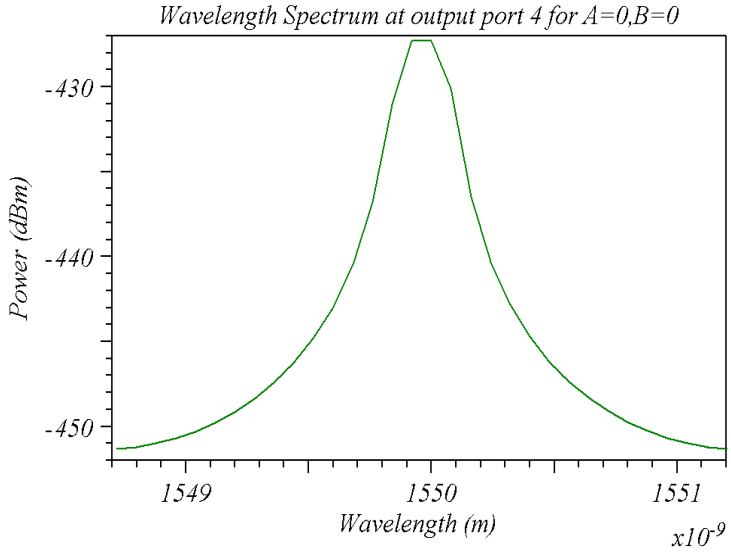
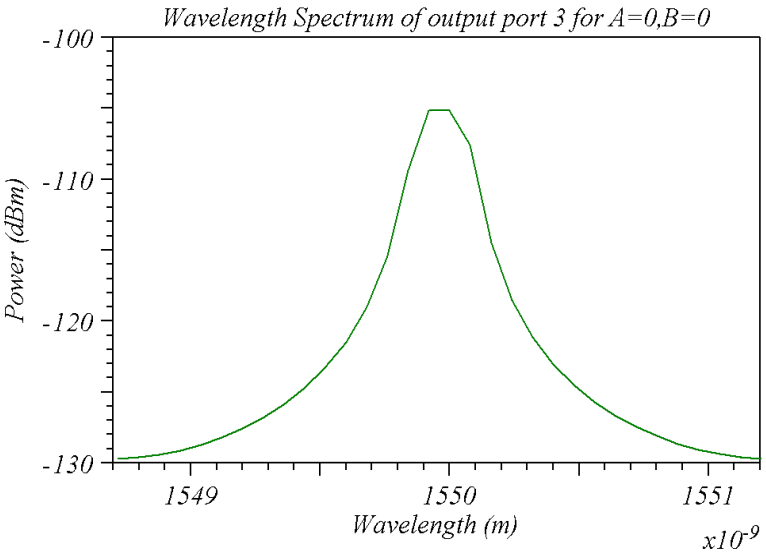


Figure 5.5: Schematic diagram of an all optical 2-to-4 decoder.

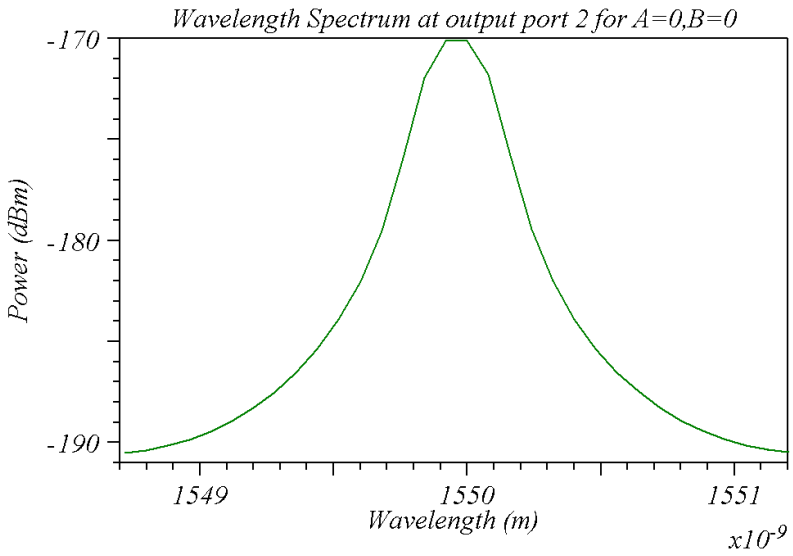
When A=0 and B=0, the light signal reaches at terminal T_1 (port 1). No light appears at the other output terminals i.e. T_2, T_3 and T_4 in this case. For this condition, optical spectrum at four output ports is depicted in Figure 5.6. It can be seen in the Figure that the positive peak of the spectrum is observed only at terminal T_1 while the spectrum peaks obtained at the remaining output terminals are less than -100dBm.



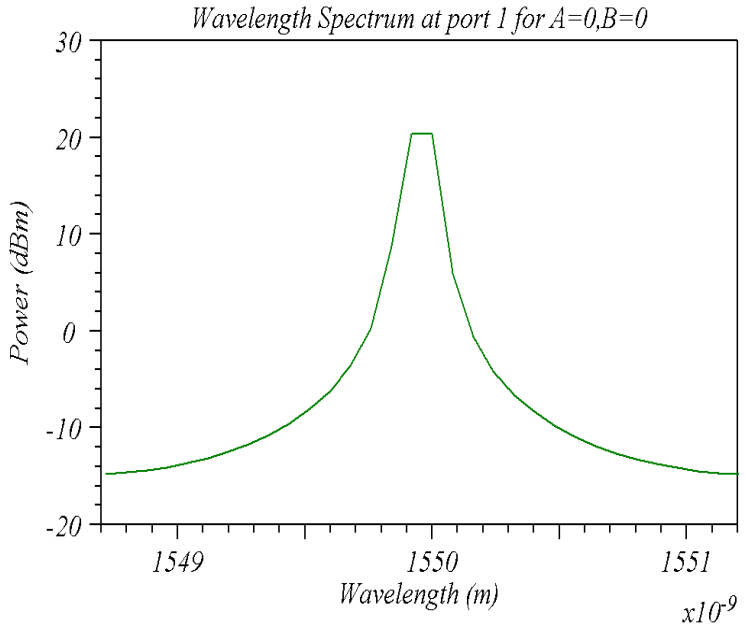
(a)



(b)



(c)



(d)

Figure 5.6: Decoder output at different output ports for the case of A=B=0. (a) Port 4 (b) Port 3 (c) port2 (d) Port1.

For the case A=0 and B=1, light signal output is present only at terminal T_2 (port 2). The positive peak of the spectrum is observed at this output terminal. Output at remaining ports is less than -60dBm. When A=1 and B=0, terminal T_3 (port 3) is in the logical high state while all other terminals are in the logical zero level. When logical 1 is applied at both the control signals, light output is observed at terminal T_4 (port 4). Peaks of the spectrum observed at all other remaining ports are less than 100dBm. Filters block the

control signal from reaching at the output. Therefore output optical spectrums are observed at 1550 nm. This is same as incoming signal wavelength.

5.2.4 System Description of Comparator

It is very essential for any computing system to determine whether a binary number A is equal to, less than or greater than another binary number B. For realizing the comparator three different output terminals are needed. First output is required to give $A\bar{B}$ operation, that indicates A is greater than B (A>B). The second output is needed to describe the equality between the two binary numbers i.e. A=B. This is achieved by boolean operation $AB + \bar{A}\bar{B}$. Third output need to provide a logical high state in the case when A is less than B (A<B). This corresponds to $\bar{A}B$ operation. Figure 5.7 shows the schematic diagram of an optical comparator.

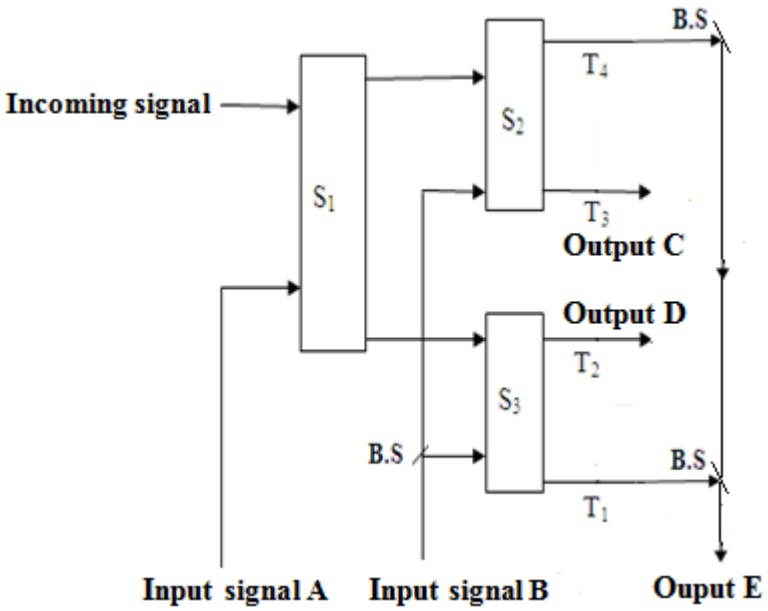


Figure 5.7: Schematic diagram of an all optical comparator.

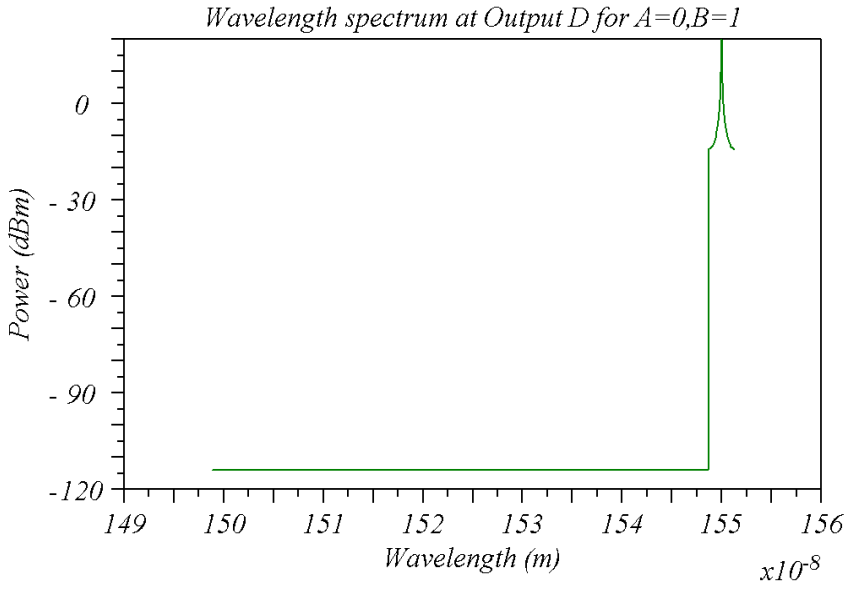
Direct modulated semiconductor lasers are directly modulated with the electrical signals. In the considered model lasers having wavelength of 1550 nm and 1500 nm act as incoming signal and control signal respectively. Lasers have 0 dBm of continuous wave power, 10 FWHM line width, ideal laser noise bandwidth and random phase. Outputs of the lasers are applied to optical couplers which have two output ports named as cross port and bar port respectively. Parameters of the coupling matrix and coupling coefficient α are optimized to obtain switching of the MZI.

Output of each arm of the coupler is applied to the SOAs. Semiconductor optical amplifier is modeled as a travelling wave amplifier. Time dependent phase change caused by the coupling of the gain and index and the time dependence of the gain due to the saturation effect is taken into consideration by semiconductor optical amplifier. For solving the rate equations for carrier density Runge Kutta technique has been used. The SOA is assumed to be polarization independent with noise figure of 6dB, confinement factor of 0.15, 200mA of pump current, fast transient time and high nonlinearity.

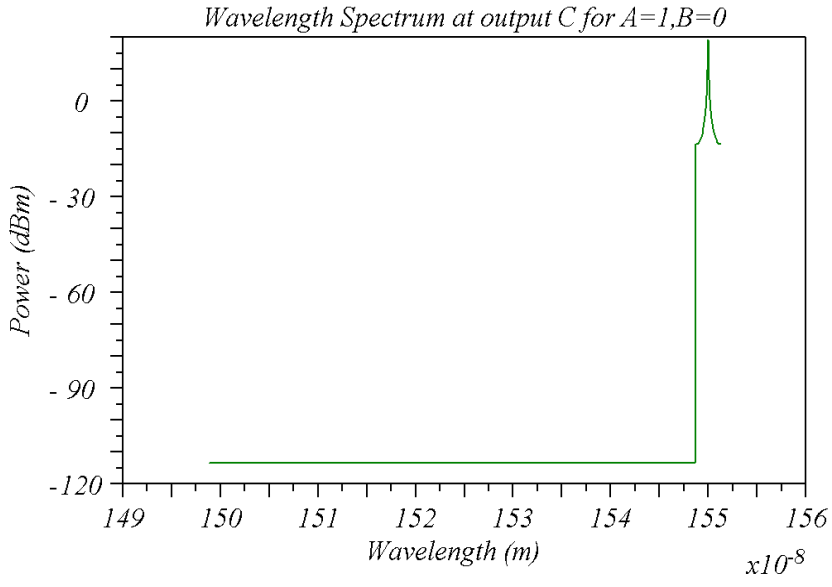
Finally, outputs of the SOAs are fed to the optical couplers in next stage. The gaussian type filter with a bandwidth of 1e-10m is used for blocking the control signal at wavelength 1500 nm. Thus a single MZI switch constitute of an input coupler, which is followed by two semiconductor optical amplifiers and an output coupler and filters. Total number of there switches are there. One of them is in the first stage. Second stage consists of two switches. Outputs of the MZI switches of second stage are applied to spectrum analyzers. These outputs constitute terminals T_1 through T_4 which give the logical operations $\bar{A}\bar{B}$, $A\bar{B}$, $A\bar{B}$ and AB.

Output C implements the AND logic function between $\bar{B}$ and A, i.e. C = $A\bar{B}$. Thus, A is greater than B is indicated by appearance of light signal at output terminal C i.e. terminal T_3. When A = 1 and B = 0, then light beam is expected only at output terminal C. No light is received at terminal C in any of the other cases i.e. A = 1, B = 1; A = 0, B = 1 and A = 0, B = 0. Thus it is clear that the light signal appears at the output terminal C only in the case of A>B.

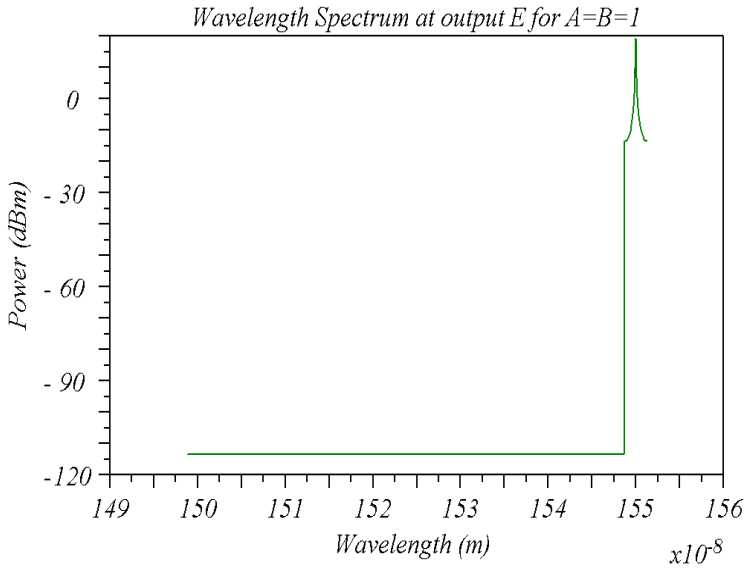
Similarly, A is less than B is indicated by the presence of light signal at the output terminal D i.e. terminal T_2. Logic operation E= $AB + \bar{A}\bar{B}$ is satisfied by the output E. Thus, light signal appears at output terminal E only in the case when either the two inputs are 1 (i.e. A = 1, B = 1) or 0 (i.e. A = 0, B = 0). In other two conditions, i.e. when A = 1, B = 0 or A = 0, B = 1, no light signal is received at output E. Thus light signal is received at output E only when A = B. Wavelength spectrums at the comparator outputs are shown in Figure 5.8.


Wavelength spectrum at Output D for A=0,B=1
0
- 30
- 60
- 90
-120
Power (dBm)
149
150
151
152
153
154
155
156
Wavelength (m)
x10-8

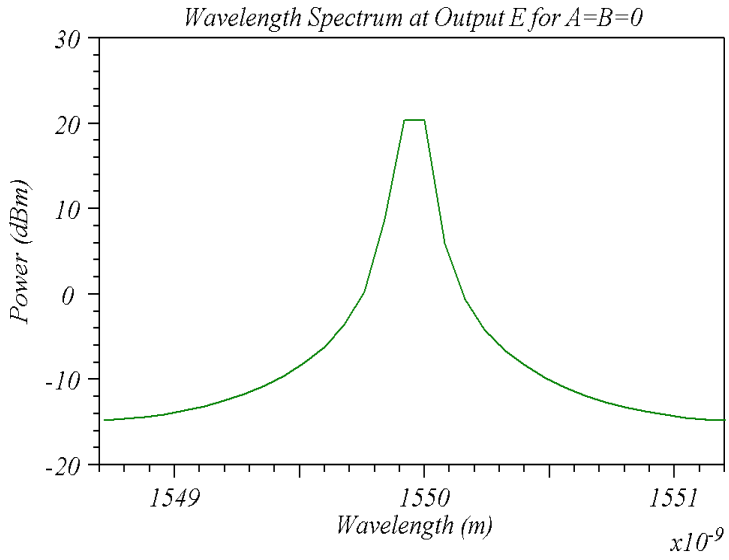
(a)


Wavelength Spectrum at output C for A=1,B=0
0
- 30
- 60
- 90
-120
Power (dBm)
149
150
151
152
153
154
155
156
Wavelength (m)
x10-8

(b)



(c)



(d)

Figure 5.8: Wavelength spectrum at the comparator outputs. (a) A<B (b) A>B (c) A=B=1 (d) A=B=0.

5.3 All optical Demultiplexer Operation based on SOA-MZI

It has been a challenge to increase the transmission capacities of optical fiber communication systems over the past few decades. Higher transmission capacities are still demanded as telecommunications systems keep on expanding over the years. This is very well known by the communication engineers that increase in the capacity of optical fiber communication systems can be achieved by either applying OTDM or WDM. A combination of both of these can also be used. Optical time division multiplexing is more economic than wavelength division multiplexing. This is due to the requirement of fewer

amounts of network management efforts and also due to the reason that existing narrow-band and single band EDFAs can operate and do not require to be replaced by the amplifiers with broad bandwidth [103].

Thus, for generating a signal at 40 Gb/s for example, it will be more convenient to utilize a single optical time division multiplexing channel with a data rate of 40 Gbit/s rather than using 4×10 Gb/s wavelength division multiplexing signal. This is especially due to the reason that test equipments at 40 Gb/s (i.e. bit error rate tester) are available commercially. Optical time division multiplexing transmission at 40 Gb/s is still subject to research and development although greater capacities could be achieved by using wavelength division multiplexing of multiple 10 Gb/s optical signals [104], [105].

In the recent years QD-SOA assisted MZI [106], PPLN waveguides [107], electrically driven electro absorption modulator (EAM) [108], and a silicon nanowire based on four wave mixing [109] have been used to carry out OTDM operations at data rates up to 160 Gb/s.

Performance of an optical time division multiplexing system depends largely upon the switching characteristics of the demultiplexer used in the system. Therefore, extensive study has been carried out to analyze the performance of different types of demultiplexing switches. Based on the investigations, it has been observed that semiconductor optical amplifier based Symmetric-Mach–Zehnder (SMZ) configuration is most suitable among the different types of switches. This is due to the thermal stability, compact size, and low power operation of the device. Symmetric-Mach–Zehnder is less venerable to jitter as it has a symmetric switching window [110], [99].

Information can be carried by data bits which are shaped into either NRZ or RZ optical pulses. Optical time division multiplexing systems utilizing RZ format are of interest in high speed backbone optical links, due to short duration [111] and long time usage efficiency of return-to-zero format [112]. OTDM requires the use of short RZ pulses. Therefore the bandwidth of the signal spectrum is very broad. This makes the optical time division multiplexing signals spectrally inefficient as well as highly sensitive to the dispersion. These issues would be alleviated with the use of ultra-high speed signals modulated with non return-to-zero modulation format. Timing jitter tolerance will be increased in the process of demultiplexing thanks to their better resilience to dispersion, as well as flat top, and increased spectral efficiency [113]. Thus both RZ and NRZ modulation formats are being used in optical time division multiplexing systems based on the type of application and their suitability.

In this Section, SOA-MZI based optical time division demultiplexing operation is analyzed for NRZ and RZ modulated signals at data rates from 40 to 160 Gbps.

5.3.1 Principle of SOA-MZI based Demultiplexing Switch

The following basic interferometric equation describes the output signal of a semiconductor optical amplifier based MZI switch:

$$P_{\text{out}}(t) = \frac{P_{\text{in}}(t)}{4}\left\{G_1(t) + G_2(t) - 2\sqrt{G_1(t)G_2(t)}\cos(\emptyset_1(t) - \emptyset_2(t))\right\} \quad (5.1)$$

$P_{\text{in}}(t)$ represents the input data signal. When no control signal is present, the Mach–Zehnder is balanced. Thus all the data signals injected into the device will be sent to the reject port i.e. cross port of the MZI.

When two control signals are present, the data signals in the both branches of the MZI interfere within the device. Data signals experience a phase shift, $\emptyset_{12}(t)$, and time-dependent gain, $G_{1,2}(t)$, as they traverse the semiconductor optical amplifiers. By properly maintaining the timing of control pulses, asymmetry may be introduced within the MZI. Thus data signals in the two branches may be made to experience different responses. This results in switching of the input data signal to the bar port i.e. output port of the MZI. The phase shift and gain experienced by signals travelling through the semiconductor optical amplifiers may be described by the following equations [114]:

$$G_{1,2}(t) = G_{\text{o}} - \Delta G \int_{-\infty}^{\infty} h_{1,2}(t')P_{\text{clk}}(t'-t)dt' \quad (5.2)$$

$$\emptyset_{1,2}(t) = \Delta\emptyset \int_{-\infty}^{\infty} h_{1,2}(t')P_{\text{clk}}(t'-t)dt' \quad (5.3)$$

The variable $h(t)$ represents the impulse response of the semiconductor optical amplifier. Whereas $P_{\text{clk}}(t)$ represents the input control signal. Initial gain of the semiconductor optical amplifier is represented by G_{o}. When the control pulse propagates through the semiconductor optical amplifier, there is a change in phase and the gain of the amplifier. The change in phase or gain is represented by $\Delta\emptyset$ and ΔG respectively. The impulse response when the control and data signals traverse simultaneously is given by:

$$h_{co}(t) = \emptyset(t)exp\left(\frac{-t}{\tau_{SOA}}\right) \quad (5.4)$$

$\emptyset(t)$ is the step function. This function takes into account the situation when the data signal is either trailing or leading the control pulse. τ_{SOA} is recovery time constant of the

dominant semiconductor optical amplifier. $h_{co}(t)$ represents the impulse response of both data signals within the SMZ configuration. Differential phase and gain evolution results due to convolution of control pulses with each response as described by equations (5.3) and (5.2) respectively. Equation (5.1) is then used to determine the interferometer switch output. Effective switching offset delays the impulse responses from one another. Δt_{cs} represents the temporal control pulse separation of the signals Control 1 and Control 2 before entering the interferometer. It determines the nominal switching window of the MZI switch such that $\tau_{win} = \Delta t_{cs}$.

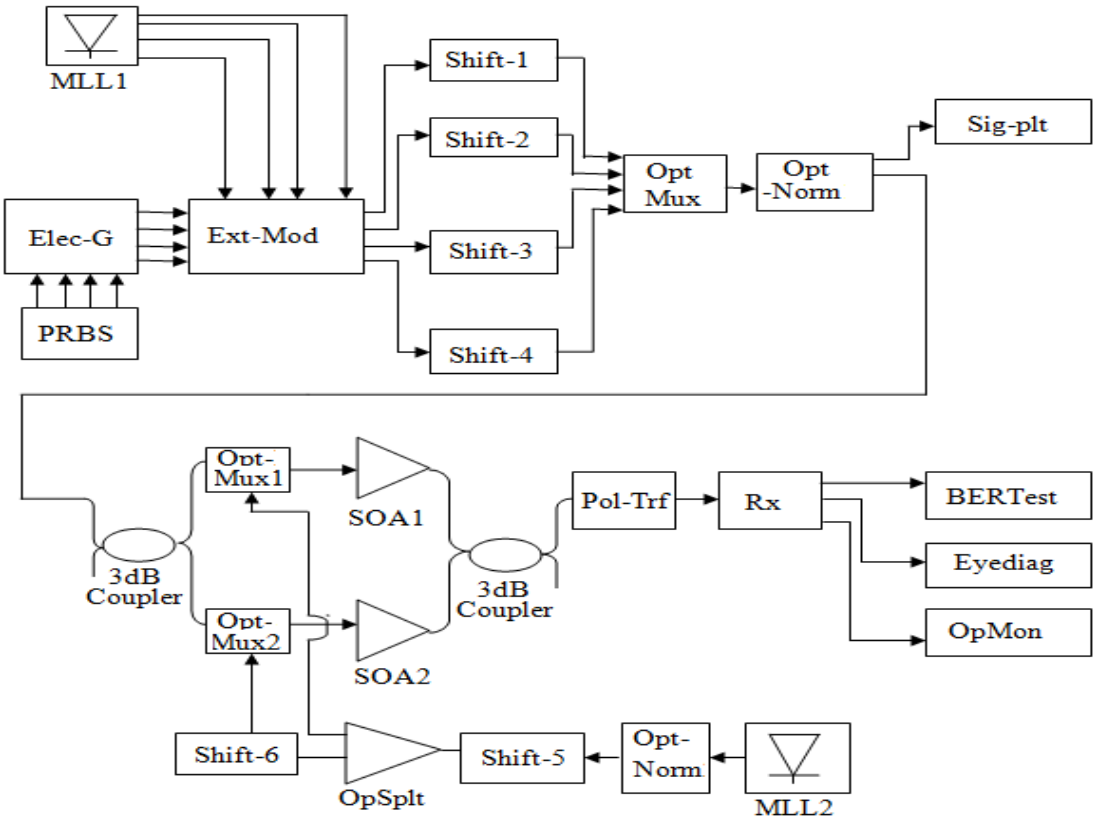


Figure 5.9: System Configuration.

5.3.2 System Setup

Figure 5.9 shows the system configuration. TDM transmitter consists of a mode locked laser diode, PRBS generator, an electrical generator, an optical multiplexer, four blocks for time shifting, and an optical normalizer. Four signals at 1550 nm wavelength are modulated using NRZ / RZ-format with different pseudo-random binary sequence patterns. The channels have a 3-dB pulse width equal to (ch_window × 0.2) ps. The channels have same 'bit_rate' and power. Each consequent channel is delayed by the time

period equal to the ‘ch_window’ before being multiplexed together. Its value is equal to 1/4 of the reciprocal of the ‘bit_rate’. An optical normalizer controls the total power of all the channels. Average output power of optical time division multiplexing signal is determined by this.

The demultiplexer comprises of an optical normalizer, a symmetric SOA-MZI switch having two output ports, pulse splitter, a linear polarizer block, two blocks for time delay and a mode locked laser diode

Mode locked laser diode generates a pulse sequence with a ‘bit_rate’ which is same as that of the sequence used at the transmitter side. Shift -5 represents the first time delay block. This sets the control signal for demultiplexing of the channel of interest. Thus, if channel 1 is required to be demultiplexed, time delay may be set to zero. Time delay is set to be equal to (‘ch_window’ × 1) ps if channel 2 is required to be demultiplexed, and so on. Prior to coupling it with data signal in two branches of symmetric interferometer, control signal is split in two parts. Shift -6 represents the second block for the time delay. This block sets the duration of the switching window, which is set to be equal to the duration of the data pulse, (ch_window × 0.2) ps. Thus, time delay between two control pulses is set to be equal to the duration of the switching window, which is same as the width of the time division multiplexing channel. Control signal power is set to be 9dB higher than the power of the data signal. Polarization state of control signal is adjusted to be orthogonal to that of the data signal.

Symmetric MZI comprises of two SOAs, two 50/50 couplers and two multiplexers. Upper input is used to inject the signal data into SMZ. SMZ consists of two output ports named as “switching” (output) port and “reflective” port respectively. To pass the switched data signals and reject the control signal, a polarization filter is utilized at the receiver. Only data signals will be used as inputs to the receiver blocks. BER meter, optical monitor and eye diagram analyzer are placed at the receiver to take the results.

5.3.3 Results and Discussion

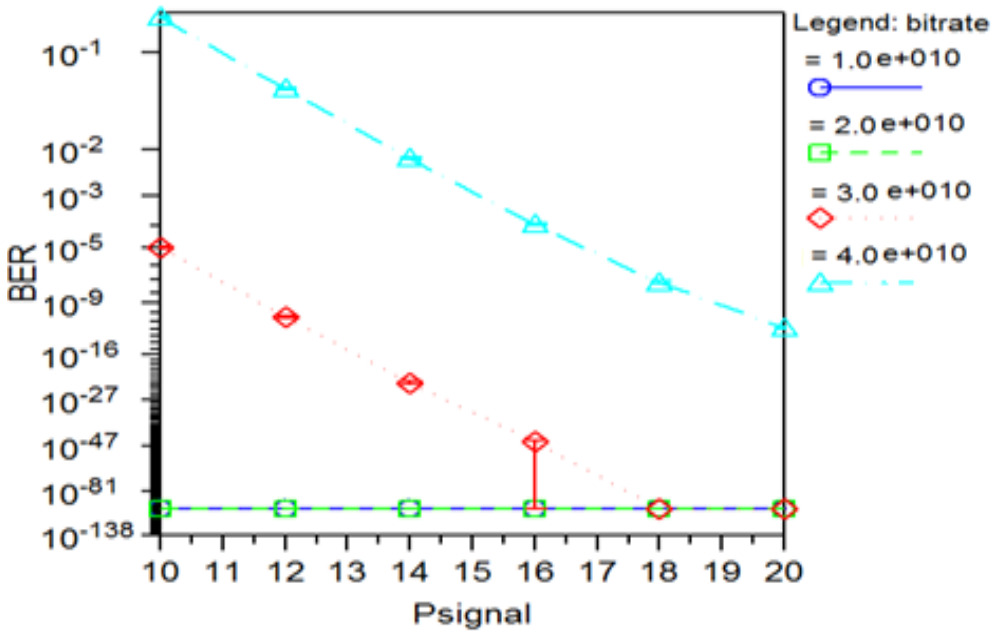
The system shown in Figure 5.9 is simulated using simulation parameters shown in Table 5.1. Noise and distortion affect performance of digital transmission. Bit errors are caused by the noise at the receiver. Distortion results in the alteration of the pulse shape causing ISI. Bit errors are also produced by Intersymbol interferences (ISI). In addition to bandwidth, BER is the major parameter characterizing a digital optical link. Extinction

ratio of the output signal should be high so that the logical 'Zero' (0) state can be easily distinguishable from logical 'High' (1).

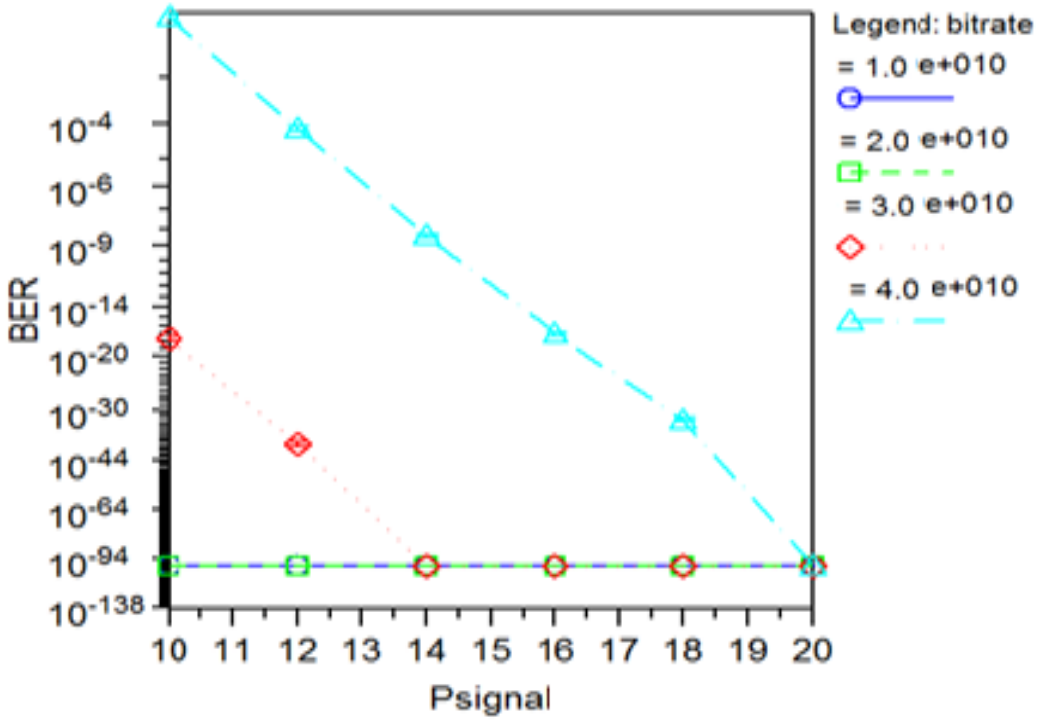
Table 5.1: Simulation parameters.

bit_rate (Gbps)	multiplexd data rate (Gbps)	ch_ window (ps)	Pulse_ width (ps)	Shift -1(ps)	Shift -2(ps)	Shift -3(ps)	Shift -4(ps)	For demultip - lexing of Channel- 1	
								Shift 6(ps)	Shift -7(ps)
10	40	25	5	0	25	50	75	0	5
20	80	12.5	2.5	0	12.5	25	37.5	0	2.5
30	120	8.33	1.68	0	8.33	16.6	25	0	1.68
40	160	6.25	1.25	0	6.25	12.50	18.75	0	1.25

First, the effect of control signals power, signal power 'P_{signal}', and pattern length is investigated on extinction value and bit error rate (BER) of the demultiplexed channel at different data rates. Further, demultiplexing operation of a 40Gb/s signal from a 160 Gb/s multiplexed signal has been demonstrated for RZ and NRZ modulated signals. Impact of variation of the width of the pulse on bit error rate is also investigated.



(a)



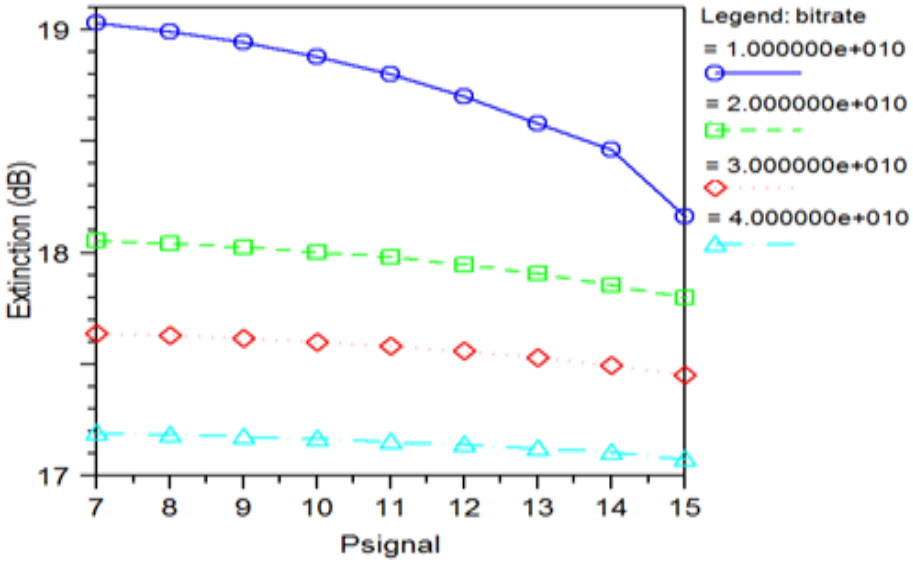
(b)

Figure 5.10: BER as a function of input signal power for different data rates (a) RZ; (b) NRZ.

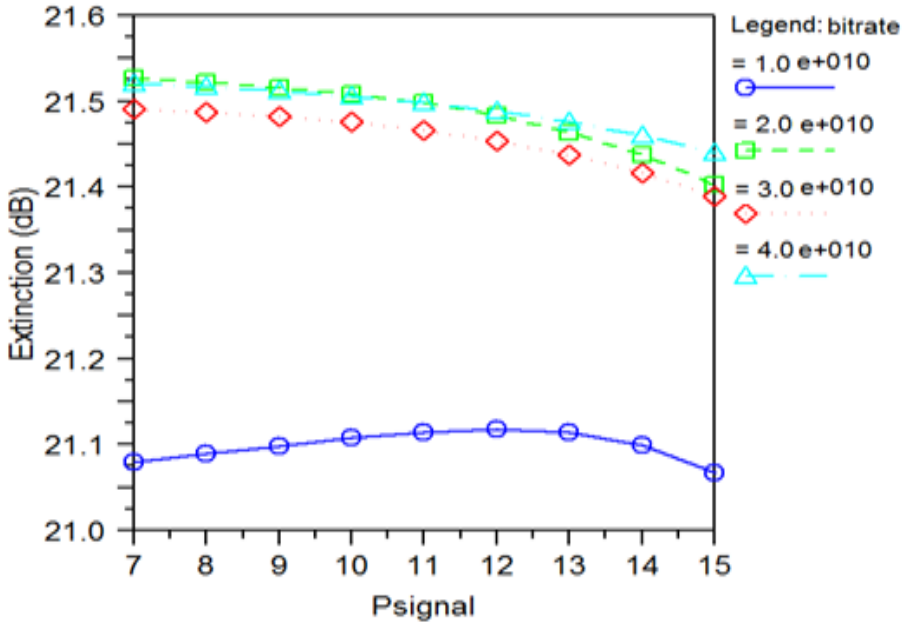
A. The impact of input signal power

Figure 5.10 shows the bit error rate of the demultiplexed channel at different data rates. Error free operation with a bit error rate of 10^{-94} is achieved at 10dBm of input signal power in the case of demultiplexing operation at 80-20 Gb/s and 40–10Gb/s respectively. For achieving the same bit error rate performance at 120-30Gb/s demultiplexing, power of input signal is required to be increased to 18 dBm for the case of return to zero modulated signals. This is 4dBm larger than the non return to zero case. Bit error rate of a digital optical receiver is inversely proportional to signal to noise ratio, which in turn depends upon optical signal power. Thus there is a decrease in the bit error rate with increase in the input signal power.

For further increase in the data rate, i.e for demultiplexing of 40Gb/s channel out of a 160Gbp/s multiplexed signal, similar bit error rate is achieved in the case of NRZ signals at the of input signal power of 20dBm. Minimum bit error rate obtained for RZ case is 10^{-9}. Extinction ratio of the demultiplexed channel is in the range of 21-21.5dB for the NRZ case. As seen in the Figure 5.11, there is a 3-5dB improvement in the extinction value as compared to the RZ case.



(a)



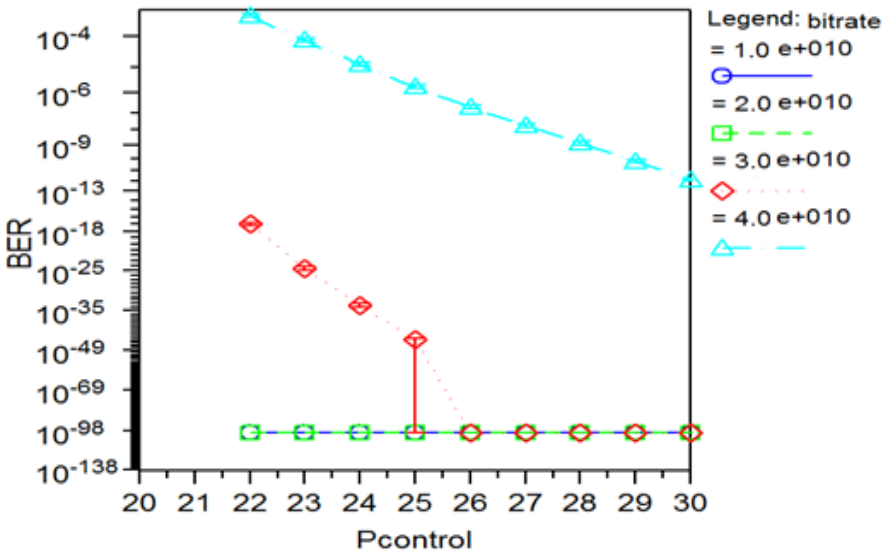
(b)

Figure 5.11: Extinction values as a function of input signal power for different data rates (a) RZ; (b) NRZ.

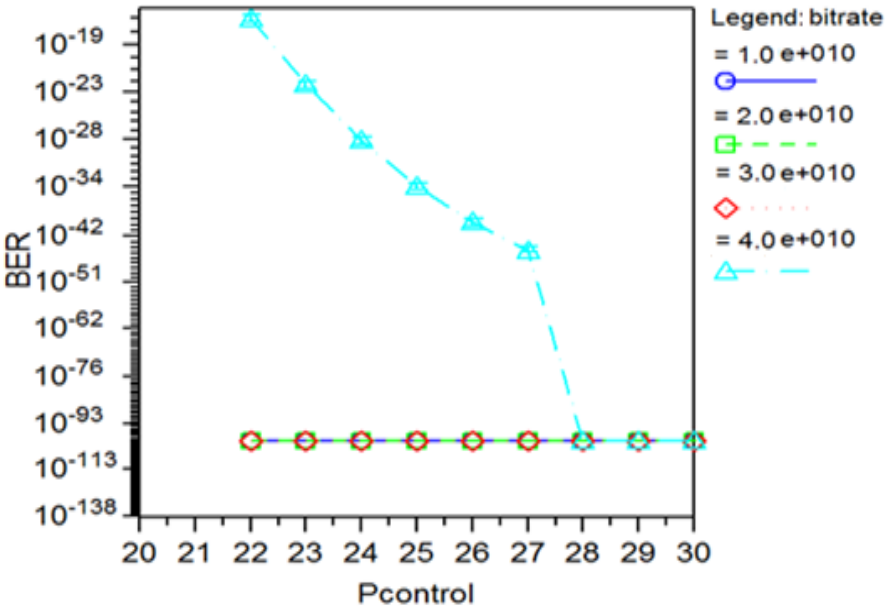
B. The Control signal power

Performance of an SOA-MZI is significantly affected by the power of control signal. Thus, one of the core issues is to investigate the performance of the receiver with the variation of control signal power. As shown in Figure 5.12, demultiplexing operation at data rates of 80 Gb/s and 40Gb/s gives a very low BER~10^{-100} at 22 dBm of '$P_{control}$' . A similar performance is observed for the NRZ case at 120 Gb/s. In the return to zero case, control signal power is required to be increased to 26dBm for operation at this data rate.

At 160 Gb/s data rate minimum bit error rate observed for non return to zero and return to zero signals is 10^{-100} and 10^{-11} at control signal power of 28 and 30dB respectively. Extinction ratio of the demultiplexed signal increases with the increase in the '$P_{control}$'. It comes out to be better in the non return to zero case for a given data rate and '$P_{control}$' values. As shown in Figure 5.13, extinction ratio lies between 14-18 (RZ) and 19.5-21.5dB (NRZ) for the input control signal power lying in the range of 25-30dB.

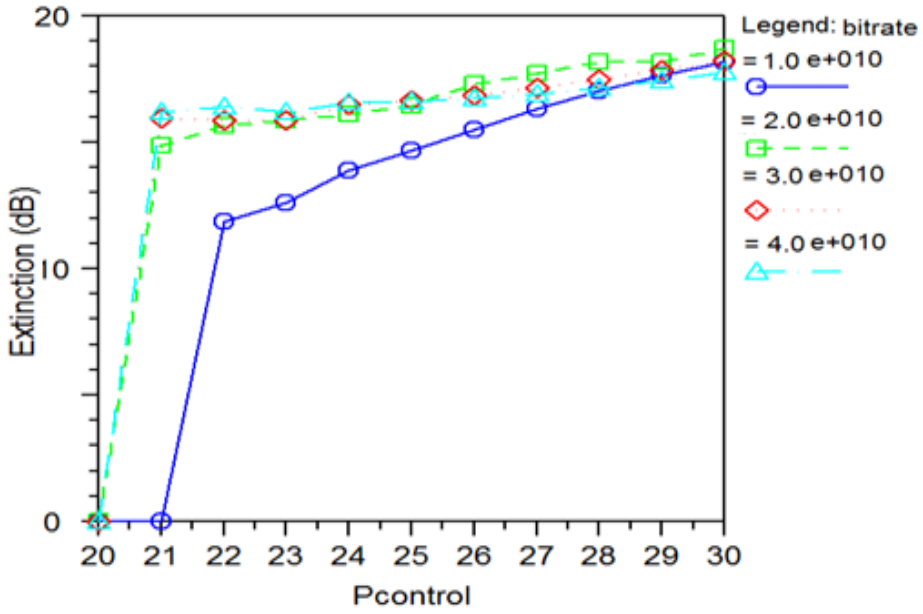


(a)

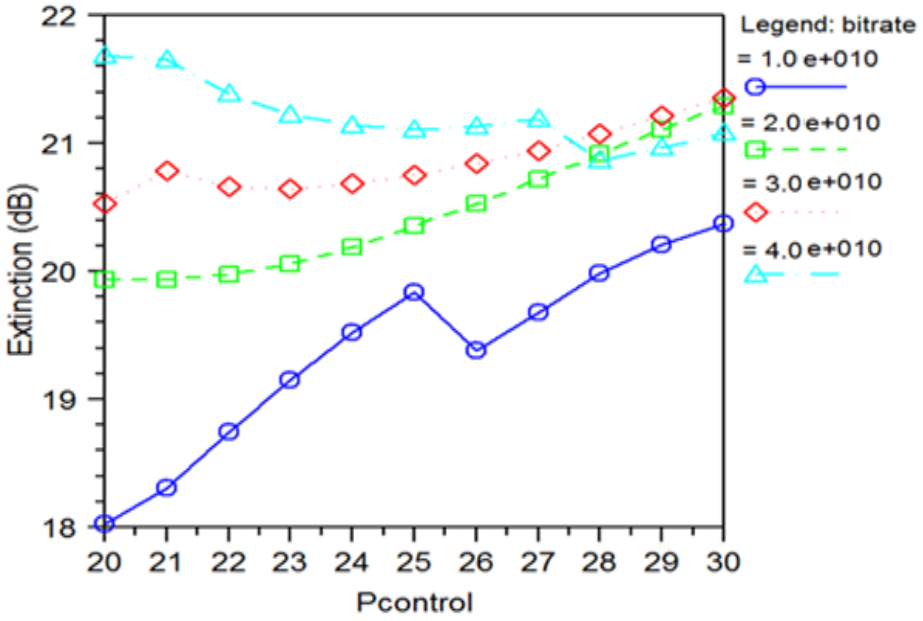


(b)

Figure 5.12: BER as a function of control signal power at different data rates (a) RZ; (b) NRZ.



(a)



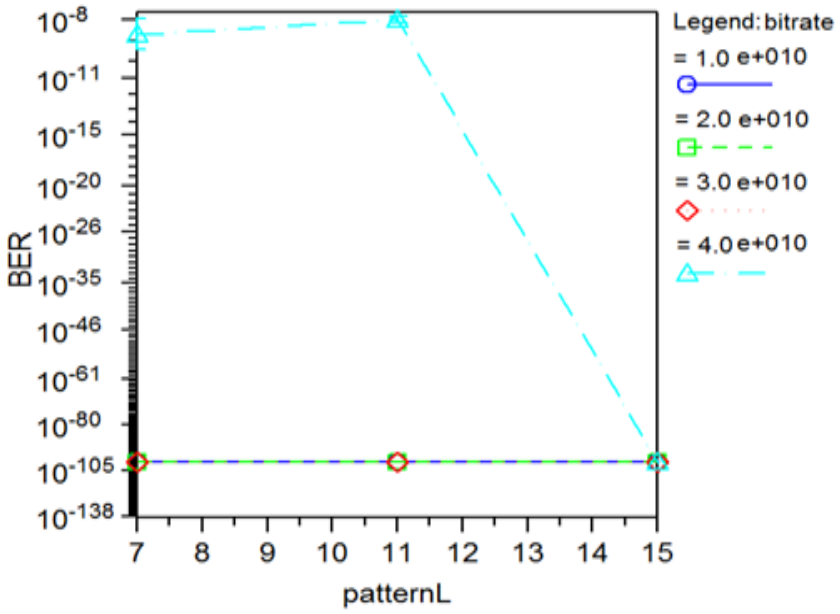
(b)

Figure 5.13: Output extinction value versus control signal power at different data rates (a) RZ; (b) NRZ.

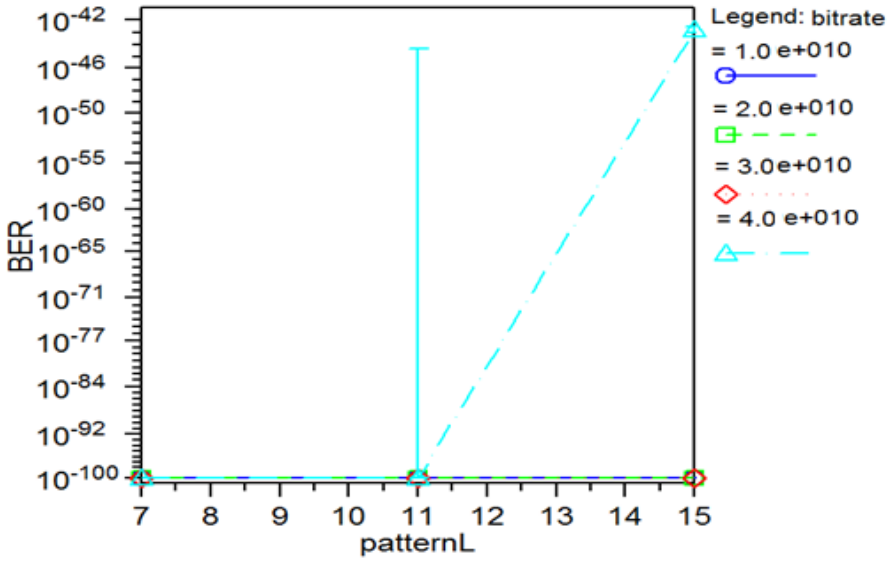
C. The Pattern Length

For verifying the tolerance against pattern induced degradations, bit error rate performance of the demultiplexed channel has also been investigated for different PRBS pattern lengths. Bit error rate has been examined for both the modulation formats at different data rates. Different pseudo-random binary sequence pattern lengths considered are 2^7-1, 2^{11}-1 and 2^{15}-1 respectively. Figure 5.14 shows that the bit error rate curves for

the non return to zero modulated signal at different pseudo-random binary sequence pattern lengths are close to each other. Bit error rate curves for the return to zero case show that there is a variation in the bit error rate at 160Gb/s data rate for different values of pattern lengths. Bit error rate observed for the pattern lengths of 2^{15}-1, 2^{11}-1 and 2^{7}-1 is 10^{-105}, 10^{-8} and 10^{-9} respectively. It shows that the use of non return to zero format may mitigate the pattern-dependent degradations in a SOA-MZI switch for operation at higher data rates.



(a)

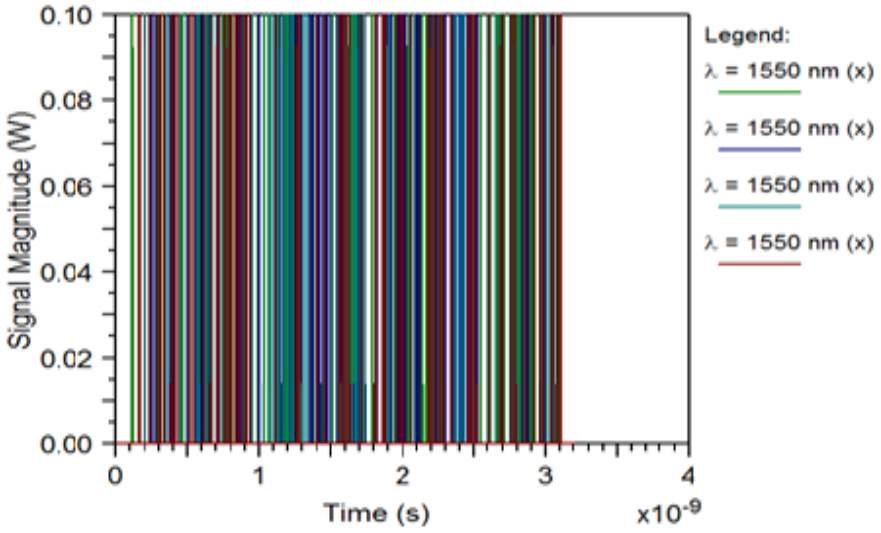


(b)

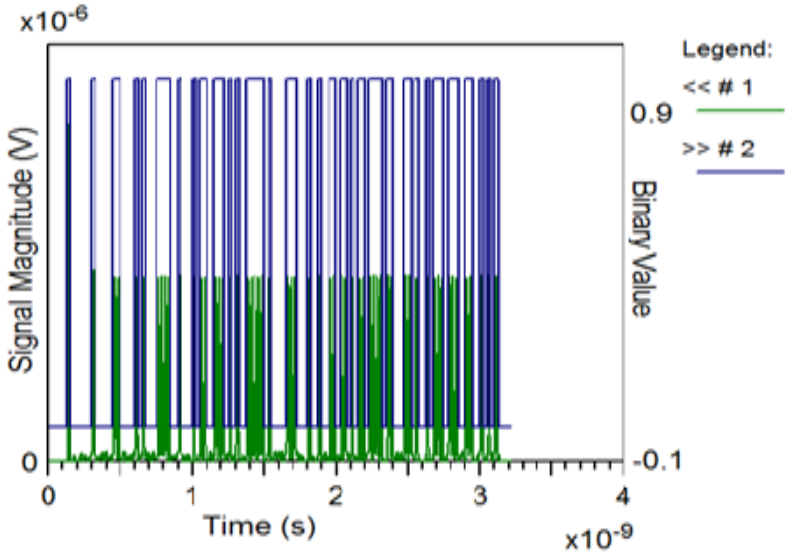
Figure 5.14: BER versus pattern length for different data rates for (a) RZ; (b) NRZ.

D. 160 Gb/s-40 Gb/s demultiplexing

Figure 5.15 (a) shows the output of 4 × 40 Gb/s TDM transmitter. Figure 5.15 (b) shows the zoom in details of the signal, after passing the signal through a linear polarizer. It is aligned with bit pattern of demultiplexed signal (channel 1 at 40 Gb/s). As seen in Figure 5.10 & 12, an error free demultiplexing operation is achieved at this data rate. Extinction value of the output signal observed in the case of NRZ and RZ modulated signals are 21.5 dB and 17dB respectively (Figure 5.11 & 5.13). No pattern induced degradation is observed for the NRZ case, in the demultiplexed channel. Bit error rate error floor appears in the case of return to zero modulated signals for different values of pattern lengths (as seen in Figure 5.14).



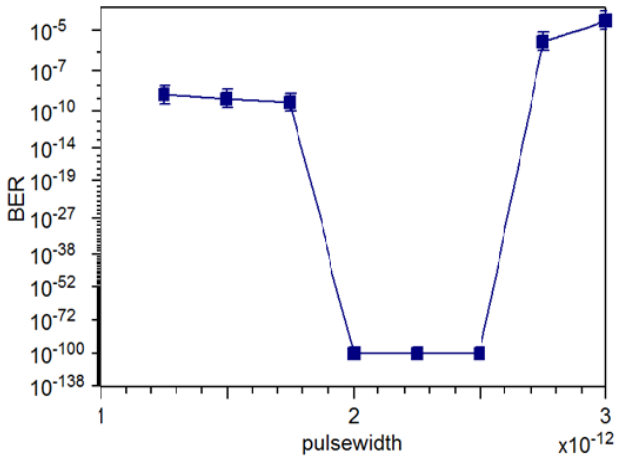
(a)



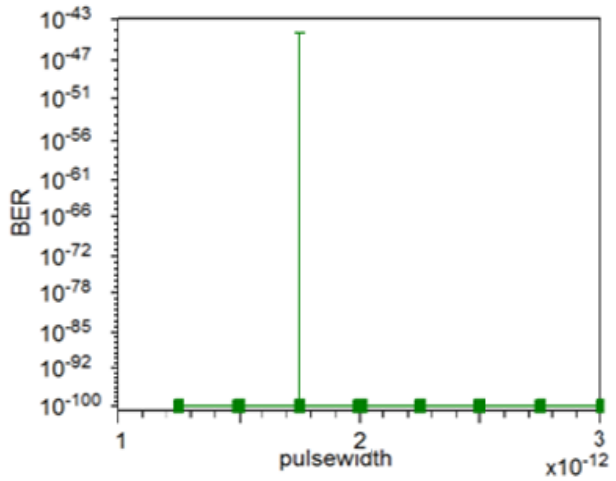
(b)

Figure 5.15: (a) Signal at the output of the multiplexer of TDM transmitter; (b) Zoom-in of SMZ output pulses at switching port aligned with bit pattern for channel1.

Further in Figure 5.16 the effect of variation of the width of the pulse on bit error rate is observed for demultiplexing at 160Gb/s-40Gb/s. Input signal pulse width is varied within the range of 1.25ps-3ps. Bit error rate of non return to zero modulated signals is independent of width of the pulse in this range. For the return to zero signals bit error rate varies, and minimum value is obtained for width of the pulse within bounds of 2 ps-2.5ps.



(a)

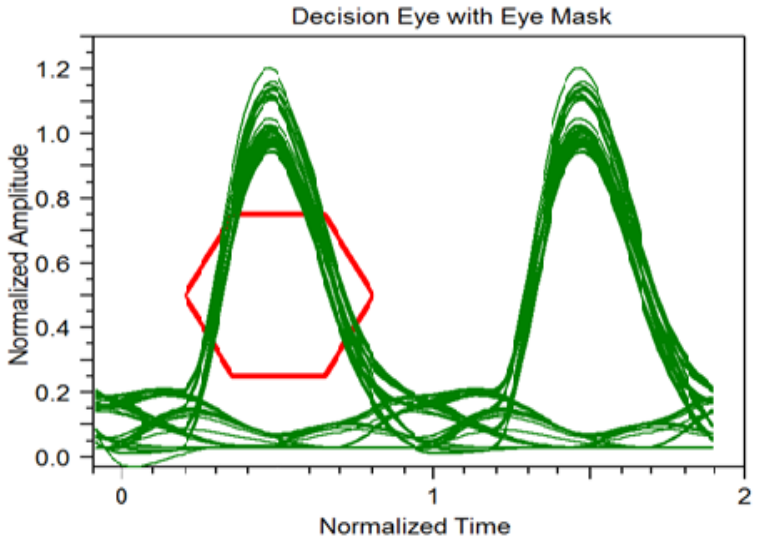


(b)

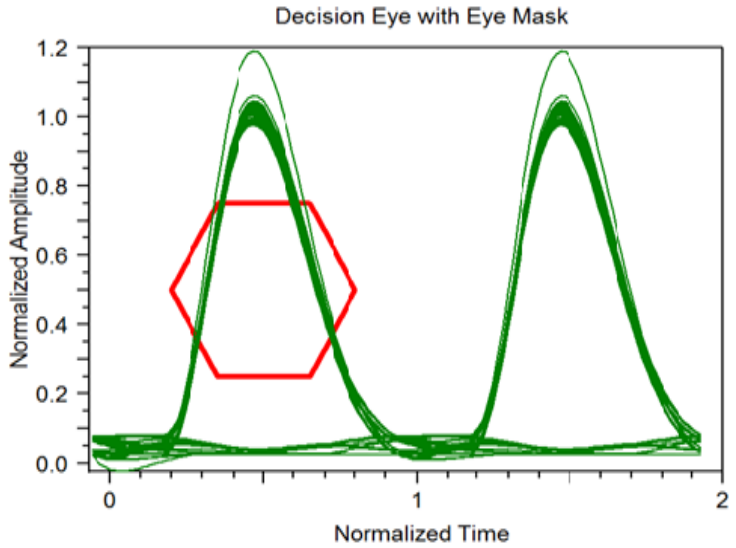
Figure 5.16: (a) BER as a function of pulse width for demultiplexing operation at 160Gb/s-40Gb/s (a) RZ; (b) NRZ signals.

Finally, Figure 5.17 shows the eye diagrams at the receiver in the case of return to zero and non return to zero modulated signals. It can be seen that the output signal at switching

port carries data information of demultiplexed channel. Other channels are nicely suppressed. Interferences from other channels are negligible.



(a)



(b)

Figure 5.17: Eye diagrams of output optical signals at switching port of the Receiver (a) RZ; (b) NRZ.

5.4 Conclusion

In this chapter, different functions of all optical digital signal processing are realized by employing nonlinear effects in a SOA. The all-optical realizations of adder, subtractor, comparator, demultiplexer, decoder etc are based on SOA-MZI. Numerical Simulations confirming the described logic devices have been presented for different input combinations.

Any complex logical function can be implemented and realized by combining beam combiners, beam splitters, and cascading different SOA-MZI switches. The scheme can be extended for any large number of input digits by suitable branch selection and by horizontal and vertical extension of the tree.

In further investigations, SOA-MZI based all optical demultiplexer operation has been analyzed in demultiplexing of an optical time division multiplexing channel at data rates up to 160 Gb/s. Demultiplexed channel shows a 3-5dB improvement in the extinction ratio for the non return to zero case at different data rates. Pattern induced degradation is observed to be negligible in the case of non return to zero modulated signals. Variation in the bit error rate performance at 160 Gb/s demultiplexing operation is observed in the case of return to zero modulated signals for different pattern lengths. Error free operation is achieved for both types of modulated signals and minimum bit error rate obtained for return to zero case is less than 10^{-9}. Bit error rate performance of non return to zero signals is independent of the width of the pulse in the range of 1.25-3ps. It varies significantly for the RZ case with minimum obtained for the value of the pulse width lying within the bounds of 2-2.5ps.

Chapter 6

Conclusions, Recommendations and Future Scope

6.1 Conclusions

All optical ultra fast signal processes such as optical arithmetic and logic processing, label swapping, pattern matching, parity checking, digital algebra and de-multiplexing play a critical role in the development of ultra fast photonic network architectures. All-optical regenerators, wavelength converters, packet switches and all optical memory are amongst the other key components for the future optical networks.

All optical Gates, optical arithmetic and logic circuits, flip-flops, counters and registers form important subsystems of these components. These devices have been investigated as they are integral components for optical computing and all optical processing in next generation optical networks.

This thesis focus on the design and investigation of all optical arithmetic and logical devices which can provide better performance (in terms of simple structure, operation at multi Gb s^{-1} speeds, photonic integration etc.) for future all optical networks.

The major results obtained from this study are summarized as follows:

1. An optical gate architecture is proposed to perform AND, OR, NOT and NOR logic gates using a single SOA. All optical logic operations are simple and reconfigurable and are implemented using RZ modulated signals at 40 Gb/s operational speed. Contrast ratio and extinction ratio values have also been analyzed for the above mentioned logic gates. Maximum extinction ratio and contrast ratio achieved are 19dB and 17.2 dB respectively, which is more adequate for all optical logic based information processing. The proposed logic gates have a very simple structure and as they are based on the semiconductor technology allow for photonic integration.
2. A simple and new scheme is proposed for all-optical SR and D flip-flop employing XGM effect in two wideband semiconductor optical amplifiers. Flip-flop operation is verified for several non complementary and complementary set and reset pulse signals confirming successful operation at 10Gbp/s. SR-FF results exhibit an ER, CR and AM of 13 dB, 13dB and 2.4 dB respectively. Improved performance of 14dB extinction ratio, 13dB contrast ratio and 1.7dB amplitude modulation is demonstrated in case of D-FF with complementary Set and Reset

input pulses. Although both types of flip-flop outputs experience a slight gain overshoot and some pattern effect when switching state, it has been clearly shown that full switching can be achieved at a operational speed of 10 Gb/s. An escalation of the speed is feasible at the expense of lower performance characteristics.

3. The performance of an all-optical circulating shift register consisting of a semiconductor optical amplifier based optical buffer and an optical AND gate is numerically investigated. The shift register is designed to store an n-bit sequence and to return its bits one by one at a lower clock rate. The operation of the circulating shift register has been verified for a 10-bit input sequence at sequence bit rate of 2.5 GHz and 10 GHz respectively with the speed being mainly determined by the fiber-based feedback loop implementation, so that multi-Gb/s operation should be considered feasible by deploying it as an integrated device. The dependence of the output *Q*-factor on SOA parameters is also investigated and discussed. The circulating shift register can be a basic building block for other applications such as optical memory and clock division.
4. An all optical binary counter is presented employing two stages of optical TFF and an optical NOT Gate. The TFF consists of a SOA based MZI and an external feedback loop. The proposed counter is implemented using the minimum number of active components among the digital optical bit counting devices reported so far. It requires only a single control signal as input. Principle of operation is numerically evaluated for the proposed counter at 5 GHz. The switching times exhibited by the counter are less than 80 ps. Feedback loop length is the main factor determining the speed of proposed counter circuit in the practical implementation. Simple structure implies low power consumption and reduced footprint and making it ideal for photonic integration.
5. Different functions of all optical digital signal processing are realized by employing nonlinear effects in a SOA. The all-optical realizations of adder, subtractor, comparator, demultiplexer, decoder etc are based on SOA-MZI. Numerical Simulations confirming the described logic devices have been presented for different input combinations.
6. In further investigations, SOA-MZI based all optical demultiplexer operation has been analyzed in demultiplexing of an optical time division multiplexing channel at data rates up to 160 Gb/s. Demultiplexed channel shows a 3-5dB improvement

in the extinction ratio for the non return to zero case at different data rates. Pattern induced degradation is observed to be negligible in the case of non return to zero modulated signals. Variation in the bit error rate performance at 160 Gb/s demultiplexing operation is observed in the case of return to zero modulated signals for different pattern lengths. Error free operation is achieved for both types of modulated signals and minimum bit error rate obtained for return to zero case is less than 10^{-9}. Bit error rate performance of non return to zero signals is independent of pulse width within the bounds of 1.25-3ps. It varies significantly for the RZ case with minimum value obtained for pulse width lying within the range of 2-2.5ps.

Therefore, this study establishes designs and investigations of all optical arithmetic and logical devices which are very essential in the high capacity core networks in order to avoid optoelectronics conversions and deal with the revolutionary growth of internet traffic for the future photonics networks.

6.2 Recommendations

The following are some of the possible recommendations based on this research work.

1. The proposed logic gates are simple, reconfigurable and, as they are based on the semiconductor technology, allow for photonic integration. In the proposed design maximum extinction ratio and contrast ratio achieved are 19dB and 17.2 dB respectively, which is more adequate for all optical logic based information processing. These all-optical functions can be used in add-drop multiplexing, wavelength conversion, regeneration, clock recovery and simple bit-pattern recognition. The proposed scheme can be feasible alternative for system utilizing schemes which are temperature and polarization sensitive. Future digital communication systems require extremely fast switches, which must operate in the pico-second range. The all optical scheme for reconfigurable logic operations operate at 40 Gb/s. Our optical gates open the door to a fully integrated, all optical communication networks.
2. The proposed flip-flop has a fast response. The distinctive simplicity of the flip-flop results in low power consumption and reduced footprint and thus making it suitable for photonic integration. It can be used as a key device for realizing many functions in optical computing and optical networks and, especially in optical

packet switches and as all-optical memories for the temporary storage of decisions in photonic packet routers

3. The proposed counter requires only a single control signal as input. This relaxes the need for generation of auxiliary signals by additional combinatorial circuitry. Thus it is able to provide successful counting operation with the minimum number of components reported so far. This reduces the power consumption and complexity requirements. It also retains the speed advantages of optical interferometric switching gates. The device can be recommended for header recognition, payload processing and as a finite state machine in optical computing and packet switching networks.
4. The shifting operation is realized by using a SOA-based optical buffer (OB) and an optical AND gate. The AND gate is implemented by incorporating FWM effect in a SOA which gives a more compact, efficient and potentially integrable solution as compared to fiber based implementation. Successful 10-bit shifting operation has been obtained at a sequence bit rate f_b = 2.5GHz and f_b =10GHz respectively. The concept can be implemented for different number of bits for a given loop length delay time. The increase in the number of bits to be stored does not increase the scheme complexity. Hence, this scheme can be recommended for applications such as serial-to-parallel converters, optical packet buffers, and synchronizers.
5. SOA-MZI types of ultra fast all-optical switches represent the most promising solution to realize all optical algebraic and logic and processors. This is as a result of their thermal stability, low power operation and compact size. Symmetric Mach-Zehender Interferometer structures provide the shortest switching window and highest flexibility. Advantages of SOA-MZI switch are extended by including OTA for the realization of optical arithmetic and logical circuits. SOA based SMZ can be used for demultiplexing of an optical time division multiplexing channel at data rates up to 160 Gb/s. Both types of modulation formats can be used based on the type of application and their suitability.

6.3 Future Scope

1. Optical logic gates presented in this Thesis have been realized at 40 Gb/s operational speed. As an immediate step forward, operation at higher bit rates, experimental validation at 40 Gbit/s should be carried out. The large amount of applications of Boolean gates has been commented within the contents of this

Thesis. One of the applications which show a special interest is the contention detection and resolution. Therefore, it would be interesting to study and design the architectures based on logic gates and switching devices (for example, flip-flops) that allow performing this task in the optical domain, without using electrical processing.

2. The new and alternative solution may be explored for the all-optical binary counter implementation avoiding the feedback loop and, hence, the limitation derived from design issues. A very promising alternative may be the use of some material at both sides of the SOA-MZI to reflect part of the power back to the device and avoid any physical loop. A way could be found to recycle the power in the unused MZI output port, thereby further reducing the overhead. This will make this design more interesting.
3. Recovery time of the semiconductor optical amplifier and intra-flip-flop coupling length are main factors in determining the speed-limit of the flip-flop. Multi-Gb/s operation is feasible if photonic integration is employed for allowing ultra-short coupling lengths between the two semiconductor optical amplifiers.
4. Any of the complex logic function can be implemented and realized by combining beam combiners, beam splitters, and cascading semiconductor optical amplifier based MZI switches. The scheme can be extended easily and successfully for any large number of input digits by suitable branch selection, proper incorporation of MZI based optical switches and by vertical and horizontal extension of the tree.
5. The operation of the circulating shift register has been verified for a 10-bit input sequence at sequence bit rate of 2.5GHz and 10 GHz respectively with the speed being mainly determined by the fiber-based feedback loop implementation. Multi-Gb/s operation should be considered feasible by deploying it as an integrated device. The research wok can be further extended for storing higher number of bits as well as operation at higher input sequence bit rates.

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