Performance Enhancement of NCFETs via Non-Uniform Interfacial Oxide and Dual-Work-Function Gate Engineering

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF ENGINEERING/MASTER OF TECHNOLOGY

in Electronics and Communication Engineering / VLSI Design

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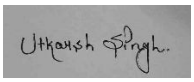
JULY, 2026

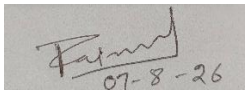
DECLARATION

I, **Utkarsh Singh** hereby declare that the work presented in this thesis entitled "**Performance Enhancement of NCFETs via Non-Uniform Interfacial Oxide and Dual-Work-Function Gate Engineering"** in partial fulfillment of the requirement for the award of degree of **Master of Engineering (ECE) /Master of Technology (VLSI Design**) submitted at **Department of Electronics and Communication Engineering**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rajneesh Sharma (Assistant Professor, DECE, Thapar Institute of Engineering and Technology)** from **August** to **December**. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.



Date: 07/08/2026

Utkarsh Singh
(6024620027)



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ABSTRACT

The miniaturization of traditional MOSFETs, the building blocks of modern electronics, faces a fundamental physical barrier known as the Boltzmann limit. This constraint prevents the subthreshold swing (SS) from falling bless than 60 mV/decade at room temperature, thereby impeding further reductions in power supply voltage and leading to increased energy dissipation. To address this critical challenge, the Negative Capacitance Field-Effect Transistor (NCFET) has been proposed as a transformative device architecture. The device works based on the incorporation of a ferroelectric material in the gate stack of the transistor, which shows a temporary negative capacitance behavior. This effect acts as an internal voltage booster, enabling the transistor to switch with a steepness that surpasses the classical limit.

This thesis presents the design and simulation of an NCFET with a non-uniform interfacial oxide and a dual-work-function (DMG) gate to enhance its electrical performance. The proposed structure was developed and analyzed using Synopsys Sentaurus TCAD. The non-uniform interfacial oxide improves capacitance matching between the dielectric layers and the ferroelectric, while the dual-work-function gate provides stronger electrostatic control near the source and suppresses drain-induced electric field effects near the drain. Together, these design modifications improve switching behavior, reduce leakage current, and increase the drive current of the device.

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CHAPTER 1

INTRODUCTION

1.1 Statement of the problem

Today's electronic devices use billions of tiny transistors called MOSFETs. As technology keeps improving, these transistors are made smaller to increase speed and reduce power use [1]. However, shrinking them further has become very difficult because of some physical limits. One big problem is that normal MOSFETs cannot have a subthreshold swing (the sharpness of the ON–OFF switching) smaller than 60 mV per decade at room temperature. This limit means that the transistor needs a certain minimum voltage to turn ON, which prevents further reduction in power supply [1]. Modern transistors are therefore less efficient, produce more heat, and use more power.

Alternative device designs that can provide quicker switching and lower power operation are desperately needed because of these restrictions. The Negative Capacitance Field-Effect Transistor (NCFET), which uses ferroelectric materials to circumvent the Boltzmann limit and enable energy-efficient transistor design for future CMOS technology, stands out among other strategies [1].

1.2 Negative Capacitance

A phenomenon known as negative capacitance is an exception to normal principles about capacitors. Namely, in any capacitor, an increase of voltage leads to an increase in electric charge that is stored; thus, the value of capacitance is positive [1].

However, for a moment of time in negative capacitance, an increase in voltage leads to a decrease in stored electric charge. This is similar to pushing something in one direction, but getting it to move in the opposite direction.

Such behaviour is not observed in regular materials. Negative capacitance appears only in ferroelectric materials that have unique electrical characteristics. Ferroelectrics can change their inner electric polarization state (orientation of electric dipoles), and during such switching, negative capacitance appears [2].

However, this negative capacitance cannot be stable on its own, therefore you cannot create an actual negative capacitor alone. It only works when combined with other layers (like in a Negative Capacitance Field Effect Transistor (NCFET), where it can be controlled and stabilized [1].

Negative capacitance is of great interest to researchers because it can lower the power required for switching transistors, the tiny switches found in all electronics. This implies that it might result in:

- Lower power consumption
- Less heat generation
- Faster and more efficient computers and mobile devices

In a conventional capacitor, the relationship between charge (Q) and voltage (V) is always positive:

$$Q = C \times V$$

where C>0 means that as voltage rises, more charge builds up.

However, a region occurs in ferroelectric materials because of their inherent nonlinear polarisation features where:

$$\frac{dP}{dV} < 0$$

This indicates a region of negative differential capacitance since the polarisation (or charge) actually decreases as the voltage rises.

This occurs physically because ferroelectric materials have two stable polarisation states (positive and negative) in their internal energy landscape. The material briefly travels through an unstable area where this negative slope happens as it moves between different states.

1.3 Ferroelectric

Steep-slope switching in a Negative Capacitance Field-Effect Transistor (NCFET) is primarily made possible by the ferroelectric (FE) layer inserted into the gate stack. Its distinct energy landscape, which has a region of negative curvature between its two stable polarisation states and is explained by the Landau theory, controls its function. The effect of such a curvature results in a temporary and negative capacitance [3]. Such a negative capacitance creates a voltage divider that increases the internal gate voltage that acts on the channel when it is connected in series with the positive capacitance of the MOSFET.

In order to get a subthreshold swing (SS) lower than 60 mV/decade at room temperature, which is necessary in order to reduce power consumption in advanced CMOS technologies, the

NCFET should cope with the "Boltzmann tyranny," and internal voltage amplification is the main method to do it [2]. Hence, in order to create a device without hysteresis and with better properties, it is necessary to match the properties of the ferroelectric (remanent polarisation and coercive field) with the capacitance of the transistor [2][3].

1.4 Negative Capacitance Field Effect Transistors

The ferroelectric material is placed in the gate stack of an advanced structure of the transistor known as the NCFET to enhance its efficiency and reduce its power consumption [4]. The major principle is to utilize the property of the negative capacitance of ferroelectric materials to achieve voltage amplification within the gate stack that allows the transistor to operate at a low voltage [5].

1.5 Basic Concept and Structure

The components of the gate stack for a regular MOSFET include the semiconductor channel, the dielectric, and the metal gate.

NCFETs have MFIS or MFMIS structures which are fabricated through replacing part or all of the dielectric with a ferroelectric material [4].

A region of negative capacitance in the ferroelectric layer has the potential to increase the voltage across the semiconductor channel.

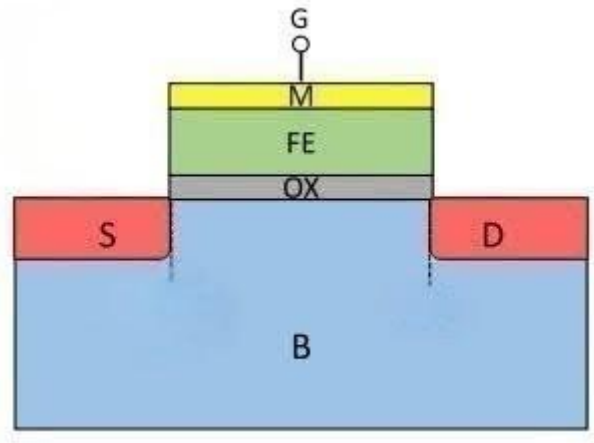

Fig. 1.1 NCFET structures of MFIS

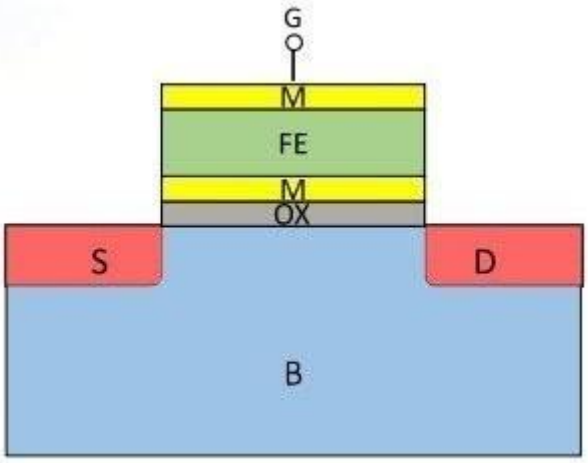

Fig. 1.2 NCFET structures of MFMIS

In order to use the Negative Capacitance (NC) effect for steep switching, the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) arrangement in Fig. 1.1 [5] incorporates a ferroelectric layer directly into the transistor gate stack. However, the strict requirements of capacitance matching and depolarisation fields frequently limit its performance. The Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) structure, which decouples the ferroelectric capacitor from the transistor, was created in Fig. 1.2 [5] as a solution. Although it increases fabrication complexity, this enables independent area scaling (A_FE<A_MOS), which provides an essential design parameter to more readily stabilise the negative capacitance state and achieve the necessary sub-60 mV/decade subthreshold swing [4].

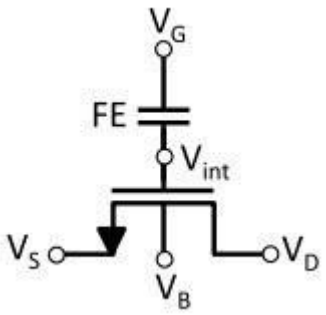

Fig. 1.3 Circuit equivalents of MFIS

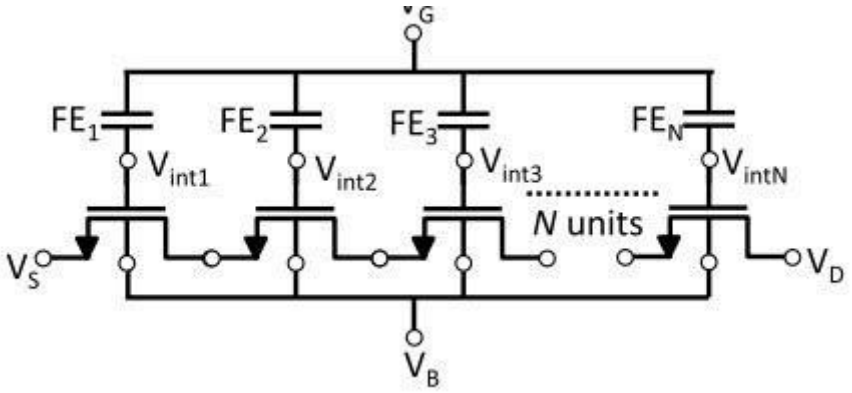

Fig. 1.4 Circuit equivalents of MFMIS

A single non-linear ferroelectric capacitor (Cfe) with negative capacitance is connected in series with the positive gate capacitor of the underlying transistor (Cins) to create an internal voltage amplification (Vint > Vg) that permits steep-slope switching. This is the basic circuit equivalent of a Metal-Ferroelectric-Insulator-Semiconductor (MFIS) structure [5]. On the other hand, a more sophisticated and useful model is provided by the Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS) equivalent, which is represented by several parallel ferroelectric domains (FE1, FE2….,FEn) connected to a common internal node (Vint). This architecture not only averages the switching behaviour of multiple domains for improved stability but, crucially, decouples the area of the ferroelectric capacitor from the transistor gate, enabling designers to independently scale Cfe to meet the critical condition (|Cfe| > Cins) for a stable and hysteresis-free negative capacitance effect[5].

1.6 The Landau Theorem

The behaviour of ferroelectric materials within a Negative Capacitance Field-Effect Transistor (NCFET) is explained by Landau theory [6]. The hypothesis says that the total energy of a ferroelectric substance depends upon its polarisation (P), which refers to the level of alignment of electric dipoles within the material. The Landau–Devonshire (L–D) model uses material-dependent constants to express this energy mathematically. This energy creates a double-well curve when plotted against polarisation, indicating two stable states (positive and negative polarisation) [7]. The negative capacitance region is the area where the energy curve bends downward between these two wells. This area effectively amplifies the gate voltage since a slight change in charge can result in a significant change in voltage in a transistor. This voltage amplification breaks the conventional 60 mV/decade subthreshold swing limit of MOSFETs by enabling the NCFET to flip more quickly and at a lower operational voltage. Nevertheless,

the ferroelectric layer must be connected to a conventional dielectric and semiconductor in order to stabilise this negative capacitance condition, which is unstable on its own.

The behaviour of ferroelectric materials is explained mathematically by Landau theory.

When an electric field is applied, ferroelectric materials' electric polarisation (P) can change direction [7].Landau's theory describes how the energy of the material changes with polarization (P).

The total energy $U(P)$can be written as:

$$U(F) = \alpha P^2 + \beta P^4 + \gamma P^6 - E \cdot P$$

Here:

- P= Polarization (how much the material's dipoles are aligned)
- E= Electric field
- α, β, γ= Material constants (decide the shape of the energy curve)

Taking into account a second order phase transition in Fig. 1.5 [8], this equation provides a curve with two mining energy levels and one maxima at Ps=0, which represents an unstable state and suggests a stable polarisation condition between the free energy versus polarisation landscape at Ep=0.

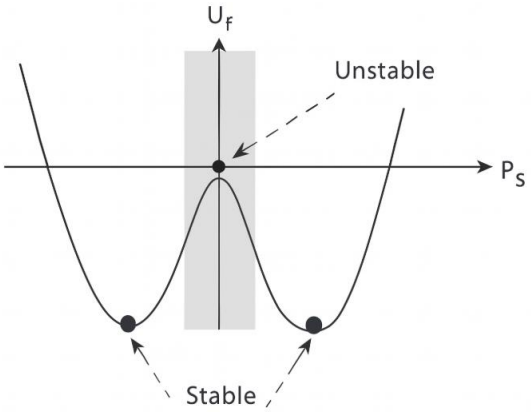

Fig. 1.5 Polarization versus free energy

From Fig. 1.6 [8] The electric field is found by minimizing the free energy with respect to polarization,

$$E(F) = 2\alpha P \quad + 4\beta P^3$$

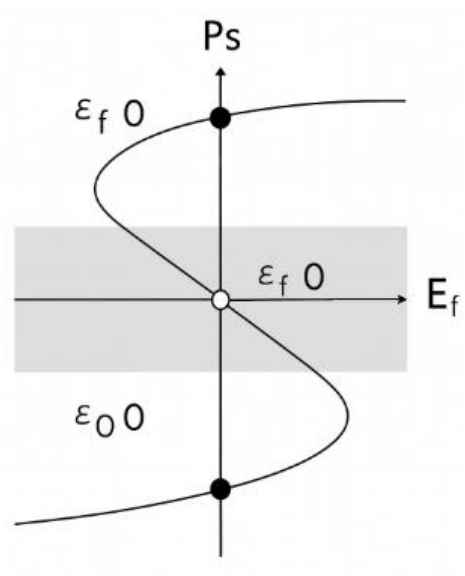

Fig. 1.6 Polarization versus electric field

1.7 How NCFET is difference from MOSFET

The gate stack architecture and the ensuing electrostatics are the primary distinction between a Negative Capacitance Field-Effect Transistor (NCFET) and a conventional MOSFET. An NCFET integrates a ferroelectric layer in series with this dielectric, whereas a typical MOSFET uses a traditional dielectric gate insulator [9]. This ferroelectric material has a negative capacitance effect when it is stabilised in its metastable condition. By acting as a voltage amplifier, this negative capacitance raises the internal gate voltage, which actually regulates the channel, in relation to the applied external voltage. As a result, an NCFET can turn on considerably more quickly than a MOSFET, reaching a subthreshold swing (SS) below the basic Boltzmann limit of 60 mV/decade of conventional transistors at ambient temperature [10]. This steeper switching directly enables lower operating voltages and significantly reduced power consumption, which is the primary motivation for developing NCFET technology as an advancement beyond the standard MOSFET [11].

Table 1.1 Comparison between MOSFET and NCFET

Features	MOSFET	NCFET
Gate Structure	Metal Oxide Semiconductor	Metal Ferroelectric Insulator Semiconductor
Switching Mechanism	Gate Voltage controls channel charge	Gate voltage + amplification from ferroelectric layer
Subthreshold Swing (SS)	Limited > 60mV/dec	Can be < 60mV/dec due to negative capacitance
Power Consumption	Higher, limited by SS	Lower, voltage amplification reduces require gate voltage
Voltage requirement	Standard Operating Voltage	Can operate at loer voltage
Speed	Standard switching speed	Faster switching due to steep SS
Energy Efficiency	Moderate	Higher, more energy efficient
Unique Feature	Stable under normal operation	Uses NC effect from ferroelectric material
Complexity	Simple structure	More complex gate stack design

Chapter 2

Literature Survey

2.1 Literature Review

2.1.1 Analysis and Compact Modeling of Negative Capacitance Transistor with High ON-Current and Negative Output Differential Resistance

This innovative IEEE work (Part II) completely validates and analyses a compact model for the Negative Capacitance FET (NCFET) and compares it to Synopsys Sentaurus TCAD simulations [12]. This research demonstrates that an NCFET with a thick PZT ferroelectric layer is capable of obtaining a sub-60 mV/dec subthreshold swing, having a new NDR in the drain current properties of the device, and providing a large enhancement of ON current up to four times larger than a reference MOSFET [12]. Moreover, the research presents a detailed discussion on the cause of this new NDR effect by connecting it to the dynamics of negative ferroelectric capacitance and internal MOSFET capacitance as the drain voltage changes. The paper also proves the symmetry of the proposed model and its transient performance in ring oscillator structures where the polarization loss in the ferroelectric severely affects the speed of switching. Temperature research indicates that the internal voltage gain and device characteristics are very temperature-dependent, and hysteresis may appear at lower temperatures. Overall, the work validates a robust compact model and reveals novel, complicated device features (high ION, NDR) of NCFETs, offering valuable insights for low-power digital and potential analog/RF circuit design [12].

Authors: Girish Pahwa, Amit Agarwal, Sourabh Khandelwal, Sayeef Salahuddin, Chenming Hu, Yogesh Singh Chauhan

Year: 2016

2.1.2 Insights into Design Optimization of Negative Capacitance Complementary-FET (CFET)

This paper provides a comprehensive design optimization study of Negative Capacitance Complementary-FETs (NC-CFETs) using calibrated TCAD simulations with an ultrathin (1.5 nm) single-crystalline HZO ferroelectric layer. The authors compare two standard gate stack configurations, Metal-Ferroelectric-Insulator-Semiconductor (MFIS) and Metal-Ferroelectric-Metal-Insulator-Semiconductor (MFMIS), within the unique CFET architecture, where n-FET and p-FET are vertically stacked and share a common gate [13]. They reveal that the

conventional advantage of MFMIS over MFIS is suppressed in CFETs because the shared internal gate causes the ferroelectric polarization charge to depend on the combined charge of both the n- and p-FETs, leading to poor capacitance matching and subthreshold swing (SS) in the standard MFMIS design [13]. To address this, the authors propose an innovative "FE-on-Top" (FEoT) MFMIS configuration, where the ferroelectric is placed only above the device, reducing the FE area by ~5.3 times. This design significantly improves capacitance matching and SS, though its performance is limited by the low remnant polarization of ultrathin ferroelectrics. The study further demonstrates that using a ferroelectric with higher remnant polarization can extend the voltage range of negative capacitance operation, boosting the on-current, and provides guidelines for optimizing MFIS NC-CFETs by adjusting coercive field, remnant polarization, and FE thickness [13]. Overall, this work offers crucial insights and design strategies for integrating negative capacitance into advanced, energy-efficient CFET technology.

Authors: Sandeep Semwal and Pin Su

Year: 2025

2.1.3 Metal oxide semiconductor-based negative capacitance field-effect transistors with a sub-threshold swing of below 30 mV/dec

The current research paper presents a new breakthrough in designing highly energy-efficient transistors. In particular, the researchers were able to design a new kind of transistor known as a Negative Capacitance Field-Effect Transistor (NC-FET) based on IGZO oxide semiconductor channel [14]. What was really unique about this experiment is the design of the gate stack made up of both ferroelectric HZO and high-k Al_2O_3 materials. By optimizing the thickness of the latter material to 5 nanometres, they were able to achieve ideal "capacitance matching" necessary to stabilize one of the most unstable physical phenomena, negative capacitance [14]. It allowed the researchers to obtain an extremely pronounced on/off switching mechanism of the transistor that was indicated by the subthreshold swing as low as 27.59 mV/decade, well below the basic 60 mV/decade threshold [14]. Moreover, the team managed to minimize hysteresis to practically zero value of 10 mV [14]. Thus, the combination of a very high on/off slope with negligible hysteresis and low voltage operation makes the described device a good candidate for future application in electronics.

Author: Ji Hyeon Min, Hyun-Suk Kim, Seong Cheol Jang, Kyong Jae Kim

Year: 2025

2.1.4 Energy Storage and Reuse in Negative Capacitance

Here, the FE film is considered to be an energy-storing device that facilitates quasi-adiabatic operation in this 2021 IEEE paper, which provides a basic energy-oriented view of NCFET [15]. The authors show that the FE releases stored energy to help the gate during the transistor's turn-on, lowering the external energy (voltage) needed to reach the target channel charge, using thorough TCAD simulations of both capacitor (MOSCAP) and transistor (MOSFET) designs [15]. On the other hand, the FE recovers and stores energy from the system during turn-off. The NCFET's increased energy efficiency is primarily due to its energy recycling mechanism. Static material free energy integration and transient circuit power integration, two complimentary techniques used in the analysis, demonstrate excellent agreement (within ~1-6% error for long-channel devices), proving the essentially lossless nature of this energy transfer. The majority of the energy storage gain is maintained even in aggressively scaled 20-nm transistors, where parasitic capacitances lower the match between the two calculation approaches. It shows that the intrinsic energy harvesting process, which provides a direct decrease in energy per switching action and represents the key way to reach ultra-low-power devices, is the major advantage of NCFETs over the subthreshold swing improvement [15].
Author: Ming-Yen Kao, Yu-Hung Liao, Sayeef Salahuddin, Girish Pahwa, Avirup Dasgupta
Year: 2021

2.1.5 TCAD Study of Giant Negative Differential Resistance in Nanoscale Ferroelectric Field-Effect Transistors

In this paper, an interesting kind of transistors – Ferroelectric Field-Effect Transistors (FeFETs) with Giant Negative Differential Resistance (NDR) is described [16]. Briefly, NDR can be defined as such a phenomenon when the increase in voltage on the transistor's drain leads to a decrease in electrical current flowing through the transistor. In other words, in NDR the transistor behaves as a reverse of a traditional resistor.

In their research, the authors performed numerical simulations of nanoscale FeFET, showing how NDR can be implemented. It appears to be achieved by utilizing a ferroelectric material in the gate stack of the transistor. As soon as drain voltage reaches some point, this polarisation reverses and, consequently, increases the threshold voltage (thus reducing the transistor conductivity), causing drastic reduction in current flow through the transistor. In the result, an enormous ratio between peak and valley currents is reached by the authors' design.

The major application of this device suggested by the authors is the possibility of implementation of highly compact static random-access memories (SRAM) [1]. This conclusion of the authors is based on the assumption that the design of the transistor is compatible with conventional chip fabrication technology.

Author: Lars Prospero Tatum, Member, IEEE, and Tsu-Jae King Liu

Year: 2025

2.1.6 Antiferroelectric Negative Capacitance Transistor for Low Power Consumption

This paper proposes a novel transistor, referred to as an Antiferroelectric Negative Capacitance Transistor, for energy saving. In particular, the paper aims at overcoming the power dissipation problem in computer chip design via the creation of a transistor with sharp switching ability and ultra-low voltage operation [17].

The core idea of the paper is the application of a specific material, antiferroelectric lead zirconate ($PbZrO_3$), in the gate stack of a transistor. This material ensures the effect of negative capacitance. This allows the transistor to achieve a very steep switching slope, hitting the ideal physical limit of 60 mV/decade, while also having an extremely thin effective gate oxide [17]. Importantly, the device shows almost no hysteresis, a common unwanted memory effect in such transistors, making its behavior stable and predictable.

In short, this work successfully combines multiple desirable features sharp switching, an ultra-thin gate, low leakage current, and minimal hysteresis in a single device. This demonstrates a highly promising path for developing future low-power electronics that could extend the life of Moore's Law [17].

Author: Leilei Qiao, Tian Lu, Cheng Song, Yongjian Zhou, Ruiting Zhao, Qian Wang, Tian-Ling Ren

Year: 2023

2.1.7 Impact of Interface Traps on Negative Capacitance Transistor: Device and Circuit Reliability

In comparison to baseline FinFETs, this 2020 study examines the crucial reliability feature of interface trap degradation in 14nm Negative Capacitance FinFETs (NC-FinFETs), studying effects from device to circuit level [18]. The work reveals a dual-edged effect using well-calibrated TCAD and BSIM-CMG compact models: the internal voltage amplification

simultaneously makes the NC-FinFET more resilient to a given trap concentration, resulting in smaller shifts in threshold voltage (Δ V), while the NC effect amplifies the electric field across the gate oxide, leading to a higher interface trap generation rate under the same voltage (especially in the high-performance scenario) [18]. T ΔV T) and subthreshold slope (ΔSS). Circuit-level analysis of Ring Oscillators (ROs) and 6T-SRAM cells reveals that NC-based circuits experience less frequency degradation and have better or comparable noise margin reliability (Hold, Read, Write) than their FinFET counterparts in the low-power scenario (where NCFET operates at a lower voltage for the same performance) because of superior electrostatic integrity [18]. The study comes to the conclusion that NCFET technology provides a strong reliability benefit for future low-power and high-density circuits, especially when used for voltage scaling, despite the faster trap formation from the higher field.

Author: Om Prakash, Ankit Gupta, Girish Pahwa

Year: 2020

2.1.8 Optimization of NCFET by Matching Dielectric and Ferroelectric Nonuniformly Along the Channel

An important design issue in hysteresis-free Negative Capacitance FETs (NCFETs) without an internal metal gate is addressed in this 2019 IEEE letter: nonuniform capacitance matching along the channel caused by fringing fields from the source and drain [19]. Performance is limited because these fringing fields produce a larger electric field at the channel margins, which results in a spatially variable MOSFET capacitance (Cmos) that is challenging to match consistently with a single-valued ferroelectric capacitance (C_FE). A nonuniform interfacial oxide (SiO_2) layer, where the oxide is thicker at the channel margins and kept thin at the core, is the novel solution that the authors suggest. By counteracting the nonuniformity caused by the fringing field, this geometry engineering produces a more uniform Cmos profile along the channel [19]. This design allows for the use of a ferroelectric with a reduced remanent polarization (Pr), improving total capacitance matching, as shown by TCAD simulations. The result is a steeper minimum subthreshold swing of 33 mV/decade and a notable 20% improvement in ON-current (Ion), all while preserving hysteresis-free functioning. The paper emphasizes how important it is to take spatial nonuniformity into account and actively design against it in order to maximize NCFET performance [19].

Author: Ming-Yen Kao, Yen-Kai Lin, Harshit Agarwal

Year: 2019

2.1.9 NCFET Design Considering Maximum Interface Electric Field

In this IEEE letter from 2018, the reliability constraint associated with the maximum value of the interface electric field (Emax) is addressed, which is an important yet often overlooked design constraint in NCFETs [20]. While the enhancement in voltage amplification provided by the ferroelectric layer improves the efficiency of the devices, this may cause a problem by increasing the electric field in the interfacial dielectric too much, causing breakdown or accelerated NBTI/PBTI effects [20]. It is explained how a design approach based on the use of compact models can be used to correlate the FE parameters (T f) in order to safely design NCFETs.

$$Q_{g,E_{max}} = \epsilon_{ox} E_{max}$$

Using this technique, through the realization of this in a 14 nm FDSOI transistor, it becomes possible for them to show that a properly engineered NCFET will be able to work with lower Vdd values (0.42V as compared to 0.8V in the baseline case), while improving the ratio of Ion/ Ioff and sub-threshold swing (SS) significantly without exceeding the maximum interface field of the baseline transistor [20]. From their findings, it becomes clear that improvement of performance need not necessarily compromise reliability.

Author: Harshit Agarwal, Pragya Kushwaha, Yen-Kai Lin, Ming-Yen Kao, Yu-Hung Liao
Year: 2023

2.1.10 Effects of Gate Offset on Negative Capacitance Field-Effect Transistors with Self-Heating Effect

In this article, a significant problem of NCFETs, known as self-heating, is addressed. During operation, the transistor produces excessive local heat, thus creating a "hot spot" at the drain region. The self-heating problem affects NCFETs especially adversely since it destroys the unique ferroelectric material of their gate, decreasing the ON current of the transistor by 30% [21].

As a solution to this issue, the authors suggest employing the "gate offset" approach. In other words, the whole gate structure is shifted a little bit to the source region, thus protecting the ferroelectric layer from the drain-side hot spot [21]. The effectiveness of this approach has been demonstrated with the help of detailed simulations.

In other words, besides solving the problem of thermal destruction and increasing the value of the ON current, the offset of the gate structure increases the sharpness of switching (the

subthreshold swing). On the other hand, there is a negative aspect of this process because it reduces the maximum speed (cut-off frequency) of the transistor [21]. That is why engineers should determine the optimum value of the gate offset considering their application preferences.

Author: Yangjin Jung, Hyeongu Lee, Mincheol Shin

Year: 2025

2.1.11 Sub-threshold Swing Analysis for NC-TFET in Low-Power Biomedical Applications

In this study, we describe a class of sophisticated transistors referred to as negative capacitance tunnel field-effect transistors (NC-TFETs). They have been proposed to be used in low power applications, for instance, in the biomedical industry. The aim of this study is to address the issue that faces ordinary transistors that cannot turn off and on properly below the so-called 60 mV/decade limit [22].

NC-TFET incorporates both of these features together. In other words, there is a use of TFET (Tunnel FET), where turning on takes place due to the quantum mechanical effect, and NC (Negative Capacitance) feature due to the presence of ferroelectric material which works as a voltage amplifier [22]. Both of these give rise to sub-threshold swing. What is emphasized in this paper is that by replacing Si with Ge in the source region a heterojunction is formed which leads to a steep switching effect with high on-off current ratio. Performance of the device has been analyzed for analog and RF application where its gain and noise effects have been considered. It can be concluded that Ge-source NC-TFET is a very promising candidate for future applications [22].

Author: Sheetal Singh and Subodh Wairya

Year: 2023

2.1.12 Negative capacitance in a ferroelectric capacitor

This pioneering research article provides the first-ever experimental evidence of negative differential capacitance in a ferroelectric system, namely, a thin epitaxial film of $Pb(Zr_{0.2}Ti_{0.8})O_3$ (PZT) [23]. This study utilized a resistor-capacitor (R-C) circuit and investigated the voltage-time response, proving that the voltage across the ferroelectric capacitor falls and the charge rises when the polarization switching takes place in the ferroelectric system, which is an inductance-like effect that is in contradiction with the typical

capacitors. This concept of negative capacitance, introduced by the Landau model but never observed directly until now, is based on the energy barrier of ferroelectric phase transition. The experimental results have been verified using the Landau-Khalatnikov simulation, where transient and hysteretic P-V behavior has been replicated [23]. Moreover, it was proven that the negative capacitance effect is independent of the changes in materials used and is tunable via the series resistance [23]. This finding is important for its application in technology as negative capacitance could surpass the Boltzmann limit (60 mV/decade) of transistors, thus allowing ultra-low power consumption of electronic devices [23]. Apart from transistors, the researchers also proposed possible use in antennas, boosters and coilless resonators. This research provides a general approach to test the negative capacitance effect in any two-state system that is divided by an intrinsic energy barrier [23].

Author: Khan et al

Year: 2014

2.1.13 14nm Ferroelectric FinFET Technology with Steep Subthreshold Slope for Ultra Low Power Applications

This paper demonstrates the successful integration of silicon-doped hafnium oxide (Si:HfO_2) ferroelectric layers (3-8 nm thickness) into a state-of-the-art 14nm FinFET replacement gate process without additional process modifications [24]. The authors propose a comprehensive model distinguishing between Negative Capacitance FETs (NCFETs) and Positive Capacitance FETs (PCFETs), determined by the capacitance matching between the ferroelectric layer and the MOS capacitor load line, which is critically influenced by the interfacial layer (IL) quality. Ferroelectric devices achieved significantly improved subthreshold slopes as low as 54 mV/dec, surpassing the Boltzmann limit, with drive current improvements up to 165% for PMOS devices and 75% for NMOS devices compared to dielectric controls. Notably, this work reports the highest drive current for NCFET devices to date (992 μA/μm for n-type devices) [24]. For the first time, the authors demonstrate that ferroelectric-based ring oscillators can operate at frequencies comparable to conventional CMOS while achieving threefold reduction in active power at 40% lower speed, and improved standby power due to reduced off-state leakage. This work also takes into account the reliability issues arising due to the increased electric field stress caused by the voltage gain in the IL, thus affecting the breakdown voltage and bias temperature instability [24]. The present integration

efforts are an important milestone in bringing about practical realization of ferroelectric negative capacitance in CMOS technology for low power devices.

Author: Krivokapic et al.

Year: 2017

2.1.14 Prospects for Ferroelectric HfZrOx FETs with Experimentally CET=0.98nm, SS_for=42mV/dec, SS_rev=28mV/dec, Switch-OFF<0.2V and Hysteresis-Free Strategies

This paper presents a demonstration of ferroelectric HfZrOx (HZO) FETs exhibiting the best figures of merit in terms of capacitance equivalent thickness (CET), which is 0.98 nm, forward subthreshold swing, 42 mV/dec, reverse subthreshold swing of 28 mV/dec, and switch-off voltage lower than 0.2 V using a 5 nm thick HZO stack with one monolayer SiO_x by ALD [25]. The negative capacitance effect was confirmed through temperature-dependent measurements (room temperature and 150 K), extracting body factors of m = 0.67 and 0.89 at V_DS = 0.1 V and 0.5 V, respectively, demonstrating operation beyond the Boltzmann limit. The authors identify that annealing temperature critically affects device performance, with only 600°C annealing achieving both sub-60 mV/dec switching and hysteresis window below 0.1 V [25]. Two strategies for achieving hysteresis-free operation are proposed, firstly using epi-Ge/Si surface channel FETs, which experimentally demonstrated a threshold voltage shift of only 3 mV due to better capacitance matching between the MOS capacitor and ferroelectric layer, and secondly reducing ferroelectric thickness to 3 nm, predicted by numerical simulations to yield hysteresis-free sub-0.2 V switching. This work establishes that careful optimization of the interfacial layer, ferroelectric thickness, and channel material can enable practical, hysteresis-free negative capacitance FETs for ultra-low-power IoT and wearable applications.

Author: Lee et al.

Year: 2015

2.1.15 Hysteresis-free Negative Capacitance Germanium CMOS FinFETs with Bi-directional Sub-60 mV/dec

This paper reports the first demonstration of hysteresis-free Ge CMOS FinFETs exhibiting bidirectional sub-60 mV/dec subthreshold slope at room temperature, achieved by integrating ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) into the gate stack with an Al_2O_3/GeO_x interfacial layer [26]. Devices with 10 nm HZO exhibited extremely steep switching with minimum SS_rev of 7

mV/dec and SS_for of 17 mV/dec, but with a large voltage hysteresis of -4.3 V due to uncompensated negative capacitance. By scaling the ferroelectric thickness down to 2 nm to achieve proper capacitance matching between C_FE and intrinsic device capacitances, the authors successfully eliminated hysteresis, achieving negligible ΔV_T of -4 mV for pFinFETs and 17 mV for nFinFETs, with minimum SS values of 41 and 43 mV/dec respectively [26]. The 2 nm HZO devices showed symmetric output characteristics without negative differential resistance, confirming stable negative capacitance operation. This work establishes that careful thickness scaling of ferroelectric HZO is a viable strategy for achieving hysteresis-free, steep-slope operation in 3D Ge CMOS devices, demonstrating the promise of combining high-mobility Ge channels with negative capacitance for future low-power integrated circuit applications [26].

Author: Chung et al.

Year: 2017

2.1.16 Energy-Efficient HfAlOx NCFET: Using Gate Strain and Defect Passivation to Realize Nearly Hysteresis-Free Sub-25mV/dec Switch with Ultralow Leakage

This paper demonstrates ferroelectric HfAlOx negative capacitance FETs achieving record performance through the synergistic application of gate strain engineering and fluorine defect passivation [27]. The strained TaN gate electrode enhances the orthorhombic phase transformation of HfAlOx, strengthening the ferroelectric polarization and negative capacitance effect, resulting in 66% I_on enhancement and 27% V_T reduction. The remote fluorine plasma treatment passivates oxygen vacancies in the HfAlOx film and interface traps, forming stable Hf-F and Si-F bonds that mitigate interface depolarization field and reinforce surface potential amplification during NC operation [27]. The combined GS and FP approaches yield nearly hysteresis-free symmetric switching with forward/reverse SS of 24/25 mV/dec, a negligible hysteresis of 20 mV, an ultralow I_off of 4 fA/μm, and an exceptionally high I_on/I_off ratio exceeding 10^8. Remarkably, the sub-60 mV/dec NC operation covers more than 4 decades of drain current, making it possible to attain sub-10 fA/μm leakage for small gate overdrive voltages of less than 0.2 V. From the variability analysis of devices, more than 90% of the devices exhibit sub-60 mV/dec SS with an average value of less than 35 mV/dec, thereby verifying reliable NC switching [27]. The study demonstrates that defect engineering

and mechanical strain could be effective approaches towards attaining hysteresis-free NCFETs that are efficient in energy consumption.

Author: Fan et al.

Year: 2017

2.1.17 Switching-Speed Limitations of Ferroelectric Negative-Capacitance FETs

In this paper, the limitation of negative capacitance field effect transistors due to high frequency switching is investigated based on multi-domain Landau-Khalatnikov simulation approach, which is calibrated with experimentally measured values of PZT [28]. It is shown that although voltage amplification in NCFET can be achieved at low frequencies (such as 5 MHz), this capability decreases and vanishes at GHz frequency, due to the viscosity coefficient ρ of ferroelectric material, which determines the finite switching time of polarization domains. For high frequencies (>=500 MHz), since the ferroelectric material is not able to respond fast enough, the symmetry breaks in P-E loop because polarization is trapped in one state, and ferroelectric acts like a very small linear capacitor that reduces the amplification of the gate voltage [28]. By deriving analytically, a minimum value for the switching time of $\tau\_min = (\rho \times t\_FE)/2 \times (C\_MOS/A)$ was obtained, indicating that the value of ρ should be less than 0.1 Ω·m to be able to get amplification with 1 ps rise time, which is much smaller than the 2 Ω·m that was extracted from PZT experiments, and 1000 times larger than they actually required 0.1 mΩ·m. This work highlights a critical trade-off while NCFETs show promise for low-power, low-frequency applications such as sensors and IoT devices, the intrinsic switching kinetics of current ferroelectric materials impose fundamental frequency limitations that may preclude their use in high-speed processors, identifying the urgent need for ferroelectric materials with substantially reduced viscosity coefficients for high-performance computing applications [28].

Author: Yuan et al.

Year: 2016

2.1.18 Work Function Engineering for Performance Improvement in Leaky Negative Capacitance FETs

This paper analyzes the detrimental effects of ferroelectric leakage on NCFET performance and proposes work-function engineering as a solution. The authors demonstrate that in NCFET

structures with an intermediate metallic layer between the ferroelectric and high-K dielectric, even small leakage currents set the initial polarization state such that the ferroelectric begins from a positive capacitance state at V_G = 0, requiring a significant gate voltage to enter the negative capacitance region, resulting in degraded subthreshold swing and on-current compared to the baseline FET [29]. Through transient simulations of a 45 nm bulk FET with 5 nm HfO_2-based ferroelectric, they show that using metals with dissimilar work-functions for the external gate electrode and intermediate metal layer shifts the ferroelectric charge-voltage characteristic along the voltage axis (V_offset = 0.2 V), enabling the negative capacitance state to be reached at much smaller gate voltages (0.2 V versus >1 V). This engineered leaky NCFET recovers steep subthreshold swing and higher on-current while maintaining the same off-current as the baseline, achieving performance comparable to non-leaky NCFETs but with improved on-off ratio [29]. The work establishes that work-function engineering is essential for practical NCFET design, as leakage is unavoidable in thin ferroelectric films, and proper engineering of the ferroelectric's effective Q-V characteristics can overcome the performance degradation that would otherwise make leaky NCFETs inferior to conventional transistors.

Author: Khan et al.

Year: 2017

2.1.19 Hysteresis Reduction in Negative Capacitance Ge PFETs Enabled by Modulating Ferroelectric Properties in HfZrOx

This paper experimentally demonstrates that hysteresis in negative capacitance Ge pFETs can be effectively reduced by modulating the ferroelectric properties of HfZrOx through post-annealing temperature control [30]. The authors fabricated NC Ge pFETs with 6.6 nm HZO films annealed at temperatures ranging from 350°C to 450°C and found that increasing the annealing temperature enhances the ratio of remnant polarization (P_r) to coercive field (E_c), which directly increases the magnitude of negative capacitance (|C_FE|). As the annealing temperature increased from 350°C to 450°C, the median hysteresis reduced from 2.60 V to 0.22 V, with some devices achieving hysteresis below 0.2 V. The 450°C-annealed NC devices achieved a small hysteresis of 0.10 V while still demonstrating significantly improved subthreshold swing compared to control devices without HZO, along with 60% I_DS enhancement at V_DS = -1.0 V and 94-105% improvement in peak transconductance [30]. The capacitance-voltage measurements confirmed the negative capacitance effect through enhanced C_G peaks, and the observed negative differential resistance was attributed to drain-

coupled NC effects. This work establishes that careful optimization of ferroelectric properties through annealing temperature provides a practical pathway to simultaneously achieve reduced hysteresis and improved device performance in HZO-based NC Ge transistors, with the condition |C_FE| > C_MOS being critical for hysteresis suppression [30].

Author: Zhou et al.

Year: 2017

2.1.20 Variation Caused by Spatial Distribution of Dielectric and Ferroelectric Grains in a Negative Capacitance Field-Effect Transistor

This paper investigates the impact of inhomogeneous crystalline phases in polycrystalline ferroelectric HfO_2-based films on NCFET performance variability, addressing a critical gap in prior studies that assumed homogeneous ferroelectric layers [31]. The authors propose a new DE-FE mixed model incorporating both dielectric (monoclinic/cubic) and ferroelectric (orthorhombic) phases, extracting material parameters by fitting experimental P-E hysteresis loops with 66.7% FE and 33.3% DE phase composition, consistent with reported XRD data showing 10-50% monoclinic phase content. Using Sentaurus TCAD simulations of an 18 nm double-gate NCFET with segmented 2 nm FE-DE layers (3×3 grain matrix), they demonstrate that the spatial distribution of DE and FE grains causes ON current variations up to 14.44% and OFF current variations up to 30.23%, arising from two mechanisms, firtstly, FE grains near the source enhance carrier injection through voltage amplification, while FE near the drain experience deamplification due to fringing fields from the drain reducing surface potential, secondly, DE grains aligned along the channel create leakage paths, whereas FE covering the drain side suppresses leakage [31]. The subthreshold slope variation is relatively small at approximately 1.3%. This work establishes that the random spatial distribution of DE phases within FE films introduces significant additional variability beyond fabrication tolerances, and provides a methodology for estimating performance variation windows using only four TCAD simulations, emphasizing the importance of considering polycrystalline inhomogeneity in NCFET design and compact modelling.

Author: Kao et al.

Year: 2018

2.1.21 Intrinsic Speed Limit of Negative Capacitance Transistors

This research paper has developed a theory framework for investigating the intrinsic response time of ferroelectric negative capacitance transistors, which was not properly considered in previous work using an arbitrary fitted Landau-Khalatnikov (LK) equation [32]. This work has shown that the LK equation is merely the slow diffusive limit of the equation of motion, hence, it cannot be used for modeling the fast response of the system. By reintroducing the inertial term and obtaining the damping constant (ρ) and kinetic inductance from FTIR spectroscopy data (10THz resonance and FWHM) of HfO_2, this work has formulated a physical model where $\rho=0.18\ \Omega\cdot cm$ corresponds to actual loss and not fitting parameter [32]. Solving the full classical equation of motion for doped orthorhombic HfO_2, the authors predict an intrinsic delay of approximately 270 fs to switch a typical inversion charge density of 1.6 $\mu C/cm^2$, far below the ~10 ps requirement for digital logic and substantially faster than conventional LK-based predictions. This work resolves the ambiguity surrounding ferroelectric response time, showing that the inertia of lattice ions enables sub-picosecond switching, and establishes that HfO_2-based ferroelectrics are fundamentally fast enough for high-performance logic applications, with tunable ferroelectric properties offering additional optimization opportunities for capacitance matching and delay minimization [32].

Author: Chatterjee et al.

Year: 2017

2.2 Gaps from these literature papers

Table 2.1 Gaps of Literature Reviews

Challenges	Causes	Impact
NDR [12][16]	Drain field degrades FE polarization	Negative gain, analog performance loss
Hysteresis [14][17]	Thick FE layers, slow polarization switching	Digital switching unreliability
SS vs. Hysteresis Trade-off [13][14][15][22]	Thicker FE improves SS but causes hysteresis	Design compromise required
Short-Channel Effects [15][18][20]	Drain coupling in ultra-scaled devices	Degraded electrostatic control
Capacitance Mismatch [13][19]	When FE layer not match with positive capacitance	Loss of voltage amplification, hysteresis, and negative differential resistance
Self-Heating [21]	Local hot spots weaken the ferroelectric material	Up to 30% drop in ON current, loses low-power benefit

2.3 Objective:

a. To improve the performance of the NCFET device by minimizing subthreshold, achieving better control of electrostatic.
b. To enhance the driving capability of the proposed NCFET structure for reliable high-speed operation.
c. To achieve a higher on-current (Ion) through optimized device design and negative-capacitance engineering.

Chapter 3

Synopsys Sentauras Tool

In this research, technology computer-aided design (TCAD) simulations were performed using Synopsys Sentaurus to model and analyze the proposed Negative Capacitance Field-Effect Transistors (NCFETs). Sentaurus is equipped with a complete physics-based simulation environment which allows solving the semiconductor equations in a self-consistent manner using models for ferroelectrics [33]. This simulator was used to solve the Landau-Khalatnikov equation along with the Poisson's equation and transport equations which allowed accurate modeling of device electrostatics, transfer behavior, and analog characteristics.

Table 3.1 Design Parameters of DMG non-uniform of interfacial layer NCFET

Parameters	Value
Gate Length	20nm
Source side Metal	10nm
Drain side Metal	10nm
FE Thickness	2nm
Spacer Length	10nm
Spacer Height	7.9nm
SiO2 Center	0.9nm
SiO2 Edge	1.8nm
Body Thickness	5nm
Source	20nm
Drain	20nm
Body	50nm

Table 3.2 Doping values in the structure of DMG non-uniform of interfacial layer

Region	Type	Dopant	Concentration
Source	n+	Phosphorus	1×10^{20} cm^{-3}
Channel	p-	Boron	1×10^{15} cm^{-3}
Drain	n+	Phosphorus	1×10^{20} cm^{-3}

Table 3.3 Work function value of Metal Gates

Metals	Work Function Value
Metal1 (near source)	5.6eV
Metal2 (near drain)	4.5eV

Table 3.4 Key Ferroelectric Parameters

Parameters	Value
Remanent Polarization (Pr)	$10.1\mu C/cm^2$
Coercive Field (Ec)	2MV/cm
Dielectric Constant (Er)	16

Table 3.5 Landau-Khalatnikov (L-K) Model Parameters

L-K Parameter	Value
Alpha (α)	$-2.17 \times 10^9 m/F$
Beta (β)	$+1.35 \times 10^{20} m^5/(C^2 \cdot F)$
Gamma (γ)	0
Rho (ρ)	0
G	$8 \times 10^{-5} cm^3/F$

3.1 Why Use Sentaurus in Research

Application of Synopsys Sentaurus TCAD in this study is driven by the crucial importance of the software in the contemporary design flow of semiconducting devices [33]. The application of the software is based on the following principal arguments:

•Performance Prediction: Simulation of electrical characteristics of innovative semiconducting devices prior to their manufacture.

•Timesaving & Economical: Less need for repetitive physical experiments.

•Gives Understanding of the Physics Behind: Helps understand the physics of the operation of a device (such as electric fields, carrier concentrations, which are hardly measurable).

•Simulates Innovative Architecture: Ability to simulate not only conventional transistors but also novel structures such as FinFETs, NCFETs, etc.

•Fast Performance Characterization: Advanced analysis tools.

3.2 The Sentaurus TCAD workflow

Synopsys Sentaurus is a powerful software suite used to design, simulate, and analyze semiconductor devices like MOSFETs, FinFETs, and NCFETs, before they are actually made in the lab [33][34]. It helps researchers and engineers understand how a device will behave by virtually modeling both the fabrication process and electrical performance.

The Sentaurus TCAD tool suite is a collection of integrated programs managed by the Sentaurus Workbench graphical user interface [35]. A typical simulation flow follows these steps:

I. Sentaurus Structure Editor (SDE): Use SDE to build the 2D or 3D geometry of the semiconductor device. This can be done by combining simple geometric shapes or by emulating manufacturing process steps like etching and deposition. The structure information, including material types and contact locations, is saved as a TDR file.

II. Sentaurus Process: For more detailed and realistic simulation, Sentaurus Process simulates the actual fabrication steps of a semiconductor device, such as ion implantation, diffusion, and thermal oxidation. This step generates a device structure with a precise doping profile.

III. Sentaurus Mesh: After creating the device structure as shown in Fig. 3.1 2D Structure of MOSFET, the simulation area is divided into a fine grid of points called a mesh. Sentaurus Mesh is an advanced tool that generates a high-quality spatial mesh, adapting the density of points to capture regions with steep gradients, such as those caused by doping Fig. 3.3 Meshing of 2D structure of MOSFET. The meshed structure is saved as a TDR file.

IV. Sentaurus Device: This is the core device simulator that uses the meshed structure and doping profiles as input. It solves complex physical equations to simulate the electrical, thermal, and optical behavior of the device. You define the physical models and simulation conditions (e.g., applied voltage, temperature) using a command-file.

V. Sentaurus Visual/Inspect: These are post-processing and visualization tools for analyzing the simulation results. • Sentaurus Visual is used for visualizing 2D and 3D data, such as the total current density inside a device. • Inspect is a plotting and analysis tool for 1D (X-Y) data, such as in Fig. 3.3 Plot of current-voltage (I-V) curves.

CHAPTER 4

Analysis of NCFET

4.1 Structure of 2D NC-FET

The schematic representation of the following device is that of a Negative Capacitance Field Effect Transistor (NCFET) made of the UTB-SOI technology. It involves two source/drain regions located on both sides of a thin silicon channel (T_BODY), above a buried oxide (BOX) layer. The gate is comprised of a regular SiO_2 oxide layer (T_SiO2) and a ferroelectric material (T_FE) layer above it, providing negative capacitance for amplification of the gate voltage. The spacers are located next to the gate, serving to prevent the short-channel effects and isolating the gate from the source/drain regions.

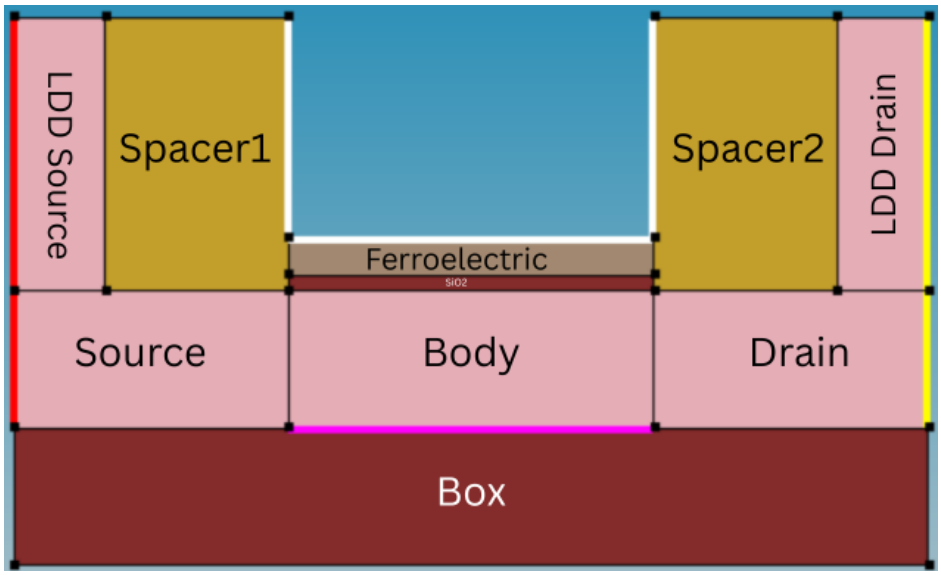

Fig. 4.1 2D Structure of uniform thickness of interfacial layer NCFET

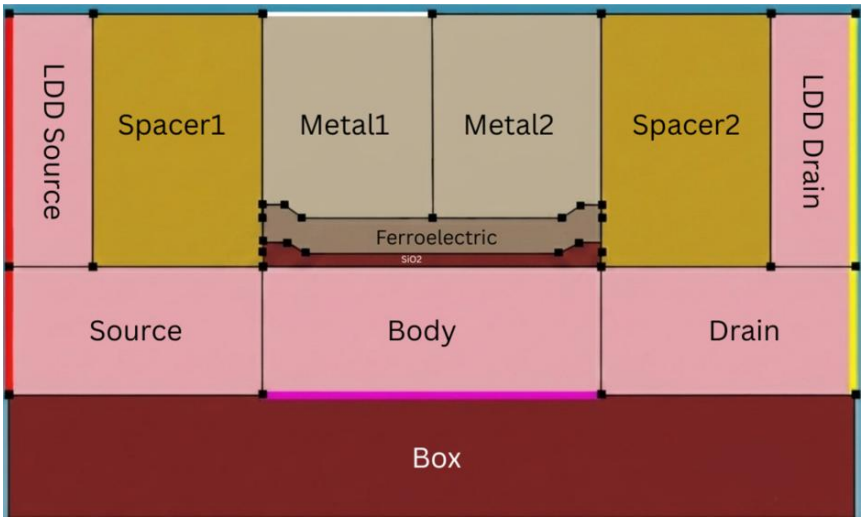

Fig. 4.2 2D Proposed structure of Double metal gate non-uniform of interfacial layer NCFET

In the base paper author used non uniform of interfacial layer with a metal gate but there are some problems occurs such as weak gate control over source side, electric field fringing occurs at the drain side and ioff can be high. Here, metal is divided into two parts, source side which has high workfuntion which means stronger gate control near the source and metal side which has low workfunction which means relaxed control near drain. Using DMG allows for tight channel control on the source side due to the high work function (resulting in steep SS), while the low work function on the drain side shields the drain field (resulting in low IOFF). Combining this with non-uniform SiO_2 also improves capacitance matching.

```
SS: 3.2841e+01 mV/dec
DOE: SS 32.841
```

```
Ion  : 5.3293e-04 A/um
DOE: Ion 0.00053293

Ioff : 1.13e-10 A/um
DOE: Ioff 1.13e-10
```

Fig. 4.3 Value of subthreshold swing, Ion and Ioff

Table 4.1 Comparison the result of Base Paper and Proposal

Parameters	Uniform Interfacial (Author)	Non-Uniform Interfacial (Author)	Uniform Interfacial	Non-Uniform Interfacial (Proposal)
Subthreshold Swing	80.3mV/dec	33mV/dec	80.93mV/dec	32.841 mV/dec
Ion	429uA/um	515uA/um	423uA/um	518.93uA/um
Ioff	188uA/um	180uA/um	183uA/um	103uA/um
Ion/Ioff	2.281	2.61	2.256	4.716

Plot:

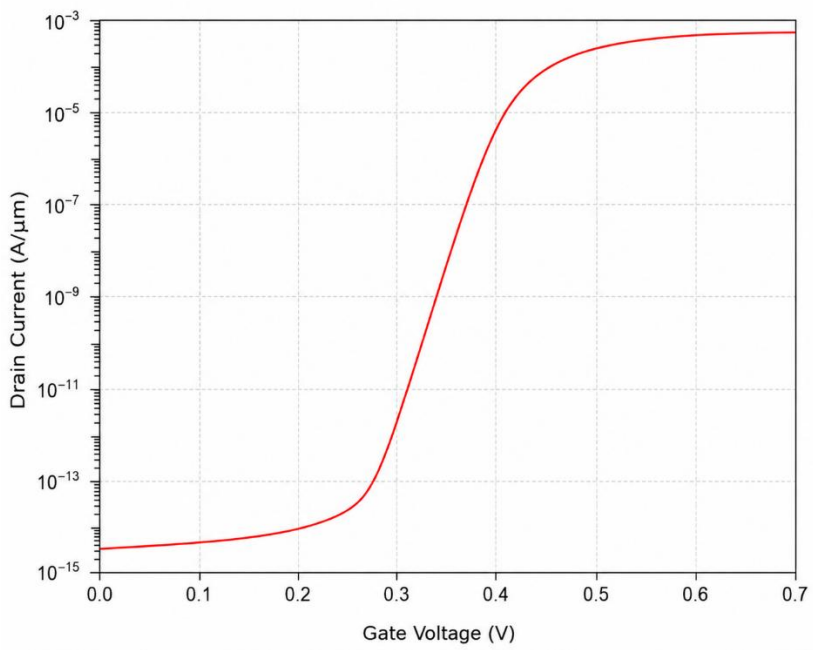

Fig. 4.4 Plot of Id-Vg of NCFET

The transfer characteristics (Id–Vg) of NCFET with a subthreshold swing (SS) of 32 mV/dec are presented in Fig.4.5. The drain current is maintained at a low level in the OFF state in the subthreshold region, but when it gets closer to the threshold voltage, it quickly rises. This shows that the transistor is able to form the channel efficiently. The sharp change between the OFF and ON states signifies the low subthreshold swing (SS) of 32 mV/dec, making the device fast

and energy-efficient. Finally, the drain current gets saturated at the ON-state current of about 10^(-3)A/µm.

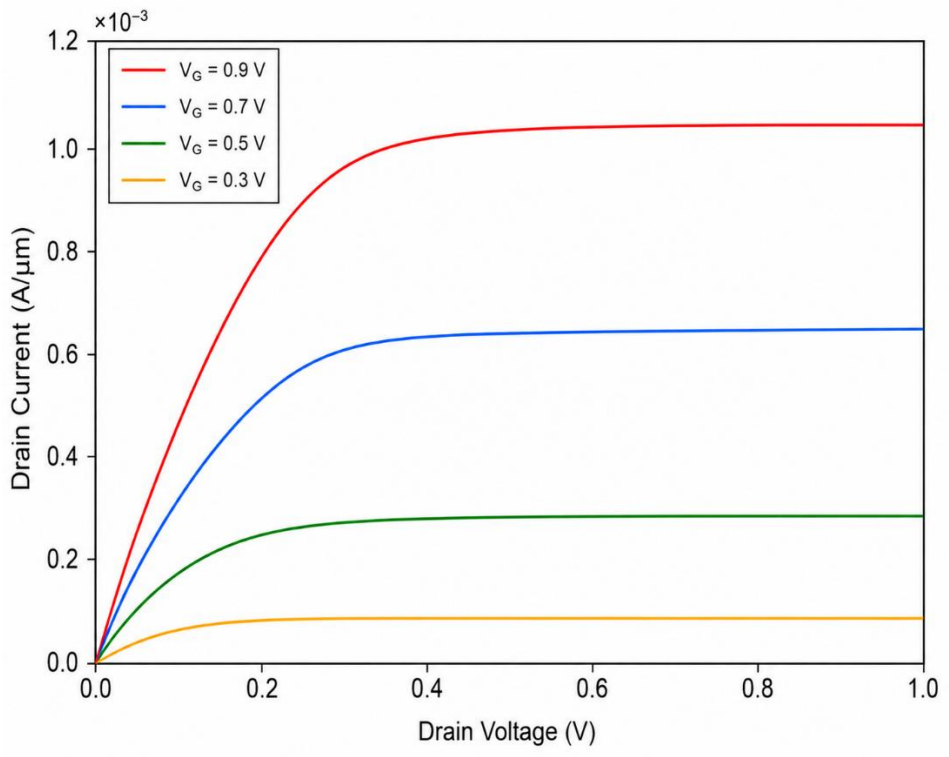

Fig.4.5 Plot of Id-Vd of NCFET

The performance of the NCFET with SS equal to 32 mV/dec is demonstrated for different values of gate voltage VG = 0.3, 0.5, 0.7, and 0.9 V. With increasing drain voltage, VD, the drain current, ID, rises linearly. It means that the NCFET operates in the linear region. However, with further increasing the drain voltage, VD, the saturation of the current occurs due to channel pinch-off effect. By increasing the gate voltage, the drain current increases since inversion of the channel is enhanced. The maximum value of the drain current is achieved when VG = 0.9V. The minimum value of ID is reached at VG = 0.3V. The maximum value of the ON-state current is about 1×10−3A/µm.

Chapter 5

5.1 Conclusion

This thesis focused on improving the performance of a Negative Capacitance Field-Effect Transistor (NCFET) by introducing a non-uniform interfacial oxide and a dual-work-function gate. The proposed device was designed and analyzed using Synopsys Sentaurus TCAD to study its electrical characteristics and compare its performance with the reference structure. These improvements demonstrate better gate control, lower leakage current, and higher drive capability than the reference device. These improvements indicate better electrostatic integrity and demonstrate that combining dual-work-function gate engineering with a non-uniform interfacial oxide is an effective strategy for enhancing NCFET performance.

In other word, the proposed NCFET structure provides an effective approach for achieving low-power and high-performance transistor operation. Although further optimization and experimental validation are still required, the results obtained in this work indicate that the proposed design has strong potential for future energy-efficient CMOS technologies and next-generation electronic devices.

5.2 Future Scope

There are a number of ways the proposed work could be extended. To further improve the capacitance matching and eliminate hysteresis, future work may focus on improving the properties of the ferroelectric material used along with its thickness. The advanced architectures of the devices such as FinFETs, Gate-All-Around FETs (GAAFETs), and CFETs could also benefit from the proposed dual work function technique. Further understanding of device reliability would also be gained through investigation into the effects of temperature, self-heating, process variations, and interface traps. Finally, the experimental fabrication and characterization of the proposed NCFET structure would be required to validate the TCAD simulation results and check the practicality of the structure.

References

[1] Kao, Ming-Yen. "Design of Negative Capacitance Field-Effect Transistor." (2020).

Chowdhury, Nadim, SM Farhaduzzaman Azad, and Quazi DM Khosru. "Negative capacitance tunnel field effect transistor: A novel device with low subthreshold swing and high on current." ECS Transactions 58.16 (2014): 1.

[2] Luk'yanchuk, I., et al. "The ferroelectric field-effect transistor with negative capacitance." npj Computational Materials 8.1 (2022): 52.

[3] Jun-Dong, Chen, et al. "Recent research progress of ferroelectric negative capacitance field effect transistors." Acta Physica Sinica 69.13 (2020).

[4] Lekshmi, T., and Nelsa Abraham. "Performance Evaluation of MFIS and MFMIS Negative Capacitance FDSOI for Low Power Applications." 2025 International Conference on Advancements in Power, Communication and Intelligent Systems (APCI). IEEE, 2025.

[5] Pahwa, Girish, et al. "Physical insights on negative capacitance transistors in nonhysteresis and hysteresis regimes: MFMIS versus MFIS structures." IEEE Transactions on Electron Devices 65.3 (2018): 867-873.

[6] Hoffmann, Michael, et al. "Modeling and design considerations for negative capacitance field-effect transistors." 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS). IEEE, 2017.

[7] Singh, Khoirom Johnson, et al. "Negative capacitance gate stack and Landau FET-based voltage amplifiers and circuits: Impact of ferroelectric thickness and domain variations." Microelectronics Journal 142 (2023): 105981.

[8] Song, Young Suh, et al., eds. Negative capacitance field effect transistors: Physics, Design, Modeling and Applications. CRC Press, 2023.

[9] Li, Jing, et al. "Comparative study of negative capacitance field-effect transistors with different MOS capacitances." Nanoscale research letters 14.1 (2019): 171.

[10] Mendiratta, Namrata, and Suman Lata Tripathi. "A review on performance comparison of advanced MOSFET structures below 45 nm technology node." Journal of Semiconductors 41.6 (2020): 061401.

[11] Chaudhary, Shalini, and Chitrakant Sahu. "Simulation study based performance projection of Negative capacitance FET." 2020 IEEE 17th India Council International Conference (INDICON). IEEE, 2020.

[12] Pahwa, Girish, et al. "Analysis and compact modeling of negative capacitance transistor with high ON-current and negative output differential resistance—Part II: Model validation." IEEE Transactions on Electron Devices 63.12 (2016): 4986-4992.

[13] Semwal, Sandeep, and Pin Su. "Insights Into Design Optimization of Negative Capacitance Complementary-FET (CFET)." IEEE Journal of the Electron Devices Society (2025).

[14] Min, Ji Hyeon, et al. "Metal Oxide Semiconductor-Based Negative Capacitance Field-Effect Transistors with a Sub-Threshold Swing of below 30 mV/dec." Materials Today Electronics (2025): 100178.

[15] Kao, Ming-Yen, et al. "Energy storage and reuse in negative capacitance." *IEEE Transactions on Electron Devices* 68.4 (2021): 1861-1865.

[16] Tatum, Lars P., and Tsu-Jae King Liu. "TCAD Study of Giant Negative Differential Resistance in Nanoscale Ferroelectric Field-Effect Transistors." IEEE Electron Device Letters (2025).

[17] Qiao, Leilei, et al. "Antiferroelectric negative capacitance transistor for low power consumption." IEEE Electron Device Letters 45.1 (2023): 52-55.

[18] Prakash, Om, et al. "Impact of interface traps on negative capacitance transistor: Device and circuit reliability." *IEEE Journal of the Electron Devices Society* 8 (2020): 1193-1201.

[19] Kao, Ming-Yen, et al. "Optimization of NCFET by matching dielectric and ferroelectric nonuniformly along the channel." *IEEE Electron Device Letters* 40.5 (2019): 822-825.

[20] Agarwal, Harshit, et al. "NCFET design considering maximum interface electric field." *IEEE Electron Device Letters* 39.8 (2018): 1254-1257.

[21] Jung, Yangjin, Hyeongu Lee, and Mincheol Shin. "Effects of Gate Offset on Negative Capacitance Field-Effect Transistors With Self-Heating Effect." IEEE Transactions on Electron Devices (2025).

[22] Singh, Sheetal, and Subodh Wairya. "Sub-threshold Swing Analysis for NC-TFET in Low-Power Biomedical Applications." 2023 IEEE Devices for Integrated Circuit (DevIC). IEEE, 2023.

[23] Khan, Asif Islam, et al. "Negative capacitance in a ferroelectric capacitor." *Nature materials* 14.2 (2015): 182-186.

[24] Krivokapic, Zoran, et al. "14nm ferroelectric FinFET technology with steep subthreshold slope for ultra low power applications." *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017.

[25] Lee, M. H., et al. "Prospects for ferroelectric HfZrOx FETs with experimentally CET= 0.98 nm SS for= 42 mV/dec SS rev= 28 mV/dec switch-off."

[26] Chung, Wonil, Mengwei Si, and D. Ye Peide. "Hysteresis-free negative capacitance germanium CMOS FinFETs with bi-directional sub-60 mV/dec." *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017.

[27] Fan, Chia-Chi, et al. "Energy-efficient HfAlO x NCFET: Using gate strain and defect passivation to realize nearly hysteresis-free sub-25mV/dec switch with ultralow leakage." *2017 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2017.

[28] Yuan, Zhi Cheng, et al. "Switching-speed limitations of ferroelectric negative-capacitance FETs." *IEEE Transactions on Electron Devices* 63.10 (2016): 4046-4052.

[29] Khan, Asif Islam, et al. "Work function engineering for performance improvement in leaky negative capacitance FETs." *IEEE Electron Device Letters* 38.9 (2017): 1335-1338.

[30] J. Zhou, Y. Peng, G. Han, Q. Li, Y. Liu, J. Zhang, M. Liao, Q.-Q. Sun, D. W. Zhang, Y. Zhou, and Y. Hao, “Hysteresis reduction in negative capacitance Ge PFETs enabled by modulating ferroelectric properties in HfZrOx,” IEEE J. Electron Devices Soc., vol. 6, pp. 41–48, Oct. 2017.

[31] Kao, Ming-Yen, et al. "Variation caused by spatial distribution of dielectric and ferroelectric grains in a negative capacitance field-effect transistor." *IEEE Transactions on Electron Devices* 65.10 (2018): 4652-4658.

[32] Chatterjee, Korok, Alexander John Rosner, and Sayeef Salahuddin. "Intrinsic speed limit of negative capacitance transistors." *IEEE Electron Device Letters* 38.9 (2017): 1328-1330.

[33] Xeni, Nikolas, et al. "The use of tcad simulations in semiconductor devices teaching." 2020 Transnational Engineering Education using Technology (TREET). IEEE, 2020.

[34] Parent, David W., and Lourdes Del Rio-Parent. "Introducing TCAD tools in a graduate level device physics course." IEEE Transactions on Education 51.3 (2008): 331-335.

[35] Chowdhury, Joy, et al. "TCAD simulation of emerging nanoscale devices." Nanoelectronics: Physics, Materials and Devices. Elsevier, 2023. 409-455.

Appendix

Saturation:

```
# ============================================================
#  DMG + Nonuniform IL NCFET — SATURATION REGION
#  T-2022.03-SP2 Syntax
#  Vd = 0.7V, Vg = 0 -> 0.7V (Forward) + 0.7V -> 0V (Reverse)
# ============================================================
File {
  Grid      = "dmg_ncfet_msh.tdr"
  Parameter = "HfO2.par"
  Plot      = "dmg_ncfet_sat.tdr"
  Current   = "dmg_ncfet_sat.plt"
  Output    = "dmg_ncfet_sat.log"
}
# ------------------------------------------------------------
# DMG Electrodes
# ------------------------------------------------------------
Electrode {
  { Name="source"    Voltage=0.0 }
  { Name="drain"     Voltage=0.0 }
  { Name="gate_m1"   Voltage=0.0  WorkFunction=5.6 }
  { Name="gate_m2"   Voltage=0.0  WorkFunction=4.5 }
  { Name="substrate" Voltage=0.0 }
}
# ------------------------------------------------------------
# Interface physics
# ------------------------------------------------------------
Physics (MaterialInterface="Silicon/Oxide") {
  GateCurrent( DirectTunneling )
}
# ------------------------------------------------------------
# Global physics — Si channel
# ------------------------------------------------------------
```

```
Physics {
  eQuantumPotential
  EffectiveIntrinsicDensity( OldSlotboom )
  Mobility(
    Enormal( Lombardi )
    DopingDep
    eHighFieldSaturation( GradQuasiFermi )
    hHighFieldSaturation( GradQuasiFermi )
  )
  Recombination(
    SRH( DopingDep )
  )
}
# ------------------------------------------------------------
# Ferroelectric physics — HfO2 layer (Nonuniform IL)
# ------------------------------------------------------------
Physics (Material="HfO2") {
  FEPolarization
}
# ------------------------------------------------------------
# Plot variables
# ------------------------------------------------------------
Plot {
  TotalCurrent/Vector
  eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi
  FEPolarization
  Polarization/Vector
  eTemperature Temperature
  ElectricField/Vector Potential SpaceCharge
  Doping DonorConcentration AcceptorConcentration
  SRH
```

```
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal
  BandGap BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eQuantumPotential
  RelativeFermiLevel
}
# ------------------------------------------------------------
# Math settings
# ------------------------------------------------------------
Math {
  Extrapolate
  Iterations     = 100
  Notdamped      = 100
  Digits         = 4
  RelErrControl
  ErRef(Electron) = 1.e10
  ErRef(Hole)    = 1.e10
  Method         = Blocked
  SubMethod      = ParDiSo
}
# ------------------------------------------------------------
# Solve sequence — SATURATION
# ------------------------------------------------------------
Solve {
  # Equilibrium
  NewCurrentFile = "sat_eq"
  Coupled (Iterations=100) { Poisson eQuantumPotential }
  Coupled { Poisson Electron Hole eQuantumPotential FEPolarization }
  # Ramp drain to Vds = 0.7V (Saturation)
  NewCurrentFile = "sat_Vd0.7"
  Quasistationary (
    InitialStep = 1e-5   Increment = 1.3
```

```
    MinStep    = 1e-7   MaxStep   = 0.05
    Goal { Name="drain" Voltage=0.7 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
  # Forward gate sweep Vg = 0 to 0.7V
  # Both gates swept together (same voltage)
  NewCurrentFile = "sat_IdVg_fwd"
  Quasistationary (
    InitialStep = 1e-4   Increment = 1.1
    MinStep    = 1e-9   MaxStep   = 0.005
    Goal { Name="gate_m1" Voltage=0.7 }
    Goal { Name="gate_m2" Voltage=0.7 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
  # Reverse gate sweep Vg = 0.7 to 0V (Hysteresis check)
  NewCurrentFile = "sat_IdVg_rev"
  Quasistationary (
    InitialStep = 1e-4   Increment = 1.1
    MinStep    = 1e-9   MaxStep   = 0.005
    Goal { Name="gate_m1" Voltage=0.0 }
    Goal { Name="gate_m2" Voltage=0.0 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
}
# ============================================================
# END OF FILE
# ============================================================
```

Linear:

```
# ============================================================
#  DMG + Nonuniform IL NCFET — LINEAR REGION
#  T-2022.03-SP2 Syntax
#  Vd = 0.05V, Vg = 0 -> 0.7V
#  Extra: Fine subthreshold sweep for accurate SS
# ============================================================

File {
```

```
  Grid      = "dmg_ncfet_msh.tdr"
  Parameter = "HfO2.par"
  Plot      = "dmg_ncfet_lin.tdr"
  Current   = "dmg_ncfet_lin.plt"
  Output    = "dmg_ncfet_lin.log"
}
# ------------------------------------------------------------
# DMG Electrodes
# ------------------------------------------------------------
Electrode {
  { Name="source"    Voltage=0.0 }
  { Name="drain"     Voltage=0.0 }
  { Name="gate_m1"   Voltage=0.0  WorkFunction=5.6 }
  { Name="gate_m2"   Voltage=0.0  WorkFunction=4.5 }
  { Name="substrate" Voltage=0.0 }
}
# ------------------------------------------------------------
# Physics (same as saturation)
# ------------------------------------------------------------
Physics (MaterialInterface="Silicon/Oxide") {
   GateCurrent( DirectTunneling )
}
Physics {
  eQuantumPotential
  EffectiveIntrinsicDensity( OldSlotboom )
  Mobility(
    Enormal( Lombardi )
    DopingDep
    eHighFieldSaturation( GradQuasiFermi )
    hHighFieldSaturation( GradQuasiFermi )
  )
  Recombination(
    SRH( DopingDep )
  )
```

```
}
Physics (Material="HfO2") {
  FEPolarization
}
# ------------------------------------------------------------
# Plot
# ------------------------------------------------------------
Plot {
  TotalCurrent/Vector
  eCurrent/Vector hCurrent/Vector
  eMobility hMobility
  eVelocity hVelocity
  eQuasiFermi hQuasiFermi
  FEPolarization
  Polarization/Vector
  eTemperature Temperature
  ElectricField/Vector Potential SpaceCharge
  Doping DonorConcentration AcceptorConcentration
  SRH
  eGradQuasiFermi/Vector hGradQuasiFermi/Vector
  eEparallel hEparallel eENormal hENormal
  BandGap BandGapNarrowing
  Affinity
  ConductionBand ValenceBand
  eQuantumPotential
  RelativeFermiLevel
}
# ------------------------------------------------------------
# Math Setting
# ------------------------------------------------------------
Math {
  Extrapolate
  Iterations     = 100
  Notdamped      = 100
```

```
  Digits          = 4
  RelErrControl
  ErRef(Electron) = 1.e10
  ErRef(Hole)     = 1.e10
  Method          = Blocked
  SubMethod       = ParDiSo
}
# ------------------------------------------------------------
# Solve sequence — LINEAR
# ------------------------------------------------------------
Solve {
  #Equilibrium
  NewCurrentFile = "lin_eq"
  Coupled (Iterations=100) { Poisson eQuantumPotential }
  Coupled { Poisson Electron Hole eQuantumPotential FEPolarization }
  #Ramp drain to Vds = 0.05V (Linear region)
  NewCurrentFile = "lin_Vd0.05"
  Quasistationary (
    InitialStep = 1e-5   Increment = 1.3
    MinStep     = 1e-7   MaxStep   = 0.02
    Goal { Name="drain" Voltage=0.05 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
  #Fine subthreshold sweep Vg = 0 to 0.3V (for accurate SS)
  NewCurrentFile = "lin_IdVg_sub"
  Quasistationary (
    InitialStep = 5e-5   Increment = 1.05
    MinStep     = 1e-9   MaxStep   = 0.002
    Goal { Name="gate_m1" Voltage=0.3 }
    Goal { Name="gate_m2" Voltage=0.3 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
  #Continue to full Vg = 0.7V
  NewCurrentFile = "lin_IdVg_full"
  Quasistationary (
    InitialStep = 1e-4   Increment = 1.1
```

```
    MinStep     = 1e-9   MaxStep   = 0.005
    Goal { Name="gate_m1" Voltage=0.7 }
    Goal { Name="gate_m2" Voltage=0.7 }
  ) { Coupled { Poisson Electron Hole eQuantumPotential FEPolarization } }
}
# ============================================================
# END OF FILE
# ============================================================
```