Performance and Analysis of Hybrid Cu/CNT as VLSI Interconnect

Thesis submitted in the partial fulfillment for the award of Degree of

Master of Technology

In

VLSI Design

Submitted by:

Ankush Bharti

Roll No. 601361006

Under the guidance of:

Mr. Karamjit Singh Sandha

Assistance Professor

ECED

Department of Electronics & Communication Engineering

Thapar University,

Patiala-147004 (Punjab)

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DECLARATION

I here declare that the work which prescribed in the dissertation entitled, "**Performance and Analysis of Hybrid Cu/CNT as VLSI Interconnect**" in partial fulfillment of the requirement for award of Master of Technology in VLSI Design submitted in Electronics and Communication engineering Department of Thapar University, Patiala, is an authentic record of my own work carried out under the guidance of Mr. Karamjit Singh Sandha (Assistant Professor), ECED and refers other researcher's which are duly listed in reference section.

The matter presented in this dissertation has not been submitted in any other University/Institute for the award of degree.

Ankush

Date: 15th July 2015

Ankush Bharti

601361006

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

15/7/15

Karamjit Singh Sandha

Assistant Professor

ECED, Thapar University

Patiala-147004

Countersigned by

Head of Department

ECED, Thapar University

Patiala-147004

Dean of Academic Affairs

Thapar Universisty

Patiala-147004

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Ankush Bharti

601361006

ABSTRACT

As technology scaled down, interconnects delay dominates the gate delay in VLSI circuits. Scaling in device size leads to increase in device density and the more length of interconnects are required to connect these devices. Scaling in technology also leads to decrease in interconnect dimension. Copper is currently used as interconnect material. When dimension of interconnect become equal to mean free path of electron of copper interconnect then effect like electro-migration, grain boundary scattering, surface scattering increase the resistivity of copper significantly. Therefore copper cannot be used in future for high speed integrated circuit as interconnect material. Replacement for copper interconnect with new interconnect material is needed in future.

Hybrid Cu/CNT can be promising candidate for future high speed VLSI circuits. The Hybrid Cu/CNT consist of mixture of copper and carbon nanotube. The ground to interconnect capacitance is large in CNT interconnect as compare to ground capacitance in copper interconnects. By covering the copper layer around the CNT results in decrease in capacitance of Hybrid Cu/CNT interconnect. This decrease in capacitance results in improve in delay performance of hybrid Cu/CNT based interconnect. Hybrid Cu/CNT has high electrical conductivity, thermal conductivity, and good mechanical strength.

In this dissertation, impedance parameter of Hybrid Cu/SWCNT as a VLSI interconnect has been calculated and results are compared with copper interconnects at 32nm, 22nm and 16nm technology nodes for global interconnects length. The effects of interconnect length on propagation delay is analyzed and compared with copper interconnect. It is revealed from result that Hybrid Copper/CNT has improvement in delay in comparison to copper in deep sub-micron technology for global length of interconnect.

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ABBREVIATIONS

CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large Scale Integration
CNT	Carbon Nanotube
EDA	Electronic Design Automation
ITRS	International Technology Road Map for Semiconductor
SWCNT	Single Wall Carbon Nanotube
MWCNT	Multi Wall Carbon Nanotube
RLC	Resistance, Inductance and Capacitance
SPICE	Simulation Program with Integrated Circuit Emphasis
PTM	Predictive Technology Model

CHAPTER 1

INNTRODUCTION TO INTERCONNECT

1.1 Introduction

The integrated circuits consist of two basic component (1) Active device (2) Interconnect. The active devices are consist of transistors. A set of wires is needed to connect the transistor to perform the circuit function. These sets of wires which connect the device on a chip are called Interconnect shown in Figure 1.1. Interconnects are also used to connect chips on a multichip module. Copper and aluminum are the commonly used metals for interconnect [1].

Figure 1.1 VLSI Interconnect [1]

As we move towards the submicron technology, the performance of IC is degrading due to increase in delay of active device and interconnect. The interconnect delay has not been a serious concern in VLSI chips until recently, since the gate delay due to capacitive load component dominated the line delay in most cases. [2]

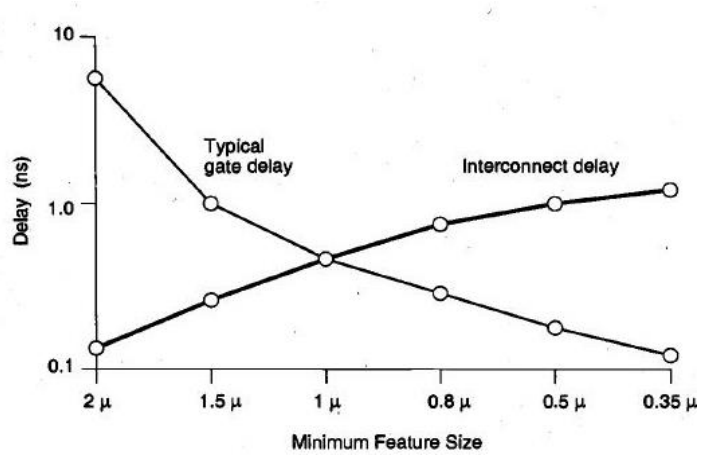


Figure 1.2 Interconnect delay dominates gate in submicron CMOS technology [2]

But for the ICs of submicron geometry, it is the interconnect delays rather than the active device delay that effects performance of the IC. Thus interconnect has gotten much attention over the past years because of its increasing effects on the overall performance of VLSI circuits. As shown in Figure 1.2 where gate delay and interconnect delay is graphically represented for different technologies. It is clear from the figure that interconnect delay starts dominate the gate delay as we move towards submicron technologies. Interconnects introduce parasitic resistances, capacitances and inductances that degrade the overall performance of the VLSI system. The interconnect capacitance presents loading to circuits which in turn increase the propagation delay and power dissipation. Therefore the associated RC delay and power dissipation further degrade the overall circuit performance. [2]

1.2 Interconnect Types:

Interconnects can be classified as

1) Local interconnect
2) Semi-global interconnect
3) Global interconnect

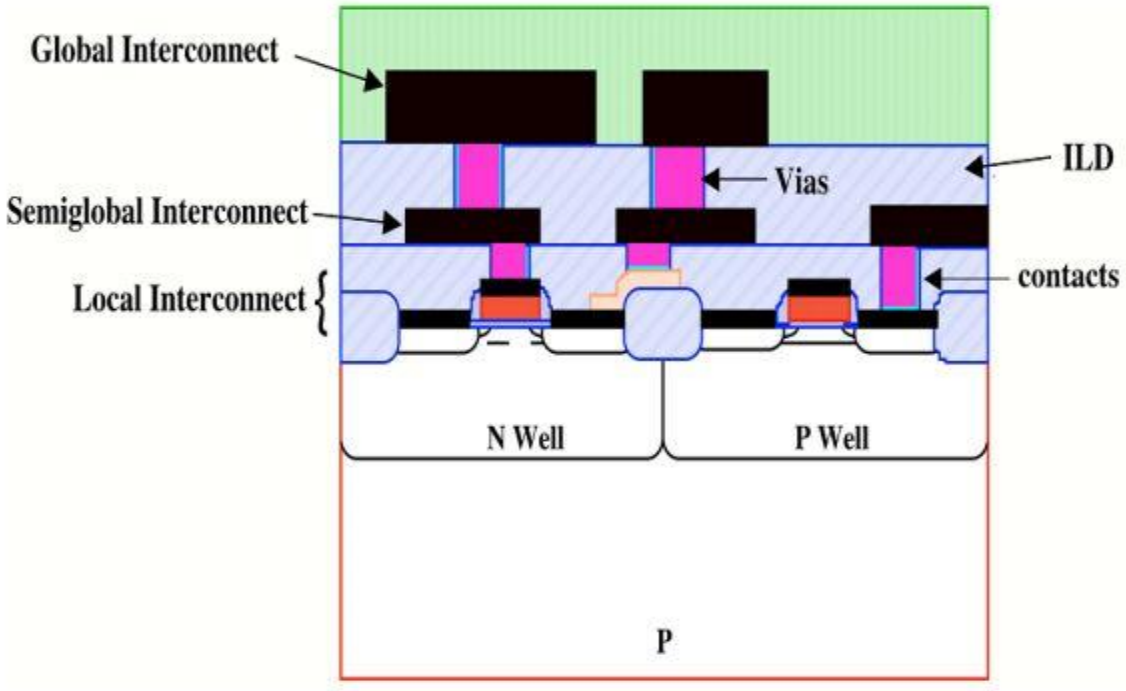


Figure 1.3 Different types of interconnects [3]

1) Local interconnects:- These are the lowest level of interconnects. They connect the gates, sources and drains in MOSFET based VLSI chips. They consist of very thin lines and generally used for making very short connections. The various types of interconnects are shown in the Figure 1.3. These types of interconnects have more resistivity as compare to the global interconnects since they are of short length. But they should able to withstand higher temperatures. [3]

3) Semi global:- This type of interconnects provides the connectivity between large modules and input/output circuitry of the device. They are generally wider, longer, and taller than local interconnects to provide lower resistivity. They provide clock and other signal within a functional block and of lengths up to 3 to 4mm.

3) Global interconnects:-They provides clock, power and long distance communication between functional blocks and provide ground to all functional blocks. They occupy uppermost one or two layers, and they long as half the chip parameter. Global interconnects covers large distances, make connections between devices and different module of the circuit, and thus are always made up of low resistive material.

1.3 Various modelling methods of interconnects:

Interconnects are three dimensional structure that has some resistance and capacitance value. The length to width ratio of interconnect shows that these parameters (R, C) are distributed, making interconnect a true transmission line. Also interconnection lines are close to numbers of other interconnection lines. The capacitive/inductive coupling and signal interference between the lines also taken into considerations. The different models for interconnects are:-

1.3.1 The Lumped Model

Interconnect parasitic are generally distributed along the interconnect length. They are not lumped into a single position. But, for fast observation of the effects of RLC parameters, it is often useful to consider the lump model then considering the parasitic as distributed. As long as the inductance of interconnect is small and the switching frequency is small, only the resistance and capacitive component of the wire are considered. [4]

1.3.1(a) The Lumped RC model

The distributed capacitive component is lumped into a single RC model is shown in Figure 1.4. RC model was used to delay calculation at low frequency. As we are moving

towards submicron technology the free in increasing in Ghzs range. At high frequency this lumped RC model is insufficient to for delay calculation. [5]

1.3.1(b) The Lumped RLC model

In submicron technology, interconnect are of low-resistive material and the increase of clock frequencies in above the GHz range, inductive effects comes into play even on ICs chip. Global interconnects are wider in width. These low resistance lines can have considerable inductive effects. Therefore lumped-RC model, is no longer sufficient for accurate estimation of delay, therefore RLC model of interconnects is used. [6]

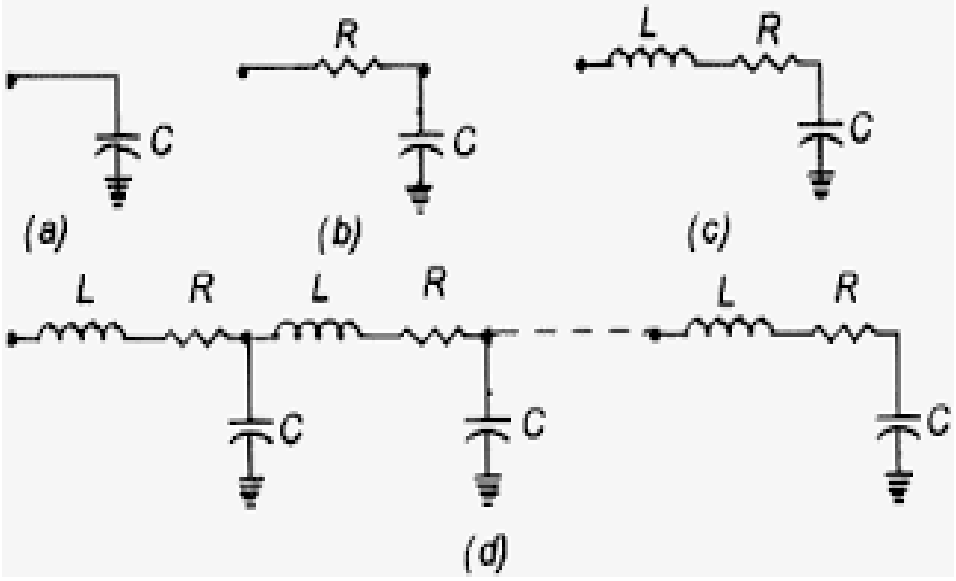


Figure 1.4 (a) Capacitive load (b) Lumped RC model (c) Lumped RLC model (d) Distributed RLC model for interconnect.

1.3.2 The Distributed RLC Line

The lumped RC model described above is a an inaccurate model. For accurate estimation of delay of lines the distributed RLC model is used. The distributed RLC model is shown in Figure 4.1. For computer-aided analysis distributed RLC line can be approximated by a lumped multi-stage RLC model. Defining the individual element values $R = R_{Total}/N$, $C = C_{Total}/N$ and $L = L_{Total}/N$. Where N defines the number of lumped RLC models [6].

1.4 Repeater Insertion

The repeater are used to reduce the propagation delay in interconnects by dividing interconnects into small segments.

1.4.1 Need of Repeater Insertion

As discussed in previous chapters interconnect delay and power dissipation were very small and can be neglected in earlier technologies. But in recent technologies number of interconnections to be used to connect the millions of devices are increasing. Thus resistance of the wires increase resulting in rise in propagation delay and power dissipation. Interconnects can be modelled as lumped (RC or RLC), distributed depending on the operating frequency. Initially interconnect circuits were modelled with RC equivalent circuits and the propagation delay was calculated using a form of Elmore delay through RC [5], which gave the good time constant approximation. But at higher frequency, length of interconnect becomes equal to a multiple fraction of the operating wavelength, which gives rise to distortion that do not exist at lower frequencies [6] .Therefore lumped impedance interconnect models is not sufficient for delay calculation. The other transmission line models such as RLC models give a good approximation of delay at higher frequency. Lumped RC and RLC equivalent circuit models are shown below in Figure 1.5. [7]

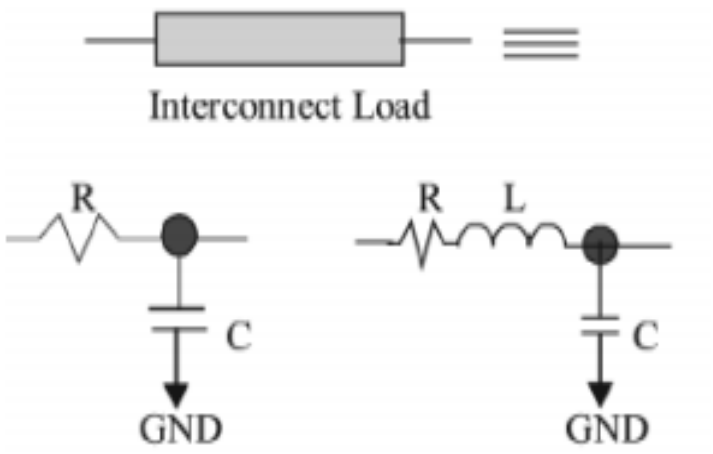


Figure 1.5 Lumped RC and RLC models for interconnect [7]

Technology scaling cause to a linear increase in capacitance and resistance values which further raise the signal propagation delay and power dissipation thus effecting the performance of the ICs. To enhance the performance, both delay and power dissipation have to be minimized. The increase in load capacitance in VLSI circuits due to long interconnect and large fan-outs, driver circuits should able discharge capacitances with acceptable speed. This can be obtained by the insertion of repeater or multi-layering. [8]

Interconnection multilayers are partially solved the delay problem. Layers of interconnect in the x-and y-directions inter-connected by vias at different levels allows long-distance signal propagation without using polysilicon or diffusion crossovers. The cross-sectional area of the top layers can also be optimized to decrease propagation delay. The lower levels can be used for local interconnection and the long-distance signal propagating wire can use the upper levels, which are wider and thicker, yield in shorter signal propagation delays. As the larger of the chip area is covered with interconnect lines, multilayers approach can also reduce chip size and improve the RC time constant because the average interconnection length is inversely proportional to the level number. [8]

On the other hand, repeaters are used to minimize the overall interconnect propagation delay by reducing the effect of resistance and capacitance.

1.4.2 Repeaters

A lot of work has been done regarding Repeaters (inverters). Figure 1.6 shows a CMOS repeater drives an interconnect wire and its equivalent symbol representation in the design. [9]

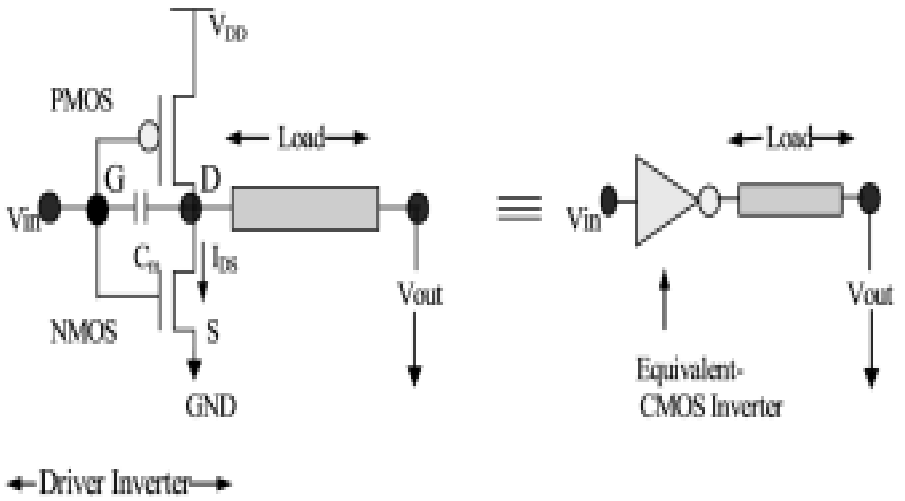


Figure 1.6 CMOS inverter drives in interconnect load and its equivalent symbol [9]

1.4.3 Insertion of Repeaters in Interconnect

When the on resistance of driver is comparable or larger than the wire resistance, propagation delay increases as the square of the wire length because both capacitance and resistance increase linearly with wire length. By dividing the long wires into small segments and inserting a repeater between every two segments, (Figure 1.7) the

propagation delay of the resulting wire becomes a linear function of the number of segments. Repeaters reduce the interconnect wire propagation delay by reducing the effect of capacitance and resistance of interconnect. Therefore interconnect with repeater inserted in it has small delay value than a conventional interconnect with repeater. This technique is called repeater (or buffer) insertion. [10]

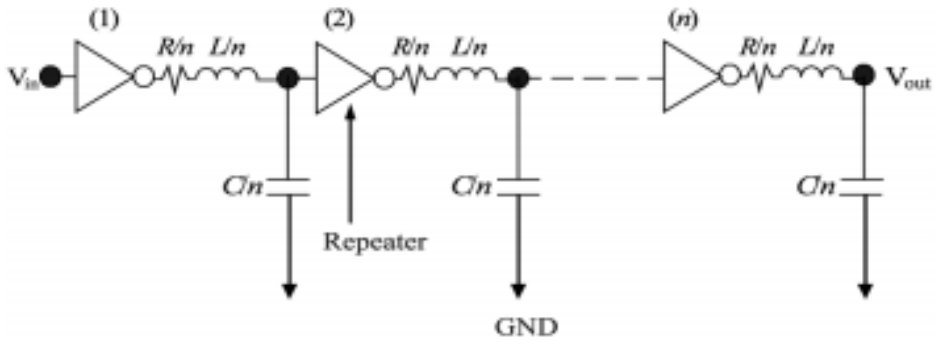


Figure 1.7 Distributed RLC Interconnect with Repeaters inserted in between [10]

Meindl et al. and Ismail et al [11] [12] have derived various models for delay calculation for repeater inserted RLC interconnect lines. Figure 1.8 below shows N number of buffers inserted in between wire, thus dividing it into small interconnect wire.

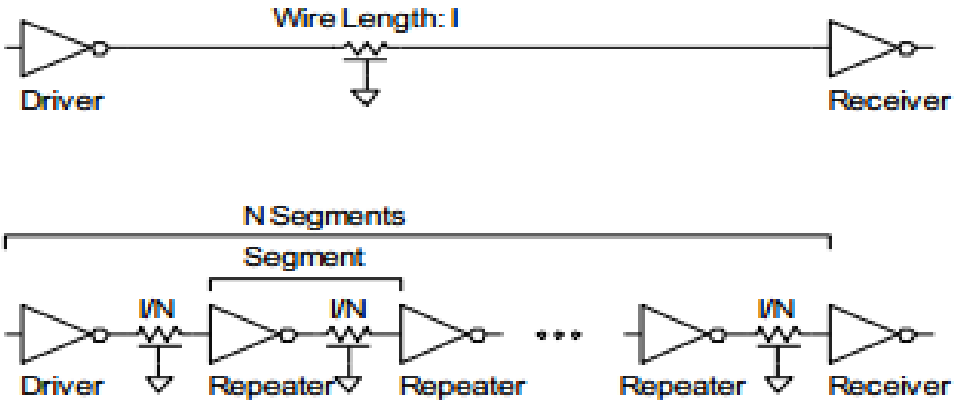


Figure 1.8 N number of repeaters inserted in between an interconnect [13]

If a interconnect wire is divided into small segments, the total RC time constant is reduced. An additional delay due to the inserted repeaters should be taken into the measure for the final calculation of the propagation delay. The number of buffers that can be inserted in an interconnect are limited because at some point, the sum of the delay caused by the repeater will become comparable, or may exceed to the propagation delay of the interconnect. Therefore, we can insert repeater only up to certain limits. [13]

A methodology is developed to reduce power dissipation by calculating the optimum repeater size and length of interconnect. Therefore Power dissipation can be minimized by repeater insertion technique. Power dissipation minimization is done at some value of delay penalty. [14] [15]

1.5 Previously Used Interconnects

1.5.1 Aluminum

Aluminum was the most commonly used interconnect material in earlier technology. This choice was made due to its good conduction of electricity and good ohmic contact with the silicon. Scaling result in increase in number of devices in the same area which further results in more number of interconnect are require to connect these device , therefore length of some chip interconnects increasing as technology scaling. This increase in length causes RLC value to increase [16]. This increased RLC value results in an increase in signal propagation delay of interconnect. Current density of interconnects is increased as the device density increased. Electro migration effect is comes in effect at high current density in aluminum. Therefore aluminum can't be used when high current density was required.

1.5.2 Copper

Copper was used as replacement of aluminum due to its high conductivity than aluminum. Copper has high (approx. 5 times more than Al) current density [17] and higher melting point ($1357\,\mathrm{K}$) than aluminum ($933\,\mathrm{K}$). Due to high melting point copper based interconnect has high thermal stability. Because of these two major advantage copper is preferred for interconnect wire material in the present day ICs.

1.6 Drawbacks of Copper Interconnect

In recent years it is found that even copper is not able to fulfil the demands of future VLSI chips. Today the main requirement of interconnects is a smaller cross sectional dimension in design with the increase in device density. Cross sectional area is being reduced rapidly to accommodate more number of interconnects in a chip. As the dimensions of copper interconnect are becoming equal to the mean free path of electrons of copper the effects like surface scattering, grain boundary effect [18] [19], and electro-migration come into effects. These effects result in an increase in resistivity of copper interconnect. Thus as technology scales increasing resistivity and the increase in interconnect resistance with

length increase delay and due to this power dissipation also increases. Electro-migration is due to gradual movement of ions in a conductor due to transfer of energy between metal atoms and conducting electrons. Electro-migration effects the performance by making circuit less reliable and connection between devices cease.

1.7 Future Interconnect

To overcome the problem with copper as interconnect search for methods and materials is needed. A lot of alternative interconnect material has been purposed. One of promising candidate can be Hybrid Cu/CNT. Research in this field shows that Hybrid Cu/CNT has the potential for being the next generation of interconnect. Hybrid Cu/CNT interconnects has large current density, high thermal stability than copper interconnect. [21] The Hybrid copper/CNT retard the surface diffusion, grain boundary diffusion that is the major cause of electro-migration in copper interconnects. [22]

CHAPTER 2
LITERATURE SERVEY

Magdy A. et al. [1] proposed that for interconnect we can use optimum tapered structure to reduce the power dissipation. It is found that the inductive effects in interconnect cannot be ignored, for global interconnect operating above GHz frequencies. Tapering of wire is used in long interconnects lines, which increase the importance of considering inductive effect in the optimization process. Tapering of wire is an efficient method to reduce signal propagation delay in RLC modeled circuit. Tapered interconnect wire can reduce the transition time at the load gate, decreasing the short-circuit current in load. The capacitance of the interconnect line decreases by tapered interconnect. This reduction in line capacitance decrease two important power (1) short-circuit power of the load gate (2) dynamic power of the driver, which reduce the total power dissipation in comparison to uniform size interconnect wire. Interconnects designed for minimum power dissipation, the total power dissipation of an optimum tapered RLC interconnects is less than the total power dissipation of a uniformly sized. With increase in the number of driven gates power reduction is much larger. It is found that for minimum interconnect line width about 72% of total power dissipation can be saved by using optimal tapering than uniform sizing.

Yehea I. Ismail **[6]** proposed the propagation delay expression for CMOS gate deriving a distributed RLC line. It is observed that as inductive effect increases the quadratic dependence of propagation delay on wire length that modeled with RC line to linear dependence. It is observed that closed form solutions for repeater insertion into RLC line are matched with numerical solution. RC model has errors of 30% in propagation delay of a repeater based system in compare to RLC model. Also including inductive effect in repeater insertion save repeater area and power dissipation. Including inductance into interconnect impedance model is needed for accurate propagation delay estimation of interconnect.

H.B. Bakoglu, James D.Meindi **[9]** proposed the optimization of delay of interconnect in VLSI circuit. Interconnect delay is a major factor effecting the performance of submicron VLSI circuits because the *RC* time constant of interconnects increases rapidly as feature size is decreased and interconnects wire dimension are scaled. In this paper a model for delay in interconnects is presented that include the effects of scaling devices, chip dimension. To improve the delay the either multi layering or repeater insertion is done. Multi layering for delay reduction is significant and improve the high performance. Multilayers also help in reduce in chip area that further reduce the interconnect length and again improves delay. Use of repeater, cascade derivers, multilevel conductors are investigated as effective method for decrease the interconnect delay. Use of cascaded deriver has small delay when deriving the large capacitive load .The optimum repeater with a cascaded stage give the minimum delay as compare to other.

Victor Adler et al. **[14]** proposed that signal propagation delay is limiting the performance of large chips due to increase in resistance of long interconnect. The repeater insertion decrease the effect of quadratic increase in delay while reduce the power by reducing the short circuit current. An equation for short circuit power dissipation value calculation for a repeater inserted circuited is presented. The contribution of the short circuit power in dynamic power is presented. It is observed that short circuit power contribution in dynamic power is up to 20%. It is observes that the repeater inserted to *RC* line can decrease the signal propagation delay.

Kaustav Banerjee, Amit Mehrotra **[15]** proposed additional power dissipation occur during the repeater insertion for delay optimization. A method is presented in the paper to find the buffer size and minimum interconnect length that minimizes the total power dissipation due to buffer insertion for a given acceptable delay. The methodology is use for power optimum buffering scheme for various technology node with a delay penalty of 5%.It is observe that short circuit and leakage power should be considered as important component of power dissipation, and ignoring them can leads to error in power calculation. The exponentially increase of leakage power is observed with device scaling and is the dominant component of power dissipation at 50nm. It is observed that the leakage power

not significant at 180nm and 120nm node. Therefore scaling is increasing the power loss due to leakage current is increasing while the switching power is decreasing as the technology scaling.

Naeemi et al. **[18]** proposed that signal propagation delay and bandwidth of global interconnects effects the performance of a high-speed chip, which connect different modules. The small latency and large data flux density is achieved for optimized width of global interconnects. It is observed that optimal width wire that causes large flux density and small latency, is not depend on the length and can be used for global interconnects. It is observed that optimum wire width is depends on the intrinsic delay of the repeaters, the resistivity of the metal and the wire geometry. Therefore global interconnect with optimum wire width has large performance than conventional wire width. It is observed that optimal wire width interconnect results in 30% smaller energy-per-bit, 84% smaller repeater area and 42% smaller latency at the penalty of 14% decrease in data-flux density, compared to using suboptimal design. On the other hand, using twice of optimum wire width has only 14% decrease in delay at the expense of a 35% decrement in data-flux density in comparison of optimum wire width.

Ke. Chu et al. **[23]** proposed the thermal conductivity is decrease in Hybrid copper/CNT nanowire as compare to CNT nanowire. Thermal conductivity is measure by laser flash technique. The CNTs incorporation into polymers has results in enhanced thermal conductivity. But in case of Hybrid Cu/CNT the thermal conductivity is much lower than CNT. It is revealed form research that the interface thermal resistance is acting as barrier to heat sink in Hybrid Cu/CNT. In the absence of interface resistance it is seen that mixing of CNT in copper leads to large thermal conductivity. Due to large value of interface thermal resistance, the thermal conductivity of copper/CNT material is not effected by content of CNT in Cu/CNT material. Copper/CNT structure has maximum thermal conductivity at 600^{o}C under 50 MPa pressure. Above the temperature of 600^{o}C, the thermal conductivity decrease with increase in hold time and CNT content. This decrease in thermal conductivity is due formation of massive kinks in CNTs at high pressure.

Kaustav Banerjee et al. **[24]** proposed due to limiting current carrying capacity of copper interconnect it cannot used in submicron technology. Metallic carbon nanotubes (CNT) can be new replacement for copper interconnect and extend the life of interconnects of IC. It is observed that metallic SWCNT has outstanding intrinsic properties, high performance. Still several challenges are yet to overcome in the field of fabrication. Also metal-nanotube contact resistance lowering is needed for local interconnects and vias applications.

Chandramouli Subramaniam et al. **[25]** presented that ampacity of Copper/carbon nanotubes hybrid structure is much greater than the copper interconnect. Cu/CNT hybrid structure was fabricated by electro depositing the Cu over carbon nanotube with electron beam lithography. It is observed that resistivity remain constant up to the current density (called ampacity) of 600 $x10^6$ Acm^2 and after that resistivity start increasing exponentially leading to failure at current density of 690 $x10^6$ Acm^2. The SEM shows that failure point was revealed by thinning of material at both end. Only carbon nanotube was found at these this ends. These results shows that the cooper diffused away from these thin region, therefore failure occur in hybrid copper/MWCNT is due to electro-migration of copper. The conductivity of copper was measured by four probe method is 4.7 $x10^5$ S/cm, which is three orders more than CNT. The high fraction of CNT in Cu/CNT hybrid resulted in 42% reduce in density as compare to copper.

Xia Zhangl et al. **[26]** presented that due to extraordinary properties and wide range of application much effort are focused on the study carbon nanotubes as interconnects. Large research has been running on CNT from academia and industry. This paper presented the research work on electronics of CNT. Some challenges faced in electronics industry for implementation of CNT are addressed. It is observed that although CNTs prove to be promising candidate for interconnect application, but still lot of research work to be performed in the field of challenge faced in fabrication of CNT.

Chengyu Yang et al. **[27]** has proposed the electronic structure and transport properties of hybrid Copper/CNT wires. Carbon nanotubes has low free electron than copper. Copper can be used as doping agent to carbon nanotubes to form hybrid Copper/CNT nanowire.

This Hybrid has large free electron density due to copper and large mean free path due to carbon nanotubes. It was theoretically predicted that a low resistivity CNT-metal hybrid can be made, but experimentally such low resistivity hybrid could not be produced. CNT (10, 0) are semiconducting in nature and adding of copper does not change its semiconducting nature. In electronic structure of Hybrid and the CNT (10, 0) band gap are observed, but when copper is added to distorted carbon nanotubes (10, 0) band gaps are reduced and new bands are formed around Fermi level in Hybrid Copper/CNT (10, 0) nanowires. CNT (5, 5) are metallic in nature and band structure of Copper/CNT hybrid nanowire has Fermi level shifted upward, towards the conduction band of carbon nanotubes and more band crossing the Fermi level are observed which increase the conduction of Hybrid Cu/CNT. The copper incorporation in metallic CNT (5, 5) enhance the density of states, transmission coefficient at Fermi level and therefore increase the conductivity.

Yang Chai et al. **[28]** presented the comparison of electro-migration in Cu/CNT hybrid and pure copper. Carbon nanotubes can be promising material for interconnect but still there are some problems to overcome like high contact resistance between metal and nanotube, purity of metallic carbon nanotube and densely packed CNT bundles. By mixing CNT with copper the problem of Electro-migration resistance can be improved. The resistivity of Copper/CNT hybrid was determined using Vander Pauw method. The resistivity of this Hybrid is 2.2 μΩ cm at room temperature and resistivity increase with increase in carbon nanotube content. Mixing CNT in copper solve the problem of grain boundary diffusion and surface diffusion, which cause the electro-migration in copper. When a void is form near carbon nanotube in Cu/CNT, copper volume decrease and the current is pass through the longer section of carbon nanotube gradually, reduce the electron wind force on copper atom.

Kenji Hata et al. **[29]** proposed that Copper/CNT hybrid has higher current caring capacity than copper. This hybrid structure has conductivity comparable to copper interconnect at room temperature and retain this high conductivity at high temperature. At room temperature Hybrid Copper/CNT has conductivity of 4.7×10^5S/cm and is slightly less than copper (5.8×10^5S/cm) at room temperature, but conductivity of this hybrid decrease

in very less value with increase in temperature than copper. It is observed that hybrid conductivity is double of cooper conductivity at 220^{o}C temperature. Electrical conductivity arise from weak inter-atomic bond as occur in metal and high ampacity needs material that has strong inter-atomic bongs as occur in CNT. When Cu mixed with CNT result in high conductivity due to presence copper metal and Carbon nanotubes suppress the diffusion process at interface and make gives the high ampacity. This hybrid structure has low density, therefore are of low weight.

Yitian Peng et al. **[30]** proposed fabrication of hybrid copper/carbon nanotube nanowire. Copper/MWCNT hybrid nanowire fabrication is synthesized by electroless copper deposition technique. This fabrication process of copper/MWCNT nanowire is realized in microfluidic reactor. In comparison to other fabrication technique, the formation of copper layer around MWCNT is effectively controlled in microfluidic reactor. Fabricated copper/MWCNT hybrid nanowire are dense and fully cover by copper over entire length.

Wen Yan Yin et al. **2011 [32]** presented the carbon nanotube as next generation interconnect. The models for CNTs are presents and performance of CNT and copper interconnect is predicted. As compared to SWCNT, the DWCNT has less crosstalk induced propagation delay is observed. The equivalent electro thermal model of single walled carbon nanotube biased with signal voltage is observed for self-heating effects. It is found that the thermal effects on signal integrity should be taken account for local interconnects.

Navin Srivastava et al. **2005 [34]** presented a model for calculation of impedance parameter for CNT bundle. The delay and power of CNT-bundle is compared with copper interconnect. It is observed that SWCNT bundle has smaller delay than copper at global/ intermediate interconnects. Copper outperform SWCNT bundle at local level due to the imperfect contact of CNT bundles It is found that there is an optimum density less than maximum packed density that will cause minimum interconnect propagation delay. Degrade in mean free path length of CNT bundle can occur due defects can change the benefits of using CNT as interconnects.

Kaustav Banerjee and Navin Srivastava **[35]** present the application of carbon nanotube bundles as VLSI interconnect. It is observed that the inductance has significant effect of SWCNT interconnects. It is found that the SWCNT has improvement in delay for global interconnects. By using CNT bundle vias in between the copper layers can provide large metal interconnect lifespan by lowering the temperature because SWCNT has good thermal conductivity in comparison to copper. SWCNT bundle has more thermal reliability than copper if SWCNT bundle are used as thermal vias. It is also observed that SWCNT bundle has improvement in power and delay over copper interconnect.

CHAPTER 3
HYBRID Cu/CNT AS VLSI INTERCONECT

3.1 Introduction

Hybrid materials are defined as mixtures of two or more materials with new properties created by new electron orbitals formed between each material, such as covalent bond between polymers. Hybrid interconnects are submicron mixture of different kinds material. Hybridization is done to for development of new interconnects material with superior property and function. [20] Lot of efforts have been carried out to fabricate hybrid nano-materials consist of metal [21], semiconductor, but little effort has been carried out to fabricate hybrids that are based on carbon nanotubes. Carbon nanotube has unique property such as high mechanical strength, current caring capacity and thermal stability etc. It can be important nanomaterial and appears to be an attractive candidate considered for the making hybrid materials.

3.2 Hybrid Cu/CNT

Carbon nanotubes are discovered in 1991 by Iijima [22]. Carbon nanotubes are one atom thick sheet of graphite (graphene) rolled up into a cylinder with diameter of a nanometer. It has excellent properties such as high mechanical strength, current caring capacity and thermal stability. It is of two types: single walled carbon nanotubes (SWCNT) and Multi-walled carbon nanotubes (MWCNT). (Figure 3.1)

Single Walled Carbon nanotubes or Multi-walled carbon nanotube are used in many Hybrid structure, including copper as metal to improve the performance of interconnect. The newly hybrid material, combination of CNT and copper has excellent mechanical, thermal and electrical properties. [23] Carbon nanotubes incorporated with Copper are called the Hybrid Copper/CNT and classified into following two types:

(1) Hybrid Cu/SWCNT (2) Hybrid Cu/MWCNT

3.2.1 Hybrid Cu/SWCNT

Hybrid Cu/SWCNT consist of combination of single walled carbon nanotubes bundle in combination with copper. Single walled CNT (SWCNT) consists of single layer graphene

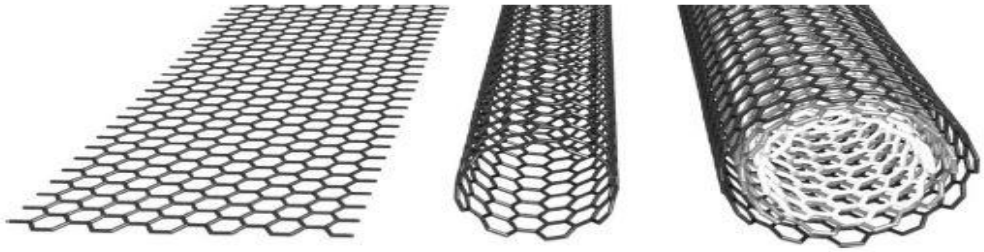
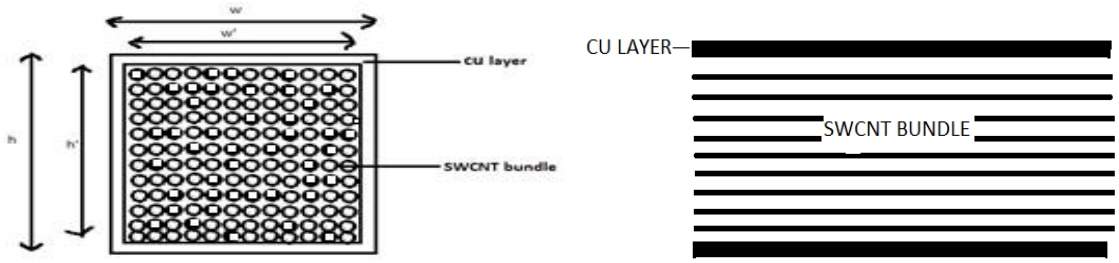


Figure 3.1 Structure of grapheme (left), SWCNT (middle), MWCNT (right) [24]

sheet seamlessly wrapped into a cylindrical tube. SWCNTs have only one layer of graphene of diameter .7 to 10nm. SWCNT bundle are consist of large number of SWCNT running in parallel. The Figure 3.2 show Hybrid Cu/SWCNT where Figure 3.2 (a) shows the front view of the Hybrid Cu/SWCNT structure, where circles represent the SWCNT bundle and outer layer as copper layer and 3.2. (a) Shows Hybrid Cu/SWCNT structure interconnect along its length [24].

. In this arrangement SWCNT bundle are inside and copper layer outside. There are different arrangement possible for Hybrid of SWCNT bundle and copper. The ground to interconnect capacitance of CNT is high in comparison to the copper interconnect. By covering the SWCNT bundle with outer copper layer the ground capacitance of Hybrid Cu/SWCNT will decrease significantly. Therefore this hybrid structure of Cu/SWCNT has low capacitance in comparison to CNT. In Hybrid Cu/SWCNT, the SWCNTs bundle runs parallel with the outer copper layer, the resistance of CNT is less than copper. Therefore SWCNT bundle will provides the low resistance path to flow of current in this Hybrid structure. Thus Hybrid Cu/SWCNT has low resistance to flow to signal as comparison to copper. Therefore, there will be significant improvement in delay performance due to decrease in value of capacitance and resistance in Hybrid Cu/SWCNT. [25]



(a) (b)

Figure 3.2 (a) Front view of the Hybrid Cu/SWCNT where circles represent the SWCNT bundle and outer copper layer (b) Hybrid Cu/SWCNT interconnect along length

3.2.2 Hybrid Cu/MWCNT

Hybrid Cu/MWCNT consist of combination of copper and multi-walled carbon nanotubes bundle. Multi walled CNT (MWCNT) consist of concentric CNT cylinders held within each other by Vander Walls forces [35]. The distance between two shells is approximately 0.34nm. MWCNT bundle consist of number of isolated MWCNT running on parallel. The Figure 3.3 show the Hybrid Cu/MWCNT. In this Hybrid multi-walled carbon nanotubes are inside and is cover by outer copper layer.

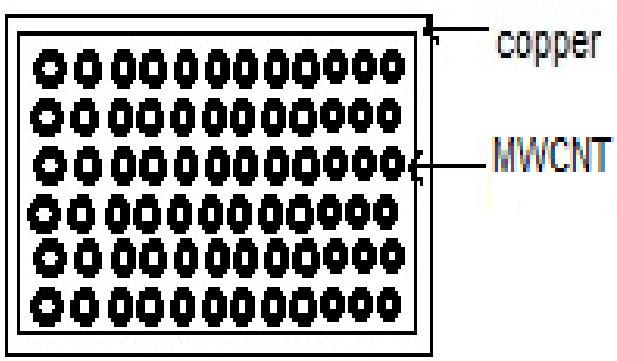


Figure 3.3 Hybrid Cu/MWCNT

3.3 Hybrid Cu/CNT as interconnect

Copper has been used as interconnect to connect electronics devices in recent VLSI circuits. Material and dimension of a wire are major factor that determine the amount of current that can flow to wire. Shrinking in size of device has results in decrease in cross section dimension of wire connecting these devices. This limits the maximum current that can flow through wire. Researcher has found that when Carbon nanotube is used together with copper, the resulting new material exhibits very high current caring capacity and has similar conductivity as that of copper [25]. Hybrid Cu/CNT can be a good wiring material for high performance integrated circuits

Carbon nanotubes and copper composites has good thermal conductivity. The interface thermal resistance between copper and CNT is crucial factor in determining the thermal conductivity of hybrid Cu/CNT. At high pressure composite placed at 600^{o}C for five minute shows the maximum thermal conductivity. [26] This thermal conductivity decreased with increase in temperature and this degradation in thermal conductivity further decrease with increase in CNT content. This reduction in thermal conductivity of Hybrid Cu/CNT is due formation of massive dents in CNT at high pressure. The thermal

conductivity observed in this hybrid is smaller as compare to CNT specimen, but it fulfill the demand of thermal conductivity that is required to for efficient heat sink in local interconnects. Therefore Hybrid copper/CNT can be considered for heat sink application in VLSI circuits.

Carbon nanotubes has low free electron density. On the other hand, copper has high free electron. Therefore Cu can be used as doping agent for Hybrid Cu/CNT interconnect which has both the large mean free path and the large free electron density. In electronic structure of copper and the CNT (10, 0) (CNT (10, 0) is semiconducting in nature) band gaps are seen ,but band structure of Hybrid Cu/CNT(10, 0) shows that incorporation of copper in CNT (10, 0) narrow the band gap of semiconducting CNT (10, 0). And new bands are formed around the Fermi level in the Hybrid Cu/CNT (10, 0). In case of metallic CNT (5, 5) the mixing of copper into it, the Fermi level shift upwards towards the conduction band of CNT (5, 5) and more band crossing the Fermi level are observed. Therefore incorporation of copper increases the conductivity of both metallic CNT (5, 5) and the semiconducting carbon nanotubes (10, 0). [27]

Carbon atom does not form intermetallic compounds with the copper and the interface bond of carbon and copper is poor in Cu/CNT Hybrid. However, enhanced electro-migration resistance shows the considerable bonding between copper and carbon nanotubes, still there is no chemical bonding between them. A strong mechanical interlocked at rough sidewall of CNT forms a high strength bonding between copper and carbon nanotubes is responsible for this enhanced electro-migration. CNT also reduce the electro-migration deriving force in Hybrid Cu/CNT. When void is form near CNT in Cu/CNT, the copper volume decreases, and the current shunted to longer section of carbon nanotube, decreases the electro-migration problem due to copper. [28]

The EM failure at the interface is due to breaking of bond between metal and surrounding material (called surface diffusion). In case of Copper/CNT, CNT has strong chemical bond with surrounding material then pure copper which has poor adhesion. Therefore Cu/CNT hybrid retard the problem of surface diffusion which enhance the EM in copper interconnects. [28]

Copper and gold has current density of 10×10^6 A/cm^2, but Copper/CNT has current density of 690×10^6 A/cm2 for same size and shape. Ampacity of material is defined as maximum

current density at which the resistivity of material is constant. This value is 6.1 $x10^6$ A/cm^2 and 6.3 $x10^6$ A/cm^2 for copper and gold. On the other hand the ampacity of copper/CNT is 600 $x10^6$ A/cm^2. Therefore Cu/CNT has higher current density and ampacity than copper and gold. At room temperature the conductivity of copper is 5.8 $x10^5$ S/cm and copper/CNT has conductivity comparable of copper (5.8 $x10^5$ S/cm). But the decrease in copper conductivity is rapid with increase in temperature than copper/CNT. Cu/CNT has double conductivity than copper at 227°C. [29]

The Copper/CNT has resistivity measured at room temperature is 2.2 μΩ cm. This resistivity increases with increase in content of CNT in Hybrid Cu/CNT.

The deposit of copper over MWCNTs is still key challenge. As the structural and geometrical properties plays (such as electrical, thermal properties) important role for various attributes of wire. Therefore for required geometric properties, deposition of copper over MWCNT need control fabrication process. In compare to other depositing process the copper layer formation around Cu/MWCNT can be controlled effectively in microfluidic reactor. The Cu/MWCNT nanowire obtained by this process are dense, completely covered by copper over entire length. [31]

Due to complexity in structure of multi-walled carbon nanotubes, the single walled carbon nanotubes has got more attention than single walled carbon nanotubes. In this thesis work analysis on Hybrid Cu/SWCNT is done.

3.4 Equivalent Circuit Model for Hybrid Cu/SWCNT Interconnect

The equivalent model for Hybrid Cu/CNT can be realized by combining the individual model of SWCNT and Cu. The Figure 3.4 shows the Equivalent circuit model for Hybrid Cu/SWCNT interconnect.

3.4.1 Resistance of Hybrid Cu/SWCNT

In Hybrid Cu/CNT the Cu and SWCNT bundle are running in parallel. Therefore the resistance of Hybrid Cu/CNT will be equal to parallel combination of resistance of copper and SWCNT bundle.

$$\frac{1}{R_{HYBRID}} = \frac{1}{R_{CU}} + \frac{1}{R_{BUNDLE}} \tag{3.1}$$

Where R_{CU} is resistance of copper and R_{CNT} is resistance of SWCNT bundle.

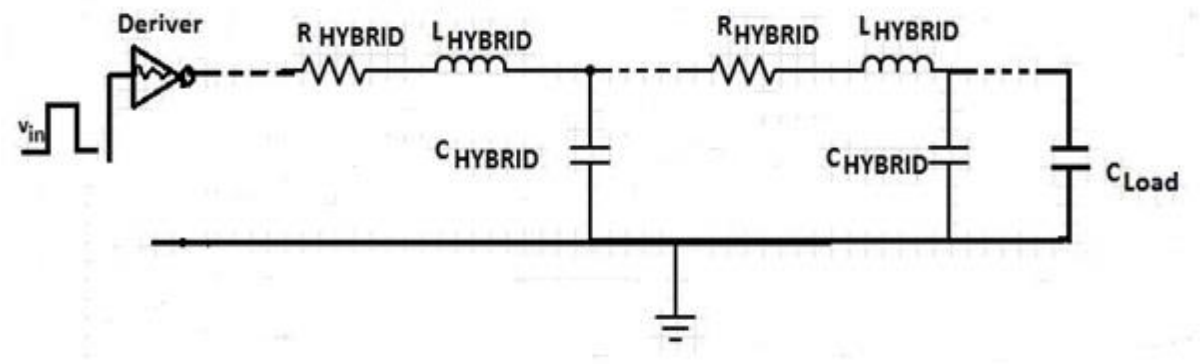


Figure 3.4 Equivalent circuit model for Hybrid Cu/SWCNT interconnect

3.4.1(a) Resistance of copper (R_{CU})

The resistance of Copper Interconnect is given by equation [31]

$$R_{CU} = \frac{\rho l}{wt} \tag{3.2}$$

Where, "ρ" is the resistivity of copper and it varies with technology, "l" is the interconnect length, "w" is the width, "t" is thickness of the wire and are technology dependent parameters.

3.4.1(b) Resistance of SWCNT Bundle (R_{BUNDLE})

The SWCNT bundles are consist of number of isolated CNT running in parallel (Figure 3.5). A CNT bundle interconnect is considered to be made of hexagonally packed identical metallic single-walled carbon nanotubes, In which each CNT is surrounded by six immediate neighbors, their centers uniformly separated by a distance 's'. The expressions to calculate the number of CNTs in the bundle are shown in following equations. [33]

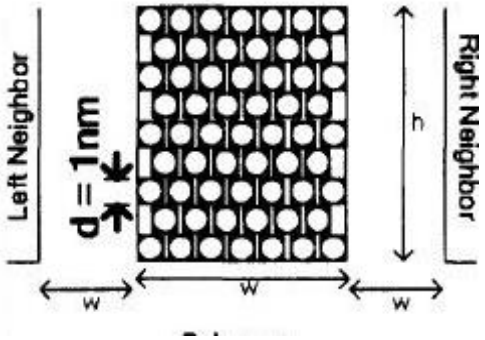


Figure 3.5 Cross-section of a SWNT bundle interconnects [34]

$$n_w = \frac{(w-d)}{x} \tag{3.3}$$

$$n_h = \frac{(h-d)}{\sqrt{\frac{3}{2}}x} \quad . \tag{3.4}$$

$$n_{CNT} = n_w n_h - \frac{n_h}{2} \qquad \text{if } n_H \text{ is even} \tag{3.5}$$

$$n_{CNT} = n_w n_h - \frac{n_h - 1}{2} \qquad \text{if } n_W \text{ is odd} \tag{3.6}$$

Where n_H is the number of rows in the interconnect bundle, n_H is the number of columns. n_{CNT} is the total number of CNTs. Figure 3.6 show the equivalent circuit model for carbon nanotube.

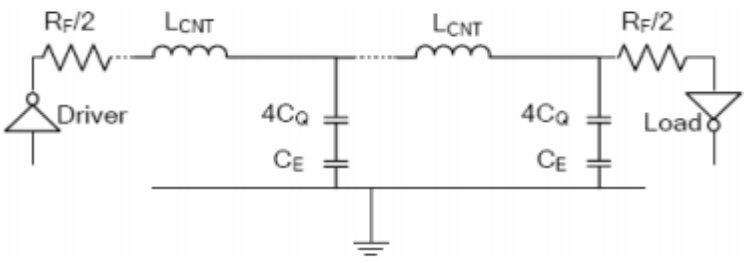


Figure 3.6 Equivalent circuit model for isolated carbon nanotube.

The diffusive component R was not modelled and was taken in ballistic limit. In such case, intrinsic impedance (also called contact or quantum resistance) is given by h/e^2 , Where e is the charge on electron and h is the planks constant.

Due to spin degeneracy and sub-lattice degeneracy of electrons in graphene, each nanotube has four 1-D conducting channels in parallel. Therefore total resistance will be $h/4e^2$ .The resistance of a carbon nanotube of length $L. < \lambda_{CNT}$ with ideal coupling to the two metal contacts at its ends is given by [35]

$$R_{CNT} = R_F = \frac{h}{4e^2} = 6.45\text{K}\Omega \tag{3.7}$$

Where h is Planck's constant and e is electron charge.

This is the fundamental resistance associated with a SWCNT as shown in Figure 3.4 below that cannot be avoided. As shown in following figure this fundamental resistance (R) is equally divided between the two contacts on either side of the nanotube.

For lengths greater than the mean free path $L > \lambda_{CNT}$, scattering leads to an additional ohmic resistance given by [36]

$$R_{CNT} = \left(\frac{h}{4e^2}\right)\frac{L}{\lambda_{CNT}} \tag{3.8}$$

Practically, the two metal-CNT contacts are never ideal leads to an additional imperfect contact resistance (R_C) which can be as high as 0- 100 KΩ. In this work the contact resistance is taken as 20kΩ

In order to calculate the effective resistance of a CNT bundle, [37] it is assumed that all CNTs packed into the interconnect structure are metallic and conducting. The CNT -bundle resistance is then given by:

$$\mathrm{R_{BUNDLE}} = \frac{R_{CNT}}{n_{CNT}} \tag{3.9}$$

3.4.2 Capacitance of Hybrid Cu/SWCNT

The capacitance of Hybrid Cu/CNT interconnects is given as

$$\frac{1}{C_{HYBRID}} = \frac{1}{C_{CU}} + \frac{1}{C_{BUNDLE}} \tag{3.10}$$

Where C_{CU} is capacitance of copper and C_{BUNDLE} is capacitance of SWCNT bundle.

3.4.2(a)Capacitance of copper (C_{CU})

The capacitance of copper is given by Ground capacitance [38]

$$C_g = \varepsilon\left(\frac{w}{h} + 2.22\left(\frac{s}{s+0.70h}\right)\right)^{3.19} + 1.17\left(\frac{s}{s+1.51h}\right)^{.76}\left(\frac{t}{t+4.53h}\right)^{.12} \tag{3.11}$$

Where "Cg" is ground capacitance, "s" is the separation between copper wires and is taken equal to the width "w", "ϵ" is the permittivity of copper wire and its value depend upon technology, h is the distance of copper from ground plane.

3.4.2(b) Capacitance of SWCNT Bundle (C_{BUNDLE})

CNT has two capacitance arise from two sources. (1) The electrostatic capacitance (C_E) is calculated by considering the CNT as a thin wire, with diameter 'd', placed a distance 'y' away from a ground plane shown in Figure 3.6 and is given by [39]

$$\mathrm{C_E} = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)} \tag{3.12}$$

(2) The quantum (C_Q) accounts for the quantum electrostatic energy stored in the nanotube when it carries current and is given by

$$C_Q = \frac{2e^2}{hv_F} \tag{3.13}$$

Where h is the Planck's constant and V_F is the Fermi velocity.

Since a CNT has four conducting channels, the effective quantum capacitance resulting from four parallel capacitances C_Q is $4C_Q$. The same effective charge carried on both these capacitances (C_E and $4C_Q$) when the CNT current flows. Therefore they come in series in equivalent circuit. [40]

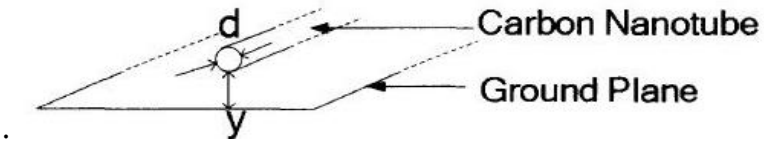


Figure 3.7 Carbon nanotube with diameter 'd' and distance 'y' below ground [40]

The capacitance of SWCNT is given by quantum capacitance. The Quantum capacitance (CQ) accounts for the quantum electrostatic energy stored in the nanotube when it carries current. Quantum capacitance is use to model the energy needed to add an electron at available quantum state above Fermi level. The expression for Quantum capacitance per unit length is given as [41]

$$C_Q = \frac{2e^2}{hv_F} \tag{3.14}$$

Where v_F is the Fermi velocity of carbon nanotube, h is plank's constant and e is charge on an electron. As a CNT consist of four conducting channel, therefore effective quantum capacitance is combination of four parallel capacitance is 4 times C_Q .In Hybrid Cu/SWCNT interconnect the SWCNT is cover with outer copper layer therefore the electrostatic capacitance is not present in Hybrid Cu/SWCNT interconnects.

The Capacitance of bundle for hybrid Cu/CNT is given by [42]

$$C_{BUNDLE} = n_{CNT}(4C_Q) \tag{3.15}$$

Where n_{CNT} is number of SWCNT in a bundle.

3.5.3 Inductance of Hybrid Cu/SWCNT

The inductance of Hybrid Cu/CNT is consist of parallel combination of inductance of copper and SWCNT bundle.

$$\frac{1}{L_{HYBRID}} = \frac{1}{L_{CU}} + \frac{1}{L_{BUNDLE}} \tag{3.16}$$

Where L_{CU} is inductance of copper and L_{BUNDLE} is inductance of SWCNT bundle

3.5.3(a) Inductance of copper (L_{CU})

The Inductance of Copper wire as an interconnect is given by [43]

$$L_{Cu} = \frac{\mu l}{2\pi}\left(\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{22(w+t)}{l}\right) \tag{3.17}$$

Where μ, l, w and t are the permeability of copper, length of copper, width and thickness of copper interconnect respectively.

3.5.3(b) Inductance of SWCNT bundle (L_{BUNDLE})

An isolated SWCNT has two types of inductances associated with it: magnetic inductance and kinetic inductance. Magnetic inductance (L_M) is due to the total magnetic energy resulting from the current flowing in the wire. The kinetic inductance (L_K) arises from kinetic energy stored in each conducting channel of the CNT. The four parallel conducting channels in a CNT results in an effective kinetic inductance of $L_K/4$. The expressions for L_M and L_K are [44]

$$L_M = \frac{\mu}{2\pi}\ln\left(\frac{y}{d}\right) \tag{3.18}$$

$$L_K = \frac{h}{2e^2 v_F} \tag{3.19}$$

Since $L_K >> L_M$, the inclusion of L_K can have a considerable impact on the delay, But from the experimental evidence the large inductive effects expected due to L_M are not observed up to frequencies as high as 10 GHz. [45]

The inductance of a CNT bundle is given by the parallel combination of the inductances corresponding to each CNT forming the bundle. The inductance of CNT bundle is given by [46]

$$L_{BUNDLE} = \frac{L_M + (L_K/4)}{n_{CNT}} \tag{3.20}$$

Where n_{CNT} is number of SWCNT in bundle.

CHAPTER 4

SIMULATION RESULT AND DISCUSSION

4.1 Introduction

From equations (3.1-3.20) of RLC explained in Chapter 3 the equivalent resistance, capacitance and inductance of Copper and Hybrid Cu/CNT for global length is calculated. After finding these value they are fitted in equivalent circuit model to find delay and power dissipation of interconnect.

4.2 Impedance analysis of Hybrid Cu/SWCNT interconnect and its comparison with Copper interconnect

The resistance, capacitance and inductance are calculated from the equation in explained in Chapter 3. Table (4.2- 4.10) show the impedance parameters at 32nm, 22nm, and 16nm technology nodes for global interconnect length. Figure 4.1-4.9 show that comparison of impedance parameters of copper and Hybrid Cu/SWCNT at 32nm, 22nm, 16nm technology node for global length.

4.2.1 Parameters Used For Calculation

Table 4.1 ITRS 2005 based parameters for calculation at 32nm, 22nm and 16nm technology nodes [44].

Technology node (nm)		**32**	**22**	**16**
Local and Intermediate	**Width W (nm)**	32	22	16
	A/R	2	2	2
	ILD	54.4	39.6	27
	ρ_{cu}($\mu\Omega$ cm)	4.83	6.01	9.03
	C_{cu} (pF/m)	144.93	131.01	110.1
Global	**Width W (nm)**	48	32	24
	A/R	3	3	3
	ILD Thickness t_{ox} (nm)	110.4	76.8	52.5
	ρ_{cu}($\mu\Omega$ cm)	3.52	4.2	6.01
	C_{cu}	179.78	163.3	140

4.2.2 Impedance Parameters at 32nm Technology Node

4.2.2 (a) Resistance: The resistance of copper and Hybrid Cu/SWCNT is given in table 4.2. Figure 4.1 Compare hybrid Cu/SWCNT and Copper interconnect graphically for global length. It can be seen from Figure that Hybrid Cu/CNT has resistance approximately five times smaller than copper for all global length at 32nm technology node.

Table 4.2 Copper and Hybrid Cu/SWCNT resistance comparison at global interconnect length.

	Resistance (Ω)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	509.259	96.6
200	1018.57	192.3
300	1527.77	288.1
400	2037.037	383.8
500	2546.296	479.5
600	3055.5	575.2
700	3564.81	671.02
800	4074.07	766.7
900	4583.33	862.4
1000	5092.59	958.2

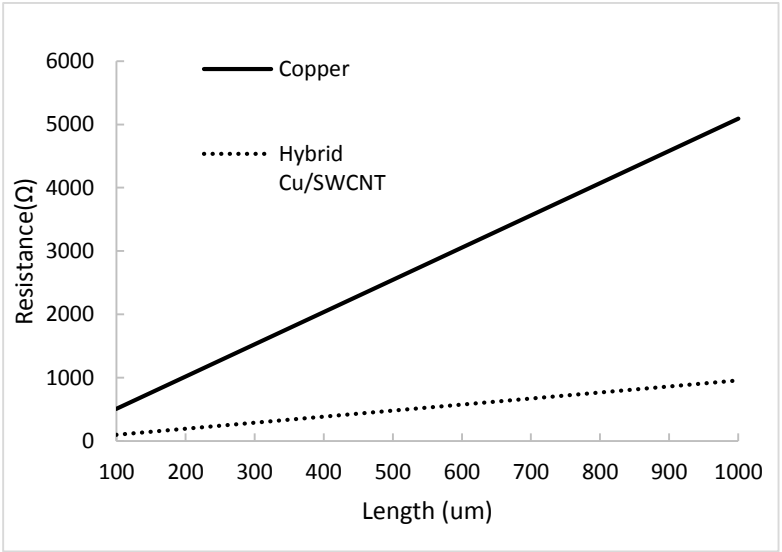


Figure 4.1 Comparison of resistance of Copper and Hybrid Cu/CNT for different global length at 32nm technology node

4.2.2 (b) Capacitance : The capacitance of Cu and Hybrid Cu/SWCNT is shown in table 4.3. Figure 4.2 shows the graphical comparison of Hybrid Cu/SWCNT for global length. It can be seen from figure that Hybrid has capacitance comparable to the copper all global length.

Table 4.3 Copper and Hybrid Cu/SWCNT capacitance comparison at global interconnect length.

	Capacitance (ρF)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.0181	0.0217
200	0.0362	0.0484
300	0.0544	0.0651
400	0.0726	0.072
500	0.09	0.09
600	0.108	0.108
700	0.126	0.122
800	0.145	0.145
900	0.163	0.163
1000	0.181	0.217

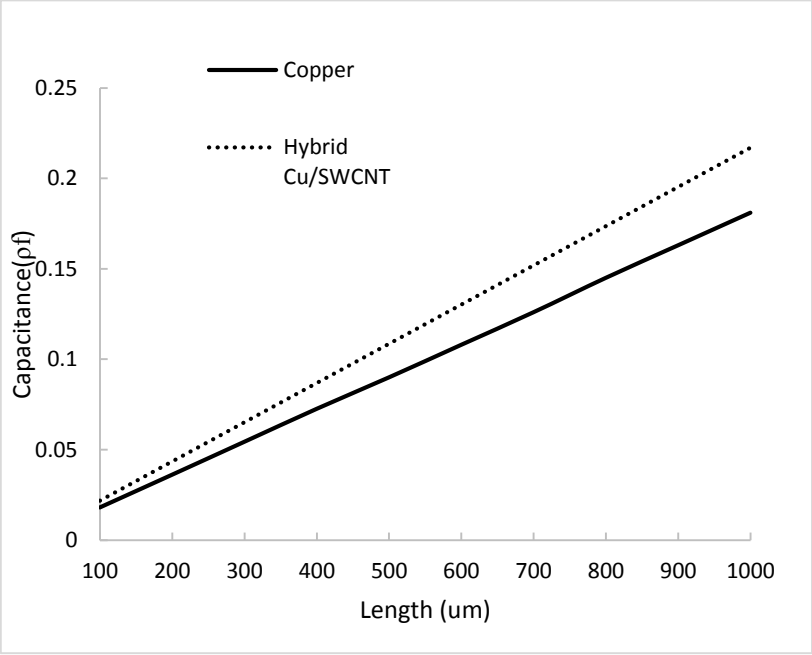


Figure 4.2 Comparison of capacitance of Copper and Hybrid Cu/CNT with global length at 32nm technology node

4.2.2(c) Inductance: The inductance of Copper and Hybrid Cu/SWCNT comparison is given in table 4.4. Figure 4.3 show the graphical comparison inductance of these interconnect for global length. It can be seen from figure that Hybrid Cu/SWCNT has less value of inductance in comparison to copper inductance for all global length.

Table 4.4 Copper and Hybrid Cu/SWCNT inductance at global interconnect length.

	Inductance (nH)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.1528	0.015282
200	0.333	0.030563
300	0.524	0.0458
400	0.722	0.0611
500	0.925	0.0764
600	1.1319	0.0916
700	1.3419	0.1069
800	1.55	0.122
900	1.775	0.137
1000	1.988	0.1528

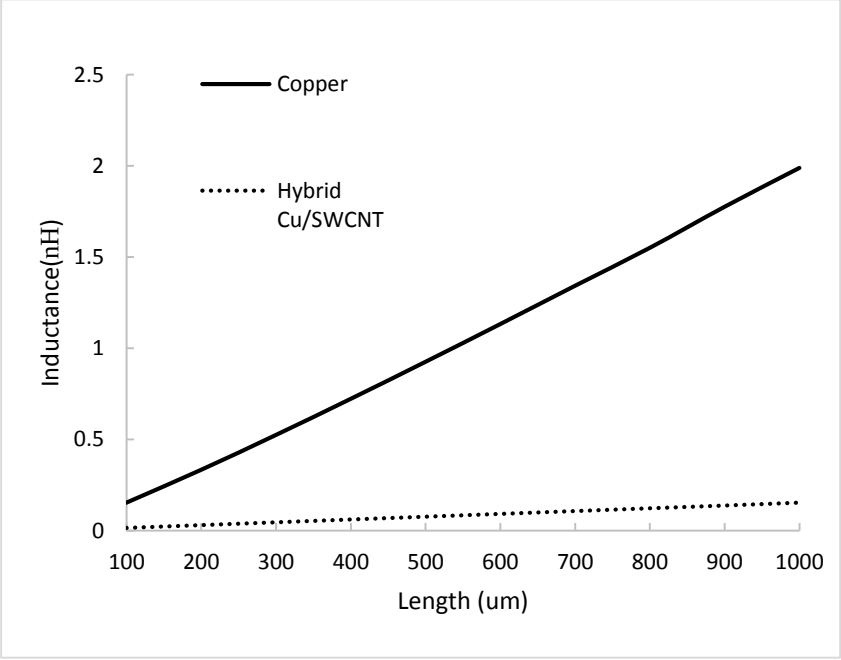


Figure 4.3 Comparison of inductance of Copper and Hybrid Cu/SWCNT for different global length at 32nm technology node

4.2.3 Impedance Parameters at 22nm Technology Node

4.2.3 (a) Resistance: The Hybrid Cu/SWCNT and copper interconnect resistance is shown in table 4.5. Figure 4.4 compare the resistance of copper and Hybrid Cu/SWCNT graphically for global length at 22nm technology node. It can be seen from the figure the Hybrid interconnect has very small resistance in compare to copper interconnect.

Table 4.5 Copper and Hybrid Cu/SWCNT resistance at global interconnect length.

	Resistance (Ω)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	1364	256
200	2734	511
300	4101	765
400	5468	1020
500	6835	1275
600	8203.1	1529
700	9570.3	1784
800	10937.4	2038
900	12304.67	2293
1000	13671.87	2547

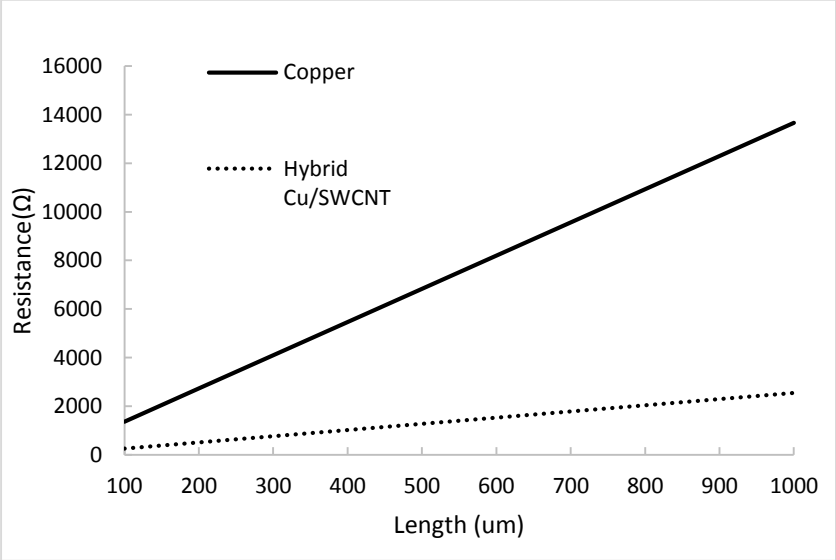


Figure 4.4 Comparison of resistance of Copper and Hybrid Cu/SWCNT for different global length at 22nm technology node

4.2.3 (b) Capacitance: Capacitance of copper and Hybrid Copper/CNT is shown in table 4.6. Figure 4.5 shows the graphical comparison of Hybrid Copper/CNT and copper interconnect with global length. It is clear from figure that both interconnect has comparable value of capacitance at 22nm technology node.

Table 4.6 Copper and Hybrid Cu/SWCNT capacitance at global interconnect length.

	Capacitance (ρF)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.0167	0.0157
200	0.0334	0.0314
300	0.0501	0.0471
400	0.0668	0.0628
500	0.0835	0.0785
600	0.1002	0.0922
700	0.1169	0.1099
800	0.1336	0.1256
900	0.1503	0.1463
1000	0.167	0.157

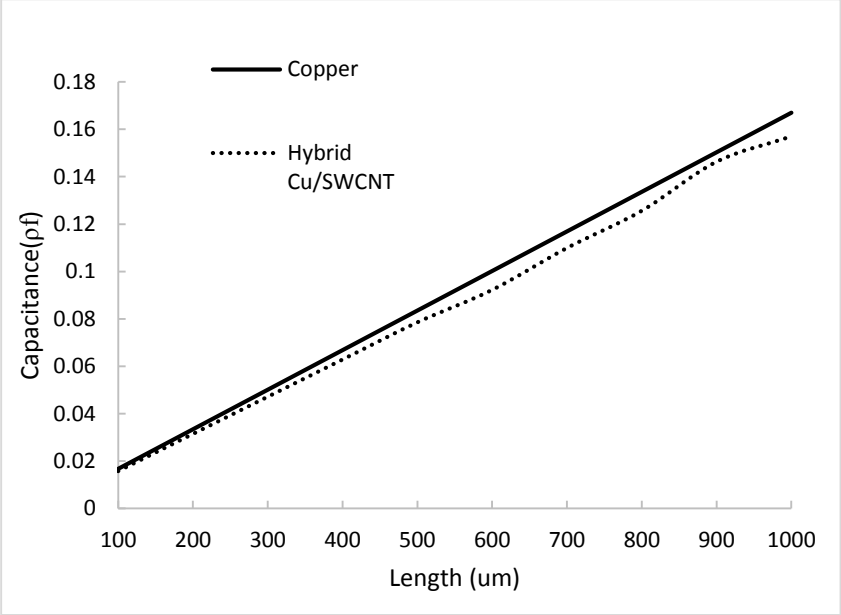


Figure 4.5 Comparison of capacitance of Copper and Hybrid Cu/SWCNT for different global length at 22nm technology node

4.2.3 (c) Inductance: The Inductance of Copper and Hybrid Cu/SWCNT shown in table 4.7. Figure 4.6 compare the inductance of Hybrid Cu/SWCNT and copper interconnect for different global length at 22nm technology node. It can be seen that Hybrid has less inductance value that copper. In Hybrid, CNT is used in with copper and CNT has very less value of inductance. Therefore Hybrid interconnect has less value of inductance.

Table 4.7 Comparison of copper and Hybrid Cu/SWCNT resistance at global interconnect length.

	Inductance (nH)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	.157	0.036
200	.341	0.073
300	.537	0.1105
400	.739	0.1473
500	.946	0.184
600	1.157	0.221
700	1.371	0.257
800	1.589	0.294
900	1.809	0.331
1000	2.030	0.368

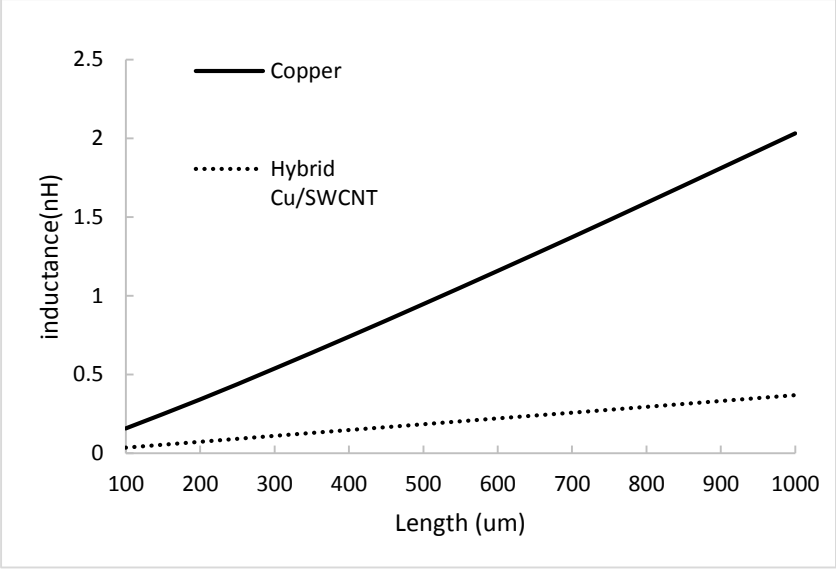


Figure 4.6 Comparison of inductance of Copper and Hybrid Cu/SWCNT for different global length at 22nm technology node

4.2.4 Impedance Parameters at16nm Technology Node

4.2.4 (a) Resistance: Table 4.8 shows the resistance comparison of Hybrid Cu/CNT and copper for different length. Figure 4.7 compare the Hybrid and copper resistance graphically. It can be seen from figure that Hybrid has less value of resistance than copper interconnect for all global length at 16nm technology nodes.

Table 4.8 Comparison of copper and Hybrid Cu/SWCNT resistance at global interconnect length.

	Resistance (Ω)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	3009	518.46
200	6018	1032.13
300	9027	1545.79
400	12037	2059.45
500	15046	2573.121
600	18006.5	3086.783
700	21064	3600.446
800	24074	4114.108
900	27083	4627.77
1000	30092	5141.43

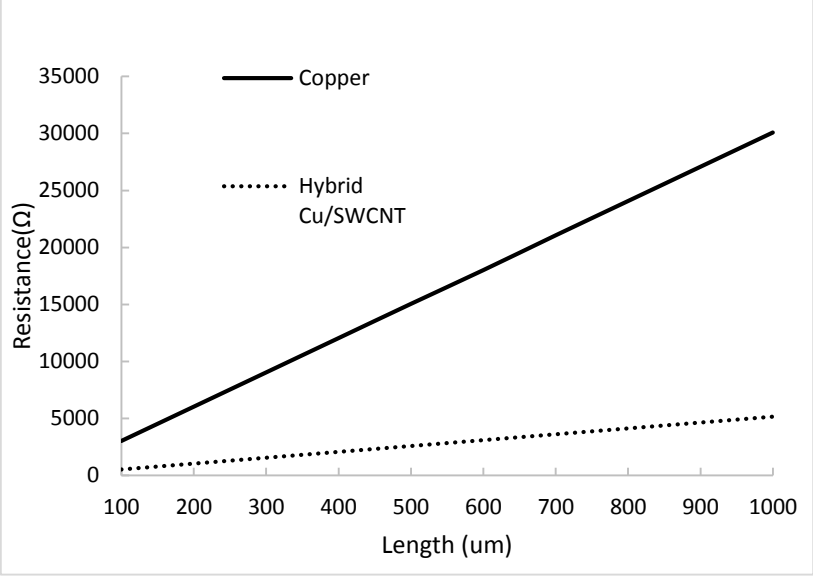


Figure 4.7 Comparison of resistance of Copper and Hybrid Cu/SWCNT for different global length at 16nm technology node

4.2.4 (b) Capacitance: Table 4.9 shows the Hybrid Cu/SWCNT and copper interconnect capacitance for different global length. Figure 4.8 compare the capacitance of Hybrid Cu/SWCNT and copper interconnect. It can be seen from the figure that they have comparable capacitance at 16nm technology node.

Table 4.9 Copper and Hybrid Cu/SWCNT capacitance at global interconnect length.

	Capacitance (ρF)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.0174	0.0105
200	0.0348	0.0211
300	0.0522	0.0317
400	0.0696	0.0423
500	0.087	0.0529
600	0.1044	0.0635
700	0.1218	0.0741
800	0.1392	0.0847
900	0.1566	0.0953
1000	0.174	0.105

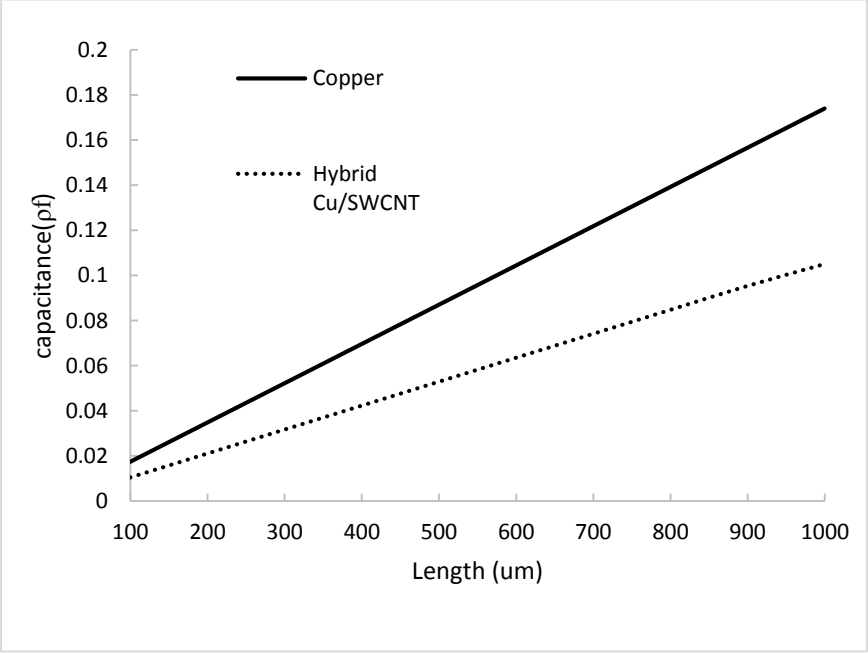


Figure 4.8 Comparison of capacitance of Copper and Hybrid Cu/SWCNT for different global length at 16nm technology node.

4.2.4(c) Inductance: The Inductance of Copper and Hybrid Cu/SWCNT shown in table 4.10. Figure 4.9 compare the inductance of Hybrid Cu/SWCNT and copper interconnect for different global length at 16nm technology node. It can be seen that Hybrid has less inductance value that copper. In Hybrid CNT is used in with copper and CNT has very less value of inductance. Therefore Hybrid interconnect has less value of inductance.

Table 4.10 Comparison of copper and Hybrid Cu/CNT inductance at global interconnect length.

	Inductance (nH)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.162	0.0105
200	0.353	0.0211
300	0.554	0.0317
400	0.762	0.0423
500	0.975	0.0529
600	1.192	0.0635
700	1.412	0.0741
800	1.635	0.0847
900	1.861	0.0953
1000	2.088	0.105

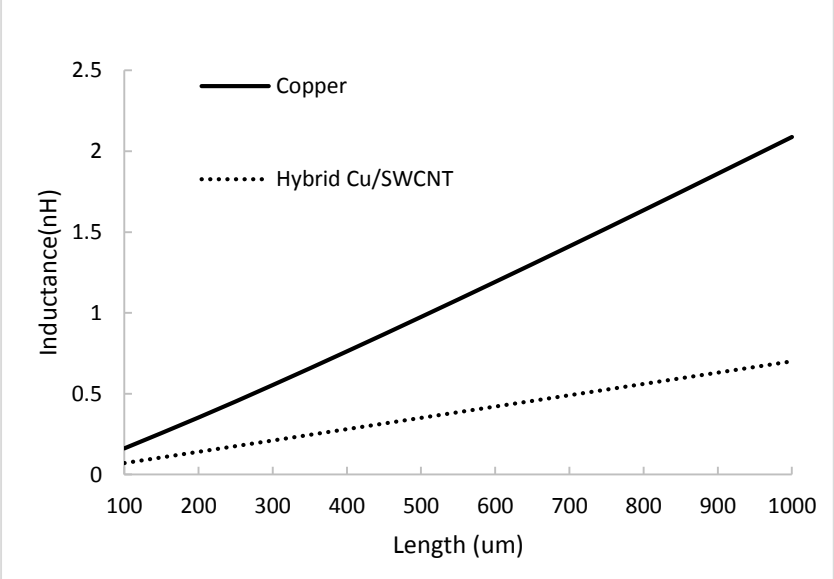


Figure 4.9 Comparison of inductance of Copper and Hybrid Cu/SWCNT for different global length at 16nm technology node.

4.3 Delay Analysis

The value of resistance, capacitance and inductance of global interconnect calculated in previous section are used for calculation of propagation delay. The optimum delay for optimum number of repeater are calculated using these value of resistance, capacitance and inductance using PTM model files [45].

4.3.1 Comparison of Copper and Hybrid Cu/SWCNT delay

The circuit considered for analysis comprise a CMOS-inverter driving a distributed RLC model of interconnect. A load capacitance of 10fF terminates interconnect and pulse with 20% rise time and fall time provides input to the CMOS inverter. The performance is studied by SPICE simulation at 32nm, 22nm, and 16nm technology nodes with Predictive technology model files (PTM) [45] and optimum number of repeaters are used.

4.3.2 Propagation Delay at 32nm Technology Node

At 32 nm technology node the optimum delay is observed at 40 aspect ratio of deriver with 10 number of repeater. Table 4.11 show the delay value of Copper and Hybrid Cu/SWCNT. Figure 4.10 show the comparison of delay of copper with Hybrid interconnect for different global length. It is observed that Hybrid interconnect has less value of delay as compare to copper interconnect. The delay is depends on RC value interconnect. As Hybrid has less value of resistance and capacitance in compare to copper at 32nm node Therefore Hybrid Cu/SWCNT has less delay in comparison to copper. The value of resistance and capacitance ins increase with length, therefore delay is also increase with interconnect length for copper and Hybrid interconnect.

Table 4.11 Delay value of copper and hybrid Cu/SWCNT interconnects for global length at 32 nm technology node.

	Delay (ρs)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	107	105
200	208	200
300	269	245
400	387	328
500	553.5	428
600	704	553
700	875	650
800	1070	738
900	1260	848
1000	1460	992

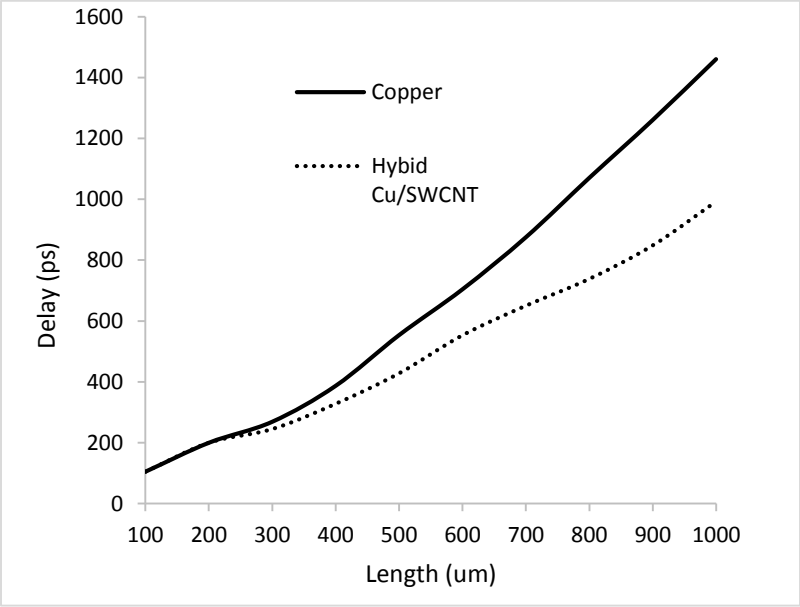


Figure 4.10 Delay comparison for Copper and Hybrid Cu/SWCNT interconnect for different length at 32nm technology node

4.3.3 Propagation Delay at 22nm Technology Node

At 22 nm technology node the optimum delay is observed at 40 aspect ratio of deriver with 11 number of repeater. Table 4.12 show the delay value on Copper and Hybrid Cu/SWCNT for different global interconnect length. Figure 4.11compare of delay of copper with Hybrid interconnect at different global length. It can be seen that Hybrid interconnect has

less value of delay as compare to copper interconnect. This is because the Hybrid Cu/SWCNT has small RC value than copper.

Table 4.12 Delay comparison of copper and hybrid Cu/SWCNT interconnects for global length at 22 nm technology node.

	Delay (ps)	
Length(um)	**Cu**	**Hybrid Cu/CNT**
100	203	162
200	373	273
300	583	446.5
400	866	611
500	1170	775
600	1650	967
700	2225	1160
800	3000	1325
900	3625	1550
1000	4160	1750

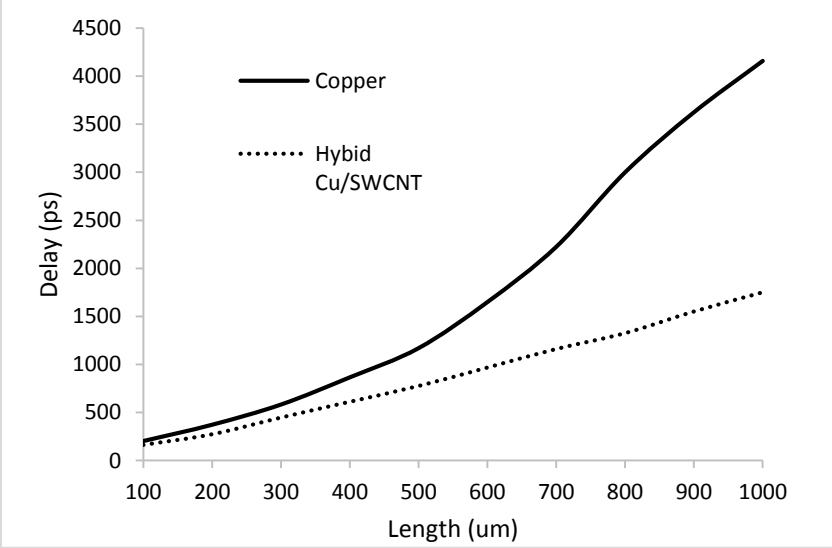


Figure 4.11 Delay comparison for Copper and Hybrid Cu/SWCNT interconnect for different global length at 22nm technology node

4.3.4 Propagation Delay at 16nm Technology Node

At 16 nm technology node the optimum delay is observed at 30 aspect ratio of deriver for 14 repeater. Table 4.13 show the delay value on Copper and Hybrid Cu/SWCNT. Figure

4.12 show the comparison of delay of copper with Hybrid interconnect for different global interconnect length. It can be seen from figure that Hybrid interconnect has less value of delay as compare to copper interconnect. Delay depends on the RC value of interconnect. For 16nm node the RC value of copper is more than Hybrid interconnect. Therefore Hybrid has less value of delay than copper. As resistance and capacitance of copper and Hybrid Cu/SWCNT increase with interconnect length therefore delay is also increase with increase in length.

Table 4.13 Delay of Copper and hybrid Cu/SWCNT interconnects for global length at 16 nm technology node.

	Delay (ρs)	
Length(um)	**Copper**	**Hybrid Cu/SWCNT**
100	212	145
200	465	227.5
300	757	300
400	1150	410
500	1615	556
600	2020	664
700	2600	793
800	4000	930
900	4910	1085
1000	5600	1210

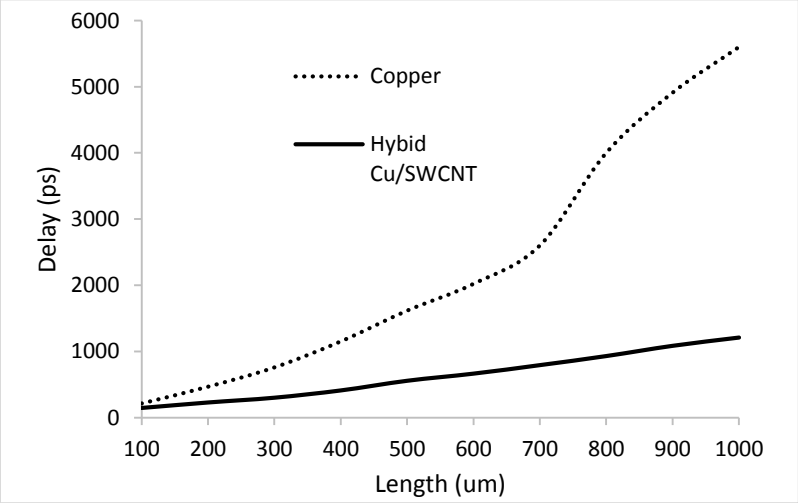


Figure 4.12 Delay comparison for Copper and Hybrid Cu/SWCNT interconnect for different global length at 16nm technology node.

4.4 Power analysis of interconnect

The power dissipation in VLSI circuits consists of two components,. Static and Dynamic. Static power is due to sub-threshold conduction through off transistors, tunneling current through gate oxide, leakage through reverse-biased diodes. Dynamic power dissipation is due to the power consumed by short circuit current when PMOS and NMOS are partially on and power consumed by the transistors while charging and discharging loading capacitors [48].

Charging and discharging power dissipation is directly proportional to square of supply voltage and linearly proportional to both loading capacitance and operating frequency. On the other hand short circuit power dissipation is proportional to the rise time and fall times of the input signal. So dynamic power is given by the expression [49]

$$P = C.V_{DD}.f_P \qquad (4.1)$$

Where C is load capacitance, V_{DD} is supply and f_P is the operating frequency.

So, dynamic power can be reduced by reducing the value of capacitance C. The increase in operating frequency (from eq. 1) leads to increase in power dissipation.

At different technology nodes, power dissipation of Hybrid Cu/SWCNT and copper interconnect is calculated and compared for different length at different technology nodes. The power dissipation can be reduced by increasing the diameter of carbon nanotubes because of decrease in capacitance of CNT bundle. [50] But the increase in diameter of CNT leads to increase in resistance and inductance, which increase the propagation delay of interconnect. Therefore a trade-off between delay and power can be made.

4.4.1 Power Dissipation at 32nm technology node

Tables 4.14 below give the SPICE simulated power dissipation for Hybrid Cu/SWCNT and Copper Interconnects respectively for 32nm technology. Figures 4.13 shows the graphically comparison of copper and Hybrid Cu/SWCNT interconnects power dissipation. The Figures show that copper interconnect has less power dissipation as compare to Hybrid interconnects. This is due to the large value of capacitance in Hybrid Cu/SWCNT than copper interconnects.

Table 4.14 Power dissipation comparison of copper and Hybrid Cu/SWCNT interconnect for different length at 32nm technology node.

	Power Dissipation (µW)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	0.9	2.2
200	0.9	2.3
300	0.9	2.4
400	0.9	2.6
500	1.1	2.62
600	1.2	2.6
700	1.2	2.6
800	1.1	2.5
900	1.1	2.6
1000	1.2	2.7

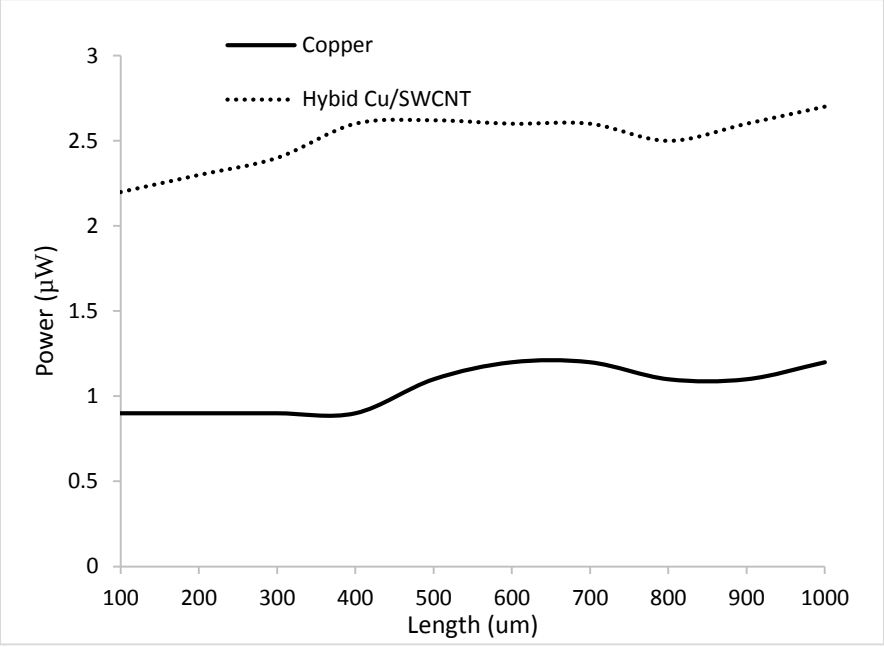


Figure 4.13 power dissipation comparison of copper and Hybrid Cu/SWCNT for global length at 32nm technology node

4.4.2 Power dissipation at 22nm Technology Node: Table 4.15 shows power dissipation for CNT and Copper Interconnects. Figure 4.14 shows the graphically comparison of copper and Hybrid Cu/SWCNT interconnect power dissipation. It can be

seen from figure than Hybrid interconnect has more power dissipation than copper interconnect. The power dissipation can be reduce by increasing the diameter of SWCNT bundles.

Table 4.15 Power dissipation comparison of copper and Hybrid Cu/SWCNT interconnect for different length at 22nm technology node.

	Power Dissipation (10E -7)	
Length (um)	**Cu**	**Hybrid Cu/SWCNT**
100	1.8	6.4
200	2.1	6.27
300	1.8	6.3
400	1.7	6.5
500	1.4	6.4
600	1.4	6.7
700	1.4	6.6
800	1.6	6.7
900	1.8	6.8
1000	1.8	6.9

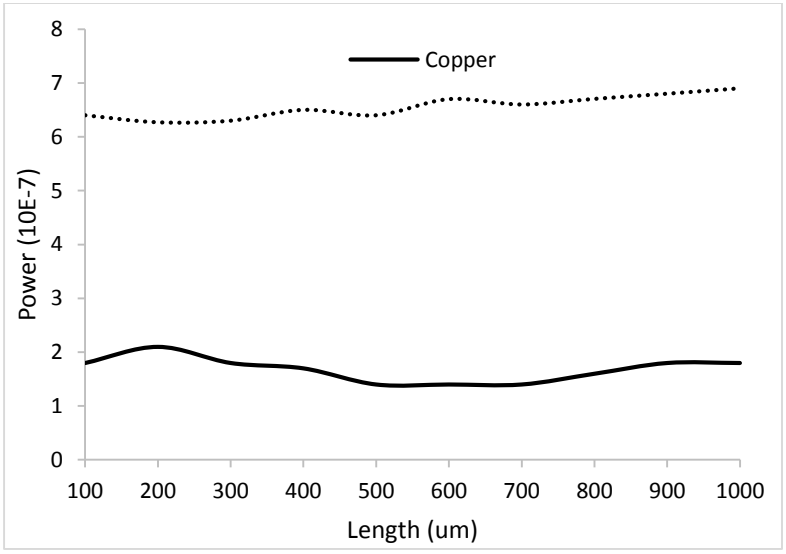


Figure 4.14 Power dissipation comparison of copper and Hybrid Cu/SWCNT for global length at 22nm technology node

4.4.3 Power Dissipation at 16nm Technology Node: comparison of power dissipation of Hybrid Cu/SWCNT and Hybrid interconnects is shown in table 4.16. Figure 4.15 shows

graphically comparison of copper and Hybrid Cu/SWCNT interconnect power. It can be seen from graph that the power dissipation is increasing with increase in length for Copper and Hybrid interconnect. Hybrid interconnect has more power dissipation than copper interconnect. This is due to the high value of capacitance of Hybrid Cu/SWCNT interconnects.

Table 4.16 Power dissipation comparison of copper and Hybrid Cu/SWCNT interconnect for different length at 16nm technology node.

	Power Dissipation (10E-7)	
Length (um)	**Copper**	**Hybrid Cu/SWCNT**
100	3.1	6.7
200	3.5	6.9
300	4	6.9
400	4	6.9
500	4.5	7.04
600	5	7.05
700	5	7.2
800	5	7.4
900	5	7.9
1000	5	7.9

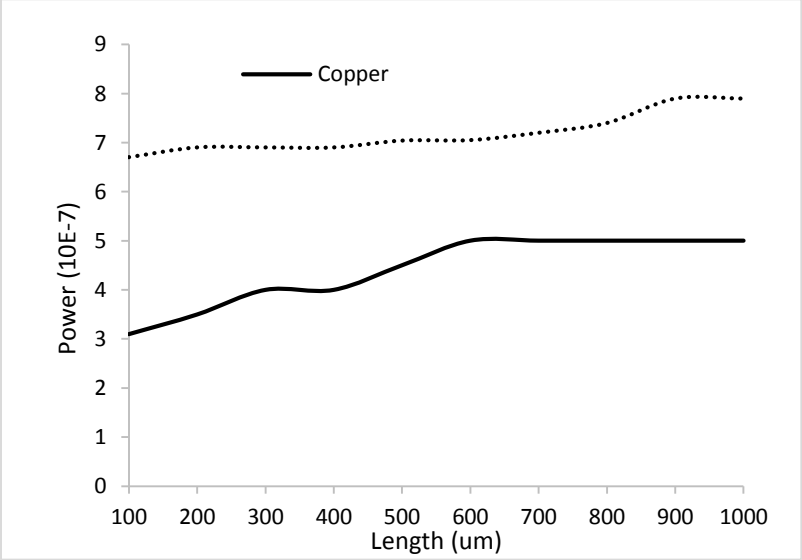


Figure 4.15 Power dissipation comparison of copper and Hybrid Cu/SWCNT for global length at 16nm technology node.

CHAPTER 5
CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The value of various parameters of interconnects viz. resistance, capacitance and inductance for Hybrid Cu/SWCNT interconnects have been calculated and compared with copper for different length at 32nm,22nm and 16nm techonology nodes As length of interconnect is increasing it can be seen that these parameter are increasing for Copper and Hybrid Cu/SWCNT interconnects.

Further the delay and power performance of Hybrid Cu/SWCNT and Copper interconnects have been compared for global length. Hybrid interconnects show significant improvement in delay performance as compared to copper interconnects. This is due to the fact that Copper have a resistance value much higher that of Hybrid Cu/SWCNT.

Power dissipation is observed for both Hybrid and Copper interconnects for different length. From the simulation results, it has been observed that the power dissipation is larger in Hybrid interconnect as compare to copper interconnects.

5.2 Future Scope

In this thesis, it is observed that Hybrid Cu/SWCNT can be used instead of copper as an interconnect material for the 32nm, 22nm and 16nm technology nodes. Further study on Hybrid Cu/SWCNT can be done for deep submicron voltage. In this thesis work, the delay and power analysis is done for 1Ghzs frequency. Further high frequency study can be done for Hybrid interconnects for delay and power analysis. A few work is done in the field fabrication of Hybrid Cu/SWCNT. Fabrication of Hybrid Cu/SWCNT interconnect can be performed and its physical structure, electrical and thermal property can be studied.

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