A Thesis Report

On

"Design of CMOS Operational Transresistance Amplifier with Improved Gain and Bandwidth"

Submitted towards the partial fulfillment of requirement for the award of degree of

Master of Technology

In

VLSI Design

Submitted by

Gitesh Mehta

Roll No: 601562010

Under the supervision of

Dr. Rishikesh Pandey

Assistant Professor

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

July 2017

DECLARATION

I, Gitesh Mehta hereby declare that the work presented in this thesis entitled "**Design of CMOS Operational Transresistance Amplifier with Improved Gain and Bandwidth**" in partial fulfillment of the requirement for the award of degree of Master of Technology submitted at Electronics and Communication Engineering Department, Thapar University, Patiala is an authentic record of work carried out under supervision of Dr. Rishikesh Pandey (Assistant Professor, ECED, Thapar University, Patiala). The matter presented in this thesis has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 11/08/2017

Gitesh Mehta

Roll No. 601562010

It is certified that the above statement made by the candidate is correct to the best of my knowledge and belief.

Date: 11/8/2017

Dr. Rishikesh Pandey

Assistant Professor

ECED, TU, Patiala

ACKNOWLEDGEMENT

This report has only been possible with the constant guidance and expertise of Dr. Rishikesh Pandey, Assistant Professor, Electronics and Communication Engineering Department, Thapar University, Patiala and I would like to take this opportunity to express my sincere gratitude to him.

I am also thankful to Dr. Alpana Agarwal, Head of ECE Department, for providing us the adequate infrastructure for carrying out the work.

I am also thankful to Dr. Hem Dutt Joshi, PG Coordinator as well as Dr. Anil Arora, Program Coordinator and the entire faculty and staff of Electronics and Communication Engineering Department for th**e** motivation and inspiration that triggered me for the work.

I would also like to thank my friends who always motivated me and have more or less contributed to the preparation of this report. I will be always indebted to them.

Last but not the least, I would like to thank my parents for their years of unyielding love and encourage. They have always wanted the best for me and I admire their determination and sacrifice.

ABSTRACT

Longer shelf life, fast operating speed are necessities for portable electronics systems. Ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain, as the current-mode circuits are low impedance node networks, and thus low time constant circuits, too. This improves system performance in terms of speed and slew rate. OTRA uses current mode designing techniques. In OTRA shunt-shunt feedback is used which makes amplifier and feedback network parallel and parallel networks support low power supply. Because of use of current-feedback technique, OTRA has bandwidth independent of closed loop voltage gain

In this thesis, a novel OTRA has been designed with improved gain and bandwidth. The proposed circuit provides gain of 165.76db and 3db bandwidth of 663.24Khz. The vital parameters of proposed circuit have also been compared with existing OTRA circuits. The proposed circuit is simulated using cadence in 180 nm CMOS technology parameters with supply voltages of ±.9 V. Corner analysis also has been performed. The comparison of proposed OTRA with OTRAs available in literature survey shows that there is considerable increase in gain and bandwidth.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACRONYMS

OTRA	Operational Transresistance Amplifier
DC	Direct Current
AC	Alternating Current
CMOS	Complementary Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
MDCC	Modified Differential Current Conveyor
CM	Current-Mode
VM	Voltage-Mode
PMOS	Positive-channel Metal Oxide Semiconductor
NMOS	Negative-channel Metal Oxide Semiconductor

CHAPTER 1

INTRODUCTION

With the evolution of VLSI technology the level of integration of millions of transistors on a single chip has forced downscaling. Low power, low voltage mixed mode circuits has become essential requirement due to requirement of portable and high performance equipments in electronics market. This requires the scaling of CMOS technology, however, threshold voltage does not scale in a linear fashion with the reduction in minimum device length. The reliability and density factors associated with technology scaling demand for reduced supply voltages. This trend of continuous reduction of the supply voltage does not put restriction on the digital circuit design but possess serious challenges such as reduced input common mode range, reduced output swing and linearity for analog circuit design. To circumvent this conflict instead of using costly CMOS technologies with lower thresholds, it is desirable to use low voltage circuit techniques that are compatible with standard CMOS processes. The voltage-mode circuits are required to provide large output swing while minimizing the total power consumption. This leads to high impedance node architecture of the voltage-mode circuits. However, the parasitic capacitances present in the circuits need to be charged and discharged with large voltage swing, thereby limiting the speed and slew rate of these circuits. Thus, simultaneous low voltage, low power and wide bandwidth operations are difficult to achieve in voltage-mode circuits. Over the last few decades current-mode processing has emerged as an alternative design technique using current signals for signal processing [1]. The current-mode circuits are low impedance node networks, and thus low time constant circuits, too. This improves system performance in terms of speed and slew rate. In current amplifiers the transistors are useful almost up to their unity gain bandwidth, thereby resulting in wider bandwidth. Additionally, in current-mode circuits the addition and subtraction operation can be performed by joining the terminals at a single point resulting in simple architecture as compared to voltage-mode circuits. This may result in power and chip area saving. Thus ever shrinking feature size of devices on ICs and consequential reduction of power supply voltage can be handled by operating in the current domain. Current-mode signal processing has led to emergence of numerous analog building blocks employing current-mode technique. In order to maintain compatibility with existing voltage mode circuits it is necessary to convert signal in voltage form to signal in current form and vice versa hence block like operational transresistance amplifier (OTRA) is emerged.

1.1 THE OTRA

OTRA is a high gain, current input, voltage output device which employ current mode circuit technique. The equivalent circuit of an OTRA is shown in Figure 1.1 [2]. An Ideal OTRA senses the currents at its two input terminals p and n, amplifies the difference in current at 'p' and 'n' terminals and transfers it to output node in terms of voltage. For ideal operations the input terminals should be grounded. Also the output voltage should be independent of the current that may be drawn from the output terminal by the load impedance. The port characteristics of OTRA can be expressed as:

$$V_o = R_m(I_p - I_n)$$

Where R_m is transresistance gain of OTRA. For ideal operations the R_m approaches infinity and forces the input currents to be equal. Though these idealized conditions cannot be realized practically yet the use of such an ideal OTRA model simplifies the mathematical analysis of OTRA circuits. The practical OTRA circuits are made to approximate the idealized characteristics.

OTRA in the simplest way can be used in an open loop configuration; however, its gain being infinity the output voltage saturates either at positive or negative saturation level. This operation has a limited number of applications. Thus OTRA should be used in a negative feedback configuration where the output is not driven into saturation and the circuit behaves as an amplifier.

.

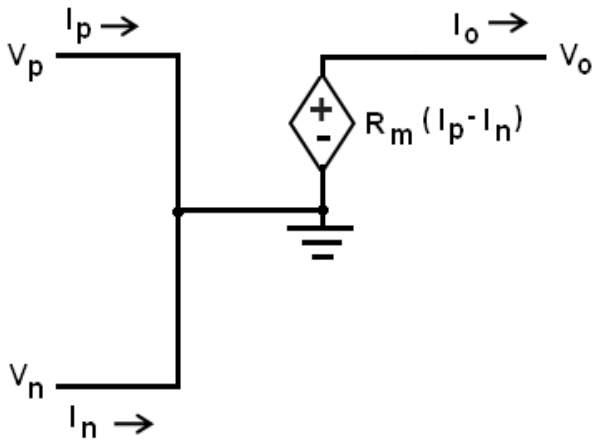

Figure 1.1 OTRA equivalent circuit [2]

The OTRA uses shunt-shunt feedback configuration which places the feedback network and amplifier in parallel. A parallel configuration is suitable for low voltage operations as it minimizes stacking of transistors thereby providing more head room for signal swing. Also using current feedback techniques makes OTRA's bandwidth almost independent of closed-loop gain.

The symbolic representation of OTRA is shown in Figure 1.2 [3]. If one terminal of a nullator is connected to the ground, the other terminal is considered as virtual ground so a low impedance node is obtained. Also, the nullator does not allow passage of current through it. In OTRA the currents I_p and I_n enter into the low impedance input terminals. This can also be modeled with the nullor if one terminal of the nullator is connected to the ground and the current at input is flowing through the norator. Hence, both the input terminals of OTRA can be modeled by using current followers (CFs) and the output voltage is equal to the difference of the input currents multiplied by transresistance gain R_m. A voltage follower consisting of a nullor is used at the output terminal to reduce output impedance.

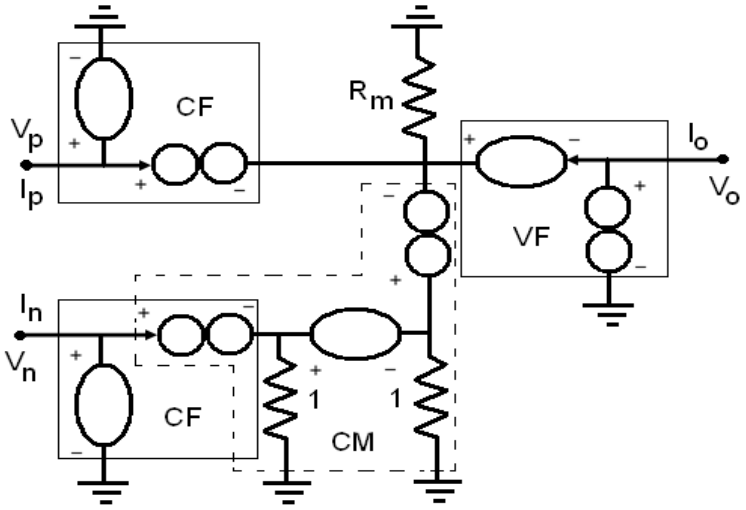

Figure 1.2 symbolic representation of OTRA [3]

1.2 MOTIVATION

Motivation to study and design a better operational transresistance amplifier (OTRA) comes from the fact that longer shelf life, fast operating speed are necessities for portable electronics systems nowadays. Circuits which operate on lower supply voltages and have larger bandwidth are in trend these days, since OTRA senses current at input and provide voltage at output terminal a shunt-shunt feedback is used which makes amplifier and feedback network

parallel and parallel networks support low power supply as it minimizes transistor stacking therefore providing more head room for signal swing. OTRA uses current-feedback technique so it has bandwidth independent of closed loop voltage gain. OTRA benefits from current mode designing techniques and simultaneously provides voltage at output port so is capable of driving voltage mode circuits directly. Also its input terminals are grounded and output impedance being low it is insensitive to parasitics so eliminating response time limitations. In this work OTRA as basic building block is presented with the objective of improving gain, decreasing voltage supplies and increasing bandwidth.

1.3 ORGANIZATION OF THE THESIS

The thesis is organized as follows:

Chapter 1: introduces the evolution of current mode signal processing and a brief study of the OTRA with an aim to bring most of the information related to OTRA implementations.

Chapter 2: describes literature review in the field of OTRA and various circuit based on OTRA.

Chapter 3: addresses the circuit description for proposed OTRA and transresistance gain calculations.

Chapter 4: It contains the simulation results of the proposed OTRA and the proposed OTRA with compensation circuit. The corner analysis of the proposed OTRA has also been performed and presented.

Chapter 5: In this chapter, the conclusion of the thesis and the future scope of OTRA have been addressed.

CHAPTER 2

LITERATURE SURVEY

This chapter discusses the recent researches and developments in the field of operational transresistance amplifier (OTRA) reported by various authors in literature [4-39].

Chen *et al.* [4], presented two-port operational transresistance amplifier (OTRA). Which has transmission properties similar to the current feedback operational amplifier but it has two input nodes and one output node with low impedances. Being a basic building block in analog Integrated circuits, OTRA is used to implement MOSFET-C differentiator which has gain independent constant bandwidth.

Chen *et al*. [5], presented MOSFET-C integrator and differentiator using OTRA proposed in [4]. Effects of parasitic capacitances are minimized and use of external elements for compensation is not required in the presented circuits. Two universal biquad filters using these circuits are also presented. These presented filters are tunable with gate voltage variations. Using these filters a second order bandpass and Chebyshev filters are realized.

Chiu *et al.* [6], reported a linear integrator using operational transresistance amplifier presented in [4]. The number of capacitors and transistors used in the proposed circuit are less than the circuit presented in [5]. The chip area of the proposed circuit is also reduced as only one capacitor is used and problem of capacitor mismatch is eliminated. The proposed integrator is insensitive to parasitic capacitances and can be interconnected without buffer. Operational transresistance amplifier reported is used in realising multiplier, voltage amplifier, continuous time filters, quadrature oscillator and integrator. These circuits have constant bandwidth virtually independent of gain.

Riewruja *et al*. [7], presented a signal power amplifier which has low input and output impedances because of negative feedback and output driver circuit used. Bandwidth of the proposed transresistance amplifier is constant and does not depends on closed loop gain. The feedback network is responsible for bandwidth and linearity enhancement of amplifier. The gain of OTRA can be tuned by adjusting the biasing current. The proposed circuit consists of the new design of transresistance amplifier cell connecting with the common Source negative feedback and the output driver circuit. The bandwidth of the circuit is high as compared to [6].

Voltage mode MOS-C integrator is proposed in [8] which has reduced parasitic capacitance effect. Required capacitor are few. Based on presented MOS-C integrator, two biquad filters

are also presented. The filters are cascadable as OTRA used in these filters has low output impedance. Third order filter that is a Chebyshev low pass filter is realized. The proposed signal processing circuits directly process voltage signals, also tuning can be done by altering gate voltages of the MOS transistors.

A class AB operational amplifier topology based on a floating low series input resistance has been presented in [9]. The propose amplifier has high gain and low power dissipation compared to [7]. The proposed circuit uses first generation current conveyor circuit as a floating input stage.

Kilinc *et al*. [10], presented a voltage-mode filter configuration. Second-order allpass and notch filtering functions are realized using single operational transresistance amplifier (OTRA). The proposed circuit configurations is insensitive to parasitic capacitances because of internally grounded input terminals of OTRA. Low output impedance of the configuration enables cascading without additional buffers.

Jae Yoo *et al.* [11], represented a transresistance amplifier in which current feedback is employed in the circuit for reduction of stacking of devices between the supply rails and to decrease the voltage signal swings, making it operatable at low voltage operation. A variable gain amplifier which is based on R-2R ladder is designed using the transresistance amplifier.

Keskin *et al.* [12], reported a minimum component oscillators (MCOs) based on grounded negative impedance using four active elements named operational transresistance amplifier, second generation positive current conveyor, current differencing buffered amplifier, and operational transresistance amplifier. These circuits have low component sensitivities with respect to the frequency.

Cekir *et al*. [14], suggested a configuration which uses an operational transresistance amplifier and a few passive elements, to implement both first order and second order allpass filters. Due to internal grounding of input terminals of OTRA, the circuit is insensitive to parasitics. The unity gain bandwidth is quite higher than conventional operational amplifier. Circuit applications are also shown by realizing the quadrature oscillator, the phase equalizer and band pass filter for analog signal processing.

Hwang *et al*. [15], reported a high-order OTRA based MOSFET-C filters which have reduced parasitic capacitance effects are presented in. Proposed filters have constant bandwidths because of the use of current-feedback configuration in OTRA. The proposed filter

configurations has simple design equations, efficient design procedures, and systematic circuit architectures.

Square wave generators using minimal external passive elements and one operational transresistance amplifier is reported in [16]. Two different circuits are presented in which the first one is general multivibrator producing almost symmetrical square wave having fixed duty cycle corresponding to different frequencies and the second circuit is square wave generator in which adjusting passive element's values the ON and OFF duty cycles of square wave can be controlled.

Massarotto *et al.* [17], presented an approach based on a two-stage topology to design differential charge and transresistance amplifiers that are high in performance is proposed. Common mode rejection is performed at first stage also this stage performs a signal conversion from differential to single ended output. The second stage used for filtering the signal. The proposed circuit have very good CURRENT-MODERR that depends only on the matching of resistors.

Hasan Mostafa *et al.* [18], proposed CMOS realization of modified operational transresistance amplifier. The proposed MOTRA is cascade of modified differential current conveyor and a common source amplifier. Bandwidth, gain of proposed OTRA is higher than OTRA presented in [4]. Based on presented OTRA, voltage gain amplifier (VGA) which is digitally controlled is also implemented.

A simple monostable multivibrator employing current mode technique is presented in [19]. The multivibrator uses OTRA as main active building block along with minimum external passive elements. Positive and negative triggering modes can be used for triggering, at different input terminals in proposed topology.

Kung Lo *et al*. [20], reported a switch controllable triangular and square wave generator. The main components of circuit are two OTRAs and a small number of passive components with three switches. DC level of triangular waveform is adjustable. The presented triangular and square wave generator can operate under inverting and non-inverting hysteresis, when operated by controlling single pole double through switches. The bandwidth of circuit using OTRA are higher than the bandwidth using conventional operational amplifier discussed.

Kafrawi *et al*. [21], suggested a differential operational transresistance amplifier (OTRA). The OTRA is used to implement Tow Thomas Biquad Filter. The circuit has used differential gain stage at output as compared to common source stage used in [18] hence gain is improved than

[6] and additional circuitry is used for the compensation of the difference between the drain voltages M2 and M3 transistors.

Two bistable multivibrator has been presented in [22]. Two different topologies have been presented in, the first one contains only OTRA and a positive feedback network whereas the second one uses (single pole double throw) switch with a biasing source to shift hysteresis either into left half part or in right half part of the voltage plane. These two proposed circuits can be operated under both clock wise hysteresis operations.

Kafrawi *et al*. [23] proposed a modified CMOS operational transresistance amplifier with differential input. The proposed circuit realized by cascading modified differential current conveyor (MDCC) with differential amplifier at the output which has improved gain and decreased offset current than OTRA circuit presented in [17]. Based on proposed realization a variable gain amplifier is also presented which is digitally controlled voltage mode amplifier.

Two sinusoidal circuits based on differential operational transresistance amplifier are presented in [24]. One circuit is capable of producing n-odd phase oscillations which are spaced equally in phase and have equal amplitudes, the other circuit produces n-odd or n-even phase oscillations. Presented circuits have wide range of frequency of oscillation with added advantage of employing current mode design technique while providing voltage at the output terminal. An alternative approach is also discussed which utilizes tunable oscillator circuit to inject signal into phase shifter.

F. Kacar *et al* [25], proposed filter topologies which use current mode processing technique. The proposed topologies use operational transresistance amplifier so filters are parasitic insensitive hence removed response time limitations and the cut off frequency is quite high. The proposed first-order allpass filter is used to realize the quadrature oscillator.

A sinusoidal oscillator which is based on an operational transresistance amplifier is reported in [26]. The oscillator provides independent control on condition of oscillation and frequency. Passive sensitivity of structure is quite low due to internally grounded OTRA terminals hence the circuit is insensitive to parasitic capacitances.

Voltage controlled oscillators which are based on differential operational transresistance amplifier are demonstrated in [27]. The circuits proposed are easy to realize and have quite low component count. In these circuits just by controlling resistor's values tuning range and sensitivity can be configured. Two voltage controlled oscillators have been proposed which provide low output impedance and low parasitics at the input and hence range of frequency of

oscillation is high. Using the triangular and square wave, sinusoidal waves can be formed at the output and voltage swing at the output is high.

Banerjee *et al.* [28], introduced a first order voltage mode multifunction. It uses three OTRA and few passive elements that is three capacitors and six resistors. All the passive elements are virtually grounded as the inputs of Operational Transresistance Amplifier are virtually grounded. Hence effect of parasitic elements are minimised and total harmonic distortion is very low. Single topology is used for the realization of first order high pass, low pass, and all pass filter functions, all the filter functions can be tapped simultaneously form the presented topology.

Singh *et al.* [29], presented an improved wireless optical receiver section. The proposed receiver section is based on a trans-impedance band pass filter using a differential operational transresistance amplifier. The improved receiver provides higher bandwidth independent of gain this is due to the fact as earlier used bootstrapping involves coupling loss but same is not true with use of OTRA.

Analog multiplier using OTRA is proposed in [30]. The proposed circuit does not use any passive component externally so it is suitable integrator applications. Total harmonic distortion and power dissipation of the proposed circuit is low. Using this circuit, amplitude modulator and squarer circuits are implemented.

Ghosh *et al*. [31], presented a multi input single output filter which is a third order voltage mode filter using an OTRA. High pass, all pass, low pass, bandpass and notch responses are realized from the same topology. Passive components matching is required in the proposed topology. All the capacitors are virtually grounded, so the proposed topology is suitable for IC implementation and effect of finite gain can be reduced by self compensation methodology.

Kumngern *et al*. [32], a single input and three outputs voltage-mode biquadratic filter has been presented which employs OTRAs as a basic building block. Compared with other OTRA-based filters, the proposed filter possesses no requirements for component-matching conditions for realizing high pass, band pass and low pass filter responses, also the proposed filter uses less active and passive components.

Approach for designing field programmable operational transresistance amplifier is demonstrated in [33]. Floating gate MOSFETs are used to make the OTRA programmable. The floating gate charge can be programmed after fabrication, based on hot-electron-injection and

fowler-nordheim tunnelling techniques. The proposed circuit's offset variation is not of significant amount.

Kumngern *et al*. [34], presented third-order quadrature oscillator which uses operational transresistance amplifiers as active elements. The proposed circuit comprises three OTRAs, three capacitors and five resistors. High precision of the frequency of oscillation can be achieved by the proposed circuit and a single passive component is needed to control.

Pittala *et al.* [35], demonstrated a quadrature oscillator using the OTRA. The presented quadrature oscillator uses two OTRAs as main active analog building blocks and a minimal number of passive components to generate the oscillations. Independent control over the oscillation condition and frequency of oscillation is provided by the circuit.

Singh *et al*. [36], presented an analog timer circuit which is used to design monostable and astable multivibrators. Astable multivibrator using proposed timer circuit generates a periodic waveform of variable duty cycle. The proposed circuits are insensitive to input parasitics and can operate at very low power supply also presented circuit does not suffer from constant gain bandwidth product.

The OTRA based grounded inductor is presented in [37]. Using this the band pass filter is designed. The bandwidth of the circuits implemented using proposed topology can changed by modifying the resistance and capacitance value.

Goel *et al*. [38], presented the design of voltage reference circuit using OTRA. The OTRA used works as a high gain amplifier which uses voltage-shunt feedback that enables the proposed voltage reference to operate at low power supply it uses negative feedback to have stable operation so voltage variation over a large range of temperature is very low.

Torteanchai *et al.* [39], reported a quadrature oscillator is demonstrated. To realize proposed circuit OTRA is used as it offers high slew rate and low parasitics, hence oscillating frequency with great precision can be achieved. The presented oscillator possesses low input impedance so it can be connected without buffer and the frequency of oscillation is high. The oscillating conditions and oscillating frequency can be controlled independently in the proposed topology.

CHAPTER 3

OPERATIONAL TRANSRESISTANCE AMPLIFIER WITH IMPROVED GAIN

3.1 PROPOSED OTRA CIRCUIT DESCRIPTION

In this chapter a novel operational transresistance amplifier has been proposed. In section 3.1 circuit description of proposed operational transresistance amplifier has been presented and section 3.2 describes proposed OTRA with compensation circuit.

The CMOS realization of high gain Operational Transresistance Amplifier is shown in Figure 3.1. It is based on cascading of modified differential current conveyor (MDCC) [2] and gain stage which is differential amplifier with increased output resistance due to cascode configuration. Transistor (M1 - M3), (M5, M6), (M8 - M11) and (M12, M13) are perfectly matched all the transistors are in saturation region. Transistors M8-M11 forms current mirror as they are matched forcing current ($I_{b)}$ current through M4 to be equal to the current passing through transistors M1, M2 and M3. This drives the gate-source voltages of M1, M2 and M3 to be equal which forces the two input terminals ($_{I+ \text{ and } I-)}$ to be grounded virtually as gate of M1, M2 and M3 are at same potential and for current to be same, the source terminals of M1-M3 also need to be at same potential.

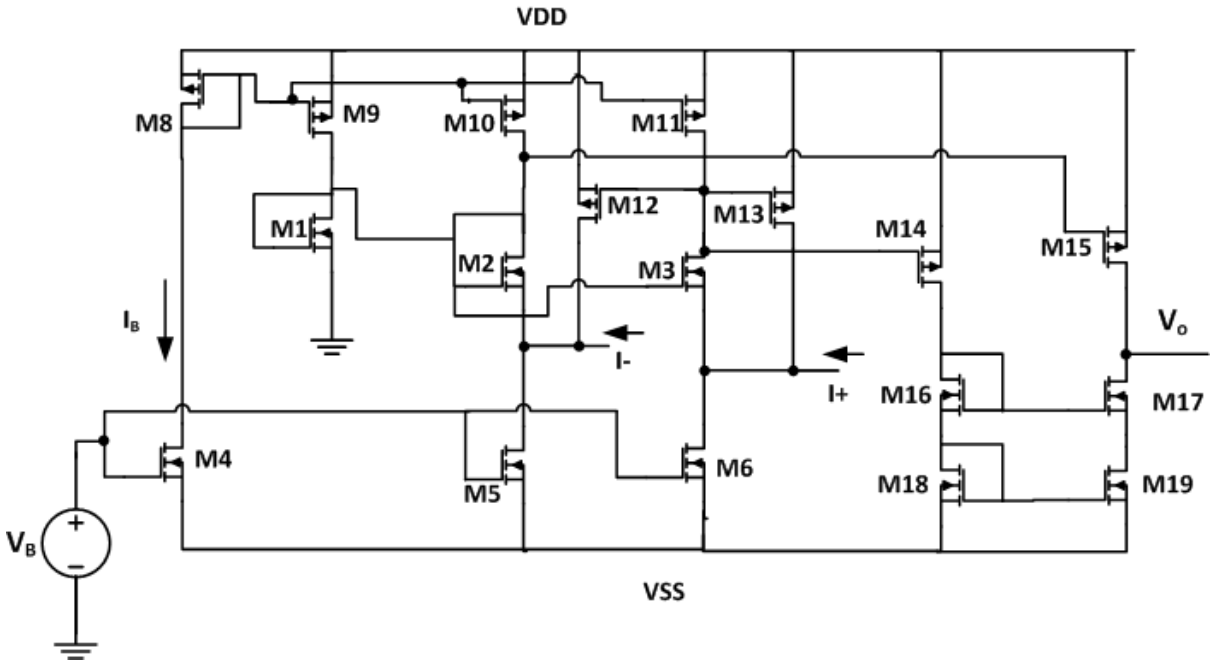

Figure 3.1 Circuit diagram of proposed OTRA.

The transistor pairs (M10 & M11) and (M13 & M14) form current mirrors and provide current differencing operation thus providing gate voltages at input terminals of amplifier which is proportional to the difference in current at input terminals. M12 and M13 perform negative feedback operation and biasing current through M5 and M6 ensures that voltage of input terminals is independent of current drawn from the.

The transresistance gain of proposed OTRA is calculated using gain stage shown in Figure 3.2.

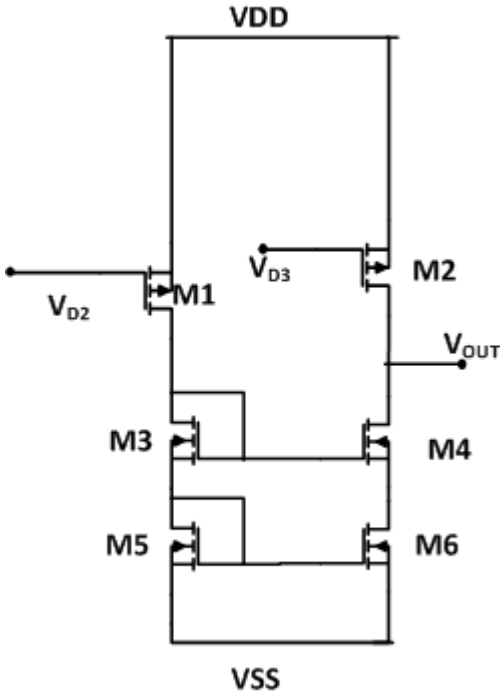

Figure 3.2 Gain stage of proposed OTRA

The gain stage uses cascode configuration to increase the gain. Cascode current mirror increases output impedance and hence, increases the gain.

The gain (Av) of differential gain stage is given as.

$$A_v = g_{m1}\left(r_{o1} \parallel g_{m3} r_{o4} r_{o6}\right) \tag{3.1}$$

From Figure 3.2 the output voltage is given as:

$$V_o = A_v\left(v_{D2} - v_{D3}\right) \tag{3.2}$$

And

$$v_{D2} - v_{D3} = \frac{1}{\frac{\lambda k}{2}\left(v_{GS} - v_t\right)^2}\left(I_+ - I_-\right) \tag{3.3}$$

Where λ is the channel length modulation parameter of transistors and $K = \mu_n c_{ox}\left(\frac{W}{L}\right)$

Using (3.2) and (3.3) the output voltage (V_0) can be written as

$$V_o = g_{m1}\left(r_{o1} \parallel g_{m3} r_{o4} r_{o6}\right)\left(v_{D2} - v_{D3}\right) \tag{3.4}$$

From (3.4) the Transresistance gain of OTRA is given as

$$R_m = \frac{g_m\left(r_{o1} \parallel g_{m3} r_{o4} r_{o6}\right)}{\frac{\lambda k_n}{2}\left(V_{GS} - V_t\right)^2} \tag{3.5}$$

3.2 PROPOSED COMPENSATED OTRA CIRCUIT

3.2.1 Circuit Description

Figure 3.3 shows the proposed OTRA along with compensation circuit proposed in [21]. The compensation circuit does not interfere the gain stage and it can work independently on any fixed current but the compensation circuit compensates for difference in drain voltages of transistors M2 and M3.

The compensation circuit is developed using proposed OTRA and compensation circuit proposed in [21].

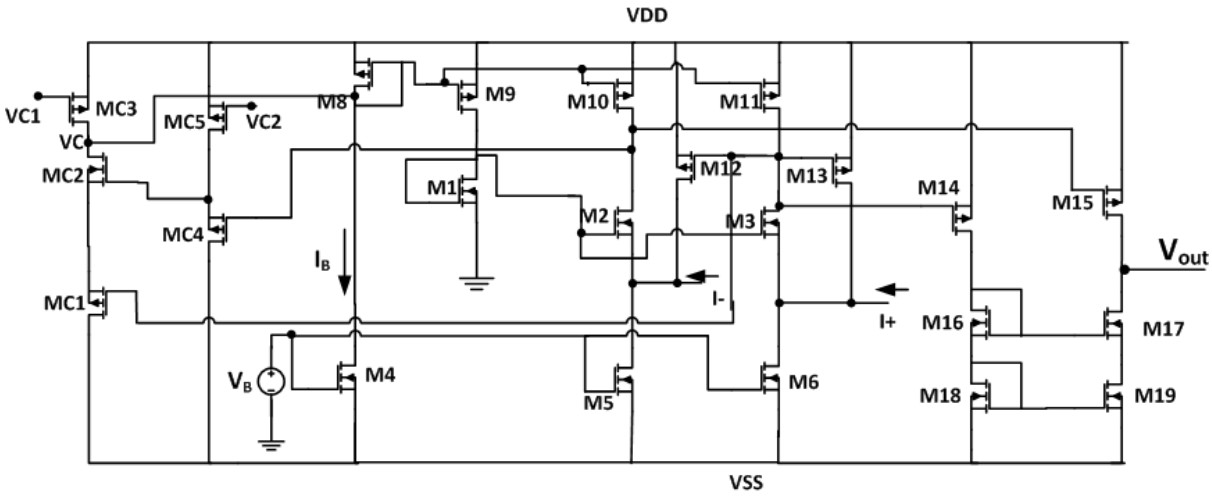

Figure 3.3 Circuit diagram of compensated circuit

The voltage at drain Terminal of the Mc3 is the difference between voltages at drain terminals of transistors M2 and M3, multiplied by gain of OTRA. The values of VC1 and VC2 must be chosen so that V_{D2}-V_{D3} becomes almost zero.

CHAPTER 4

SIMULATION RESULTS

The proposed circuit is designed and simulated in Cadence Virtuoso Analog Design Environment using BSIM3V3 180 nm CMOS technology.

The DC transfer characteristics of proposed OTRA in inverting and non-inverting configurations are shown in Figures 4.1 and 4.2 respectively. The Biasing voltage ($V_{b=}$-200 mV) equal to -200 mV is applied at gate terminal of transistor M1.

The plots in Figure show the variation in output voltage (V_o) with respect to increase in input current (I_+) for the different values of current (I-) both in the range of -50 µ*A* to 50 µA.

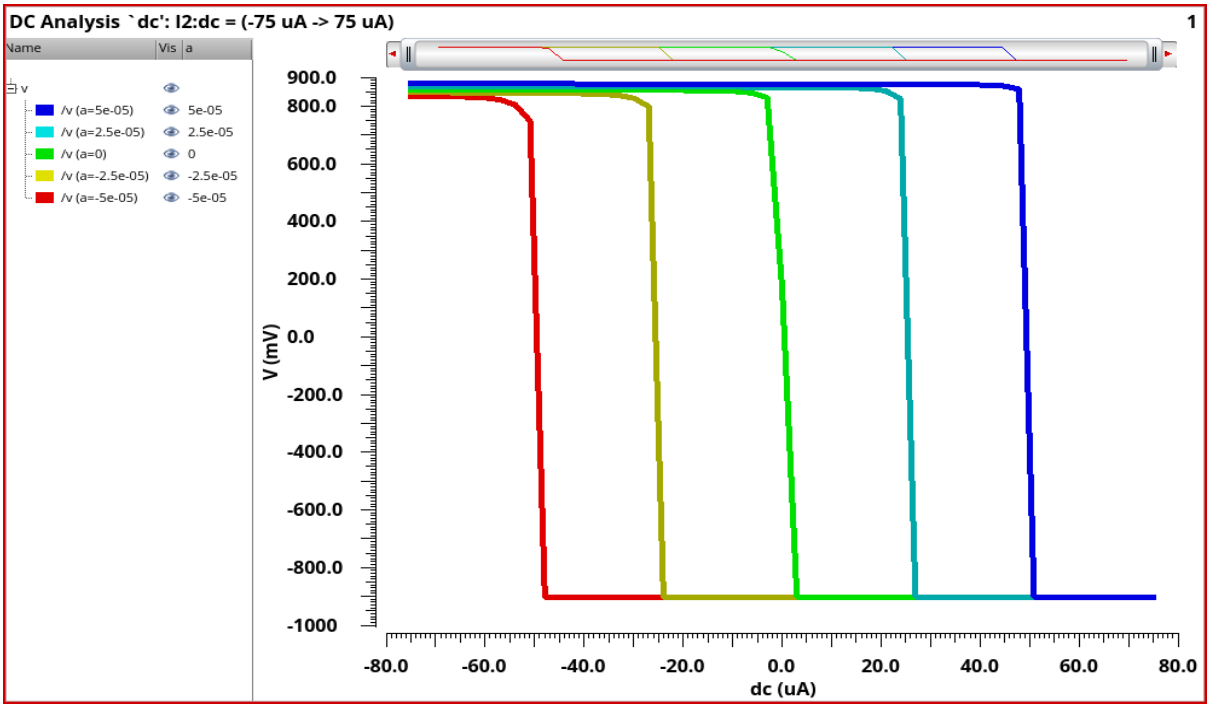

Figure 4.1 DC transfer characteristics of proposed OTRA, inverting configuration

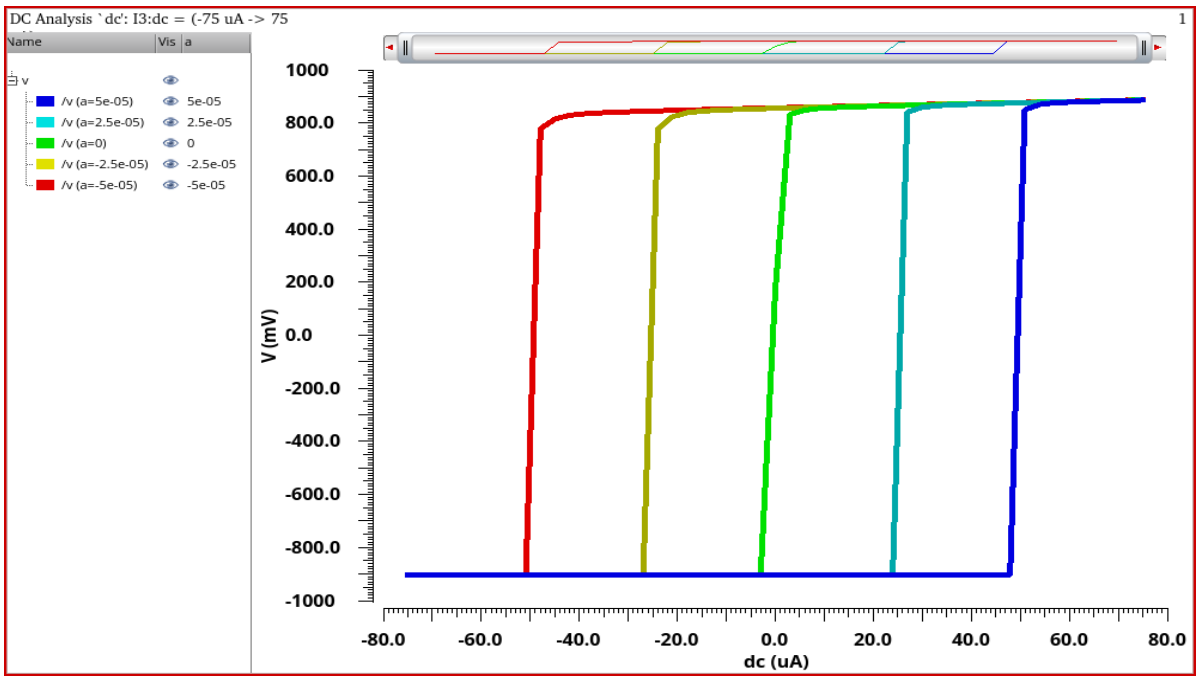

Figure 4.2 DC transfer characteristics of proposed OTRA, non-Inverting configuration

The DC transfer characteristics of compensated OTRA circuit are shown in Figures 4.3 and 4.4 the biasing voltages Vc1 and Vc2 are chosen as .54mV and 0mV such that V_{D2}-V_{D3} becomes 0.The plots show variation of output voltage (V_o) with increase in input current (I_+) for different value of (I-) for range of -50µA to 50µA.

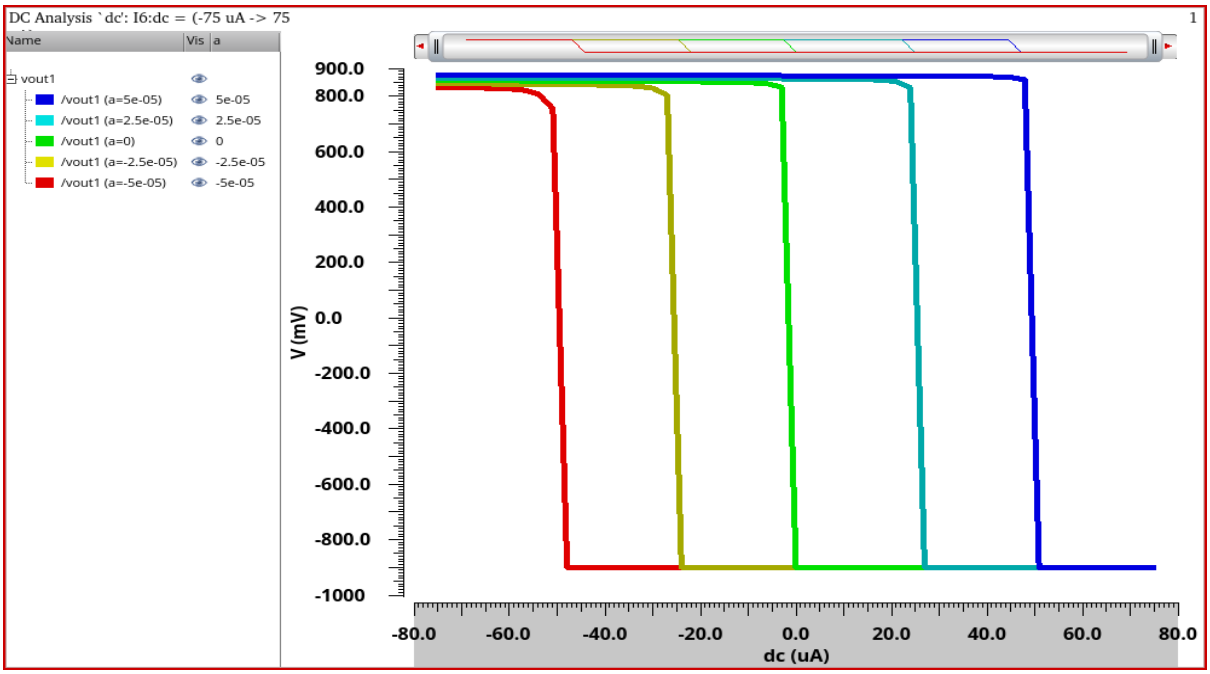

Figure 4.3 DC transfer characteristics of compensated OTRA circuit, inverting configuration

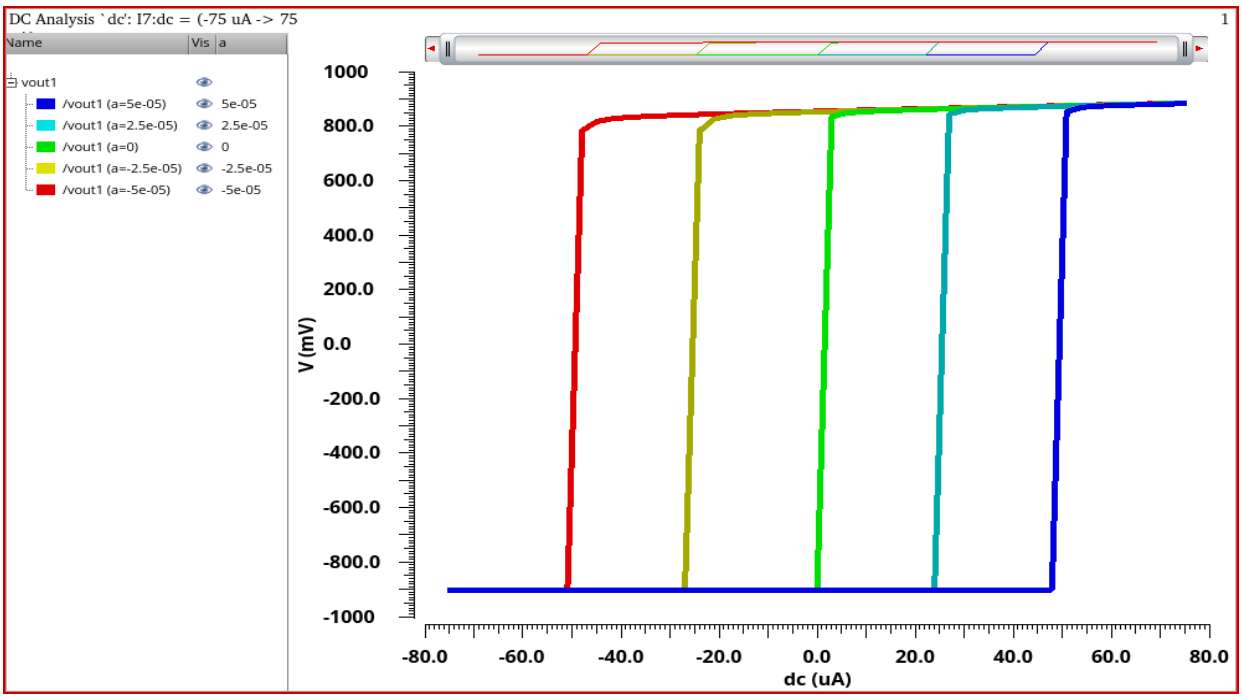

Figure 4.4 DC transfer characteristics of compensated OTRA circuit, non-inverting configuration

The AC analysis of proposed OTRA shown in Figure 4.5 has been performed with input currents (I_{+} and I_{-}) of AC magnitude 4 µA and 2 µA with DC offset current of 10 nA.

From 663.243 KHz, respectively. Figure 4.5 the gain and bandwidth of the proposed circuit are obtained as 165.76 db, and

The plot in Figure 4.6 shows the variation of differential input resistance of proposed OTRA circuit with the increase in frequency.

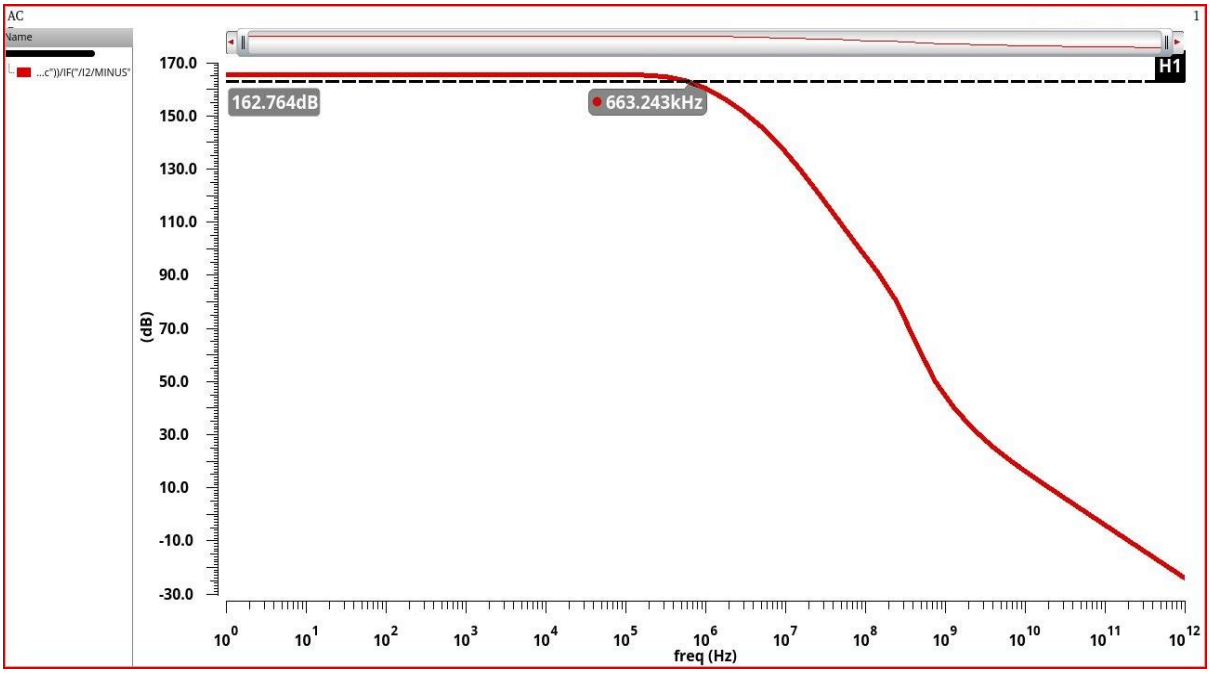

Figure 4.5 Frequency response of proposed OTRA

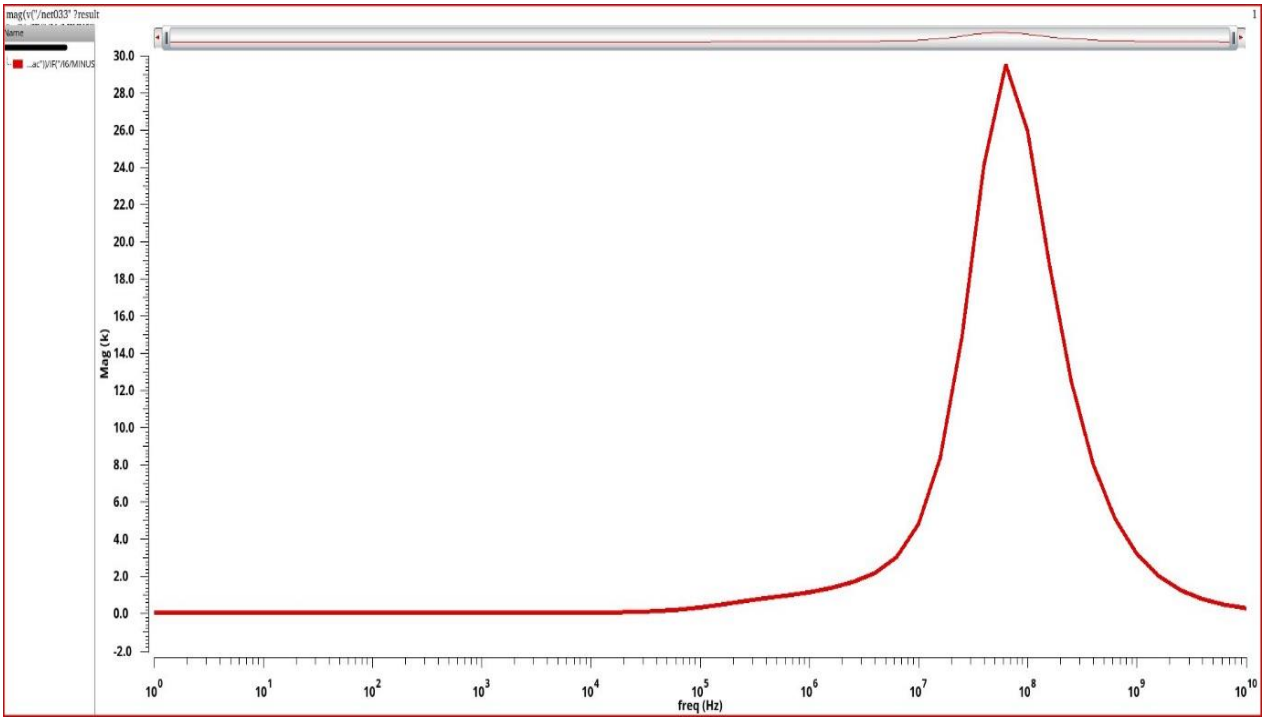

Figure 4.6 Input resistance plot of proposed OTRA

The frequency response of compensated OTRA circuit is shown in Figure 4.7 from the frequency response gain and bandwidth are observed as 179.73db and 238KHz, respectively. Input resistance plot of compensated OTRA is shown in the Figure 4.8

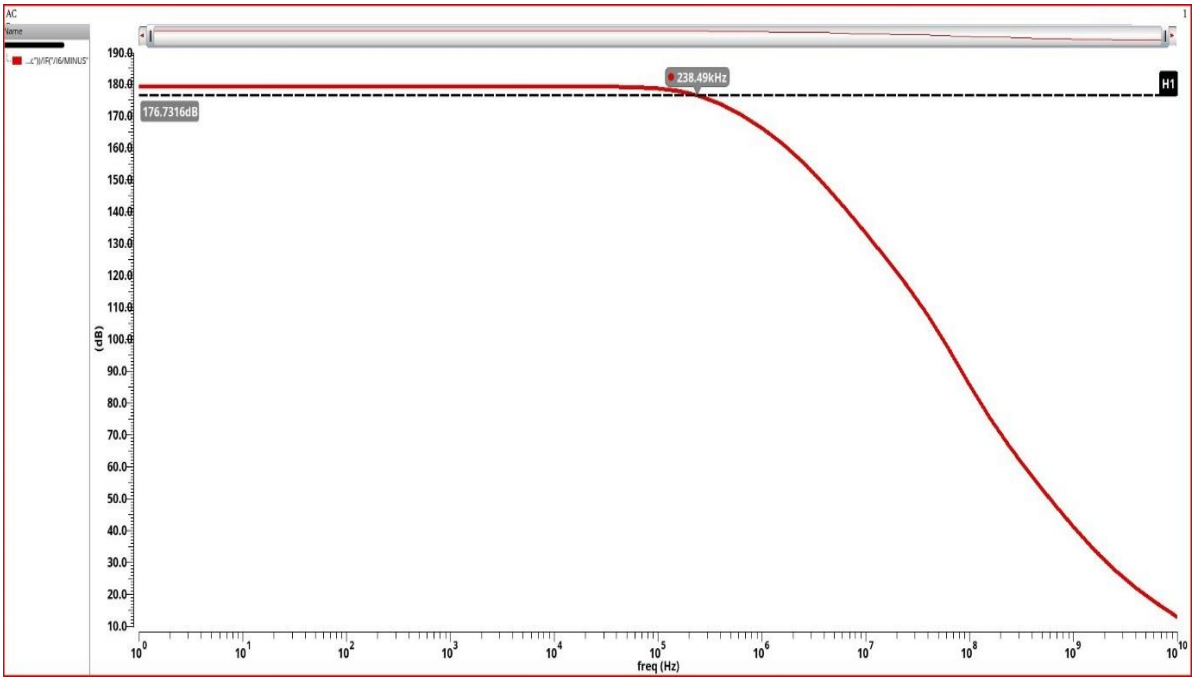

Figure 4.7 Frequency response of compensated OTRA circuit

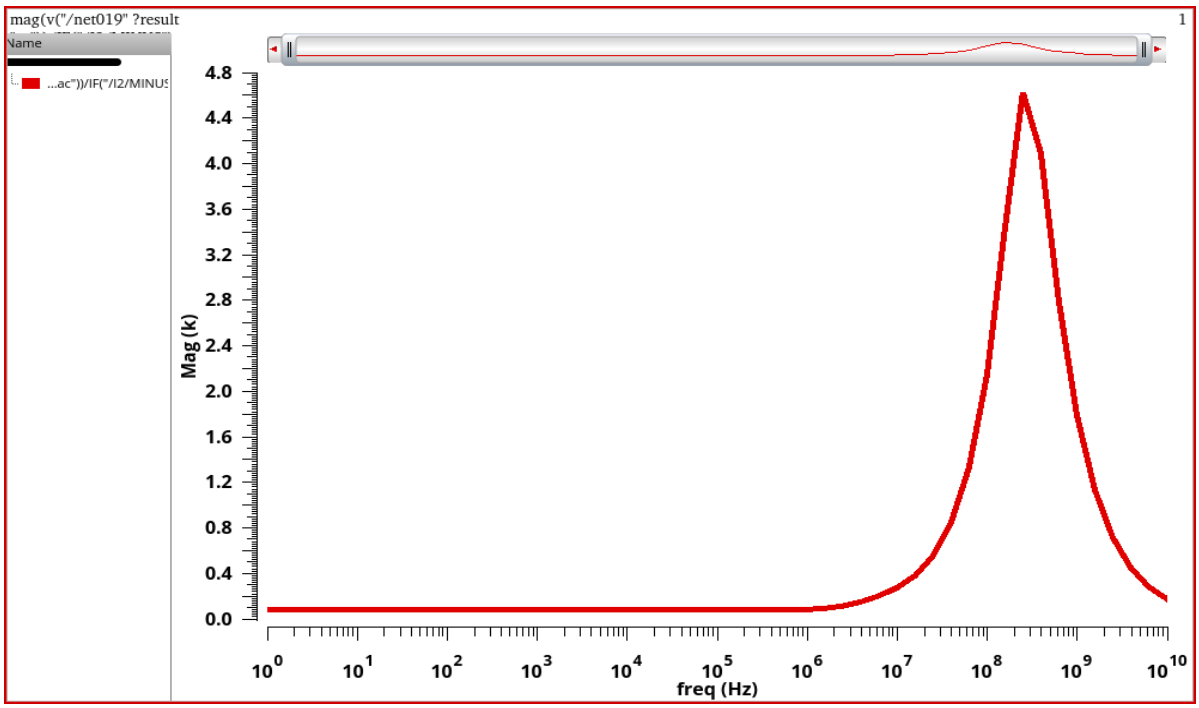

Figure 4.8 Input resistance plot of compensated OTRA

Power supply rejection ratio of proposed OTRA is calculated for both the power supplies (V_{DD} and V_{SS}). The PSRR for V_{DD} is obtained as 147.04db and for V_{SS} is obtained as 116.3 db. The PSRR of for compensated circuit are obtained as 153.4db and 131.9db for V_{DD} and V_{SS}, respectively.

Table 4.1 shows the comparison of proposed OTRA and compensated OTRA circuits with existing OTRA circuits reported in literature [7, 18, 21, 23].

Table 4.1 Comparison of OTRA and compensated OTRA with existing OTRAs

Parameters	OTRA proposed in [7]	OTRA proposed in [18]	OTRA proposed in [21]	OTRA proposed in [23]	Proposed OTRA	Proposed Compensated OTRA
Open Loop Transresistance Gain (db)	80	130	179.12	163.2	165.76	179.73
CMOS Technology(um)	1.2	.25	.25	.25	.18	.18
Power Supply (V)	±2.5	±1.5	±1.5	±1.5	±0.9	±0.9
Number of Transistors	17	14	21	20	18	23
PSRR+ (db)	---	---	---	186.2	147.04	153.4
PSRR- (db)	---	---	---	150.1	116.3	131.9
Input Current Dynamic Range (µA)	-200 to +200	-50 to +50	-50 to +50	-50 to +50	-50 to +50	-50 to +50
Offset Current(µA)	1.25	0.3	0.097	0.1	0.01	0.01
Bandwidth (MHz)	---	---	---	0.4	0.663	0.233
Rise Time/ Fall Time for 1 MHz (ns)	---	0.023/1.74	0.023/1.74	0.025/1.1	1.01/1.07	1.23/2.39
Power Dissipation (mW)	0.9	0.709	0.82	0.83	0.457	0.507

From Table 4.1 it is concluded that gain and bandwidth has improved and Power supply has also been reduced to ±.9V.

Corners analysis offers the performance outcomes generated from the most extreme variations expected in the manufacturing process. In a real manufacturing scenario, process variables fluctuate randomly around their ideal values. This random variation results in an uncertain yield for the designed circuit.

The corner analysis ensures the largest possible yield of the circuit, in case all parameters produce acceptable results. To ensure reliable outcomes under extreme conditions, a designer must take into account the effect of process corner variations on the performance of circuit. In order to observe circuit's performance.

Besides one TT (typical NMOS typical PMOS) corner. The circuit is observed mainly at four corners: SS (slow NMOS slow PMOS), FF (fast NMOS fast PMOS), SF (slow NMOS fast PMOS) and FS (fast NMOS slow PMOS).

The SS corner is applied with lowest supply voltage (-10% Vsupply) and highest temperature, thus it provides worst speed. FF corner is applied with highest supply voltage (+10% Vsupply) and lowest temperature, thus it provides worst power. Table 4.2 and 4.3 shows the table of corners to obtain simulation results for the proposed OTRA.

Table 4.2 Corners Simulation Table

Corner	Supply voltage (V)	Temperature $\left(^{\circ}C\right)$
TT	±.9	27
SS	±.81	125
FF	±.98	-55
SF	±.9	27
FS	±.9	27

The DC transfer characteristics and frequency response of proposed OTRA for the different process corners are shown in Figure 4.9 and 4.10 respectively.

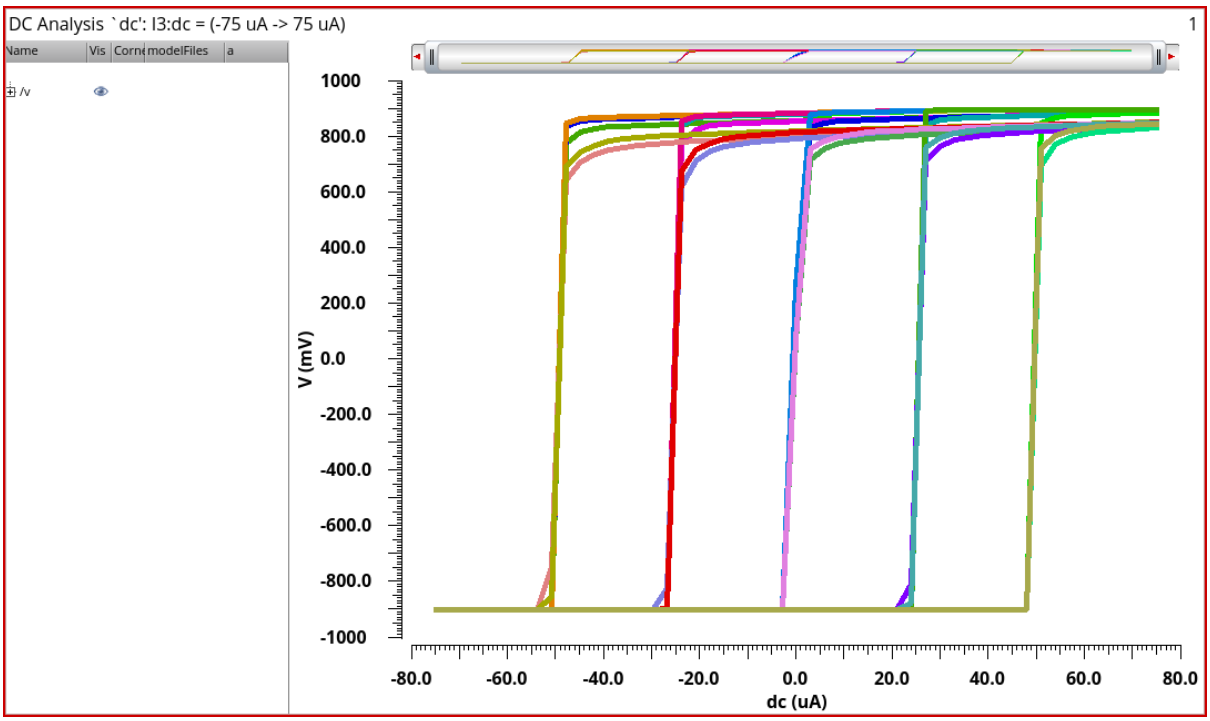

Figure 4.9 DC transfer characteristics for various process corners

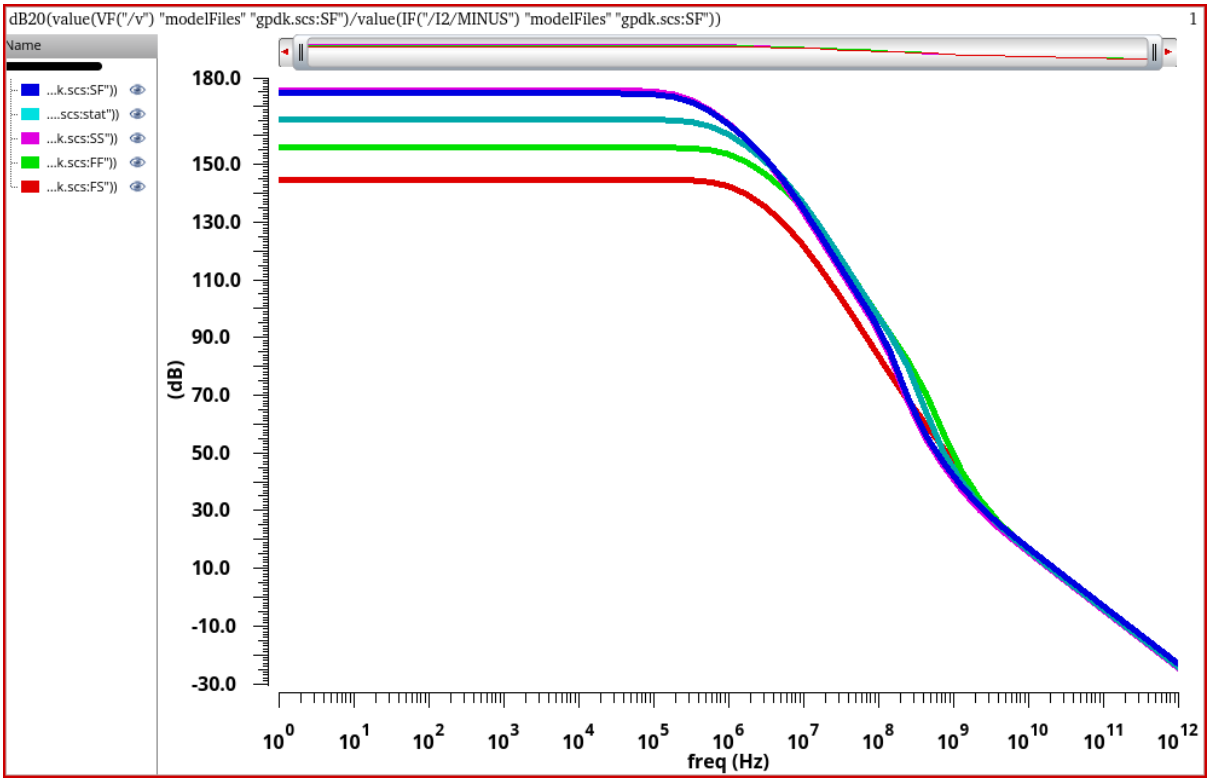

Figure 4.10 Frequency response of proposed OTRA for various process corners

Table 4.3 presents the values of open loop gain and bandwidth of the proposed circuit for the different process corners.

Table 4.3 Gain and bandwidth of OTRA at various process corners

Parameters	TT	**SS**	FF	SF	FS
Open loop DC gain (dbΩ)	165.75	175.3	156	173.72	144.93
Bandwidth (Kh_z)	663.24	418	1200	431	1150

From the table it is concluded that variations of gain and bandwidths for extreme parameters are within the acceptable range.

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

Circuits which operate on lower supply voltages and have larger bandwidth have become essential requirement for electronics market. OTRA is low impedance, constant bandwidth active analog building block because of use of current feedback technique. This thesis presents a novel OTRA circuit in which cascode current mirror is used at the gain stage which improves gain of the OTRA. The proposed circuit is simulated in Cadence Virtuoso Analog Design Environment BSIM3V3 180 nm CMOS technology. Comparison with OTRAs available in literature has been done and it is concluded that the proposed OTRA has high gain, high bandwidth and reduced power supply requirement. To test the reliability of proposed circuit for extreme parameters process corner analysis has also been performed and presented.

5.2 Future Scope

In the thesis OTRA, a most suitable analog building block has been presented. The proposed work is most suitable for transresistance mode applications and can be used to implement oscillators, filters, interface circuits, triangular and square wave generators etc.

REFERENCES

[1] A. S. Sedra, G. W. Roberts and F. Gohh, "The current conveyor: history, progress and new results," in *IEE Proceedings G - Circuits, Devices and Systems*, vol. 137, no. 2, 1990, pp. 78-87.

[2] I. A. Awad and A. M. Soliman, "New CMOS realization of the CCII-," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 46, no. 4, pp. 460-463 ,Apr 1999.

[3] C. Sanchez-Lopez *et al*. "Pathological Element-Based Active Device Models and Their Application to Symbolic Analysis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 6, pp. 1382-1395, June 2011.

[4] J.J. Chen, H.W. Tsao and C.C. Chen. "Operational transresistance amplifier using CMOS technology," *Electronics Letters*, vol. 28, no.22, 1992.

[5] J.J. Chen, H.W. Tsao, S.I. Liu and W. Chiu, "Parasitic-capacitance-insensitive current-mode filters using operational transresistance amplifiers," *IEE Proceedings - Circuits, Devices and Systems,* vol. 142, no. 3, 1995.

[6] Chiu, Wenwei *et al.,* "Single-capacitor MOSFET-C integrator using OTRA," *Electronics Letters,* vol. 31, no. 21, 1995.

[7] K. N. Salama and A. M. Soliman, "CMOS operational transresistance amplifier for analog signal processing applications," *Microelectronics Journal*, vol. 30, pp. 235–245, 1999.

[8] Riewruja, J. Parnklang and A. Julprapa, "Current tunable CMOS operational transresistance amplifier," *IEEE International Symposium on Industrial Electronics Proceedings ISIE*, vol.2, Pusan, 2001, pp. 1328-1338.

[9] Chen, J.J., H.W. Tsao and S.I. Liu., "Voltage-mode MOSFET-C filters using operational transresistance amplifiers (OTRAs) with reduced parasitic capacitance effect," *IEE Proceedings - Circuits, Devices and Systems,* vol. 148, no. 5, 2001.

[10] H. Barthelemy, I. Koudobine and D. Van Landeghem, "Bipolar low-power operational transresistance amplifier based on first generation current conveyor," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 6, pp. 620-625, Jun 2001.

[11] S. Kilinc and U. Cam, "Operational transresistance amplifier based first-order all pass filter with an application example," *The 2004 47th Midwest Symposium on Circuits and Systems, MWSCAS '04*, vol.1, 2004, pp. I-65-8.

[12] Seoung-Jae Yoo, A. Ravindran and M. Ismail, "A low voltage CMOS transresistance-based variable gain amplifier," *IEEE International Symposium on Circuits and Systems*, vol.1, 2004, pp. I-809-12.

[13] A. U. Keskin, "Design of minimum component oscillators using negative impedance approach based on different single active elements," *Proceedings of the 12th IEEE Mediterranean Electrotechnical Conference*, vol.1, 2004, pp. 83-86.

[14] C. Cakir, U. Cam and O. Cicekoglu, "*IEEE Transactions on Circuits and Systems II: Express Briefs IEEE Trans. Circuits Syst. II",* 2005.

[15] Yuh-Shyan Hwang, Jiann-Jong Chen and Wen-Ta Lee, "High-order linear transformation MOSFET-C filters using operational transresistance amplifiers," *IEEE International Symposium on Circuits and Systems*, 2005, pp. 3275-3278, vol. 4.

[16] C. L. Hou, H. C. Chien and Y. K. Lo, "Squarewave generators employing OTRAs," in *IEE Proceedings - Circuits, Devices and Systems*, vol. 152, no. 6, pp. 718-722, 9 Dec. 2005.

[17] M. Massarotto, A. C. Garcia and A. J. Lopez-Martin, "Two-Stage Differential Charge and Transresistance Amplifiers," *2006 IEEE Instrumentation and Measurement Technology Conference Proceedings*, Sorrento, pp. 1920-1925.

[18] Mostafa, Hassan, and Ahmed M. Soliman. "A Modified CMOS Realization of the Operational Transresistance Amplifier (OTRA)." Frequenz60.3-4 (2006).

[19] Y. K. Lo and H. C. Chien, "Single OTRA-based current-mode monostable multivibrator with two triggering modes and a reduced recovery time," in *IET Circuits, Devices & Systems*, vol. 1, no. 3, pp. 257-261, June 2007.

[20] Lo, Yu-Kang, and Hung-Chun Chien. "*Switch-Controllable OTRA-Based Square/Triangular Waveform Generator." IEEE Transactions on Circuits and Systems* II: Express Briefs54.12 (2007).

[21] Kafrawy, Abdelrahman K., and Ahmed M. Soliman. "New CMOS operational transresistance amplifier." 2008 International Conference on Microelectronics.

[22] Lo et al. "Switch-controllable OTRA-based bistable multivibrators." IET Circuits, Devices & Systems2.4 (2008)

[23] Kafrawy, Abdelrahman K., and Ahmed M. Soliman. "A modified CMOS differential operational transresistance amplifier (OTRA)." AEU - *International Journal of Electronics and Communications*63.12 (2009).

[24] R. Pandey and M. Bothra, "Multiphase sinusoidal oscillators using Operational Trans-Resistance Amplifier,"*2009 IEEE Symposium on Industrial Electronics & Applications*, Kuala Lumpur, 2009, pp. 371-376.

[25] F. Kacar, "Operational transresistance amplifier based current-mode all-pass filter topologies," *2009 Applied Electronics*, Pilsen, 2009, pp. 149-152.

[26] R. Pandey *et al. "*A novel OTRA based oscillator with non-interactive control," *International Conference on Computer and Communication Technology* (ICCCT), 2010.

[27] Mayank "Versatile voltage controlled relaxation oscillators using OTRA." 2011 *3rd International Conference on Electronics Computer Technology*.

[28] K. Banerjee, A. Ranjan and S. K. Paul, "New first order multifunction filter employing operational transresistance amplifier,"*2012 5th International Conference on Computers and Devices for Communication (CODEC)*, Kolkata, 2012, pp. 1-3

[29] A. Singh, K. Trivedi, M. Agrawal and V. Srivastava, "Improved OTRA based receiver section in Wireless Laser Communication link," *2012 18th Asia-Pacific Conference on Communications (APCC)*, Jeju Island, 2012, pp. 713-715.

[30] R. Pandey *et al*. "Single OTRA Based Analog Multiplier and Its Applications." ISRN Electronics2012

[31] A. Ranjan, M. Ghosh and S. K. Paul, "Voltage-mode third order band pass filter employing operational transresistance amplifier," *2012 5th International Conference on Computers and Devices for Communication (CODEC)*, Kolkata, 2012, pp. 1-3

[32] M. Kumngern, S. Junnapiya and J. Chanwutitum, "Voltage-mode lowpass, highpass, bandpass biquadratic filter using OTRAs," *2013 IEEE International Conference on Control System, Computing and Engineering*, Mindeb, 2013, pp. 230-233.

[33] S. Mittal *et al."*Analog field programmable CMOS operational transresistance amplifier (OTRA)," *2013 Students Conference on Engineering and Systems (SCES)*, Allahabad, 2013, pp. 1-6.

[34] M. Kumngern and I. Kansiri, "Single-element control third-order quadrature oscillator using OTRAs," *2014 Twelfth International Conference on ICT and Knowledge Engineering*, Bangkok, 2014, pp. 24-27

[35] C. S. Pittala and A. Srinivasulu,"Quadrature oscillator using operational transresistance amplifier," *2014 International Conference on Applied Electronics*, Pilsen, 2014, pp. 117-120.

[36] D. S. Rajput and R. Singh, "Timer circuit using OTRA and its application as astable and Monostable multivibrator," *2015 2nd International Conference on Electronics and Communication Systems (ICECS)*, Coimbatore, 2015, pp. 1047-1050.

[37] A. Pramanik, "Design of operational transresistance amplifier based grounded active inductor and implementation of bandpass filter," *2015 2nd International Conference on Electronics and Communication Systems (ICECS)*, Coimbatore, 2015, pp. 842-844

[38] A. Goel, R. Pandey, N. Pandey and S. Yadav, "Operational transresistance amplifier based low-voltage reference," *2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES)*, Delhi, 2016, pp. 1-5.

[39] U. Torteanchai, P. Phatsornsiri and M. Kumngern, "Quadrature Oscillator Using Operational Transresistance Amplifiers," 2016 *7th International Conference on Intelligent Systems, Modelling and Simulation (ISMS)*, Bangkok, 2016, pp. 403-406.

APPENDIX A

Model file of NMOS

Generic PDK BSIM3V3 Spectre nmos1.scs

model nmos1_int bsim3v3

type=n lmin=0.18e-6 lmax=0.501e-6 wmin=0.4e-6 wmax=10.001e-6 minr=1e-60 tnom=25
+version=3.1 tox=toxn xj=1.6e-7 nch=3.9e+17 lln=1 lwn=1 wln=1 wwn=1 lint=1e-8 ll=0
+lw=0 lwl=0 wint=1e-8 wl=0 ww=0 wwl=0 mobmod=1 binunit=2 xl=-2e-8 dlxn xw=0
+dxwn dwg=0 dwb=0 ldif=9e-8 hdif=hdifn rsh=6.8rd=0 rs=0 vth0=0.48 dvthn lvth0=1.18e-8
+wvth0=-7.08e-9 pvth0=-3.07e-15 k1=0.49 lk1=4.82e-8 wk1=-1.67e-8 pk1=-4.58e-15
+k2=0.03 lk2=-2.01e-8 wk2=6.03e-10 pk2=5.87e-16 k3=0 dvt0=0 dvt1=0 dvt2=0 dvt0w=0
+dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=84638 lvsat=-0.0002 wvsat=0.001 ua=-5.07e-10
+lua=-5.58e-17 wua=-4.34e-17 pua=2.42e-23 ub=1.98e-18 lub=4.99e-26 wub=-2.70e-26
+pub=-5.53e-32 uc=7.19e-11 luc=1.46e-17 wuc=-3.71e-19 puc=-1.43e-23 rdsw=170
+prwb=0 prwg=0 wr=1 u0=0.04 lu0=5.93e-10 wu0=-5.39e-10 pu0=5.68e-16 a0=0.54
+la0=7.71e-8 wa0=1.31e-7 pa0=-6.57e-14 keta=-0.027 lketa=1.75e-9 wketa=2.62e-9 a1=0
+pketa=-9.24e-16 a2=0.99 ags=0.039 lags=-8.58e-9 wags=-1.49e-9 pags=6.84e-16 b0=0
+b1=0 voff=-0.13 lvoff=1.25e-10 wvoff=5.07e-9 pvoff=-2.82e-15 nfactor=1 cit=0.0002
+lcit=1.32e-10 wcit=4.29e-11 pcit=-1.97e-17 cdsc=0 cdscb=0 cdscd=0 eta0=-0.0003
+leta0=1.93e-10 weta0=3.35e-11 peta0=-1.54e-17 etab=0.0014 letab=-6.99e-10
+wetab=4.11e-11 petab=1.89e-17 dsub=0 pclm=0.97 lpclm=7.37e-8 wpclm=2.16e-7
+ppclm=-1.59e-15 pdiblc1=1e-6 pdiblc2=-0.0035 lpdiblc2=4.38e-9 wpdiblc2=-1.24e-9
+ppdiblc2=5.71e-16 pdiblcb=0.01 drout=0 pscbe1=4e+08 pscbe2=1e-6 pvag=0 delta=0.01
+alpha0=6.27e-8 beta0=11.60 kt1=-0.23 lkt1=1.96e-9 wkt1=1.35e-9 pkt1=1.97e-15 kt2=-
+0.027 lkt2=-3.83e-10 wkt2=-5.19e-9 pkt2=1.23e-15 at=20000 ute=-1.09 lute=-6.90e-8
+wute=-4.80e-7 pute=6.18e-14 ua1=1.22e-9 ub1=-5.72e-20 lub1=-1.26e-25 wub1=-1.61e-24
+pub1=2.31e-31 uc1=1.07e-10 luc1=-1.73e-17 wuc1=-1.51e-16 puc1=3.17e-23 kt1l=0 prt=0

+cj=cjn pb=0.69 mj=0.36 cjsw=cjswn pbsw=0.69 mjsw=0.20 cjswg=cjswgn pbswg=0.69
+mjswg=0.44 cgdo=cgon cgso=cgon cta=0.001 ctp=0.0006 pta=0.0016 ptp=0.0016 js=8.38e-
+6 jsw=1.6e-11 n=1 xti=3 capmod=2 nqsmod=0 xpart=1 cf=0 tlev=1 tlevc=1 dlc=3e-9
+noimod=2 noia=5.0e+19 noib=4.0e3 noic=-4.0e-13 em=3.0e+07 ef=0.883

Model file of PMOS

Generic PDK BSIM3V3 Spectre pmos1.scs

model pmos1_int bsim3v3

type = p lmin=0.17e-6 lmax=0.501e-6 wmin=0.4e-6 wmax=10.001e-6 minr=1e-60 +tnom=25 version=3.1 tox=toxp xj=1.7e-7 nch=3.9e+17 lln=1 lwn=1 wln=1 wwn=1 +lint=1.5e-8 ll=0 lw=0 lwl=0 wint=1.5e-8 wl=0 ww=0 wwl=0 mobmod=1 binunit=2 dxlp +xw=0 dxwp dwg=0 dwb=0 ldif=9e-8 hdif=hdifp rsh=7.2 rd=0 rs=0 vth0=-0.43 dvthp +lvth0=-1.37e-8 wvth0=-8.48e-9 pvth0=5.43e-15 k1=0.75 lk1=-1.21e-8 wk1=-1.56e-7 +pk1=1.88e-14 k2=-0.04 lk2=6.06e-9 wk2=5.28e-8 pk2=-7.49e-15 k3=0 dvt0=0 dvt1=0 +dvt2=0 dvt0w=0 dvt1w=0 dvt2w=0 nlx=0 w0=0 k3b=0 vsat=130812 lvsat=-0.00036 +lua=6.66e-17 wua=9.31e-16 pua=-1.27e-22 ub=1.71e-18 lub=-7.86e-26 wub=-+1.10e-24 +pub=1.21e-31 uc=-2.69e-11 luc=5.12e-18 wuc=-1.38e-16 puc=7.55e-24 rdsw=530 prwb=0 +prwg=0 wr=1 u0=0.0063 lu0=2.97e-10 wu0=1.59e-9 pu0=-2.39e-16 a0=0.38 la0=1.91e-7 +wa0=6.28e-7 pa0=-1.11e-13 keta=0.016 lketa=-1.31e-9 wketa=7.53e-9 pketa=-1.55e-15 +a1=0 a2=0.4 ags=0.0068 lags=5.95e-9 wags=1.68e-8 pags=-7.56e-15 b0=0 b1=0 voff=-0.13 +lvoff=5.74e-10 wvoff=2.75e-9 pvoff=-2.44e-15 nfactor=1 cit=0.00013 lcit=4.80e-11 +pcit=3.58e-18 cdsc=0 cdscb=0 cdscd=0 eta0=-0.00047 leta0=2.56e-10 etab=0.00067 +letab=-3.47e-10 dsub=0 pclm=0.84 lpclm=7.067e-8 wpclm=7.40e-8 ppclm=-3.33e-14 +pdiblc1=1e-6 pdiblc2=0.0096 lpdiblc2=1.70e-10 wpdiblc2=-2.10e-9 ppdiblc2=9.45e-16 +pdiblcb=0.01 drout=0 pscbe1=3.5e+08 pscbe2=5e-7 pvag=0 delta=0.01 alpha0=8.93e-7 +beta0=22.68 kt1=-0.22 lkt1=-4.41e-9 wkt1=1.69e-9 pkt1=4.61e-16 lkt2=-3.22e-9 at=10000 +wkt2=-9.67e-9 kt2=-0.017 pkt2=2.43e-15 ute=-0.58 lute=9.19e-9 wute=-5.58e-8 +prt=0pute=-3.93e-16 ua1=1.22e-9 ub1=-1.64e-18 lub1=7.95e-26 wub1=1.12e-25 ef=1.064

+pub1=-3.52e-32 uc1=-5.64e-11 luc1=1.18e-17 wuc1=1.13e-16 puc1=-1.48e-23 kt1l=0 prt=0 +cj=cjp pb=0.89 mj=0.4476 cjsw=cjswp pbsw=0.89 mjsw=0.37 cjswg=cjswgp pbswg=0.89

+mjswg=0.37 cgdo=cgop cgso=cgop cta=0.001 ctp=0.0004 pta=0.0016 ptp=0.0016 js=4.92 +jsw=9e-10 n=1 xti=3 capmod=2 nqsmod=0 xpart=1 cf=0 tlev=1 tlevc=1 dlc=2e-9 +noimod=2 noia=7.0e+19 noib=8.0e3 noic=5.4e-12 em=3.0e+07

601562010_gitesh_mehta

by Gitesh Mehta

FILE	601562010_GITESH_MEHTA.PDF (1.04M)		
TIME SUBMITTED	17-JUL-2017 01:10PM	WORD COUNT	6991
SUBMISSION ID	831331253	CHARACTER COUNT	39177

601562010_gitesh_mehta

ORIGINALITY REPORT

%16	%10	%10	%0
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	dspace.thapar.edu:8080 Internet Source	%3
2	Pandey, Rajeshwari, Neeta Pandey, Gurumurthy Komanapalli, Alok Kumar Singh, and Rashika Anurag. "New realizations of OTRA based sinusoidal oscillator", 2015 2nd International Conference on Signal Processing and Integrated Networks (SPIN), 2015. Publication	%1
3	www.scilit.net Internet Source	%1
4	M. Siripruchyanun. "High-performance BiCMOS current Controlled CDBA and application", 2007 International Symposium on Communications and Information Technologies, 10/2007 Publication	%1
5	docslide.us Internet Source	%1
6	digital-library.theiet.org Internet Source	%1

7	M.H. Hristov. "Design of CMOS OTA core for practical education", 27th International Spring Seminar on Electronics Technology Meeting the Challenges of Electronics Technology Progress 2004 ISSE-04, 2005 Publication	%1
8	Abdelrahman K. Kafrawy. "New CMOS operational transresistance amplifier", 2008 International Conference on Microelectronics, 12/2008 Publication	<%1
9	www.hindawi.com Internet Source	<%1
10	Ashwani Goel, Rajeshwari Pandey, Neeta Pandey, Sapna Yadav. "Operational transresistance amplifier based low-voltage reference", 2016 IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), 2016 Publication	<%1
11	Kumngern, Montree, and Ittipol Kansiri. "Single-element control third-order quadrature oscillator using OTRAs", 2014 Twelfth International Conference on ICT and Knowledge Engineering, 2014. Publication	<%1

12	Lo, Y.-K., and H.-C. Chien. "Single OTRA-based current-mode monostable multivibrator with two triggering modes and a reduced recovery time", IET Circuits Devices & Systems, 2007. Publication	<%1
13	Pittala, Chandra Shaker, and Avireni Srinivasulu. "Quadrature oscillator using operational transresistance amplifier", 2014 International Conference on Applied Electronics, 2014. Publication	<%1
14	A. Ravindran, A. Savla, I. Younus, M. Ismail. "A 0.8V CMOS filter based on a novel low voltage operational transresistance amplifier", The 2002 45th Midwest Symposium on Circuits and Systems, 2002. MWSCAS-2002., 2002 Publication	<%1
15	dspace.cusat.ac.in Internet Source	<%1
16	cora.ucc.ie Internet Source	<%1
17	Salama, K.N.. "CMOS operational transresistance amplifier for analog signal processing", Microelectronics Journal, 199903 Publication	<%1
18	radioelektronika.org	

Internet Source

<%1

19	article.sapub.org Internet Source	<%1
20	Massarotto, Marco, Alfonso Carlosena, and Antonio J. Lopez-Martin. "Two-Stage Differential Charge and Transresistance Amplifiers", IEEE Transactions on Instrumentation and Measurement, 2008. Publication	<%1
21	Pandey, R., N. Pandey, Mandeep Singh, Manish Jain, and Sajal K. Paul. "Voltage mode biquadratic filter using single OTRA", 2012 IEEE 5th India International Conference on Power Electronics (IICPE), 2012. Publication	<%1
22	Rajeshwari Pandey. "Multiphase sinusoidal oscillators using Operational Trans-Resistance Amplifier", 2009 IEEE Symposium on Industrial Electronics & Applications, 10/2009 Publication	<%1
23	Wen-Ta Lee. "High-Order Linear Transformation MOSFET-C Filters Using Operational Transresistance Amplifiers", 2005 IEEE International Symposium on Circuits and Systems, 2005 Publication	<%1

24	Yu-Kang Lo. "Switch-Controllable OTRA-Based Square/Triangular Waveform Generator", IEEE Transactions on Circuits and Systems II Express Briefs, 12/2007 Publication	<%1
25	www.iirs.gov.in Internet Source	<%1
26	Mittal, S., G. Kapur, C. M. Markan, and V. P. Pyara. "Analog field programmable CMOS operational transresistance amplifier (OTRA)", 2013 Students Conference on Engineering and Systems (SCES), 2013. Publication	<%1
27	advances.utc.sk Internet Source	<%1
28	gnu.inflibnet.ac.in Internet Source	<%1
29	digitalcommons.mcmaster.ca Internet Source	<%1
30	www.waset.org Internet Source	<%1
31	www.researchgate.net Internet Source	<%1
32	spectrum.library.concordia.ca Internet Source	<%1

EXCLUDE QUOTES	ON	EXCLUDE MATCHES	< 10 WORDS
EXCLUDE BIBLIOGRAPHY	ON		