Design of Rail-to-Rail Operational Amplifier

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VLSI Design & CAD

Submitted by

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CERTIFICATE

I hereby certify that the work which is being presented in the thesis entitled **"DESIGN OF RAIL TO RAIL OPERATION AMPLIFIER"** in partial fulfillment of requirement for award of degree of **Master of Technology** in **VLSI Design & CAD** from **Thapar University**, is an authentic record of my own work carried under the supervision and guidance of **Mr. Mohd. Iliyas**, Project Faculty, Electronics & Communication Engineering department, Thapar University, Patiala.

The matter presented in this thesis has not been submitted in any other university or institute for the award of any other degree.

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ABSTRACT

In the thesis a compact two stage rail to rail OP-Amp with rail to rail common mode inputs and rail to rail output swing reaching nearly 95% of total supply voltage. The design is implemented using 0.35µm, 3.3V TSMC CMOS n-well process. The OP-Amp contains a constant g_m rail to rail input stage and class AB output stage. This compact operational amplifier provides differential voltage gain 95 dB, unity gain frequency 8.38 MHz, phase margin 55^0 while driving a 10pf load capacitor and power consumption is 512 µW.

A rail to rail input common mode range is an important requirement in operation amplifier for some application. Conventional techniques to achieve a constant g_m rail to rail complementary N-P differential input stage require complex additional circuitary. In addition, the frequency response and common mode rejection ratio (CMRR) are degraded. A power efficient technique to overcome these problems has been utilized in this work. Simulation results demonstrate very less variation in the low frequency differential voltage gain with change in input common mode level.

CHAPTER 1

INTRODUCTION

This chapter discusses the background and motivation behind the rail-to-rail operational amplifier and ideal requirement for the input stage rail-to-rail op amp. This chapter also discusses various applications of rail-to-rail op amp.

1.1 BACKGROUND

Operational amplifiers are the backbone for many analog circuit designs. It is used in numerous applications such as amplifiers, filters, control, feedback, and regulation like monitoring circuitry, cellular phones, portable devices, Medical instrumentation, and solar–powered systems. It is a fundamental building block for many circuit designs that utilize its high gain, high input impedance, and low output impedance. The operational amplifier can be used in two basic configurations: inverting and non-inverting. These configurations place different requirements on the common-mode input range. The required range varies from almost zero to a full rail to rail. An op-amp can easily be designed to achieve rail-to-rail output swing with simple class-A or class-AB designs. The key problems lie at the input stage, and the classic two stage architecture demands a rail-to-rail transconductor function with both constant *gm* and limiting current, so that unity-gain bandwidth and slew rate are maintained over the full common-mode input range. Rail-to-rail input means that input signal can be anywhere between the supply voltages with all the transistors in the saturation region (and often at 100 mV or more beyond). Rail-to-rail input is required in a Unity gain buffer configuration if wide output voltage swing is required. It may not be required in close-loop gains greater than unity. Inverting amplifiers rarely require rail-to-rail input. The differential amplifier is used as the input stage for operational amplifiers. The problem is that it behaves as a differential amplifier only over a limited range of common-mode input. Therefore, to make the operational amplifier versatile, its input stage should work for rail-to-rail common-mode input range. The most common method to achieve this range is to use a complementary differential amplifier at the input stage.

1.2 MOTIVATION

A wide input common mode voltage range may be required when the amplifier is used in the voltage follower configuration or in front end circuits, where the useful

input signal is superposed on comparatively high and variable common mode voltages, as occurs in some critical sensor applications. The need for a wide output dynamic range (the ratio of output voltage swing over the total output error contribution, i.e. offset plus noise) in most applications is reflected in the additional requirement for a rail-to-rail output voltage range.

The minimum power consumption of analog circuits at a given temperature is basically set by the required SNR and the frequency of operation (or the required bandwidth). Since this minimum power consumption is also proportional to the ratio between the supply voltage and the signal peak-to-peak amplitude, power efficient analog circuits should be designed to maximize the voltage swing.

In rail-to-rail differential input operational amplifier circuits, the common mode input voltage extends to rail-to-rail; however, the differential input voltage is very small.

1.3 RAIL TO RAIL INPUT STAGE OPERATIONAL AMPLIFIER

The ideal requirements of a rail-to-rail input stage can be summarized in three main features.

Firstly, a constant transconductance is needed to maintain the gain-bandwidth product and, hence, the small-signal behaviour constant over the entire input CM range. Ideally, this target must be achieved in a robust and universal way [3, 5, and 6] so as to avoid the fabrication process dependence as well as to ensure that the technique is valid for any gm vs. I_D characteristic of the input transistors.

Secondly, a constant SR is needed to maintain the large-signal response constant over the entire *VI, cm* range. To ensure a constant SR, the total limiting current of the input stage must be kept constant. This limiting current coincides with the sum of the biasing currents of the differential pairs in the input stage.

Finally, another important requirement is that the technique used for maintaining the small-and large-signal behaviours constant, should not substantially limit the operating frequency range of the whole circuit. This fact is of primordial importance for high-frequency applications.

Common mode rail-to-rail capability is achieved usually by using an NMOS differential pair with transconductance g_{mN} and a PMOS differential pair with transconductance g_{mP} in parallel [2, 3].

$$g_{mt} = g_{mN} + g_{mP} \qquad (1.1)$$

This circuit has three operating regions with respect to the input CM voltage range:

1) When the CM input voltage is a threshold voltage (V_T) plus a saturation voltage (a few hundreds of mill volts) above the negative power supply (V_{SS}), only the p-channel transistor pair is on.

2) When the CM input voltage is a threshold voltage and a saturation voltage below the positive voltage supply (V_{DD}), only the n-channel input pair is on.

3) For CM input voltages between these two limits, both transistor pairs are on. This circuit provides a rail -to-rail CM input range, but it also introduces a major problem. In the region where both pairs are on, the transconductance of the input stage is twice as big as in the regions where only one pair (NMOS or PMOS) is on. When the CM voltage moves from one range into another the transconductance of the input stage changes by a factor of two. This prevents frequency compensation from being optimal since the bandwidth is proportional to that transconductance. Moreover, transient distortion occurs when fast changes in the common-mode voltage abruptly saturate and restore the tail-current sources [7]. The optimization of noise performance is also avoided since the thermal noise, which is inversely proportional to g_m, increase when one of the amplifier differential pair is off.

The use of a constant gm input stage in operational amplifiers, as is well known, is necessary to obtain the following:

(i) A differential gain and bandwidth (*Ft*) which is independent of the input common mode voltage, results in stable phase margin and hence improves the settling time.

(ii) Simplified frequency compensation of the amplifier.

(iii) Increased CMRR.

(iv) Reduced voltage gain non-linear ties and harmonic distortion (THD).

The above features are particularly important in low voltage applications where common mode voltage may be comparable with useful signals.

A virtually constant transconductance (*gm*) within the input common mode voltage range, good noise and offset performances and capable of operating at very low supply voltages.

Different circuit techniques for maintaining the transconductance (*gm*) of rail-to-rail op-amps constant over the whole input CM range have been proposed [1-6]. Many of these techniques are based on dynamic feedback loops that limit the speed performance of the amplifier [1-3, 5]. One of the simplest techniques to improve the op amp performance in this respect consists in shifting the CM response of the PMOS (NMOS) input differential pair in the negative (positive) direction so as to make its

transition region (i.e., the input CM voltage range where its tail current source operates in the triode region) to overlap that of the complementary pair. Overlapping the transition regions in a rail-to-rail input stage can be achieved by adding an appropriate constant voltage *VS* to the input CM component applied to the PMOS (NMOS) differential pair, so as to obtain the constant *gm* performance. The idea of CM response overlapping has been recently introduced [1].

1.4 RAIL TO RAIL OUTPUT STAGE OPERATIONAL AMPLIFIER

It is well known that, if the supply voltage to a class-AB CMOS amplifier is reduced below the sum of two threshold voltages of NMOS and PMOS, both the transistors go to the cut off state under quiescent condition. This reduces the dynamic range and increases output distortion. In order to overcome this problem and to achieve rail-to-rail output swing, the output stage is driven by two floating biases which prevent the output transistors going to cut off state at the quiescent operating condition. The rail-to-rail output stage requires the push-and-pull output transistors connected in common-source configuration. A class-AB controlled circuit is then necessary, in order to achieve a good comprise between distortion and quiescent dissipation. The output stage requires a minimum supply voltage of only one gate-source voltage plus one saturation voltage. It is also clear that, in any low power op-amp circuit design low output impedance is desirable but classical source follower configurations are not allowed in low voltage applications as the dynamic range gets reduced considerably. Most of the class-AB output stages have high output impedance as they employ common source configuration. As a result, the output swing gets reduced. Ideally, the source follower and common source gain stages are combined to achieve low output impedance.

1.5 APPLICATIONS OF RAIL-TO-RAIL OP AMP

1. Portable communications [16]
2. Microphone amplifiers [16]
3. Portable phones [16]
4. Sensor interface [16]
5. Active filters [16]
6. PCMCIA cards [16]
7. ASIC input drivers [16]
8. Wearable computers [16]

9. Voltage reference buffers [16]
10. Battery-powered devices [16]
11. Personal digital assistants [16]

1.6 ORGANIZATION OF THESIS WORK:

An **Introduction** to the concept of designing rail-to-rail constant *gm* operational amplifiers using complementary differential pair input stages is presented in chapter 1.

Chapter Two starts with explaining the reasons for the need of a rail-to-rail operation. Different architectures available for constant *gm* for the rail-to-rail architectures and their comparisons.

Chapter Three presents the analysis of complementary input stage and introduces the idea of overlapping the transition region of tail current for the n- and p-pairs to achieve overall constant *gm* using PMOS level shifter as a solution to achieve the rail-to-rail input common-mode range.

Chapter Four presents the calculations and the simulation results of the final circuit, the schematic and layout both have been displayed and LVS has been performed, Post layout simulation and Process corner simulation also have been displayed.

Finally Chapter Five, which is the concluding chapter the design, has been analyzed for further improvements, which are possible.

CHAPTER 2

LITERATURE SURVEY

This chapter explains about a number of common input stages and output stage for rail to rail op amp and also explains how the design is shaped by constraint from specification. Input common mode range and output rail to rail swing requirement is primary constraint. The related constraints are DC loop Gain, UGB, Slew rate.

2.1 RAIL TO RAIL OPERATION

Operational amplifiers are the back bone for many analog circuit designs. It is used in numerous applications such as amplifiers and filters. The operational amplifier can be used in two basic configurations: inverting and non-inverting. These configurations place different requirements on the common-mode input range. The required range varies from almost zero to a full rail to rail.

The differential amplifier is used as the input stage for operational amplifiers. The problem is that it will behave as a differential amplifier only over a limited range of common-mode input. Therefore, to make the operational amplifier versatile, its input stage should work for rail to rail common-mode input range. The most common method to achieve this range is to use a complementary differential amplifier at the input stage. This method uses an n-type and a p-type differential pairs simultaneously. Although the method achieves a rail to rail common-mode input operation, it introduces suboptimal operational amplifiers. This is due to the non-constant transconductance (gm) of the complementary differential amplifier. However, there are methods that keep gm variations small over the entire input common mode range.

2.1.1 THE INPUT STAGE

The input stage of every op-amp is a differential amplifier. In CMOS technology the differential amplifier can be realized using a PMOS or NMOS differential pair. There are several tradeoffs that determine which differential pair to use. One criterion that is considered in making the choice is the common mode input range. To analyze the common mode input range of the NMOS differential input stage, a simplified diagram will be used as shown in Figure2.1. Several modifications are made to the simple differential pair in actual implementation such as active loads and cascodes, however this is sufficient for the purpose of illustration. The range extends from the positive

supply to (Vgs,n + VDsat,b) above the negative supply. This minimum voltage is needed to keep the NMOS differential pair and the tail current source in saturation.

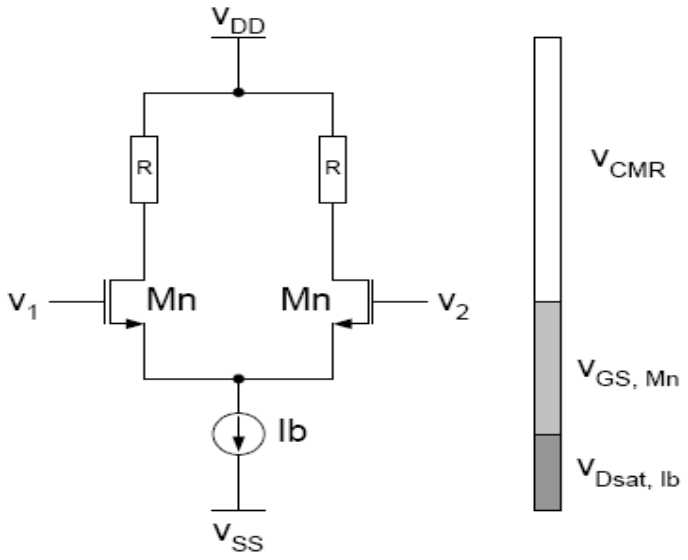


Fig2.1 NMOS Differential Pair Common Mode Input Range

A similar analysis can be carried out for the PMOS differential pair shown in Fig2.2. The range extends from Vgs,n+VDsat,b below the positive supply to the negative supply. This minimum voltage is needed to keep the PMOS differential pair and the tail current source in saturation.

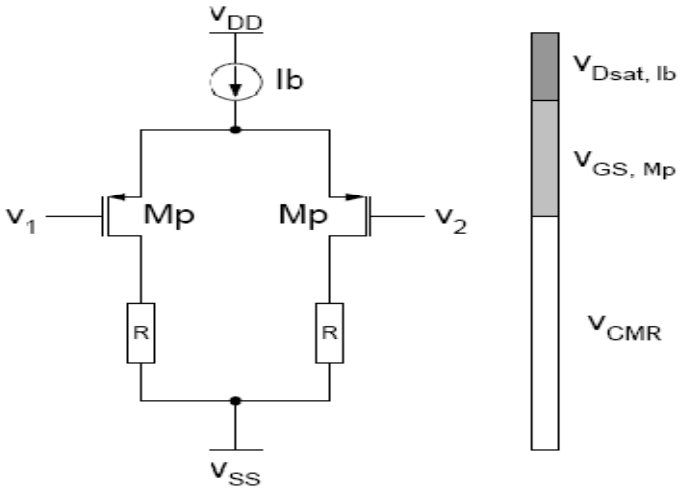


Fig2.2 PMOS Differential Pair Common Mode Input Range

The simple differential pair can not meet the rail to rail common mode input requirement. A possible solution to the problem is to use both NMOS and PMOS

differential pairs simultaneously. The resulting compound differential pair is called the complementary differential pair and is shown in Figure 2.3.

For low common mode input, the PMOS differential pair is in saturation and NMOS is off. For high common mode input, the NMOS differential pair is in saturation and PMOS is off. Therefore, the total effect is that the complementary differential pair is always working and the rail to rail common mode input requirement is met.

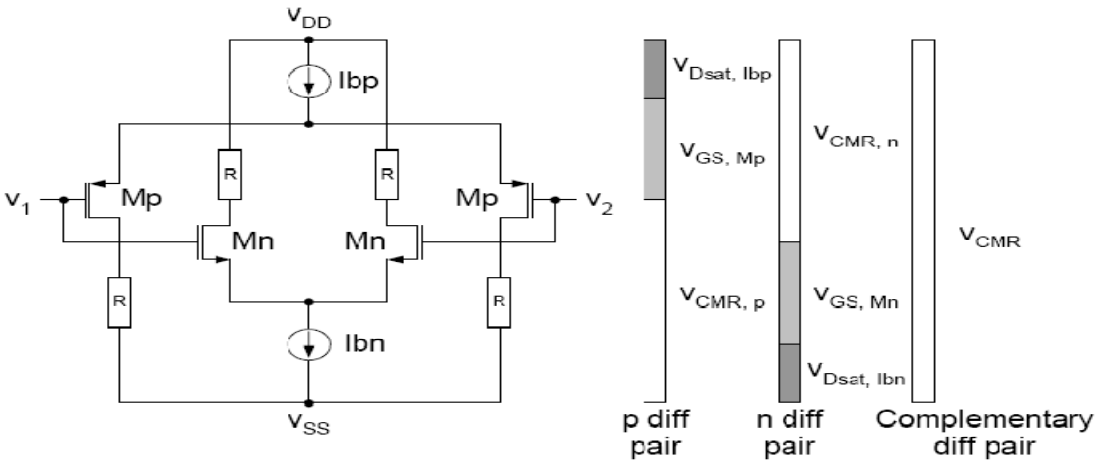


Fig2.3 Complementary Differential Pair Common Mode Input Range

It should be noted that for common mode input in the middle region both pairs are working, this will have a significant effect on the performance of the circuit. To understand the effect, how the transconductance of each pair and of the complementary pair changes with common mode input signal. First the transconductance verses input common mode of the NMOS pair is shown in Figure 2.4.

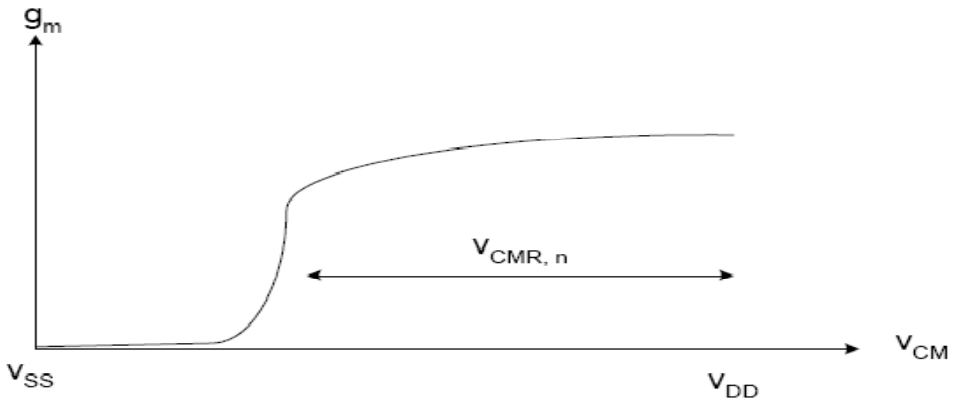


Fig2.4 NMOS Differential Pair Transconductance Verses Input Common Mode

Similarly, the transconductance verses input common mode of the PMOS pair is shown in Fig 2.5.we see that the transconductance of each pair is almost constant over its common mode range and drops to zero outside this range.

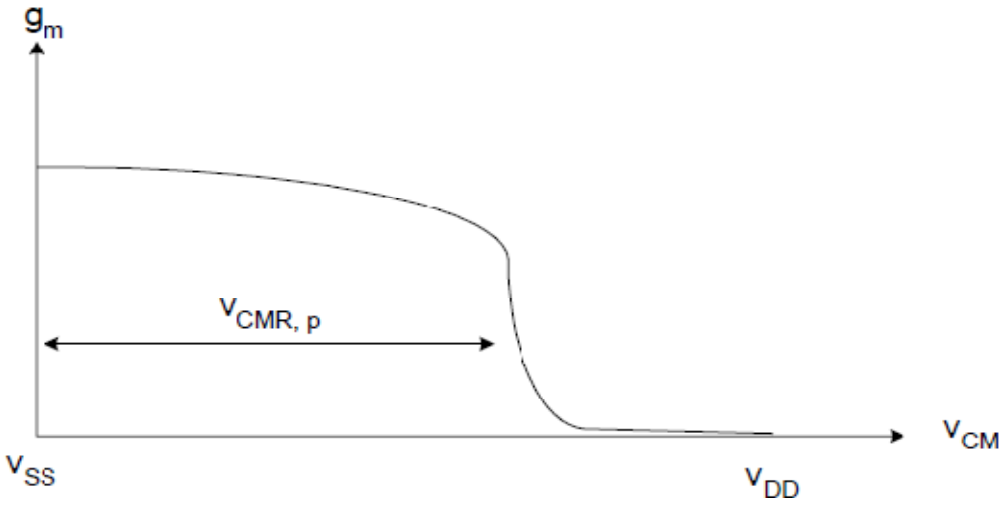


Fig2.5 PMOS Differential Pair Transconductance Verses Input Common Mode

Combining these two graphs gives the transconductance verses input common mode of the complementary pair as shown in Fig2.6. It is assumed here that both pairs in the complementary structure had been sized appropriately to obtain equal transconductance in their region of operation.

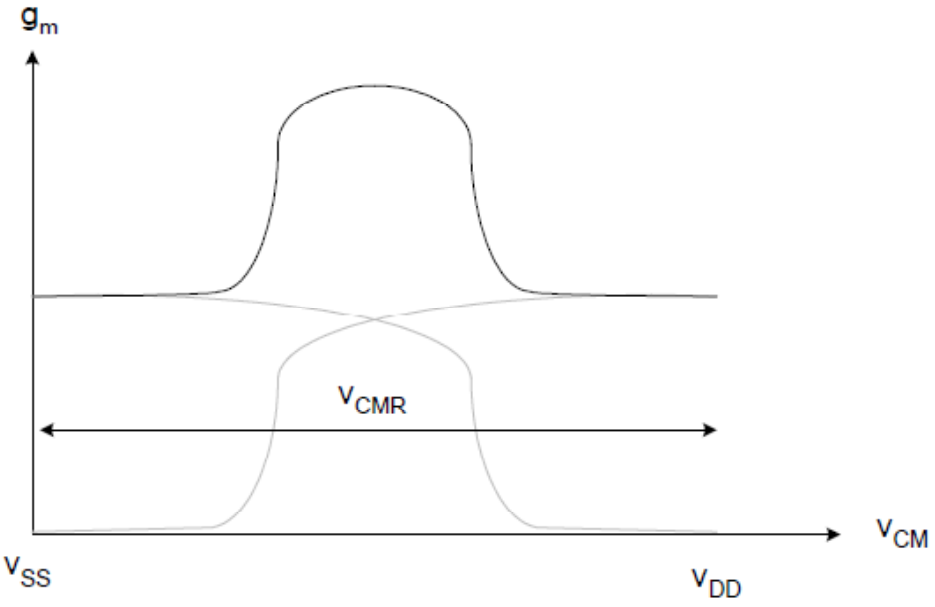


Fig2.6 Complementary Differential Pair Transconductance Verses Input Common Mode Voltage

The transconductance of the complementary differential pair ($g_{m,np}$) is almost constant for high or low common mode input when only one of the pairs is active.

In the middle region, both pairs are on and the effective transconductance is twice that of the other regions. The large variations in the transconductance will result in a suboptimal op-amp design with the complementary differential pair used as the input stage.

The large variation of the complementary differential pair transconductance is not desirable. Its main disadvantage is the power suboptimal frequency compensation of the amplifier. Methods for reducing the transconductance variation are discussed next.

2.1.2 CONSTANT TRANSCONDUCTANCE INPUT STAGE

We need to formulate $g_{m,np}$ to explore possible methods for achieving a constant transconductance input stage. Assuming all transistors are in the saturation region and using the square law models, the complementary differential pair transconductance is given by:

$$g_{m,np} = g_{m,n} + g_{m,p} \quad (2.1)$$

$$g_{m,np} = \sqrt{\mu n\, Cox(\frac{w}{l})In} + \sqrt{\mu pCox\frac{w}{l}Ip} \quad (2.2)$$

Or, $$g_{m,np} = \mu n\, Cox\left(\frac{w}{l}\right)Veff,n + \mu p\, Cox\left(\frac{w}{l}\right)Veff,p \quad (2.3)$$

Investigating these formulas gives us suggestions on how to keep gm,np constant. From (2.1), we see that we can accomplish this by controlling the tail current or the aspect ratio of either NMOS or PMOS differential pair or both. From (2.2), we see that we can also obtain constant gm,np by controlling the effective voltage of the transistor.

2.1.2.1 Constant $g_{m,np}$ by means of Tail Current Control

We will start with a condition to simplify the relationship given by (2.1). If we choose:

$$\sqrt{\mu n\, Cox\, \left(\frac{w}{l}\right)} = \sqrt{\mu p\, Cox\, \left(\frac{w}{l}\right)} = k \quad (2.4)$$

Then 2.1 simplifies to:

$$gm,np = k\left(\sqrt{In} + \sqrt{Ip}\right) \quad (2.5)$$

Therefore, to keep gm,np constant, we have to keep $\left(\sqrt{In} + \sqrt{Ip}\right)$constant. This can be done using translinear circuits to obtain a square root biasing scheme. The

disadvantage of this design is its relative complexity. Also, it is not very accurate since it uses the square law models of the MOS transistors and for today's deep submicron technology; there is a significant deviation from the ideal relation.

Another method that uses tail current to maintain constant $g_{m,np}$ can be understood by putting another condition $\sqrt{In} = \sqrt{Ip} = \sqrt{I}$ therefore Equation 2.4 becomes:

$$g_{m,np} = 2k\sqrt{I} \qquad (2.6)$$

However, $g_{m,np}$ is only half the value given in *(2.5)* when only one differential pair is operating because I is half. Therefore, in the regions where one pair is working, an increase in the tail current by a factor of 4 will keep $g_{m,np}$ constant. This can be implemented by diverting the tail current of the non working pair to the working pair after multiplying by a factor of 3. The multiplication by 3 can be accomplished by using a three-times current mirror. The disadvantage of this technique is the limited accuracy due to ideal square law dependence. Also, the transition between the three regions is not well controlled and will cause variations in $g_{m,np}$.

2.1.2.2 Constant $g_{m,np}$ by means of Voltage Control

We can rewrite equation (2.2) using condition (2.3) to simplify the expression, we get the following:

$$g_{m,np} = k^2(Vgs,n + Vsg,p - Vthn - |Vthp|) \qquad (2.7)$$

Therefore, to keep $g_{m,np}$ constant, we have to keep $Vgs,n + Vsg,p$ constant. This can be done by connecting a voltage source between the common source of the NMOS and the common source of the PMOS differential pairs. This will keep both pairs working for all common mode input voltage. One method for implementing the voltage source is by using two diode connected MOS transistors and sizing them appropriately. The disadvantage of this technique is that the behaviour of the diode connected transistors is a function of the voltage across them. Therefore, $g_{m,np}$ still has some variations over the common mode input range.

2.1.2.3 Constant $g_{m,np}$ by means of Aspect Ratio Control

A closer look into (2.2) or (2.3), reveals the possibility of controlling gm,np by controlling the aspect ratio of one or both differential pairs. One method for implementing this is by using a second NMOS and a second PMOS differential pairs in standby that are connected in parallel to the complementary differential pair. In the middle region of operation, both pairs in the complementary differential pair are

operating and the other two pairs are off. To explain how the circuit operates in the other two regions, let's start with the input common mode voltage in the middle region and going down towards Vss. When the voltage becomes low enough for the PMOS pair to turn off, the other NMOS differential pair will be activated. Effectively, doubling the aspect ratio for low common mode input, therefore, $g_{m,np}$ is constant. The same happens if the voltage increases towards V_{dd}, the second PMOS differential pair will be activated and the effective aspect ratio is doubled to keep $g_{m,np}$ constant. The disadvantage of this technique is that in the transition between the three regions results in a non-smooth current transition. This causes relatively large variations in $g_{m,np}$ which results in a suboptimal performance.

2.1.2.4 Constant $g_{m,np}$ by Alternative Means

This section reports two alternative methods for making $g_{m,np}$ constant.

The first method utilizes a maximum selection circuit. The principle of operation is to allow only one pair to operate in the middle region.

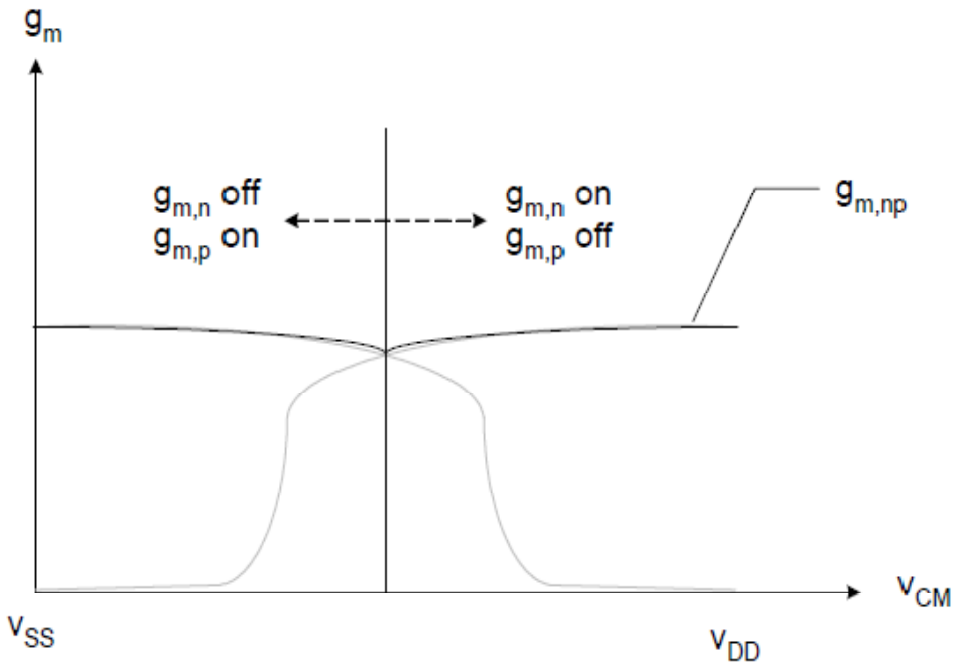


Fig2.7 Selecting Maximum g_m

This can be done by keeping the differential pair that has the larger tail current operating and turn the other differential pair off. The scheme assumes that the differential pair with larger tail current is operating properly while the other pair is going into (or just coming out of) triode region. The principle is illustrated in Figure

10. The disadvantage of this design is its relative complexity. This method was used in [4] and [5] which achieves 5% $g_{m,np}$ variations. Another alternative method uses DC level shifting. The principle of operation is to shift the transconductance characteristics curve of the NMOS differential pair to the left or the transconductance characteristics curve of the PMOS differential pair to the right such that the sum of g_{mn} and g_{mp} is constant. This can be accomplished simply by applying a DC level shift to the NMOS pair (or PMOS pair) to make its turn on voltage higher (or lower).
The principle is illustrated in Fig2.8 for NMOS shift.

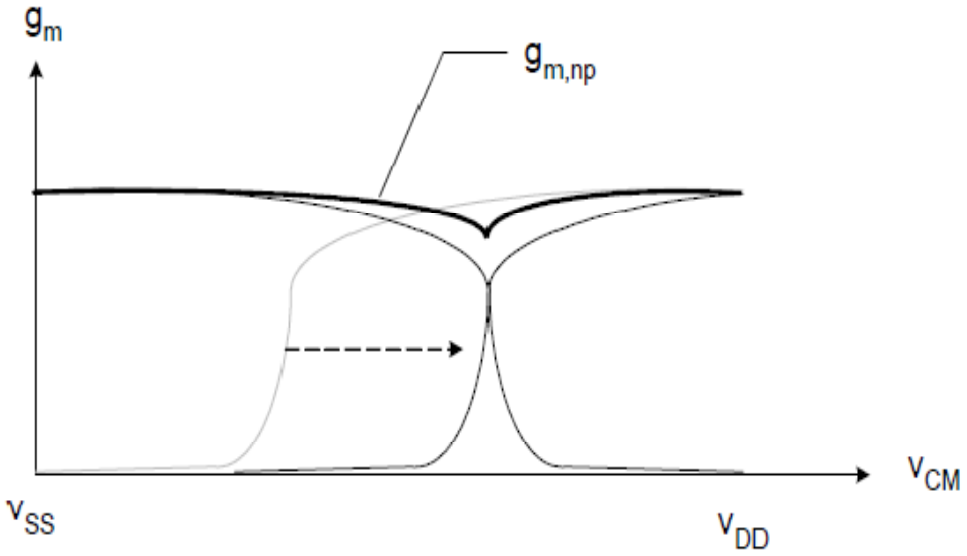


Fig2.8 DC Level Shifting

The disadvantage of this method is its need for tuning. Because the characteristics will vary with process, voltage, and temperature, the optimal DC level will change. If the shift level is not tuned, large or small $g_{m,np}$ will appear around the transition region, therefore, instability might occur. This method was used in [11] and achieves 13% gm,np variations before tuning and 5% $g_{m,np}$ variations after tuning.

2.1.2.5 Summary of Constant $g_{m,np}$ Methods

This section provides a summary of all the methods discussed to achieve constant transcond- uctance for the complementary differential input stage.

Table 2.1 Comparison of Various Constant g_m Methodology

Principle	$g_{m,np}$ variation
Tail current control I: $(\sqrt{In} + \sqrt{Ip})$=constant	10% [2] 5% [3]

Tail current control II: $(\sqrt{I}\,)$= constant	15% [4], [5], and [6]
Voltage control	8% [7] 28% [7]
Aspect ratio control	20% [8]
Maximum selection circuit	5% [9] and [10]
DC level shifting	13% [11] before tuning 5% [11] after tuning

2.1.3 OUTPUT STAGE

A typical op amp consists of a differential input stage, intermediate gain stage, and a class AB output stage. Class AB buffers are used for their relatively high power conversion efficiency and for their current-handling capabilities which allow them to drive small resistive loads. Under idle conditions, the quiescent current (Iq) must be as small as possible to reduce the standby power consumption, while the current in the class B mode should be as large as possible [13].

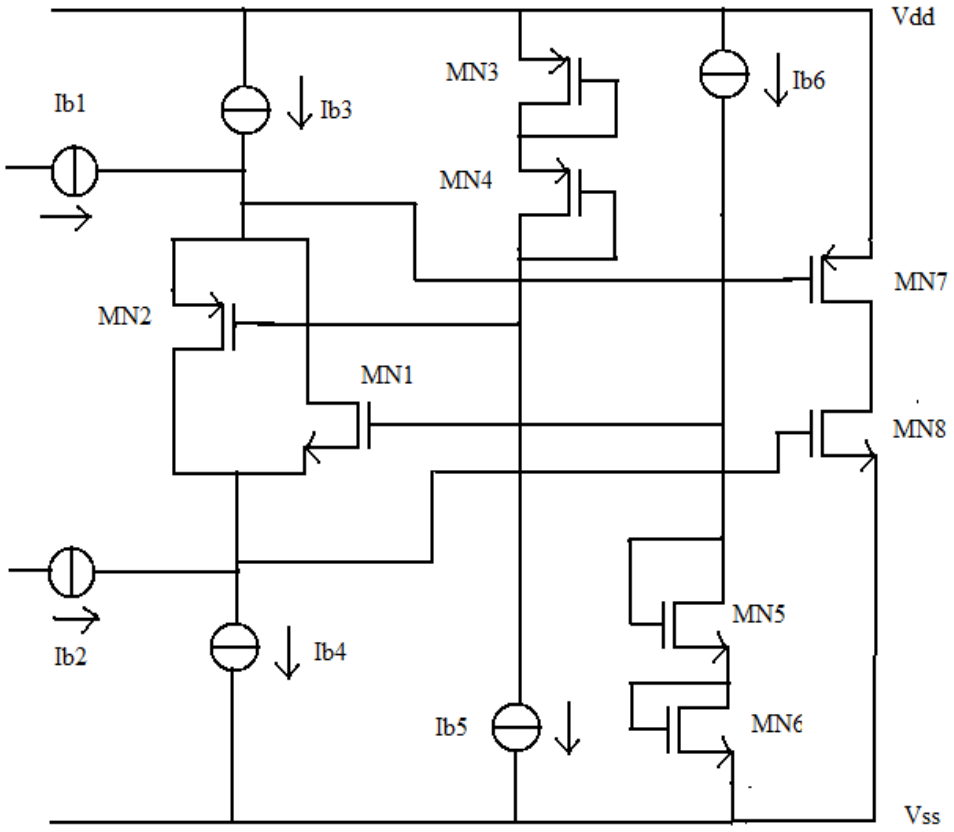


Fig.2.9 Rail-to-rail output stage with floating class-AB control

In a conventional 5 V op amp, source followers are widely used as class AB buffers because of their low output impedance. They are, however, not suitable for low-voltage applications because of their small output swing.

To make efficient use of the supply voltage and supply current, an opamp requires class-AB biased output transistors connected in a common-source configuration. Moreover, the class-AB control should be compact to efficiently use die area.

The compact class-AB output stage is shown in Fig. 2.9. It consists of two common-source connected output transistors, MN7 and MN8, which are directly driven by two in-phase signal currents, Ib1 and Ib2. The floating class-AB control is formed by MN1 and MN2. The stacked diode-connected transistors, MN3 - MN4 and MN5 – MN6, bias the gates of the class- AB transistors MN7 and MN8, respectively. As was shown in the previous section the minimum required supply voltage is limited by the demand for a fully rail-to-rail common-mode input range. Therefore, two stacked gate-source voltages are allowed in the class-AB output stage. The floating class-AB control transistors, the stacked diode connected transistors and the output transistors set up two translinear loops MN2, MN3, MN4, MN7 and MN1, MN5, MN6 and MN8 which determine the quiescent current in the output transistors.

The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. Suppose the in-phase signal current sources, I_{bl} and I_{b2}, are pushed into the class-AB output stage. As a result, the current of the P-channel class-AB transistor, MN2, increases while the current in the N-channel class-AB transistors, MN1, decreases by the same amount. Consequently, the gate-voltages of both the output transistors move up. Thus the output stage pulls a current from the output node. This action continues until the current through the P-channel class-AB transistor is equal to Ib3**.** Now, the current of the P-channel output transistor is kept at a minimum value, which can be set by *W* over *L* ratios of the class-AB control transistors. Note that the current through the N-channel output transistor is still able to increase. A similar discussion can be held when input signals are pulled from the class-AB output stage.

A drawback of the Class-AB control is that the quiescent current of the output transistors depends on supply voltage variations. The supply voltage variations are directly put. By the gate-source voltages of the output transistors, across the finite output impedances of the floating class-AB transistors. The result is a power-supply dependent variation of the quiescent current.

CHAPTER 3

DESIGN OF RAIL TO RAIL OPAMP

As different constant g_m topologies are discussed in last chapter an immediate and simple technique for reducing the variations in the small-signal response of rail-to-rail input stages, consists in shifting the CM response of one input pair so as to make its transition region to overlap that of the complementary input pair. Indeed, with this approach, provided that the two differential pairs are perfectly matched, variations in the total amplifier transconductance can only arise in the common transition region of the two pairs, and are much lower with respect to the traditional composite rail-to-rail input stages. In the particular case of this figure, an appropriate positive value of *VS* shifts the takeover region of the PMOS input pair, as seen by the signal inputs *V*i+ and *Vi*-, to a V_{icm} voltage range closer to the lower supply voltage. The idea of overlapping the takeover regions in rail-to-rail input stages has been introduced in the literature [11].

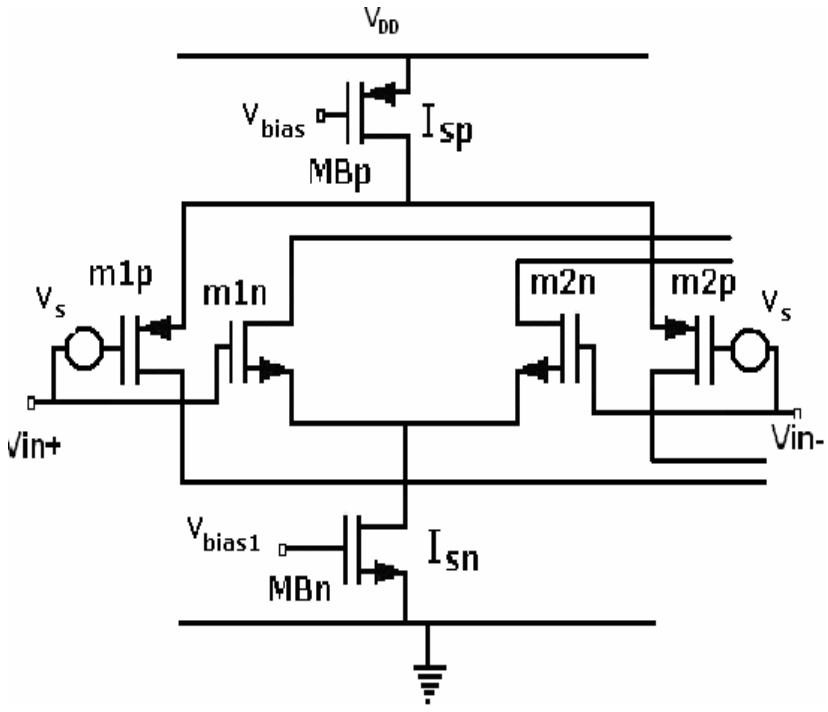


Fig 3.1 Rail-To-Rail CMOS Amplifier Input Stage with Floating Voltage Sources *Vs* for CM Response Overlapping.

3.1 IMPLEMENTATION OF RAIL TO RAIL OP-AMP

The op-amp consists of three stages:

1) Complementary input stage with constant gm circuitry,

2) Folded cascode summing stage,

3) Class AB output stage

3.1.1 ANALYSIS OF COMPLEMENTARY INPUT STAGE

The schematic of a complementary input stage is shown in Fig.3.2, where M1n, M2n, and M1p, M2p constitute the n- and p-type differential input pairs, respectively. The N-channel input pair,m1n & m2n, is able to reach the positive supply rail while the P-channel input pair, m1p & m2p, is able to reach the negative supply rail. A drawback of the rail-to-rail input stage is that its gm varies by a factor of two over the common-mode input range. In order to obtain a constant gm over the common-mode input range, the gm at the lower and upper part of the common mode input range has to be increased by a factor of two. Since the gm of a MOS transistor operating in strong inversion is proportional to the square-root of its drain current, the tail current of the actual active input pair could be increased by a factor of four.

This principle is realized in the circuit as shown in Fig.3.2 [13]. The gm-control is implemented by means of two current switches, m3n and m5p, and two current mirrors, m3p – m4p and m5n – m4n each with a gain of three. The principles of the gm control can be best understood by dividing the common-mode input range into three parts. If low common-mode input voltages are applied, only the P-channel input pair operates.

The N-channel current switch conducts while the P-channel one is off. The N-channel current switch takes away the reference current I_{sn} and directs it to the current mirror, m3p-m4p, where it is multiplied by a factor three and added to I_{sp}. Since I_{sp} and I_{sn} are equal, the tail-current of the P-channel input equals $4I_{sn}$.

If intermediate common-mode input voltages are applied, the P-channel as well as the N-channel input pair operates. Now, both current switches are off. The result is that the tail currents of the N-channel input pair and that of the P-channel input pair are equal to I_{sn} or I_{sp}. If high common-mode input voltages are applied only the N-channel input pair operates. The P-channel current switch conducts while the N-channel current switch is off. The P-channel current switch takes away the current I_{sp} and feeds it into the current mirror, m4n-m5n, here it is multiplied by a factor 3 and added to the current I_{sn}. The result is that the tail-current of the N-channel input pair equals

$4I_{sn}$.It can be calculated that for each part of the common-mode input range the gm is given by:

$$g_m = \sqrt{k\ Isn} \tag{3.1}$$

With,

$$k = \mu_n c_{ox}(w/l)_n = \mu_p c_{ox}(w/l)_p \tag{3.2}$$

where μ is the mobility of the charge carriers, Cox is the normalized oxide capacitance, *W* and *L* are the width and the length of a transistor, respectively. The subscripts n and p refer to an N-channel or P-channel input transistor respectively.

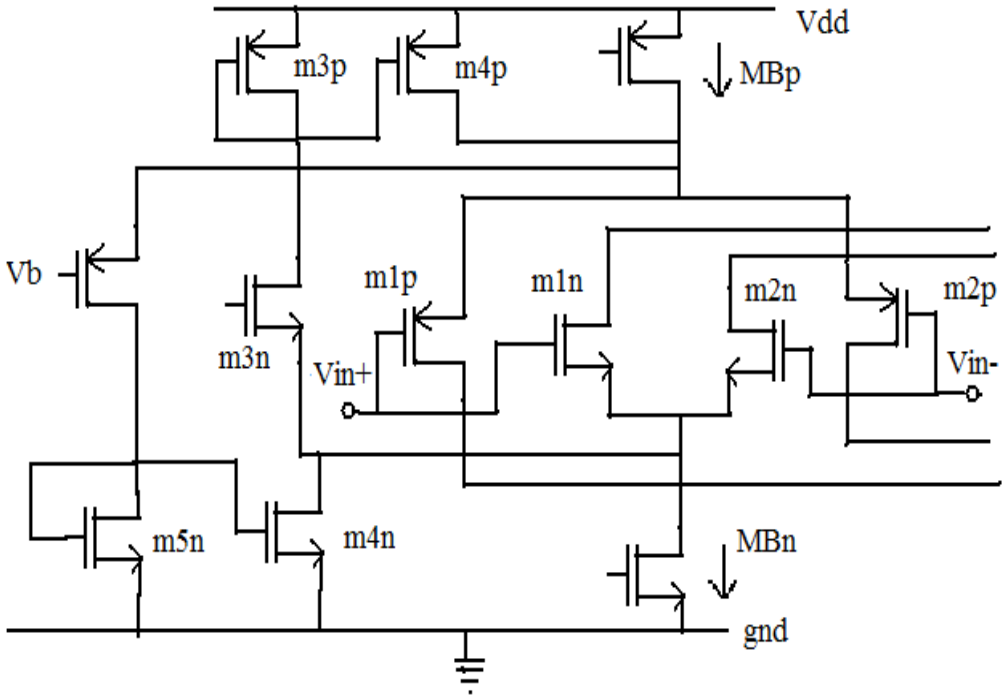


Fig.3.2 Schematic of Complementary Input Stage With g_m Control Circuitry

From (3.2) it can be observed that for a constant gm the w over l ratios of the P-channel and the N-channel input pair has to obey the following relation:

$$\frac{\mu_n}{\mu_p} = \frac{(w/l)_p}{(w/l)_n} \tag{3.3}$$

If the ratio μ_n over μ_p differs from its nominal value because of process variations, the gm will have an additional variation.

3.1.2 CASCODE SUMMING STAGE

The amplifier uses a folded-cascode current-summing gain stage output branches to provide output voltage for the class AB output stage. The gain stage consists of PMOS cascode transistors M4, M8 and NMOS cascode transistors M5, M9 along with PMOS current sources M3, M7 and NMOS current sources M6, M10.

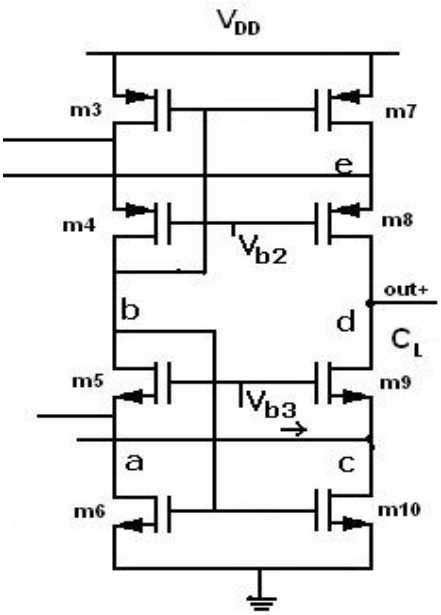


Fig 3.3 Cascode Summing Stage

3.1.3 CLASS AB OUTPUT STAGE

To make efficient use of the supply voltage and supply current, an opamp requires class-AB biased output transistors connected in a common-source configuration. Moreover, the class-AB control should be compact to efficiently use die area [5].

The floating class-AB control transistors, the stacked diode connected transistors and the output transistors set up two translinear loops m13, m14, m11, m17 and m12, m15, m16, m18, which determine the quiescent current in the output transistors. The class-AB action is performed by keeping the voltage between the gates of the output transistors constant. The current of the P-channel class-AB transistor, M11, increases while the current in the N-channel class-AB transistors, M12, decreases by the same amount. Consequently, the gate-voltages of both the output transistors move up. Thus the output stage pulls a current from the output node. The current of the P-channel output transistor is kept at a minimum value, which can be set by W over L ratios of the class-AB control transistors.

A drawback of the Class-AB control is that the quiescent current of the output transistors depends on supply voltage variations. The supply voltage variations are directly put by the gate-source voltages of the output transistors, across the finite output impedances of the floating class-AB transistors. The result is a power-supply dependent variation of the quiescent current.

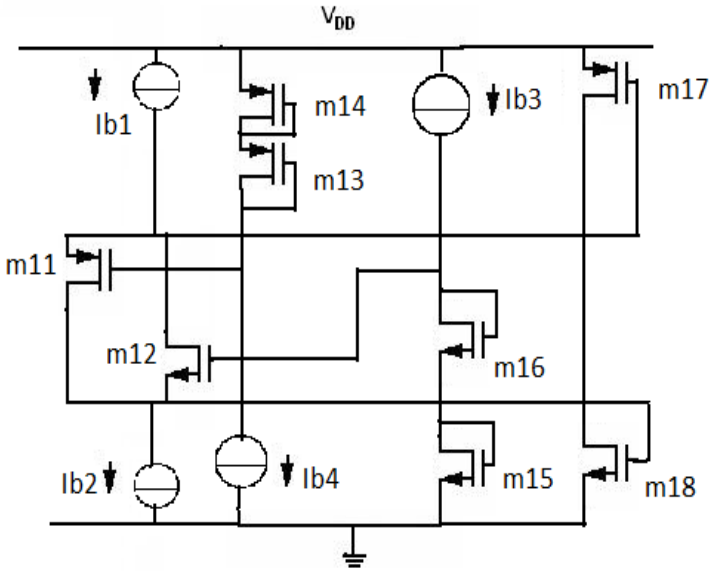


Fig 3.4 Class AB Output Stage with Quiescent Current Control Circuitry

An alternative way to reduce the noise and offset contribution of the class-AB control, without the cost of die area and a loss of unity-gain frequency, is to shift the floating class-AB control, m11 and m12 in to the summing circuit, the floating class-AB control is biased by the cascodes of the summing circuit. Now, the noise and offset of the amplifier are mainly determined by the input transistors and the summing circuit. A drawback of shifting the class-AB control into the summing circuit is that the quiescent current of the output transistors depends on the common-mode input voltage. When the common-mode input voltage varies, the tail currents of the input pairs, and therefore the currents through the cascades change. The result is that the bias current of the class-AB control, and consequently the quiescent current of the output transistors, depends on the common-mode input voltage.

This problem can be overcome by using a summing circuit with two current mirrors which are biased by two separate current sources [5]. A drawback of the separate biased current mirrors is that the bias current sources of the current mirrors contribute to the noise of the amplifier because the current gain between the current sources and the drain currents of the input transistors is equal to one. Mismatch in the bias current

sources will also contribute to the offset of the amplifier. Because of the floating architecture of the current source, it does not contribute to the noise and offset of the amplifier [5], [15]. The class-AB control, and therefore the quiescent current in the output transistors, suffers from supply voltage variations. To make the quiescent current of the output transistors insensitive to supply voltage variations, the floating current source should have the same supply voltage dependency as the class-AB control. Fig. 3.5 shows the amplifier with a practical realization of such a floating current source m21 and m22. The floating current source has the same structure as the floating class-AB control.

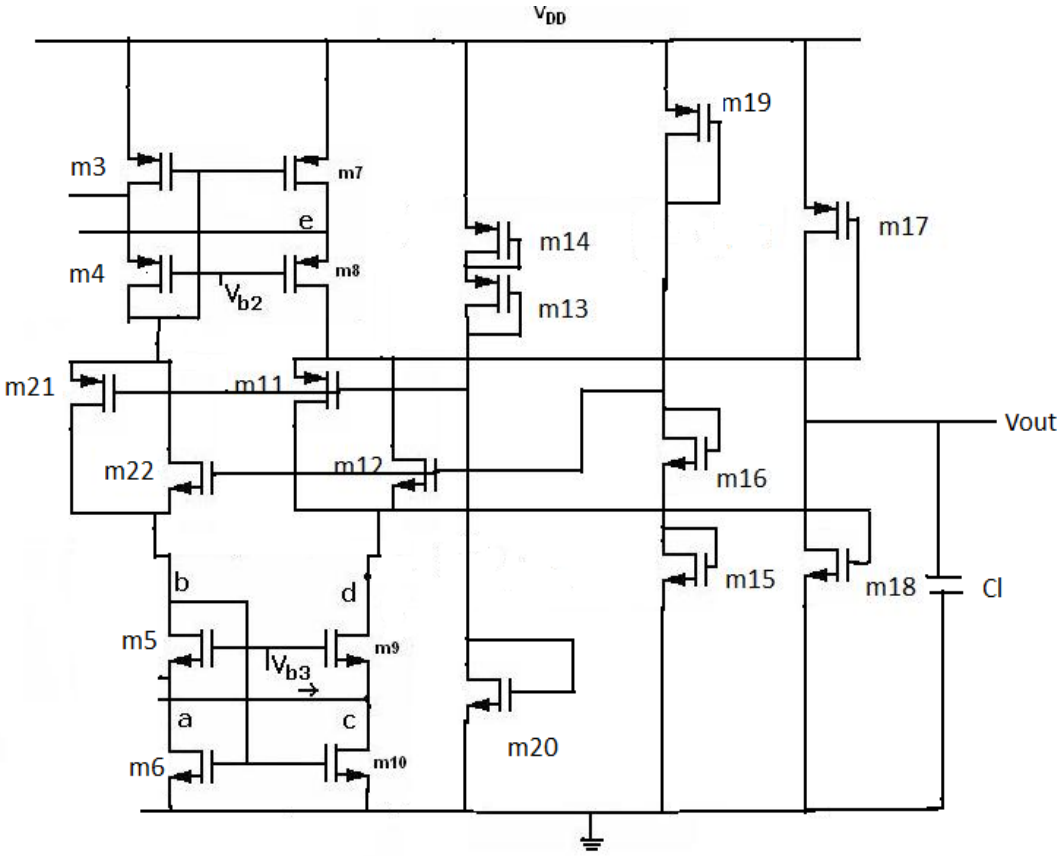


Fig 3.5 Complete Class AB Output Stage with Class AB Control Circuitry

3.2 OVERALL CIRCUIT DESIGN

A compact opamp with Miller compensation has been designed, and is shown Fig. 3.6. The opamp consists of the rail-to-rail input stage, m1n, m2n, m1p, m2p, gm-control, m3n-m5n and m3p-m5p , a summing circuit, m3-m12, and a rail-to-rail class-

AB output stage, m17-m18. The floating current source, m21-m22, biases the summing circuit and the floating class-AB control.

The value of the current source is set by two translinear loops, m13, m14, m3, m21 and m6, m15, m16, m22. The mirrors, m3, m4, m7, m8 and m5, m6, m9, m10, are loaded by the drain currents of the input pairs m1n-m2n and m1p-m2p, respectively. These drain currents, and consequently the gate-source voltages of m3 and m6 change with the common-mode input voltage. If, for example, the common-mode input voltage approaches the positive supply rail, the gm control circuit increases the current I_{sp} and decreases I_{sn}. As a result, the gate-source voltage of m3 decreases while the gate-source voltage of m6 increases. However, this hardly effects the value of the floating current source, m21-m22 because an increase of the gate-source voltage of one mirror compensates for a decrease in the other mirror.

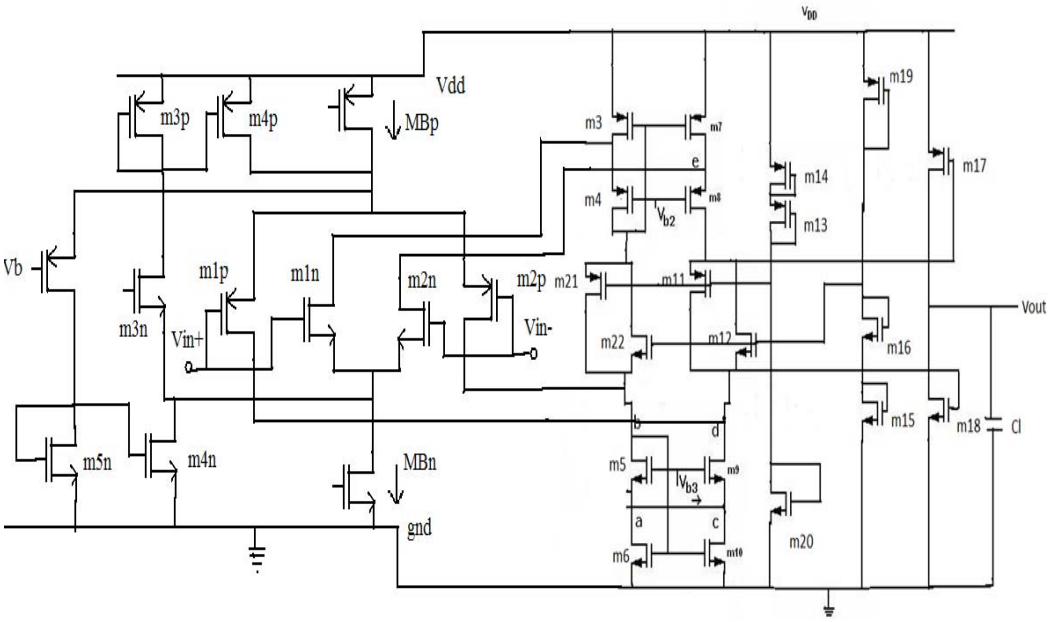


Fig3.5 Complete circuit of Rail-to-Rail Opamp

The capacitors C_{m1} and C_{m2} around the output transistors, m17 and m18, split apart the poles ensuring a 20 dB per decade roll off of the amplitude characteristic. The conventional Miller splitting shifts the output pole up to a frequency of approximately

$$\omega_{out} = \frac{g_{m0}}{C_l} \qquad (3.4)$$

Table 3.1 Rail-to-Rail operational Amplifier Device Sizes

Device	**Width/Length(in Micron)**	**Functions**
m1n, m2n	70/1.4	Input N pair Diff. stage
Mbn	7/1.4	Current Source
m1p, m2p	180/1.4	Input P pair Diff. stage
Mbp	28/7	Current Source
m3n	28/1.4	Constant g_m stage
m5p	8.4/1.4	Constant g_m stage
m3p, m5n	1.4/1.4	Constant g_m stage
m4p, m4n	4.2/1.4	Constant g_m Stage
m3, m4, m7, m8	42/1.4	PMOS Cascode transistors
m5, m6, m9, m10	14/1.4	NMOS Cascode transistors
m11, m21, m13, m14	4.2/1.4	Class AB control stage
m12, m22, m15, m16	1.4/1.4	Class AB control stage
m20	1.75/1.4	Class AB control stage
m19	9.1/1.4	Class AB control stage
m17	46.5/1.4	Class AB output PMOS transistor
m18	17.5/1.4	Class AB output NMOS transistor

CHAPTER 4

SIMULATIONS RESULTS, LAYOUT AND PROCESS CORNER SIMULATION

The amplifier is to be powered from a 3.3 volts power supply and with a tail current reference of 4µA. The current sources/sinks required for biasing can be derived from the given current reference using current mirrors.

Based on the constant-gm input stage using overlapping of transition region, a rail-to-rail input/output CMOS Op Amp has been designed and simulated in a standard 0.35 µm CMOS technology. For Rail to Rail output swing Class AB output stage is used.

4.1 TEST RESULTS

This design provided a gain of 95.7dB with a common mode rejection of over 101 dB. Output Voltage Swing is greater than 3.0 V and ICMR is about 3.3v. Unity gain bandwidth obtained was 8.38MHz. Slew rates obtained were in excess of 2.81V/us. The phase margin came out to be nearly 55^0 making design relatively stable. Power dissipation is nearly 500 µW which is quite low.

4.1.1 AC RESPONSE

In Figure 4.1, one method of measuring the AC performance is presented. In this configuration, the amplifier is open loop, and the AC small signal is applied at the input.

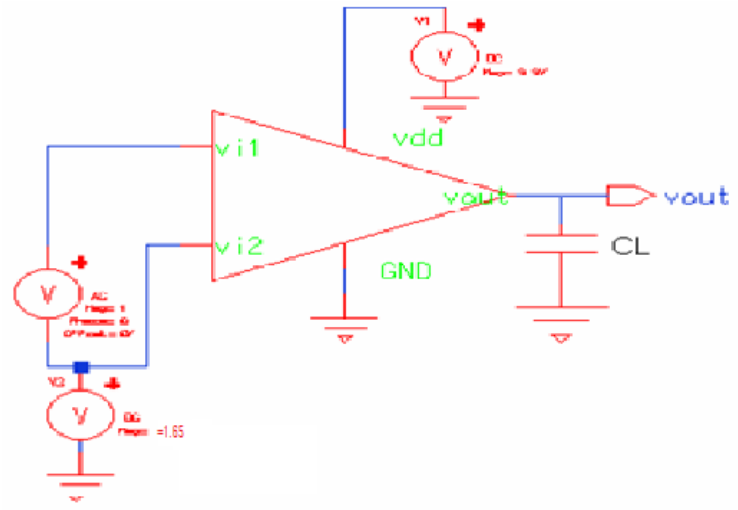


Fig 4.1 Configuration for Simulating Frequency Response of the Open Loop Op-Amp

In Fig 4.2, a Bode and phase plot for 3.3V & 27°C is shown. As can be seen, the open loop gain is above 95dB, and a phase margin is 55.57°. The 3-db frequency is 146.2 Hz and UGB is 8.38 MHz.

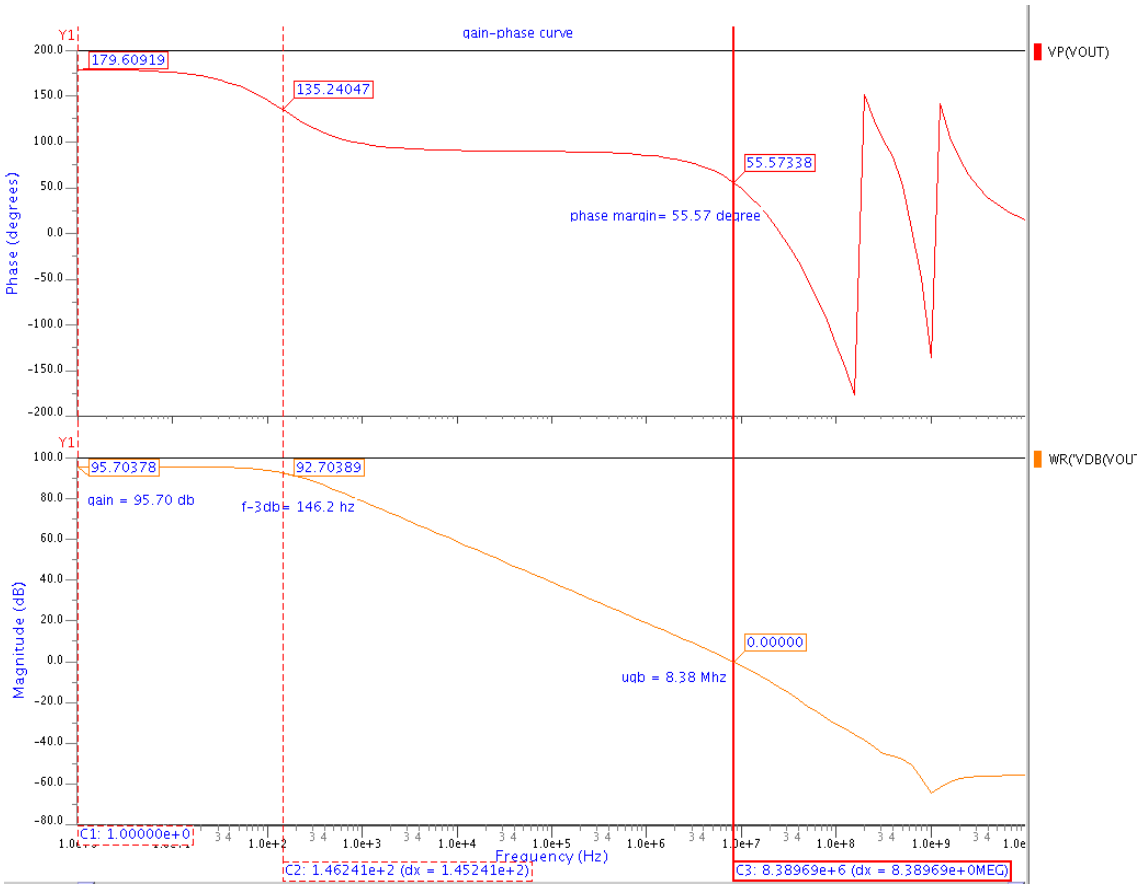


Fig 4.2 Frequency Response of Op-Amp

4.1.2 TRANSIENT RESULTS

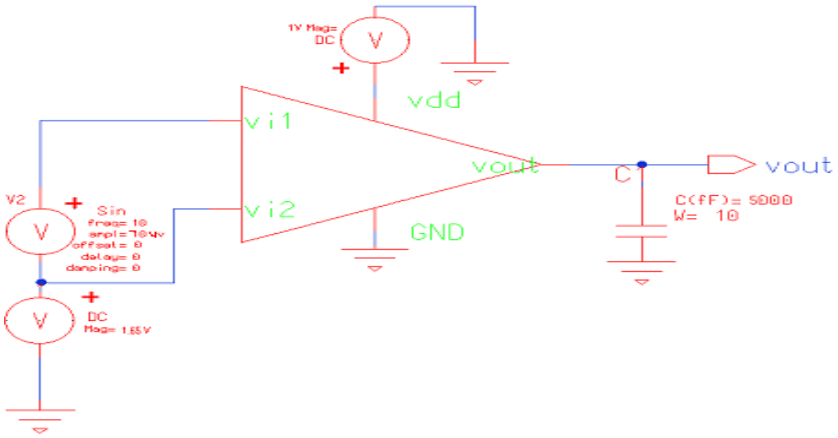


Fig 4.3 Schematic for the Simulation of the Transient Response

A transient simulation of the amplifier in unity gain configuration with the swing at the input rail-to-rail is the most insightful simulation presented (Fig 4.4), because it exercises the amplifier over the entire common mode range and shows the amplifier is not slewing and is exhibiting reasonable linear behaviour.

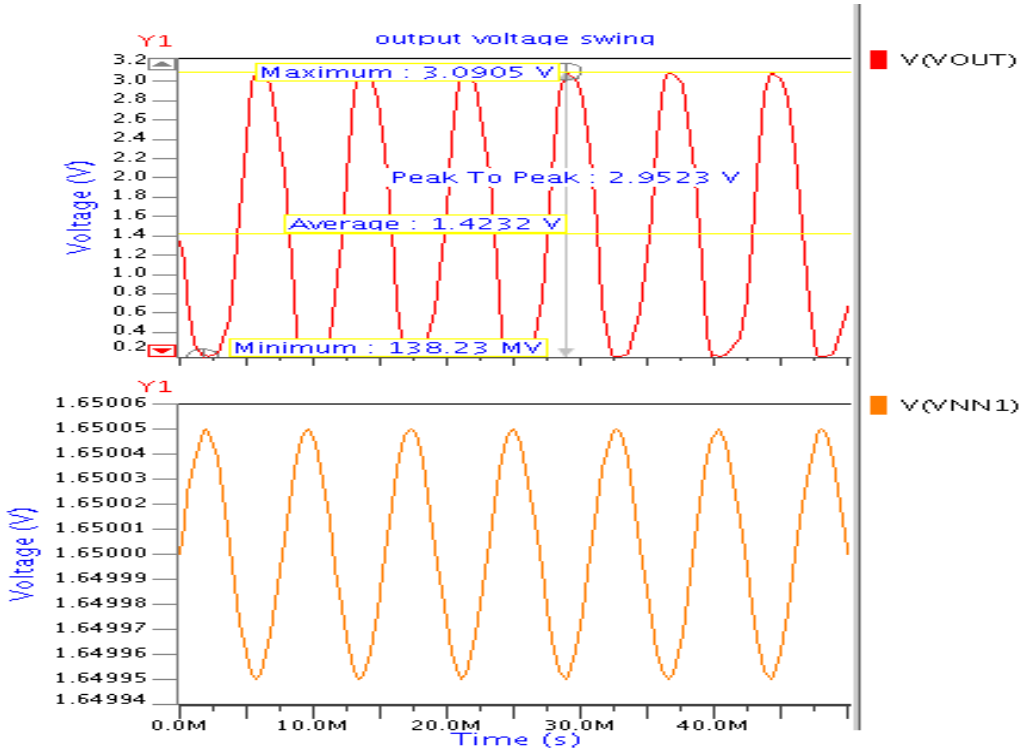


Fig 4.4 Output Voltage Swing

4.1.3 STEP RESPONSE

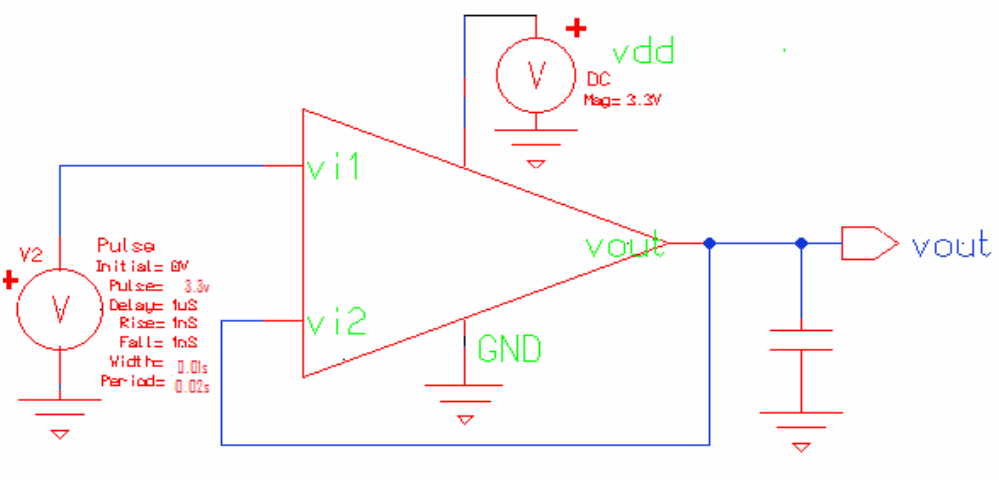
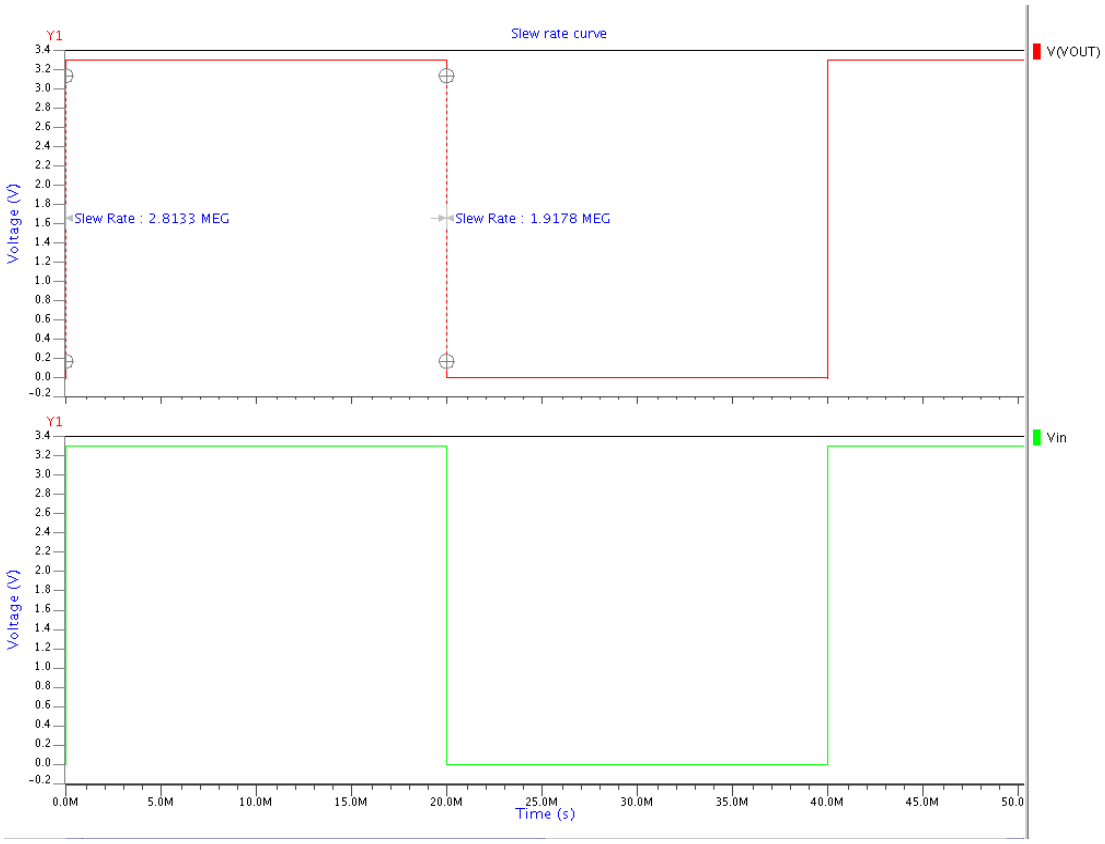
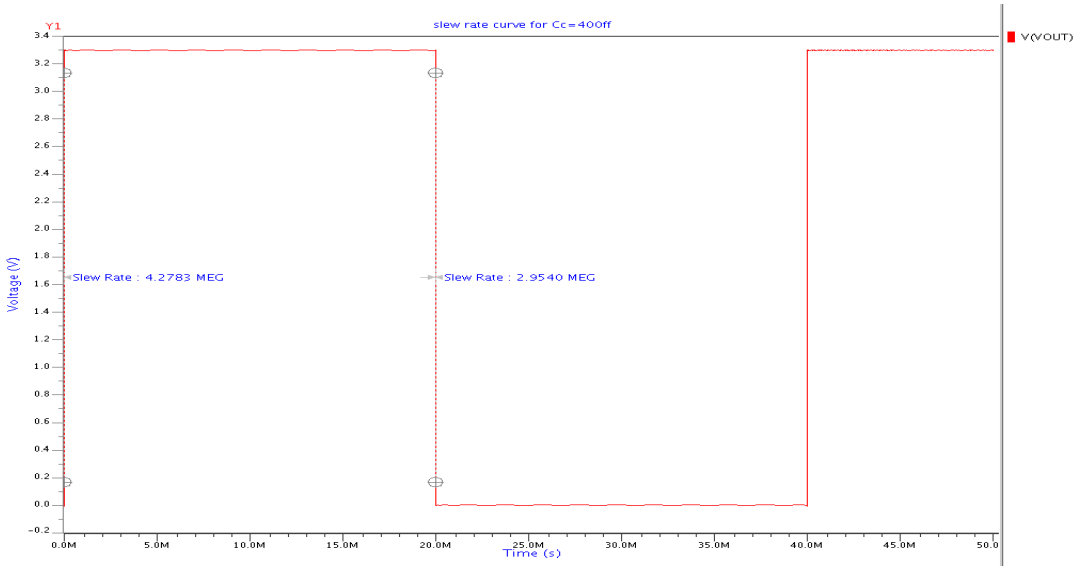


Fig 4.5 Schematic for the Simulation of the Step Response

In Fig 4.6, a step from ground to V_{DD} is applied at the input with unity feedback configuration. The amplifier's slew rate is 2.81V/μs for the rising edge and 1.91V/μs for the falling edge.



. **Fig 4.6 Slew rate for the Rising and Falling Edge with Op amp in Unity Gain Configuration**



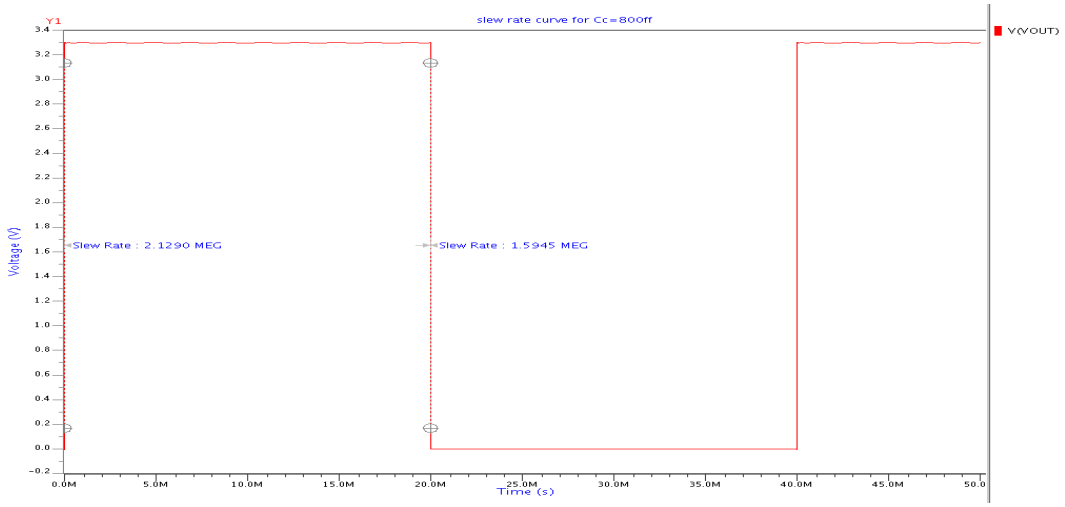


Fig 4.7 Variation of Slew Rate with Change in the Compensation Capacitor values

Fig 4.7 shows the variation of the slew rate with the compensation capacitance .As slew rate is inversely proportional to this capacitance value with the increase in the capacitance value from 400ff to 800fF Slew Rate varies from 4.27V/µs to 2.12V/µs.

4.1.4 SETTLING TIME

This is the length of time for the output voltage of an operational amplifier to approach, and remains within, a certain tolerance of its final value. This is usually specified for a fast full-scale input step. In Fig 4.8 shows the settling time of the input pulse of 3.3V magnitude in unity gain configuration for different tolerance values.

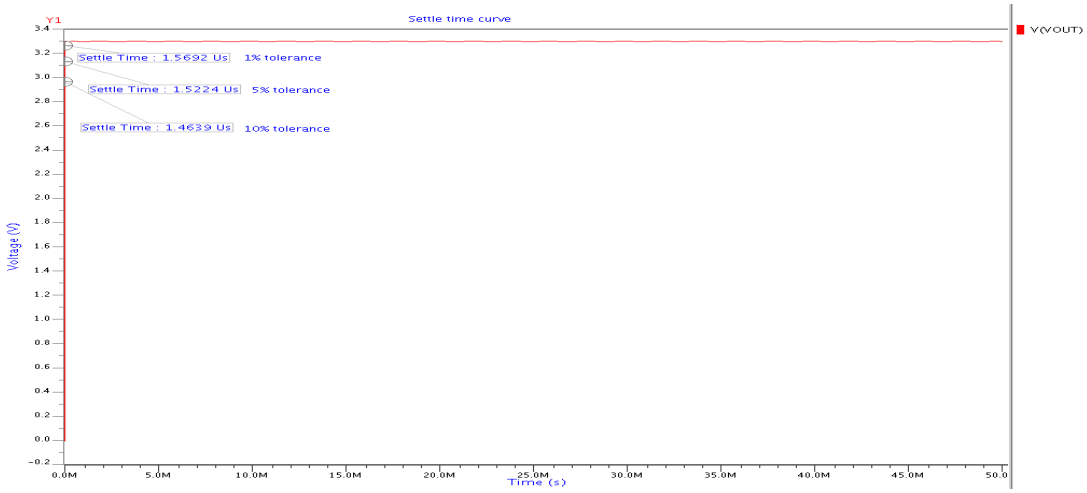


Fig 4.8 Settling time for the Different Tolerance values with Unity Gain Configuration

4.1.5 COMMON MODE REJECTION RATIO

In order to simulate common mode rejection, a 1V AC source is placed on the positive input as shown in Fig 4.9. When the simulator sweeps the frequency, there will be a 1V AC source on both the positive and negative inputs and hence the AC signal at the output will be the common mode gain. The previously calculated gain (Fig 4.2 can be divided by this gain to give the CMRR. The common mode rejection ratio was found to be 101dB at low frequency.

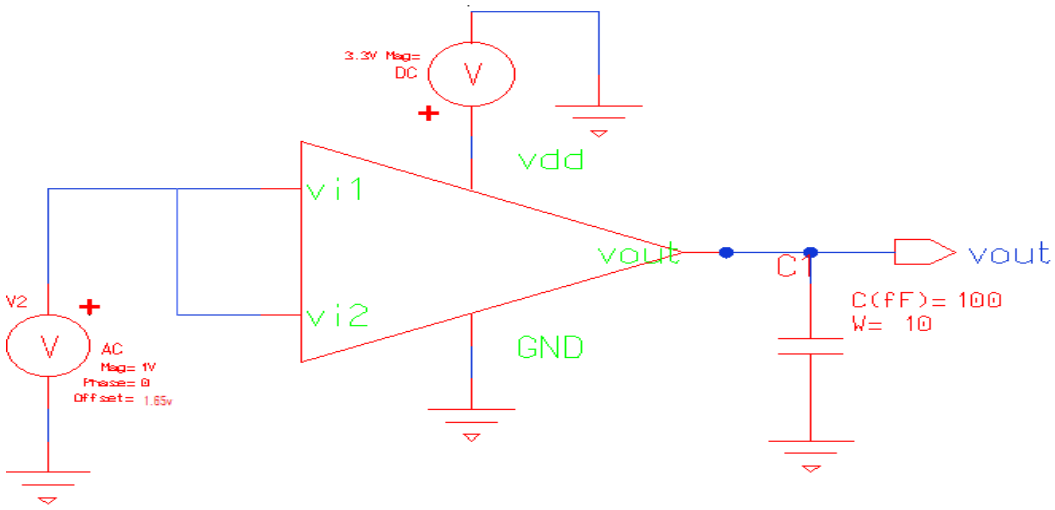


Fig 4.9 Schematic for the simulation of CMRR

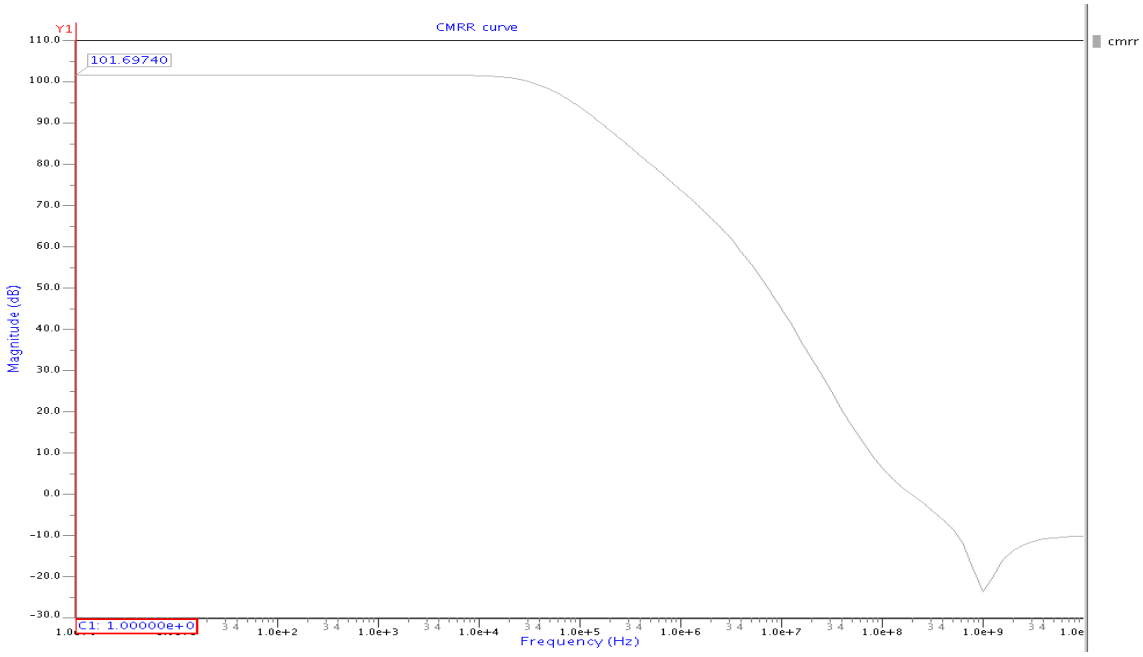


Fig 4.10 Simulation Result of Common Mode Rejection Ratio

4.1.6 POWER SUPPLY REJECTION RATIO

PSRR was measured by placing a 1V AC signal on the power supply. PSRR is equal to the ratio of the AC signal at the output node to the AC signal on V_{DD}.

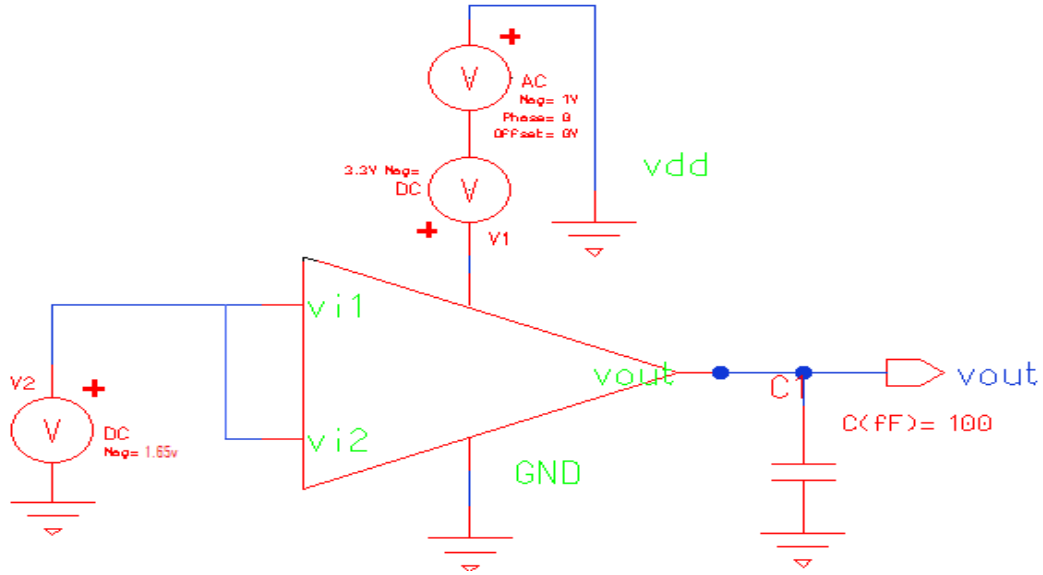


Fig 4.11 Schematic for the simulation of positive PSRR

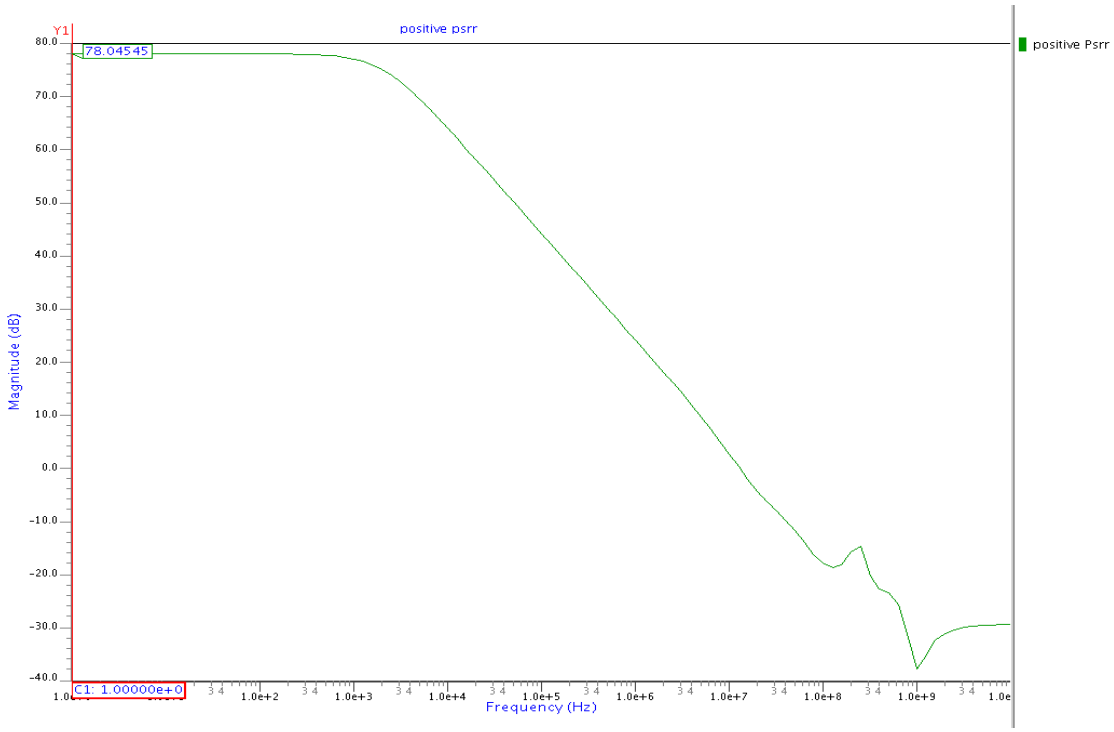


Fig 4.12 Simulation Result of positive Power Supply Rejection Ratio

At low frequencies a result of 78.045 dB was measured.

The test setup shown below is for negative PSRR in this method we apply only common mode dc potential to the input transistors and a 1V AC signal is inserted between ground and the op-amp. The gain obtained from this should be subtracted from differential gain A_D (dB), and then the plot we get is the PSRR plot.

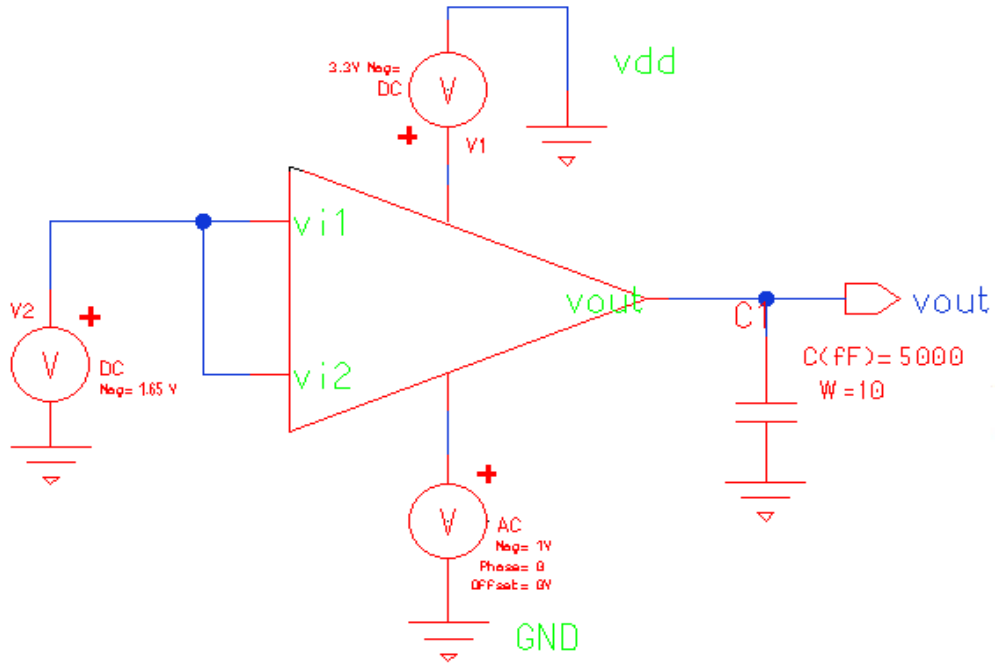


Fig 4.13 Schematic for the Simulation of Negative PSRR

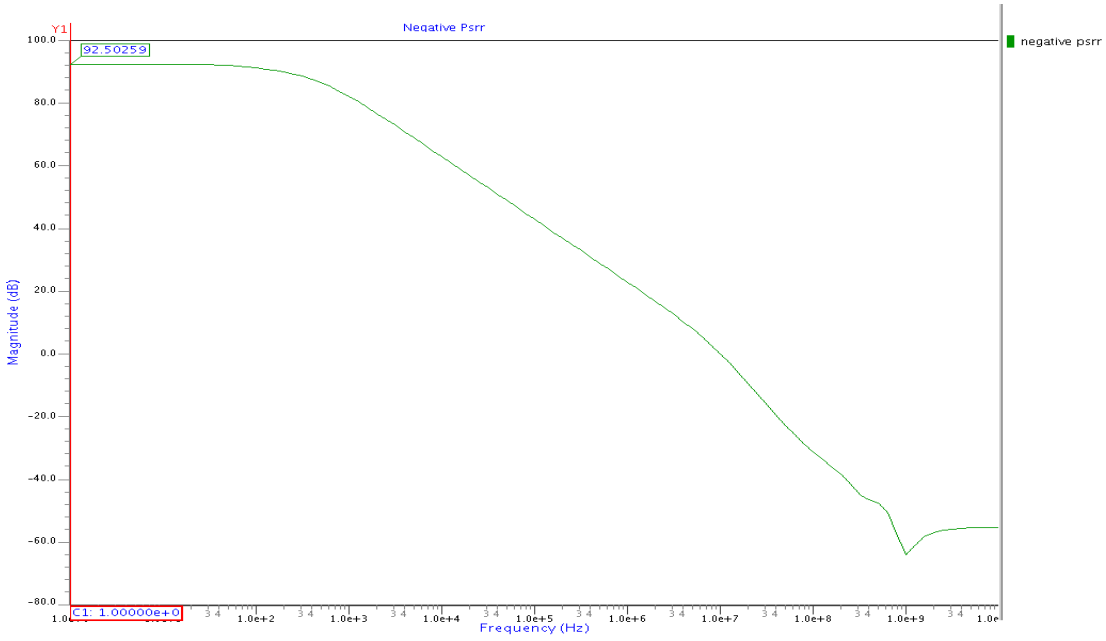


Fig 4.14 Simulation Result of Negative Power Supply Rejection Ratio

At low frequency a result of 92.50 dB was measured.

4.1.7 INPUT COMMON MODE RANGE

Fig 4.15 shows the setup of simulating ICMR op amp is in unity gain configuration and at non-inverting terminal dc voltage sweep from 0 to 3.3 is applied. As shown in Fig 4.16 at 0 V input voltage, output value is 0V and at 3.3V input voltages, output value is 3.3V.

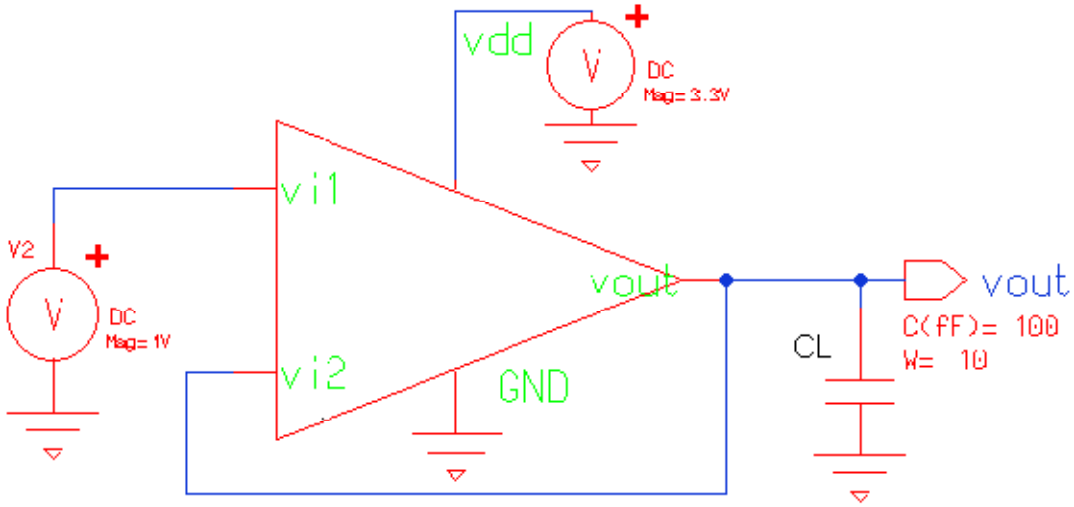


Fig 4.15 Schematic for the Simulation of Input Common-Mode Range

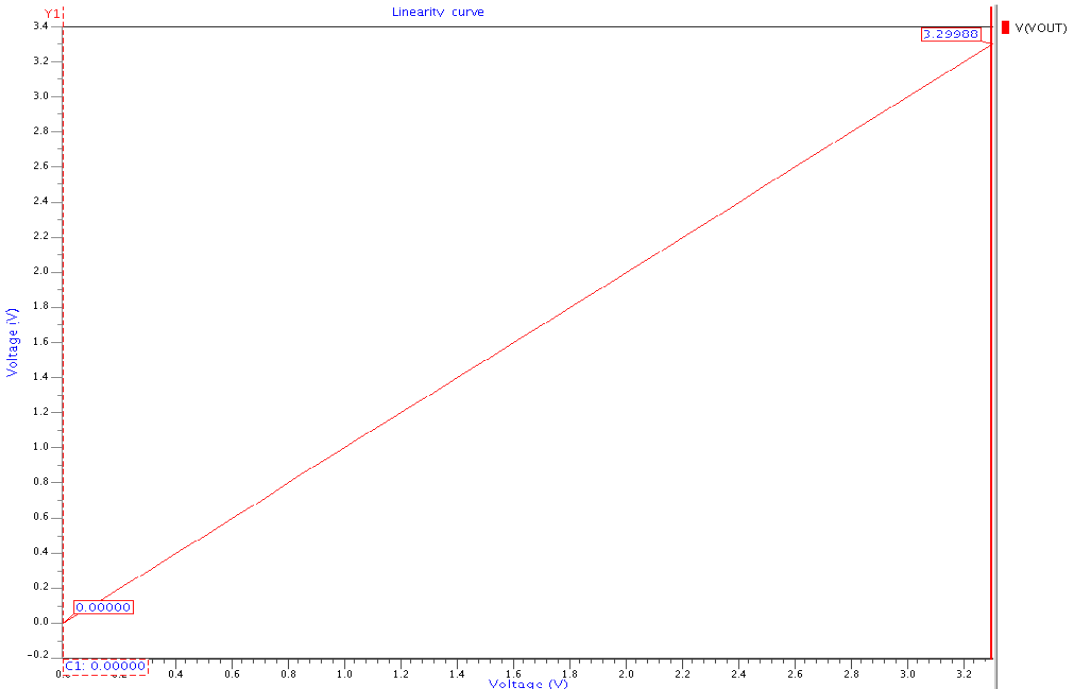


Fig 4.16 Simulation Result of Input Common-Mode Range

4.1.8 EFFECT OF COMMON MODE VARIATION ON THE DC GAIN

The amplitude and the phase are heavily dependent upon the applied common-mode input voltage V_{cm}. In contrast, Fig. 4.17 shows the frequency responses of the op-amp for the common-mode input voltage varying from rail to rail by a step of 0.1 V. The amplitudes and the phases of the proposed op-amp are almost independent of the applied.

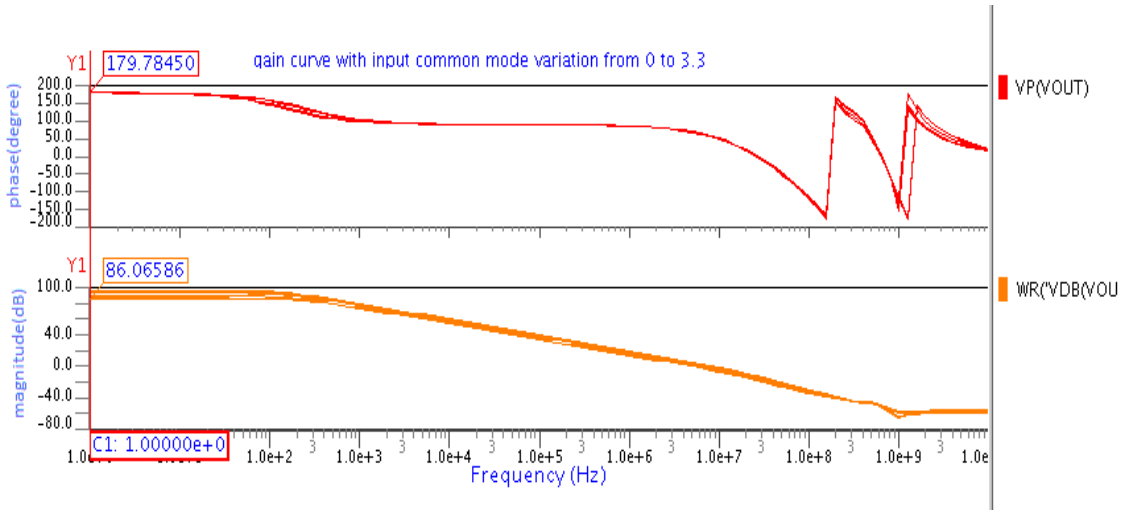


Fig 4.17 Frequency Response of Op-Amp for the Input Common –Mode Input varies from Rail-To-Rail by a step of 0.1 V

4.1.9 VARIATION OF FREQUENCY RESPONSE WITH LOAD CAPACITANCE

Fig 4.18-4.20 shows the effect of variation of load capacitance (1pF, 5pF, 10pF) on the frequency response of the op amp.

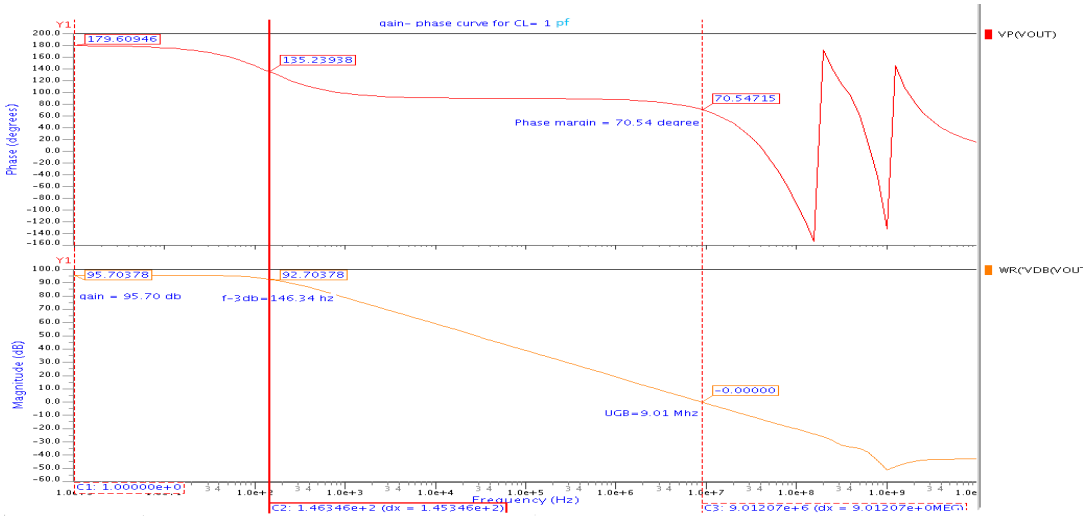


Fig 4.18 Frequency Response at load capacitance 1pF

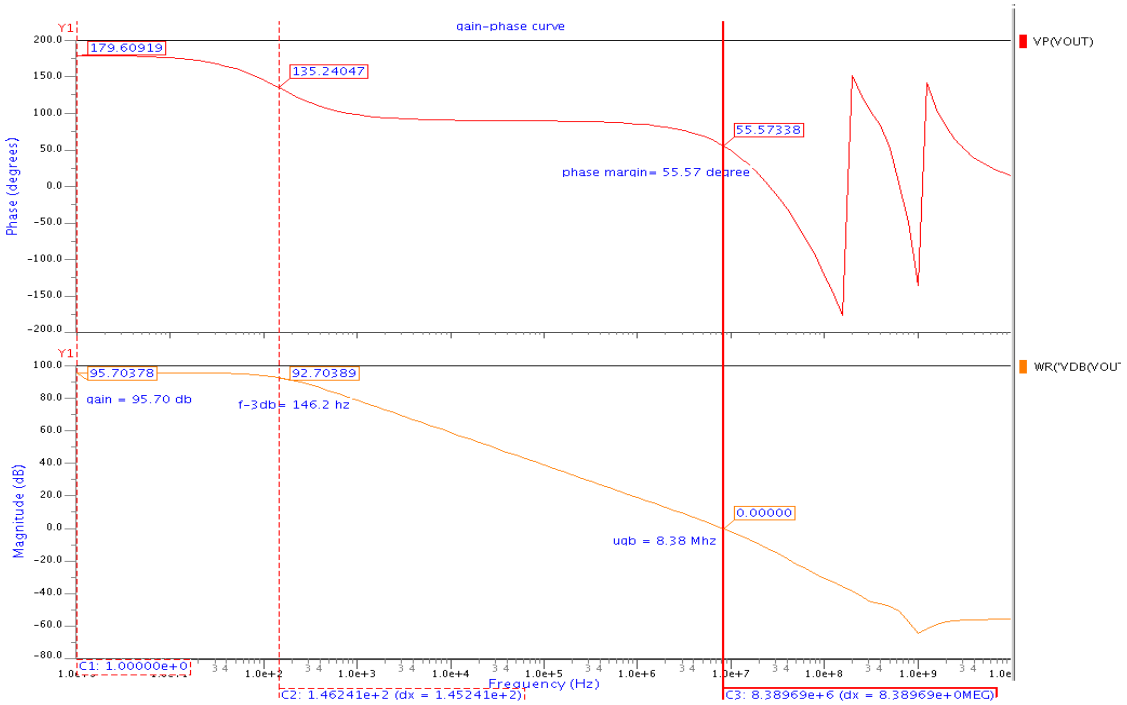


Fig 4.19 Frequency Response at Load Capacitance 5 pF

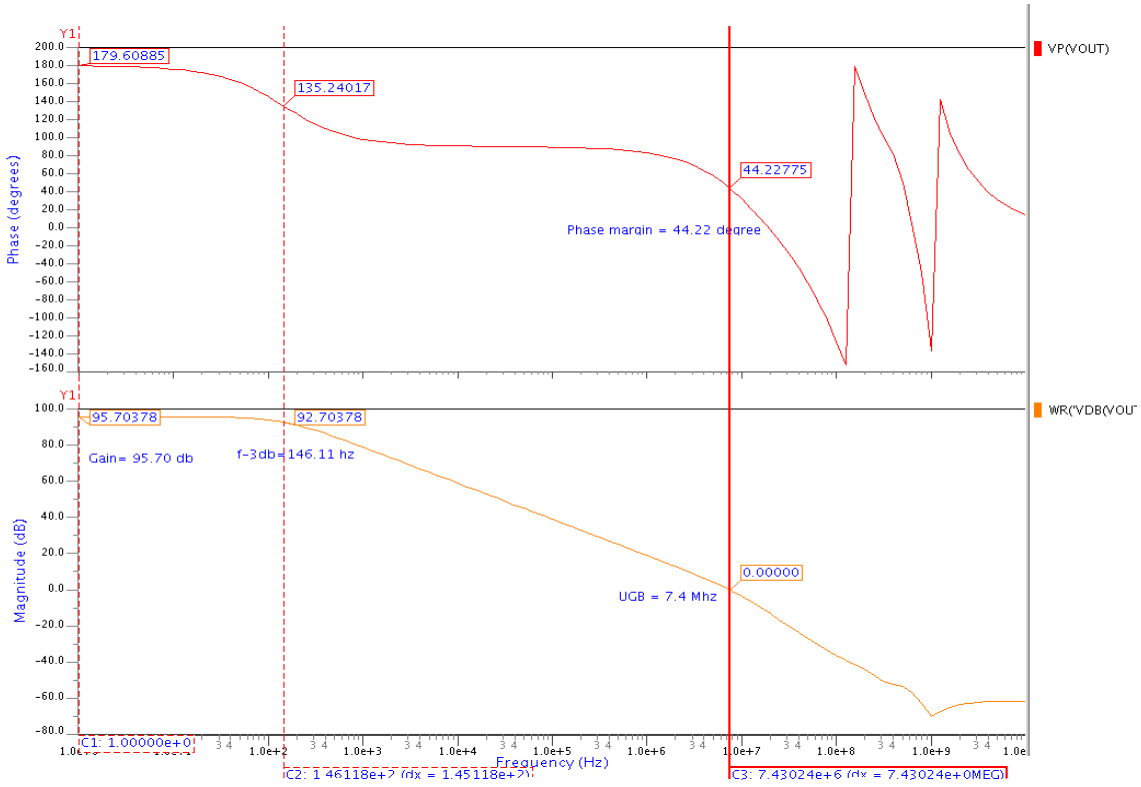


Fig 4.20 Frequency Response at load capacitance 10pF

Table 4.1 Variation of Unity Gain Bandwidth and phase margin with change in the Load Capacitance (CL)

Load capacitance (C_L) (pF)	Unity gain Bandwidth (MHz)	Phase Margin (deg)
1	9.01	70.54
5	8.38	55.57
10	7.40	44.22

Table 4.1 shows there is not very much variation on the UGB and phase margin with the variation in the load capacitance (*CL*) similar is the case with the slew rate it does not change significantly with the variation in load capacitance.

4.1.10 EFFECT OF VARIATION OF COMPENSATION CAPACITANCE

Fig. 4.21 & Fig. 4.22 shows the effect variation of compensation capacitor on the frequency response of op amp. Table 4.2 shows the unity gain bandwidth and phase margin changes with compensation capacitance.

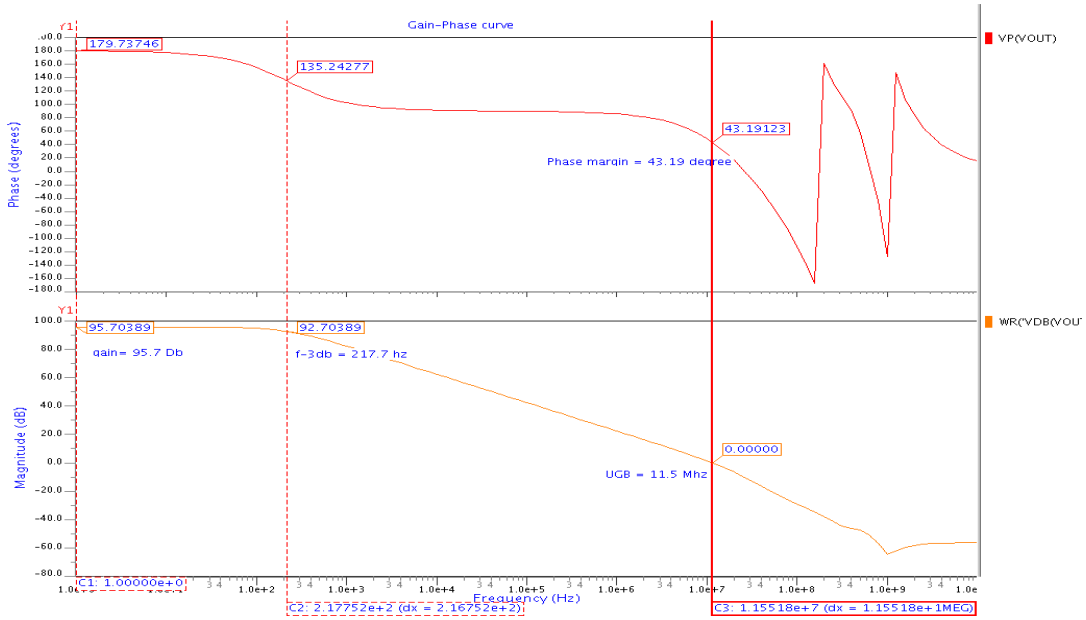


Fig 4.21 Frequency Response with compensation capacitance 400fF

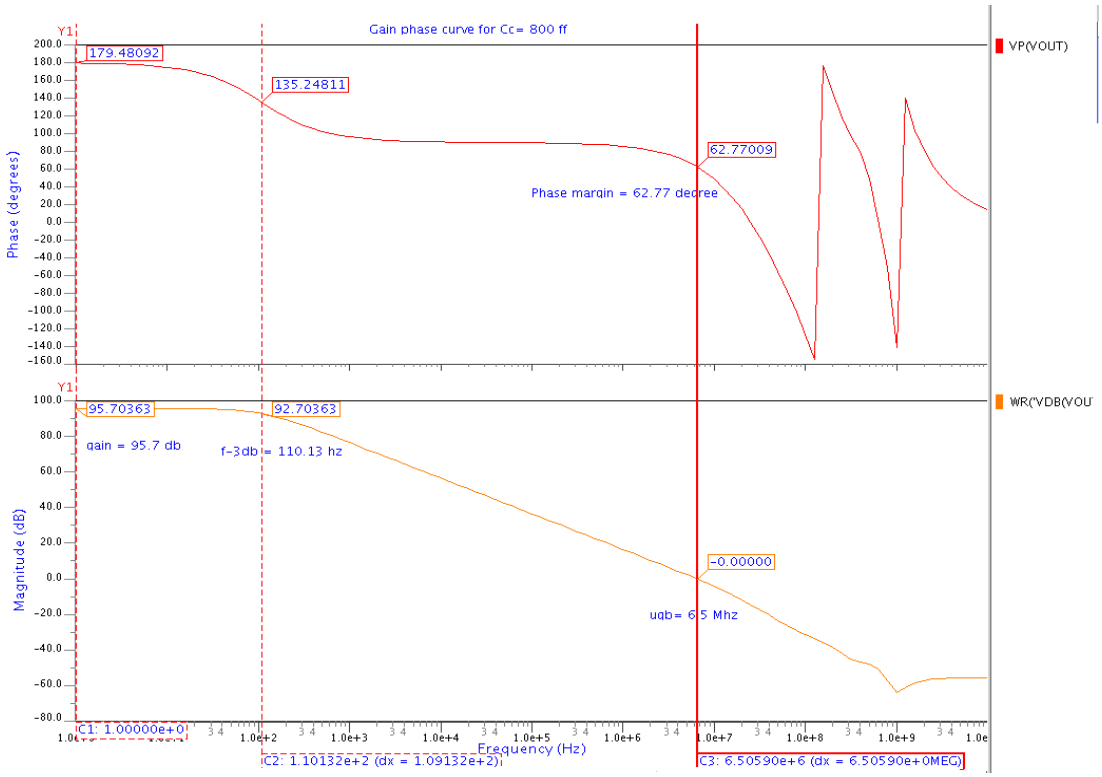


Fig 4.22 Frequency Response with compensation capacitance 800fF

Table 4.2 Variation of Unity Gain Bandwidth and Phase margin with change in the Compensation Capacitance

Coupling Capacitor (Cc) (fF)	**Unity Gain Bandwidth (MHz)**	**Phase Margin (deg)**
400	11.5	43.19
600	8.38	55.57
800	6.50	62.77

4.1.11 EFFECT OF VARIATION OF TEMPERATURE ON AC RESPONSE

Fig 4.23 shows the effect of variation of temperature from -30^{0} to $+130^{0}$ on AC Response. As temperature increase DC gain and UGB decreases.

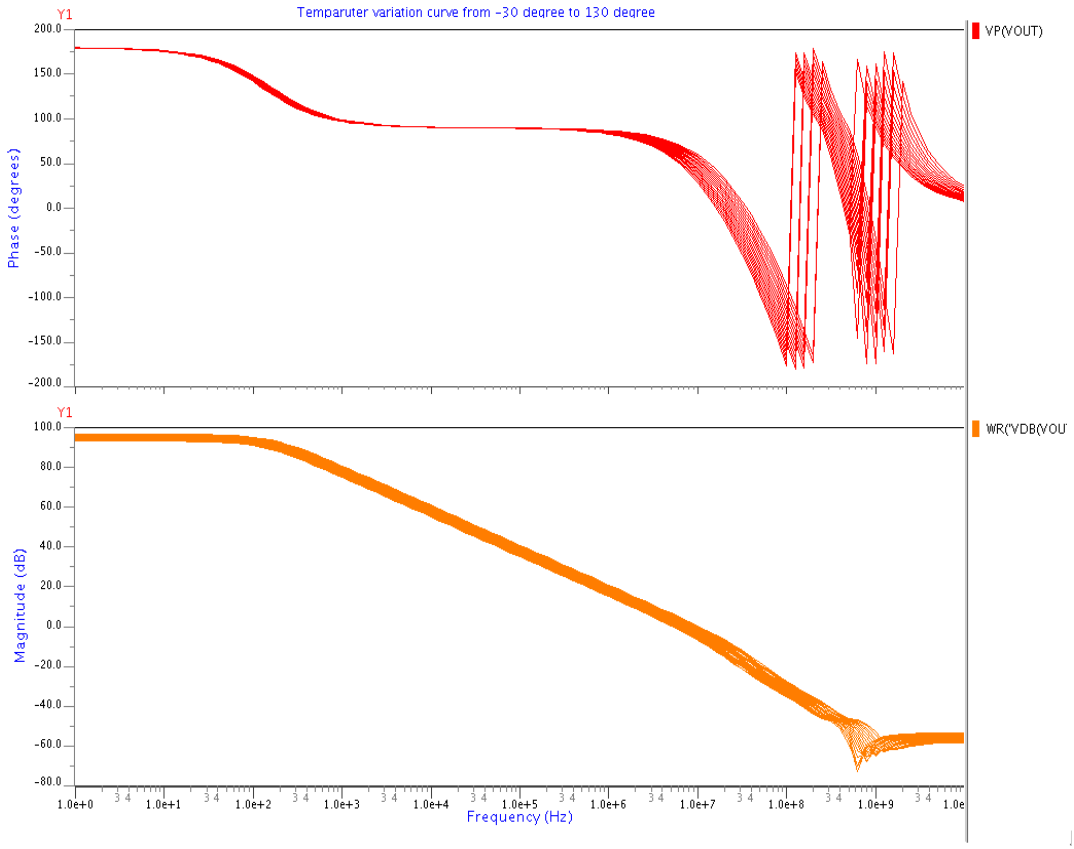


Fig 4.23 Frequency Response variation with Temperature from -30 deg to 130deg

Table 4.3 Simulation Results of Rail-to-Rail Op Amp

Specification Parameter	Target Specification	Simulation Result
Gain(dB)	**> 80**	**95.5**
UGB(MHz)	**8**	**8.38**
Phase Margin(degree)	**60**	**55.57**
Input Stage Swing(v)	**3.30**	**3.30**
Output Stage Swing(v)	**3.30**	**2.95**
Power Consumption(µW)	**200**	**512**
Slew Rate(v/µs)	**2.4**	**2.81**

Settling Time (μs)(10%)	-	**1.46**
CMRR(dB)	-	**101.69**
PSRR+(dB)	-	**78.04**
PSRR –(dB)	-	**92.50**

4.2 LAYOUT, POST LAYOUT AND PROCESS CORNER SIMULATION

4.2.1 LAYOUT

In doing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, everything should be considered simultaneously. In addition to the speed and the area, other equally critical considerations should be taken into account. For example, for amplifier design, good matching in devices is necessary to minimize the offset voltage, and good shielding is required to protect critical nodes from being disturbed. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the amplifiers.

4.2.1.1 Layout Issues

Analog Layout has number of issues which are discussed as follows:

1. Matching Of Devices

Matching of individual devices is of paramount concern in analog circuit design. In fact almost the entire analog layout techniques' are actually methods for improving matching between different devices on a chip. Matching is important because most analog circuit designs use a ratio based design technique (e.g. current mirrors). Some common techniques that help improve device matching are MULTI-GATE FINGER LAYOUT and COMMON-CENTROID LAYOUT.

The device mismatch is due to number factors like local process variation, global lithographic variations, local lithographic variations and process gradients. These factors affect all devices transistors, resistor, capacitors, and therefore similar techniques can be used to match all elements. During fabrication phase mismatch in physical parameters like doping concentration (Na), mobility (μ), oxide thickness (

tox) and layout dimensions (W, L) gives origin to mismatch in electrical parameter like V_T and β and thus mismatch in I_D.

2. Noise

Noise is important in all analog circuits because it limits dynamic range. In general there are two types of noise, random noise and environmental noise. Random noise refers to noise generated by resistors and active devices in an integrated circuit; environmental noise refers to unwanted signals that are generated by humans. Two common examples of environmental noise are switching of digital circuits and 60 Hz 'hum'. In general, random noise is dealt with at the circuit design level. However the are some layout techniques which can help to reduce random noise. MULTI-GATE FINGER LAYOUT reduces the gate resistance of the poly-silicon and the neutral body region, which are both random noise sources. Generous use of SUBSTRATE PLUGS will help to reduce the resistance of the neutral body region, and thus will minimize the noise contributed by this resistance.

Environmental noise is also dealt with at the circuit level. One common design technique used to minimize the effects of environmental noise is to employ a 'fully-differential' circuit design, since environmental noise generally appears as a common-mode signal. However SUBSTRATE PLUGGING is also very useful for reducing 'substrate noise', which is a particularly troublesome form of environmental noise encountered in highly integrated mixed-signal systems and Systems-On-a-Chip (SOC). Substrate noise occurs when a large amount digital circuits are present on a chip.

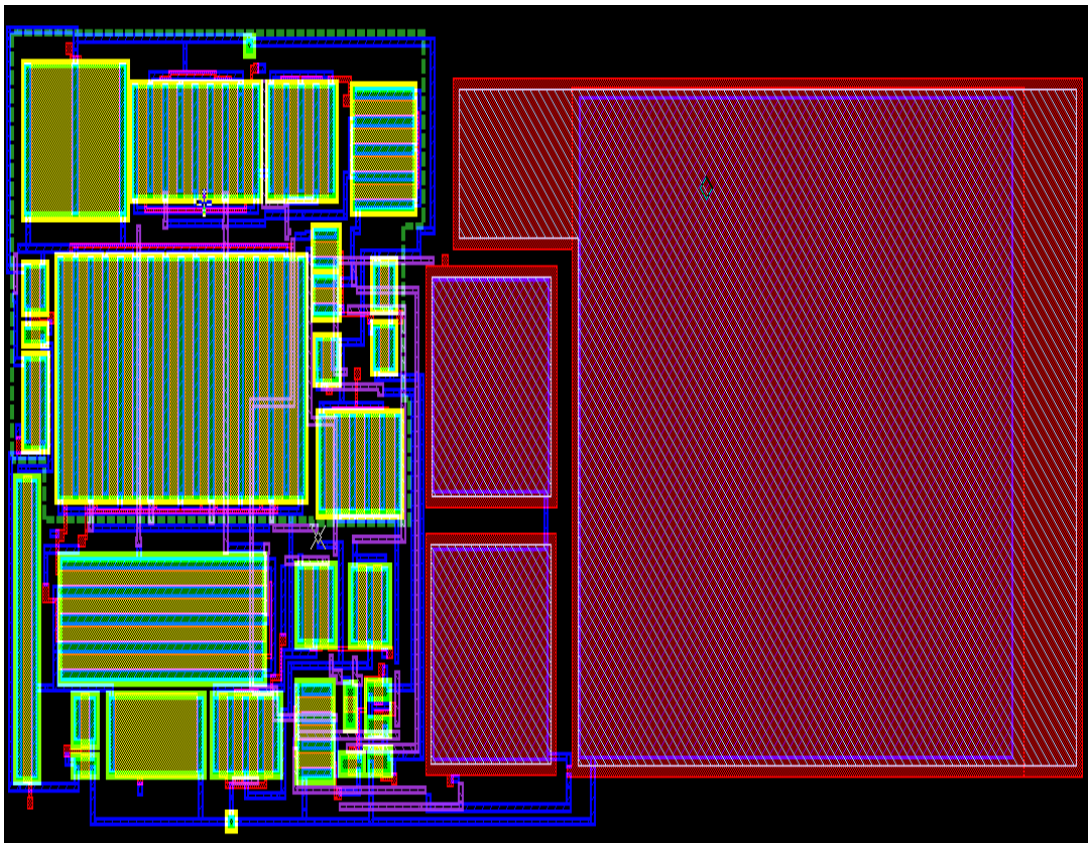


Fig.4.24 layout of complete op-amp with capacitive load

After completing layout LVS have to match with schematic the report of LVS checking is as

```
################################################
                  ##
##
                  ##            C A L I B R E     S Y S T E M
##
                  ##
##
                  ##                      L V S     R E P O R T
##
                  ##
##

################################################
```

```
REPORT FILE NAME:         rail_lay.lvs.report
LAYOUT NAME:              rail_lay.calibre.gds
SOURCE                                                    NAME:
/home/lokesh/rail2rail/rail2rail.src.net ('rail2rail')
RULE FILE:                /home/lokesh/_tsmc035.rules_
LVS MODE:                 Mask
RULE FILE NAME:           /home/lokesh/_tsmc035.rules_
CREATION TIME:            Fri Jun  5 09:38:57 2009
CURRENT DIRECTORY:        /home/lokesh
USER NAME:                lokesh
CALIBRE VERSION:            v2006.2_30.26     Fri Jul  7 22:37:10
PDT 2006


****************************************************************
*******************************************
                              OVERALL COMPARISON RESULTS
****************************************************************
*******************************************


                        #       ###################       _   _
                      #         #                 #       *   *
                   #   #        #     CORRECT     #         |
                    # #         #                 #       \___/
                      #         ###################


---------------------------------------------------------------
-----------------------------------------

INITIAL NUMBERS OF OBJECTS
--------------------------

               Layout    Source         Component Type
               ------    ------         --------------
```

Ports:	11	11		
Nets:	98	27	*	
Instances:	24	16	*	MN (4 pins)
	47	16	*	MP (4 pins)
	3	3		C (2 pins)
Total Inst:	74	35		

NUMBERS OF OBJECTS AFTER TRANSFORMATION

	Layout	Source	Component Type
Ports:	11	11	
Nets:	27	27	
Instances:	16	16	MN (4 pins)
	16	16	MP (4 pins)
	3	3	C (2 pins)
Total Inst:	35	35	

* = Number of objects in layout different from number in source.

****
****
LVS PARAMETERS
****
****

4.2.2 POST LAYOUT SIMULATION

After completing the PEX, Post layout simulations have been done on extracted netlist.

4.2.2.1 AC RESPONSE

Post layout gain curve is shown below.The results show that there is a very small negligible variation in performance of op-amp.

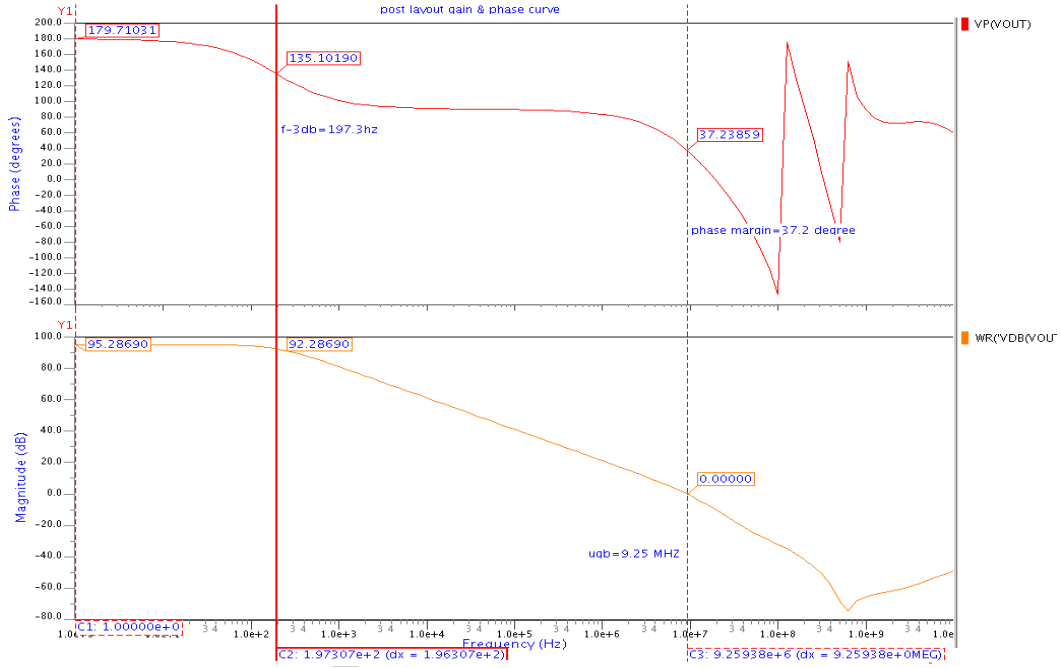


Fig 4.25 Post layout simulation - AC analysis

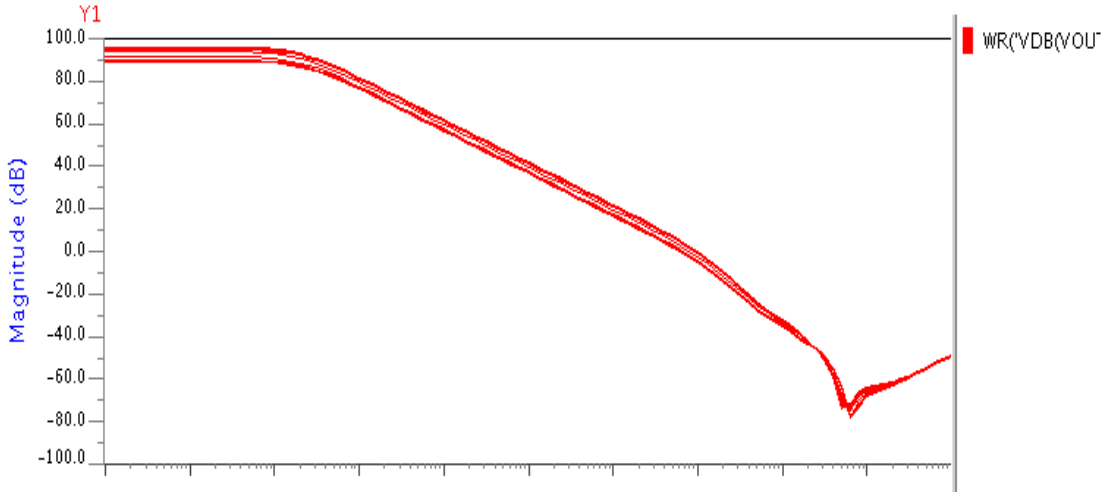


Fig 4.26 Post layout simulation - AC analysis with Common Mode Input Voltage Variation of 0.1 v Step

4.2.3 PROCESS CORNER SIMULATION

Process corner simulation deals with variation in parameter during fabrication. Semiconductor process technology has been continually scaling down for the past four decades and the trend continues. As integrated circuit device geometries shrink and clock speeds increase, the extraction and simulation of parasitic resistance, capacitance and inductance assumes an increasingly important role in physical verification and the production of successful silicon. Closer physical geometries, faster clock and signal net switching speeds, and longer, thinner interconnect lines can lead to increased parasitic capacitance, resistance and inductance values .These parasitics can significantly degrade logic levels, delay clock and signal speeds, as well as chip performance and yield. One naming convention for process corners is to use two-letter designators, where the first letter refers to the NMOS corner, and the second letter refers to the PMOS corner. For example, the FS corner designates fast NFETs and slow PFETs. There are therefore five possible corners: typical-typical (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The first three corners (TT, FF, SS) are called even corners, because both types of devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. The resulting devices can function at slower or faster clock frequencies, and are often binned as such. The last two corners (FS, SF) are called "skewed" corners, and are cause for concern. This is because one type of FET will switch much faster than the other, and this form of imbalanced switching can cause one edge of the output to have much less slew than the other edge. Simulation has been done on extracted netlist from layout. Another netlist included is the netlist of coupling capacitors in adjacent layers. Due to these parasitic care has to be taken for process corners.

Here in this simulation, process parameter like oxide thickness, mobility and electrical parameter threshold voltage are considered with variations of 10% in each.

For n-MOS to be fast, V_{th} = 0.4941V u_0 = 463.518 t_{ox} = 7.02E-9

For n-MOS to be slow, V_{th} = 0.6039V u_0 = 379.247 t_{ox} = 8.58E-9

For p-MOS to be fast, V_{th} = 0.6126V u_0 = 171.071 t_{ox} = 7.02E-9

For p-MOS to be slow, V_{th} = 0.7487V u_0 = 139.959 t_{ox} = 8.58E-9

4.2.3.1 AC RESPONSE

Fig 4.27 to 4.30 shows process corner, ac analysis of op-amp circuit.

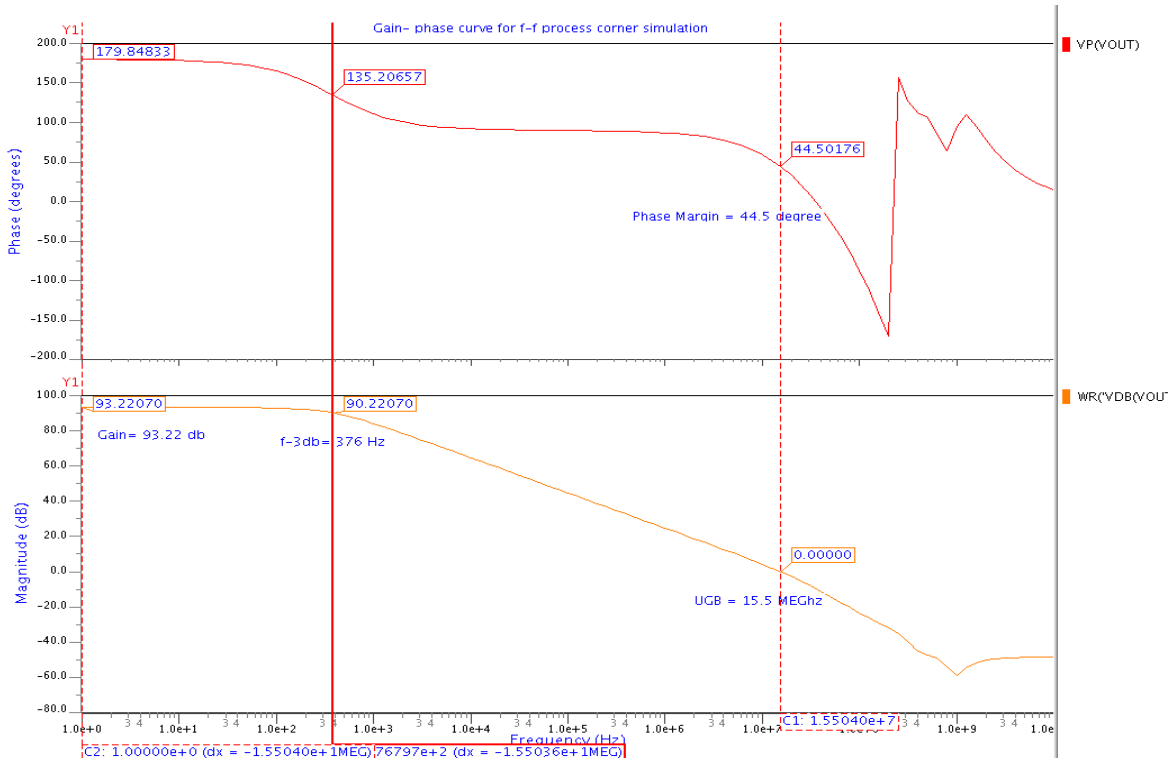


Fig 4.27 Process corner –f-f simulation for AC analysis

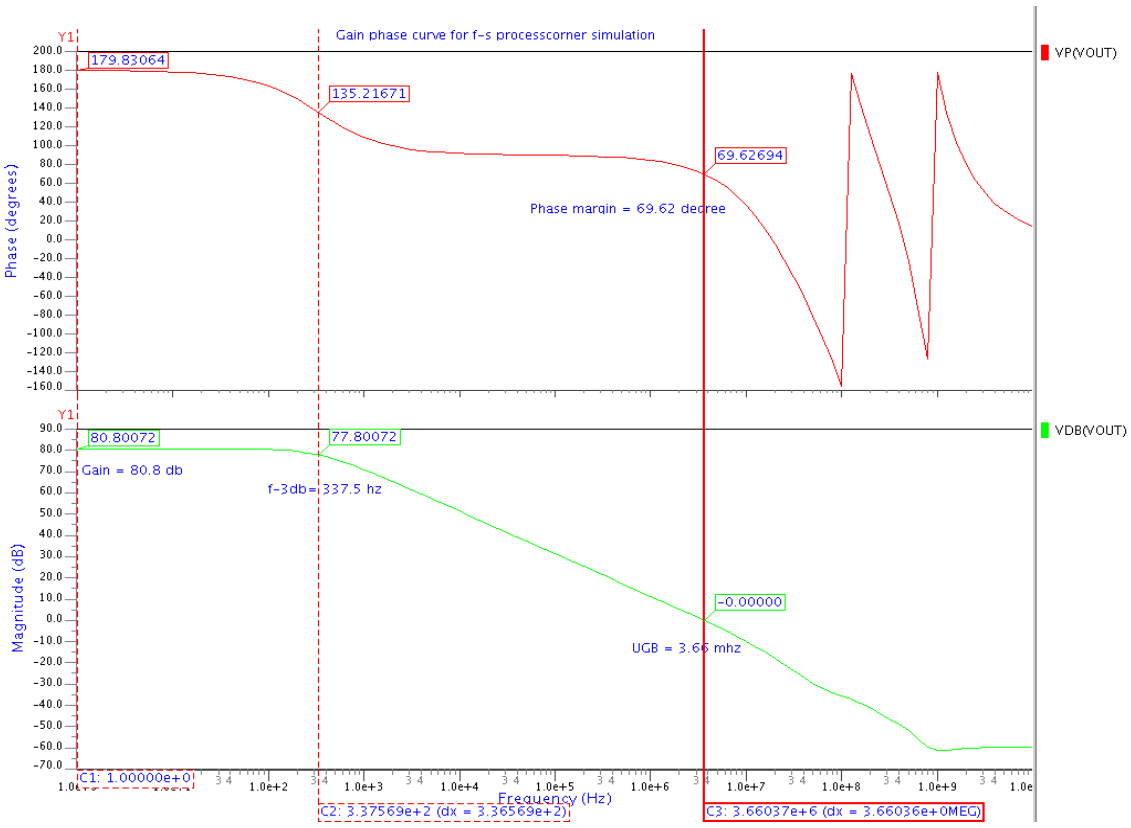


Fig 4.28 Process corner –f-s simulation for AC analysis

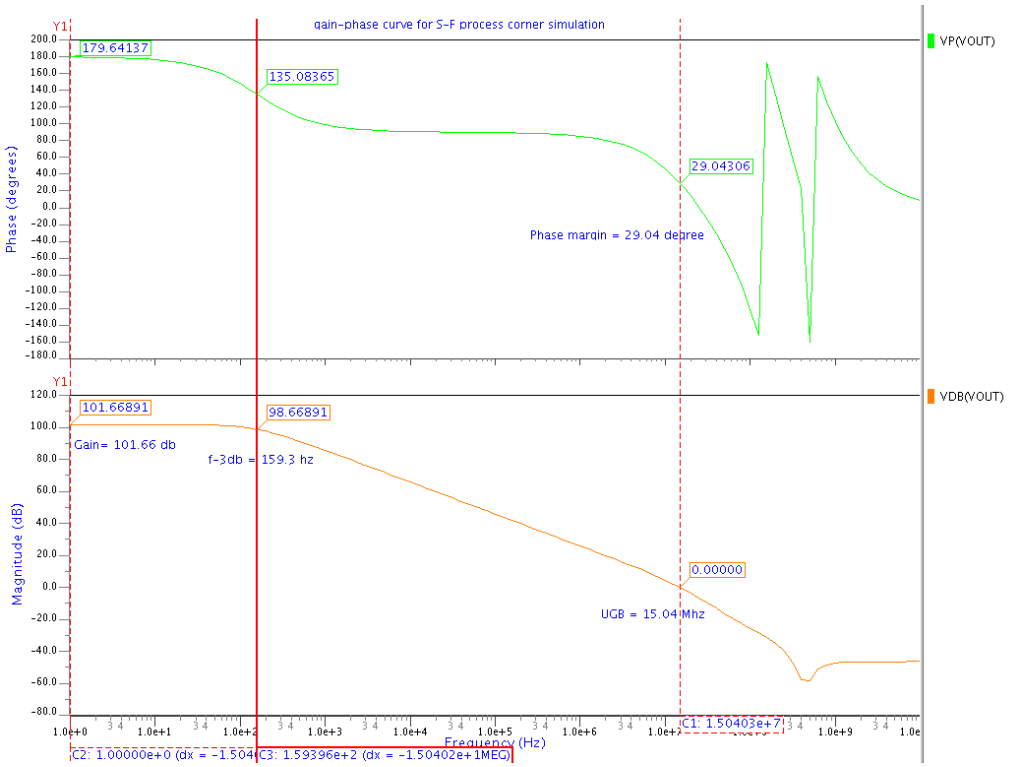


Fig 4.29 Process Corner –s-f simulation for AC analysis

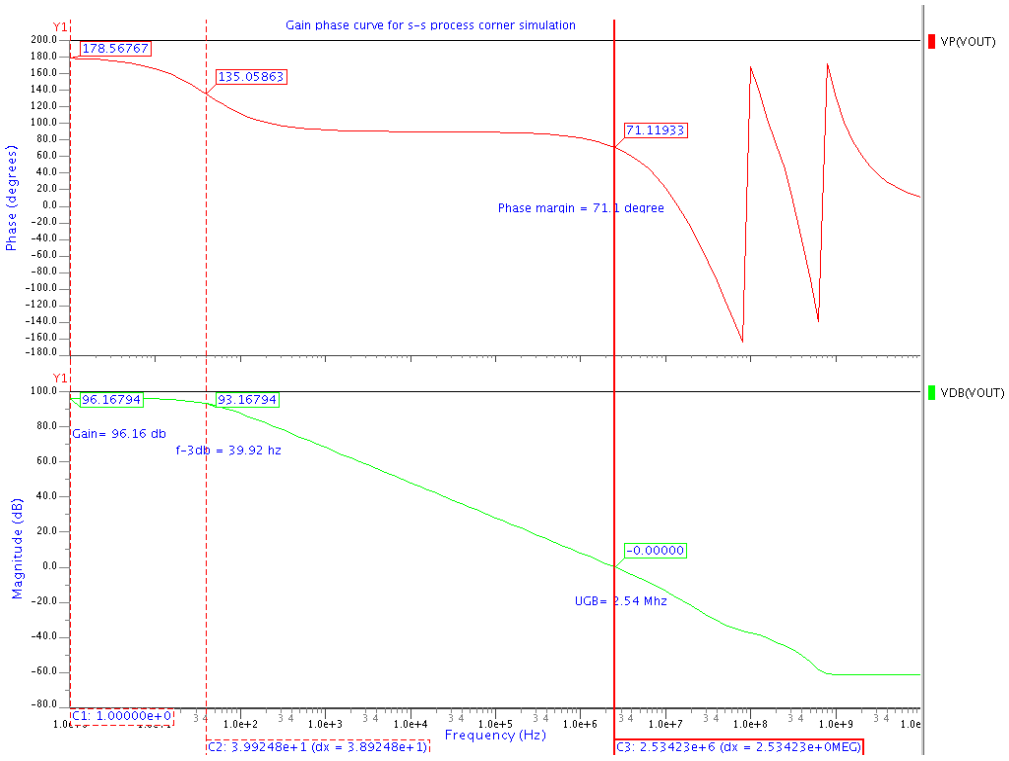


Fig 4.30 Process Corner –s-s simulation for AC analysis

4.2.3.2 COMMON MODE REJECTION RATIO

Fig 4.31 to 4.34 shows process corner, CMRR of op-amp circuit.

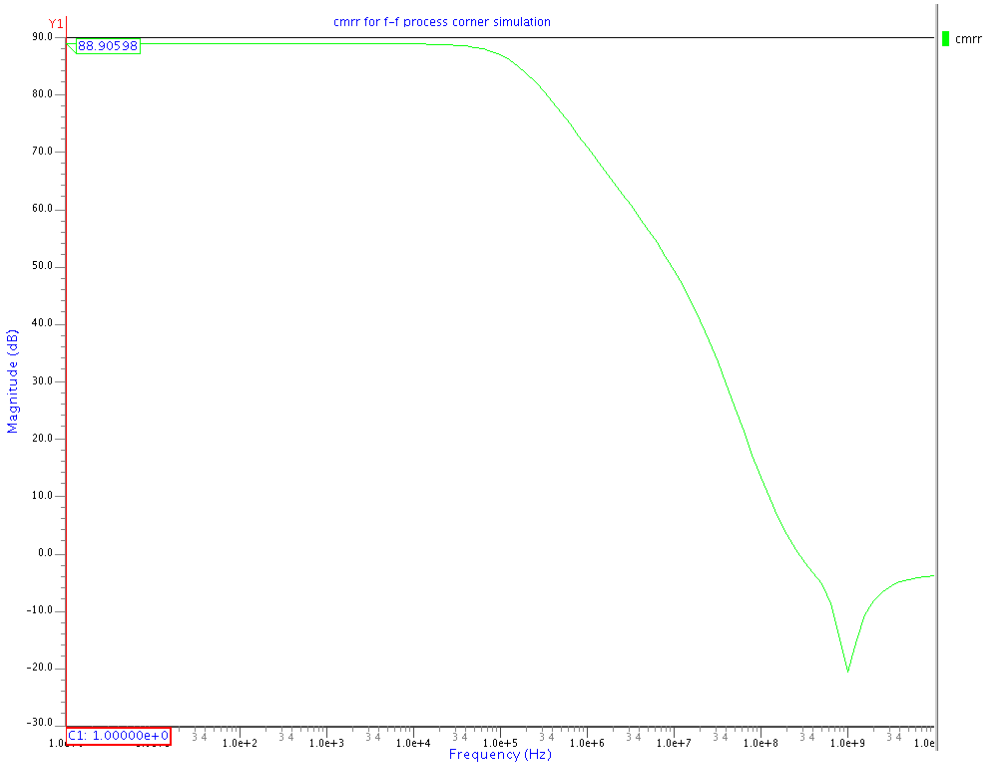


Fig 4.31 Process Corner –f-f simulation for CMRR analysis

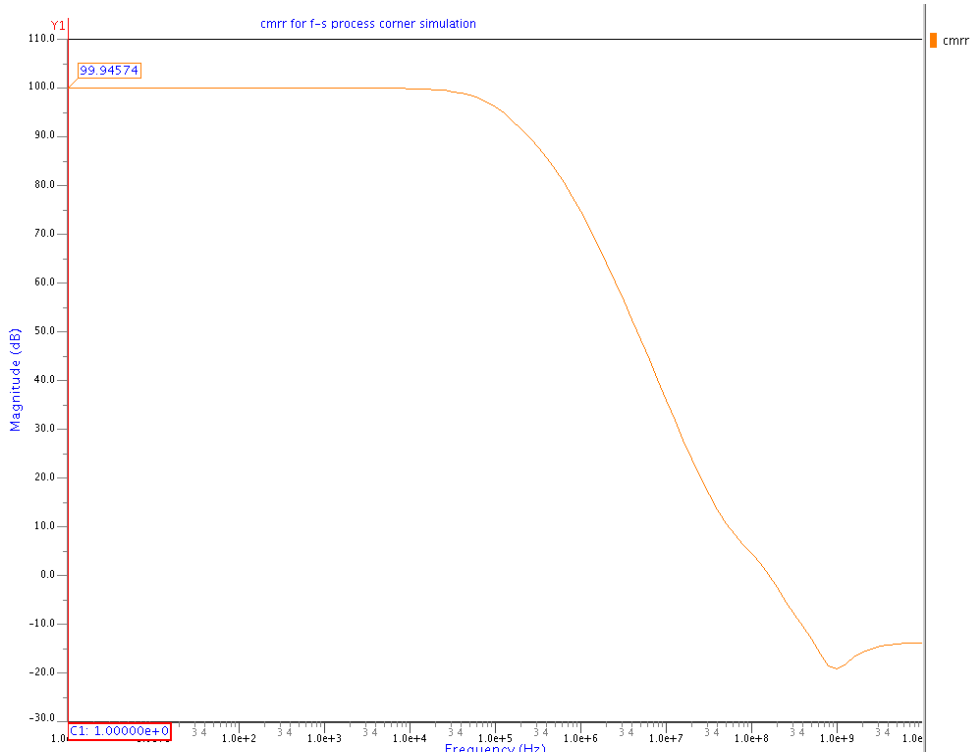


Fig 4.32 Process Corner –f-s Simulation for CMRR Analysis

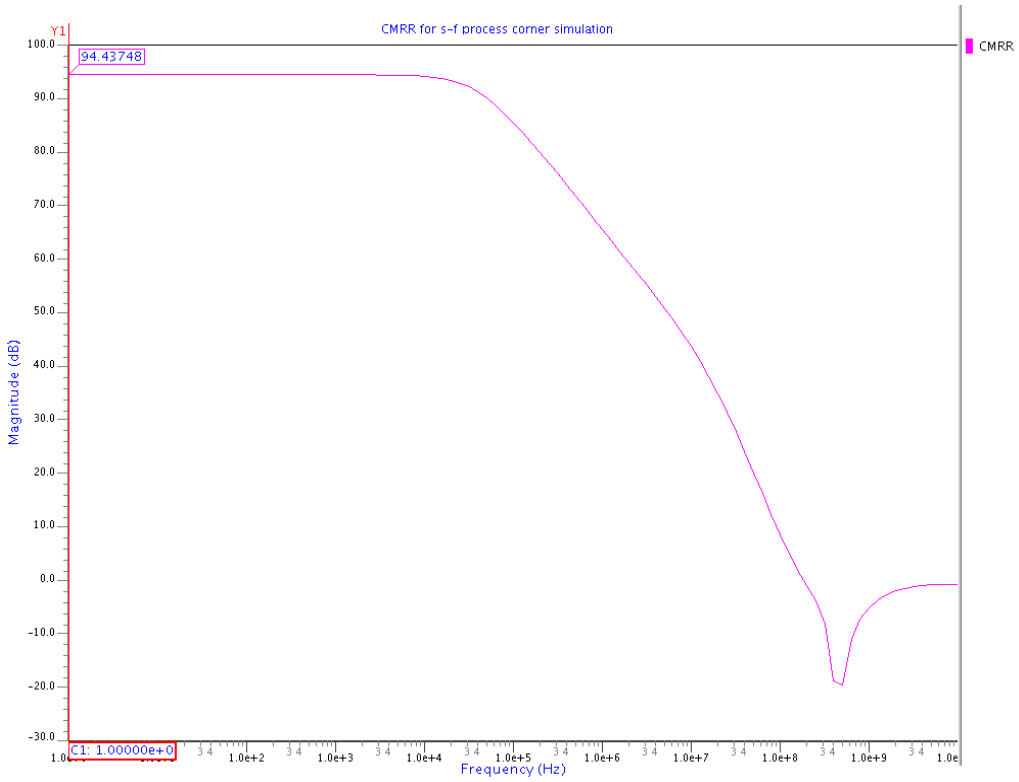


Fig 4.33 Process Corner –s-f simulation for CMRR analysis

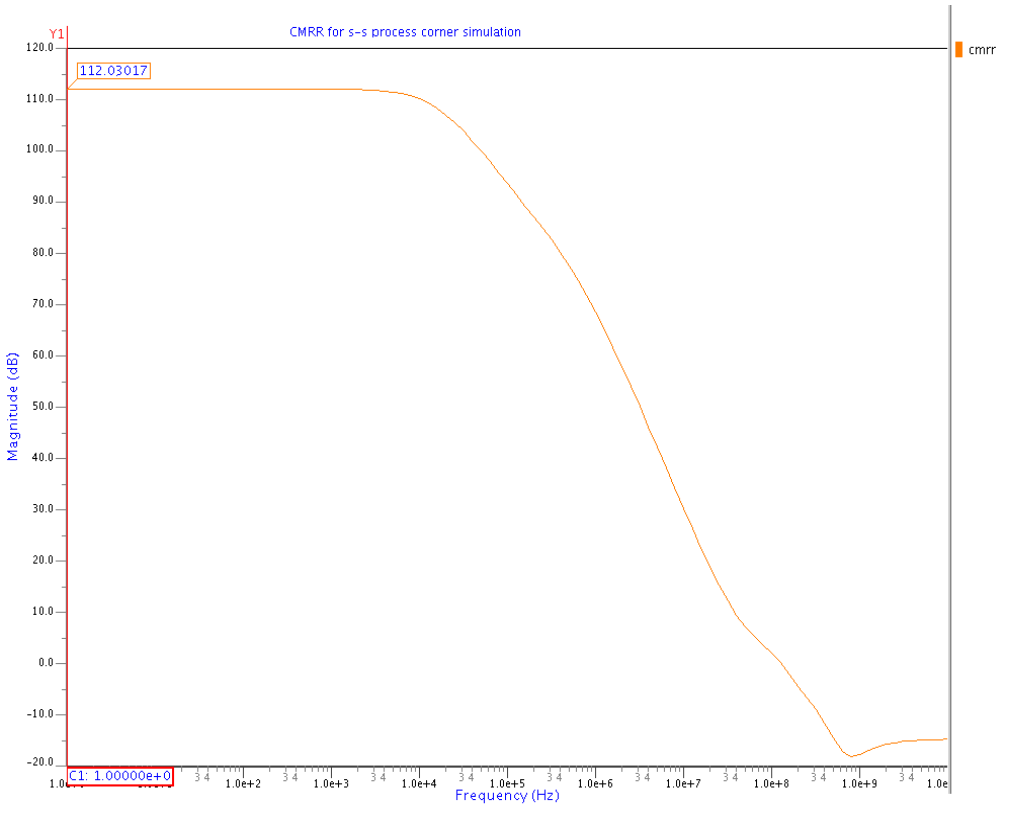


Fig 4.34 Process Corner –s-f simulation for CMRR analysis

4.2.3.3 TRANSIENT RESULTS

Fig 4.35 to 4.38 shows process corner, transient analysis of op-amp circuit.

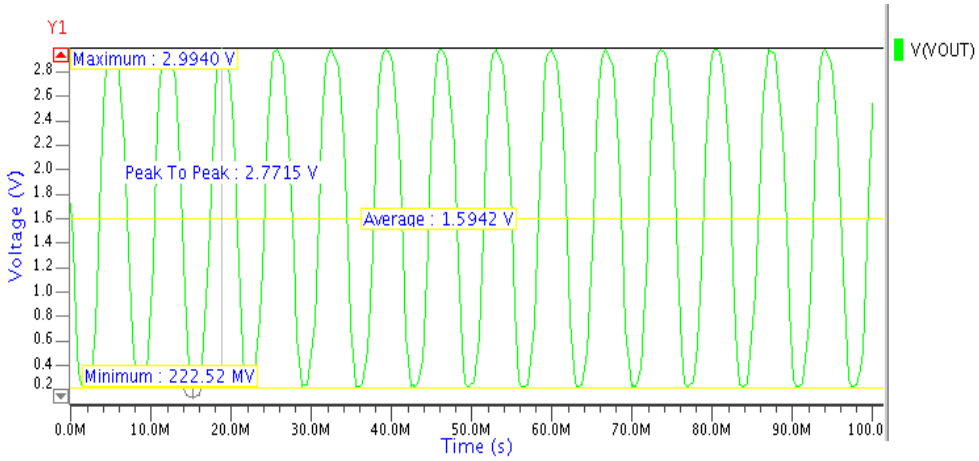


Fig 4.35 Process corner –f-f simulation for transient analysis

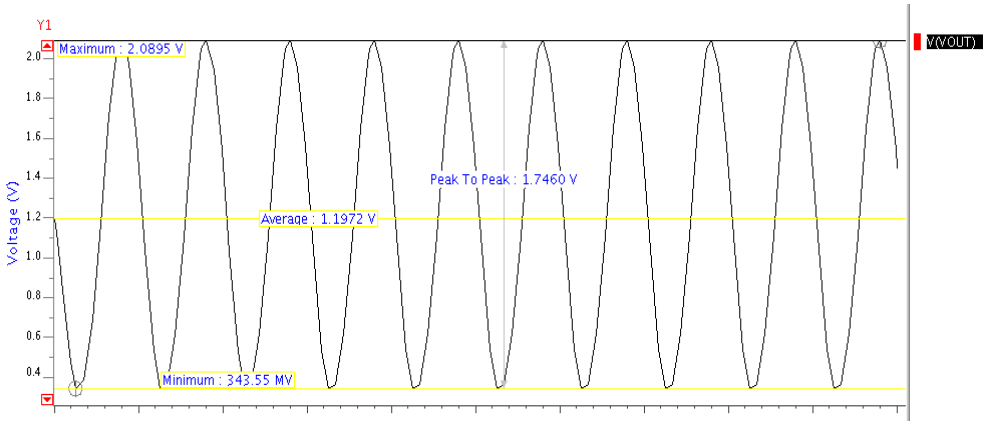


Fig 4.36 Process corner –f-s simulation for transient analysis

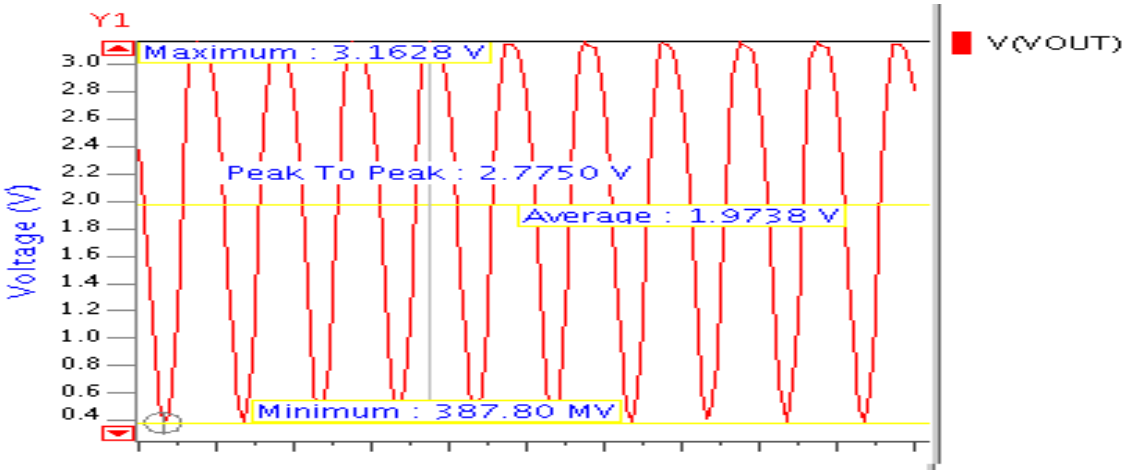


Fig 4.37 Process corner –s-f simulation for transient analysis

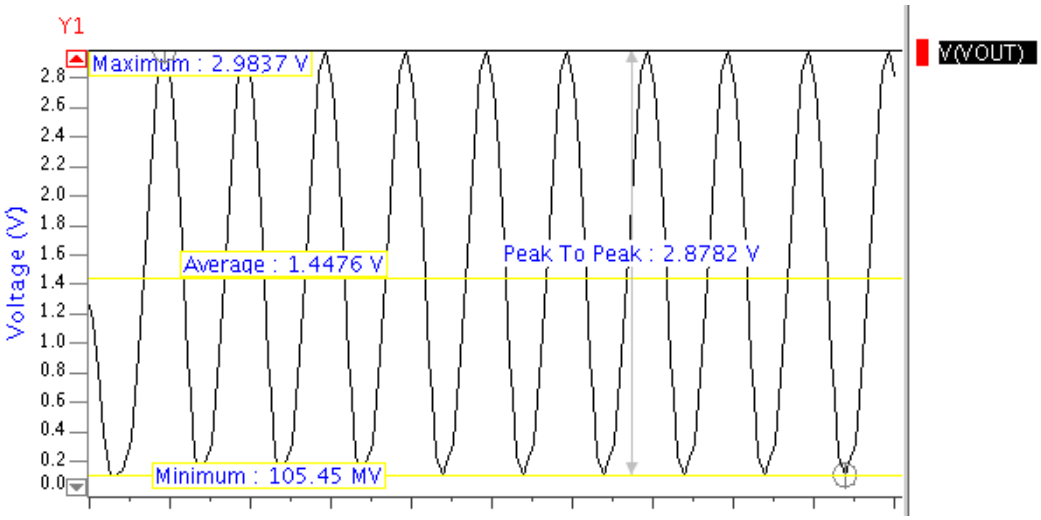


Fig 4.38 Process corner –s-s simulation for transient analysis

4.2.3.4 STEP RESPONSE – SLEW RATE MEASUREMENT

Fig 4.39 to 4.42 shows process corner, transient analysis of op-amp circuit.

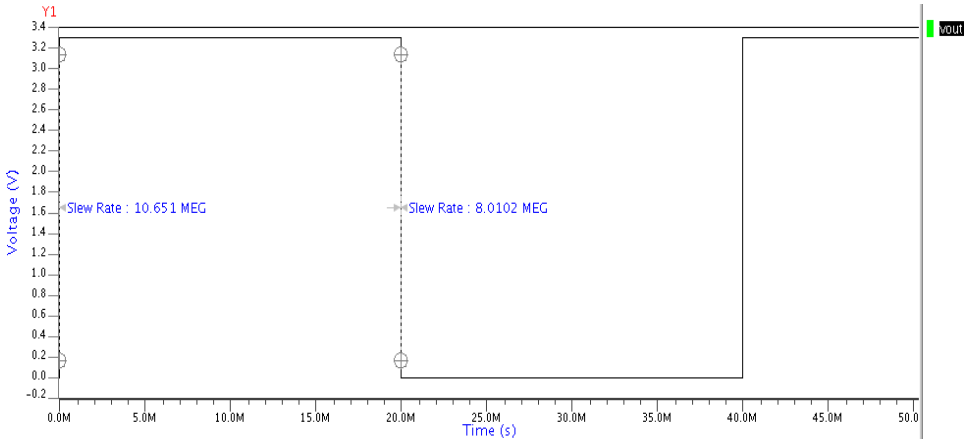


Fig 4.39 Process Corner –f-f simulation for Slew rate analysis

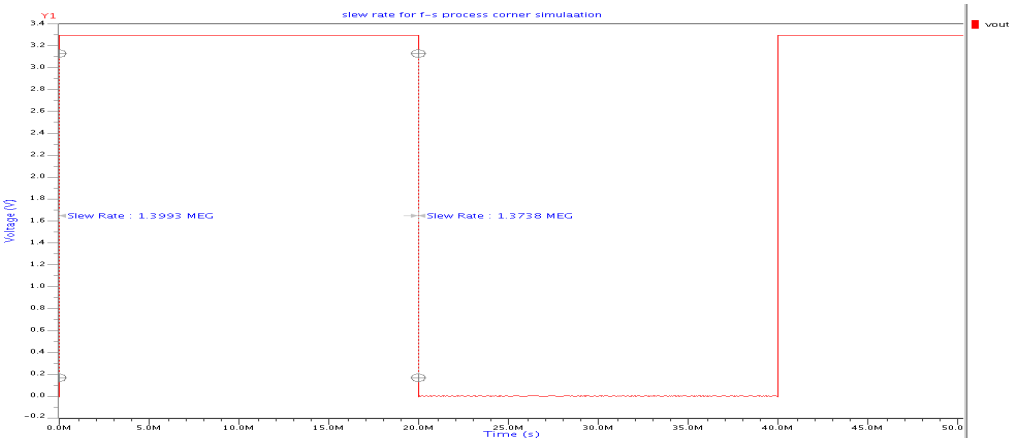


Fig 4.40 Process Corner –f-s simulation for Slew rate analysis

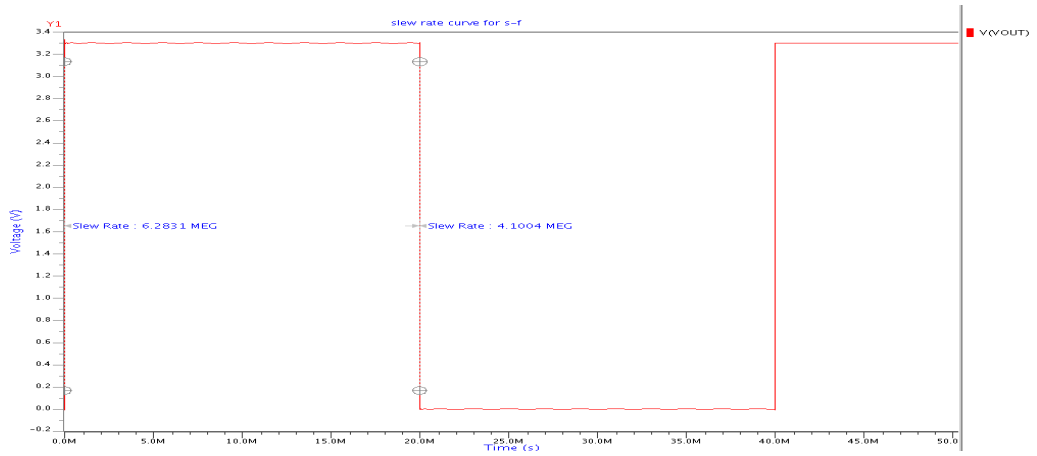


Fig 4.41 Process Corner –s-f simulation for Slew rate analysis

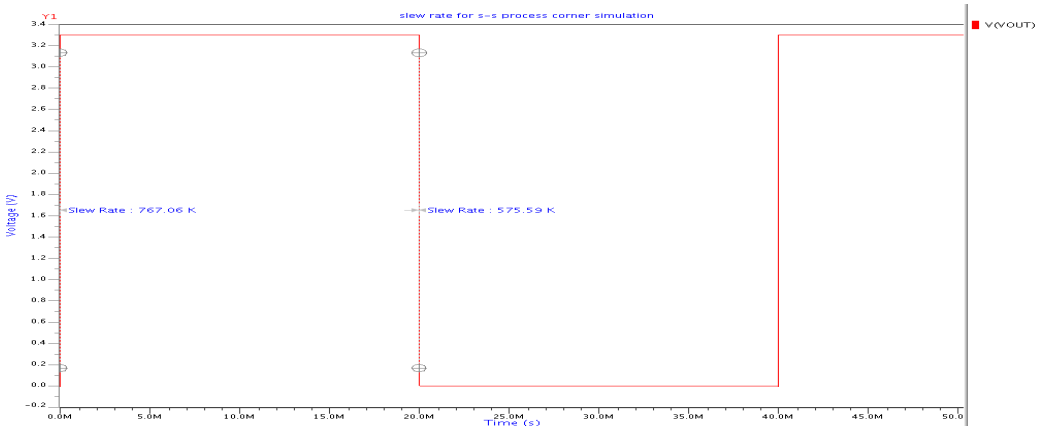


Fig 4.42 Process Corner –s-s simulation for Slew rate Analysis

4.2.3.5 SETTLING TIME

Fig 4.43 to 4.47 shows process corner, settle time analysis of op-amp circuit.

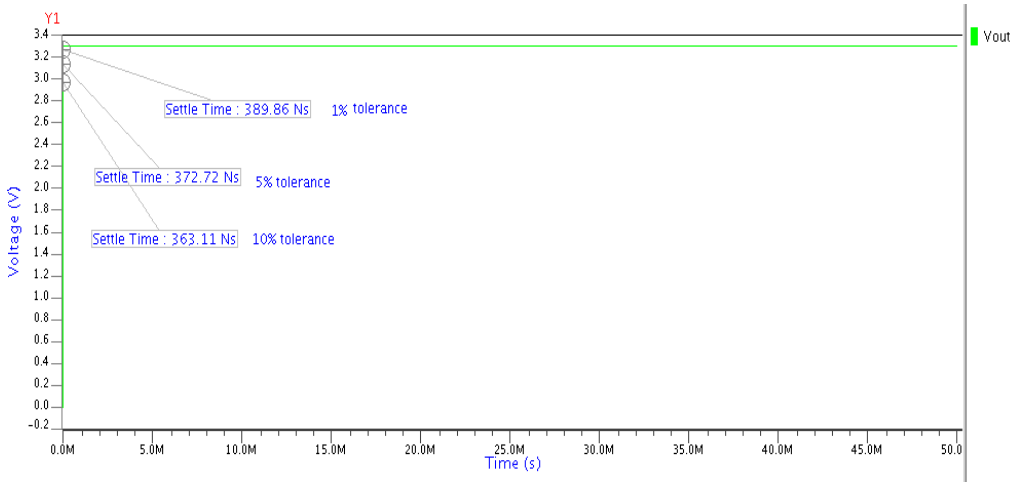


Fig 4.43 Process Corner –f-f simulation for Settle Time Analysis

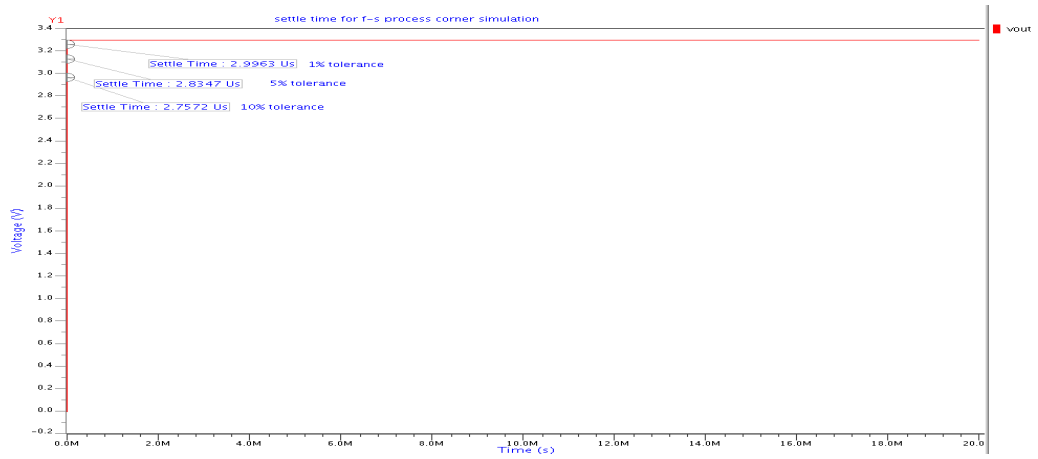


Fig 4.44 Process Corner –f-s simulation for Settle Time analysis

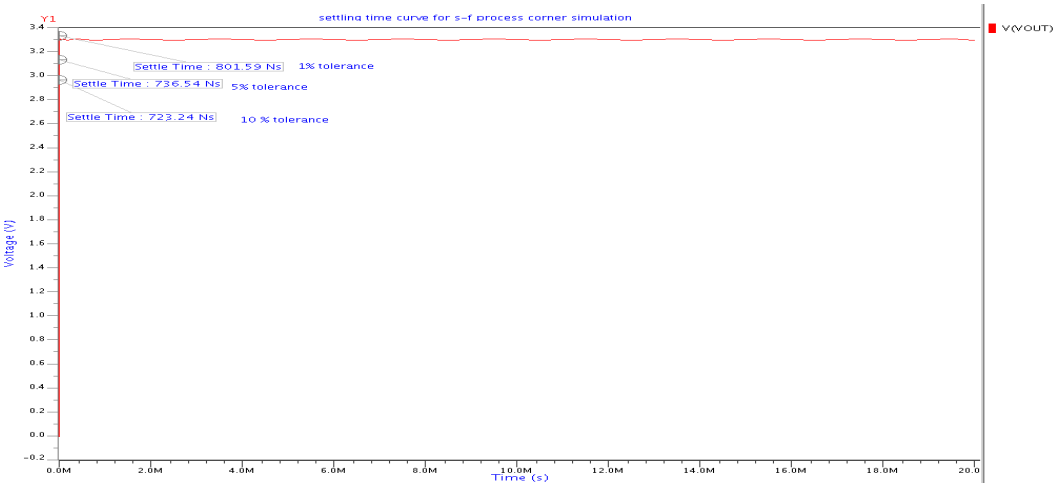


Fig 4.45 Process Corner –s-f simulation for settle time analysis

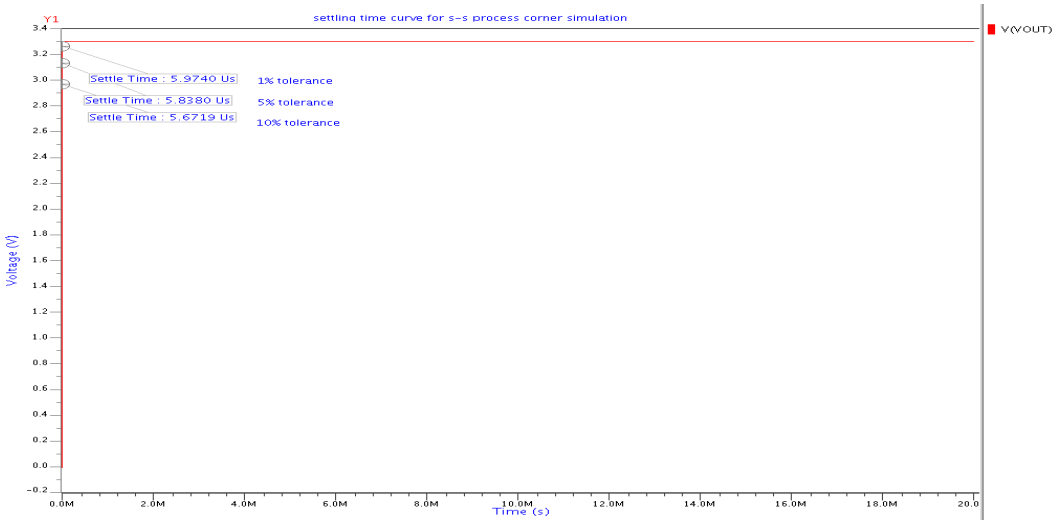
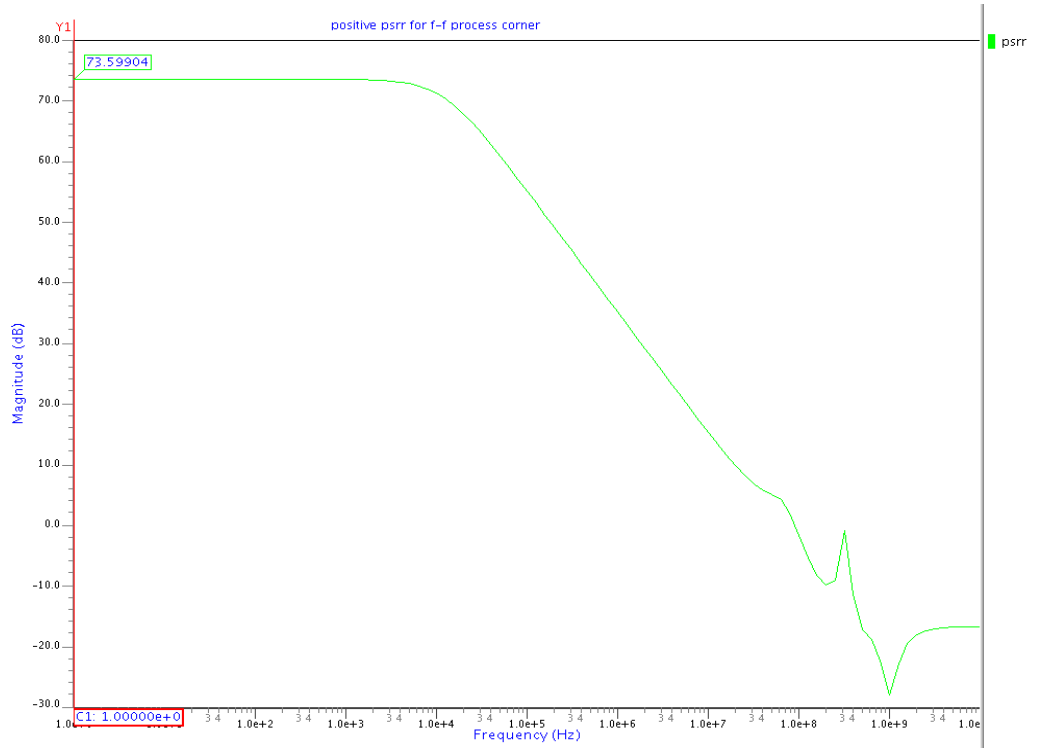


Fig 4.46 Process Corner –s-f simulation for settle time analysis

4.2.3.6 POWER SUPPLY REJECTION RATIO

Fig 4.47 to 4.50 shows process corner, PSRR of op-amp circuit.



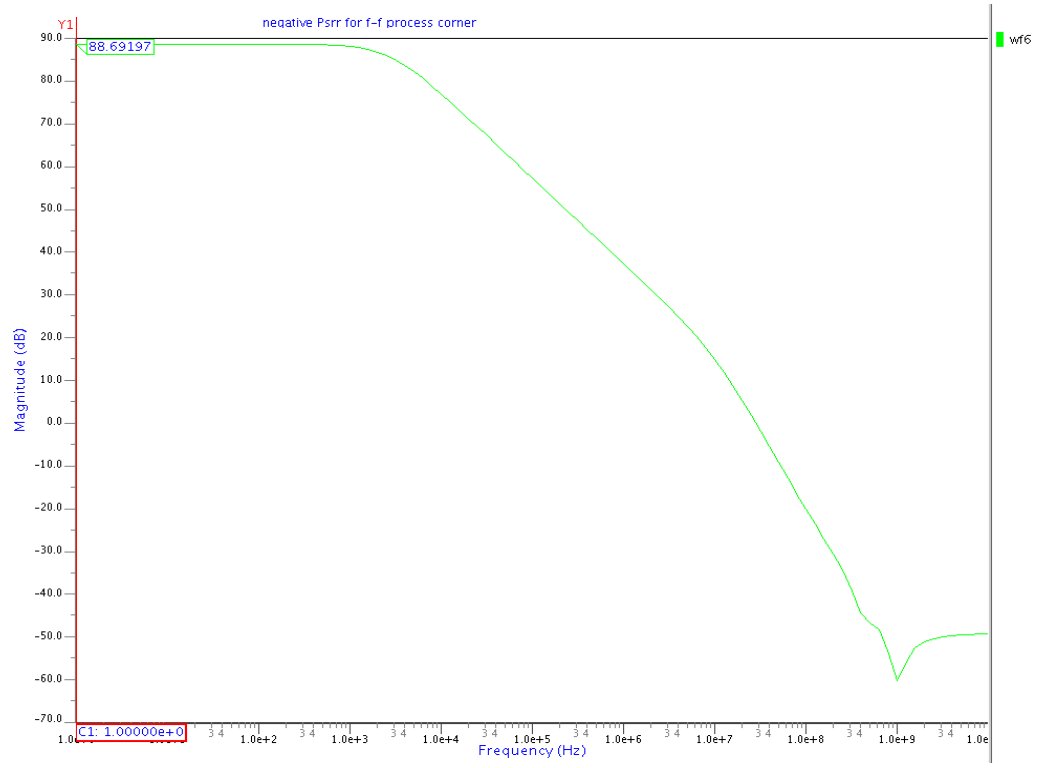


Fig 4.47 Process Corner –f-f simulation for PSRR analysis

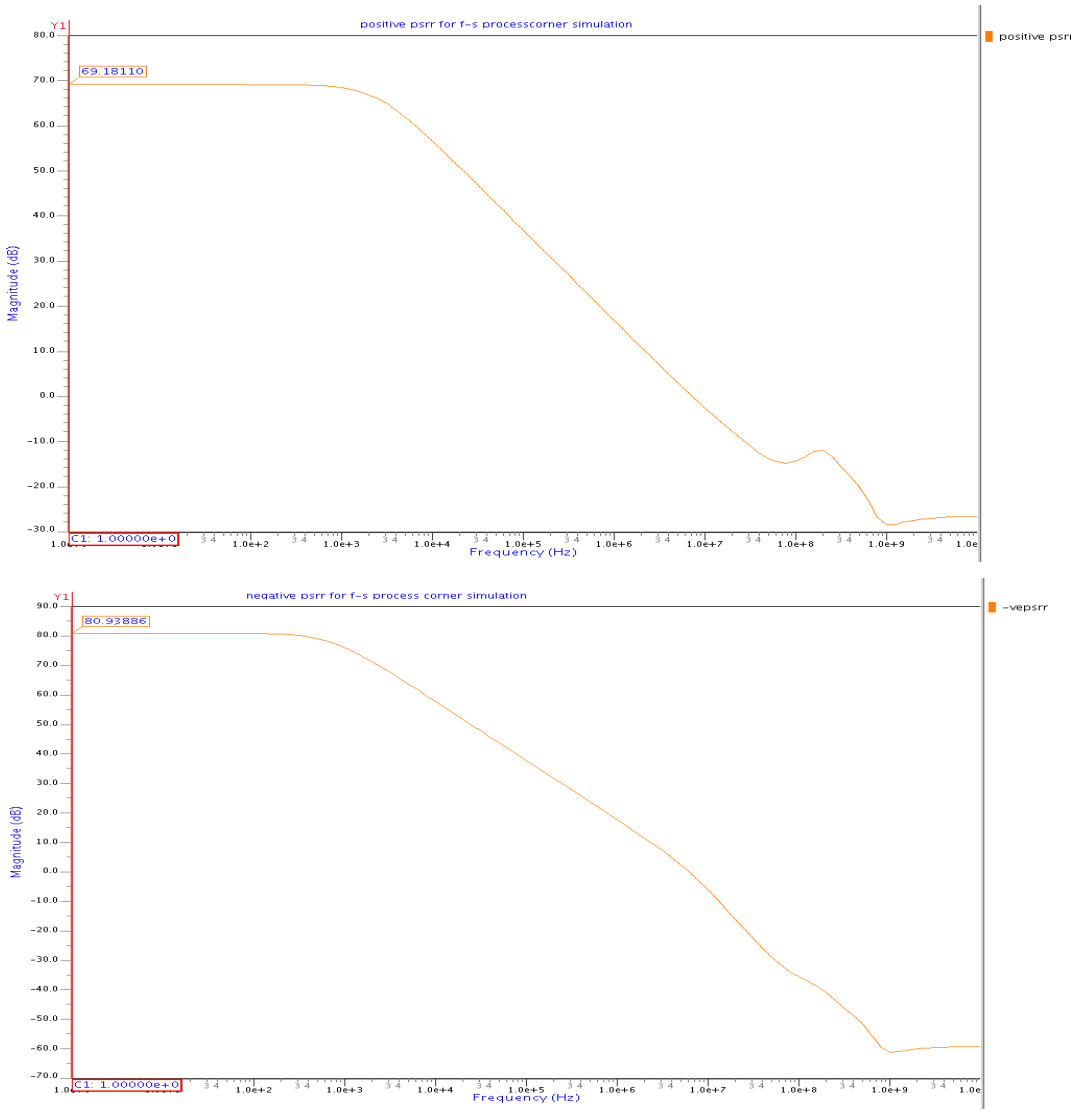
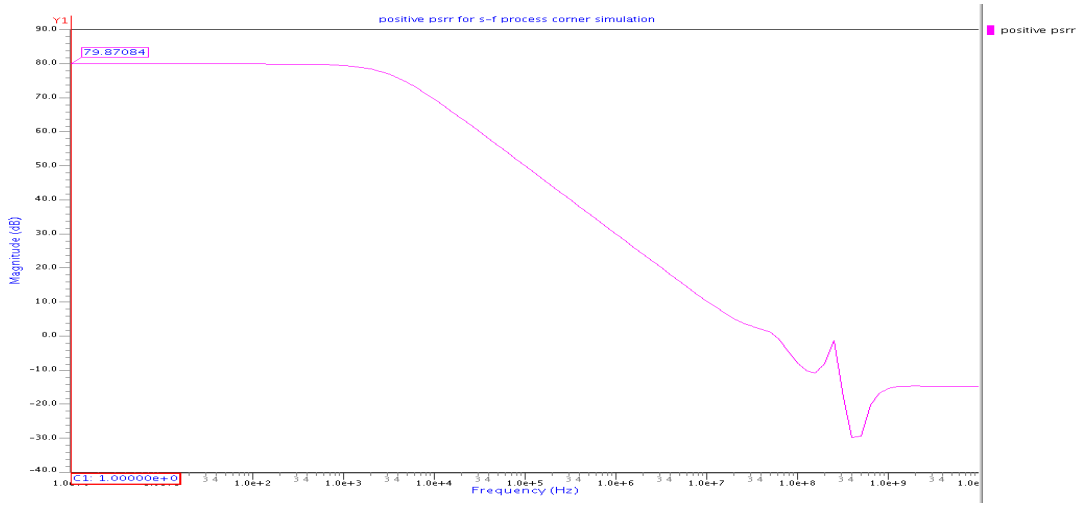


Fig 4.48 Process Corner –f-s simulation for PSRR analysis



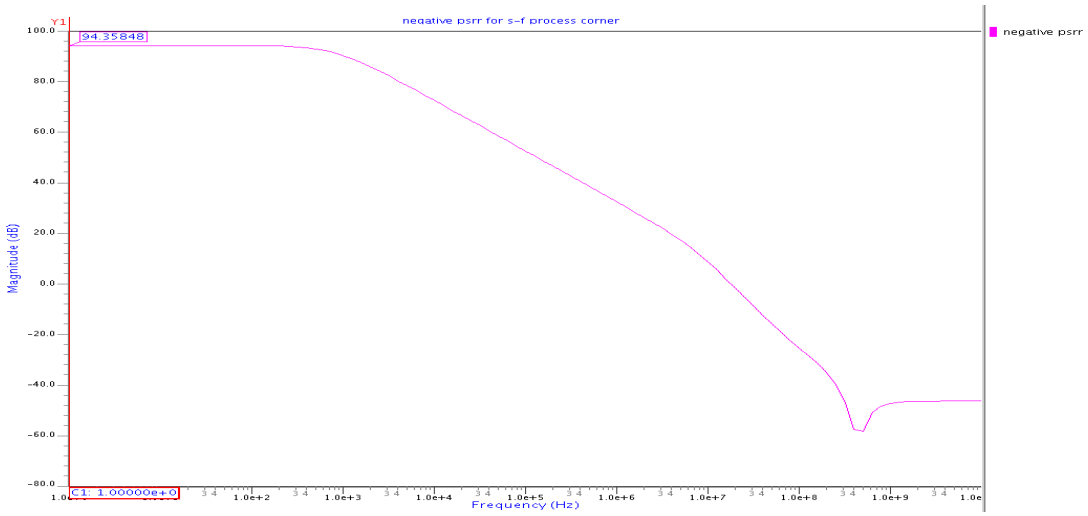


Fig 4.49 Process Corner –s-f simulation for PSRR analysis

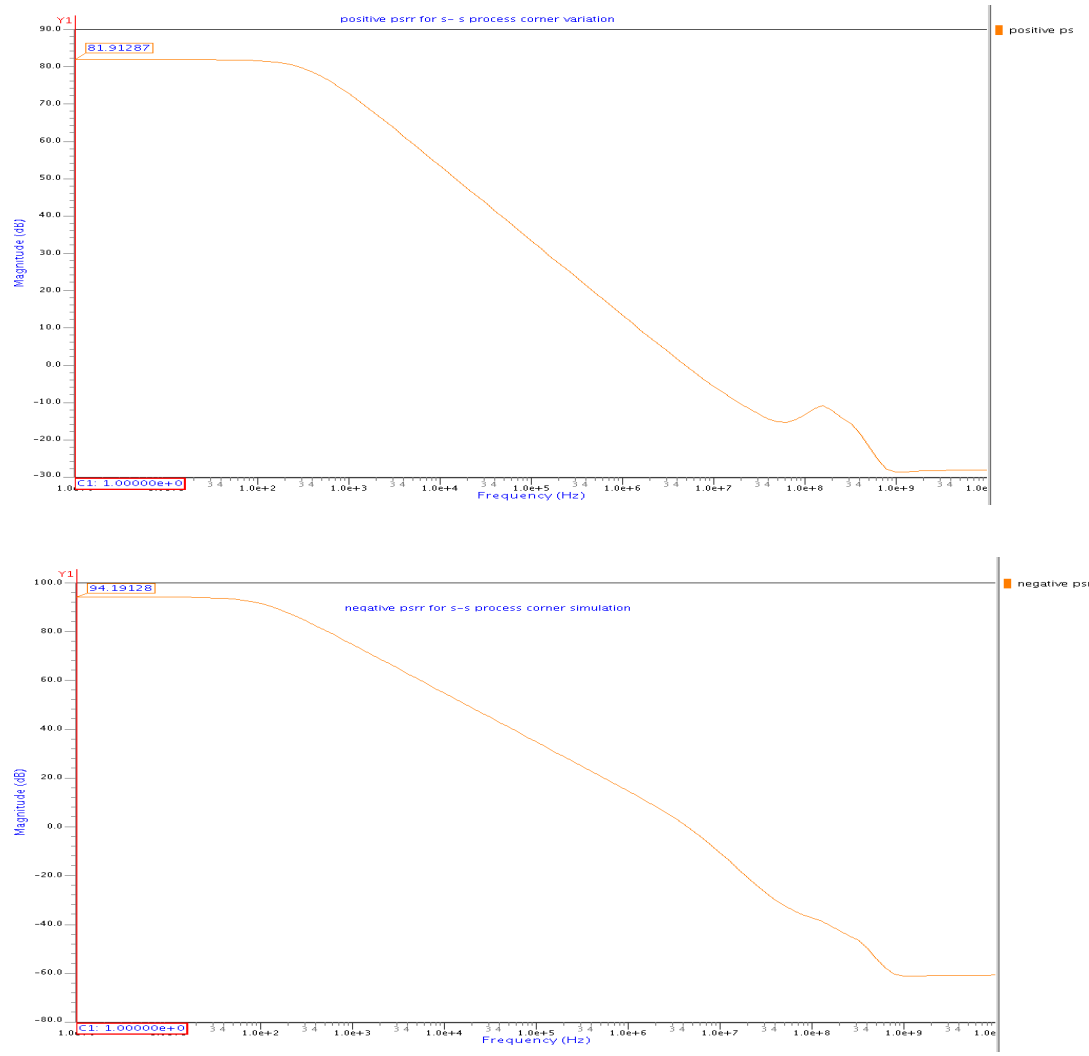


Fig 4.50 Process Corner –s-s simulation for PSRR analysis

4.2.3.7 INPUT COMMON MODE RANGE

Fig 4.51 to 4.54 shows process corner, ICMR of op-amp circuit.

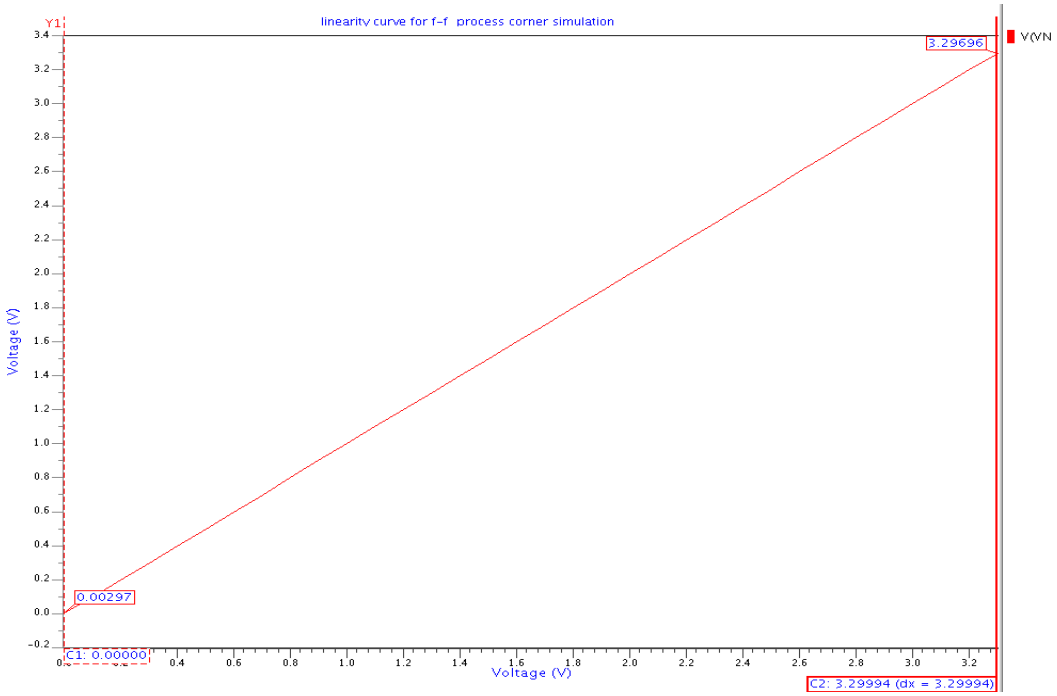


Fig 4.51 Process Corner –f-f simulation for ICMR analysis

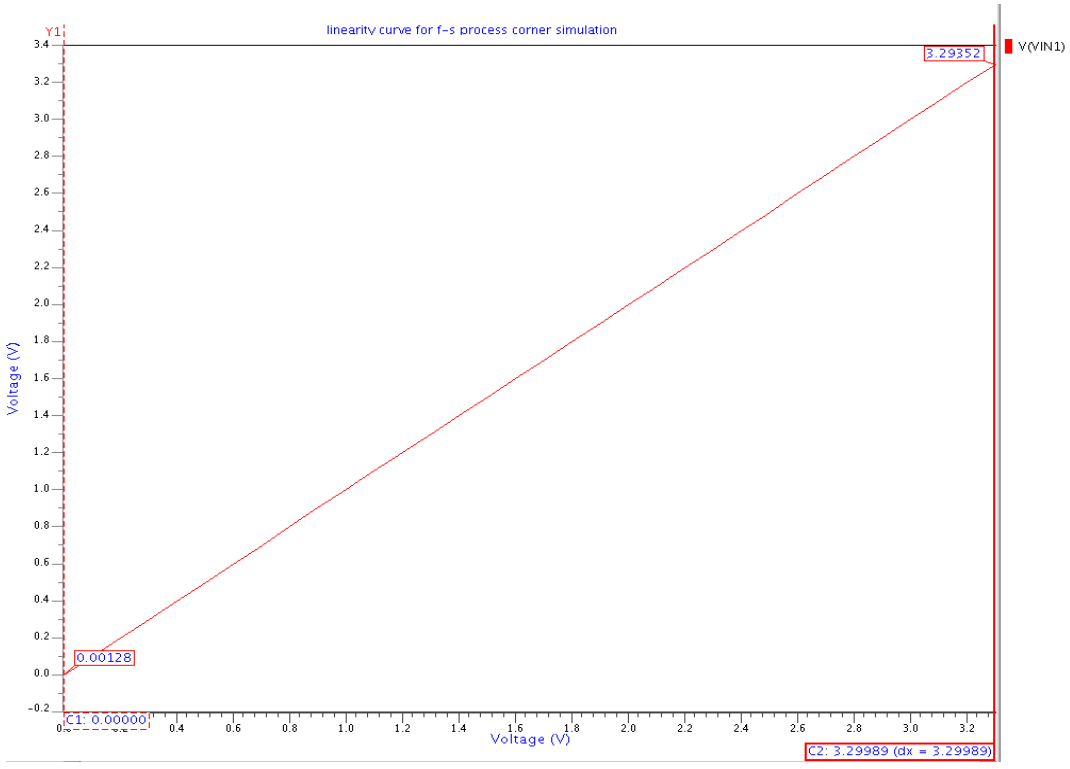


Fig 4.52 Process Corner –f-s simulation for ICMR analysis

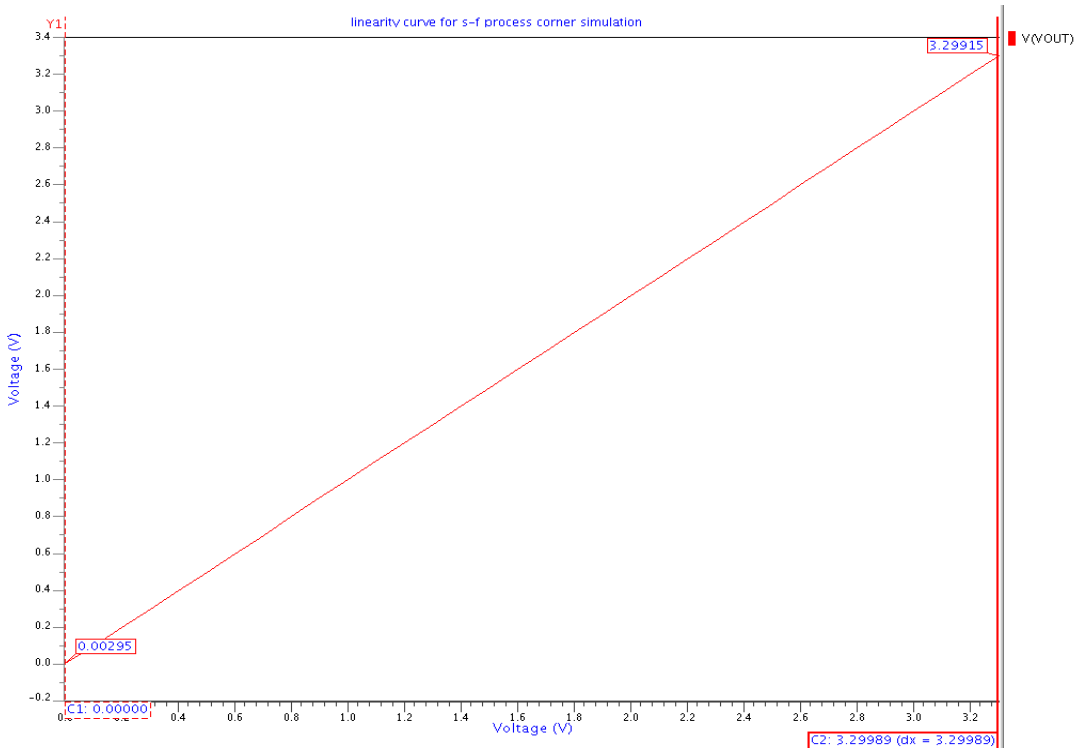


Fig 4.53 Process Corner –s-f simulation for ICMR analysis

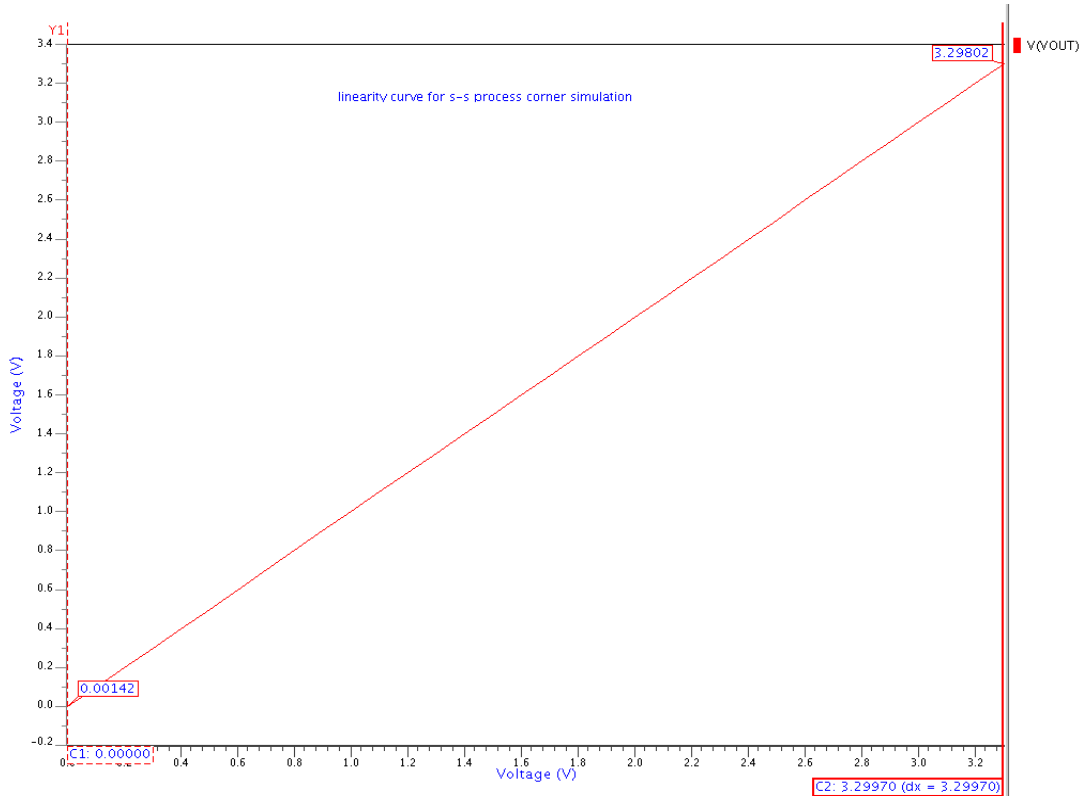


Fig 4.54 Process Corner –s-s Simulation for ICMR analysis

4.2.3.8 COMPARISON OF FOUR PROCESS CORNERS:

Table 4.4 Comparison of Four Process Corner Simulation

Specification	**Typical value**	**Process corner(f-f)**	**Process corner(f-s)**	**Process corner(s-f)**	**Process corner(s-s)**
DC Gain(dB)	95.7	93.2	80.8	101.6	96.1
UGB(MHz)	8.38	15.50	3.66	15.04	2.54
3-dB(Hz)	146.20	376	337	159	39
Phase margin(degree)	55.57	44.50	69.62	29.04	71.10
Slew Rate(v/µs)	2.81	10.65	1.39	6.29	0.76
Settling Time(ns)	1460	363.11	2757	723.24	5671.9
Power Dissipation(µw)	512	921	437	522	266
CMRR(dB)	101.69	88.90	99.94	94.43	112.03
Output Voltage Swing(V)	2.95	2.77	1.74	2.77	2.87
Positive PSRR(dB)	78.04	73.59	69.18	79.87	81.91
Negative PSRR(dB)	92.50	88.69	80.93	94.35	94.19

Above table shows comparison of process corners with schematic results.

CHAPTER 5

CONCLUSION AND AREA OF IMPROVEMENT

5.1 CONCLUSION

In this thesis work, a two-stage single ended rail-to-tail Op Amp is designed and simulated with the layout of the circuit. Complementary NP pair with the summing stage is used along with miller compensation is required between the first stage and second stage. An economical power efficient technique to achieve a constant rail-to-rail complementary N-P differential input stage used for achieving rail-to-rail input stage.

Simulation also shows that the frequency response of an op-amp using this constant *gm* input stage is nearly independent of the input common-mode voltage. The minimum CMRR is 101dB, which is acceptable. The high (full) output swing at the output of Op amp is obtained without slewing and with less power consumption by using Class AB output stage. Process corner simulation results shows that it can work efficiently in all process corners except in s-f process corner simulation.

5.2 AREA OF IMPROVEMENT

Due to the nature of the wide research topic, there are still several Areas of improvement for future work in this op amp. Total transconductance variation is about 5-10%. Due to this, Low frequency gain varies with input common mode voltage; it can be reduced to 2-3%. Simulation results for this op-amp are not good enough for s-f process corner simulation as phase margin is very lesser for this, it can be improved.

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