Performance Comparison between Optical and Copper Interconnects

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Submitted By:

Mahesh Kumar

Roll No.: 801161016

Under the Guidance of:

Mr. Karamjit Singh Sandha

Assistant Professor

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

THAPAR UNIVERSITY

(Established under the section 3 of UGC Act, 1956)

PATIALA – 147004 (PUNJAB)

CERTIFICATE

I, Mahesh Kumar, hereby certify that the work which is being presented in this thesis entitled "**Performance Comparison Between Optical and Copper Interconnects**" by me in partial fulfillment of the requirements for the award of degree of Master of Engineering in Electronics and Communication Engineering from Thapar University (Deemed University), Patiala, is an authentic record of my own work carried out under the supervision of Mr. Karamjit Singh Sandha.

The matter presented in this thesis has not been submitted in any other University/Institute for the award of any other degree.

Date: 15/07/2013

Mahesh Kumar
Roll No. 801161016

It is certified that the above statement made by the student is correct to the best of our knowledge and belief.

Date: 15/07/2013

Mr. Karamjit Singh Sandha
Asst. Professor (ECED)
Thapar University, Patiala

Countersigned by:

(Dr. Rajesh Khanna)
Professor and HEAD ECED
Thapar University, Patiala

(Dr. S.K. Mohapatra)
Dean of Academic Affairs
Thapar University, Patiala

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Mahesh Kumar

Mahesh Kumar
Roll No. 801161016

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ABSTRACT

Interconnect is basically used for data transmission inside an electronic device or system. Generally, it is used when the transmission distance is short. Device dimensions shrinks on chip, with future technology nodes. Some modifications are needed to be made in interconnect designing process based on the criteria of delay uncertainty, power consumption, bandwidth and noise. The conventional copper interconnects are not able to fulfil different design requirements. Copper based interconnects are facing many challenges. Because of dispersion, reflections and ringing, attenuation and its variation with frequency the high-speed signals are distorted. The performance of parallel links in conventional devices is also limited by the cross talk due to coupling from neighbouring signals. Copper interconnects have high power consumption, high latency, high cross talk and limited bandwidth. Interconnects are responsible for 70 to 80% of the signal delay in high-speed systems at deep submicron technology. Advancements must be done during design stage. Optical interconnects can be considered as a another alternative to meet these requirements. Optical interconnect due to its high bandwidth, low signal attenuation. Low signal delay, less power dissipation and cross talk, is an ideal candidate to tackle the challenges imposed by copper interconnects for on-chip applications at global interconnect level.

Because modern ICs require high bandwidth, less delay and low power dissipation, a study of performance comparison between copper and optical interconnects is necessary. This comparison helps in setting clear goals on the requirements of optoelectronic devices to give high performance as compared to conventional electrical (copper) devices. For on-chip applications at global interconnect level, optical interconnects can reduce latency and provide high-bandwidth at relatively low power. Optical interconnects provide better results in terms of delay and power dissipation as compared to conventional copper interconnects at global interconnect level.

In this thesis, delay and power dissipation results are simulated for optical and copper interconnects at various technology nodes. Simulation is done using SPICE simulation tool at global interconnect level. Optical interconnects give better delay performance as compared to conventional copper interconnects at each technology node. Power dissipation of optical and copper interconnects increases with future technology nodes because of higher clock

frequency and leakage current, but optical interconnects dissipate less power as compared to copper interconnects. Therefore, optical interconnects give better performance in terms of delay and power dissipation than conventional copper interconnects at global interconnect level for on chip applications.

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ABBREVIATIONS

ICs	Integrated circuits
OIs	Optical interconnects
CIs	Copper interconnects
CMOS	Complementary metal oxide semiconductor
PMOS	P channel metal oxide semiconductor
NMOS	N channel metal oxide semiconductor
PD	Photo detector
MSM	Metal semiconductor metal
TIA	Transimpedance amplifier
RC	Resistive capacitive
LA	Limiting amplifier
MQW	Modulator quantum well
VCSEL	Vertical cavity surface emitting laser
SOI	Silicon on insulator
CR	Contrast ratio
IL	Insertion loss
BR	Bit rate
WDM	Wave division multiplexing
VLSI	Very large scale integration
TSM	True Scale Miniatures
FOM	Figure of merit
MOSFET	Metal oxide semiconductor field effect transistor
MZM	Mach–Zehnder modulator
CNT	Carbon nanotube
EMI	Electromagnetic interference
EMC	Electromagnetic compatibility
PWB	Printed wiring board

CHAPTER 1

INTRODUCTION

1.1 Motivation

The performance of silicon ICs has improved as the number of functions per chip has become very large. Therefore, the cost per function has decreased. However, this performance is limited by fundamental limitations like high power dissipation, less bandwidth, and signal delay. Many of these problems arise from the physical limitations of Cu based electric wires [1]. Basically, copper interconnects use strip lines on a printed wiring board (PWB). The problems mentioned above have created a situation in which the performance of the system is degraded by the interconnect capacity and this situation is called interconnection bottleneck. An example of such a case is shown with the help of fig. 1.1 [2] which compares the development of the processor clock rate to the clock rate of the interconnection between the processor and the memory. The off chip I/O capacity is more lacking the internal performance of the IC.

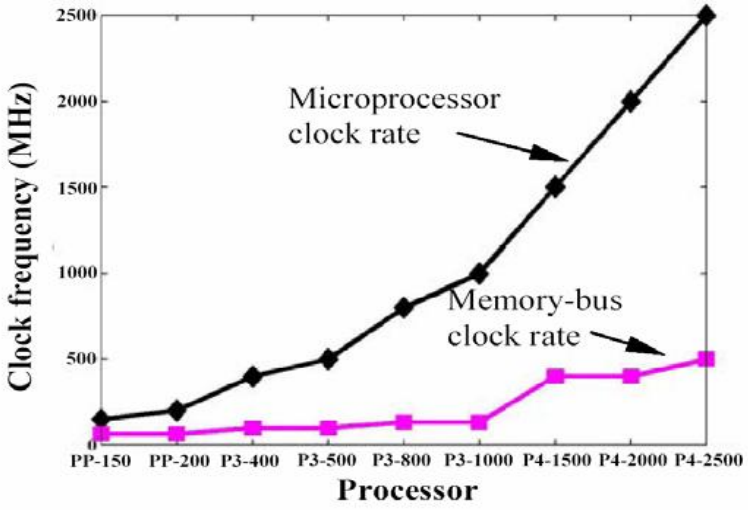

Fig. 1.1 Comparison of clock frequencies of Intel Pentium processor ICs and their memory buses [2].

Copper-based electrical interconnects are facing many challenges which are dispersion, reflections and ringing, attenuation and its variation with frequency. The high-speed signals can be distorted due to these factors. The attenuation of high frequency signals results in a need to use high-power line-drivers, which causes thermal management issues. Electromagnetic interference (EMI) causes noise and design constraints due to the need to fulfil electromagnetic compatibility (EMC) specifications [3]. The performance of parallel links is limited by the cross talk due to coupling from

neighbouring traces and the signal skew caused by variations in the delay between different signal traces. Following technological approaches can be used to address these problems [4].

- Increasing the aspect ratio
- Increasing the number of metal layers
- Reducing dielectric constant
- Reducing resistivity of metal line

It has been shown that even with the use copper of low-k dielectrics, these approaches are not successful. These techniques encounter limits and may slow down advances in integrated electronics [3]. It is predicted that interconnects are responsible for nearly 70 to 80% of the signal delay in high-speed systems [5]. If not considered during the design stage, these interconnect effects can cause damage like logic faults that can make a digital circuit inoperable, or the analog signal may be distorted such that it may not be able to fulfil its requirements. Extra iterations in the design cycle are costly, it is necessary to do accurate prediction of these effects in high-speed designs. Hence, it becomes extremely important for designers to simulate the entire design along with interconnect sub circuits efficiently while keeping the accuracy of simulation. Therefore, it is necessary to consider alternate interconnect scheme for future integrated circuits. The most novel candidate is optics based interconnects. Optical interconnect due to its high bandwidth, low signal attenuation and cross talk, is an ideal candidate to tackle the challenges imposed by electrical interconnects for both off-chip and possibly on-chip applications. Because the modern ICs require high system bandwidth and a large power density. A study of performance comparison between electrical and optical interconnects is very important. This performance comparison helps in setting clear goals on the requirements of opto-electronic devices to deliver a superior performance than their electrical counterparts. For on-chip application, optical interconnects can reduce latency, provide high-bandwidth at relatively low power. However, an optical waveguide, has a relatively larger size (pitch~0.6μm), making it difficult to provide high bandwidth density. This problem can be overcome by using wavelength division multiplexing (WDM). Optical interconnects, have some other advantages also over conventional copper interconnects, thus making it easier to achieve and maintain good signal integrity. Optical interconnects have lower signal dispersion, lower distortion, lower attenuation, lower skew and easier impedance matching of transmission lines, as well as immunity of

the signal path to EMI. The latter enables reduced signal crosstalk, easier EMC design and the possibility for higher interconnection density in parallel links [2]. Moreover, optical interconnects can be seen as architectural enabler: for instance, the low attenuation of the high-speed signal path would allow placing the processor and memory farther from each other. The value of these advantages mentioned above, depends on the application and all other constraints involved in the design and implementation of the system.

1.2 Overview

Interconnects are used to connect components on a VLSI chip, to connect chips on a multichip module, to connect multichip modules on a system board. In conventional copper interconnects CMOS buffer is used as a buffer or inverter. Interconnect load can be replaced with R, L and C lumped model. R, L and C parameters are determines from the physical specifications of interconnects. In long interconnects repeaters are inserted to reduce the overall interconnect delay. CIs have high power dissipation and high interconnect delay. CIs are described in detail in chapter 3.

Basically, optical interconnection refers to the data transmission in which the data signal is transmitted as a modulation of optical carrier wave (light) through an optically transparent media (optical fibre, planar optical waveguide or air). The intensity of the light source, such as a laser diode, is modulated and the transmitted optical signal is converted back to the electrical domain by the use of a photo detector in the receiver. The conventional electrical interconnects usually transmit data as a modulation of electric signal (voltage) through an electrically conductive media, such as copper wire. Regardless of the term optical, almost all optical data links actually operate at the near-infrared wavelength range between 800 nm and 1600 nm [2].

Basically, the use of the term optical interconnects is assumed to deal with data transmission inside an electronic device or system. It is basically used when the transmission distance is short. This can be compared to the term optical communication, which refers to optical data transmission between distant and independent systems. Sometimes, the term optical interconnects may also refer to optical communication links as well. Optical communications through fibre is preferred for high-speed long-distance data links. Gradually, as the capacity requirements of the systems have increased, the optical links have been used into shorter distance applications, such as fibre-to-the-home, local area network (LAN) and even into fibre-optic interconnects between boards and cabinets inside electronic equipment, which are to be referred as optical interconnects [2].

It was predicted that this trend would be continued and optics would perhaps be used to interconnect chips on a board or even to be used in intra-chip interconnects. Therefore, the conventional electrical interconnects are likely to replaced by optical interconnects in some applications. Although there is no clear distinction between the terms optical communications and optical interconnects, this work is clearly about the latter. This is because the technologies to be discussed are preferred for relatively short distance interconnections less than 1 meter and only to be used inside electronic equipment.

For the introduction of optical interconnects into VLSI architectures compatibility with CMOS technology is required. Due to the absence of an efficient silicon-based laser, only those configurations that utilize an external laser as a light source are preferred. A basic block diagram of an optical interconnects system is shown in fig.1.2 [6].

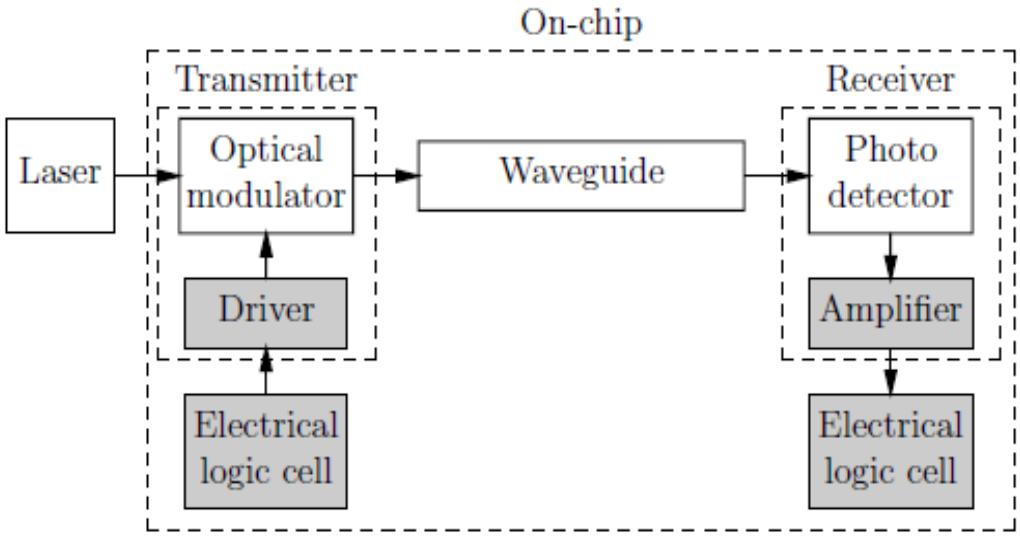

Fig. 1.2 Basic block diagram of an on chip optical interconnect data path [6].

Considering the compatibility with a CMOS technology, a practical solution is a 1.5 μm wavelength light source with a silicon modulator and a SiGe or Ge photo-detector. Unlike electrical devices, optical devices are not easily scalable due to the light wavelength constraInternational The performance and integration ability of optical devices, however, are expected to be further improved by technology inventions and structural optimization techniques. A transmitter is composed of an electro-optical modulator and a driver circuit. The design of a fast and cost efficient CMOS compatible electro-optical modulator is one of the most challenging tasks on the path towards the realization of on-chip optical interconnects [6]. To improve the performance of a modulator, a comprehensive closed-form model is used to determine a proper trade-off among all physical parameters of a MOS modulator. A series of tapered inverters is used

as the driver circuit which is used to drive the modulator. For a specific operating wavelength of 1.5μm, low refractive index strip polymer waveguides are assumed with a core cross section of 1.5 μm×1.5 μm. The core index and cladding index are 1.6 and 1.1, respectively. The mode effective index is assumed as 1.48. The receiver circuit has two components: a photo-detector and an amplifier. In this work, interdigitated SiGe p-i-n or metal semiconductor metal (MSM) detectors are considered due to the fast response and reasonable quantum efficiency of these structures. Recently some advances have been made in the last few years, which have resulted in development of a hybrid-silicon laser as a source of optical power, high speed silicon based electro-optic modulators based on the carrier interactions [7], [8], low-loss input couplers and optical amplifiers [8], Si-Ge based photo-detectors, thereby promising the possibility of an more accurate on-chip optical communication system. It has also been found that for global interconnect distances of typical length (~25mm), optical SOI (silicon-on-insulator)-waveguide based interconnects give better latency and power advantages than electrical interconnects for future technologies. With Wave Division Multiplexing (WDM) the spatial-bandwidth for the optical interconnects is also higher than their electrical counterpart. Multiple architectures have been proposed for on-chip optically connected multi-processor systems. Based on these systems architects have found modest performance improvement against their electrical counterparts. However, most performance evaluations ignore the technological challenges that will arise out of integration, such as controlling the thermal sensitivity of optical devices.

Despite the significant progress achieved in the intensive research done by many groups worldwide, optical interconnects are not much used inside commercially available electronics products. Only fibre-based interconnects are in use up to some extent. One reason is perhaps that the introduction of this technology would represent a significant technological step in the design and production of electronic equipments. Such a step would require a major R&D investment from the industry. In addition, the historical aspect also plays an important role. Even if optical interconnects were to demonstrate superior performance over the electronic alternative, technology transfer is not necessarily guaranteed due to the fact that the experience with materials, design procedures and manufacturing processes of electrical interconnects is well known and established [9]. The logical conclusion is that in order to ease transfer to a novel technology with the high bit-rate optical interconnects; the needed technological step should be made as small as possible. In other words, the novel technology has to be

developed based on the existing technology instead of developing a completely new one. Consequently, on board-level interconnects, the technologies should be made compatible with the conventional circuit board processes and assembling practices. Therefore, there are at least two obvious prerequisites for the introduction of optical interconnects in commercial applications: the costs per interconnect capacity should be competitive with copper-based interconnects in mass-production, and the required PWB area or volume should not exceed that of equivalent copper solutions.

1.3 Types of interconnects

Interconnects are often classified using the International packaging level hierarchy (Tummala & Rymaszevski 1989), which is based on the type of interconnected components and their typical interconnection distances as following [10]:

- Chip level (intra-chip) 0...10 mm
- Multi-chip-module level (intra-MCM or chip-to-chip) 1...100 mm
- Board level (MCM-to-MCM or chip-to-chip) 10...300 mm
- Backplane level (board-to-board) 0.1...1 m
- Cabinet level (rack-to-rack) 0.3...5 m
- System level (cabinet-to-cabinet) 1...100 m.

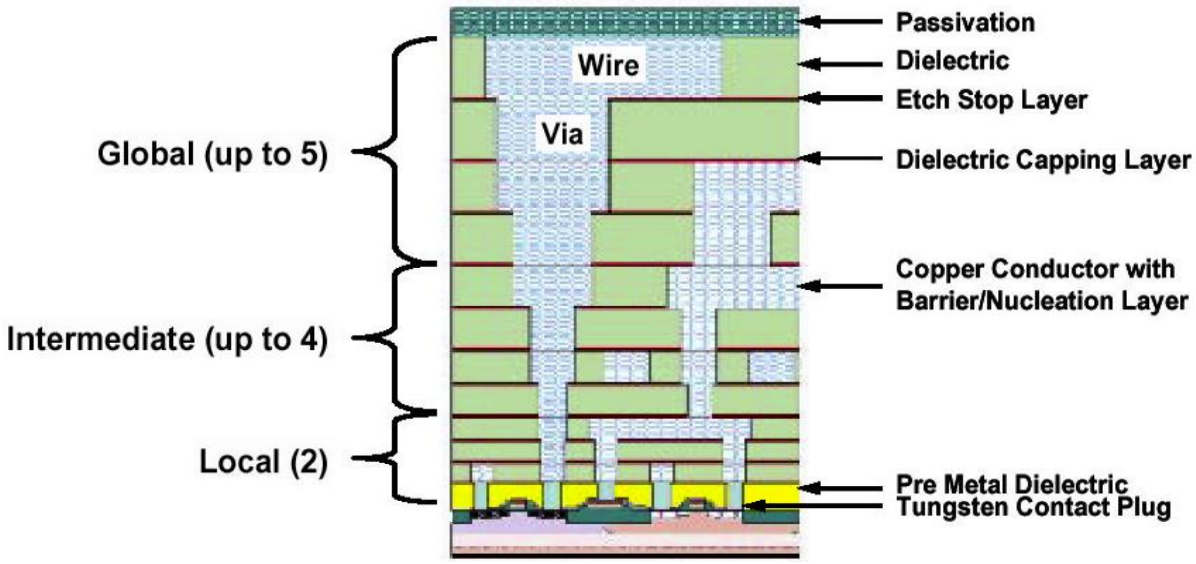

Fig. 1.3 Schematic showing the hierarchy of metal levels for distribution of interconnects in modern ICs [11].

On a modern IC chip interconnects can also be broadly characterized into three groups according to the functions they perform. These are as following:

- Signalling interconnects
- The clock distribution interconnects

- Power and ground supply distribution interconnects

Interconnects can be further subdivided into following three categories according to the range of their lengths and their cross section dimensions [11]. These are as following:

a) the local interconnects
b) semi-global or intermediate interconnects
c) the global interconnects

The global interconnects are used for long distance communication on a chip and have a larger cross sectional area to minimize the resistance. Whereas, the local interconnects have the shortest range and the least cross sectional dimensions. Modern ICs have multiple levels of interconnects to accommodate their large numbers, starting from the local at the lowest level to the global at the top most levels. This is depicted in Fig. 1.3 [11].

1.4 Performance Metrics for Interconnects

Performance metrics for interconnects discussed are mostly applicable to all physical type of interconnects. However, there are some properties which are more relevant to the metal-based interconnect systems. Out of these metrics some have more importance than others. For example, delay and power are very important for signalling interconnects. While, for clock distribution, it is more important to have interconnects with a less delay and low power. The other figures of metrics of importance are the cross talk and electro migration reliability. The capacitive cross talk can eventually cause delay uncertainty in clocks wires and deterioration of reliability of logic level communication in signal wires. On the other hand, in the extreme case, the electro migration reliability failure can cause circuits to stop working.

The delay of the wires can be well approximated by the product of resistance (R) and the capacitance of the wire (C), if inductive effects are not so important [12]. The wire capacitance basically has three components: inter-level, inter-metal (within the same level between metal lines) (Fig. 1.4) and the fringe component. The delay of longer wires is more accurately modelled by RC product because this component is proportional to square of the length of the wire. Whereas, for very short lengths, the wire delay is better approximated by purely the loss-less inductive delay formula (length divided by the speed of the light in the medium) [12] and only increases linearly with length. Because the wire

resistance is increasing very rapidly as compared to the inductance, the wire delays are becoming more and more RC at even shorter distances. To model the RC delay of the wires it is necessary to accurately model both the resistance and the capacitance accurately.

Power dissipation due to interconnect is an important metric. It depends on charging and discharging of its capacitance. At a given technology node, the interconnect power is heavily dependent on its total capacitance.

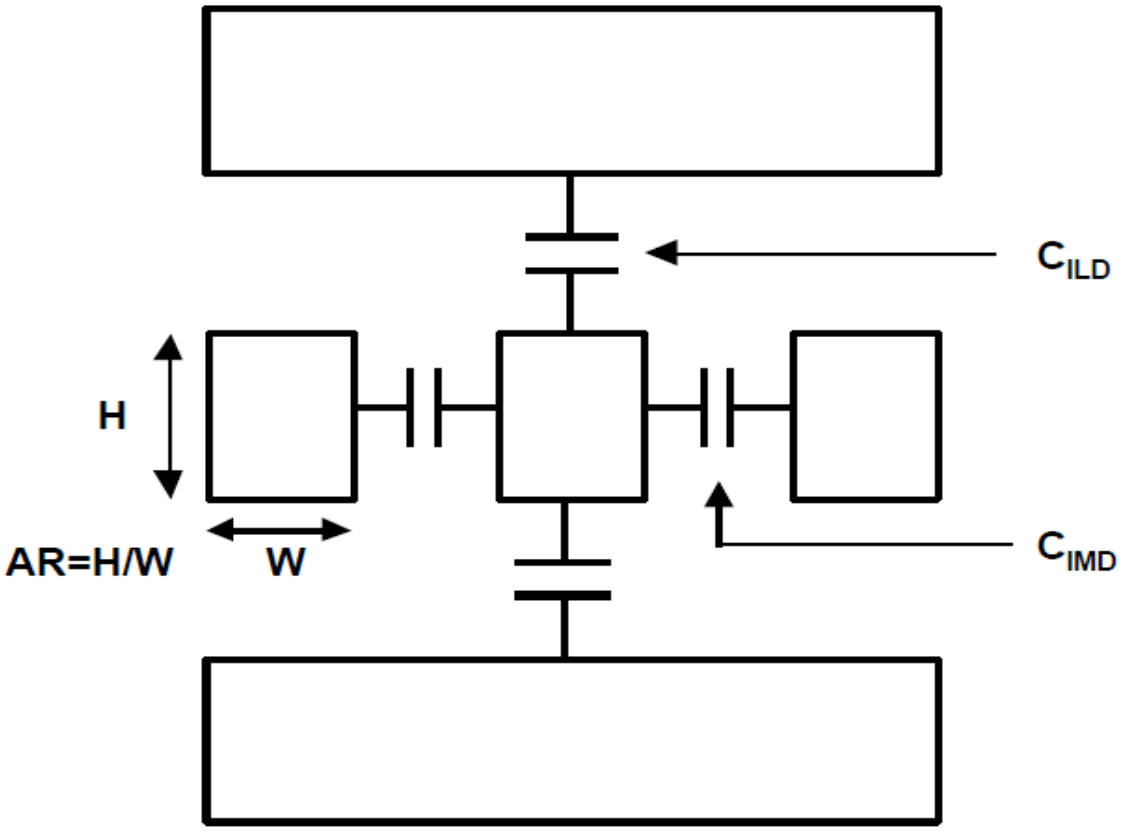

Fig. 1.4 Schematic showing the inter-metal and the inter-level components of capacitance. Also showing aspect ratio (AR) [13].

Capacitive crosstalk is another important metric, falls under the category of signal transmission reliability related to both timing and logic level. Other potentially important source of noise influencing the signal reliability is the inter-symbol interference (ISI) and it is caused by impedance discontinuities in the electrical transmission lines [13]. Cross talk is proportional to the ratio of the inter-metal to the total capacitance [13] of the wire. Thus, from the perspective of cross talk it is more beneficial to lower just the inter-metal capacitance. Therefore, sometimes an inhomogeneous backend dielectric approach is adopted, where; the inter-metal dielectric constant is lower than the inter-level dielectric constant.

Electro migration reliability is another very important aspect for metal based interconnects. The current through metal wires flows to metal atom migration due to momentum exchange between electrons and metal atoms [14]. This migration leads to the depletion of enough material so as to initially increase the wire resistance and finally cause an open circuit. On the other hand, it also causes excess metal atoms to accumulate at a different location along the wire, which can cause a short to the adjacent wire through metal hillocks in extreme cases. The primary factors, which influence the electro migration, can be divided into those which are related to the physical structure of the metal wire and to the conditions of operation. Some crystal orientation of thin films (metal wire) is more conducive to preventing electro migration. Among the conditions of operation, temperature and the current density play an important role in dictating electro migration (Black's equation [14]) and their minimization is the responsible for good reliability. The current density of a wire is dependent on the cross-sectional dimensions of the wire, if the driver resistance dominates and dictates the current. The wire resistance may dominate over the driver resistance in the case of very long wires and in the future (rising metal wire resistance). In that case, the current will be dictated by the wire dimensions, thus changing the cross sectional area will change both the current and the area, leaving current density unchanged to the first order. Therefore, wire dimensions again play a critical role in deciding electro migration reliability.

The final figure of merit is the joule heating because of interconnects. It is imperative to mention here that a non-negligible and increasing resistance of the wires leads to an I^2R (I is the current) power dissipation in the form of heat. This increases the temperature of interconnects above the device temperature, especially if lower dielectric constant material, are used, which are also invariably poorer heat conductors.

It can be noticed from above discussion that almost all interconnect metrics for metal based wires depend on their resistance and capacitance, which, in turn, are influenced by the 1) physical dimensions (both resistance and capacitance) 2) dielectric constant (capacitance) and 3) material resistivity (resistance). To improve these figures of metrics, it is clear that one needs to lower both dielectric constant (k) and material resistivity. To lower the material resistivity copper based wires were recently introduced instead of the higher resistivity Aluminium based wires. This also had an advantage of better electro migration properties. Various performance metrics have been discussed above. Out of these metrics, delay and power dissipation of the copper and optical interconnects are addressed here.

1.5 Thesis Objectives

Aim of this work is to compare the conventional copper interconnects and optical interconnects for various technology nodes. The objective is to find a prediction of the performance characteristics of future CMOS compatible optical devices. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. As the technology is scaled, it has become quite difficult for the conventional copper interconnects to satisfy the design requirements of integrated circuits. In the recent times optical interconnects at global interconnect level has been considered as a proper alternative to the conventional copper interconnects. In this thesis work, copper and optical interconnects are compared for delay and power dissipation at different technology nodes. Results for delay and power dissipation for both copper and optical interconnects are simulated using SPICE simulation tool. Results show that optical interconnects is a better option than copper interconnects at one cm channel length.

1.6 Thesis Organization

Keeping the performance comparison between optical and copper interconnects in terms of power and delay at various technology nodes, this thesis is divided into 6 chapters. All aspects of copper interconnects and optical interconnects are discussed in the following chapters. Literature survey of about the topic is also given. Simulation results are discussed to compare both interconnects at various technology nodes using different parameters. Based upon the simulation results for delay and power dissipation a conclusion is made, which is elaborated properly. The future work that must be done in this area, is also shown.

Chapter 2 gives literature survey about the topic. In order to start the thesis, the first step is to study the papers that have already been published by other researchers. Papers related to this work are chosen and studied. With the help of literature review, it becomes easier to perform this work. A review of various aspects of copper interconnects is presented. It is shown in the papers, that how the conventional copper interconnects are not able to fulfil the requirements of modern IC designs. It is shown that optical interconnect is a potential candidate to tackle the challenges of modern ICs. Various requirements for the implementation of optical interconnects are also shown.

Chapter 3 describes the conventional copper interconnects. Various aspects of copper interconnects are shown. It is shown how they are not able to fulfil the

requirements of modern ICs in term of various criteria. . The negative aspects are wire resistance, causing delay and dispersion, and high capacitance, causing large power consumption at large voltage swings. They face challenges like reflections and ringing, attenuation and its variation with frequency. The attenuation of high frequency signals results in a need to use high-power line-drivers and thus causing thermal management issues. Electromagnetic interference (EMI) causes noise and design constraints due to the need to fulfil electromagnetic compatibility (EMC) specifications. Moreover, the performance of parallel links is limited by the cross talk due to coupling from neighbouring traces and the signal skew caused by variations in the delay between different signal traces. Then its basic CMOS circuit is shown. Model of global interconnect is shown. Various equations are given for calculating its R, L and C parameters. It is shown how repeaters are inserted in long interconnects to reduce the delay. Delay and power analysis is done.

Chapter 4 describes the optical interconnects. It is shown how they can tackle the various challenges imposed by conventional copper interconnects. Optical interconnects are described as potential alternative to the conventional copper interconnects at global interconnect level. Basic optical data path at 1 cm length is shown. Optical interconnect based systems require a means of transforming the electrical signal to the optical domain (modulator), a super buffer to derive the modulator, a waveguide to route the optical signal, and a photo detector to convert the optical signal back into an electrical signal and then transimpedance amplifier to convert current into voltage. Transmitter, waveguide and optical receivers are described in detail. Delay and power dissipation analysis of each part of the optical interconnect system is done.

Chapter 5 gives results and discussion. Interconnect load can be represented by R, L and C parameters. These parameters are determined from the physical geometries of interconnects which are given for various technology nodes. R, L and C parameters of interconnect are calculated at various technology nodes for different numbers of repeaters using physical parameters of interconnect. Then delay simulation is done for optical and copper interconnects at different frequencies for various technology nodes. It is shown optical interconnects give better performance than copper interconnects in terms of delay. Delay of optical interconnects decreases with future technology nodes, whereas delay of copper interconnects increases. Delay of both interconnects decreases with frequency. Power dissipation simulation is also done for optical and copper interconnects at different

technology nodes at global interconnect level. In the contrast to delay, power dissipation of optical interconnects increases with future technology nodes. Power dissipation of conventional electrical interconnects (copper interconnects) also increases with future technology nodes. As the technology is scaled down, power dissipation increases for both type of interconnects because of higher clock frequency and leakage current.

Chapter 6 gives conclusion and future work. The performance characteristics of future CMOS compatible optoelectronics devices are predicted. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. The performance comparison between optical and copper interconnects is done in terms of delay and power dissipation. For performance comparison delay and power dissipation are simulated for both type of interconnects at various technology nodes. SPICE simulation tool is used for delay and power dissipation simulation. Delay and Power dissipation are simulated at 90nm, 65nm, 32nm, 22nm and 14nm technology nodes. For minimization of delay in copper interconnects repeaters are inserted. Delay and power dissipation are simulated for each individual part of the transmitter and receiver in an optical interconnect system. It is shown optical interconnects give better results than copper interconnects in terms of delay and power. Scope of future work related to this topic is also shown.

CHAPTER 2
LITERATURE SYRVEY

2.1 INTRODUCTION

In order to start the thesis, the first step is to study the papers that have been already published by other researchers. Paper related to this work are chosen and studied. With the help of literature review, it becomes easier to perform this work. A review of various aspects of copper interconnects is presented. It is shown in the papers, that how the conventional copper interconnects are not able to fulfil the design requirements of modern ICs. It is shown that optical interconnect is an potential candidate to tackle the challenges of modern ICs. Various requirements for the implementation of optical interconnects are also shown.

2.2 Research Paper Literature Survey

Guoqing Chen et al. [6] stated that Interconnect has become a primary bottleneck in integrated circuit design. As CMOS technology is scaled, it will become quite difficult for conventional copper interconnects to satisfy the design requirements of delay, power, bandwidth, and noise. On-chip optical interconnects have been considered as potential substitute for electrical interconnects in the past two decades. Predictions of the performance of CMOS compatible optical devices are made based on current state-of-art optical technologies. Electrical and optical interconnects are compared for various design criteria based on these predictions at different technology nodes. The critical dimensions beyond which optical interconnects become advantageous over electrical interconnects are shown to be approximately one tenth of the chip edge length at the 22 nm technology node.

Rajeev K. Dokania and Alyssa B. Apsel [7] proposed that Optical interconnects are considered as the solution to the performance bottleneck of future interconnects in scaled technology nodes. Though significant steps have been made in realizing silicon photonic devices that can give high performance in controlled lab environments, there still exists some technical challenges preventing dense integration and reliability in varying conditions. Such problems are examined while suggesting possible solution space and proposing some alternatives. Actual power advantage is also calculated that optical links will have compared to an electrical link while considering the thermal stabilization and

other technological issues. It is shown that the ~4X power advantage that ideal on-chip global optical interconnects have been projected to have is reduced to null when the power required for thermal regulation of critical optical components alone are added into the calculations. They also discuss latency, spatial bandwidth, polarization and a host of other technological issues and reassess the benefits of dense on-chip optical interconnects for dense global routing. This work is the first work in on-chip optical interconnects that analyzes the performance impact of the challenges in on-chip optical interconnects in detail. They also propose solutions for the challenges and study the impact of the solution on the performance and reassess the improvement. But silicon-photonic devices still require a lot of work before using for dense integration and on-chip interconnect applications. Though, Material system changes may drive their dense-integration in future. In near term, off-chip or chip-chip interconnects with integrated interface optical components look more reasonable and practical solution. The power, distance, latency and data-rate tradeoffs are more significant for off-chip optical interconnects as compared to on-chip optical interconnects.

Guoqing Chen et al. [8] described that in deep sub micrometer VLSI technologies, it has become quite difficult for conventional copper based electrical interconnect to meet the design requirements of delay, power, bandwidth, and delay uncertainty. One potential candidate to solve this problem is optical interconnect. Based on a practical prediction of optical device development, a comprehensive comparison between optical and electrical interconnects is described. Delay uncertainty is also considered. Delay-optimal designs of RLC interconnect is presented. A prediction of the performance characteristics of future CMOS compatible optical devices is described. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. Critical lengths beyond which optical interconnect becomes advantageous are also presented. These lengths are significantly below the expected chip die size dimensions.

Helmut Graeb [9] updated a section on analog design technology challenges in recent 2011 version, The International Technology Roadmap for Semiconductors. The challenges and their solution approaches are discussed. Structure and symmetry analysis, analog placement, design for aging, discrete sizing, sizing within loop layout, and performance space exploration are shown.

H.B.BAKOGLU [15] stated that the propagation delay of interconnects is an important factor deciding the performance of VLSI circuits, because the RC time constant of interconnects increases very rapidly as chip and interconnect dimensions are scaled. To decrease the interconnect time delay, properly-scaled multilevel conductors, repeaters, cascaded drivers, and cascaded drivers as repeaters are presented. The delay model presents optimum cross sectional interconnect dimensions and driver/ repeater configurations that can reduce interconnect time delays by more than an order of magnitude.

Charles Thangaraj et al. [16] shown that Nanometer CMOS technologies have become a better interconnection technology, as long global interconnects have been shown to be a design bottleneck. Optical interconnect technology is a potential alternate to conventional interconnects and has immense potential to improve interconnect delay, clock skew, jitter and have better signal integrity. The keys to successful adaptation of on-chip optical interconnects are ease of integrating optical components into standard CMOS manufacturing and low manufacturing cost. They demonstrate a truly CMOS compatible optical clock distribution system and enable successful adoption of on-chip optical interconnects. The proposed optical clock distribution system and clock recovery components were implemented on silicon as a test vehicle in a mature 0.35 micro meter CMOS process for feasibility analysis. Although there is still a chance of improvement in many aspects of the test circuit designs, experiments on the test chip have established the feasibility of the proposed approach and the overall system functionality. They observe no concerning fundamental challenges in successfully implementing the design presented here in advanced nanometre CMOS technologies that require greater that 10 GHz clock frequency.

Rajeevan Chandel et al. [17] stated that delay and power dissipation are the two major design aspects in very large scale integration (VLSI) circuits. These arise due to millions of active devices and interconnections connecting large number of devices on the chip. Repeater insertion in long interconnections is an important technique used to reduce delay in VLSI circuits has been reported during the last two decades. This work deals with delay, power dissipation and the role of voltage-scaling in repeaters loaded long interconnects in VLSI circuits for low power dissipation. Trade off between delay and power dissipation in repeaters inserted long interconnects has been reviewed here with a bibliographic survey. SPICE simulations have been used to validate the findings.

Optimum number of uniform sized CMOS repeaters inserted in long interconnects, improve interconnect delay. Voltage-scaling is an effective solution in reduction of power dissipation in repeaters loaded long interconnects. It is shown that optimum number of repeaters required for delay minimization decreases with voltage-scaling. This leads to area and further power saving. The bibliographic survey needs to be revised in future, taking the various other aspects of VLSI interconnects viz. noise, cross talk extra into consideration. This work is of high significance in VLSI design and low-power high-speed applications. It is also valuable for new researchers in this emerging field.

B.Dhoedt et al. [18] elaborated that the performance of future generation data processing systems will be degraded by interconnect limitations rather than by IC performance. The main reason for this expected I/O bottleneck is the projected increase in CMOS IC-density and complexity, in terms of chip size, number of I/O pads and clock frequency. Problems inherently associated with closely packed electrical interconnects (such as cross-talk, signal distortion, EMI) will lead to bandwidth limitations, eventually resulting in a mismatch between silicon processing capabilities and interconnect performance. Two-dimensional optical interconnects have been proposed, improving the chip level input/output performance. Two optical arrangements were made and discussed, for inter-MCM (*micro optical* module) and intra-MCM interconnects respectively, and first results on optical components were presented, as well as performance characteristics of first generation opto-electronic components.

Min Tang et al. [19] presented a novel methodology of global interconnect optimization for high performance integrated circuits. The effects of interconnect width and spacing on various performances like delay, power dissipation and chip area are considered. There is a trade-off between delay and power dissipation of global interconnects with repeaters insertion. Optimum line width is calculated by the minimum delay-power product which is defined as a figure of merit (FOM). As the silicon area and wire ability of chip are considered, the delay-power-area product is introduced as another FOM to optimize the global interconnects. Optimizations of global interconnect size in different scenarios are applied for different International Technology Roadmap for Semiconductor technology nodes.

Claudio I. Estevez et al. [20] described that efficient coupling scheme of VCSELs (vertical cavity surface emitting lasers) and PIN PD through waveguides of optical interconnects systems is a challenging task and research is being done on this. Previous

technical approaches prefer flat-mounted VCSELs and the use of mirrors to guide the light into the waveguide and into the PIN PD. The use of mirrors causes relatively a large power penalty and hampers the scalability of integration. It is shown that by using the proposed integration process, losses are reduced, caused by the use of mirrors or other optical coupling techniques with a similar purpose. The process is quite simple and the required components are not expensive. Coupling efficiencies of approximate 20% are achieved in this work over a waveguide of 10.8 cm length. The process presented a lenient alignment constraInternational A misalignment of 20 μm in any direction from the center of the waveguide was found to cause a loss of less than 3 dB. It is shown that the similarity in multi-channel system performance confirms that the process is stable and reproducible. The manufacturing process can be cheap and with the performance attributes shown before, this architecture is a promising solution for mass produced networking equipments such as information access networking products for home and office environments.

Sandeep Saini et al. [21] analysed that in VLSI interconnects buffers are used to restore the signal level deteriorated by the parasitic. However, buffers have a certain switching time that contributes to overall signal delay. Moreover, the transitions that occur in interconnects also contribute to crosstalk delay. Therefore, the overall delay in interconnects is due to combined effect of both buffer and crosstalk delay. A replacement .of buffers with Schmitt trigger is proposed for the same purpose of signal level restoration. Because of the lower threshold voltage of Schmitt trigger signal can rise early and the large noise margin of Schmitt trigger helps in reducing the noise glitches as well. Simulation results shows that the approach using the Schmitt trigger gives 20% delay reduction as compared to 10.4% in case of buffers**.**

Yun-Parn Lee and Yulei Zhang [22] stated that although a great deal of research has been carried out over the last decade in which many different techniques for devising optoelectronic interconnects have been proposed, more detailed analysis of the performance parameters like power, latency, and area of different optical technologies is yet to be done. Optoelectronics offer potential for new approaches to the production of VLSI interconnects, but previous works have made clearly simplified assumptions for optoelectronic interconnections. Based on this analysis, it is concluded that the three-dimensional free-space optoelectronic interconnect network has the best speed area product performance as compared to fiber-optical interconnects and optical micro

electromechanical systems (MEMS) interconnects. Second, although the optoelectronic interconnect offers higher data rates and less power per bit as compared to electronic interconnects, the bipolar encoding scheme on the source plane and the detector plane means that a larger area and volume will be needed.

Arun Palaniappan and Samuel Palermo [23] described that high-bandwidth inter-chip optical interconnects architectures have the capability to address increasing input–output bandwidth demands. Comparison is done of several optical interconnect architectures on the basis of power efficiency in 90-nm and 45-nm CMOS technologies. Under consideration are a near-term architecture containing discrete vertical-cavity surface-emitting lasers (VCSELs) with p-i-n photo detectors (PDs) and three long-term integrated photonic architectures which use waveguide metal–semiconductor–metal photo detectors and either electro absorption modulator (EAM), ring resonator modulator (RRM), or Mach–Zehnder modulator (MZM) sources. An optimal current density approach with normalized transistor parameters extracted from circuit simulations is applied to jointly optimize driver and receiver circuitry to minimize the over all link power dissipation. Based on this analysis, it is shown that the VCSEL-based link is limited by VCSEL bandwidth and maximum power levels, rather than circuit bandwidth, and achieves a maximum of 24 Gb/s in both the 90-nm and 45-nm technologies nodes. The EAM and the RRM are both potentila integrated photonic technologies capable of scaling data rates past 30 Gb/s at power efficiency levels near 0.5 mW/Gb/s in the 45-nm node and are basically limited by coupling and device insertion losses. However, the MZM offers robust operation due to its wide optical bandwidth, significant improvements in power efficiency must be achieved to become applicable for high-density applications.

K. H. Koo et al. [24] presented that the on-chip interconnect bottleneck with conventional Cu/low-k and delay optimized repeater scheme provides a substantial reason to investigate novel interconnect circuit architectures. The capacitive driven low-swing interconnect (CDLSI) has the ability to affect a significant energy saving and latency reduction. An accurate analytical, optimized model was developed for CDLSI wire scheme. Comparison of the delay and energy expenditure was done for not only different interconnect circuit schemes, but also different future technologies such as Cu, carbon nanotube and optics. It was found that CDLSI circuit scheme outperforms the conventional interconnects in latency and energy per bit for less bandwidth requirement, while these advantages degrade for higher bandwidth requirements.

Mandeep Bamal1 et al. [25] stated that several technological and architectural solutions have been used to solve the "Interconnect performance bottleneck", such as the use of on-chip transmission lines, carbon-nanotube (CNT) interconnects, wafer-level package (WLP) interconnects, 3D interconnects, RF and microwave interconnects and optical interconnects. It is imperative to accurately estimate the interconnect performance and power gains achievable by these approaches and to understand the various trade-offs involved between the different metrics of interest. A performance comparison in terms of energy and density metrics has been carried out among the different options for global interconnects. This comparison shows that 3D interconnects offer an attractive option to reduce the energy dissipation and propagation delay of long on-chip wires. This analysis also verifies that optical interconnects offer reduced latency compared to scaled Cu/Low-k technologies but they do not offer significant improvement compared to other technologies like WLP interconnects. It is also shown that CNT interconnects compare favourably to scaled Cu/Low-k interconnects in terms of latency with a 42% reduction in delay.

Slaviša Aleksi et al. [26] described that architecture of network elements such as large routers and switches is becoming more and more complex because of the continously increasing requirements on both capacity and performance. Already today, high-performance routers having capacities of more than several Tb/s can't be packaged in a single rack of the equipment. Complex and spatially distributed multi-rack routers consisting a large number of line cards, switching modules and high-speed ports have already become reality. A consequence of this trend is that internal interconnecting system also becomes large and complex. Interconnection distances, total number of cables and power consumption enhance rapidly with the increase in capacity, which can cause limitations in the scalability of the whole system. Needs and limitations of large-scale optical interconnects are addressed. Various point-to-point interconnects and two optically switched interconnection options with regard to their scalability are also investigated by taking into the account different optical signal impairments, number of fiber links and over all power consumption. Optical point-to-point interconnects require a large number of fiber links, specially the options providing a low data rate per channel. The total number of fibers needed can be decreased by increasing the data rate per channel and by transmitting several channels over a single fiber in a WDM manner. However, the number of fibers can't be lower than that required by optically switched

interconnects. It is shown that optically switched interconnects have the potential to improve the energy efficiency of high-capacity switches and routers. Their scalability is mainly limited by the optical impairments that need to be effectively compensated.

Ashok V. Krishnamoorthy et al. [27] stated that optical links have successfully replaced electrical links when their aggregated bandwidth distance product exceeds over 100 Gb/s-m because their link energy per bit per unit distance is lower. Optical links will continue to be adopted at distances of 1 m and below if the link power falls below 1 pJ/bit/m. Providing optical links directly to a switching/routing chip can potentially improve switched energy/bit. An early experimental switched CMOS-vertical-cavity surface-emitting laser (VCSEL) system is presented operating at Gigabit Ethernet line rates that achieves a switched interconnect energy of less than 19 pJ/bit for a fully non blocking network with 16 ports and an aggregate capacity of 20 Gb/s/port. The CMOS-VCSEL switch achieves an optical bandwidth density of 37 Gb/s/mm^2 even when operating at a modest line rate of 1.25 Gb/s and is capable of scaling to much higher peak bandwidth densities (350 Gb/s/mm^2) with 5–10 pJ/s bit. Silicon photonic system design is also reviewed that will lower link energies to 300 fJ/bit, while providing multiterabits per second per square millimeter bandwidth densities. This system will ultimately provide switched optical interconnect at less than a pj (picojoule) per switched bit and computer/router system energies of tens of picojoule per bit. Progress made to date on the silicon photonic components is reviewed and analyzed an energy and bandwidth–density for future advances toward these goals.

Naida Fehratović and Slaviša Aleksić [28] described that three realizations of optically switched interconnects were analyzed regarding power consumption and scalability and compared with electronic backplane and optical point-to point options. Based on the results, it is shown that optically switched interconnects provide higher power efficiency. Optically switched interconnects dissipate less power than the two other options considered. AWG-based optically switched interconnects show the worst scalability when in band crosstalk is considered. Whereas, if the in band crosstalk is eliminated, very large switches are imaginable. It is shown that, MEMS-based interconnects are the most power efficient and scalable solution but they suffer from large switching times.

H. Wong and C. K. Wong [29] stated that silicon integrated photonics has attracted much attentions recently because of the available of silicon-based quantum devices and optical components. The successful development of Si integrated photonics will enable

on-chip optical interconnects for future microprocessors and giga-scale integrated circuits. It will be one of the major steps for next technology revolution. Technology for making micro optical waveguides based on CMOS process has been developed and several proposals were given for making Si-based light sources. This discussion reviews some attempts reported recently for making waveguide and light emitting devices based on the conventional CMOS processes. Special emphasis was given on the on-chip optical interconnects applications.

Thijs Spuesens et al. [30] analysed that as the demand for bandwidth increases, optical interconnects are coming closer to the chip. Optical interconnects on silicon-on-insulator (SOI) are desirable as this allows for integration with CMOS and the mature processing can be used for the photonic integrated circuits. A heterogeneous integration process can be used to include III-V active optical components on SOI. For dense integration compact sources and detectors are required, but they typically need different epitaxial structures to be efficient which limits the integration density. It is proposed to use an epitaxial structure, which contains both the layers for a laser and for a detector, hereby enabling very compact integration of sources and detectors. Microdisk lasers and waveguide detectors were fabricated in a 200mm CMOS pilot line and the results are discussed.

Shaloo Rakheja and Vachan Kumar [31] described that with continuous shrinking of device dimensions on chip, major advancements in intra chip interconnect technology are needed to minimize delay, energy dissipation and cross-talk. Two alternatives on chip interconnects technology options are viewed, namely the plasmonic and optical interconnects. It is shown that plasmonic interconnects can be 3 orders of magnitude faster than minimum sized CMOS interconnects at the 2016 technology node. But, their propagation length is limited to few microns and hence they can be used only as short local interconnects. Energy per bit of plasmonic interconnects is shot-noise limited and it increases exponentially as the interconnect length increases. Cross-over length beyond which plasmonic interconnects become less energy efficient compared to CMOS interconnects is calculated. It is shown that 10 micro meter for Ag cylindrical plasmonic waveguides of 100-nm diameter embedded in SiO_2 dielectric at free-space wavelength of 1 micro meter. Although plasmonic interconnects show potential as future local interconnects, plasmonic switches are needed for their implementation at the GSI (GigaScale Integration) level. Without plasmonic switches the energy and circuit overhead associated with signal conversion will be prohibitive. On the other hand, optical

interconnects are limited to be used only at the global level because of the fundamental limitations on their size. Although the native interconnect delay of optical interconnects is quite less, their bandwidth density is limited because of the fundamental limitations on the minimum pitch. Wavelength division multiplexing is identified as one of the solutions towards increasing the bandwidth density of optical interconnects. Critical length beyond which optical interconnects offer higher bandwidth as compared to copper interconnects is identified to be equal to the chip edge in absence of WDM. In presence of 4 channels WDM, the critical length improves to 0.4cm. Critical length assessment based on energy comparison with CMOS interconnect is evaluated to be 0.15cm.

N. *C.* LI et al. [32] described that the super buffer is a set of cascaded inverters, and the size of each inverter is larger than the previous one by a constant parameter. The value of this constant factor is chosen typically between three and four to minimize the overall propagation delay of the super buffer and is determined from the parameters of a minimum size transistor for a given CMOS technology. The first inverter is of minimum size, and the last inverter drives the modulator.

Osman Kibar et al. [33] investigated that the design optimization of digital free-space optoelectronic interconnections with specific goal to minimize the power dissipation of the overall link, and maximize the interconnect density is calculated. An approach of minimizing the total power dissipation of an interconnect link at a given bit rate is discussed. The impact on the link performance of two competing transmitter technologies, vertical cavity surface emitting lasers (VCSEL's) and the multiple quantum-well (MQW) modulators and their associated driver-receiver circuits including complementary metal–oxide–semiconductor (CMOS) and bipolar transmitter driver circuits, and p-n junction photo detectors with multistage transimpedance receiver circuits. Operating bitrates and on-chip power dissipation are the main performance parameters. The transmitter driver circuit is an important component in a link design, and it dissipates about the same amount of power as that of the transmitter itself.

Daniel A. Van Blerkom et al. [34] stated that optical transimpedance receivers implemented in CMOS VLSI technologies are modelled and optimized for free space optoelectronic interconnections. Analysis is done in terms of sensitivity, bandwidth, power dissipation, and circuit area for receivers using three different submicron CMOS processes. A comparison with the circuit noise limited optical power shows that, for

digital computing applications, the receiver sensitivity is limited by the gain-bandwidth product of the receiver amplifiers and the necessary noise margin of logic circuits.

D. Miller et al. [35] analysed the current performance and future demands of interconnects to and on silicon chips. Comparison is done of electrical and optical interconnects and project the requirements for optoelectronic and optical devices if optics is to solve the major problems of interconnects for future high performance silicon chips. Optics has potential benefits in interconnect density, energy, and timing over conventional technology. The necessity of the low interconnect energy imposes low limits specially on the energy of the optical output devices, with a 10 fJ/bit device energy target emerging. Some optical modulators and radical laser techniques may meet this requirement. Low (e.g., a few femto farads or less) photo detector capacitance is important. Very compact wavelength splitters are necessary for connecting the information to fibers. Dense waveguides are necessary on chip or on boards for guided wave optical approaches, especially if very high clock rates or dense wavelength-division multiplexing (WDM) is to be avoided. Free-space optics potentially can handle the essential bandwidths even without fast clocks or WDM. With such technology, however, optics may enable the continued scaling of interconnect capacity required by future chips.

J. H. Collet et al. [36] defined the marks that optoelectronic solutions will have to beat for replacing electric interconnects at chip level. The electric response of future electrical interconnects is simulated considering the reduction of the CMOS feature size λ from 0.7 to 0.05 μm. The architectural evolution of chips is also considered to analyze the latency issues. It is concluded that: 1) it does not seem necessary in the future chips to consider the integration of optical interconnects (OIs) over distances shorter than 1000–2000 λ, because the performance of electric interconnects is sufficient; 2) the penetration of OIs over distances longer than 10^4 λ could be considered (on the sole basis of the performance limitation) provided that it will be possible to demonstrate new generations of (cheap and CMOS-compatible) low-threshold high-efficiency vertical cavity surface emitting lasers (VCSELs) and ultrafast high-efficiency photodiodes; 3) the first possible application of on chip OIs is likely not for inter-block communication but for clock distribution as the energy constraints (imposed by the evolution of CMOS technology) are weaker and because the clock tree is an extremely long interconnect.

2.3 Gaps in Study

With reference to literature review, it has been observed that various advancements have been done in the area of optical interconnects but a very little work has been done that analyzes the performance impact of the challenges in optical interconnects at deep submicron technologies. In deep submicron VLSI technologies, as the package density increases, overall length of interconnects also increases, so the transmission line exhibits more delay and power dissipation. Optical interconnects are proposed as a solution to the above mentioned problems. Silicon-photonic devices still require a lot of work before they may be used for dense integration and on-chip interconnect applications. It has also been that very little work has been done at deep submicron technology. Parameters like delay and power dissipation must also be considered for its performance prediction. An analysis must be done to compare both the conventional copper interconnects and optical interconnects at various submicron technology nodes.

CHAPTER 3

COPPER INTERCONNECTS

3.1 Introduction

Since the inception of the integrated circuit manufacturing, aluminium as a conductor and silicon dioxide (SiO_2) as an insulator has been the materials of the choice. The transition from aluminium to copper as a conductor is one of the most significant changes in the semiconductor industry. From a long time manufacturers have recognised the advantages of using the copper interconnects, but considering copper only became a priority in the late 1980s as the feature size decreased. The most important benefit of using copper in the integrated circuits is that copper has low resistivity than aluminium which has been the dominant interconnects material [37]. The use of a low resistivity material like copper decreases the interconnect delay, which, in turn, increases the IC speed. The intrinsic speed limit of any integrated circuit is determined by the frequency at which its transistors can be turned on and off. Since smaller transistors have basically higher clock frequencies, advances in IC speed historically have been achieved by downward scaling of the feature sizes. The speed limit of advanced ICs is decided by the delay in signal propagation in the metal interconnect lines [37], which is determined by the time constant of the line. The time constant is the product of the resistance of the line and the capacitance between the line and all adjacent lines. RC time constant of interconnect can be reduced by reducing the resistivity of the interconnect material, using a dielectric with a low permittivity or making the line lengths as small as possible. Copper, which has a resistivity ρ of only 1.7μΩ.cm, provides almost 40% reduction in resistivity over aluminium, which has a ρ of 2.7μΩ.cm; typical aluminium alloys can have ρ as high as 3μΩ.cm. Since the RC time constant is directly proportional to the resistivity, a 40% reduction in the RC time constant can be gained by using copper rather than aluminium. By combining the copper interconnect with a dielectric material with a low permittivity, the interconnect RC delay can decrease upto 50% of that for Al/SiO_2. The interconnect RC delay can also be reduced by increasing the thickness T of the metal layer, i.e., by increasing the aspect ratio AR, or by increasing the pitch P of the line. However, when the aspect ratio is increased by increasing T, the capacitance C_L is also increased, and high aspect ratios are hard to fill uniformly; therefore, industry roadmaps predict local wiring AR <1.7 and global wiring AR < 2.2, [38]. Other advantages of using

copper include that copper has twice the thermal conductivity of aluminium and copper has ten to 100 times more resistance to electro migration failures as compared aluminium. Electro migration causes transport of the conductor material as a result of high current densities, which can eventually lead to a void in the conductor [39]. The use of copper results in power dissipation reduction of 30% at a specific frequency. By using copper rather than aluminium as an interconnect material, interconnect routing can be simplified, reducing the number of interconnect levels and resulting in fewer process steps. This is cost saving and give higher performance.

The limitations of conventional electrical interconnects has been extensively discussed during the last decade [13]. The negative aspects of these limitations are dominating. The negative aspects are wire resistance, causing delay and dispersion, and high capacitance, causing large power dissipation at large voltage swings [18]. The limitations of electrical interconnects have lead to a search for alternative techniques, such as OIs. The risk with such a situation is that new techniques are investigated; leading to too optimistic views of the new techniques.

The most important limitations of copper interconnects are considered to be delays (latency), data-rates and power dissipation. Delay and power consumption are considered here. Interesting in the present context is to compare electrical and optical solutions to some interconnect challenges. It is therefore, important to perform a fair comparison. This means that alternative solutions (OIs) should be described at the same level, for example at a fundamental limitations level, or at a practical implementation level.

3.2 Overview

In copper interconnects, repeater or buffer is basically implemented as CMOS inverter [15] as shown in fig. 3.1. In this work, for the design of CMOS inverter PMOS is assumed as thrice as NMOS. A CMOS inverter is used to derive interconnect load as shown in fig. 3.1. The CMOS inverter is the simplest buffer or repeater in VLSI interconnects. fig. 3.1 shows a CMOS buffer driving a interconnect load and its equivalent symbolic representation.

Figure 3.2 gives the equivalent RC and RLC lumped model representations of a long interconnect line. Square law models are used in which drain current changes as a square of the effective gate voltage of a long channel MOSFET, which have been used extensively for CMOS analysis. Alpha-power MOS model [40] is considered for current

voltage characteristics for short channel MOSFETs. Input waveform slope effects and parasitic drain-source resistance effects are included. The short channel CMOS inverter delay becomes less to the input waveform slope and to the V_{dd} variation as compared to the conventional MOSFETs based on the square law model.

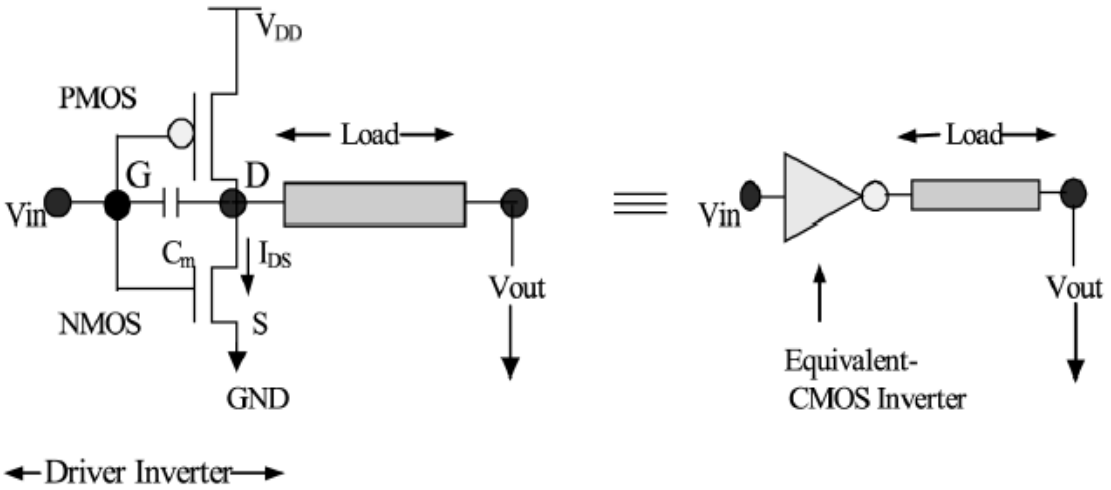

Fig. 3.1 CMOS buffer driving an interconnect load [15].

The linear resistor capacitor delay method can be used empirically to calculate the delay in digital CMOS circuits. SPICE simulation is used here to get the analytical results. A simple MOSFET model can be considered for circuit analysis, using *n*th power law for short channel devices. A comprehensive analytical [41] scheme can be used to analyse the delay of a CMOS inverter. The turn points are specified for both infinitely fast and slow input rise times and used a smooth curve fitting to predict the delay over a large range of input signal slopes and different fanouts. Analytical model [42] can be used for the short channel CMOS inverter transient and propagation delay using fast ramp and slow ramp inputs, using α-power law MOS model. The current through both the transistors and gate to drain coupling capacitance are taken into account. Interconnect load can be represented by R, L and C parameters. Its RC/RLC lumped model is shown in fig. 3.2.

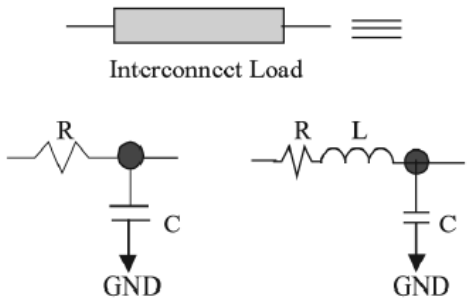

Fig. 3.2 RLC lumped model representations of an interconnect line [15].

R, L and C parameters per unit length are determined from the physical geometries of interconnects. The space between adjacent interconnects is same as interconnect width.

3.2.1 Model of global interconnect

The global interconnect design is commonly regarded as a key potential bottleneck to the advancing performance of high-speed ICs [19]. This issue has been discussed in a number of resent researches, and a lot of optimization techniques have been presented in order to achieve the optimum system performance [43]. For a given process technology and a given layer, the interconnect thickness T, the height of the metal layer from the substrate H, the width W and spacing between the signal and ground line S are the commonly used variables in the optimization of global interconnect. Analytical expressions for optimum interconnect width are developed [43] to maximize a specified figure of merit (FOM). Nevertheless, only delay and the bandwidth effects are included in the FOM. Other performance parameters such as power dissipation and area are not taken into account. Consequently, the optimization results can't ensure overall the optimum system performance. The interconnect width and spacing are optimized under two scenarios, 1) spacing is kept at its minimum value and 2) spacing is kept the same as line width, for various International Technology Roadmap for Semiconductors (ITRS) technology nodes.

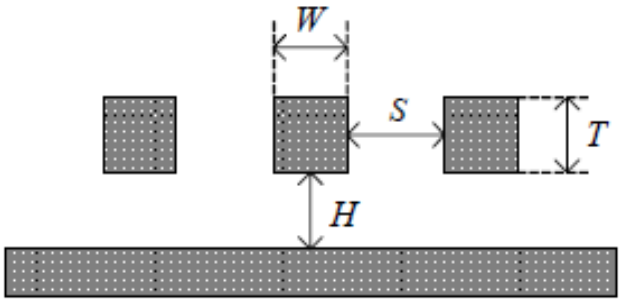

Figure 3.3 **Cross section of global interconnects [19].**

The global interconnect cross section is shown in Figure 3.3, where *W* is the interconnect width, *S* is the spacing between the neighbour interconnects, *T* is the interconnect thickness and *H* is the dielectric height.

This equivalent model can now be analysed through SPICE. Formulae used here are:

Shyh-Chyi Wong's TSM model [44]:

Resistance (R):

$$R = \frac{\rho . l}{w . t} \tag{3.1}$$

For Cu: resistivity, ρ=2.2μohm

Inductance (L):

$$L = \frac{\mu_o . l}{2\pi}\left[ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.22(w+t)}{l}\right] \quad (3.2)$$

Here, μ_o=4π×10^{-7} H/m

Capacitance (C):

C_{total} : Total capacitance of the wire

$$C_t = C_g + 2C_c \quad (3.3)$$

Here,

C_g: Area and fringe flux to the underlying plane

$$C_g = \varepsilon\left[\frac{w}{h} + 2.04\left(\frac{s}{s+0.54h}\right)^{1.77} . \left(\frac{t}{t+4.53h}\right)^{0.07}\right] \quad (3.4)$$

Here,

C_c: coupling capacitance

$$C_c = \varepsilon\left[1.41\frac{t}{s}e^{\frac{-4s}{s+8.01h}} + 2.37\left(\frac{w}{w+0.31s}\right)^{0.28} . \left(\frac{h}{h+8.96s}\right)^{0.76} . e^{\frac{-2s}{s+6h}}\right] \quad (3.5)$$

Here,

l= Length of the interconnect

ρ = Resistivity

t = Thickness of interconnect

w = Width of interconnect

h= Height of metal layer from the substrate

s = Spacing between the signal and ground line

3.3 Repeater Insertion

There is a need to minimize both the propagation delay and power dissipation in high performance VLSI circuits [17]. The increase in the load in VLSI circuits especially due to large fanouts and the long interconnects; emphasizes the need for effective driver circuits that can charge/discharge capacitances with sufficient speed, therefore, helping in delay minimization. For driving long interconnects, a single buffer is not a good solution, as they present a very large resistive-capacitive (RC) load at the terminals of the gate(s) connected to it. Instead, a number of buffers are inserted at regular intervals of distance in interconnect, which are termed as repeaters. Therefore, in long interconnects inserting

repeaters at optimally spaced points along the line reduce the delay significantly. The insertion of repeaters is used to minimize the interconnect response time by reducing the effect of resistance and capacitance. The present status and problems in CMOS repeaters in VLSI circuits taking the propagation delay and power dissipation into consideration are discussed.

Repeater insertion is generally used to reduce the delay, transition times, and the crosstalk noise of long global interconnects [19]. Analytic model to obtain the optimal repeater size and the segment length is used for a given technology node. Since a large number of repeaters are inserted to drive global interconnects for high-performance design [45], significant power will be consumed by these repeaters. Additionally, the repeaters can take up significant fraction of active silicon and routing area, which would severely reduce the wire ability of the chip.

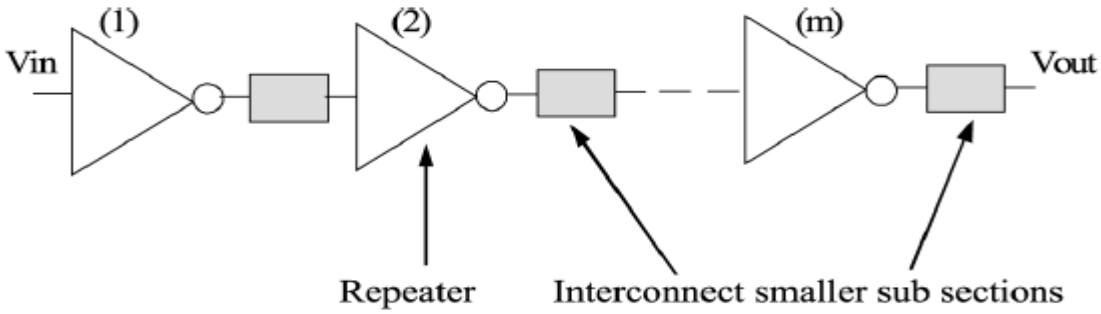

Fig. 3.4 m number of repeaters driving an interconnect divided into subsections [17].

Owing to increase in the chip complexity, number of metal layers has gone up [17]. Therefore, as a result the length of the interconnections, especially the power and the clock lines, has increased. The parasitic resistance and capacitance of interconnects increase linearly with length, resulting in high propagation delays. This increases the overall delay of the VLSI circuit. Repeaters are compatible for driving high resistive capacitive loads. Figure 3.4, shows m number of repeaters inserted in interconnects divided into subsections. As interconnect is divided into subsections, the RC constant is decreased. However, the additional delay due to repeaters has to be taken into consideration. The repeaters can be of different types :

1 uniform minimum sized;

2 optimum sized;

3 variable tapered repeaters and precharge tapered repeaters which use an extra precharge circuitry and clock for faster charging/discharging of the parasitic loads;

4 tapered cascaded buffers, containing of optimum number of repeaters in one stage, an appropriate tapering factor and the total number of such stages required for interconnect.

An electrical interconnect with repeaters can also be represented with R, L and C parameters as shown below in fig. 3.5.

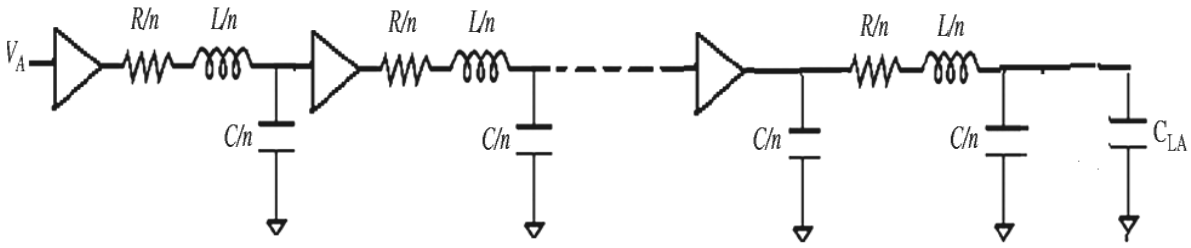

Fig. 3.5 Copper interconnects with R, L and C parameters [23].

3.4 Delay and Power Dissipation

Consider a global interconnect with resistance per unit length *r* and the capacitance per unit length *c* buffered by repeaters, as shown in Figure 3.6.

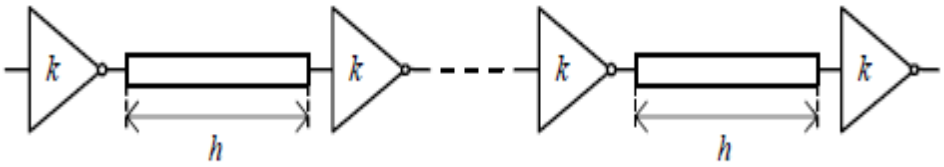

Fig. 3.6 Repeaters insertion in a long global Interconnect [19].

Assume that for a minimum sized repeater, the input capacitance is c_o, the output parasitic capacitance is c_ρ and the output resistance is r_s. Therefore, for long global interconnects with repeater insertion, if the length of line segment is *h* and the repeater size is *k*, the time constant of the segment is as following [13].

$$\tau = r_s\left(c_0 + c_p\right) + \frac{r_s}{k}ch + rhkc_0 + \frac{1}{2}rch^2 \tag{3.6}$$

The total delay of interconnect is proportional to $\frac{\tau}{h}$ which is shown below;

$$\frac{\tau}{h} = \frac{r_s}{h}\left(c_0 + c_p\right) + \frac{r_s}{k}c + rkc_0 + \frac{1}{2}rch \tag{3.7}$$

The optimal repeater size and the segment length which are

$$k_{opt} = \sqrt{\frac{r_s\, c}{r_s\, c_0}} \tag{3.8}$$

$$h_{opt} = \sqrt{\frac{2r_s\left(c_0 + c_p\right)}{rc}} \tag{3.9}$$

Therefore, the delay per unit length after optimization is given by

$$\left(\frac{\tau}{h}\right)_{opt} = 2\sqrt{r_s c_0 \frac{\rho}{T}}\left(1 + \sqrt{\frac{1}{2}\left(1 + \frac{c_p}{c_0}\right)}\right)\sqrt{\frac{c}{W}} \propto \sqrt{\frac{c(W,S)}{W}} \tag{3.10}$$

Combining equations (3.8) and (3.9);

$$\frac{k_{opt}}{h_{opt}} = c\sqrt{\frac{1}{2c_{0(c_0+c_p)}}} \propto c(W,S) \tag{3.11}$$

The delay of one segment of length h_{opt} driven by a buffer of size k_{opt} is a constant:

$$\tau_{opt} = 2r_s\left(c_0 + c_p\right)\sqrt{\left(1 + \frac{2c_0}{(c_0+c_p)}\right)} \tag{3.12}$$

When the interconnect spacing *S* is kept constant at S_{min} , increasing the width *W* will reduce $\left(\frac{\tau}{h}\right)_{opt}$ for all technology nodes.

The power dissipation per unit length for a global interconnect is as following;

$$\frac{P_{total}}{h_{opt}} = k_1\left[\frac{k_{opt}}{h_{opt}}\left(c_0 + c_p\right) + c\right] + k_2\frac{k_{opt}}{h_{opt}} + k_3\frac{k_{opt}}{h_{opt}} \tag{3.13}$$

Where

$$k_1 = \alpha V_{dd}^2 f_{clock}$$

$$k_2 = \frac{3}{2}V_{dd}I_{offn}W_{n_{min}}$$

$$k_3 = \alpha V_{dd}I_{short-circuit}W_{n_{min}}f_{clock}\tau_{opt}ln3$$

Here, V_{dd} is the power supply voltage, α is the switching factor which can be taken as 0.15, f_{clock} is the clock frequency, $I_{leakage}$ is the leakage current flowing through the repeater, I_{offn} is the leakage current per unit NMOS transistor width, $W_{n_{min}}$ is the width of the NMOS transistor in the minimum sized inverter and $I_{short-circuit}$ is the short circuit current per unit width which is approximately 65μA/μm.

Substituting equations (3.11) and (3.12) in (3.13), the power dissipation per unit length for a global interconnect is given by

$$\frac{P_{total}}{h_{opt}} \propto c(W,S_{min}) \tag{3.14}$$

CHAPTER 4

OPTICAL INTERCONNECTS

4.1 Introduction

For the long term, material innovation with traditional scaling will no longer satisfy the performance requirements. Interconnect innovation with optical, RF, or vertical integration will provide the solution. Continually shrinking feature sizes, higher clock frequencies, and growth in the complexity are all negative factors as far as switching charges on metallic interconnect is concerned. Even with the low resistance metals such as copper and low dielectric constant materials, bandwidths for long interconnect will be insufficient for future operating frequencies. Already the use of metal tracks to transport a signal over a chip has high cost in terms of power: clock distribution for instance requires a significant part (30-50%) of total chip power in high performance systems.

A promising approach to the interconnect problems is the use of an optical interconnect layer, which could empower an increase in the ratio between the data rate and power dissipation. At the same time it would enable synchronous operation within the circuit and with the other circuits, relax constraints on the thermal dissipation and sensitivity, signal interference and distortion, and also free up routing resources for complex systems [31]. However, this comes at a price. Firstly, high-speed and low-power interface circuits are required, design of which is not so easy and has a direct influence on the overall performance of OIs. Another important constraint is the fact that all fabrication steps have to be compatible with future IC technology node and also that the additional cost incurred remains affordable. Additionally, predictive design technology is required to quantify the performance gain of optical interconnect solutions, where information is less and disparate concerning not only the optical technology, but also the CMOS technologies for which optics could be used.

An on-chip optical link as in fig. 4.1 contains the following components [31]: (a) A off chip Laser source which is coupled to the modulators; (b) Optical modulator that is used to manipulate a property of light often of an optical beam such as a laser beam. Silicon optical modulators have been extensively studied; (c) an optical waveguide that can be implemented as a silicon strip waveguide or a rib waveguide for a 2-D

confinement; (d) photo-detector which generates current proportional to the incoming light intensity and (e) a transimpedance amplifier followed by gain stages.

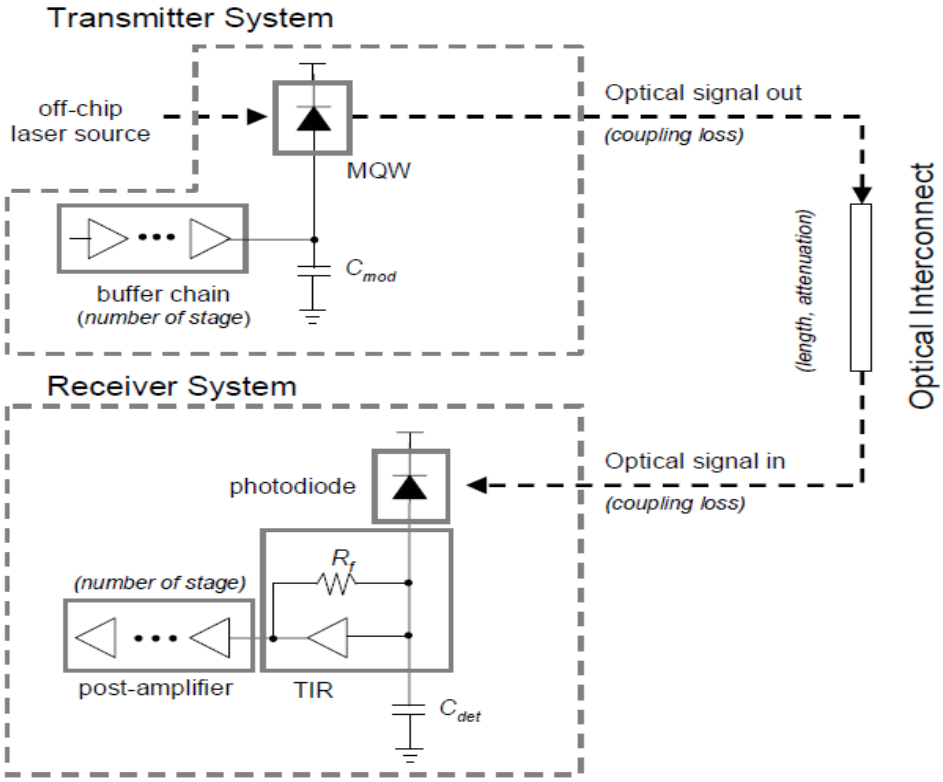

Fig. 4.1 Schematic showing high-speed optical interconnect system [24].

Optical interconnect based systems (Fig. 4.1) require a means of transforming the electrical signal to the optical domain (modulator), a waveguide to route the optical signal, and a photo detector to convert back the optical signal into an electrical signal. Other optical components such as optical amplifiers, filters, couplers and splitters are also required for a large interconnect system. Recent advances in the last few years have resulted in the development of a hybrid-silicon laser as a source of optical power; high speed silicon based electro-optic modulators based on carrier interactions [46]; Si-Ge based photo-detectors, low-loss input couplers and optical amplifiers, therefore promising the possibility of an on-chip optical communication system.

It has also been found that for global interconnect distances of typical length (~25mm), optical SOI-waveguide based interconnects [47] give better latency and power dissipation advantages than their electrical counterparts for future technologies as is summarized in the fig. 4.2. With Wave Division Multiplexing (WDM) the spatial-bandwidth for the optical interconnects is also higher than electrical interconnects. Multiple architectures have been proposed for on-chip optically connected multi-processor systems. Based on these systems architects have found the modest performance

improvement against their electrical counterparts [48]. However, most performance evaluations ignore the technological challenges that will arise out of integration, such as controlling the thermal sensitivity of optical devices.

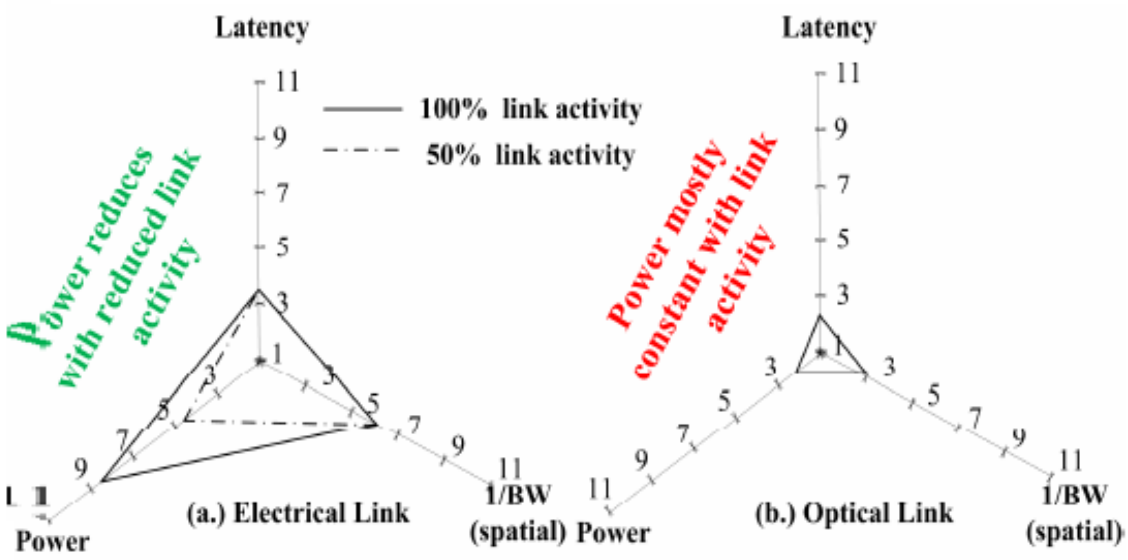

Figure 4.2 Relative latency, power and spatial bandwidth comparison chart for electrical and idealized optical link at 32nm technology node (in relative scale) (A smaller triangle means better performance) [7].

The delay of an optical link t_{opt} is given as in (4.1)

$$t_{opt} = t_{tx} + t_{wg} + t_{rx} \tag{4.1}$$

where t_{tx} is the delay of the transmitter is, t_{wg} is the delay of the waveguide and t_{rx} is the receiver delay.

4.2 Transmitter

A transmitter consists of an electro-optical modulator and a driver circuit [11]. The design of a fast and cost efficient CMOS compatible electro-optical modulator is a challenging task on the path towards realizing on-chip optical interconnects. In a modulator, conversion between electrical and optical signals is performed in two steps. First, certain optical properties of the medium (the refractive index or absorption coefficient) are changed by the electrical signals. Second, the optical signals are modulated, either in amplitude or in phase, by varying the optical properties.

Unstrained bulk crystalline silicon, unfortunately, does not have a linear Pockels effect, and refractive index changes due to the Kerr effect are very weak [49]. One of the few compatible mechanisms for varying the refractive index in pure silicon is the free carrier plasma dispersion effect [50]. There are mainly two electrical structures for changing the carrier concentration in silicon devices. The conventional approach is to

inject and deplete carriers in the intrinsic region of a p-i-n diode. With this approach, a major change in the carrier concentration can be obtained over a large volume. The speed of this structure, however, is greatly limited by the slow carrier recombination process. An alternative electrical structure is a MOS capacitor. The change in the carrier concentration is obtained by redistribution rather than injection and depletion of carriers, causing a higher modulation speed. The first MOS capacitor based electro-optical modulator was explained by Liu et al. [46] and operates at frequencies greater than one gigahertz. By design optimization and technology improvements, such as thinning the gate oxide and using an epitaxial over-growth approach, the bandwidth of the modulator is expected to increase to 30 GHz to 40 GHz by the year 2016.

The delay of the transmitter can be expressed as [31]:

$$t_{tx} = N_{opt}\, u_{opt}\, \tau_r \tag{4.2}$$

where N_{opt} is the optimum number of stages in the driver chain and is equalto $N_{opt} = ln\,(C_{mod}\,/C_o)/ln(3.6)$ where $C_o$is the input capacitance of a minimum size drive and C_{mod} is the modulator capacitance r. u_{opt} is the optimum size which is assumed to be 3.6 and τ_r is the delay of the minimum size driver.

In this section, MQW modulators and VCSEL's with their driver circuits are analysed. CMOS circuits are examined for driving both MQW modulators and VCSEL's.

4.2.1 MQW Modulators with CMOS Driver Circuits

Fig. 4.3 shows the circuit schematic of a MQW modulator driven by a CMOS superbuffer circuit. Driver circuit is a CMOS superbuffer which is used to drive the modulator. The superbuffer is basically a set of cascaded inverters. In the superbuffer size of each inverter is geater than the previous one by a constant factor β. The value of β is taken between three and four to decrease the delay of the superbuffer. Its value is determined from the parameters of a minimum size transistor for a given CMOS technology [32]. The number of stages in the transmitter driver is changed, while ensuring the propagation delay through the transmitter driver does not exceed the bit period of the link. More stages in the transmitter driver leads in a shorter rise time of the output optical signal, thus a higher maximum operating bit rate. However, these extra stages in the superbuffer, increase the power dissipation in the transmitter circuit. The optimum designs are the ones resulting in the minimum power dissipation at a given operating bit rate.

The total power dissipated in a superbuffer is given as [33]:

$$P_{sb} = C_{total\,.} V_{dd}^2 . \frac{BR}{2} \quad (4.3)$$

Where $C_{total\,.}$ is the total capacitance of the superbuffer (i.e. of *n* inverters) and *BR* is the bit rate with the units of bits/second, and the transient on-current is neglected. The total capacitance is the sum of input capicatnce and output capacitance of all the inverters and is in the form of

$$C_{total} = (C_{load} - C_{in.min}) + \sum_{k=0}^{n-1} \left(C_{in.min} + C_{out,min}\right) . \beta^k \quad (4.4)$$

Where $C_{in.min}$ and $C_{out,min}$ are the input and output capacitance of a minimum size inverter for a given CMOS technology, and C_{load} is the load capacitance of the superbuffer and contains the modulator capacitance and any parasitic capacitance as seen by the last inverter of superbuffer.

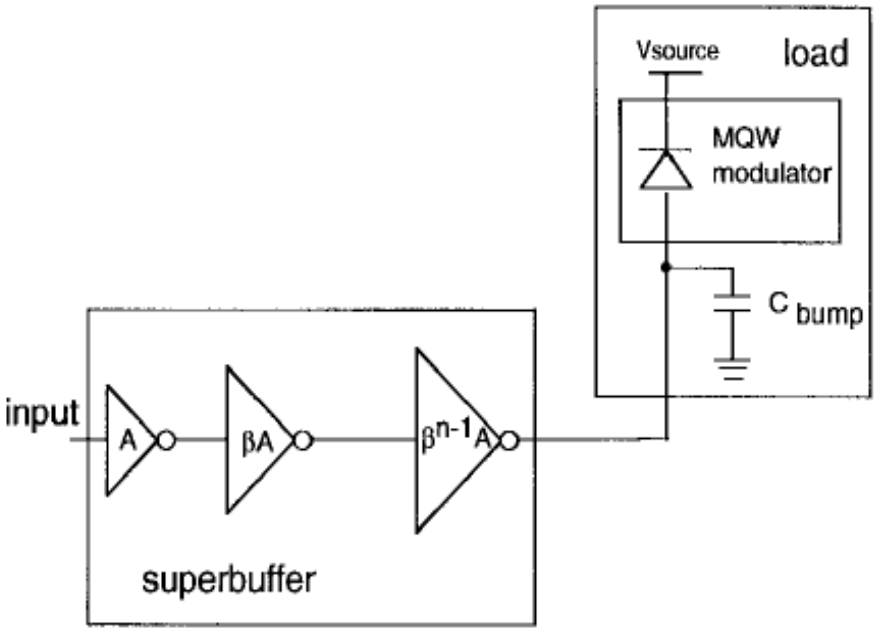

Fig. 4.3 CMOS superbuffer driving the MQW modulator [33].

In most of the cases, the modulator capacitance is small enough (10fF) that a single inverter is sufficient to drive the modulator. However, a larger superbuffer with more inverters can be conisdered to reduce the rise-time of the output optical signal, provided the total propagation delay of the superbuffer does not exceed the bit period. The fast rise time in turn decreases the power dissipation in the receiver. The cost is, however, the additional electrical power dissipation of the superbuffer circuit. In the design process, the optimum number of superbuffer stages is determined by balancing the power dissipated in the superbuffer stages and in the receiver circuit such that the total power dissipation is minimum at a given bit rate.

The minimum MQW modulator area used is 10μm*10μm with capacitance of 0.1fF/μm^2. The flip-chip bump capacitance is assumed to be 50fF, so the total bonded diode capacitance is taken to be 60fF for all CMOS feature sizes. The modulator performance is determined by its contrast ratio (CR) and insertion loss (IL) at its optimal bias voltage (V_{bias}) with a voltage swing (ΔV). The maximum voltage swing is found by the voltage supply of the driver circuit (V_{dd}).

For a MQW modulator of a contrast ratio (CR) and an insertion loss (IL), we have

$$\eta_H = IL \text{ and } \eta_L = 1 - \frac{1-IL}{CR} \tag{4.5}$$

where η_H and η_L are the absorption coefficients of the modulator for high and low states, respectively.

The voltage supply, V_{dd} determines the maximum voltage swing available at the output of superbuffer that is $\Delta V = V_{dd}$. The voltages that the modulator is at the low and the high optical output states are $V_L = V_{bias}$, and $V_H = V_L - V_{dd}$ respectively.

Given that the fan-out (F) and the link efficiency (η_{link}) of a system, the required external light power incident on the modulator is

$$P_{external} = \frac{2.F.P_{opt,rec}}{\eta_{link}(\eta_L - \eta_H)} \tag{4.6}$$

Where $P_{opt,rec}$ is the average optical power required at the detector input (i.e., one half of the required optical power swing between high and low states). Then, the average dissipated electrical power in the modulator due to the absorbed light power is simply

$$P_{diss,MQW} = P_{external} \cdot \frac{q}{h\nu} \cdot \left(\frac{\eta_H.V_H + \eta_L.V_L}{2}\right) \tag{4.7}$$

Substituting equations (4.5) and (4.6) into (4.7), and rearranging terms, we get an expression for dissipated power in the modulator in terms of the modulator parameters

$$P_{diss,MQW} = \frac{F.P_{opt,rec}}{\eta_{link}} \cdot \frac{q}{h\nu} \cdot \frac{V_{bias} \cdot \left(1 + IL - \frac{1-IL}{CR}\right) - V_{dd}.IL}{(1-IL) \cdot \left(1 - \frac{1}{CR}\right)} \tag{4.8}$$

where $P_{opt,rec}$ is the average optical power required at the receiver input, F is the system fan-out, and η_{link} is the optical system efficiency. The total power dissipation of the transmitter is the sum of the power dissipated in the modulator due to optical absorption described by equation (4.8) and the switching power of the superbuffer described by equation (4.3). The optical power in a modulator-based system is generated by an external light source, and the electrical power dissipation of the light source is thus not considered in the total on-chip power dissipation

4.2.2 VCSEL's with Driver Circuits

A typical laser driver circuit contains impedance matching circuitry at the input and the output, an adaptive stage, and an output driving stage [33]. The adaptive stage has logic circuits to reduce the overall power consumption, shift the levels of various signals, compensate for the current variations, eliminate jitter, and/or to balance the rise and fall times. The output driving stage gives the current (the threshold as well as the modulation currents) to the laser. The load contains the laser diode and a parasitic capacitance. Usually, the power dissipated in the last output stage is much greater than that in all other auxiliary circuits.

In the analysis, set the low current value of the data signal to equal the threshold current of the VCSEL. In practice, the threshold current of the VCSEL's changes across a large array, and the low current level should be approximately 10% higher [51], [52] than the mean threshold current of the array to account for the non uniformity. However, the modulation current of the VCSEL's is actually much greater than the threshold current at high bit rates, and therefore contributes more to the overall power dissipation in the link. As a result, assuming the low current value to be the mean threshold current of the array does not alter the trends of the analysis or the final conclusions, but simplifies the calculations.

Additionally, the turn-on time of the VCSEL does not limit the system bandwidth at high bit rates. The reason is that at high bit rates, the modulation current exceeds the threshold current, so the bias point of the VCSEL is well above the threshold, which decreases the turn-on time [53]. Also, the values of the modulation current and the bias current are set such that the VCSEL never operates below its threshold (i.e. the low value equals the threshold current), which makes sure that the turn-on delay time of the VCSEL can be neglected in estimating the operating bandwidth [54], [55].

4.2.2.1 VCSEL with a CMOS Driver

The output stage of the CMOS VCSEL driver circuit (Fig. 4.4) consists of two NMOS transistors (N_B and N_A) providing the threshold and the modulation currents, respectively, and a superbuffer driving the gate of N_A. The superbuffer is implemented in the same way as described previously [33].

The total electrical power dissipated in the driver and VCSEL can be divided into two parts: the power dissipation of the superbuffer given by equation (4.3), and the power dissipation of the VCSEL and the two transistors due to their current flow. The bias

transistor (N_c) can be shared by multiple drivers, its power dissipation is thus neglected in the single link calculation. The total laser current (I_{Total}) is the sum of the threshold current (I_{th}) and the average modulation current (I_m). The modulation current is supposed to have a 50% duty cycle. The source voltage (V_{Source}) is the sum of the threshold voltage (V_{th}) of the VCSEL, the voltage drop across the series resistance (R_s) when the modulation current flows, and the minimum source-drain voltage ($V_{dd} - V_{tn}$) required to make sure that the transistor (N_A) is in its saturation region. The total electrical power consumed in the VCSEL and the output stage is then

$$P_{CMOS,\ VCSEL} = I_{Total}.V_{Source} = \left[I_{th} + \frac{I_m}{2}\right].[V_{th} + R_s.I_m + (V_{dd} - V_{tn})] \quad (4.9)$$

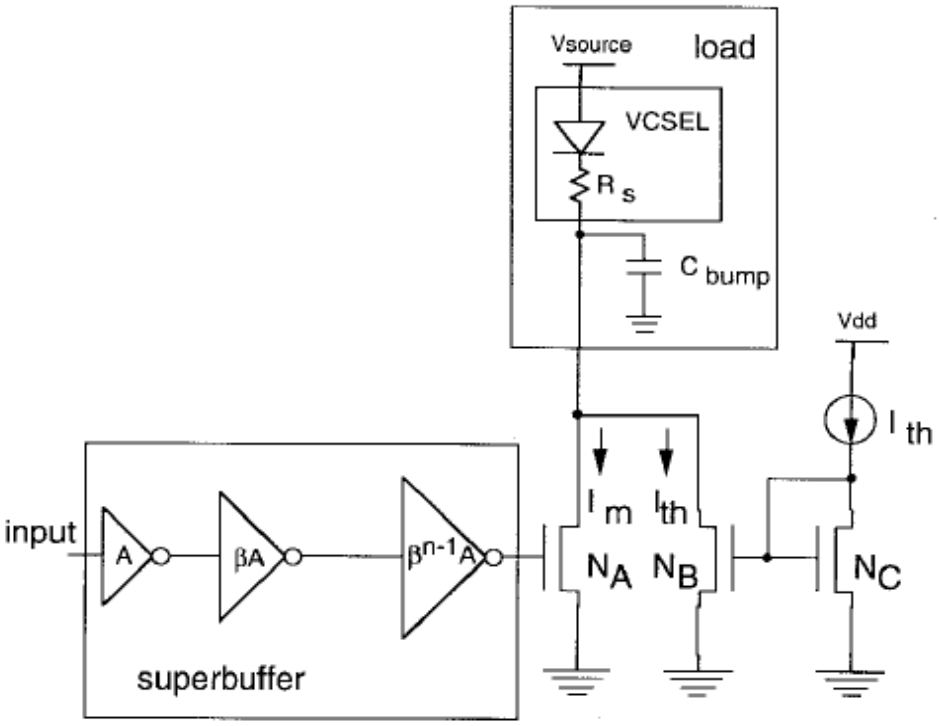

Fig. 4.4 Output driving stage of a CMOS driver connected to the VCSEL [33].

For a given laser slope efficiency (η_{LI}), the average output optical power is given as

$$P_{CMOS,\ VCSEL} = \frac{I_m\,\eta_{LI}}{2} \quad (4.10)$$

where the spontaneously emitted power at threshold is neglected. The total power dissipated in the transmitter circuit is then the sum of (4.3) and (4.9) minus the laser output from (4.10). From equation (4.9) one can see that the last term in the second parenthesis, ($V_{dd} - V_{tn}$), is completely from the driver circuit. The power dissipated in the driver circuit is equal as in the VCSEL itself using 0.5µm CMOS technology. Therefore, the power conversion efficiency, including the power dissipation of the driver circuit, decreases by about 50% compared to that when considering the VCSEL alone.

4.2.2.2 VCSEL with a Bipolar Driver

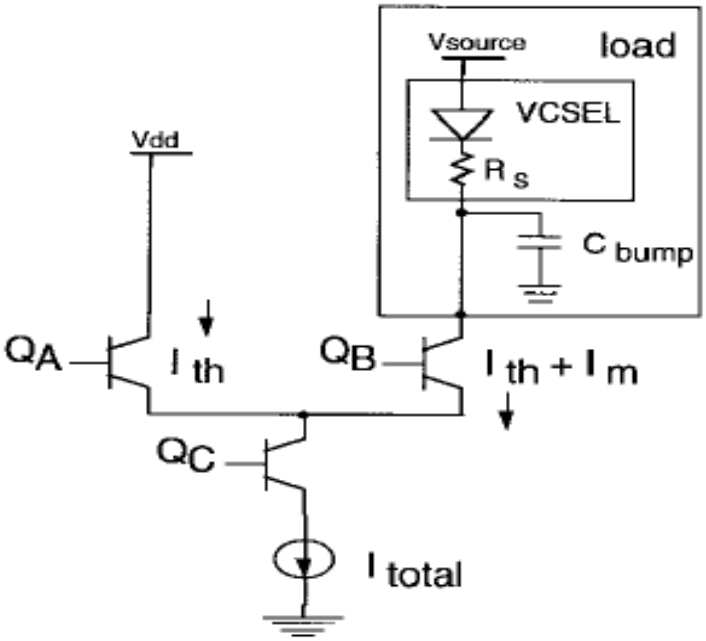

Fig. 4.5 Output driving stage of a bipolar driver connected to the VCSEL [33].

The output driving stage implemented using bipolar transistors is shown in fig. 4.5. Because of the parameter variations in bipolar technology, a differential configuration is imperative [56], [57]. The sum of the emitter currents of transistors Q_B and Q_A is fixed by joining a current source to the transistor Q_C. The partitioning of the fixed current between Q_B and Q_A is dependent on the differential voltage supplied to the bases of these two transistors. The currents in these transistors are designed such that when the threshold current (I_{th}) flows through Q_B, the current through Q_A is equal to I_{th} + I_m, and vice versa. The total current in the output driving stage is thus ($2I_{th} + I_m$). The power supply voltage for the bipolar driver circuit is the sum of the threshold voltage, the voltage drop across its series resistance, and the collector-emitter voltage (V_{ce}) across both Q_B and Q_C. For a high frequency operation, both Q_B and Q_A are generally biased in their active regions. V_{ce} is typically 1 V or higher when a BJT is in its active region. The total dissipated power is then

$$P_{bipolar\ ,VCSEL} = [2I_{th} + I_m].[V_{th} + R_s.I_m + 2V_{ce}] \quad (4.11)$$

which is almost twice as that in a CMOS driver.

4.3 Waveguide

Wavelength of the optical signal and optical material limit the performance of waveguide [11]. Although a novel waveguide like photonic crystal waveguide decreases the waveguide pitch but gives optical losses. There are two types of the waveguide

material for the operating wavelength of the signal. A silicon-on-insulator (SOI) structure is used for the applications requiring dense and short waveguide arrays because of its smaller waveguide pitch. Low loss polymers are used for longer links as they give smaller losses and optimized propagation delay [58] [59]. Area required by polymer waveguide for fabrication is larger than the area required by SOI waveguides but polymer waveguides are fabricated on an additional layer, so they do not reduce the on-chip silicon resources. Polymer waveguides have low refractive index. They have effective index of 1.4 [59].

The delay through the optical waveguide can be expressed as [31]:

$$t_{wg} = \eta_{eff} \frac{L}{c} \tag{4.12}$$

where η_{eff} is the effective refractive index of the mode in the waveguide medium, c is the speed of light in the vacuum and L is the waveguide length.

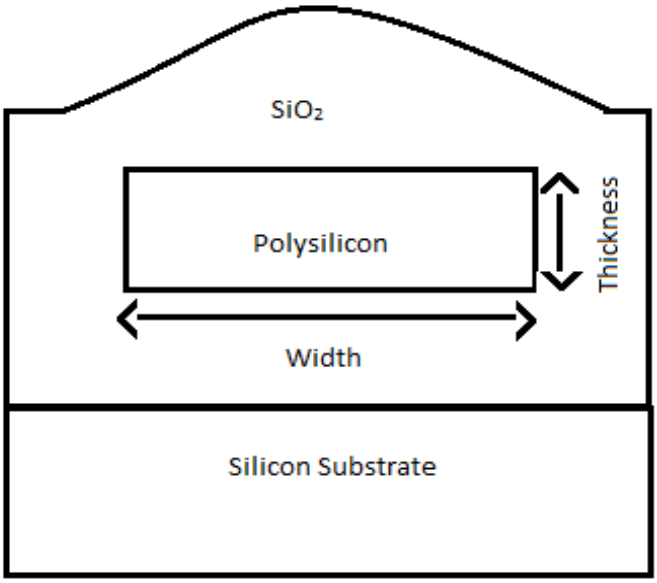

Fig. 4.6 Polysilicon Waveguide

Waveguides on the chip, as illustrated in Figure 4.6, are fabricated using Si/SiO_2. The high dielectric contrast confinement shrinks the wavelength of the light to dimensions of $\frac{\lambda}{n}$. Smaller sized devices are preferred because they provide faster optoelectronic transduction, higher local fields to drive non-linear interactions and higher levels of integration which gives new functionality at lower costs [31]. The variation in waveguide dimensions results in skews at different branches.

4.4 Optical Receiver

In this analysis, the receivers considered are mainly of the transimpedance type due to their high bandwidth, low noise, and ease of biasing [60], [61].

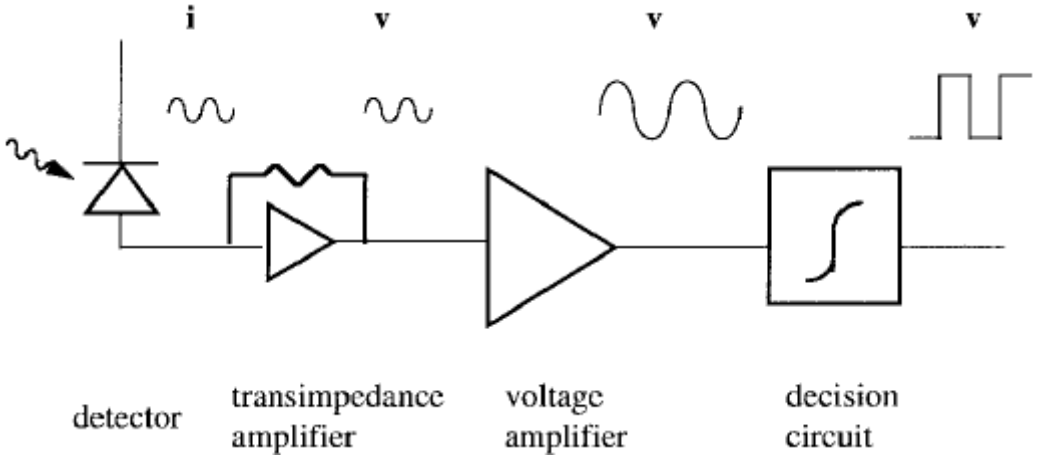

Fig. 4.7. Block diagram of a receiver circuit [33].

The operational model of a transimpedance receiver can be divided into four components (Fig. 4.7) which are; the detector, the transimpedance amplifier, the voltage amplifier, and the decision circuit. The detector generates the photo-current based on an optical signal, and an MQW photodetector with a 60-fF total capacitance (including the diode and the bump capacitance) is supposed. Decreasing the photo detector capacitance increases the optical to electrical conversion efficiency for the receiver, and improves the overall link performance [62], but the improvement is not dependent on the transmitter used in the system, so in analysis, it can be kept as a constant as scale down the CMOS technology, and compare the two transmitter technologies for the given receiver circuits. TIA (the transimpedance amplifier) converts the photocurrent from the detector to an analog voltage. After that voltage is amplified by the voltage amplifier to match the input requirements of the decision circuit. The decision circuit gives a digital voltage output to the following computational logic circuits.

The optimization objective is to reduce the total optical link power dissipation, including the receiver TIA and LA stages, transmitter pre driver and driver circuits. Transimpedance amplifier based receiver architecture is shown in fig. 4.8. It shows CMOS circuit of transimpedance amplifier and voltage amplifiers.

There are many different types of photo detectors such as the photodiodes with a p-n or a p-i-n structure, M-S-M photo detectors, avalanche photo detectors and photo multipliers. The M-S-M photo detector has the fastest response and good quantum efficiency. The response time of the M-S-M photo detector is dependent on the carrier

transit time and the RC charging time of the detector capacitance. Thus the response time is given as [8]:

$$T_{r=}(\tau_{tr}^2 + \tau_{RC}^2)^{1/2} \quad (4.13)$$

$$tr = \frac{X}{v} \quad (4.14)$$

$$\tau_{RC} = 2.2RC \quad (4.15)$$

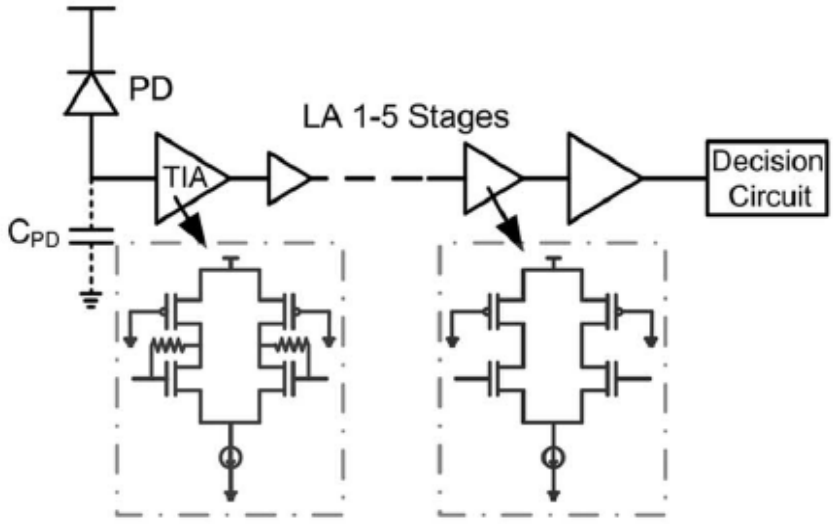

Fig. 4.8 Transimpedance amplifier based receiver architecture [25].

where *v* is the carrier drift velocity and *X* is the drift distance covered by the carriers. τ_{RC} is the time needed for the photo generated carriers to drift to the electrical contact, and τ_{RC} is the RC response time of the detector. The delay of the M-S-M photo detector can be expressed as [8]:

$$T_D = 0{:}315T_r \quad (4.16)$$

The limiting factor in the delay of photo detectors is in the carrier transit time [8]. The response time of the photo detector decreases as the electrode is made smaller in area. However, there is an optimum area at which the response time of the detector is minimum [8]. The reason for this is that when the electrode is too narrow then the response time is mainly dominated by RC and when it is too wide the response time is dominated by the transit time.

The transimpedance amplifier (TIA) is required in order to amplify the photo current signal produced by the photo detector before the signal is fed into the digital gates. Therefore, the optical link delay must incorporate the delay of the TIA. The delay of the TIA is calculated by supposing that the system is a one-pole system and hence the delay is approximated as per [63]:

$$T_D = \frac{0.693}{2\pi\Delta f} \tag{4.17}$$

where Δf is the bandwidth requirement. Thus the overall delay associated with the optical receiver using equations (4.16) and (4.17) is:

$$t_{rx} = 0.315\sqrt{(2.2RC)^2 + (X/v)^2} + \frac{0.693}{2\pi\Delta f} \tag{4.18}$$

The receiver designs considered are based on the CMOS current-source inverters. For a given CMOS technology, the design of the receiver provides the receiver rise/fall time ($t\Gamma_{rec}$), the needed average optical power at the detector ($P_{opt,rec}$), and the electrical power dissipation in the receiver ($P_{elec,rec}$). The design parameters are the number of stages in the TIA (s) and in the voltage amplifier (p) and the widths and bias gate-source voltages (w and v) of the amplifying transistors. The complete analysis of these circuits and the derivations of the analytical models are explained in [34].

The maximum bit rate of the receiver circuit can be found by placing requirements on the pulse shape of the output signal. The rise and fall time of the output pulse are set to be a certain fraction of the bit period to ensure a reasonable bit error rate. The maximum bit rate can then be expressed as

$$BR = \frac{\zeta}{\sqrt{t\Gamma_{in}^2 + t\Gamma_{rec}(s,p,w,v)^2}} \tag{4.19}$$

where $t\Gamma_{in}$ is the rise time of the optical input signal (as determined by the transmitter driver), and $t\Gamma_{rec}$ is the rise time of the receiver amplifiers and is a function of the design parameters. The diffusion capacitance associated with the forward-biased VCSEL p-n junction in determining the rise time of the optical signal can be neglected, because the diffusion capacitance is much smaller than the VCSEL driver output capacitance and reduces as with $w^{-1/2}$ increasing frequency [64], [65].

The average optical power swing required at the detector can be given as

$$P_{opt} = \frac{V_{dd}}{2.A_{dc}.R_{pd}.[A_v(w,v)]p.Z_f(s,w,v)} \tag{4.20}$$

where A_{dc} is the gain of the decision circuit, R_{pd} is the responsivity of detector, A_v is the gain of the voltage amplification stages, and Z_f is the transimpedance of the transimpedance amplifier. The transimpedance is determined by finding the feedback resistor that provides a flat magnitude response from the transimpedance amplifier. The needed optical power at the detector is related to the optical power output from the transmitter by an efficiency (η_{link}) of the optical system between them and the transmitter

fan-out (F), i.e., $FP_{opt,rec} = \eta_{link} P_{opt,trans}$. The electrical power dissipated in the receiver is given as

$$P_{elec.rec} = (s + p).I_{ds}(w, v).V_{dd} \tag{4.21}$$

where I_{ds} is the bias current and is dependent on the parameters w and v. Therefore, the number of stages in the amplifiers, and the width and bias voltage of the amplifying transistors calculate the optical power requirement and power dissipation of the receiver. However, the bit rate of the receiver is not only determined from these parameters; but it is also a function of the rise time of the input optical signal.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 R, L and C Parameters of Copper Interconnects

Interconnect load can be represented by R, L and C parameters. R, L and C parameters are determined from the physical geometries of interconnects. For a given process technology and a given layer, the interconnect thickness T, the height of the metal layer from the substrate H, the width W and spacing between the signal and ground line S are the commonly used variables in the optimization of global interconnect. Consequently, the optimization results can't ensure the optimum system performance in whole. The interconnect width and spacing are optimized under two scenarios, 1) spacing kept at its minimum value and 2) spacing kept the same as line width, for various International Technology Roadmap for Semiconductors (ITRS) technology nodes. Width and space are kept same. Various parameters w, s, t, h and dielectric constant k are shown below in table 5.1 for various technology nodes.

Table 5.1: Technology and equivalent circuit model parameters for top layer metal for different technology node Based on the ITRS.

Technology nodes	width(µm)	space(µm)	thickness(µm)	height(µm)	Dielectric const. k	length(µm)
90nm	0.50	0.50	1.20	0.30	2.8	10000
65nm	0.45	0.45	1.20	0.20	2.2	10000
32nm	0.048	0.048	0.144	0.1104	2.25	10000
22nm	0.032	0.032	0.096	0.0768	2.05	10000
14nm	0.024	0.024	0.072	0.0528	1.95	10000

Now based upon the values given in table 5.1 R, L and C parameters using Shyh-Chyi Wong's TSM model are calculated. Parameters are calculated for different technology nodes for different numbers of repeaters as shown in tables below. Values of R, L and C parameters are calculated for technology nodes 90nm, 65nm, 32nm, 22nm and 14nm. If R, L and C are the values for one repeater, then for n number of repeaters it will be $\frac{R}{n}$, $\frac{L}{n}$ and $\frac{C}{n}$. .

Table 5.2: R, L and C parameters for 90nm technology.

No. of Repeaters	R(ohm)	L(nH)	C(fF)
1 R	366.67	19.55	2596.72
3 R	122.2	6.51	865.57
5 R	73.33	3.91	519.34
7 R	52.38	2.79	370.96
9 R	40.74	2.17	288.52

Table 5.3: R, L and C parameters for 65nm technology.

No. of Repeaters	R(ohm)	L(nH)	C(fF)
1 R	407.41	19.81	2284.75
3 R	135.80	6.60	761.58
5 R	81.48	3.96	456.95
7 R	58.20	2.83	326.39
9 R	45.26	2.20	253.86

Table 5.4: R, L and C parameters for 32nm technology.

No. of Repeaters	R(ohm)	L(nH)	C(fF)
1 R	31.83k	24.11	202.27
3 R	10.61k	8.04	67.42
5 R	6.37k	4.82	40.45
7 R	4.55k	3.44	28.89
9 R	3.54k	2.68	22.47

Table 5.5: R, L and C parameters for 22nm technology.

No. of Repeaters	R(ohm)	L(nH)	C(fF)
1 R	71.61k	24.91	176.61
3 R	23.87k	8.31	58.87
5 R	14.32k	4.98	35.32
7 R	10.23k	3.56	25.23
9 R	7.96k	2.76	19.62

Table 5.6: R, L and C parameters for 14nm technology.

No. of Repeaters	R(ohm)	L(nH)	C(fF)
1 R	90.56k	26.61	156.38
3 R	30.18k	8.87	52.12
5 R	18.11k	5.32	31.27
7 R	12.94k	3.80	22.34
9 R	10.06k	2.95	17.37

These values of R, Land C parameters are used for interconnect load with CMOS inverter as per the number of repeaters, then delay and power dissipation for different technology nodes are simulated using SPICE simulation.

5.2 Delay

Delay uncertainty is caused by geometric process variations and environmental changes. Variations in the environment include power/ground noise, temperature fluctuations, and crosstalk coupling. Delay due to environmental changes is not considered here. The delay uncertainty of the optical interconnect is expected to be lower in future technology nodes. The delay uncertainty of the conventional copper interconnect, in contrast, is expected to slowly increase in future technology nodes due to the larger number of inserted repeaters. For copper interconnects simulation is done for delay at for different numbers of repeaters and optimum results are shown here. The optimal number and size of repeaters along an RLC interconnect can be determined to achieve the minimum delay. Delay of the waveguide is taken as the propagation delay of the signal through it which is same for all technology nodes. The delay of each individual part of the transmitter and receiver of optical interconnects is simulated using SPICE simulation. Delay of copper and optical interconnects is simulated at different technology nodes for different time period (i.e. at different frequencies). As the time period increases, frequency decreases, therefore, delay of the optical and copper interconnects also increases. Delay of optical and copper interconnects is shown in table 5.7 at 34MHz.

Table 5.7: Delay (ps) distribution in a 1 cm optical data path as compared with the copper interconnects delay at 34MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 nm
Modulator driver	79.6	70.6	55.3	50.3	38.6
Modulator	67.3	59.3	47.6	38.6	30.6
Detector	18.2	14.2	12.2	11.3	9.6
Receiver amplifier	76.3	65.1	51.4	42.3	29.4
Waveguide	48.3	48.3	48.3	48.3	48.3
Total optical	289.7	257.5	214.8	190.8	156.5
Copper	1610	1720	2090	2510	2740

Table 5.8: Delay (ps) distribution in a 1 cm optical data path as compared with the copper interconnects delay at 50MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 nm
Modulator driver	74.6	64.8	47.8	44.8	32.2
Modulator	60.3	50.2	41.5	32.6	25.3
Detector	13.3	10.6	8.8	7.6	5.6
Receiver amplifier	70.5	60.1	47.3	37.3	25.1
Waveguide	48.3	48.3	48.3	48.3	48.3
Total optical	267	234	193.7	170.6	136.5
Copper	1300	1460	1750	2140	2380

Table 5.9: Delay (ps) distribution in a 1 cm optical data path as compared with the copper interconnects delay at 67MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 nm
Modulator driver	71.3	58.6	45.9	40.2	25.8
Modulator	57.6	46.3	39.6	30.1	22.3
Detector	10.3	8.9	7.6	6.3	3.6
Receiver amplifier	67.8	57.8	45.3	33.6	23.9
Waveguide	48.3	48.3	48.3	48.3	48.3
Total optical	255.3	219.9	186.7	158.5	129.9
Copper	1120	1250	1510	1960	2150

It is clear that delay increases as the frequency decrease. Optimum results are obtained at 100MHz. The results of delay of the transmitter for optical interconnects are shown in table 5.10.

Table 5.10: Delay (ps) distribution of Transmitter in Optical interconnect system at 100MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 Nm
Modulator driver	68.3	54.9	42.5	36.1	23.6
Modulator	54.4	43.3	36.5	27.5	20.2
Total for Transmitter	122.7	98.2	79.0	63.6	43.8

Fig. 5.1 shows the performance of the transmitter of the optical interconnects at different technology nodes.

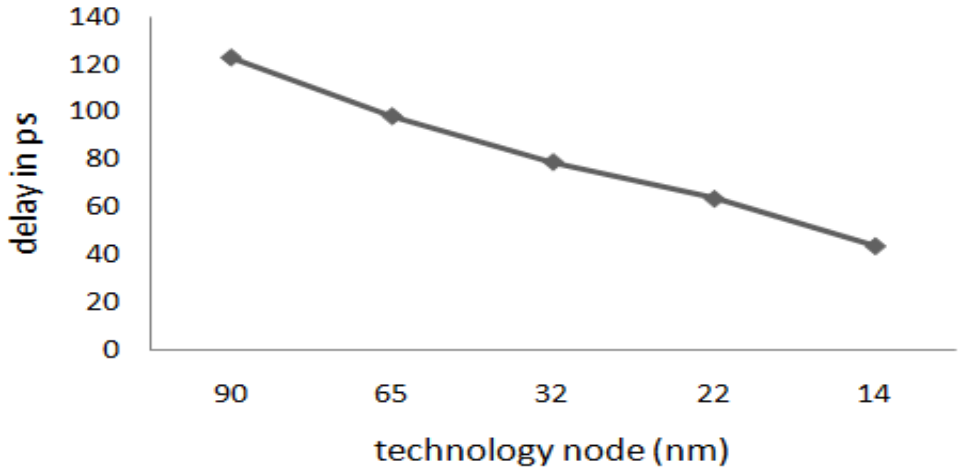

Fig. 5.1 Transmitter delay with respect to technology node.

The results of delay of the receiver of the optical interconnect for various technology nodes are shown in table 5.11 at 100MHz.

Table 5.11: Delay (ps) distribution of Receiver in Optical interconnect system at 100MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 Nm
Detector	8.2	6.9	4.2	3.1	1.9
Receiver amplifier	65.6	55.3	42.8	32.7	21.4
Total for Receiver	73.8	62.2	46.0	35.8	23.3

Delay of receiver of the optical interconnects also changes as technology is scaled. Fig. 5.2 shows the performance of the receiver of the optical interconnects at different technology nodes.

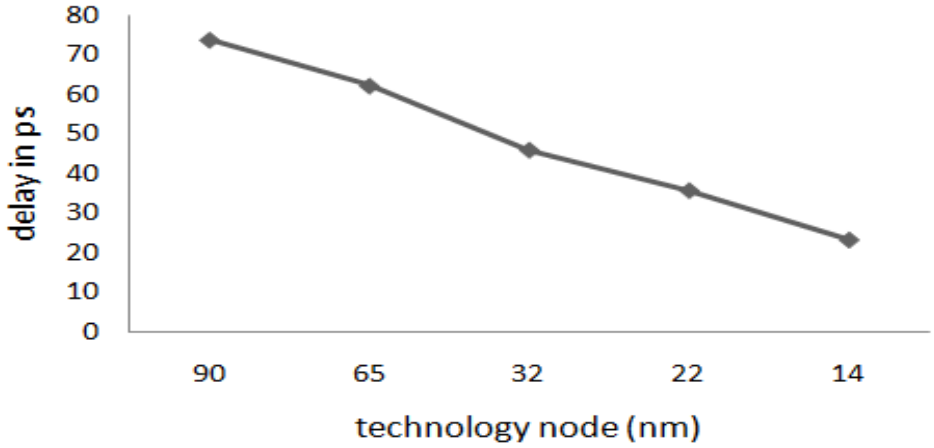

Fig. 5.2 Receiver delay with respect to technology node.

Performance of optical interconnects and copper interconnects with respect to delay for different technology nodes at 100MHz is shown in table 5.12.

Table 5.12: Delay (ps) distribution in a 1 cm optical data path as compared with the copper interconnects delay at 100MHz.

Technology node	90 nm	65 nm	32 nm	22 nm	14 nm
Transmitter	122.7	98.2	79.0	63.6	43.8
Receiver	73.8	62.2	46.0	35.8	23.3
Waveguide	48.3	48.3	48.3	48.3	48.3
Total optical	244.8	208.7	173.3	147.7	115.4
Copper	980	1150	1430	1840	2050

Fig. 5.3 shows the performance comparison of optical interconnects and copper interconnects at different technology nodes.

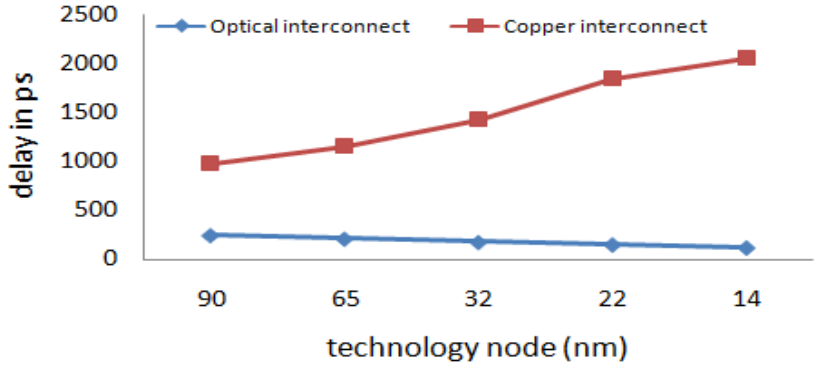

Fig. 5.3 Delay comparison between Optical interconnects and Copper interconnects.

It is clear from the results that optical interconnects give better results as compared to copper interconnects in terms of delay . Delay of optical interconnects decreases with future technology nodes whereas, delay of copper interconnects decreases.

5.3 Power Dissipation

For electrical interconnects, the power should be evaluated under specific design requirements, such as delay and bandwidth. A minimum sized wire without repeaters consumes minimum power, however, this configuration is not practical for global interconnect due to the significant delay and low bandwidth of the line. Due to small length optical power loss in the waveguide is negligible. In this work, only electrical power is evaluated for the optical interconnects. The power consumed by the transmitter dominates the power of the receiver. Both the electrical and optical interconnect power increases with future technology nodes due to higher clock frequencies and greater leakage current. Simulation is done for the power dissipation for both type of interconnects at various technology nodes for different time periods (i.e. at different frequencies). Power dissipation for both optical and electrical interconnects at 100MHz is shown in table 5.13.

Table 5.13: Power dissipation (mw) in 1cm optical data path as compared with the copper interconnects power dissipation at 100MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 nm
Transmitter	0.8	1.4	3.8	7.2	9.1
Receiver	0.5	1.1	2.4	4.3	5.7
Total optical	1.3	2.5	6.2	11.5	14.8
Copper	2.8	4.6	10.8	18.3	24.3

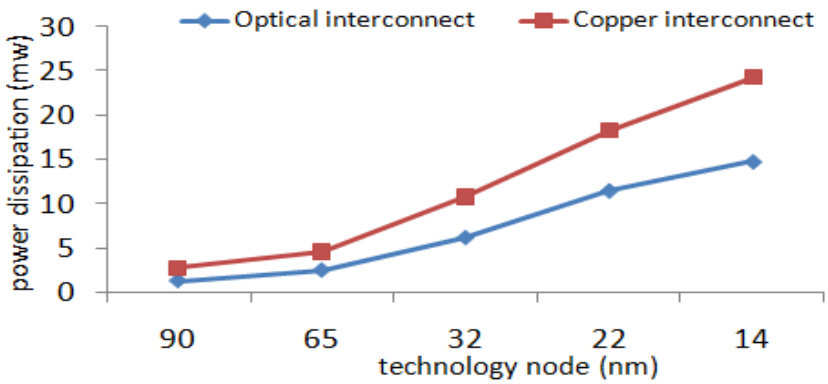

Fig. 5.4 Comparison between Optical interconnects and Copper interconnects in terms of power dissipation.

Fig. 5.4 shows the performance comparison of optical interconnects and copper interconnects in terms of power dissipation at different technology nodes. Optical interconnects consume less power as compared to copper interconnects at each technology node.

Table 5.14: Power dissipation (mw) in 1cm optical data path as compared with the copper interconnects power dissipation at 67MHz.

Technology node	90 nm	65 Nm	32 nm	22 nm	14 nm
Transmitter	0.1	0.6	1.3	2.3	5.6
Receiver	0.06	0.3	0.9	1.3	2.8
Total optical	0.16	0.9	2.2	4.6	8.4
Copper	0.8	2.4	4.9	10.9	15.8

Table 5.15: Power dissipation (mw) in 1cm optical data path as compared with the copper interconnects power dissipation at 50MHz.

Technology node	90 nm	65 nm	32 nm	22 nm	14 nm
Transmitter	0.06	0.1	0.5	1.2	2.3
Receiver	0.004	0.08	0.1	0.9	1.3
Total optical	0.064	0.18	0.6	2.1	3.6
Copper	0.09	1.1	2.3	5.3	9.6

Table 5.16: Power dissipation (mw) in 1cm optical data path as compared with the copper interconnects power dissipation at 34MHz.

Technology node	90 nm	65 nm	32 nm	22 nm	14 nm
Transmitter	0.004	0.008	0.08	0.1	0.9
Receiver	0.0009	0.007	0.03	0.07	0.09
Total optical	0.0049	0.015	0.09	0.17	0.99
Copper	0.008	0.05	0.6	1.3	2.7

Power dissipation of both type of interconnects increases with future technology nodes because of higher clock frequency and leakage current. Power dissipation of optical and copper interconnects decreases as the frequency decreases. Optical interconnects give better performance in terms of power also as compared to conventional copper interconnects.

CHAPTER 6

CONCLUSION and FUTURE SCOPE

6.1 Conclusion

In this thesis, the performance characteristics of future CMOS compatible optoelectronics devices are predicted. Based on this prediction, electrical and optical on-chip interconnects are compared for various design criteria at different technology nodes. The performance comparison between optical and copper interconnects is done in terms of delay and power dissipation. For performance comparison delay and power dissipation are simulated for both type of interconnects at various technology nodes. SPICE simulation tool is used for delay and power dissipation simulation. Delay and Power dissipation are simulated at 90nm, 65nm, 32nm, 22nm and 14nm technology nodes. For minimization of delay in copper interconnects repeaters are inserted. Delay and power dissipation are simulated for each individual part of the transmitter and receiver in an optical interconnect system.

The aim of repeater insertion is to optimize the delay performance of interconnects. In optical interconnects, in the transmitter section, driver circuit (super buffer) is used to derive electro-optical modulator. Number of stages in the super buffer is chosen to optimize the performance of the driver circuit. In the super buffer size of each inverter is larger than the previous one by a constant value β. The value of β is chosen between three and four to reduce the delay of the super buffer. In the receiver section, transimpedance type amplifier is used. Comparing the delay between the optical and copper interconnect for varying time period (i.e. at varying frequencies) and fixed interconnect length 1cm (at global interconnect level) shows that optical interconnects give better performance than copper interconnects. Delay of optical interconnects decreases with future technology nodes whereas delay of conventional copper interconnects increases. Delay of both type of interconnects increases as the frequency decreases.

Power dissipation simulation is also done for optical and copper interconnects at different technology nodes at global interconnect level. In the contrast to delay, as the technology is scaled down, power dissipation increases for both type of interconnects because of higher clock frequency and leakage current. In optical interconnects, the power consumed by the transmitter dominates the power of the receiver. Due to small

length optical power loss in the waveguide is negligible. Optical interconnects give better performance in terms of power dissipation compared to copper interconnects at each technology node.

6.1 Future Scope

Future work can be implemented in areas such as the circuitry, the optoelectronic device, and integration. Noise immunity, crosstalk and variation effects must be considered in designing the circuitry. Some power saving techniques must be considered. In these techniques supply voltage is also reduced. Various improvements can be made in the receiver circuitry. A redesign of the silicon detector is required. Silicon-photonic devices still require a lot of work before they may be used for dense integration and on-chip interconnect applications. In case of integration of integration two aspects must be considered, one containing waveguides, silicon detector and receivers on a single chip, the other containing VCSEL arrays on chip together with the receivers. These solutions can speed up the insertion of optical interconnect for shorter distance applications. Very little work has been done at 14nm technology. Parameters like bandwidth density and area must also be considered for its performance prediction.

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