Reliability Issues and their Analysis on FD-SOI Standard Cell Library

A Thesis submitted in partial fulfillment of the requirement for the Award of the Degree of

MASTER OF TECHNOLOGY

in VLSI Design

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DECLARATION

I, Aditi Negi hereby declare that the work presented in this project **"Reliability Issues and their Analysis on FD-SOI Standard Cell Library"** in partial fulfillment of the requirement for the award of degree of **Master of Technology (VLSI Design)** submitted at **Electronics and Communication department**, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Rajneesh Sharma (Assistant Professor, ECED, TIET)** and **Mr. Rajnish Garg/External Supervisor (Manager, Characterization and CAD view generation, STMicroelectronics)** from June 2018 to May 2019. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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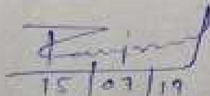

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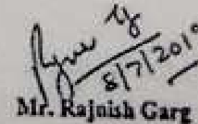

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This is to certify that **Aditi Negi** (Regn.No.601762001), a student of M.Tech (VLSI Design), **Thapar Institute of Engineering & Technology (Deemed to be University), Patiala** has successfully completed one year (June 2018 –May 2019) internship program in **STMicroelectronics INDIA PVT.LTD Greater Noida.** Her tittle of dissertation is **"Reliability Issues and their Analysis on FD-SOI Standard Cell Library".**

During the period of her internship program, she was punctual and hardworking. I wish her every success in life.

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ABSTRACT

The semiconductor industry has made extraordinary advancement in the fields of research and innovation. The ever increasing customer demands have greatly challenged the semiconductor business. The semiconductor industry needs to meet the PPA (performance, power and area) requirements along with fulfilling the speed and cost requirements. To meet the standards, technology (transistor geometries) have been scaled down tremendously. Transistor architectures used over the last couple of decades like the "Bulk technology" at around 20nm have been scaled down to their last feasible physical limits. Scaling the bulk technology beyond this limit hindered the proper functioning of the transistors due to overlapping of electric fields. Therefore, it was not practical to manufacture an economically and functionally feasible transistor beyond 20nm. New technologies like FINFET and FD-SOI make the transistors better in terms of functionality and performance. However, they still suffer from reliability issues which need proper attention. This work therefore analyzes the impact of two such unreliability issues namely Bias temperature instability and Hot carrier injection effects on standard library cells. Together these phenomena are termed as ageing phenomena and the degradation caused due to these phenomena is known as ageing. The work also focuses on the asymmetric impact of these effects on the cell's/gate's rise and fall delays. Also the individual impact of BTI and HCI is studied and the increase in the threshold voltage of PFET and NFET is calculated. The work also investigates channel length dependency of the above mentioned effects. Finally, we observe the asymmetric impact of ageing where BTI individually in comparison to HCI leads to more degradation in delay. Also the threshold voltage of NFET's and PFET's see a significant increase in the values. Therefore, this study will be of help to the designers to understand the issues in reliability, the shift in transistor parameters which may lead to violation of timings and help designers decide the exact design margins by considering ageing during designing.

Keywords: BTI, HCI, Standard cell library, FD-SOI, Reliability

TABLE OF CONTENTS

ACKNOWLEDGMENT .... **IV**

ABSTRACT .... **V**

TABLE OF CONTENTS .... **VI**

LIST OF FIGURES .... **VIII**

LIST OF TABLES .... **X**

LIST OF ABBREVIATIONS .... **XI**

1 INTRODUCTION **12**

1.1 INTRODUCTION TO UNRELIABILITY 12

1.2 OVERVIEW OF RELIABILITY ISSUES 12

1.2.1 Failure Mechanisms *13*

1.3 SPATIAL RELIABILITY ISSUES 14

1.4 TEMPORAL RELIABILITY ISSUES 17

1.4.1 Hot Carrier Injection (HCI) *17*

1.4.2 Bias Temperature Instability (BTI) *19*

1.5 INTRODUCTION TO FD-SOI 21

1.6 INTRODUCTION TO STANDARD CELL LIBRARY 24

1.6.1 Standard Cells representation – Views *25*

1.7 INTRODUCTION TO SIMULATION 27

1.7.1 Reliability Simulation *27*

1.7.2 Reliability simulation – STMicroelectronics *28*

2 LITERATURE REVIEW **30**

3 PROBLEM STATEMENT **38**

4 IMPLEMENTATION AND RESULTS **41**

4.1 METHODOLOGY 41
4.2 AGEING – NEGATIVE IMPACT 45
4.2.1 Threshold Voltage shift due to ageing effect 45
4.2.2 Asymmetric impact of ageing effects 47
4.2.3 Individual Vs Combined impact of BTI and HCI 48
4.2.4 Channel length dependency of ageing 51
4.2.5 Drive strength dependency of ageing impacts 53
4.2.6 Input slew and output load dependency of ageing effects 54
4.3 AGEING – POSITIVE IMPACT 57
4.4 AGEING MITIGATION 58
5 CONCLUSION AND FUTURE SCOPE 60
REFERENCES 61

LIST OF FIGURES

Figure 1-1 Reliability issues in MOSFET 13

Figure 1-2 Lithography Setup 16

Figure 1-3 Hot carrier Injection (CHE) 18

Figure 1-4 Drain avalanche hot carrier injection 18

Figure 1-5 Representation of the dangling bonds at the body-dielectric 20

Figure 1-6 Structure of UTBB FD-SOI device 22

Figure 1-7 Basic design flow 24

Figure 1-8 Basic standard cell library composition 25

Figure 1-9 Basic views - cell representation 26

Figure 1-10 Reliability simulation – STMicroelectronics 29

Figure 3-1 Bathtub curve - representation of failure rate in semiconductor devices 38

Figure 4-1 28nm FD-SOI Standard cell libraries provided by STMicroelectronics 42

Figure 4-2 High performance Vs High density libraries 43

Figure 4-3 Shift in the threshold voltage values of PFET and NFET due to ageing 46

Figure 4-4 Asymmetric ageing impact on NOR cells of standard cell library 47

Figure 4-5 Asymmetric ageing impact on NAND cells of standard cell library 48

Figure 4-6 Channel length dependency of ageing for a standard cell (NOR) of 28nm FDSOI standard cell library 52

Figure 4-7 Channel length dependency of ageing for all cells of 28nm FDSOI standard cell..library 53

Figure 4-8 Ageing impact variation with respect to cell drive strength - NOR cell 53

Figure 4-9 Drive strength affecting percentage delay degradation of aged cells (in comparison to fresh cells) in a 28nm FDOI standard cell library 54

Figure 4-10 Dependency of ageing impact on slew – observed for cell rise 55

Figure 4-11 Dependency of ageing impact on slew - observed for cell fall 55

Figure 4-12 Dependency of aging impact on output load - observed for cell rise 56

FIGURE 4-13 DEPENDENCY OF AGEING IMPACT ON OUTPUT LOAD - OBSERVED FOR CELL FALL 56

FIGURE 4-14 IMPACT OF AGEING ON DIFFERENT COMPONENTS OF POWER - NOR CELL 57

FIGURE 4-15 A TREND OF %AGE DECREASE IN POWER OF AGED CELLS OVER VARYING PB VALUES............. 58

FIGURE 4-16 TRANSISTOR SIZING – LESSENING THE IMPACT OF AGEING 59

LIST OF TABLES

TABLE 1-1 CATEGORIES OF TRANSISTOR RELIABILITY ISSUES 14

TABLE 1-2 SPATIAL RELIABILITY ISSUES - RANDOM VS SCHEMATIC........ 15

TABLE 1-3 COMPARISON OF BTI MECHANISMS IN NANOMETER TECHNOLOGIES........ 19

TABLE 2-1 DIFFERENCE BETWEEN ERROR DETECTION AND CIRCUIT FAILURE [1] 31

TABLE 4-1 BTI AND HCI ANALYSIS COMBINATIONS........ 48

TABLE 4-2 INDIVIDUAL AND COMBINED IMPACT OF BTI AND HCI ON STANDARD CELL DELAY 49

TABLE 4-3 INDIVIDUAL AND COMBINED IMPACT OF HCI AND BTI ON CELL RISE........ 50

TABLE 4-4 INDIVIDUAL AND COMBINED IMPACT OF HCI AND BTI ON CELL FALL........ 51

LIST OF ABBREVIATIONS

PPA	Power, performance and area
nm	Nano-meter
FINFET	Fin shaped field effect transistor
FD-SOI	Fully depleted silicon on insulator
BTI	Bias temperature instability
HCI	Hot carrier injection
PFET	Positive channel field effect transistor
NFET	Negative channel field effect transistor
IoT	Internet of things
R&D	Research and development
CMOS	Complementary metal oxide transistor
IC	Integrated circuits
MOSFET	Metal oxide field effect transistor
RDF	Random dopant fluctuation
UTBB	Ultra - thin buried box
V_t	Threshold voltage
PVT	Process voltage temperature
CAD	Computer aided design
EDA	Electronic design automation
ASIC	Application specific integrated Circuit
I/O	Input/output
CDL	Circuit description language
SPICE	Simulation program with integrated circuit emphasis
UDRM	User defined reliability model
PBP/PB/P	Poly-bias (extended channel length in nm)

CHAPTER 1

1 INTRODUCTION

1.1 INTRODUCTION TO UNRELIABILITY

With continuous device scaling and technology advancements, reliability issues have become a major concern for all devices/circuits. In the Nano-scale FD-SOI CMOS devices, Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI) greatly affect the delay of the digital circuits. FD-SOI in comparison to the bulk CMOS devices provide improvement in speed but the delay degradation due to ageing effects may lead to timing violations and functional failures in the device. With increasing innovations, the introduction of FD-SOI (Fully Depleted Silicon on Insulator) is considered as a big achievement. FD-SOI has major benefits over the existing Bulk technology MOSFETs. FD-SOI has an ultra-thin buried oxide (BOX) layer in the substrate which not only reduces leakages due to the good isolation it provides, it also makes the application of increased substrate voltages possible as compared to the Bulk technology MOSFET. It is also low power oriented and supports low power techniques such as power-gating and clock-gating. It also supports multiple power domains and offer multi threshold voltages. Overall, the FD-SOI technology offers better performance in comparison to the bulk technology but its reliability needs to be focused on because reliability compliments a good design.

The thesis topic is thus selected because identifying the amount of timing degradation in standard library cells is crucial as in the later steps of the design flow as in the case of technology mapping the standard libraries are the target libraries. Timing issues in the library cells/gates should be evaluated to avoid timing or/and functional failures later. Also Static Timing Analysis is performed later which refer to the look up tables provided with the standard libraries which means proper timing analysis of the library cells with and without ageing is necessary. Better analysis means better design margins and safer designs.

1.2 OVERVIEW OF RELIABILITY ISSUES

Reliability of the devices was first studied in the early sixties when advanced Integrated Circuit(IC) development was occurring. “Purple plague” was the very first reliability issue that was encountered. It was a bonding issue that occurred in 1970’s along with other issues that were seen later like corrosion and ionic contamination. These issues were however related to the design packaging [9]. Effects such as Hot carrier injection was first noticed in the middle of 1980’s which was attributed to

the scaling of the oxide thickness and therefore the electric fields related to it. Initially hot carrier injection was considered deterministic in nature as it caused a performance degradation shift which could be mitigated by a technique as simple as voltage (stress) application. Later on as the device dimensions were greatly scaled and designers entered into the nanometer dimensions, unreliability became a serious threat to high yield and proper circuit functionality. The categories of reliability issues can be seen in Figure 1-1.

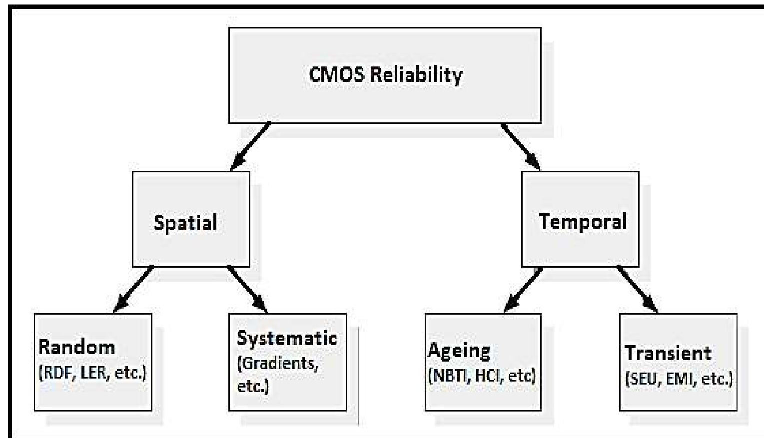

Figure 1-1 Reliability issues in MOSFET

1.2.1 Failure Mechanisms

A reliable circuit by definition is a design circuitry which performs its assigned tasks as it is intended to, under different working conditions over a period of time. Reliability guarantees less failure rate during the operating lifetime of the circuit. A very famous bath tub curve tells us about the very basic failures over the time period which may occur at the time of production, device operation and end of the operation time. Moreover, there are two fundamental categories of reliability issues namely spatial reliability issues and temporal reliability issues. Random and systematic issues are sub categorized under the spatial issues in reliability which include line edge roughness, random dopant fluctuation etc. On the other hand, the temporal issues include in itself ageing and transient issues which are the bias temperature instability, hot carrier injection electromigration etc. The contrast between the spatial and temporal issues in reliability is shown in the Table 1-1. Our focus shall remain on the temporal reliability issues consisting of the ageing phenomenon.

Table 1-1 Categories of transistor reliability issues

Spatial Reliability Issues	**Temporal Reliability Issues**
Fixed in time	Time varying
Physical design dependent which includes geometry and layout.	Dependent on switching activity factor, temperature and voltage.
Might result in loss of yield	May lead to circuit failure.
These issues can be: • Systematic issues • Random issues	These issues can be: • Transient issues • Ageing issues
Examples: Random dopant fluctuation Line edge roughness/ Line width roughness	Examples: Hot carrier injection, Bias temperature instability

1.3 SPATIAL RELIABILITY ISSUES

Spatial unreliability/process variability is an increasing problem in the fabrication of nanometer technology. No two transistors fabricated are exactly identical in terms of its parameters. They show certain mismatch with respect to one another. These variations put forward the need to make adaption of circuit against such variations which may be a serious cause of circuit failure. The difference between performances of devices is the result of spatial unreliability. This causes no two chips manufactured at different times to be identical. The spatial variations can occur between one manufactured lot and another, between two different chips, between two different wafers and across the area of a single wafer as well. The effects of spatial issues as mentioned in Table 1-1 do not vary with time. They are dependent on the device geometry and layout which means they are physical design dependent [9]. They might lead to loss in the yield where the yield represents the good wafers out of the total wafer count. Spatial reliability issues can be categorized as Random issues and Systematic issues. The systematic issues are also referred to as deterministic issues. They are referred to as deterministic because the variation of parameters from the normal value show a dependency on the location of the device on the wafer and die. The occurrence of these issues is attributed to the problems encountered during the technology processing techniques and fabrication.

Table 1-2 Spatial reliability Issues - Random Vs Schematic

Random Issues	**Systematic Issues**
It results due to physical phenomenon such as RDF (random dopant fluctuation), LER (line edge roughness), presence of fixed charges in dielectric, LWR (line width roughness) etc.	Shows dependency on the physical dimensions that is it is layout characteristic dependent where the processing steps are limited by the resolution.
Causes transistor mismatch	Causes large variations in high density/high interconnect area of the design

These discrepancies during processing and fabrication can be a misalignment or out of focus lens, effects of chamber etc. The lithographic setup can be seen in Figure 1-2. The stochastic variations which are another name for the random variations as the name suggests are unpredictable in nature. Reason for their occurrence might be random dopant fluctuations, introduction of dust particles during fabrication etc. The broad difference between the two is discussed further in the Table 1-2 shown above.

An overview of the causes of occurrence spatial reliability issues is discussed below. The common sources are listed below:

- Line edge roughness- With the scaling down of feature sizes the photoresist granularity causes the formation of a channel length which is not uniform along the length of poly gate. This further causes an exponential increase in the off state current thus increasing the overall leakage. As a result, threshold voltage degradation along with degradation in transistor's short channel characteristics occurs.
- Variations in lithography – Lithography refers to the patterning of a layer onto a surface. The feature sizes to be printed have their dependency on the lithographic system's control.

Lithographic variations can occur due to the different speed of movement of reticle and wafer, scanner vibrations, focus depth non uniformity and the variation in exposure of light. The result of such lithography may lead to non-uniform printing of dimension lines causing leakages and speed reduction.

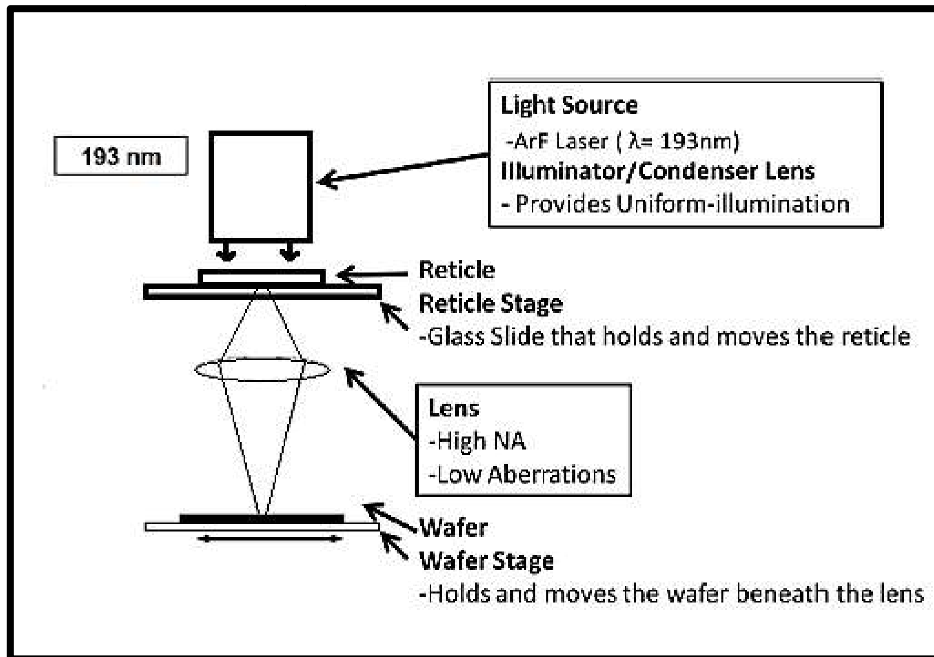

Figure 1-2 Lithography Setup

- Well proximity effects- This effect depends on the layout of the design. In small feature sizes the ion implants scatter (laterally) such that these ions having high energy have a collision with photoresist's edge on shallow trench isolation's top which is followed by their projection into channel before formation of gate (polysilicon). The consequence is increased threshold voltage.

- Random fluctuation in dopants - If there is a variation in the number of dopants or a fluctuation in their location along the length of a transistor's channel it is referred to as random dopant fluctuation. This leads to effects such as DIBL, short channel effects etc. There is also an unavoidable impact on the threshold voltage of the transistor and electrical parameters.

1.4 TEMPORAL RELIABILITY ISSUES

The work focuses on ageing due to BTI and HCI mechanisms. After circuit fabrication, during utilization of the circuit under specific temperature and environmental conditions the circuit performance begins to degrade. Our aim here is to understand the contribution of these factors in ageing process and a way to mitigate ageing.

1.4.1 Hot Carrier Injection (HCI)

In short channel devices the increase in horizontal fields near the drain region cause acceleration in charge carriers of PFET and NFET till they have sufficient energy to abandon the channel and enter the dielectric leaving behind space charges. This high electric field accelerates the charge carriers in the channel causing them to become energetic or otherwise termed as "**hot**". These hot carriers instead of following their intended trajectory overcome the potential barrier at the substrate-dielectric interface, thus penetrating into the dielectric (silicon dioxide) layer which is the forbidden region. This therefore changes the dielectric properties of the silicon dioxide layer causing device degradation. It affects the threshold voltage of the device and parameters such as mobility and threshold voltage. Also this effect is asymmetric in nature damaging the drain region of the transistor. The hot carrier injection can be differentiated into four types:

- Channel hot electron injection (CHE)
- Drain avalanche hot carrier (DAHC)
- Secondary generated hot electron injection (SGHE)
- Substrate hot electron (SHE)

1.4.1.1 Channel hot electron injection (CHE)

When the gate voltage and the drain voltage are equal channel hot electron injection is prominent. The lucky/hot electrons surmount the Si-Sio2 barrier after being accelerated in the direction of the gate under the influence of the applied gate voltage and enter the silicon dioxide layer.

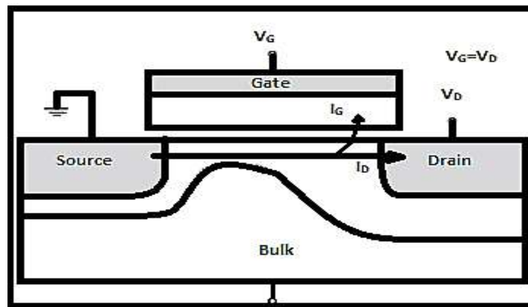

Figure 1-3 Hot carrier Injection (CHE)

In the figure shown above Figure 1-3 represents applied gate voltage, V_d represents the applied drain voltage.

1.4.1.2 Drain Avalanche Hot Carrier Injection (DAHC)

The DAHC is mainly a result of the process known as impact ionization and avalanche multiplication. The hot electrons due to impact ionization generate electron hole pairs which accelerate and further cause generation of these electron hole pairs. Some of these carriers damage the device by entering the oxide layer. Figure 1-4 shows DAHC.

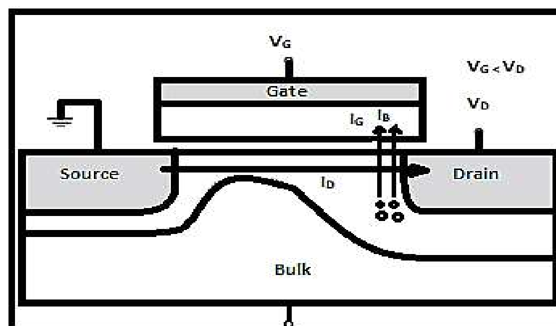

Figure 1-4 Drain avalanche hot carrier injection

When the applied drain to source voltage is almost twice the gate to source voltage value this effect is maximum. As per the literature the hot carrier injection effect is modeled as an increase in the device threshold voltage and a decrease in the mobility value.

1.4.2 Bias Temperature Instability (BTI)

Bias temperature instability is a very important reliability issue which adversely affects both PFET and NFET especially those that are implemented in the nanometer technology. This occurs when the gate terminal of the FET is subjected to high bias voltage at elevated temperatures. The two main BTI mechanisms observed are:

- NBTI (negative bias temperature instability)
- PBTI (positive bias temperature instability)

NBTI occurs in a PFET on application of a negative bias voltage while PBTI occurs in a NFET when a positive bias voltage is applied. The major differences between the two are tabulated below in Table 1-3. The BTI mechanism occurs in two main phases:

- Stress phase
- Recovery phase

During the stress phase the dangling bonds (Si bonds) at the channel-substrate interface are transformed into the SI-H bonds during the process of passivation (hydrogen passivation) which is performed after the oxidation process. These SI-H bonds are weak and might/might not break during the operation of the device. Breaking of these bonds leads to decrease in the drive current due to diffusion of hydrogen atoms into the dielectric. This stress phase is modeled as a shift in the threshold voltage value. The recovery mode takes place when the gate voltage with respect to the source voltage is made zero. At this moment there is no stress condition and the diffused hydrogen atoms in the oxide anneal the previously broken Si-H bonds. Hence, the shift in the threshold voltage reduces. Figure 1-5 represents dangling bonds at the body-dielectric.

Table 1-3 Comparison of BTI mechanisms in nanometer technologies

NBTI	**PBTI**
Caused due to hole trapping in oxide defects	Caused due to trapping of electrons in the traps

NBTI	PBTI
Results in generation of interface states at the interface of channel in the substrate and the silicon dioxide dielectric layer	Results in the trap generation process followed by channel carrier trapping in the new traps formed or the preexisting ones
NBTI affects a PFET	PBTI affects a NFET
Causes a parametric shift in the transistor threshold voltage	Causes a parametric shift in the transistor threshold voltage

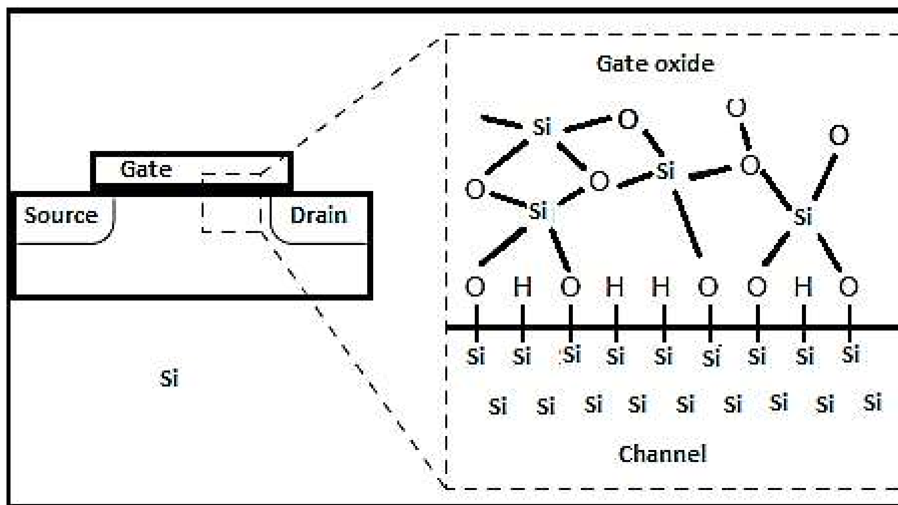

Figure 1-5 Representation of the dangling bonds at the body-dielectric

1.4.2.1 NBTI (Negative bias temperature instability)

The study of this phenomenon was initially conducted by Grove and Deal at Fairchild Semiconductors in 1960's. At that time the device dimensions were large therefore the phenomenon did not gain much attention. Entering into the nanometer and the sub-nanometer domains worsened its impact. PFET's have a very high tendency of generating interface traps in the presence of a negative bias voltage applied for a long duration of time. This leads to the creation of interface states and fixed charges. The

study of NBTI is done for a longer time duration over an elevated voltage and temperature. NBTI is enhanced factors such as gate oxide thickness (lesser thickness leads to higher oxide electric field), power dissipation (higher power dissipation leads to elevation of temperature) etc.

1.4.2.2 PBTI (Positive bias temperature instability)

PBTI affect NFET's leading to trap generation and trapping of electrons in the pre-existing traps. This occurs when the gate of the PFET's are subjected to greater voltages at high temperatures over a longer duration of time. The introduction of new materials for fabrication also increases the PBTI effect, for example: High k dielectric (HF) for reducing gate leakage results in greater PBTI in transistors.

1.5 INTRODUCTION TO FD-SOI

FD-SOI stands for "Fully depleted silicon on insulator" and the geometrical representation can be seen in Figure 1-6. It is a technology that was developed mainly to overcome the shortcomings of Bulk CMOS technology. The main issue with the shrinking channel length in already existing bulk CMOS technology was the subthreshold leakage. FD-SOI and FINFET were the alternatives proposed to combat the limitations imposed. The 28nm bulk CMOS technology suffered from short channel effects like drain induced barrier lowering, gate induced drain leakage, reverse diode leakage currents, gate tunneling currents and mainly subthreshold leakage. There was a very severe issue known as latch up problem which causes permanent damage to the device. Random dopant fluctuation (RDF) variability which refers to the variability in the number or/and position of dopants in the channel of the transistor leading to transistor variability (different transistors in the chip show random variation in the threshold voltage values) was also predominant. This leads to leakage increase and device instability at the chip level. The CMOS process nodes were also limited in terms of body biasing.

The UTBB on the other hand offers a wide range of advantages to cope up with the limitations. We shall see the structure and advantages of the UTBB FD-SOI over the conventional CMOS processnode. UTBB FD-SOI is a planar CMOS technology where the transistors are fabricated in a silicon layer with thickness of around 7nm (ultra-thin) which is present above a buried oxide (BOX/Film) layer with thickness of around 24nm when taking about a 28nm process (STMicroelectronics). The control of the gate over the channel in this technology is very good. The channel formation takes place between the oxide layer and the BOX at top and bottom and confined

between the source and the drain at the sides. The channel in the FD-SOI operates in a fully depleted mode. FD-SOI is a self-aligned process with no latch up problem. Also the steps involved in fabrication/processing of this technology is 15% less than conventional Bulk CMOS technology and easier than the processing steps of FinFET.

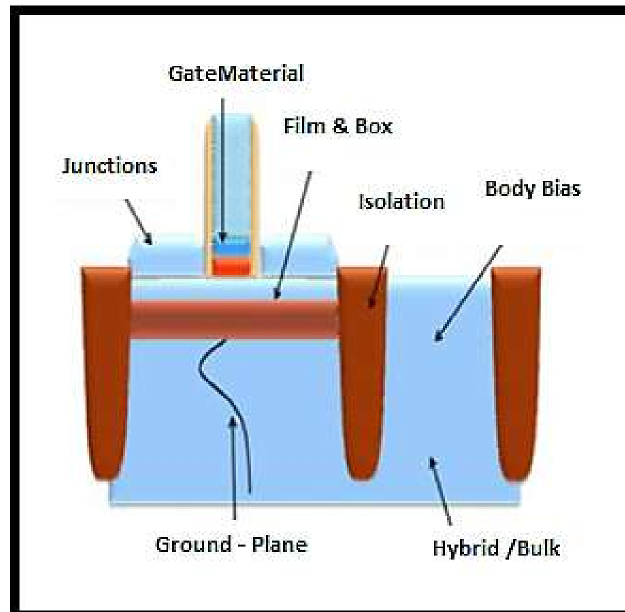

Figure 1-6 Structure of UTBB FD-SOI device

FD-SOI devices require no channel doping thus reducing or eliminating the RDF (random dopant fluctuation) induced variability in threshold voltage. The leakage power dissipation also sees a reduction in this technology due to the absence of the junction formed between the source-body and drain-body. FD-SOI devices can be efficiently optimized for leakages and speed as it offers various V_t flavors and extended bulk bias capability. Therefore the major advantages of Overview of FD-SOI can be summarized as follows:

- Planar technology
- Easy fabrication steps
- No latch up problem
- Greater control of gate over channel (no channel doping required)
- Reduced leakage currents

- Short channel effects limited
- Multiple V_t flavors
- Reduced Drain induced barrier lowering especially at low supply voltage

Major reliability challenges in FD-SOI technology are hot carrier injection, bias temperature instability and time dependent dielectric breakdown. The very basic explanation of time dependent dielectric breakdown is the process of failure leading to the gate oxide breakage due to the application of continuous electric stress. Time dependent dielectric breakdown is not a sudden breakdown phenomenon but a very slow, low electric field dependent breakdown. In this phenomenon a conductive path between the substrate from the gate oxide is formed when transistor is operated beyond or close to its operating voltages. The other two reliability issues are discussed above beforehand. The hot carrier injection refers to the carriers gaining high energy from the electric fields at the drain end which leads to the carriers deviating from their intended trajectory and entering into the oxide leading to trapping and interface state formation. The bias temperature instability on the other hand is the transistor reliability issue caused when the transistor is being operated at elevated temperatures and are being subjected to high voltages. The overview is provided in the sections 1.4.1 and 1.4.2.

The objective of the thesis is the analysis of the degradation caused due to ageing phenomenon causing wear out failures occurring due to ageing for different PVT conditions, across varying input slopes and output loads for different cells of standard cell libraries by focussing on the degradation in the delay both rise and fall delays in basic combinational standard cells. The results point out the study done across different channel lengths for a reference standard cell library. The shift in the process parameter of the transistors that is the V_{th} (threshold voltage) is observed in the result section. The threshold voltage shift further causes degradation of the device performance which may lead to functional errors or/and device failure. The analysis is followed by identifying technique to mitigate the phenomenon of ageing because unnecessary margins in a design causes decrease in optimum device performance, moving from one technology node to the next/another. The work presented therefore provides results pertaining to degradation in timing of a gate in order to prevent under/over assignment of safety margins.

1.6 INTRODUCTION TO STANDARD CELL LIBRARY

Over the past decades, Moore's law has always held true, credits to the extraordinary advancements in technology. Sizes (feature sizes) over the years have shrunken from around 500nm in the 1990's to around 10nm at present. With this continuous scaling, the CAD/EDA tools have become of utmost importance in order to automate the entire design and fabrication process to avoid manual errors, provide ease and fasten the time to market. The miniaturization of sizes have led to the chips being highly dense therefore making it extremely difficult rather impossible for being assembled, verified and tested manually. The standard cell library (semi-custom design) helps in the automation of the design flow. The very important power, performance and area (PPA) of the standard cells decide or are coupled tightly to the power, performance and area of the whole chip. Standard cell library is a consolidation of basic gates (Boolean logic) known as cells represented as views specifically designed for applications in need and requirements enlisted by the customer. These cells form a part of the very low level design space and are of a standard height.

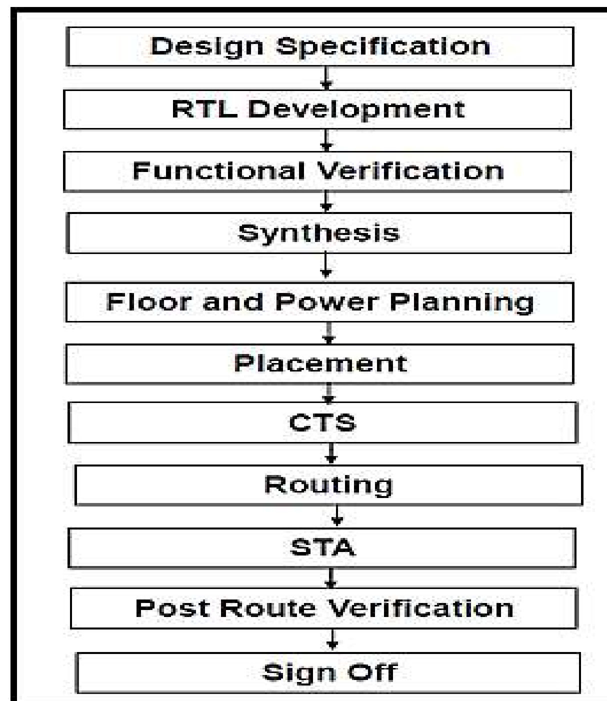

Figure 1-7 Basic design flow

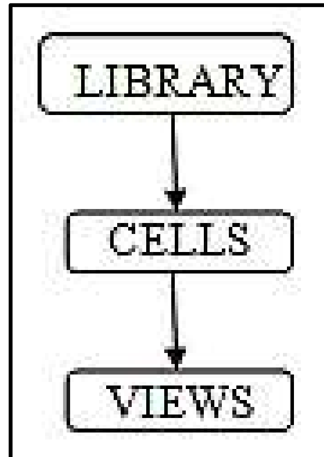

Figure 1-8 Basic standard cell library composition

Figure 1-7 represents the ASIC design flow and Figure 1-8 represents the composition of standard cell library. A standard cell library consists of cells of different drive strengths and different architectures characterized by varying slope and loads over different PVT (process, voltage and temperature) conditions. The cells of the standard cell library characterized as the "Foundation IP" form the basis/foundation of the ASIC design. Standard cell library is the target library which is an input to the logic synthesis step of the design flow which requires mapping of the higher level design to a target technology library. The various types of libraries are as follows:

- Standard cell libraries
- Memory libraries
- I/O libraries
- Macros libraries
- Analog and mixed signal libraries

1.6.1 Standard Cells representation – Views

Views are a particular representation of cells. Each cell may have a layout view, schematic view, timing view etc. A cell is delivered as a set of views which are used by different tools in a given design flow. The standard cell views are shown in Figure 1-9.

The representation of the standard cells as views as seen in Figure 7 are as follows:

- Front end views
- Back end views

The FE (front end) views are related to the timing and modeling information of the cells whereas as the BE (back end) views are related to the physical design of the cell. The front end and back end views together can be classified as primary views and secondary views where the secondary views are vendor specific and compatible with only certain tools provided by the vendors. The views are used at various steps of the design flow and by various tools. The primary views are overall compatible with all the tools at the design steps required. The secondary views are derived from the primary views.

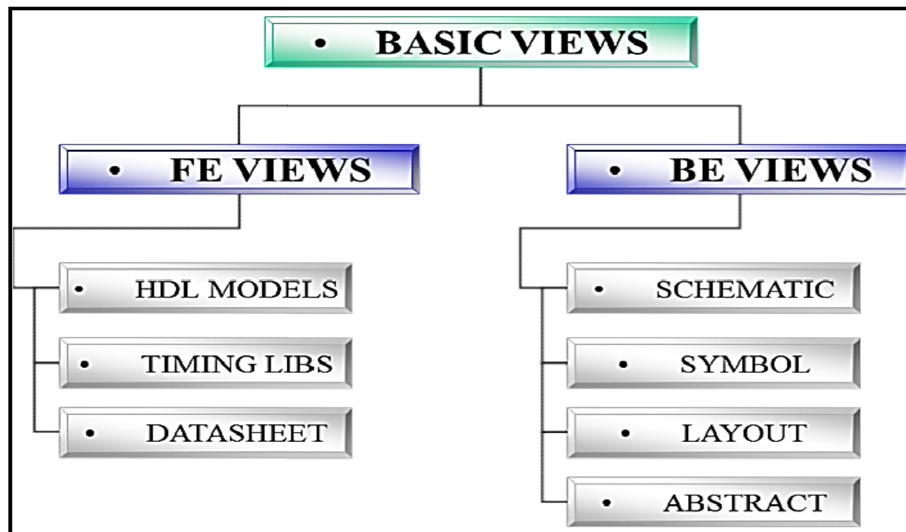

Figure 1-9 Basic views - cell representation

The primary views are mentioned below:

- Synopsys technology file (.libs)
- GDSII (graphical design system)
- CDL (circuit description language)

The secondary views are as follows:

- Avanti (by Synopsys)
- Magma
- Encounter

1.7 INTRODUCTION TO SIMULATION

Any circuit (digital, analog or mixed) is comprised of sub circuit elements. The complete circuit behavior is dependent on the behavior of these sub circuit elements. The analysis of these elements therefore is important and is done with the help of circuit simulators which are commonly the SPICE simulators or otherwise the analytical simulators. SPICE stands for simulation program with integrated circuit emphasis. The SPICE simulators are responsible for predicting the real time behavior of the circuit design therefore checking the circuit integrity. They provide ac (linear), dc(non-linear), transient (non-linear) and noise analysis. Any simulator essentially needs three primary files namely:

- The circuit netlist specifying all the elements of the circuit along with their interconnections in a textual form.
- The Models which represent the expression (analytical) whose basis is the study both theoretical and experimental.
- The initial conditions of the circuit under study.

The analysis carried out by the simulator is strictly in accordance to the electrical laws like ohms, KCL, KVL etc. by solving a set of equations (linear/non-linear). The result of the analysis at the end of the simulation can be viewed in a graphical interface.

1.7.1 Reliability Simulation

Reliability simulation is performed in two stages. In the very first stage a standard simulation is performed by a SPICE simulator in the absence of the application of stress conditions. In this work the simulations are performed by ELDO – SPICE simulator by Mentor graphics. Simulations can also be performed by other simulators like the HSPICE by Synopsys. The initial simulations also known as the fresh simulations are performed using ELDO which

yields results predicting the lifetime of the circuit by evaluating activities of the circuit and circuit behavior. This is followed by the next simulations known as the age simulations. During the age simulations a stress condition is applied to the circuit. The models used in the former and latter simulation stages are different. In the fresh simulation a conventional SPICE model is chosen while in the latter a degraded SPICE device model is considered. The degraded device model is a transistor model taking into account the BTI and HCI ageing phenomenon. The age simulation is performed as a two-step process involving the characterization and stress phase. The results of the two simulations are later compared to evaluate the degradation in circuit parameters, performance and lifetime.

1.7.2 Reliability simulation – STMicroelectronics

The reliability simulation flow can be seen in Figure 1-10. As mentioned earlier the device model is a primary input to the simulator. Therefore it is obvious to have a degraded device model beforehand to be able to carry out the reliability simulations. SPICE solely represents the device with the designer. The definitions in SPICE models are very complex and reliability models additionally have coefficients which are independent to other model coefficients. The coefficient calculation for the models is done indirectly from interlinked coefficients. This enables simulation with or without reliability.

A standard BSIM model is compared with a reliability model in the reliability simulation. The degraded model of the device at STMicroelectronics is calculated by an interface application known as the ELDO-UDRM. UDRM stands for user defined reliability module. UDRM and ELDO interact with each other for the calculation of degradation for every transistor in the circuit. The model implementation is done using the interface after which the compilation is done in ELDO. Every transistor's operating point is calculated initially at the beginning of the flow by ELDO. UDRM makes use of this information for degradation calculation of every transistor for which the step time is same as the ELDO simulation step time.

The ELDO – UDRM application program interface provides write access and read access functions to the threshold voltage value and mobility values. During stress assessment, evaluation of parameter values in accordance to the operating conditions is done. The degradation is represented by a modified SPICE parameter which is used to perform the simulations for the transistor.

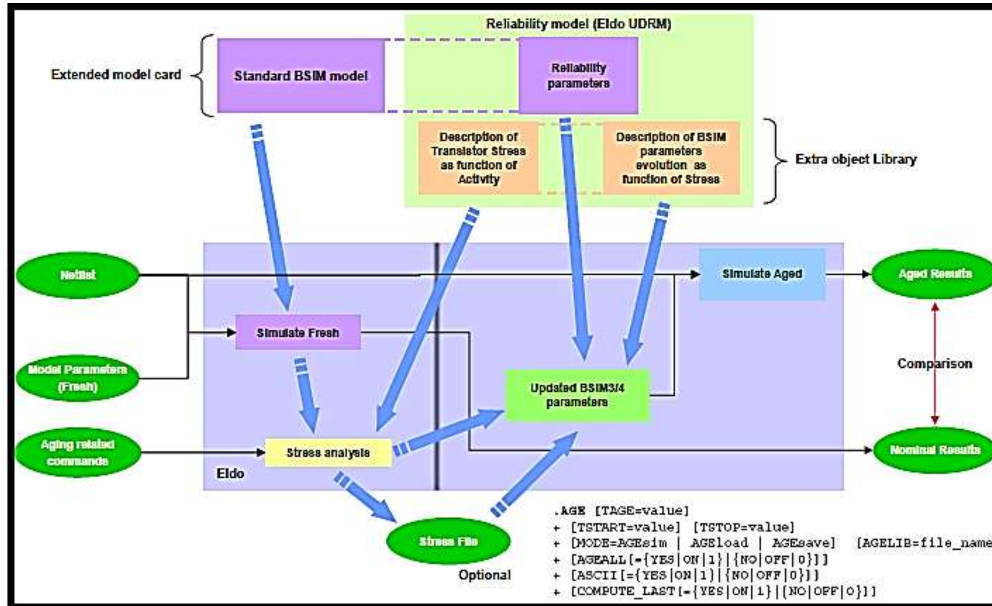

Figure 1-10 Reliability simulation – STMicroelectronics

The stress assessment is based on two working principles which are as follows:

- Linearization - The modeling of degradation is done as a power function of stress. The stress is modeled linearly with respect to time.

$$\text{Degradation} = (\text{Stress})^{\text{time}}$$

- Integration - The modeling of stress is done as a product of the ratio of the time desired for reliability simulation to the time required for unit simulation with the integrated value of function of operating points over the operating times.

There is no limitation on the number of stress vectors used for simulations. Any number of stress vectors can be used for storage of additional data during the analysis of stress. The information extracted from the simulations sets run later are beneficial for a complete and closer to real time stress assessment. Apart from the stress file, the simulations of any set are entirely independent to any other simulation sets. The information is useful for assessing the impact on performance. While the later simulation runs are being carried out the parameters in the BSIM models specified in the UDRM are updated in order to represent the aged device parameters. The stress which is calculated in the first simulation may be used for any number of age simulations.

CHAPTER 2

2 LITERATURE REVIEW

Moore's law predicted a continuous decrease in the size of the devices. The very first point contact functioning transistor (germanium) was made at the Bells lab by William Shockley and his fellow colleagues. Later Shockley invented the bipolar junction transistor popularly known as BJT which was followed by the first integrated circuit made in 1958 by Jack Kilby of Texas Instruments. This BJTinvention led to the beginning of the Silicon age in the year 1958. The first CMOS logic gate was invented in 1963 followed by Intel's invention of the microprocessor. Over the time the semiconductor industry made extra ordinary advancements. In order to fulfill the requirements of power, area and performance new technologies were introduced and feature sizes were reduced to support the Moore's law. In this section we shall see the various works of research related to the reliability issues which came into the picture with scaling and new technologies. The publications help in the understanding of the unreliability phenomenon, parameters of the devices affected due to reliability issues and failure prediction.

Mridul Agarwal et al[1]in 2007 presented a paper introducing the concept of prediction of failures in circuits. They focussed on practically demonstrating its implementation and showing its effectiveness for transistor ageing in PMOS (NBTI). The ageing mechanism in PMOS led to reduction in the transistors speed observed over time. This further led to the occurrence of delay faults. The technique proposed was, that instead of following the common and conventional approach of enabling the worst case design alternate approach of enabling the close to best case design be followed. The technique of failure prediction was demonstrated on 90nm and 65nm technologies where the results of simulation showed that the performance of the design improved significantly for the proposed technique. They also tabulated the main differences between the error detection and circuit failure prediction and showed how the two together can be combined and used efficiently. The authors in the paper presented that the prediction of failures in a design before-hand helps in adopting corrective measures before error occurrence, propagation and detection actually takes place. Difference between error detection and circuit failure is elaborated by the authors in Table 2-1.

Table 2-1 Difference between error detection and circuit failure [1]

Circuit Failure Prediction	Error Detection
Before error appears	After error appears
No corrupt data or states	Corrupt data and states
Can collect data over several cycles before predicting failure	Long error detection latency causes data integrity problems
Generally inexpensive	Generally expensive
Self – diagnostic possible	Limited self - diagnostics
Incorrect prediction can be a problem	Insufficient coverage can be a problem
All failures not predictable	General applicability
Both can be efficiently combined	

Wenping Wang et al[2]in 2007 proposed the idea of identifying the critical gates, which is the gates that are of utmost importance in timing degradation. The identification of such gates as per the proposal protected the circuit from the process of ageing. This was also a beneficial proposal as it had minimum design overhead. The critical gates were identified by a new way of timing analysis that made use of an ageing aware library (NBTI aware). The degradation in timing for the worst case existed for a specific signal probability. This method was applied to circuits implemented in 65nm technology nodes and was ITC and ISCAS benchmarked. The results showed that as few as 1% gates needed protection to control ageing within 10% range over a period of 10 years. The proposed method was quite efficient as every critical path needed to be analysed only once.

Rui Zheng et al [3] in 2009 carefully studied the famous RD model (reaction-diffusion) and identified the assumptions that were mainly responsible for the degradation of PMOS due to NBTI. Based on the study a novel model for ageing with a different diffusion profile was proposed that helped in detailed and correct analysis of degradation in low power applications. The phenomenons modelled were HCI and NBTI. The proposed model well predicted the degradation in 45nm and 65nm

technology node CMOS devices. The model was validated on a ring oscillator structure which was fed patterns for operation (realistic). The model proposed, proved beneficial for avoiding thepessimistic approach in analysing ageing effect therefore helping in reducing the design margins which are kept in order to increase reliability of the circuit.

Bogdan Tudor et al [4]in 2011 proposed a model for HCI and BTI ageing phenomenon which were analysed on silicon level for and below 32nm – 28nm. BTI occurs in two phases, the stress phase and the recovery phase both of which need to be properly modelled. The model formulated and presented in the work takes into account these phases, biasing voltage, temperature and geometry. The proposed model was implanted in a MOSRA circuit where translation of the magnitude of electrical stress into degradation of the device otherwise termed as age was done accurately. This translation could be explained by two model techniques namely, table based and parameter based where the latter was preferred over the former as it was easily addressable and predictive.

Sanjay V. Kumar et al [5] in 2011 proposed in their work that by using the low power techniques namely body biasing (adaptive) and voltage scaling (supply voltage), an aged circuit could maintain its performance (optimal). The proposed technique was beneficial due to the minimum overhead of area and power it offered. Moreover the merits of adaptive body biasing and synthesis were used such that the circuit's constraints were successfully met over the lifetime of the CMOS circuits under study and otherwise.

Gates in path	Fresh		Transition type	Aged ($2x10^6$s)	
	Gate delay (ps)	Path delay (ps)		Gate delay (ps)	Path delay (ps)
DFF1	192.6	192.6	Fall	192.6	192.6
Inv1	20.7	213.3	Rise	22.8	215.4
Inv2	11.1	224.4	Fall	11.1	226.5
Inv3	17.2	241.6	Rise	19.2	245.7
Inv4	11	252.6	Fall	11	256.7
Inv5	17.1	269.7	Rise	19.1	275.8
Inv6	10.9	280.6	Fall	10.9	286.7
Required data arrival time		285	Required data arrival time		285
Setup slack		+4.4	Setup slack		-1.7

Figure 2-1 Delay comparison in fresh and aged delay [6]

Jyothi Bhaskarr Velamala et al [6] in 2011 modelled the ageing induced delay in the circuits using the already available models for the shift in gate delay with respect to the V_{th} (threshold voltage). The new proposed model – “Delay model”, helped to calculate the change (shift) in gate delay induced due to V_{th} shift by making use of the information about delay as a function of the supply voltage change which is provided in the standard cell library. This method was proposed in order to avoid simulations for calculation of delay due to ageing. In the work it was also identified that the end of the standby mode of the circuit operation was the most critical moment in ageing induced degradation calculation. The demonstration of the entire analysis was done on an ISCAS89 benchmarked sequential circuit. The delay comparison by the authors is shown in Figure 2-1.

Mehdi Kamal et al [7] in 2012 presented in their work a simulation flow to analyse the ageing mechanism in transistors due to HCI which included a logic level cell characterization and an efficient simulation of complete chip. The technique presented offered a faster run time and was highly efficient. The modelling proposed was based on the famous RD model (reaction – diffusion) framework. HCI was analysed at gate level followed by HSPICE simulations. It was observed that the ageing phenomenon had varying impact on different transistors by different amounts. The structure of the logic cells played a very crucial role in the amount of degradation experienced by different transistors. Furthermore, the transistors were categorized into groups namely: critical and non-critical. The run time in the proposed method was very less based on the technique that the simulations for the critical transistors were performed in very small steps of time while the simulations for the non-critical transistors was performed in bigger steps of time.

Authors of Springer [8] in 2013 presented a reliability overview and explained in detail Failure mechanisms such as Bias temperature instability, Hot Carrier injection, Electro-migration etc. Bias Temperature Instability (BTI) and Hot carrier injection (HCI) as of late picked up a ton of importance because of its increasingly adverse impact in nanometer CMOS technologies. BTI is typically observed as a V_{th} shift after a bias voltage has been applied to a MOS gate at elevated temperature. For instance, when estimated over a lifetime of 5 years and under typical working conditions, V_{th} movements of up to 30mV can be normal for transistors prepared in a sub-45nm innovation.

Jyothi B. Velamala et al [9] in 2013 presented in their work a proposal for analysis of failure in continuation to their work presented in 2011. This analysis was focussed on the asymmetric impacts of ageing in the digital circuits. The proposed method involved no re-characterization of a standard library cells. It instead used the timing/delay information of the standard library cells for prediction of

ageing and reliability analysis. The work was demonstrated on a standard cell library implemented in 45nm technology. The standard cell library was ISCAS benchmarked. It was observed from the work that the library cells were reliable at higher frequencies, frequencies above 1MHz against NBTI phenomenon. This method was also faster in terms of run time and avoided the extra effort for library re-characterization.

Mohamed Mounir et al[10]in 2014 presented in their work a VLSI circuit level design technique for circuits against the effects of BTI induced degradation. The design technique helped in eliminating the effect of bias temperature instability thus increasing the reliability of the circuits. The proposed technique also helped in reducing the power dissipation by 36%. This technique was the very first work which compared all the circuit level techniques used to mitigate/prevent the effects of BTI. The authors depict the gates under stress during ageing in the circuit under consideration in Figure 2-2.

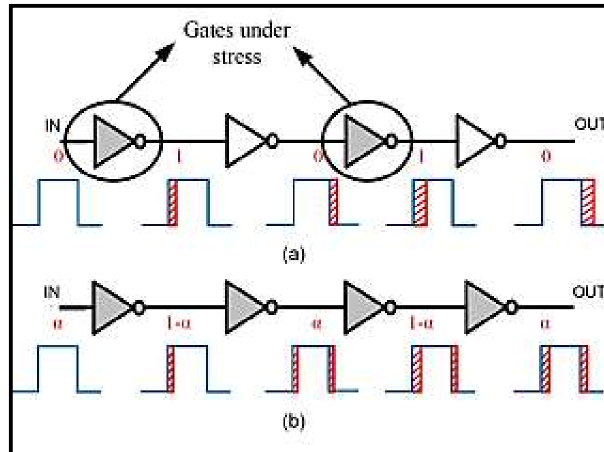

Figure 2-2 Asymmetric ageing in digital circuits [10]

Usman Khalid et al [11] in 2015 presented a work focussed on observing timing related failures specially the timing violations which lead to the write failures. The focus was so because it was important to address the issues related to reliability in CMOS and Fin-FET technologies which have an impact on the noise margin and later on may lead to failure. The reason behind the unreliability was addressed as NBTI and process variability. The analysis was done focussing on the local level cell variations in CMOS cells which had equivalent/same thickness of oxide, length of the channel and the channel width. The analysis was particularly related to noise margin (write) of memory elements. The memory elements were of focus in the work because degradation in such cases lead to system event upsets. Monte Carlo simulations were performed and the variations in the parameters

due to ageing were observed. Both, the nominal value and the standard deviation of the write noise margins were recorded.

Daniele Rossi et al [12] in 2016 presented the positive impacts of unreliability effects where they showed that the BTI mechanism in transistors not only cause degradation in circuit performance and transistor parameters but also prove beneficial in terms of the static power consumption. This benefit obtained in the power consumption reduction is mainly due to the reduction in the sub threshold component of leakage current. The work presented by the authors revealed a dependency of the reduction in static power on the stress application and the operating temperature. The structure under study was a chain of cascaded inverters, 10 inverters in the chain on which HSPICE simulations were performed. The inverter chain was implemented in 32nm HKMG-CMOS (high K dielectric, metal gate) technology node. The results of their work revealed a reduction in the static power consumption by 50%. This reduction was obtained after an operating period of 30 days which increased to a higher percentage over more period of time (reduction in static power consumption of 78% over a period of operation of 10 years).

Charles Augustine et al[13]in 2016 carried out a study on the characteristics of a flip-flop. The study was related to the timing margins for the sequential logic. The dependency of the characteristics of the flop for different process, voltage and temperature conditions along with degradation due to ageing was demonstrated. They demonstrated inter die and intra die variations in hold time. Hold time is defined as the time after the triggering edge of the driving clock for which the data should remain stable. This demonstration was carried out via a novel test structure. The fluctuations in hold time were studied across process skews for different temperatures over varying voltages for different operating lifetimes. The work aided in the guidance of design methodologies (Si calibrated) for mitigation of delay related failures (minimum delay) that too near the threshold voltage.

Maoxiang Vi et al[14] in 2016 proposed a way to tackle with the degradation of transistor parameters, hence the ageing induced degradation due to BTI and HCI in the typical gate CMOS circuits. They proposed a low power technique involving the reordering of the inputs to mitigate positive bias temperature instability and hot carrier injection induced degradation termed as ageing effects. The simulations were performed on HSPICE, the results of which displayed the degradation in the timing delay of the test circuit (CMOS circuitry) of around 2%. Their work also showed that the lifetime of the circuit can be increased on an average of around 13% to 14% through the proposed method of reordering the inputs.

Boukary Ouattara et al [15] in 2016 presented a paper in which they stated the importance of reliability analysis. They stated that ageing of circuits is the main source of reliability issues and studying the factors that are involved in the ageing process helps a designer in the optimization of the design. It is presented in the paper that NBTI is the main source of degradation in digital circuits greatly affecting PMOS. In an industry characterization of any technology in hand is performed against various factors including ageing to observe the impact of the parameters related to ageing on the transistors of that particular technology. A drawback being that usually the impact of ageing on interconnects is not considered/studied. The key parameters affecting the propagation of any signal through a logic gate are operating temperature, process, supply voltage, time of operation and switching activity. To consider the effect on interconnects the load capacitance at input and output is considered. The key findings of the work were:

- NBTI induces delay which is attenuated by increase in supply voltage.
- Ageing is greater at lower temperatures and during initial operating lifetime.
- Increase in switching activity (expressed as a function of signal probability) increases ageing induced degradation.
- The neighboring circuitry impacts ageing of the current logic gate.

There are a few noteworthy conclusions derived in this section. All circuits degrade over time due to reliability issues. Positive bias temperature instability, negative bias temperature instability and hot carrier injection are a few of the main culprits facilitating circuit degradation. It is mentioned that for the reliability issue study usually interconnects are not considered but they play a very important role in causing degradation so the resistance and capacitance values extracted from the layout are incorporated in our study. Failure prediction as opposed to error detection is wiser to use and is helpful in implementing a reliable circuit. Analyzing reliability issues and their impacts in 28nm FD-SOI technology nodes is shown in this work. In earlier works the unreliability issues are mentioned but the individual and combined contribution of the main factors acting individually or/and in presence of other factors are missing which if calculated would prove to be of help in circuit design and reliability study. Low power techniques can be incorporated in the circuit design in order to tackle ageing. The Timing of any circuit is the major area of interest therefore if the impact of ageing of the rise and fall delay components of the technology nodes can be known it would prove beneficial while trying to perform balancing for aged circuits. Also in this report both the positive and negative

impacts of ageing are observed. Lastly how transistor sizing is useful in reliability of standard cell libraries is also seen.

CHAPTER 3

3 PROBLEM STATEMENT

The term “Reliability” is the probability of any circuit or system performing as per its intended functionality under the working conditions (preferably a larger range of PVT’s) over a certain period of lifetime. The reliability of any system gives an assurance of the system leading to lesser rate of failures encountered. The failure rates for a reliable system is fairly lower than the maximum failure rate (targeted rate of failures) intended in the targeted lifetime.

The reliability of any system is represented by a curve popularly known as the “Bathtub curve” or “Failure rate curve” shown in Figure 3-1. The bathtub curve is named so due to the shape of the curve. This is the most common curve used to study the reliability of the semiconductor devices and systems. The curve is divided into 3 main regions representing different causes of failure. The regions of the failures are as listed below:

- Infant failures
- Operating lifetime failures
- Wear out failures

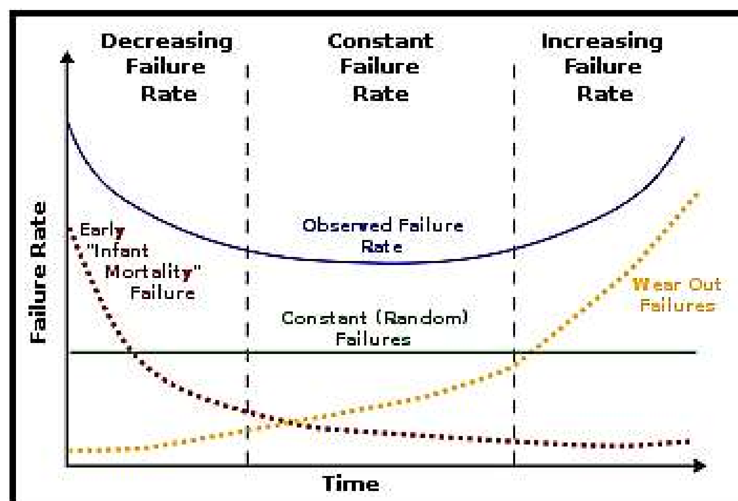

Figure 3-1 Bathtub curve - representation of failure rate in semiconductor devices

Infant failures or infant mortality occur in the very beginning of circuit operation period. They occur due to the defects like dust particles etc. in the material which manifest themselves in materials during processing or manufacturing stage such as lithography process. The presence of these defects in the materials shortens the lifetime of the device making the device highly unreliable. The number of infant device failures reduces with the operational life time of the devices because only the devices with very latent defects fail at the very beginning of lifetime. The infant failures signify problems with material, manufacturing or processing steps. These failures represent problems in technology too.

Operating lifetime failures occur during the normal operating period of the devices. The failures occurring here occur are random and may occur due to soft failures or/and power surges or/and sudden application of high stress in the device. These failures should be less in number and should not really occur. It is expected that the devices should operate as reliable/stable devices after the infant mortality failures due to the absence of latent defects in the materials. The failure rate during this period is very low and almost constant.

Wear out failures occur near/during the end of targeted lifetime of the device. These are attributed to the ageing of the device which means the degradation in device parameters thus degrading the device performance, hence leading to device failures. The aim of any designer is to build a robust system which is reliable and performs the intended functions well and for a long period of time (preferably closest to the targeted period). The occurrence of failures during this last phase increases significantly, almost mirroring the initial infant failure curve.

The technology is being scaled at an increasing rate to fulfil the PPA (power, performance and area) requirements. During the scaling down of the technologies a scaling limit came into picture where the proper functionality of the device at the miniaturized size was challenged. For any technology such scaling limit exists. Introduction of newer materials followed by newer technologies was the alternative to the scaling limit issue in conventional technologies in use. This is how FDSOI came into picture and replaced at many fronts the conventional Bulk CMOS technology. With the newer technologies in use it became important to address the reliability issues and to analyse their impact on the device performance. Ageing became a serious concern and its study therefore became mandatory. The degradation of device parameters and performance due to phenomenon like BTI and HCI in newer technology nodes in short channel devices needed to be studied as they became prominent. The FDSOI in comparison to the bulk CMOS offered various advantages such as lower subthreshold

leakages and no latch up problem but it is also important to study ageing to not overdo the design margins to reduce the design cost and designers efforts.

Reliability issues, especially at lower technology nodes are obstructing the maximum performance of a device and decreasing the device lifetime. Defects cause time dependent short term failures or permanent irreparable damage in certain cases. The objective of the thesis is the analysis of the degradation caused due to ageing phenomenon causing wear out failures occurring due to ageing for different PVT conditions, across varying input slopes and output loads for different cells of standard cell libraries by focussing on the degradation in the delay both rise and fall delays in basic combinational standard cells. The study is done across different channel lengths for a reference standard cell library. The aim is to observe the shift in the process parameter of the transistors that is the V_{th} (threshold voltage). The threshold voltage shift further causes degradation of the device performance which may lead to functional errors or/and device failure. The analysis is followed by identifying techniques to mitigate the phenomenon of ageing because unnecessary margins in a design causes decrease in optimum device performance, moving from one technology node to the next/another. The work presented therefore provides results pertaining to degradation in timing of a gate in order to prevent under/over assignment of safety margins.

CHAPTER 4

4 IMPLEMENTATION AND RESULTS

4.1 METHODOLOGY

The structure of the analysis framework is described in this section. Depending on the user defined specifications and requirements STMicroelectronics Pvt. Ltd. provides high performance and high density standard cell libraries. For my study I considered standard library cells implemented in 28nm FDSOI technology. BTI and HCI affect the electrical performance of all digital standard cells. To obtain a better understanding of the effects of BTI and HCI on standard library cells it is important to take into account the parameters of the circuit some of them being the output capacitance, input slope, output drive and many more. BTI and HCI affect the timing of any circuit which makes the analysis of delay the most important aspect during reliability analysis. Delay of signals propagating through standard cells is dependent on the transistor ageing and design factors.

The behavior of the propagation delay with respect to the operating conditions and capacitance is widely known to be non-linear. The propagation delay through a gate can be understood as the transition time of the output voltage to switch from one stable state to another. This transition time is governed by the charging and discharging of the load capacitance which is represented as the output lumped capacitance. Another way to model the propagation delay is through the concept of charge sharing at the output node. The results in this work show the impact of BTI and HCI on the delay both rise delay and fall delay to help us analyze the ageing phenomenon. In order to work on the problem statement illustrated in Chapter 4 this analysis was carried out on a CORE standard cell library. ST offers various standard cell libraries some of them being as mentioned below:

- **Core** – contains basic combinational and sequential cells.
- **Clock** – contains cells required for clock network such as clock gating and balanced cells and metastable tolerant flip flops.
- **Shift** – contains basic level shifter cells.

- **PR** – contains place and route cells.
- **Sync-space** – contains radiation hardened synchronizer flip flops.

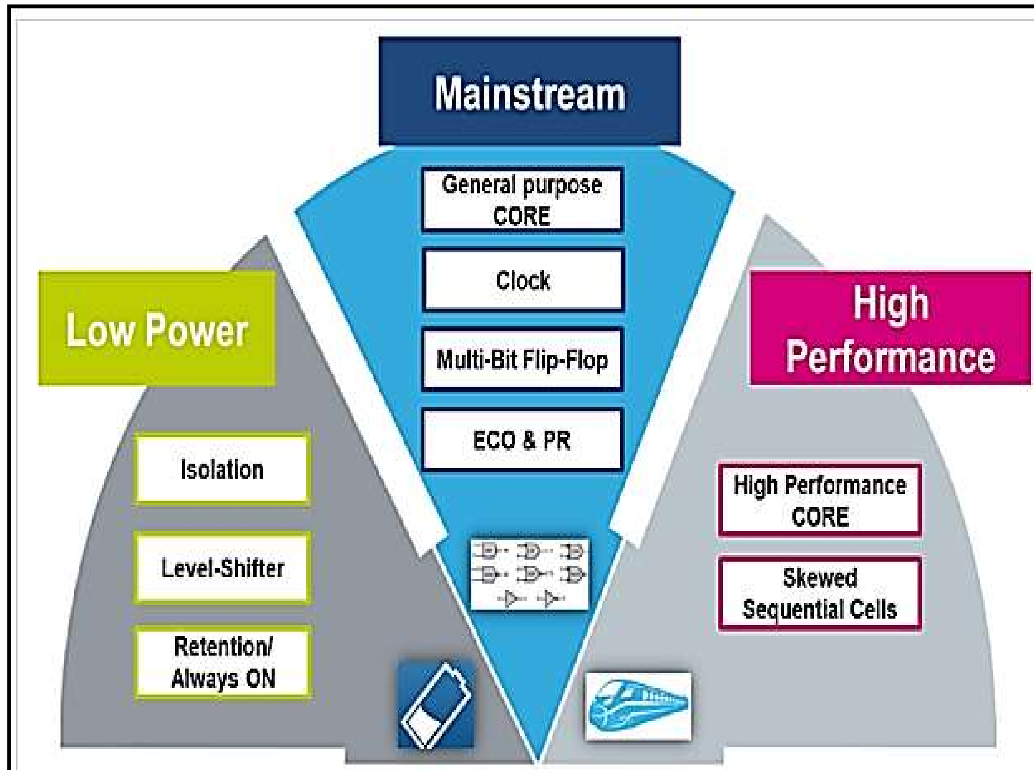

Figure 4-1 28nm FD-SOI Standard cell libraries provided by STMicroelectronics

Figure 4-1 shows different types of standard cell libraries. The libraries provided by the standard cell team have varying channel lengths (additional channel length in nanometer is represented by PBP/PB) with cells having different drives for both the high density and high performance libraries. The analysis in this work is done on high density (8Track) CORE library cells of different PB values. The PB values considered in my work are 0, 4, 10 and 16. The Core Library cells are optimized for balanced timing arc, speed, power and area.

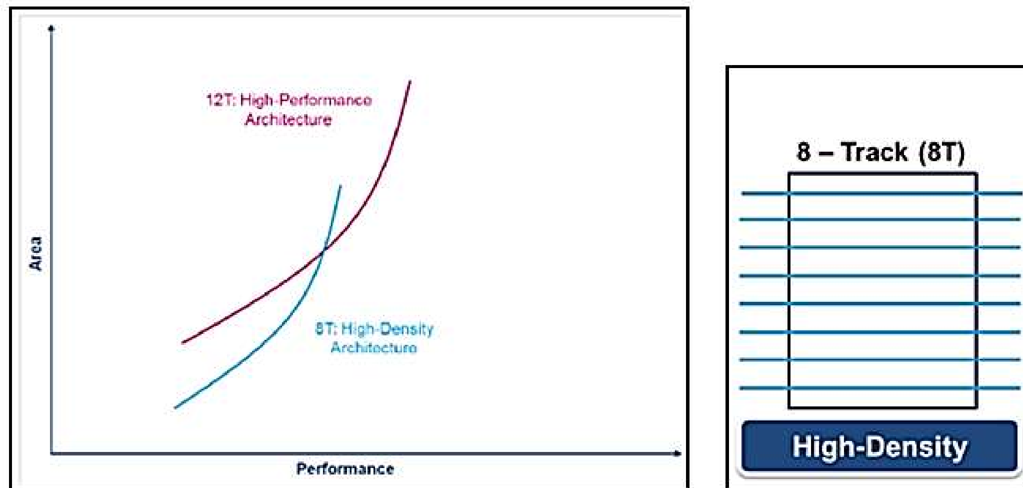

Figure 4-2 High performance Vs High density libraries

The analysis was carried out on C28SOI_SC_8T_CORE_LL standard cell libraries with different poly biasing. STMicroelectronics provides 28nm FD-SOI high performance and high density libraries as shown in Figure 4-2. The libraries considered are as follows:

- C28SOI_SC_8_COREPBP0_LL= "8 track Standard Cell Library comprising commonly used booleans and sequential cells"
- C28SOI_SC_8_COREPBP4_LL= "8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 4 nm"
- C28SOI_SC_8_COREPBP10_LL= "8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 10 nm"
- C28SOI_SC_8_COREPBP16_LL= "8 track Standard Cell Library comprising commonly used booleans and sequential cells, poly biased by 16 nm"

Standard cells of different drive strengths were selected from the above mentioned libraries so that a proper reliable intra and inter-library observation could me made with respect to the aging performed (aging period = 2 years). The ageing PVT for the analysis was ss_0.90V_m40_2ey. The basic combinational cells selected from the library are mentioned below:

- IVX5 = “Inverter cell (low threshold voltage, low power) with an output drive strength of 5”
- IVX10 = “Inverter cell (low threshold voltage, low power) with an output drive strength of 10”

- IVX29 = “Inverter cell (low threshold voltage, low power) with an output drive strength of 29”
- BFX2 = “Buffer cell (low threshold voltage, low power) with an output drive strength of 2”
- BFX5 = “Buffer cell (low threshold voltage, low power) with an output drive strength of 5”
- BFX9 = “Buffer cell (low threshold voltage, low power) with an output drive strength of 9”
- BFX29 = “Buffer cell (low threshold voltage, low power) with an output drive strength of 29”
- NAND2X2 = “2 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 2”
- NAND2X4 = “2 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 4”
- NAND2X19 = “2 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 19”
- NAND3X3 = “3 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 3”
- NAND3X7 = “3 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 3”
- NAND3X20 = “3 input inverted AND cell (low threshold voltage, low power) with an output drive strength of 20”
- NOR2X2 = “2 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 2”
- NOR2X4 = “2 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 4”
- NOR2X27 = “2 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 27”
- NOR3X3 = “3 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 3”
- NOR3X7 = “3 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 7”
- NOR3X21 = “3 input inverted OR cell (low threshold voltage, low power) with an output drive strength of 27”
- AND2X5 = “2 input AND cell (low threshold voltage, low power) with an output drive strength of 5”

- AND2X29 = “2 input AND cell (low threshold voltage, low power) with an output drive strength of 29”
- OR2X5 = “2 input OR cell (low threshold voltage, low power) with an output drive strength of 5”
- OR2X29 = “2 input OR cell (low threshold voltage, low power) with an output drive strength of 29”
- SDFPQX5 = “A low threshold voltage, low power Data flip flop”

Timing was considered as the parameter of importance because timing violations may lead to circuit failures. Output rise delay and output fall delay were the parameters under observation. Tools internal to ST Microelectronics were the working environment/platforms chosen. The standard cell library production was done using ALTO (advanced library tool). It is a product of STMicroelectronics’s central research and development, Design automation and integrated systems. It is divided into three areas where the first area is a pure logical engine which extracts timing and timing checks, calculates the truth table and generates stimulus. The second area characterizes the cells and produces technology dependent database. The last area generates the Synopsys Technology file also referred to as the .lib file which was used for this analysis. It requires design kits for SPICE models and absolute limits, Library for cell list, operating range, characterization methodology, tool and library compatibility. Lastly it requires cells for functionality and loading.

4.2 AGEING – NEGATIVE IMPACT

In this section we shall have a look on the disadvantages of the ageing phenomena by looking at the negative impacts of these phenomena on the standard library cells.

4.2.1 Threshold Voltage shift due to ageing effect

The ageing analysis was initially carried out at transistor level and later was done at an abstraction level higher than the transistor level that is the gate level. Ring oscillator circuits based on 28nm FD-SOI standard library cells were used as the test subject for the ageing analysis after obtaining data through fresh and reliability simulations. The implementation was divided into sub objectives to give the analysis a proper frame. The very first objective was to observe the effect of BTI and HCI on the threshold voltage of PFET and NFET.

The impact of the ageing mechanisms primarily result in a change in the threshold voltages of transistors and their mobility. This change in threshold voltage further leads to delay degradation in cells/gates which may ultimately result in timing violations or/and functional failures. The PVT dependency of ageing effects have been already studied in-depth in various works and publications. This analysis therefore is done for SS corner at low operating voltage and at low temperature value (ss_0.9V_-40degree Celsius). According to previous studies on greater technology nodes (Bulk CMOS > 60nm) around 50 mV shift for PFET is expected over the entire lifetime. The ageing mechanisms usually manifest themselves as an increase in the threshold voltage value in NFETS and PFETS.

The first observation that can be made here is that the shift in threshold voltage in PFET (which experiences NBTI and HCI) is less than the shift in threshold voltage for NFET (which experiences PBTI and HCI). PBTI in NFET here causes greater degradation than caused by NBTI in PFET. The second observation made here is that the amount of threshold voltage shift increases with the increase in channel length (additional channel length in nm denoted by PBP/PB/P) for NFET. For PFET on the other hand with increase in PB the shift reduces.

Polybias	Time duration	shift-Vth-lin PFET	shift-Vth-sat PFET	Shift-Vth-lin NFET	Shift-Vth-sat NFET
PB0	2ey	35mV	33mV	48mV	48mV
PB0	3ey	38mV	36mV	54mV	54mV
PB0	7ey	44mV	41mV	68mV	68mV
PB16	2ey	33mV	32mv	68mV	68mV
PB16	3ey	36mV	35mv	76mv	75mV
PB16	5ey	39mv	38mv	87mV	86mV

Figure 4-3 Shift in the threshold voltage values of PFET and NFET due to ageing

Further, NFET experiences a symmetric amount of shift in linear and saturation threshold values whereas the PFET has a slightly different amount of shift of linear threshold voltage

value and saturation threshold voltage value. Also there is a significant amount of shift in the threshold voltage values over the ageing period with the maximum portion of the shift being experienced in the very first few years of circuit operation alone.

4.2.2 Asymmetric impact of ageing effects

The analysis at a higher abstraction level that is the gate level is presented in this section. This analysis was done on a ring oscillator circuit made up from the standard library cells as mentioned above. Velamina et al., introduced the concept of asymmetric aging. Our initial aim at the gate level was to observe whether the impact of ageing on rise and fall delays is symmetric or asymmetric and if asymmetric then which delay out of the considered two (rise and fall) was impacted more. It was interesting to note that the cells of the standard cell library did not show a symmetric amount of rise and fall delay degradation. As shown in the figures Figure 4-4 and Figure 4-5 below for considered NOR cells and NAND cells (universal gates) percentage degradation in rise delay dominated thus portraying the asymmetric impact.

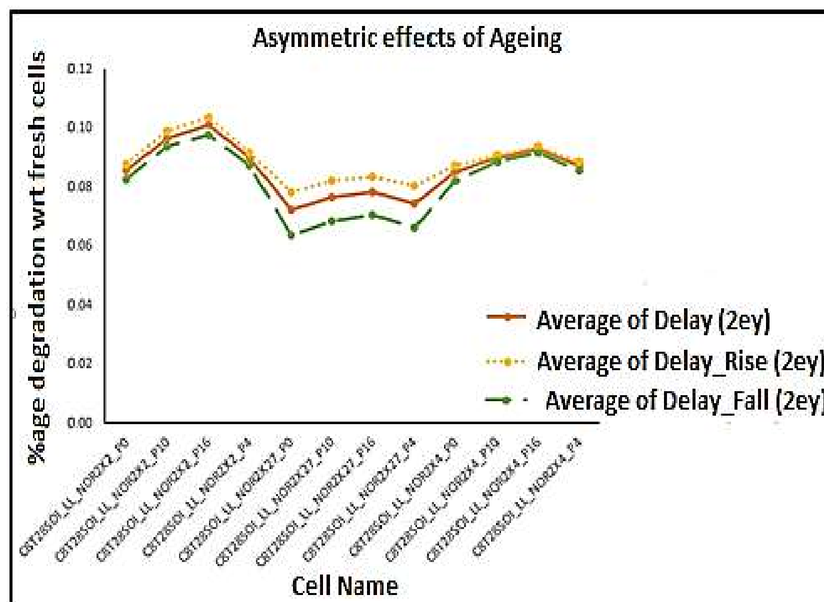

Figure 4-4 Asymmetric ageing impact on NOR cells of standard cell library

The y axis in Figure 4-4 and Figure 4-5 represent the amount of degradation in delay experienced by aged gates compared to fresh gates with the delay of fresh gates taken as a zero reference in terms of percentage value. The x axis denotes the cells under consideration while the rise delay and fall delay along with the total delay is represented by the orange, grey and blue lines respectively.

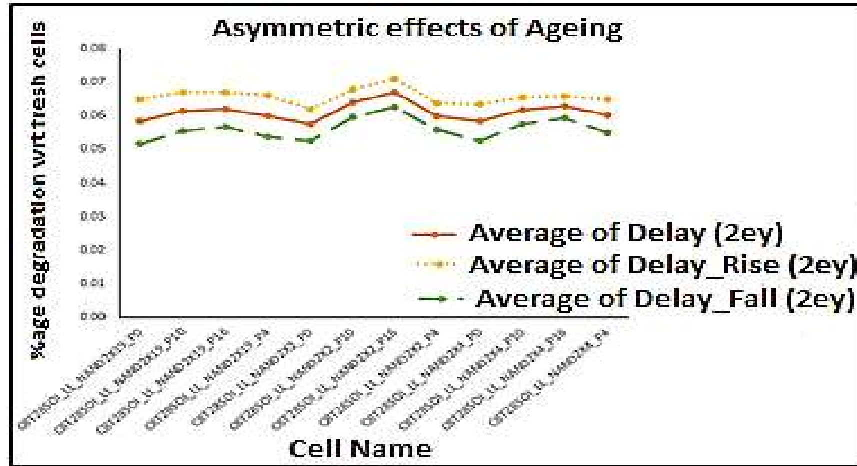

Figure 4-5 Asymmetric ageing impact on NAND cells of standard cell library

4.2.3 Individual Vs Combined impact of BTI and HCI

This section deals with analyzing the individual impacts of BTI and HCI that is when only one of them acts on the device and later determining the cumulative effect of both that is when both HCI and BTI act together. There are four possible combinations for this analysis which are represented in the table below. 1 means impacting and 0 means not impacting.

Table 4-1 BTI and HCI analysis combinations

BTI	HCI	Inference
0	0	Fresh device = 0 age
0	1	HCI acting individually

1	0	BTI acting individually
1	1	Both BTI and HCI acting simultaneously

Table 4-1 shows the different combination of BTI and HCI application. Here a comparison of the average degradation in delay of standard cells in terms of percentage was analyzed. The average of percentage delay degradation obtained for individual cells with same functionality but varying drive strengths was calculated. As seen from the table below BTI individually leads to a greater degradation in cell delay in comparison to the individual impact due to HCI. Moreover, when HCI and BTI act simultaneously the impact on the two as observed is not additive in nature. This may be because the two effects have different physics behind them. HCI is frequency dependent and BTI I impacts as stated previously under applied bias voltages at high temperatures.

The average impact on delay for a standard cell library as in our case is around 7% after the process of ageing keeping the delay of fresh cells as the zero reference which is significant while being observed for a 28nm technology library.

Table 4-2 Individual and combined impact of BTI and HCI on standard cell delay

Standard cell	BTI = 1 HCI =1	BTI = 0 HCI = 1	BTI = 1 HCI = 0
NOR	8.55%	1.89%	8.46%
OR	7.53%	3.02%	7.35%
INVERTER	6.42%	3.69%	6.24%
BUFFER	7.10%	4.83%	6.41%

NAND	6.34%	3.14%	6.21%
AND	5.94%	2.43%	5.90%

As observed in Table 4-2, the effect of BTI and HCI is not additive in nature which means that the two phenomenon interact with each other where their interaction does not cause degradation as a sum of the degradations caused by both individually. Similar are the results observed for rise delay and fall delay.

Table 4-3 Individual and combined impact of HCI and BTI on cell rise

Standard cell	BTI=1 HCI=1	BTI=0 HCI=1	BTI=1 HCI=0
NOR	8.73%	1.52%	8.70%
OR	6.72%	4.49%	6.53%
INVERTER	6.59%	3.83%	6.45%
Standard cell	BTI=1 HCI=1	BTI=0 HCI=1	BTI=1 HCI=0
BUFFER	7.56%	6.31%	6.85%
NAND	6.23%	3.37%	6.19%
AND	6.48%	2.99%	6.44%

Table 4-4 Individual and combined impact of HCI and BTI on cell fall

Standard cell	BTI=1 HCI=1	BTI=0 HCI=1	BTI=1 HCI=0
NOR	8.32%	2.36%	8.14%
OR	8.20%	4.49%	8.03%
INVERTER	6.23%	3.54%	6.00%
BUFFER	6.52%	2.92%	5.83%
NAND	6.49%	2.83%	6.24%
AND	5.37%	1.83%	5.34%

From the above tables, Table 4-2, 4-3 and 4-4 it can be concluded that BTI individually impacts the cell delays in approximately the same amount as observed for both effects impacting the cell together. Also the percentage degradation in delay due to HCI alone on an average is smaller at around 3%.

4.2.4 Channel length dependency of ageing

In this section the variation in the amount of degradation with increasing channel length will be observed. The term PB/PBP/Polybiasing will be used in our work which will reflect the additional channel length. The numerical value following PB/PBP is the length in nanometer added to the original channel length defined/considered for the technology node.

The y axis in the following figure denotes the increase in the delay in terms of percentage for cells aged for two years time duration when compared to the delay in the unaged/fresh cells with aging period of zero years. The x axis represents the PBP value which is the additional channel length value to the defined 28nm channel length. For example, in the table below the values in the first column under Row Labels represent the increased channel length value in

nanometer beyond 28nm technology node. So 0 represents 28nm technology node plus 0nm, 4 represents 28nm technology node plus 4nm and similarly the same follows for the remaining two. The delay model used is the CCS (composite current source) model. Figure 4-6 shows the dependency of degradation due to ageing with extended channel length.

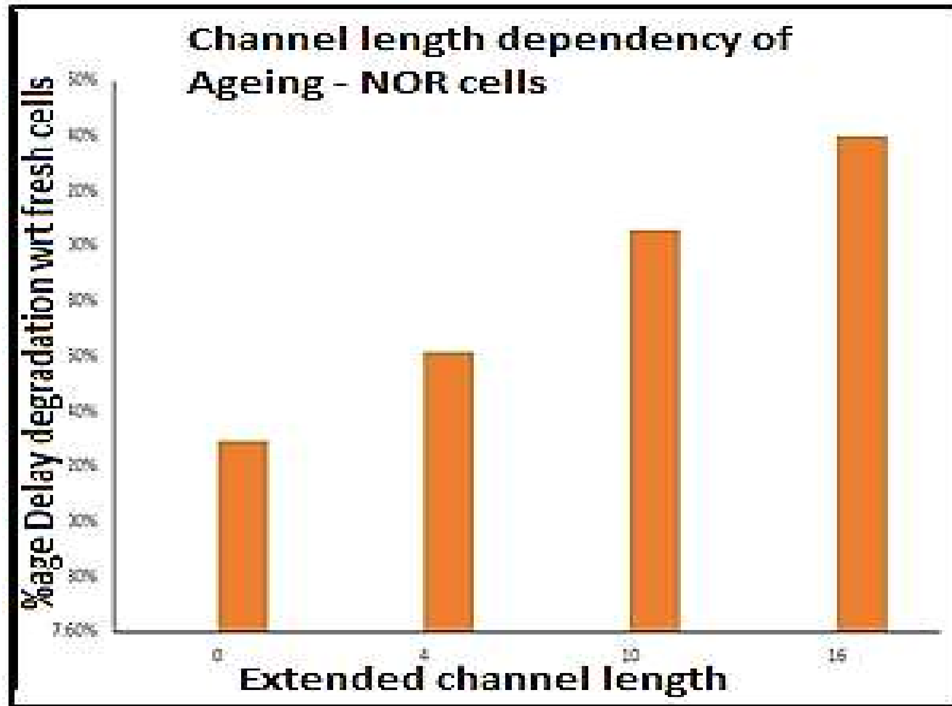

Figure 4-6 Channel length dependency of ageing for a standard cell (NOR) of 28nm FDSOI standard cell library

In the figure above X axis represents the additional channel length of 0, 4, 10 and 16. The Y axis shows the degradation in the delay of the NOR cells of a standard cell library with respect to the delay observed in their fresh counterparts. The NOR cells are exclusively shown here because they experience the maximum degradation out of all the considered cells.It can be observed that with increasing channel length the impact on percentage degradation of delay increases, which can be attributed to the fact that as the channel length increases the length of theoxide – semiconductor interface increases which increases the area for trap generation and trapping of electrons/holes. Figure 4-6 represents the results for basic standard cell NOR

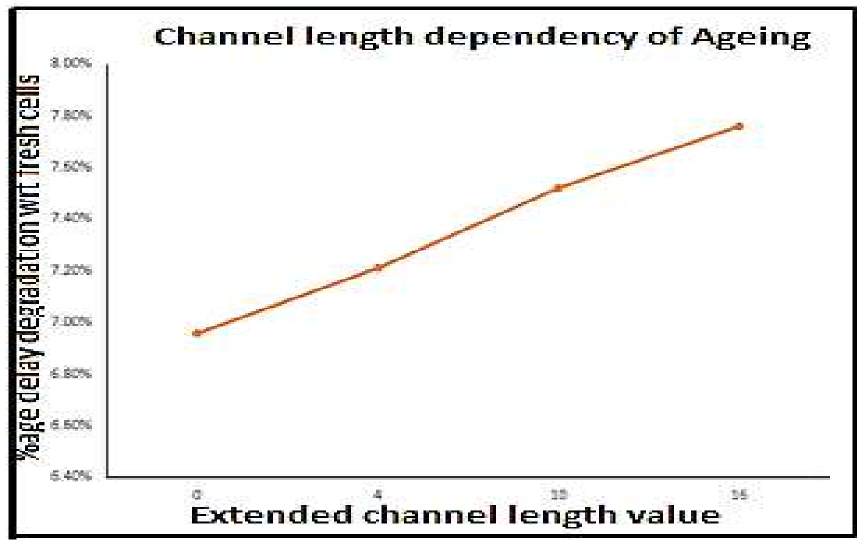

Figure 4-7 Channel length dependency of ageing for all cells of 28nm FDSOI standard cell library

Figure 4-7 represents the general dependency of ageing on cells of a standard cell library. Therefore, it can be concluded that the amount of degradation shows a dependency on the length of the interface between the source and the drain junctions. Longer the channel length more is the impact of ageing effects on the transistors due to the chances of increased trap generation and/or oxide trapping in pre-existing traps.

4.2.5 Drive strength dependency of ageing impacts

Figure 4-8 Ageing impact variation with respect to cell drive strength - NOR

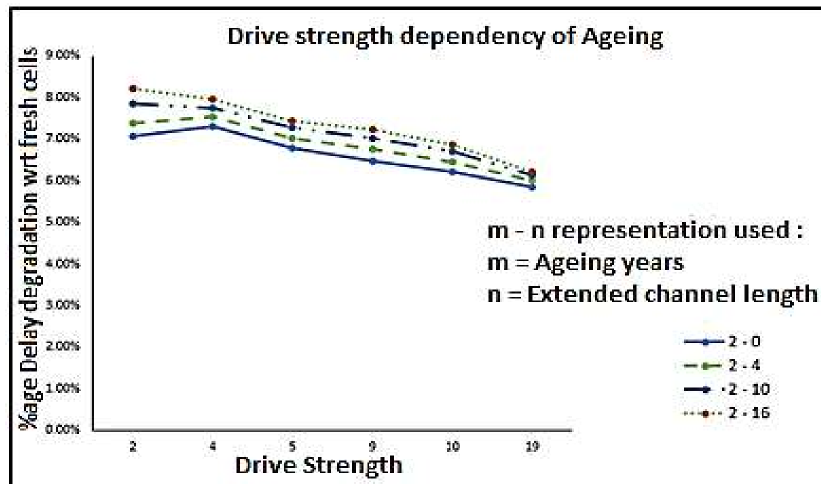

Figure 4-9 Drive strength affecting percentage delay degradation of aged cells (in comparison to fresh cells) in a 28nm FDOI standard cell library

The amount of percentage degradation in delay for aged cells (aged for a period of 2 years) for different drive strengths can be seen in Figure 4-8 and Figure 4-9 respectively. For NOR cells considered in Figure 4-8 we see that the average of delay degradation in percentage after ageing follows the same format with respect to PBP behavior as seen in the previous section of the work whereas for increasing drive strengths the impact of ageing effects decrease with increasing drive strengths. For the entire standard cell library, the trend is almost similar.

4.2.6 Input slew and output load dependency of ageing effects

A standard cell library is characterized over a number of input slopes also known as slew and output loads which helps determine the operation points of the standard cells. The slope at the output of previous gate's determine the present gate input slew. The output load on the other hand is determined by the cells/gates (type and number) connected at a cell's output. The trend for the same can be seen in Figure 4-10, Figure 4-11, Figure 4-12 and Figure 4-13.

A trend appears which shows the slope and load dependency of degradation. Switching strongly depends on the input slope or the input ramp signal said otherwise. It can be observed that the amount of degradation for lesser slopes is less whereas the

amount of degradation in the opposite case that is for greater slopes is more. The trends for the rise delay and fall delay are same and is shown in the following figures.

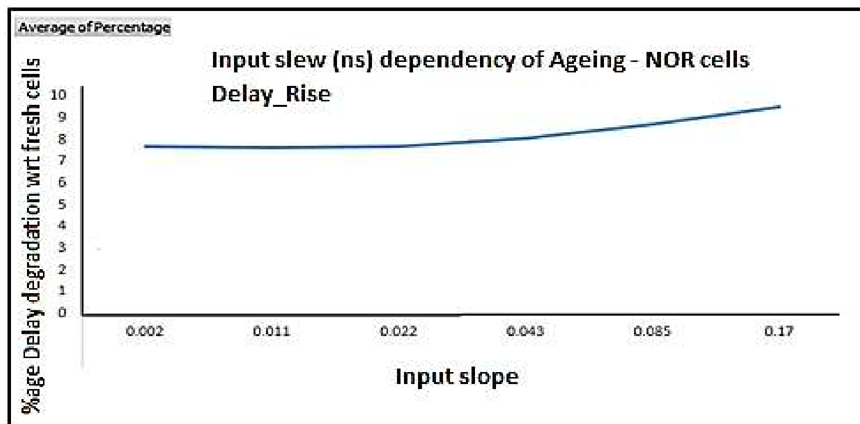

Figure 4-10 Dependency of ageing impact on slew – observed for cell rise

Larger slope causes greater degradation which can be explained by the current level available while switching in case of slow ramps compared to the current level available for faster ramps. STMicroelectronics library characterization however is not able to provide the current during switching therefore this is a possible assumption for the results obtained. The detailed explanation is provided in a document protected under the STMicroelectronics Confidentiality agreement.

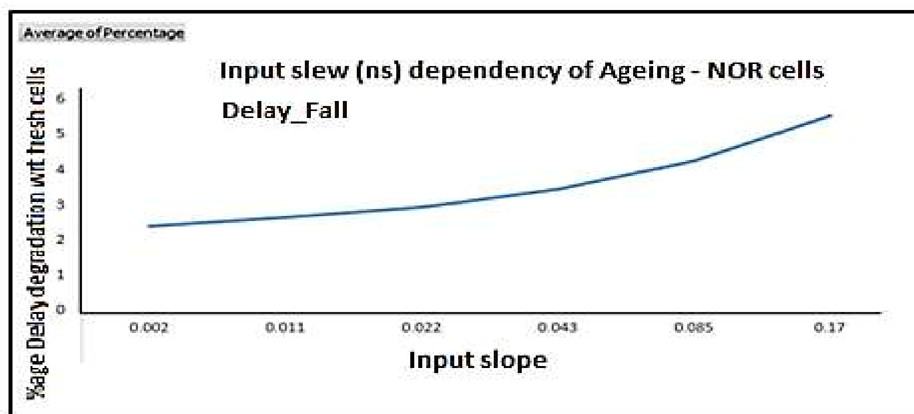

Figure 4-11 Dependency of ageing impact on slew - observed for cell fall

It can be seen that percentage degradation of cell's average delay increase with increasing slope. As for the increasing output load value the percentage degradation decreases. For all the other cells in the library the trend remains the same with the amount of degradation depending on the cell's configuration which is the stacking and multiplicity of the transistors**.**

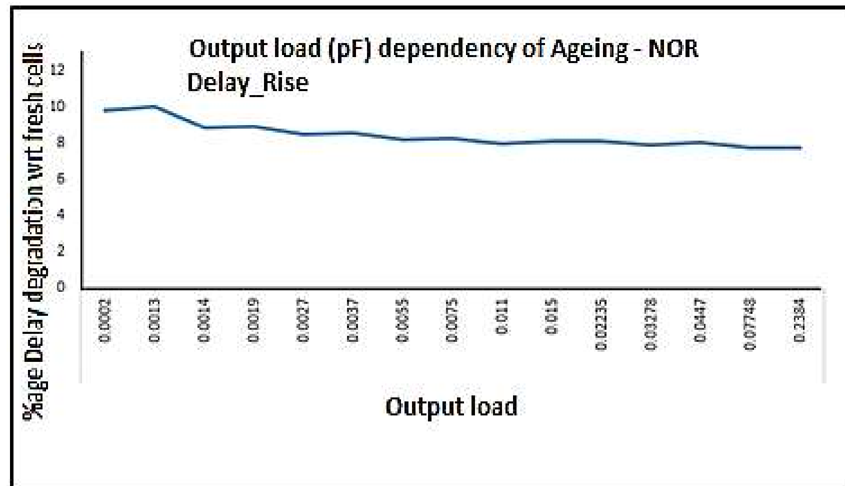

Figure 4-12 Dependency of aging impact on output load - observed for cell rise

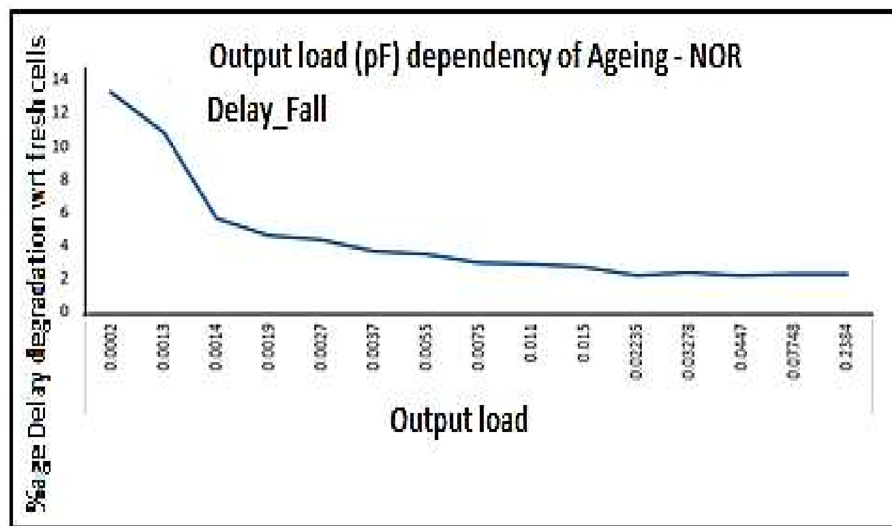

Figure 4-13 Dependency of ageing impact on output load - observed for cell fall

4.3 Ageing – Positive impact

The previous sections of the work focused on the degrading parameters of the cell/gate. In this section we will see the positive impact of BTI and HCI effects. The power trends ccan be seen in Figure 4-14 and Figure 4-15. Power at present is an important area of consideration. Power dissipation if broadly classified, is either static power dissipation or dynamic power dissipation. Here in this work we see that there is reduction in power. There is a significant reduction in the leakage component of power of approximately 40% for NOR cell. The Dynamic power and short-circuit power see insignificant reduction due to the two being independent of the threshold voltage.

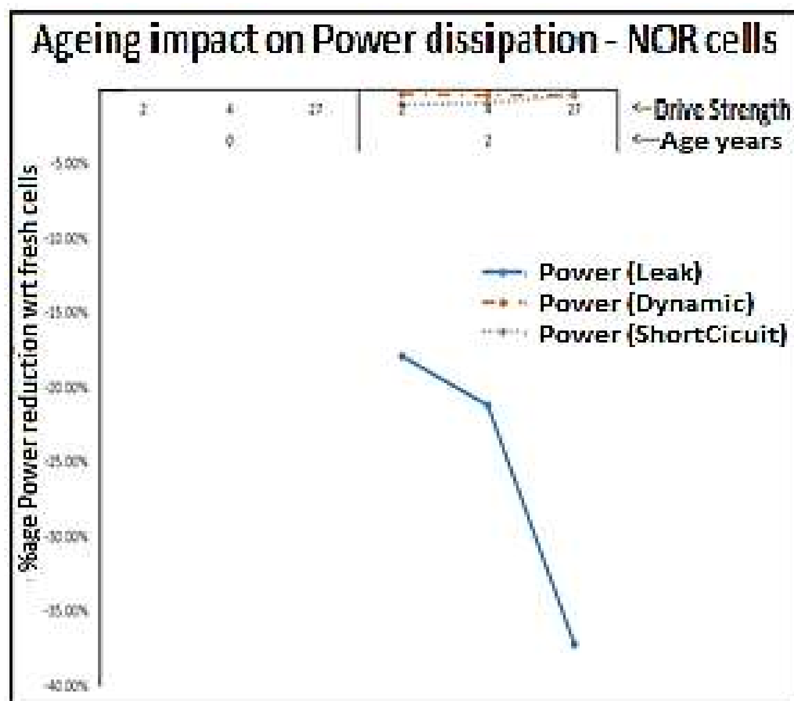

Figure 4-14 Impact of ageing on different components of power - NOR cell

The reduction in power seems to be a positive impact when studied for the above case which represents the impact of ageing on NOR cell's power after 2 years of ageing. Overall the power is reducing but let us see the broader picture.

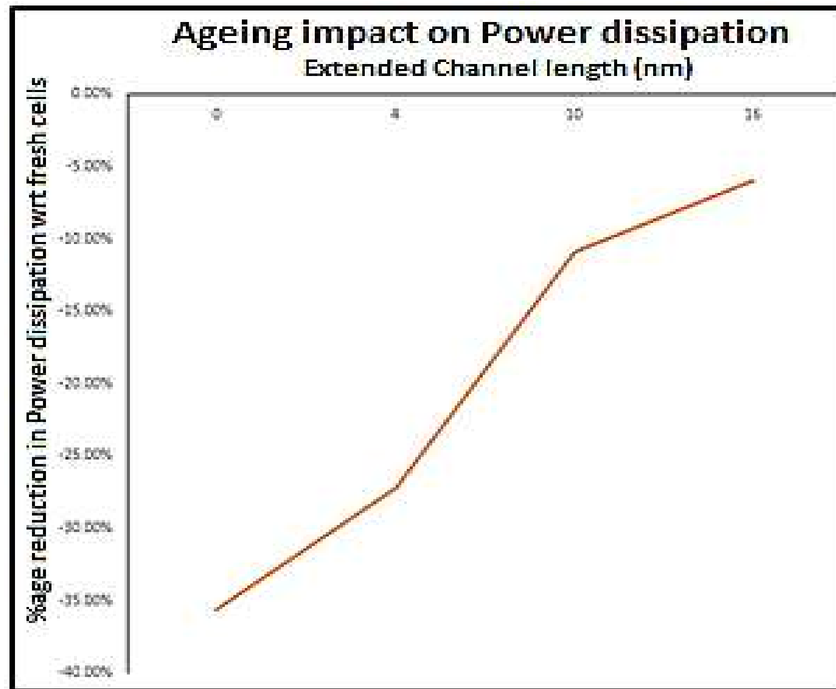

Figure 4-15 A trend of %age decrease in power of aged cells over varying PB values

If we consider the trend of power over extended channel lengths there is definitely a reduction in power as compared to the fresh cells but the power reduction for increasing channel length is not significant. Also it becomes a huge disadvantage as the delay degrades with extended channel lengths and the power also does not reduce by large percentages. Therefore it can be concluded that ageing overall has a huge contribution in circuit delay degradation but the reduction in the leakage component of power is a great benefit in the low power applications.

4.4 AGEING MITIGATION

Mitigation refers to the technique of reducing the severity of a certain process. As seen in the previous sections ageing causes degradation in a device which leads to device failure. This requires unnecessary design margins which increases designer's efforts along with the increase in design cost and complexity. Therefore design techniques to mitigate ageing are necessary. This chapter deals with one such technique to lessen the impact of ageing. Transistor sizing helps in ageing mitigation as seen in Figure 4-16.

β ratio is defined as the ratio of the width of PFET to the width of NFET. A standard cell library's height is constant (sum of the widths of PFET and NFET). Transistor sizing in such a case means changing the widths of PFET and NFET maintaining the β ratio constant. Hence, transistor sizing is done in such a way so that the standard cell height remains fixed. The sizing is done by maintaining the stage ratio of the adjoining stages in a stage configuration. Results for the same are depicted in the table below. The analysis is done for basic Inverter and Buffer cell at two operating voltage values of 0.6V and 0.9V.

INVERTER_P0

	0.6V - supply			0.9V - supply		
β Ratio	Delay (Δ%)	Delay Rise (Δ%)	Delay Fall (Δ%)	Delay (Δ%)	Delay Rise (Δ%)	Delay Fall (Δ%)
0.28	25.07	24.18	26.18	7.88	7.59	8.35
0.38	23.83	22.61	25.27	7.99	7.25	8.09
0.58	22.23	20.79	23.83	7.17	6.91	7.52
0.85	21.10	19.35	22.98	6.84	6.75	6.94
1	20.65	19.01	22.37	6.66	6.63	6.69
1.17	20.13	18.54	21.79	6.50	6.53	6.47
1.27	19.88	18.23	21.58	6.49	6.56	6.41
1.37	19.70	17.98	21.48	6.47	6.61	6.31
1.45	19.50	17.72	21.34	6.42	6.58	6.23

BUFFER_P0

	0.6V - supply			0.9V - supply		
β Ratio	Delay (Δ%)	Delay Rise (Δ%)	Delay Fall (Δ%)	Delay (Δ%)	Delay Rise (Δ%)	Delay Fall (Δ%)
0.85	21.32	23.67	18.87	7.02	8.05	6.21
1	20.92	23.37	18.56	6.92	7.92	6.19
1.17	20.47	22.94	18.27	6.88	7.83	6.25
1.27	20.32	22.83	18.18	6.85	7.78	6.26
1.37	20.23	22.79	18.12	6.81	7.71	6.26
1.45	20.12	22.71	18.04	6.79	7.72	6.24

Figure 4-16 Transistor sizing – Lessening the impact of ageing

It is observed that with the increase in the β ratio the degradation of delay decreases. Also for larger supply voltages the degradation is less. Transistor sizing is a good solution to mitigate ageing effects but it has an area overhead associated to it. There are many other techniques as well that have been proposed by researchers which include low power techniques like AVS (adaptive voltage scaling), frequency scaling, body biasing etc.

CHAPTER 5

5 CONCLUSION and FUTURE SCOPE

Our analysis on standard cell library leads to the following conclusions:

- The impact of BTI and HCI is asymmetric in nature. Degradation of rise delay and fall delay are different.
- BTI and HCI are interactive but not additive. Individual effects of both ageing phenomenon cannot be added up to estimate their combined impact.
- BTI degrades the delay of the cell by a much larger percentage in comparison to HCI.
- Ageing effects worsen for transistors with the increase in channel length.
- With increase in the drive strength of a cell/gate the percentage degradation on average of delay reduces.
- On the transistor level of abstraction the threshold voltage of a PFET and NFET are affected. The threshold voltage for the transistors degrade.
- Only the leakage component of power is greatly affected by ageing, the remaining components of power remain nearly unaffected due to them not being dependent on the threshold voltage.
- The leakage power component sees an improvement by approximately 40% thus proving beneficial for low power applications.
- Transistor sizing is an effective way to mitigate impact of ageing.

As a continuation of this work in future new techniques including newer technologies, new architectures and use of existing approaches such as the low power approaches can be thought of as a way to mitigate ageing. The reduction in power can be considered as a primary focus to move in the direction of designing an ageing and power reliable device. The analysis done in this work can be beneficial for designers while keeping margins to design circuits. Ageing causes circuit degradation therefore needs proper attention.

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