Design and Analysis of CMOS Combined Reference Circuit

A dissertation submitted in partial fulfillment of the

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Submitted by

Madhusoodan Agrawal

Roll No. 601161021

Under the supervision of

Dr. Alpana Agarwal

Associate Professor, ECED

Thapar University, Patiala

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT

THAPAR UNIVERSITY
(Established under the section 3 of UGC Act, 1956)
PATIALA – 147 004 (PUNJAB)

Declaration

I hereby declare that the dissertation report entitled **"Design and Analysis of CMOS Combined Reference Circuit"** is an authentic record of my work carried out as requirement for the award of degree of M.Tech (VLSI Design & CAD) at Thapar University, Patiala, under the supervision of **Dr. Alpana Agarwal**, Associate Professor, ECED and refers other researcher's work which are duly listed in the reference section.

The matter embedded in this dissertation has not been submitted in any other University/Institute for the award of any degree.

Date: 14/06/2013

Madhusoodan Agrawal

Roll No. 601161021

It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

Alpana Agarwal
Associate Professor, ECED
Thapar University, Patiala

Countersigned by:

Head
Electronics & Communication
Engineering Department
Thapar University, Patiala

Dean of Academic Affairs
Thapar University, Patiala

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Madhusoodan Agrawal
Roll no. 601161021

Abstract

This work presents the design of CMOS Combined Reference Circuit with Supply and Temperature compensation using 0.18 μm UMC technology. It consists of a start-up circuit, a current generator, and a voltage generator.

Many current reference and voltage reference circuits have been reported. The references are used individually for generating fixed value of current or voltage for the particular use in mixed signal design. These individual current and voltage reference circuits fail, when there is a requirement of both fixed current and voltage in any circuit, *e.g.* a oscillator circuit requires both current and voltage reference. So the main aim of this work is to offer a design methodology for a combined reference circuit, which provides both current as well as voltage with a better supply and temperature independency.

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List of Symbols

V_{DD}	Positive supply voltage
V_{SS}	Negative supply voltage
I_D	Drain current
K_p	PMOS process trans-conductance parameter
K_n	NMOS process trans-conductance parameter
W	Channel Width
L	Channel length
μ_n	Mobility of electrons
μ_p	Mobility of holes
C_{OX}	Oxide capacitance
I_o	Bias current
V_T	Threshold voltage
V_{GS}	Gate to source voltage
V_{DS}	Drain to source voltage
I_{REF}	Reference current
V_{REF}	Reference voltage
R_{in}	Input resistance
λ	Channel length modulation parameter

Abbreviations

Opamp	Operational Amplifier
CMOS	Complementary Metal Oxide Semiconductor
ESD	Electrostatic Discharge
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PTAT	Proportional to Absolute Temperature
NMOS	N-channel Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
RF	Radio Frequency
CAD	Computer Aided Design
UMC	United Microelectronics Corporation
BJT	Bipolar Junction Transistor
CM	Current Mirror
SS	Slow NMOS Slow PMOS
TT	Typical NMOS Typical PMOS
FF	Fast NMOS Fast PMOS
SF	Slow NMOS Fast PMOS
FS	Fast NMOS Slow PMOS

Chapter 1 Introduction

1.1 Introduction

The modern Application Specific Integrated Circuits (ASICs) are systems usually composed by mixed-signal blocks (analog and digital), as shown on Figure 1.1 [1]. The analog blocks, in particular, need to be biased by voltage and current references, the accuracy of reference circuits certainly determine the maximum performance of all blocks.

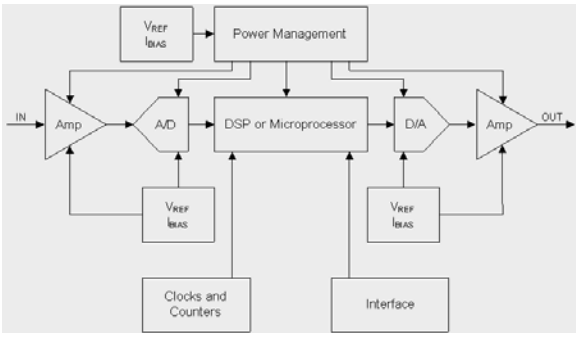


Figure 1.1: A Generic Mixed-Signal ASIC [1]

Reference Circuit is a key component in the design of many analog and mixed signal applications including PLL, Analog-to-Digital Convertor (ADC), Voltage Regulators, Digital to Analog Convertor (DAC) and many other measurement and control systems. Voltage references vary widely in performance; a regulator for a computer power supply may only hold its value to within a few per cent of the nominal value, whereas laboratory voltage standards have precisions and stability measured in parts per million.

A voltage reference must be inherently well defined and insensitive to temperature, power supply and fabrication process. The resolution of an ADC or DAC converter is limited by the precision of its reference voltage over operating temperature ranges. A voltage reference is an electronic device that produces a fixed voltage irrespective of the power supply variations, temperature changes, and the process variation.

The most common voltage reference circuit used in integrated circuits is the bandgap voltage reference. It may be integrated into a data converter, included in the microprocessor or be a standalone IC.

In the voltage mode, a bandgap circuit is implemented to ensure the correct biasing over a wide temperature range, but in the current mode it is much more difficult to obtain this level of performance [2].

1.2 Organization of Dissertation Work

The Dissertation is organized as follows:

Chapter 1: This chapter gives an overview of Reference Circuit.

Chapter 2: The comparative study of different types of current and voltage reference with their applications is discussed in this chapter.

Chapter 3: This chapter discusses the design and Layout of Proposed CMOS Combined Reference Circuit.

Chapter 4: The Various Simulation and Results of Proposed CMOS Combined Reference Circuit has been discussed in this chapter. This chapter also discusses results of designed circuit at different corners.

Chapter 5: A brief conclusion and possible improvements have been discussed in this chapter.

Chapter 2 Literature Review

Analog circuits incorporate voltage and current references extensively. Such References are dc quantities that exhibit little dependence on the temperature and power supply [3].The large-signal current and voltage characteristics of an Ideal current and voltage reference are shown in Figure 2.1 [4].

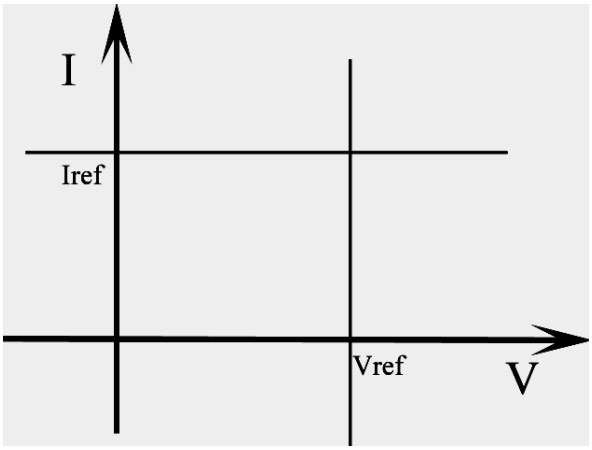


Figure 2.1: *I-V* characteristics of Ideal current and voltage references [4]

In this section, we deal with the design of reference generators in CMOS technology. The main objective of reference generation is to establish a dc voltage or current that is supply independent, process independent and temperature independent [3].

A precision voltage reference and current reference circuit is very important in the design of mixed-signal and analogue integrated circuits such as differential amplifier, and data convertors [3]. Reference voltages with little dependence to temperature prove useful in many analog circuits. As many process parameters vary with temperature, if a reference is temperature-independent, it is usually process independent as well. If two quantities with opposite temperature coefficient are added with proper weighting, the resultant quantity theoretically exhibits zero temperature coefficient [5].

2.1 Current Reference Circuits

Current Reference is a basic building block in analog circuits as a bias source for oscillators, amplifiers, PLL's and etc. All mentioned applications make extensive use of current

references and their accuracy is strongly related to the temperature and process stability of these references. This section describes some basic and advanced current references in bipolar and CMOS technology.

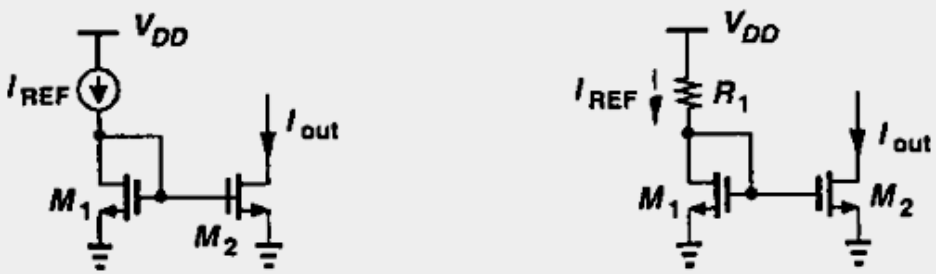
2.1.1 Current Mirror

Figure 2.2(a) shows the basic current mirror which is a conventional method of biasing. Since $V_{GS1}= V_{GS2}$ the same current or a multiple of the current in M_1 will be copied to each stage on basis of the sizes of each transistor, provided all transistors stay in saturation region. The current I_{D1} is given by

$$I_{D1} = \frac{\beta_1}{2}(V_{GS1} - V_{THN})^2 \tag{2.1}$$

If M_2 is assumed in saturation region, the current flowing in M_2 is

$$I_{D2} = I_o = \frac{\beta_2}{2}(V_{GS2} - V_{THN})^2 \tag{2.2}$$



(a) (b)

Figure 2.2: Current-mirror biasing using (a) an ideal current source (b) a resistor [3]

Since $V_{GS1} = V_{GS2}$, the ratio of the drain currents is given by

$$\frac{I_{D2}}{I_{D1}} = \frac{W_2 L_1}{W_1 L_2} = \frac{\beta_2}{\beta_1} \tag{2.3}$$

This equation shows *W/L* ratio of the two devices to can be adjusted to achieve the desired output current. If I_{REF} does not vary with V_{DD} and channel length modulation of M_2 is

neglected, then I_D remains independent of the supply voltage. A resistor is tied from V_{DD} to the gate of M1 (Figure 2.2(b)) .Now the output current of this circuit is sensitive to V_{DD}.

$$\Delta I_{out} = \frac{\Delta V_{DD}}{R_1 + 1/g_{m1}} \cdot \frac{(W/L)_2}{(W/L)_1} \tag{2.4}$$

These references are required to be stable over process, power supply voltage, and temperature variations.

In order to get supply independent current, the circuit must bias itself *i.e.* I_{REF} must be derived from I_{out}. The idea is that if I_{out} is to be independent of V_{DD} then I_{REF} is the copy of I_{OUT}. In Figure 2.3, M_3 and M_4 copy I_{out}, thereby defining I_{REF}. If M_1- M_4 operates in saturation and channel length modulation is neglected then the following relation can be obtained.

$$I_{REF} = K.I_{out} \tag{2.5}$$

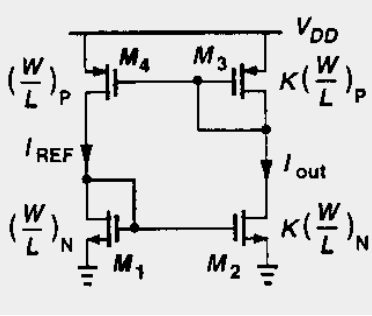


Figure 2.3: Simple supply independent current reference [3]

Since, a current source is fed to each diode connected device, I_{out} and I_{REF} are relatively independent from V_{DD}.

2.1.2 Beta multiplier reference

For defining currents uniquely a resistor R_S is used (Figure 2.4(a)). This configuration is known as beta multiplier reference.

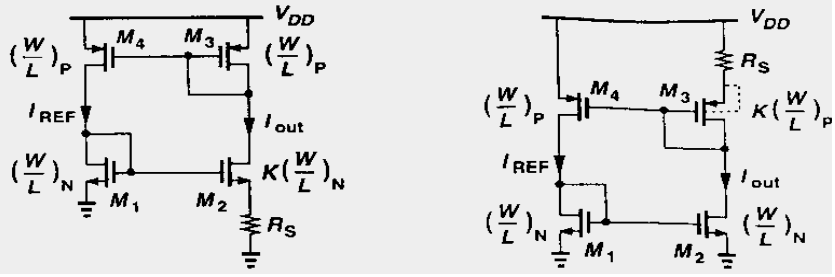


Figure 2.4: Beta multiplier reference [3]

The width of M_2 is made K times larger than the width of M_1 and L_1=L_2, so that

$$\beta_2 = K \cdot \beta_1 \tag{2.6}$$

Therefore, it can be written

$$V_{GS1} = V_{GS2} + I_{D2}R_S$$

Or

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}\left(W/L\right)_N}} + V_{TH1} = \sqrt{\frac{2I_{out}}{\mu_n C_{ox}K\left(W/L\right)_N}} + V_{TH2} + I_{out}R_S \tag{2.7}$$

On neglecting body effect, we have

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox}\left(W/L\right)_N}}\left(1-\frac{1}{\sqrt{K}}\right) = I_{out}R_S$$

And hence

$$I_{out} = \frac{2I_{out}}{\mu_n C_{ox}\left(W/L\right)_N} \cdot \frac{1}{R_S^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \tag{2.8}$$

This is the basic design equation for this reference. The size parameter K must always be greater than 1. In the above calculation, it is assumed that V_{TH1} and V_{TH2} are equal but in actual these are not equal because the sources of M_1 and M_2 are at different potential. To

avoid this problem the resistor is placed at the source of M_3 (Figure 2.4(b)) while tying source and bulk of each PMOS transistor for eliminating body effect.

2.2 Voltage References

Reference voltages with little dependence to temperature prove useful in many analog circuits. As many process parameters vary with temperature, if a reference is temperature-independent, it is usually process independent as well. If two quantities with opposite temperature coefficient are added with proper weighting, the resultant quantity theoretically exhibits zero temperature coefficient [5].

A voltage reference is an analog circuit block that generates a voltage of known magnitude with little dependence on supply or process variations and with a well defined dependence on temperature. Voltage references are applied in order to bias other circuits (i.e. to set transistors in the proper operating region), to quantify a physical property (i.e. to use a signal as a standard by A/D and D/A converters and measurement systems such as temperature sensors), and to stabilize supply as part of a voltage regulator.

The latter, voltage stabilization, may also be a needed in order to the voltage reference itself in order to suppress sensitivity to supply variations. This kind of sub circuit is referred to as a reference voltage stabilizer. The supply variations it aims to suppress can be caused by numerous internal and external sources and over a wide range of frequencies: from a slowly declining battery level to fast transients of the switching digital circuits.

2.2.1 Conventional Bandgap Voltage Reference

The bandgap voltage reference is required to exhibit both high power supply rejection and low temperature coefficient, and is probably the most popular high performance voltage reference used in integrated circuits today. Among various devices in the semiconductor technology, the characteristics of the bipolar transistors have proven the most reproducible and well-defined quantities that provide positive and negative temperature coefficients. Figure 2.5 shows the basic principle of bandgap reference. The forward voltage of a p-n junction diode or the base-emitter voltage of bipolar transistor exhibits a negative TC. The PTAT term is realized by amplifying the voltage difference of two forward-biased diodes

(i.e. base-emitter junctions).Thus a reference voltage with zero temperature coefficient is obtained and given by:

$$V_{ref} = V_{BE} + K \cdot V_{PTAT} \tag{2.9}$$

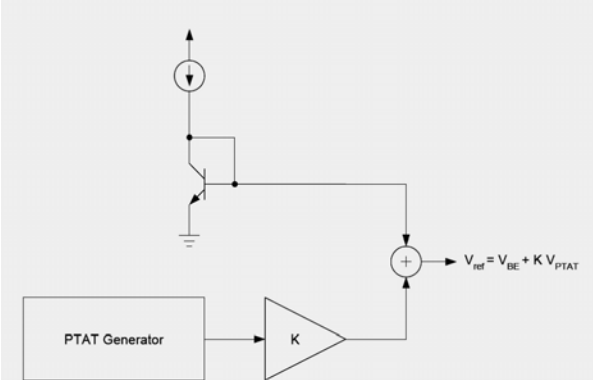


Figure 2.5: Principle of bandgap reference [3]

For bipolar transistor the collector current

$$I_C = I_S \exp\left(V_{BE} \big/ V_T\right) \tag{2.10}$$

Where, $V_T = \frac{k.T}{q}$, I_S is the saturation current which is proportional to $\mu\, kTn_i^2$ where μ is the is the mobility of minor carrier and n_i is the carrier concentration of silicon. Again the temperature dependency of μ and n_i are represented by

$$\mu \propto \mu_0 T^m$$

$$n_i^2 \propto T^3 \exp\left(-E_g \big/ kT\right)$$

Where $m \approx -3/2$ and $E_g \approx 1.12eV$ is the bandgap energy of silicon. Thus it is given by

$$I_S = bT^{4+m} \exp\left(E_g \big/ kT\right) \tag{2.11}$$

Where, b is proportionality factor. For simplifying the analysis the I_C is assumed constant with temperature. Taking the derivative of I_C with respect to T and by using the above equation (2.11), the temperature coefficient of base emitter voltage is obtained and given by

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_T}{T}\ln\frac{I_C}{I_S} - (4+m)\frac{V_T}{T} - \frac{E_g}{kT^2}V_T = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \qquad (2.12)$$

This is negative and has revealing dependence on the magnitude of V_{BE} itself. Exact Cancellation of the dependence of V_{ref} to temperature is not possible because of component tolerances and second order effects such as the nonlinearity of the dependence of V_{BE} on temperature. For PTAT term two bipolar transistors operate at unequal current densities are used, (as shown in Figure 2.6).

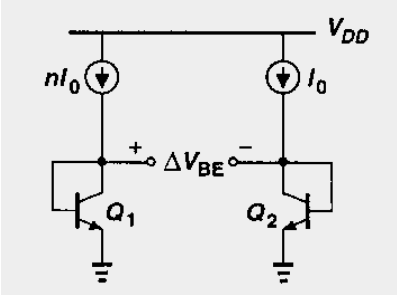


Figure 2.6: Generation of PTAT voltage [3]

Now the difference between their base-emitter voltages is given by

$$\Delta V_{BE} = V_{BE1} - V_{BE2}$$

$$V_T \ln\frac{nI_0}{I_{S1}} - V_T \ln\frac{I_0}{I_{S2}} = V_T \ln n \qquad (2.13)$$

Thus, V_{BE} exhibit positive temperature coefficient, which is given by

$$\frac{\partial V_{BE}}{\partial T} = \frac{k}{q}\ln n \qquad (2.14)$$

With the negative and positive TC, a reference (V_{REF}) having a zero temperature coefficient can be developed and given by

$$V_{REF} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n) \tag{2.15}$$

At room temperature, $\frac{\partial V_{BE}}{\partial T} \approx -1.5mV/K$, whereas $\frac{\partial V_T}{\partial T} \approx +0.087mV/K$. If α_1=1 then for zero TC, $\alpha_2 \ln n$ is chosen such that $\alpha_2 \ln n(0.087) = 1.5$.

A conventional CMOS bandgap reference for n-well process is shown in Figure 2.7. Transistors Q1 and Q2 are assumed to have emitter base areas of A_{E1} and A_{E2}, respectively.

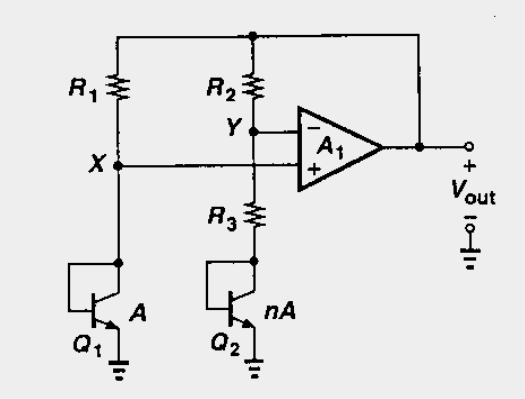


Figure 2.7: Implementation of bandgap reference [3]

If offset voltage of op-amp is assumed to be zero, then

$$V_{out} = V_{BE2} + \frac{V_T \ln n}{R_3}\left(1 + \frac{R_2}{R_3}\right) \tag{2.16}$$

Where n = A_{E2} / A_{E1}. The first term is the CTAT term and the second the PTAT term.

2.2.2 DTMOST Based Bandgap Reference Circuit

In classical bandgap reference circuit, (as shown in Figure 2.7), the output voltage is the sum of a base to emitter voltage diode voltage and the voltage drop across R3. When properly designed, bandgap reference circuits give an output voltage that is somewhat higher than the material bandgap extrapolated to 0 K; for mainstream CMOS processes 1.2 V. A dynamic threshold MOS transistor (DTMOST) can be used in place of BJT as shown in Figure 2.8, which is suitable for the reduced supply voltage range. On layout level, this device is basically a MOS transistor with an interconnected well and gate. For twin well p-substrate

CMOS processes, only the P-type DTMOST's can be used due to the fact that their N-wells can be controlled: the P-well of N-type DTMOST's has a low-ohmic path to the P-substrate. In the DTMOST, the well is connected to the gate. The Diode connected BJT has an exponential voltage-to-current relationship above 650mV while the DTMOST device is exponential within a region from 100mV to 220mV. Voltage across the DTMOST is conversely proportional to the absolute temperature [6].

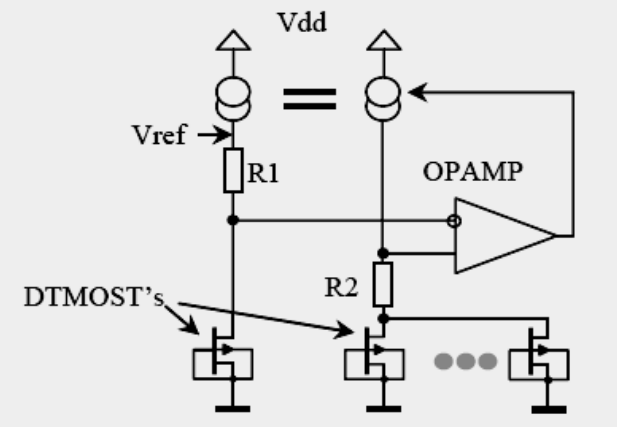


Figure 2.8: Architecture of DTMOST Based Band gap Voltage Reference Circuit [6]

2.2.3 Voltage reference based on Compensation of Mobility and Threshold Voltage Temperature Effects

The CMOS voltage reference shown in Figure 2.9 uses compensation of mobility and threshold voltage temperature effects. In this reference, the nested connection of two NMOS transistors M_1 and M_2 supplies a PTAT term, and the diode-connected NMOS transistor M_3 supplies a CTAT term. These two circuits are connected in series via an operational amplifier, and the resulting voltage that appears in the output stage of this amplifier has low temperature coefficient [7].

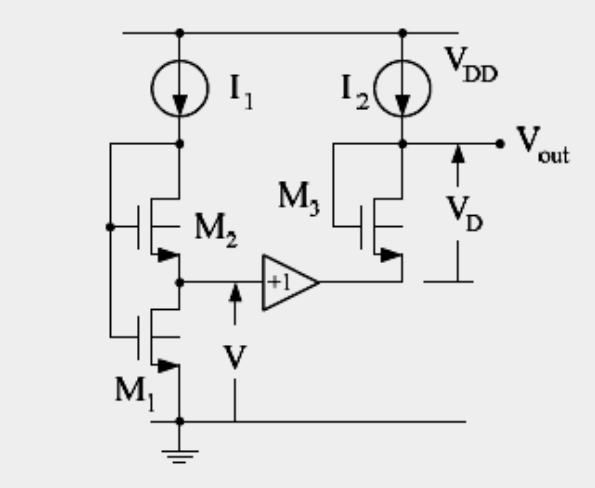


Figure 2.9: Voltage reference based on Compensation of Mobility and V_{TH} Temperature Effects [7]

In the nested connection transistor M_1 operates in triode region, and M_2 operates in saturation. Thus the current I_1 can be given by

$$I_1 = K_1[(V_{GS1}-V_{TN})V-(V^2/2)] \quad (2.17)$$

and

$$V_{GS2} = V_{TN} + [(2I_1)/K_2]^{1/2} \quad (2.18)$$

Where $K_i = \mu_n C_{ox} (W / L)_i$, V_{TN} is the threshold voltage of NMOS transistors, and VGS_i (i =1,2) is the transistor gate-source voltage (the body effect is neglected).

In addition

$$V_{GS1} = V + V_{GS2} \quad (2.19)$$

Substituting (2.17) and (2.19) in (2.18) one obtains that

$$I_1=K_1 [(K_1/K_2)^{1/2}\{(K_1/K_2)+1\}^{1/2}+(K_1/K_2)+(1/2)]V^2 \quad (2.20)$$

Finally, inverting (2.20) one finds that

$$V = A\sqrt{(2I_1)/(\mu_n C_{ox})} \quad (2.21)$$

Where,

$$A = [\sqrt{(L/W)_1 + (L/W)_2} - \sqrt{(L/W)_2}]$$

Assume, for a while, that the current I_1 is constant. The mobility μ_n is decreasing with an increase of temperature. Hence, the voltage V is also increasing with temperature. The temperature coefficient of this voltage, hence, can be found as

$$\frac{\partial V}{\partial T} = -\frac{A}{2}\sqrt{\frac{2I_1}{\mu_n C_{ox}}}\left(\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T}\right) = -\frac{V}{2}\left(\frac{1}{\mu_n}\frac{\partial \mu_n}{\partial T}\right) \tag{2.22}$$

It is known that

$$\mu_n \approx \mu_{n0}(T / T_0)^{-2} \tag{2.23}$$

Substituting this result in (2.22) one can find that

$$\partial V / \partial T \approx V / T \tag{2.24}$$

To take into consideration the body effect for M_2 one may consider that the threshold of this transistor is increased by

$$\Delta V_{TH} \approx (\gamma V)/(2\sqrt{2|\phi_f|}) \tag{2.25}$$

and reduce the voltage V in (2.24) by this value. The simulations show that one may neglect the temperature dependence of the body effect coefficient γ and the Fermi voltage Φ_f and consider that

$$\frac{\partial V}{\partial T} \approx \frac{V}{T}\left(1 - \frac{\gamma}{2\sqrt{2|\phi_f|}}\right) \tag{2.26}$$

The voltage V_D at the diode-connected transistor M_3 is equal to

$$V_D = V_{TN} + \sqrt{\frac{2I_2}{\mu_n C_{ox}(W/L)_3}} = V_{TN} + V_{ov} \tag{2.27}$$

Where, V_{ov} is the overdrive voltage. Using (2.23) again one finds that

$$\frac{\partial V_D}{\partial T} \approx \frac{\partial V_{TN}}{\partial T} + \frac{\partial V_{ov}}{T} \tag{2.28}$$

The first term in (2.28) has a negative value. It is defined by the technology and varies from –0.4 to –4mV/°C. This value is usually higher than $\partial V / \partial T$. But the second term is positive, and one can adjust the coefficient $\partial V_D / \partial T$ using the different values of I_2 to the value which is required to compensate $\partial V / \partial T$. Hence, the following equation should be satisfied in the circuit design.

$$\frac{\partial V_{out}}{\partial T} = \frac{V + V_{ov}}{T} + \frac{\partial V_{TN}}{\partial T} \approx 0 \tag{2.29}$$

The influence of the body effect of the transistor M_3 may be, as with M_2 above, in the first approximation, neglected as well.

2.2.4 Threshold voltage based CMOS voltage reference

This CMOS voltage reference design uses the temperature dependence of NMOS and PMOS threshold voltages to form a temperature-insensitive reference. No diodes or parasitic bipolar transistors are used. The circuit architecture accommodates a wide range of output voltages. The basic operation of long-channel MOS devices is described by the following equations. In the active region [8]:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_{tn})^2 \tag{2.30}$$

and in the linear region:

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)\left((V_{GS} - V_{tn})V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right) \tag{2.31}$$

Where C_{ox} is the gate capacitance per unit area, μn and μp are the mobility of electrons and holes respectively near the silicon surface. W and L are gate width and length and Vtn is the threshold voltage of an NMOS device (Vtp is used for a PMOS device). In these equations, mobility, μ_n and threshold voltage, Vtn both are two important temperature dependent parameters.

$$V_T(T_{device}) = V_T(TNOM) + \left(KT1L + \frac{KT1L}{Leff} + KT2V_{BS}\right) \times \left(\frac{T_{device}}{TNOM} - 1\right) \tag{2.32}$$

where V_T(TNOM) is the threshold voltage at a nominal temperature, KT1 is the TC of the threshold voltage, KT1L is the channel-length coefficient of the threshold voltage's temperature dependence and KT2 is the bulk-bias coefficient of the threshold voltage's temperature dependence. This linear model has been found to provide an excellent fit for the I–V characteristics at various temperatures [9].

The mobility factor, on the is a nonlinear function of temperature [9] and its temperature dependence is given by

$$U0(T_{device}) = U0(TNOM) \times \left(\frac{T_{device} + 273.15}{TNOM + 273.15} \right)^{UTE} \quad (2.33)$$

Where U0(TNOM) is the mobility at a nominal temperature and UTE is the temperature coefficient for U0, which is typically in the range –2.0 to –1.5.

Since mobility is a nonlinear function of temperature, it is difficult to build voltage references that rely on MOSFET characteristics. In this design, the mobility factor is cancelled completely. This voltage reference is based upon two voltages, V_P and V_N that are proportional to PMOS device threshold voltage and NMOS device threshold voltage, respectively and thus linear with temperature. By subtracting V_P and V_N, the TCs are cancelled and the resulting voltage can be adjusted to the desired output reference voltage [6]. The basic concept of this reference circuit is shown in Figure 2.10.

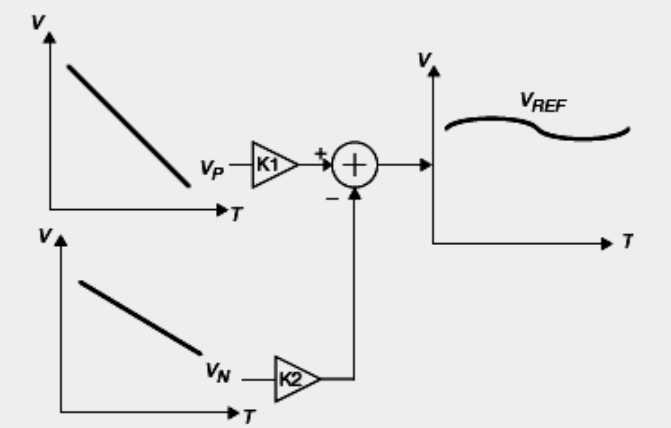


Figure 2.10: Concept of Threshold voltage based CMOS voltage reference [8]

Figure 2.11 shows the schematic implementation of this voltage reference. In block I, V_P is generated using PMOS transistors MP_1 and MP_2. Similarly Block II generates V_N using NMOS transistors MN1 and MN_2. The two voltages are then combined by a subtractor to generate a zero-TC reference voltage in block III. Owing to the op amps, V_P and V_N are both supply independent. MP_3 and MP_4 are start-up devices to avoid an operating point at 0V; they are off during normal operation.

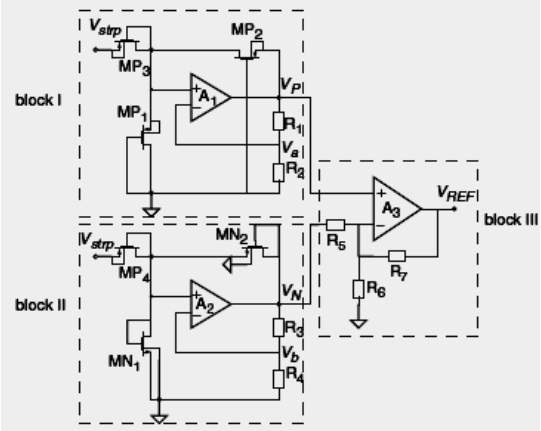


Figure 2.11: Threshold voltage based CMOS voltage reference schematic [8]

In 2007, Luis Toledo et al. [10] presented a voltage reference which was based on threshold voltage difference principle. The principle of the circuit relies on two independent groups of NMOS and PMOS as shown in Figure 2.12. Observe that resistors are not used and its temperature dependence is avoided. If the mobility is cancelled, the only dependency with the temperature comes from the threshold voltage.

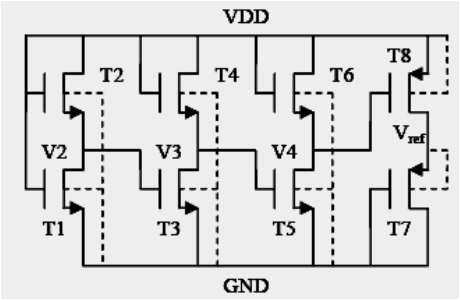


Figure 2.12: Luis Toledo's Voltage Reference [10]

Due to the circuit architecture the mobility factor is completely cancelled. It does not use resistors and all transistors works in strong inversion. The circuit is simple, op-amp less and can be implemented in a standard CMOS process.

2.3 Low Power Reference Circuits

2.3.1 Ultralow-Power Temperature-Insensitive Current Reference Circuit

This current reference circuit, (as shown in Figure 2.13) consists of a constant-current sub-circuit and a bias-voltage sub-circuit. The latter supplies a bias voltage to the former. This is suitable with low temperature dependence for micro-power electronic applications [11]. A source-coupled amplifier is used to ensure the same current flowing in M_A and M_B. To use

the source-coupled amplifier, a cascode configuration of nMOSFETs is adapted in the constant-current sub-circuit.

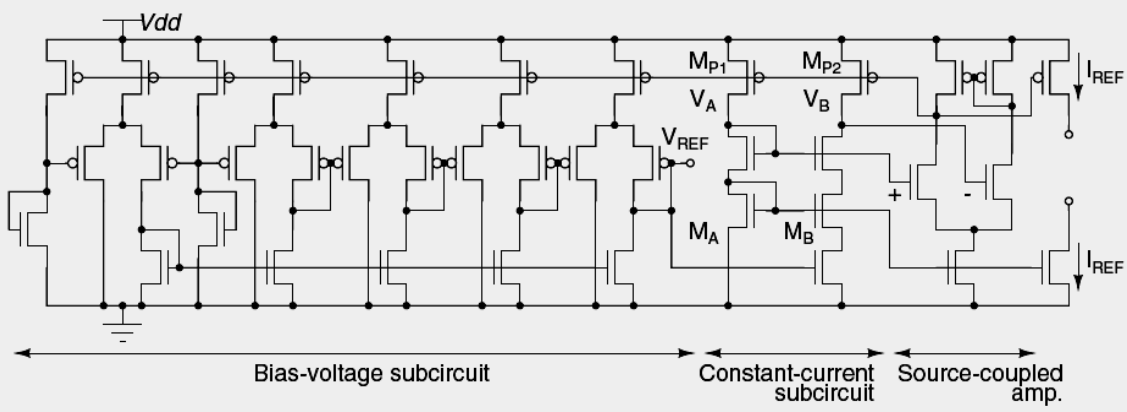


Figure 2.13: Current reference consisting of bias voltage sub-circuit and constant-current sub-circuit [11]

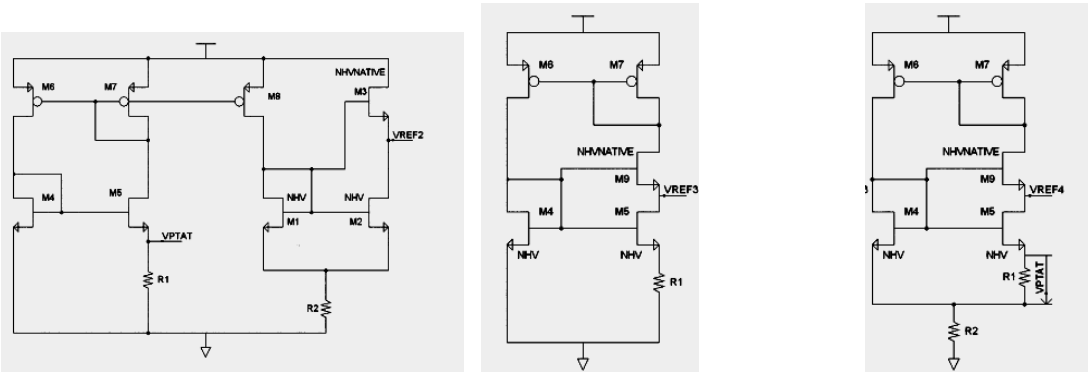
The source-coupled amplifier and the constant-current sub-circuit construct the unity gain configuration. The voltage of V_A is monitored by the non-inverting terminal of the unity gain circuit, and then the output voltage of V_B is set at the same voltage with V_A. This ensures the same current value in transistors M_A and M_B. AC analysis of this unity gain circuit shows that the phase margin at the unity gain frequency is 45 degree, and the circuit is stable.

2.3.2 Low Power Voltage Reference circuits

With the scaling of transistor sizes and reduction in voltage of operation, power consumed by circuits has become a critical parameter in circuit design. The growing trend of ASIC (Application Specific Integrated Circuits) design has given rise to the development of precision and small analog components in metal oxide semiconductor (MOS) technology, Those ASICs would be suitable for power aware applications, such as portable mobile devices, smart intelligent sensors and Life-biomedical devices. Reference circuits are the foremost building blocks in the mixed-signal ultra-low power domain.

In 2009, Srikanth R. et al. [12] proposed three methods (shown in Figure2.14) for generating voltage reference. The first architecture (Figure 2.14(a)) focuses on low voltage high precision reference voltage for the temperature range of –40 to 100°C. The second architecture (Figure 2.14(b)) focuses on low voltage low power reference bringing down

current consumption to focuses on low voltage low power reference bringing down current consumption to half. The third one (Figure2.14(c)) is a hybrid architecture with lesser voltage reference variation and lesser power consumption but has higher operational voltage.



(a) (b) (c)

Figure 2.14: (a) low voltage high precision (b) low voltage low power (c) low voltage low power high precision voltage reference Circuits [12]

In 2010, Haesick Sul et al. [13] proposed a simple method for generating a precise low voltage low power voltage reference, which uses the body effect of MOS transistors. This voltage reference takes advantage of the body effect of MOS transistors, presented in Figure 2.15 which is insensitive to temperature variation. To derive the body effect component, identical bias currents are applied to transistors, M1, M2, M3 and M4, as shown in Figure 2.15. Transistors, M2, M3 and M4 are made to have no body effect by connecting their bodies to the source. Meanwhile, M1 is made to have the body effect by connecting its body to the ground.

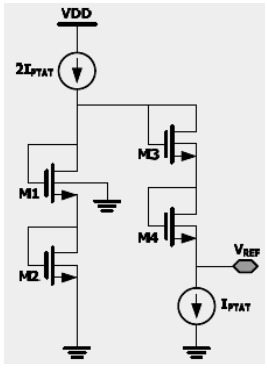


Figure 2.15: Conceptual structure of the voltage reference based on body effect [13]

The structures of two proposed voltage reference circuits are shown in Figure2.15. The circuit in Figure 2.16(a) is a ground-based voltage reference, which is modified from

Figure2.15 for sub-1-V supply operation. Figure 2.16(b) is a VDD-based voltage reference, whose operation is similar to that in Figure 2.16(a) except that the output is referenced to VDD. Each proposed voltage reference is divided into two parts. The first part is a PTAT current generator consisting of M1~M4, p^+ poly resistor. The second part is a reference voltage generator consisting of M5~M12 transistors. [13]

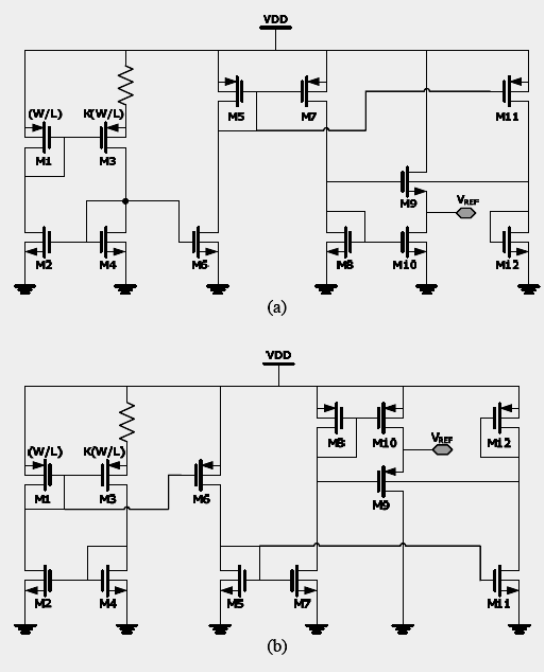


Figure 2.16: The structure of voltage references: (a) ground-based, (b) VDD-based [13]

The output voltage is obtained at the source of M9 which can be acquired by subtracting V_{GS} of M9 from V_{GS} of M8. Here, V_{GS} of M9 is always smaller than that of M8 due to negative body effect.

In 2011, Huimin Zhang et al. [14] presented another Ultra-low Power voltage reference circuit using sub-threshold and body effect techniques with power consumption of only 0.209 μW under a supply voltage of 1.7 V at room temperature that consists of three main sub-circuits (as shown in Figure 2.17).The first is a $PTAT^2$ current sub-circuit composed of transistors working in sub-threshold (M4, M6) and others in saturation. It will generate a current I_2, which is proportional to the square of absolute--temperature. The second is a voltage reference sub-circuit composed of two source-coupled pairs (M11-M15), among which all transistors are operated in the sub-threshold except for M16-M18. It accepts the current I_2 through current mirrors and generates two voltages with a negative temperature

coefficient V_{TH} and a positive temperature coefficient V_T. Then the two voltages are combined to produce a reference voltage V_{REF} with a zero TC. The third is a start-up circuit composed of MS1, MS2 and MS3 that are used to making sure the entire circuit work in stable state.

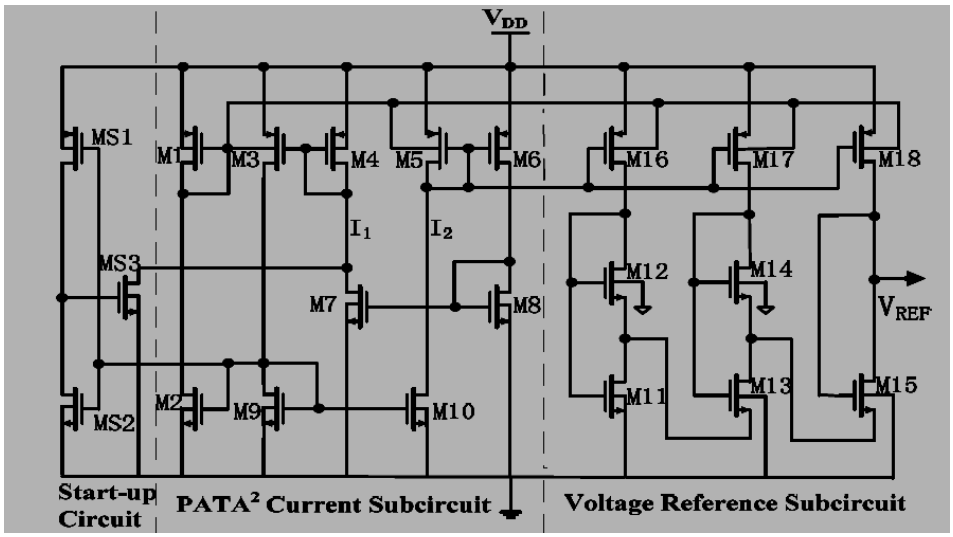


Figure 2.17: Ultra-low Power voltage reference circuit using sub-threshold and body effect techniques [14]

2.4 A High Precision Current and Voltage Reference Generator

A high precision temperature insensitive current and voltage reference generator is presented in [15]. It is specifically developed for temperature compensated oscillator.

As shown in Figure 2.18. It consists of two sub circuits, the startup circuit and reference generator. The startup circuit is provided to ensure that the current reference generated from the circuit will be moved from the undesired bias point where all current are equal to zero and work on the right equilibrium point.

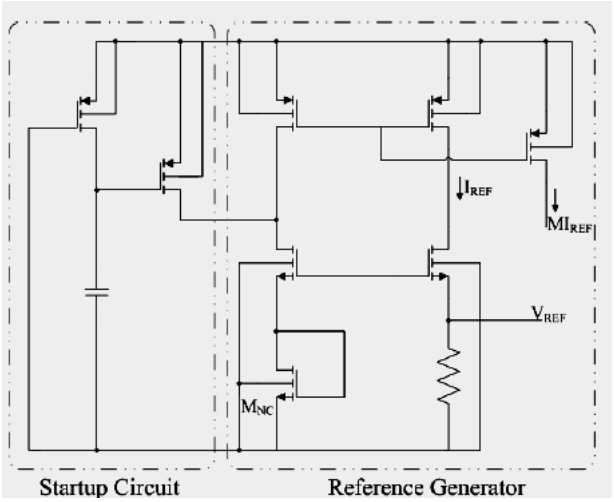


Figure 2.18: Current and voltage reference circuit [15]

The reference generator circuit is a hybrid of a proportional to absolute temperature (PTAT) current reference circuit as shown in Figure 2.19.

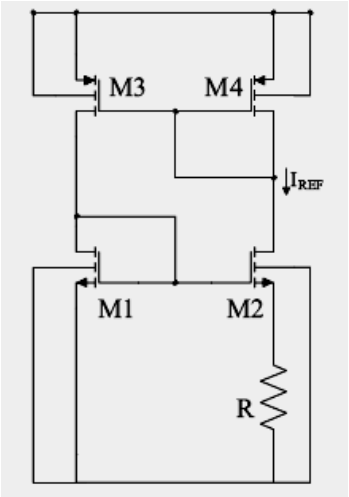


Figure 2.19: PTAT current reference [15]

The PTAT circuit operates by causing the two branch of the circuit to have equal current flowing through them. This is done through the use of mirrored PMOS transistor.

Chapter 3 Design of Combined Reference Circuit

3.1 CMOS Combined Reference Circuit

The Combined Reference Circuit is illustrated in Figure 3.3.The circuit consists of mainly three blocks. The first block is start-up circuit, which is used to set the desired operating point of the circuit. The second block is current generator, which produces a constant current with supply and temperature compensation and the last block is voltage generator, which have an active load for producing Voltage with supply and temperature compensation.

3.1.1 Start-up Circuit

A start-up circuit is used to set the desired operating point of the circuit. Once the desired state is reached, the start-up circuit should not interfere with the circuit. The start-up circuit is shown in Figure

3.1.2 Supply and Temperature Independent CMOS Current Generator

The nonzero supply dependency of the conventional self-biased current reference is compensated as shown in Figure 3.1. Two self-biased current references generate I_1 and I_2, respectively, and the current mirror M6 and M9 multiplies I_2 to get NxI_2. The size of the transistors and the resistance R_S are determined so the two current outputs I_1 and NxI_2 have the same supply dependency and different magnitude. Then, by subtracting NxI_2 from I_1, the supply independent output current I_{SI} can be obtained as shown conceptually at the bottom of Figure 3.1.

Through a simple analysis, the supply compensated output current I_{SI} is

$$I_{out} = \frac{2I_{out}}{\mu_p C_{ox}\left(W/L\right)_p} \cdot \frac{1}{R_S^2}\left\{\left(1-\frac{1}{\sqrt{K_1}}\right)^2 - N\left(1-\frac{1}{\sqrt{K_1}}\right)^2\right\}$$

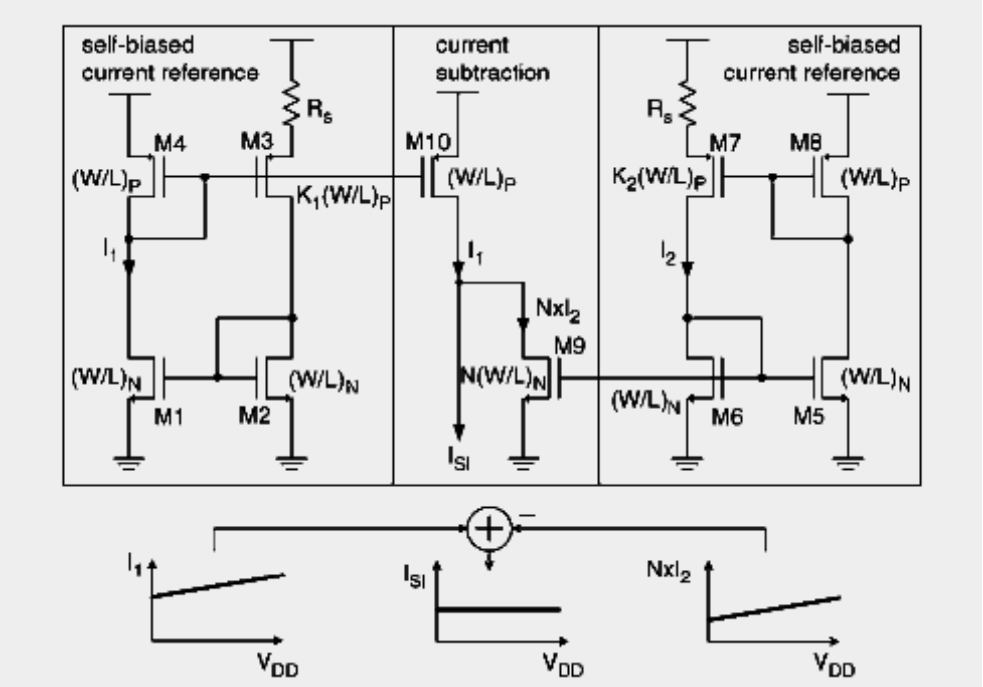


Figure 3.1: Supply independent current generation [16]

The supply independent current I_{SI} has a positive temperature coefficient because of the negative temperature coefficients of μ_p and R_S. The temperature dependency is compensated also by a simple current subtraction as shown in Figure 3.2. The drain current of M_{14}, I_T, is proportional to I_{SI} and therefore its temperature coefficient is also positive. By subtracting I_T from I_{SI}, the temperature compensated output current I_{out} can be obtained. Because I_{SI} and I_T are all supply independent, the output current I_{out} is also supply independent [16].

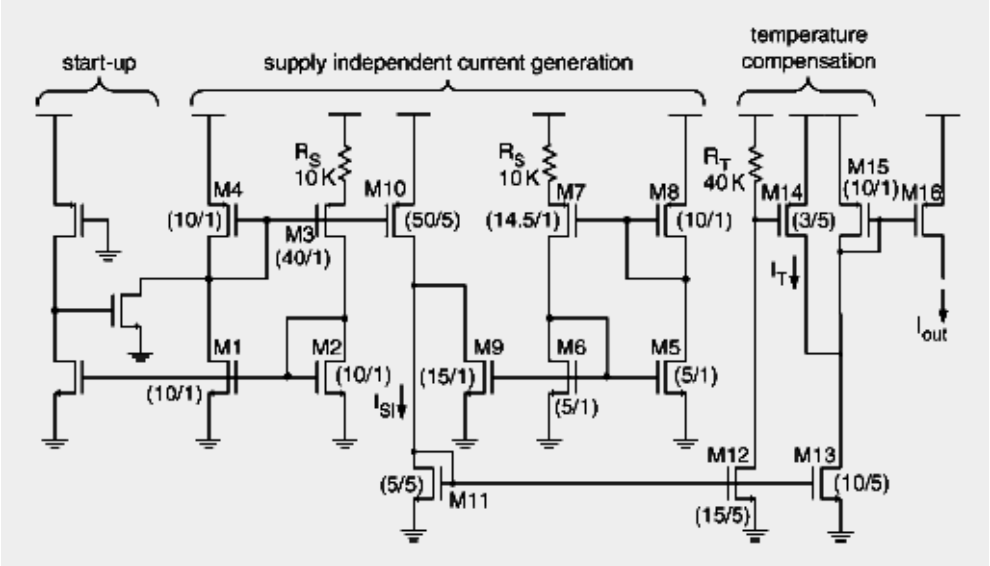


Figure 3.2: Supply and Temperature compensated CMOS current reference [16]

3.1.3 CMOS Voltage Reference with Active Load

The principle of our voltage reference circuit is illustrated in Figure 3.3. The circuit consists of a sub-circuit that generates a bias current I0. I0 is injected into the active load consisting four Transistors to generate the reference voltage, VREF.

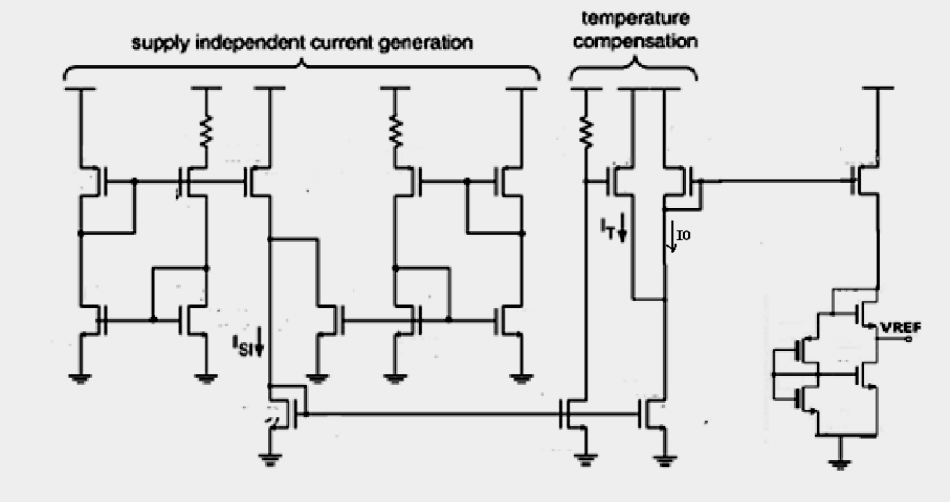


Figure 3.3: Supply and Temperature compensated CMOS Combined Reference Circuit [16]

3.2 Layout of CMOS Combined Reference Circuit

This Section describes the Layout design of CMOS Combined Reference Circuit. The physical layout design has been made in standard UMC 0.18μm CMOS Technology. Cadence Virtuoso layout editor tool is used for the layout design and DRC, LVS and RCX have been performed by using Cadence Assura.

Design Rule Check (DRC) is performed in order to verify that layout fulfills all electrical and geometric rules provided by foundry and finally, LVS (Layout Vs Schematic) is performed on the layout design to provide equivalence between the Layout and Schematic.

The basic design rules are summarized below:

Metal 1 to metal 1 spacing	0.24 μm
Minimum contact size	0.24 μm*0.24 μm
Poly to poly spacing	0.24 μm
Poly to metal spacing	0.28/0.00 μm
Contact overlap to p+ diffusion	0.1 μm
Metal 1 width	0.24 μm
Poly extension beyond active	0.22 μm
Minimum contact spacing	0.26 μm
N well overlap p+ diffusion	0.43 μm
Diffusion contact to poly spacing	0.15 μm
Minimum p+ implant overlap p+ diffusion	0.22 μm
Poly width	0.18 μm
Minimum poly extension on to field region	0.22 μm
Poly contact to diffusion edge spacing	0.18 μm
Minimum poly overlap contact	0.1 μm
Minimum metal area	0.1764 μm*μm
Minimum metal2 width	0.28 μm
Metal1 and metal2 overlap over via	0.08 μm
Minimum equal potential N-well spacing	0 μm or >=0.9 μm
Minimum non equal potential 1.8 V N well spacing	2μm

The Layout of designed circuit is shown in Figure 3.4.

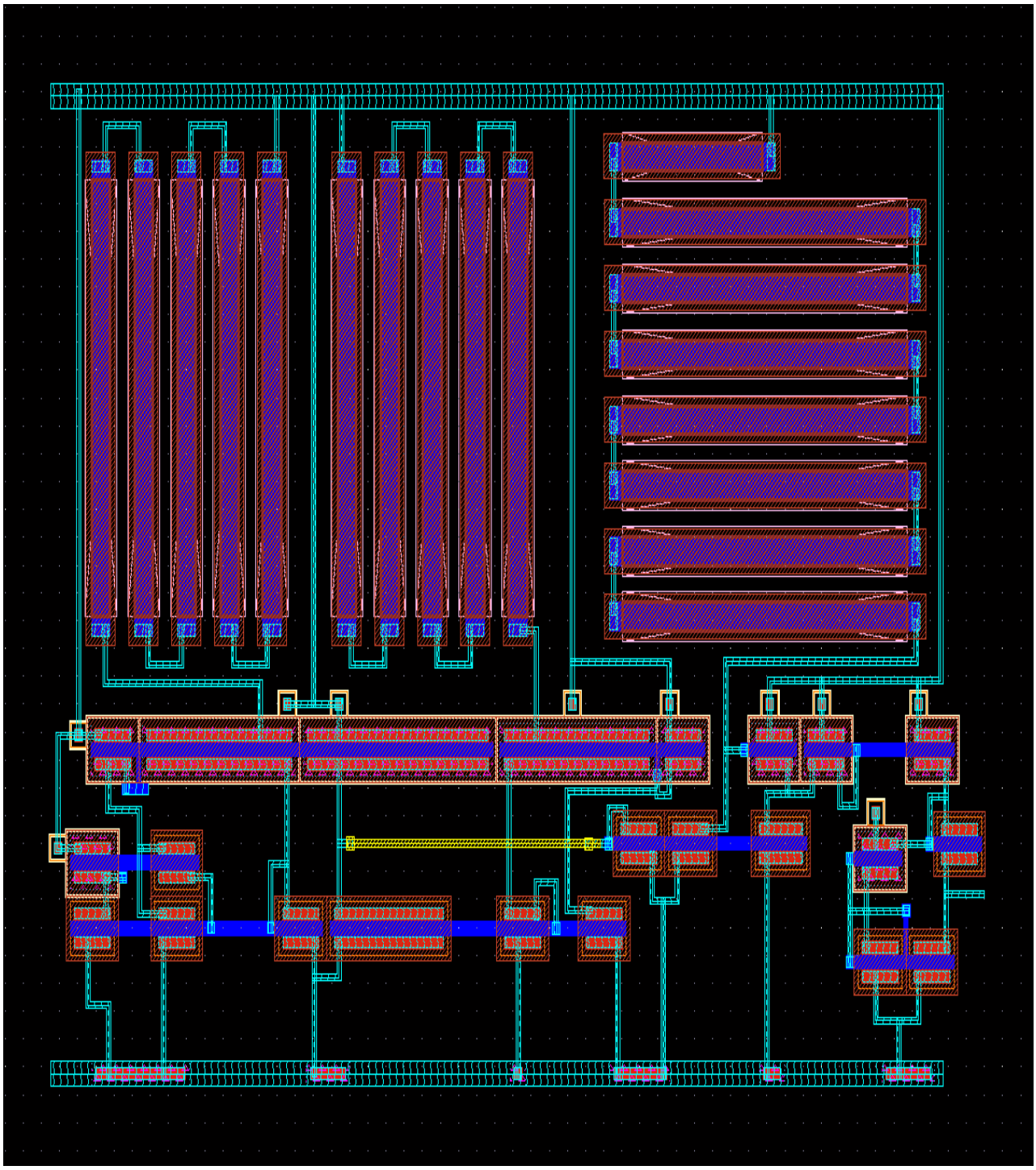


Figure 3.4: Layout of Supply and Temperature compensated CMOS Combined Reference Circuit

The RC extracted view of CMOS Combined Reference Circuit is shown in Figure 3.5.

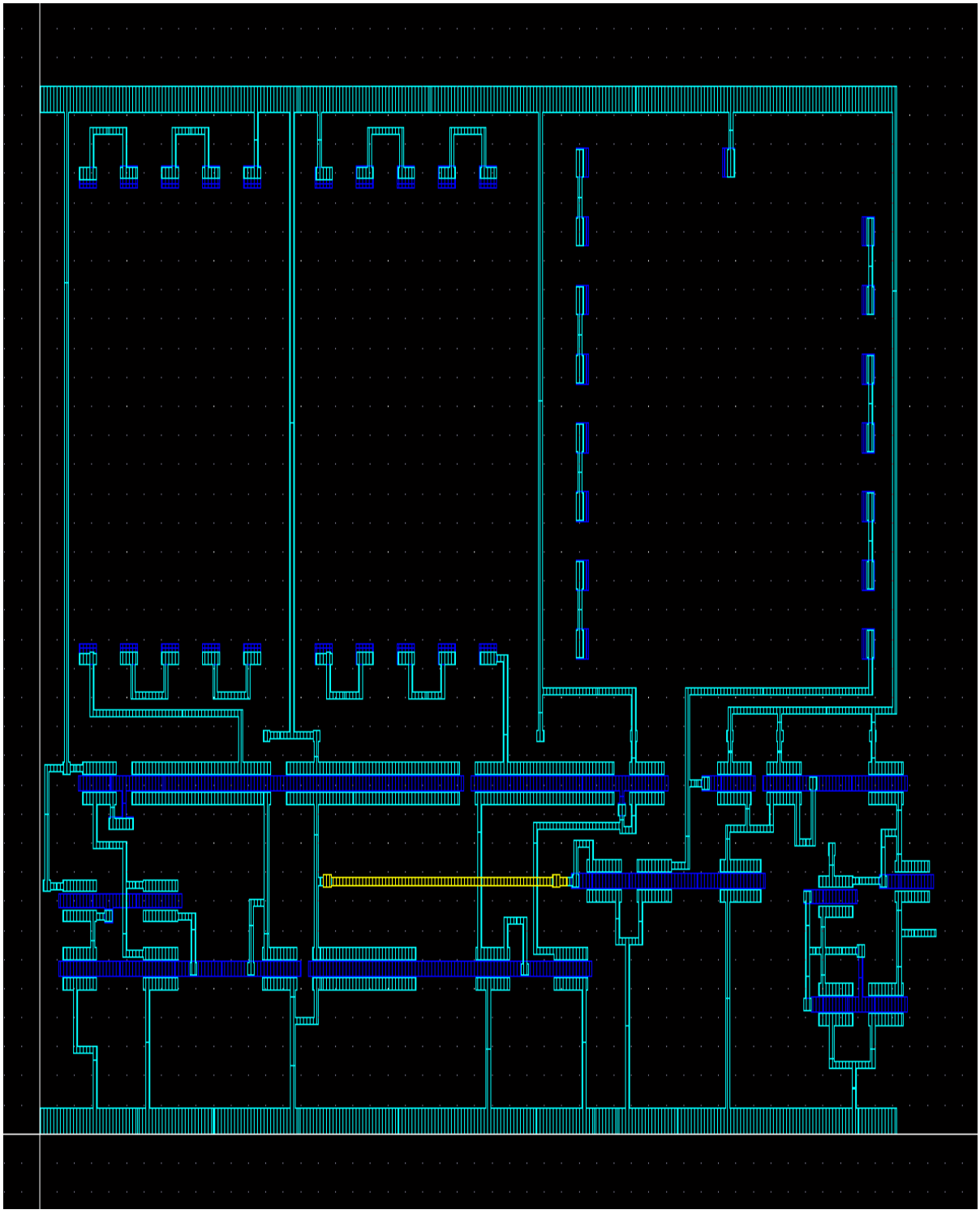


Figure 3.5: RC extracted view of Supply and Temperature compensated CMOS Combined Reference Circuit

The supply and temperature compensated CMOS Combined Reference Circuit has been implemented in a UMC 0.18 µm standard CMOS process.

4.1 Beta Multiplier

It is a basic unit of the designed circuit. The schematic of Beta Multiplier is shown in Figure 4.1 and its simulated waveforms are shown in Figure 4.2 and Figure 4.3 as follows

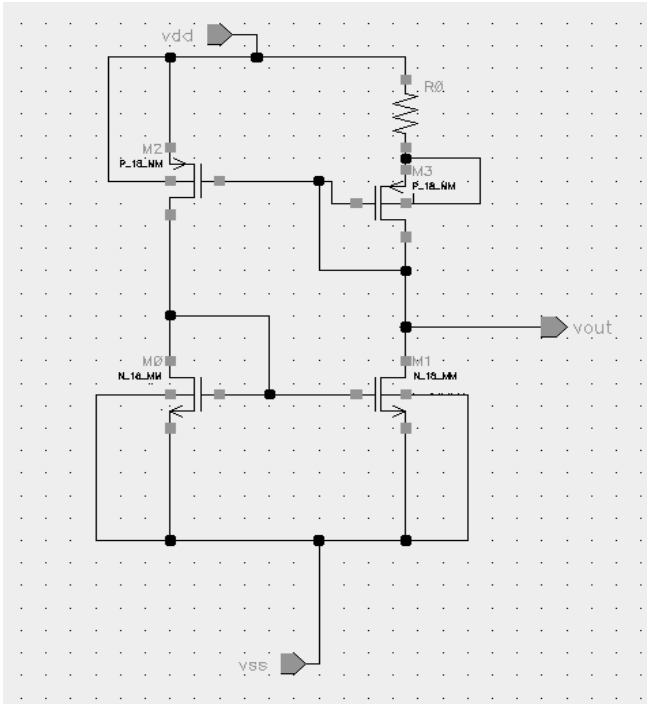


Figure 4.1: Schematic of the Beta Multiplier Reference

Table 4.1: Different parameters in Beta Multiplier

Name of Component	$(W/L)_p$	$(W/L)_n$	Resistance
M0		**2 µ /0.5µ**	
M1		**2 µ /0.5µ**	
M2	**2 µ /0.5µ**		
M3	**8 µ /0.5µ**		
R0			**10KΩ**

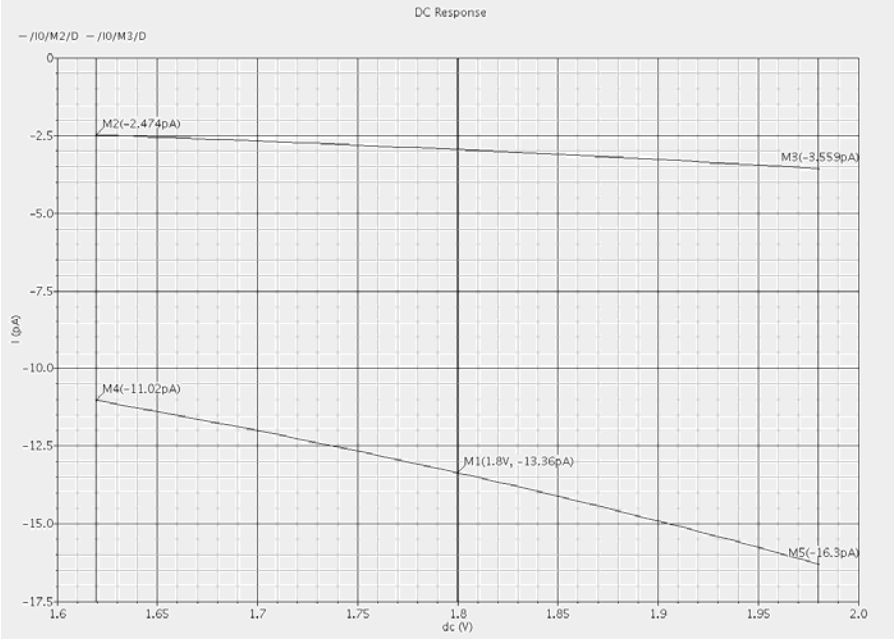


Figure 4.2: Simulated behavior of the Beta Multiplier Reference with Supply Variation

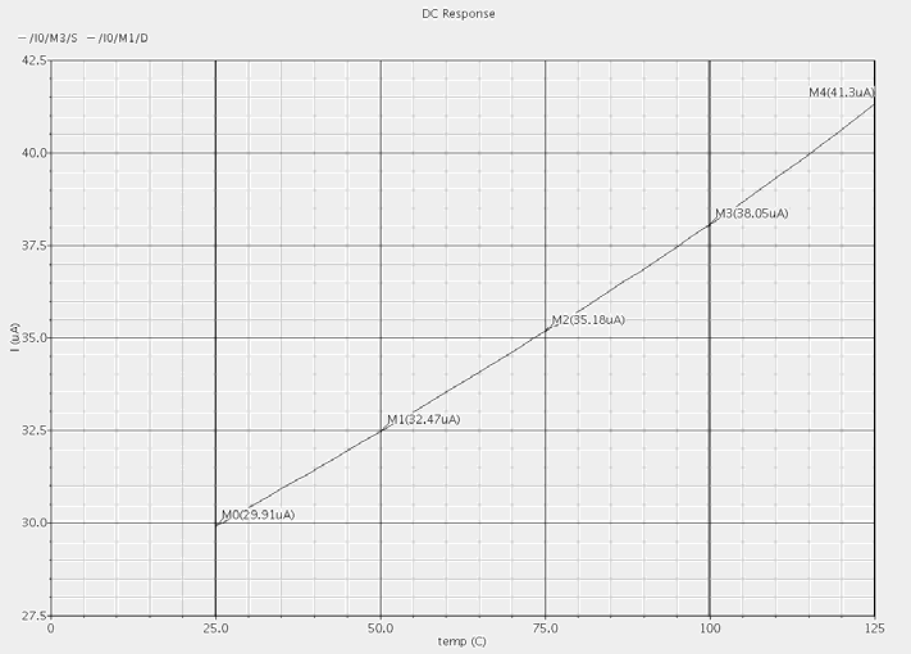


Figure 4.3: Simulated behavior of the Beta Multiplier Reference with Temperature Variation

Figure 4.2 and Figure 4.3 shows the variation of reference current with supply voltage and temperature, respectively. Here the reference current varies from 2.474pA to 3.559pA with ±

10% variation in supply voltage. Whereas the reference current varies from 29.91µA to 41.3 µA with temperature varies from 25°C to 125°C.

4.2 Supply Independent Reference circuit

This is a new approach to get the reference current, which is independent from supply voltage variation. In this approach two Beta-Multiplier circuits and one Subtractor Circuit is used in the required reference current. Figure 4.4 shows the required Schematic for supply independent reference current.

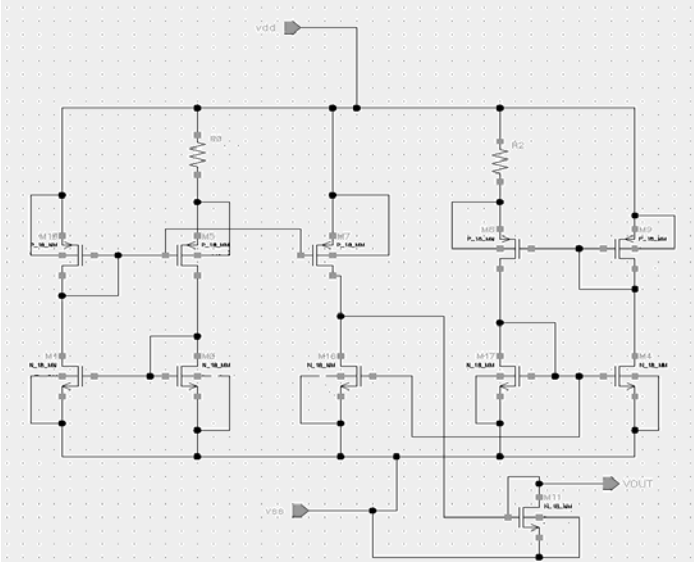


Figure 4.4: Schematic of the Supply Independent Reference

Table 4.2: Different Components of Supply Independent Reference

Name of Component	$(W/L)_p$	$(W/L)_n$	Resistance
M0		**2 µ /0.5µ**	
M1		**2 µ /0.5µ**	
M4		**2 µ /0.5µ**	
M5	**8 µ /0.5µ**		
M7	**8 µ /0.5µ**		
M8	**8 µ /0.5µ**		
M9	**2 µ /0.5µ**		
M10	**2 µ /0.5µ**		
M16		**6 µ /0.5µ**	

M17		**2 µ /0.5µ**	
R0			**10KΩ**
R2			**10KΩ**

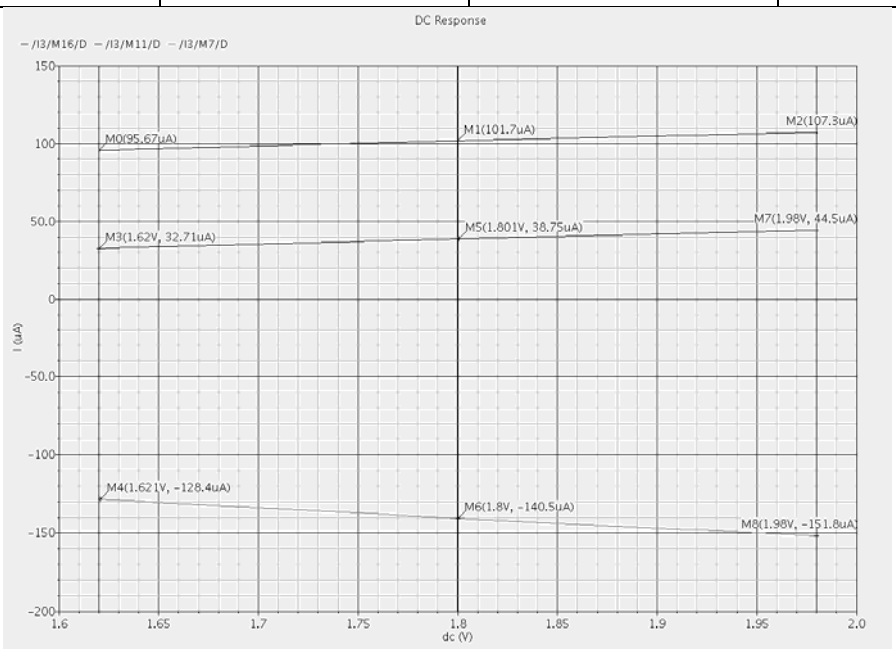


Figure 4.5: Simulated behavior of the Supply Independent Reference with Supply Variation

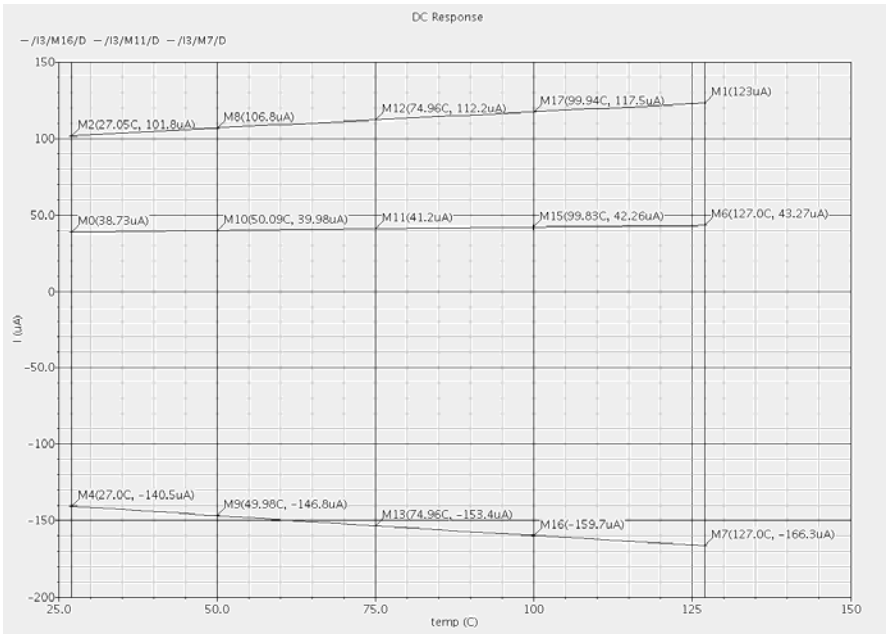


Figure 4.6: Simulated behavior of the Supply Independent Reference with Temperature Variation

Figure 4.5 and Figure 4.6 shows the variation of reference current with supply voltage and temperature, respectively. Here the reference current varies from 32.71µA to 44.5µA with ± 10% variation in supply voltage. Whereas the reference current varies from 38.73µA to 43.27 µA with temperature varies from 25°C to 127°C.In Figure 4.7 the reference current is drawn by varying width of one transistor.

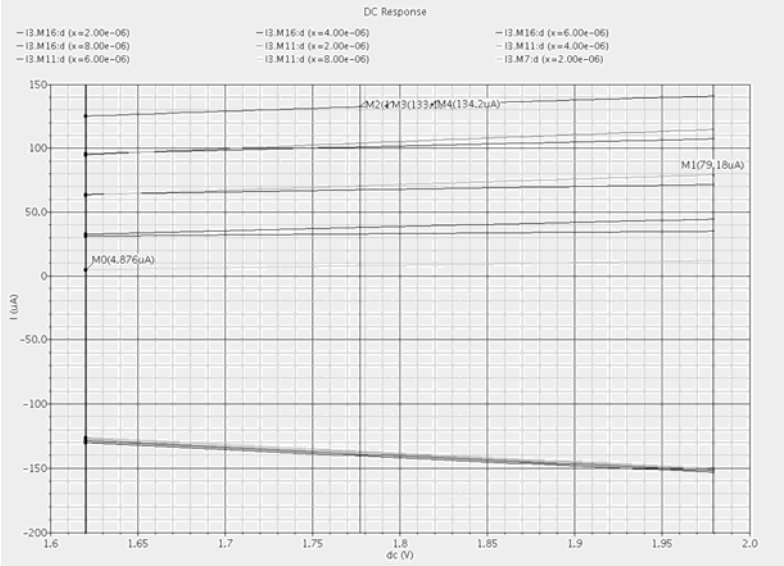


Figure 4.7: Simulated behavior of the Supply Independent Reference with Supply and width Variation

4.3 Supply and Temperature Compensated CMOS Current Reference

The Schematic of Supply and Temperature Compensated CMOS Current Reference is shown in Figure 4.8

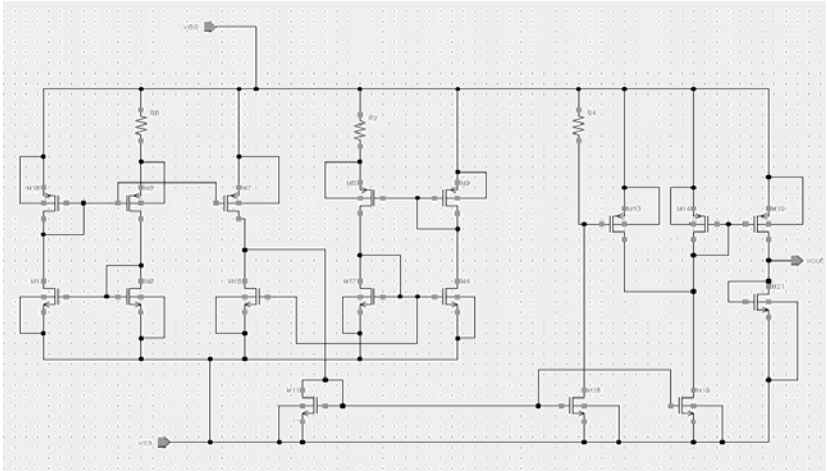


Figure 4.8: Schematic of the Supply and Temperature Compensated CMOS Current Reference

In Figure 4.5 the supply independent reference current is drawn with temperature variation. But this value of reference current is strongly depending on temperature variation. So here the additional circuitry is applied for temperature compensation technique. The Schematic (as shown in Figure 4.8) is the required circuit for Supply and Temperature Compensated CMOS Current Reference.

Table 4.3: Different Component of Supply and Temperature Compensated Current Reference

Name of Component	$(W/L)_p$	$(W/L)_n$	Resistance
M0		5 µ /0.5µ	
M1		5 µ /0.5µ	
M4		2.5 µ /0.5µ	
M5	20 µ /0.5µ		
M7	25 µ /2.5µ		
M8	7.25 µ /0.5µ		
M9	5 µ /0.5µ		
M10	5 µ /0.5µ		
M11		2.5 µ /2.5µ	
M13	2.5 µ /0.5µ		
M14	5 µ /0.5µ		
M15	5 µ /0.5µ		
M17		2.5 µ /0.5µ	
M18		7.5 µ /2.5µ	
M19		5 µ /2.5µ	
M21	2.5 µ /2.5µ		
R0			10KΩ
R2			10KΩ
R4			40KΩ

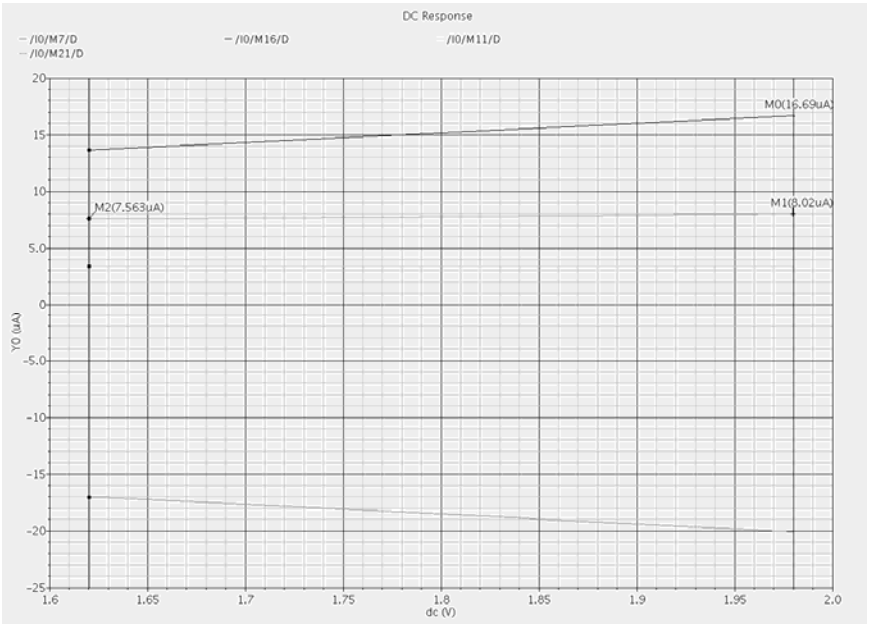


Figure 4.9: Simulated behavior of the Current Reference with Supply Variation

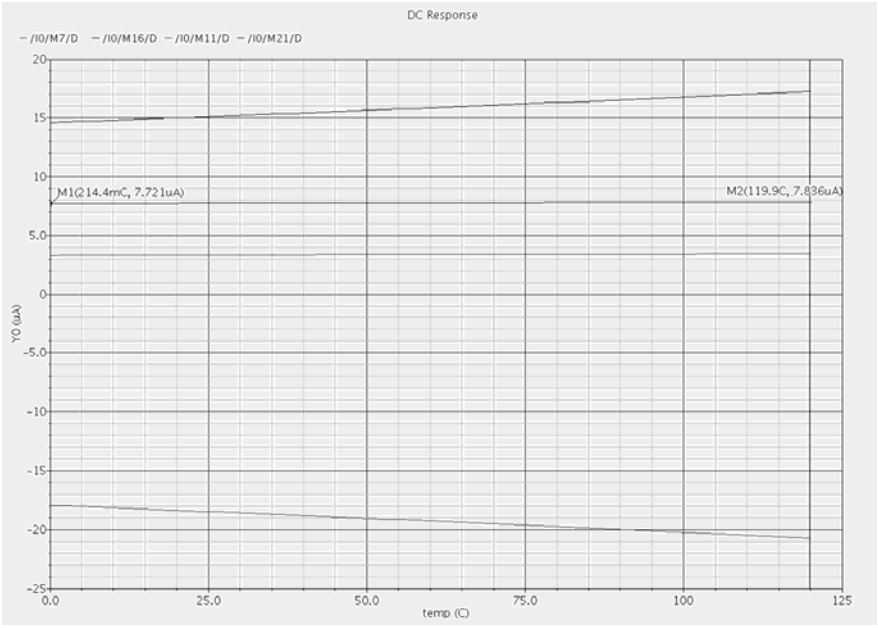


Figure 4.10: Simulated behavior of the Current Reference with Temperature Variation

Now here we get required waveforms. Figure 4.9 and Figure 4.10 shows the variation of reference current with supply voltage and temperature, respectively. Here the reference current varies from 7.536µA to 8.02µA with ± 10% variation in supply voltage. Whereas the

reference current varies from 7.721µA to 7.836 µA with temperature varies from 0°C to 120°C.

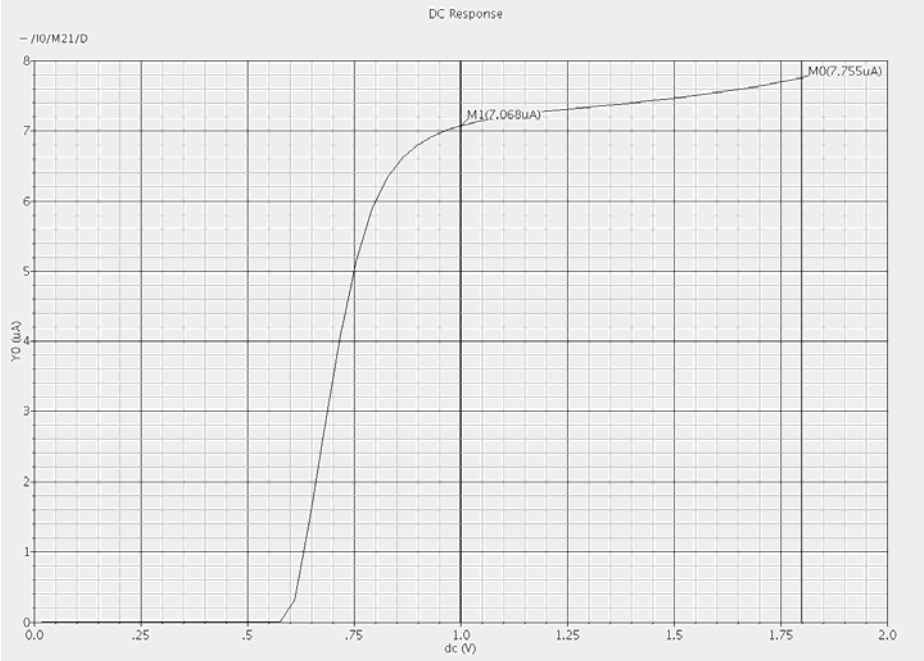


Figure 4.11: Simulated output current against supply voltage

Figure 4.11 shows the simulated output current with respect to supply variation. Here the value of output current is 7.068µA at 1 V and 7.755µA at 1.8 V.

4.4 Supply and Temperature compensated CMOS Combined Reference Circuit

The Schematic (as shown in Figure 4.12) is the required circuit for Supply and Temperature Compensated CMOS Combined Reference Circuit. It consists of a start-up circuit, a current generator and a voltage generator.

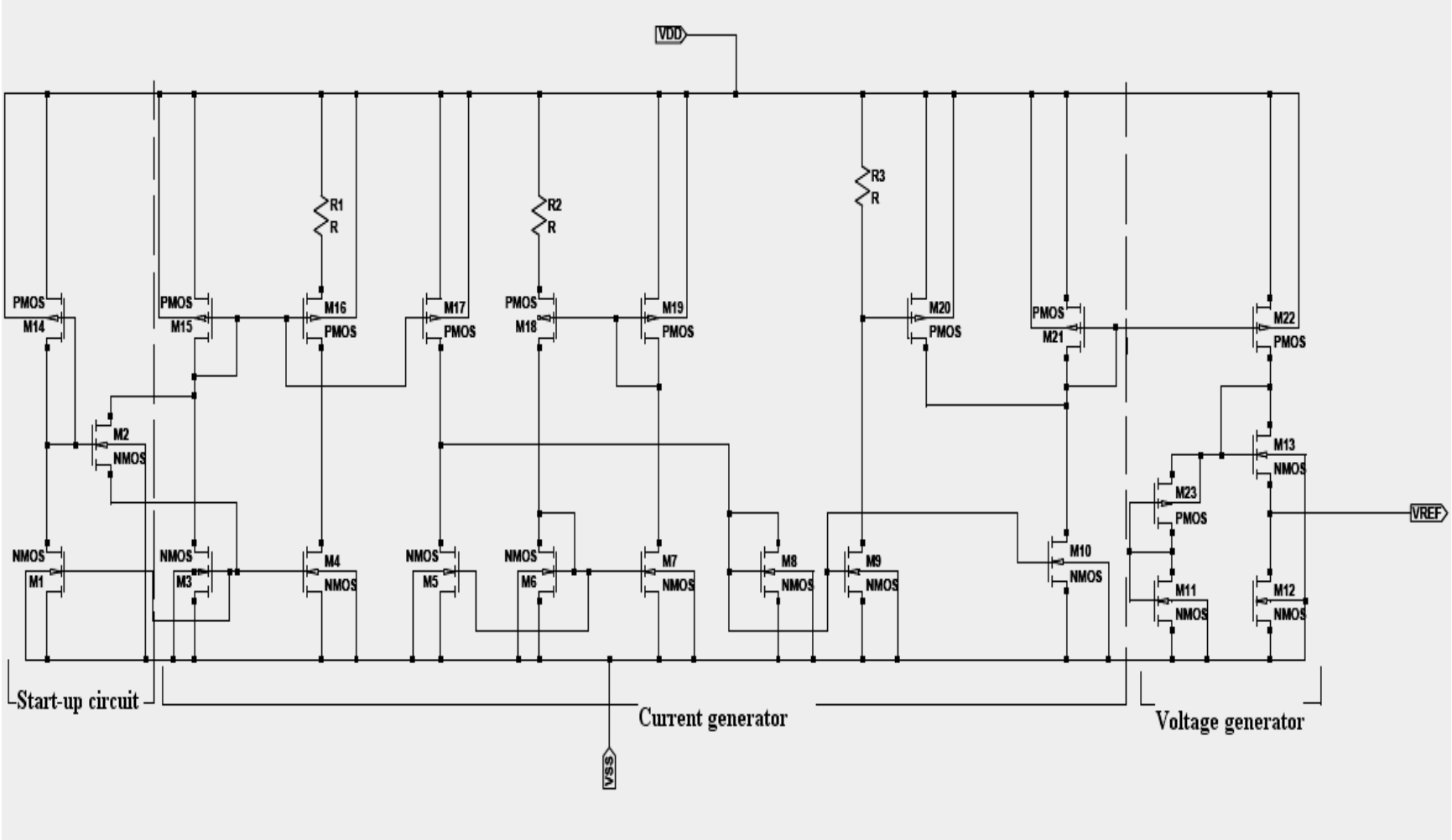


Figure 4.12: Schematic of CMOS Combined Reference Circuit

Table 4.4: Different Component of Supply and Temperature CMOS Combined Reference Circuit

Name of Component	$(W/L)_p$	$(W/L)_n$	Resistance
M0	2 µ /0.5µ		
M1		2 µ /0.5µ	
M2		2 µ /0.5µ	
M3	2 µ /0.5µ		
M4	8 µ /0.5µ		
M5		2 µ /0.5µ	
M6		2 µ /0.5µ	
M7	10 µ /.5µ		
M8		6 µ /0.5µ	
M9	8 µ /0.5µ		
M10	2 µ /0.5µ		
M11		2 µ /0.5µ	
M13		2 µ /0.5µ	
M14		2 µ /0.5µ	
M15		2 µ /0.5µ	
M17	2 µ /0.5µ		
M18	2 µ /0.5µ		
M19	2 µ /0.5µ		
M21		2.4 µ /0.5µ	
M22		2 µ /0.5µ	
M23	2 µ /0.5µ		
M24		2 µ /0.5µ	
M25		2 µ /0.5µ	
R0			10KΩ
R2			10KΩ
R4			15KΩ

4.4.1 Pre Layout Simulation of CMOS Combined Reference Circuit

The CMOS Combined Reference Circuit achieves a nominal value of 50 µA and 777 mV for current and voltage respectively, from a 1.8 V supply voltage. The line sensitivity of 285 ppm/V and 348 ppm/V for current and voltage is achieved respectively, under the ±10 % variation in supply voltage. The temperature coefficient for current and voltage of 98 ppm/° C and 293 ppm/° C respectively is achieved, with temperature ranges from −40 ° C to 125 ° C.

Figure 4.13 and Figure 4.14 shows the variation of Combined Reference with supply voltage and temperature, respectively. Here the reference current varies from 47.23µA to 52.48µA and reference voltage varies from 723.3 mV to 820.8 mV with ± 10% variation in supply voltage. Whereas the reference current varies from 49.58µA to 50.41 µA and reference voltage varies from 753.1 mV to 790.7 mV with temperature varies from –40°C to 125°C.

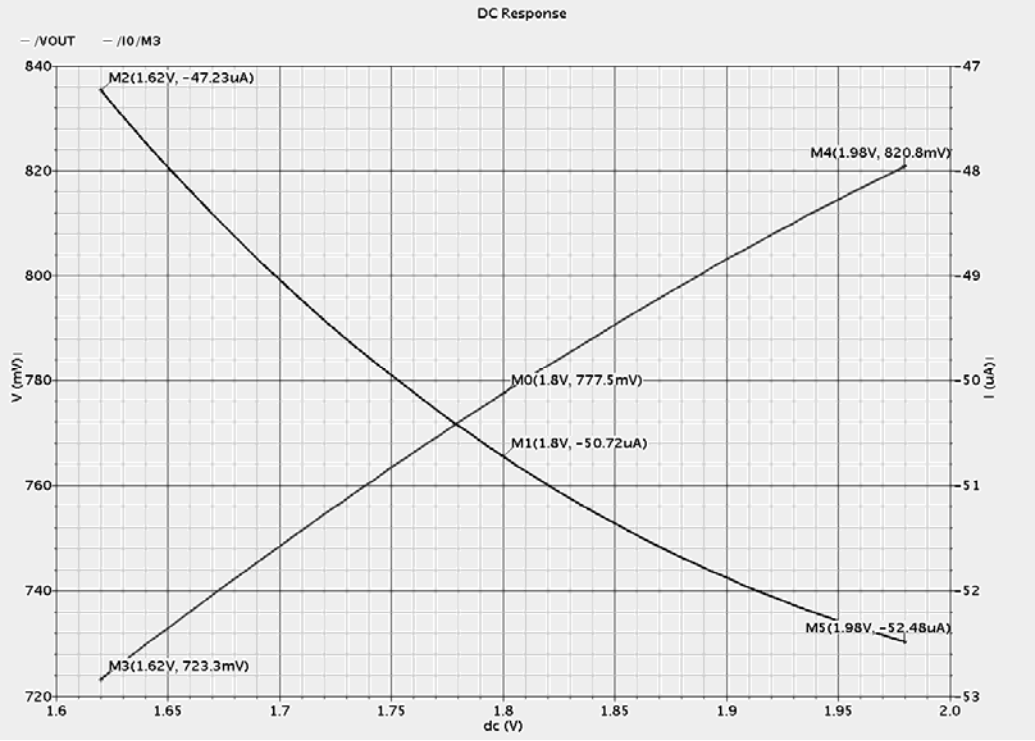


Figure 4.13: Pre-Simulated behavior of the CMOS Combined Reference with Supply Variation

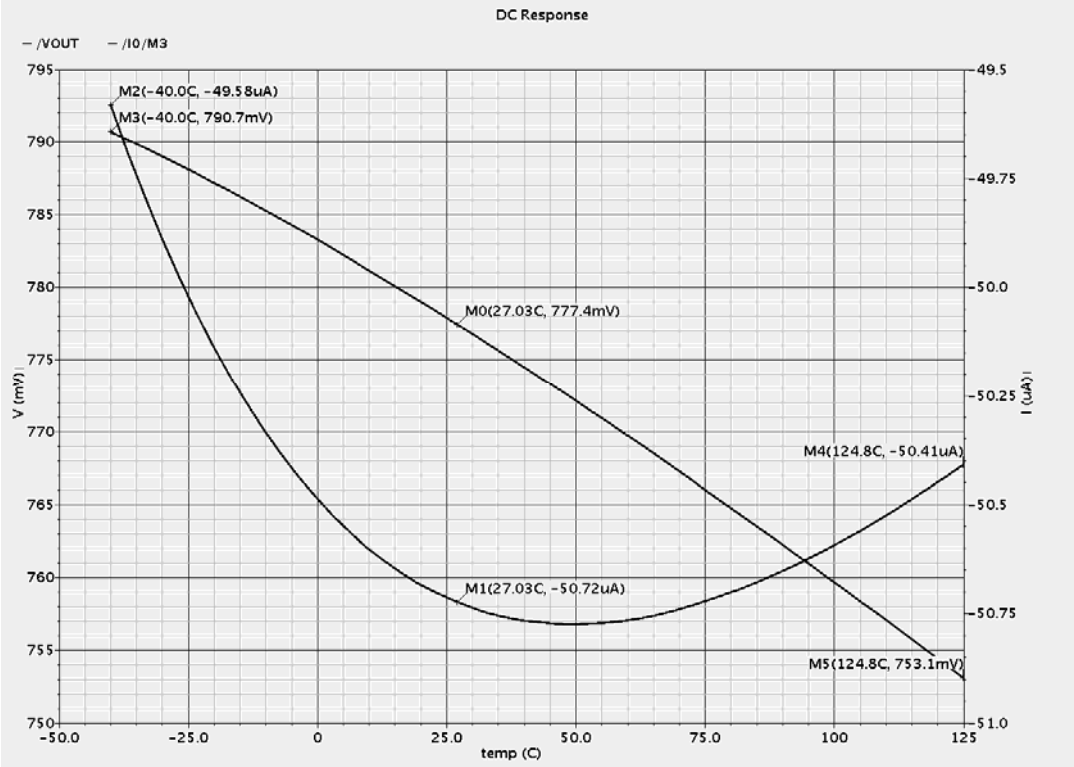


Figure 4.14: Pre-Simulated behavior of the CMOS Combined Reference with Temperature Variation

4.4.2 Post Layout Simulation of CMOS Combined Reference Circuit

Figure 4.15 and Figure 4.16 shows the variation of Combined Reference with supply voltage and temperature, respectively. Here the reference current varies from 46.68µA to 51.83µA and reference voltage varies from 722.6 mV to 819.5 mV with ± 10% variation in supply voltage. Whereas the reference current varies from 48.99µA to 49.76 µA and reference voltage varies from 752 mV to 789.8 mV with temperature varies from –40°C to 125°C.

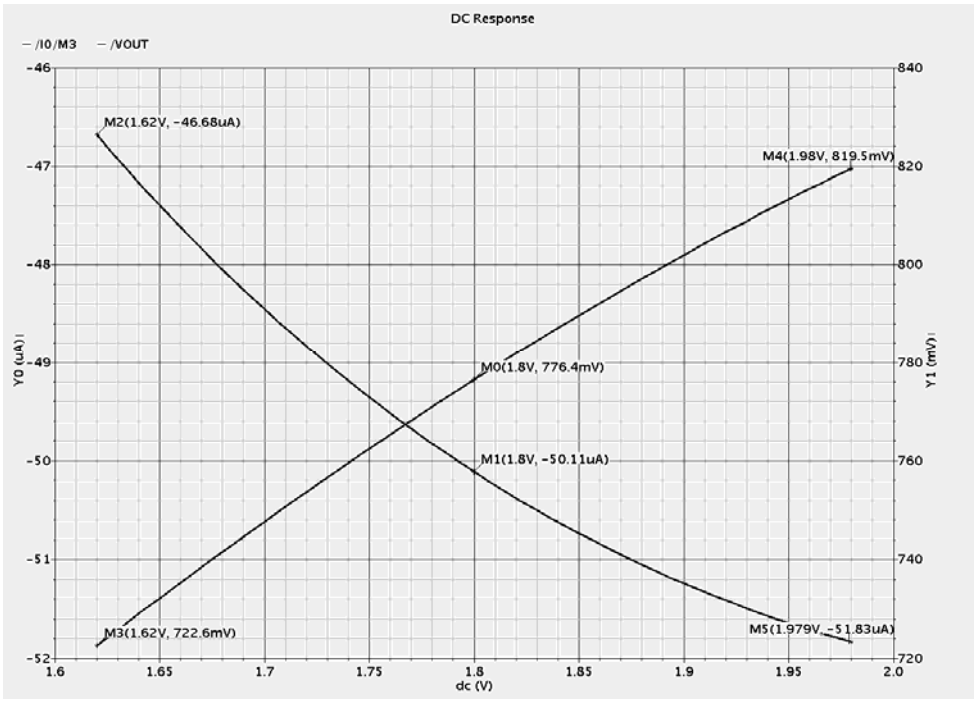


Figure 4.15: Post-Simulated behavior of the CMOS Combined Reference with Supply Variation

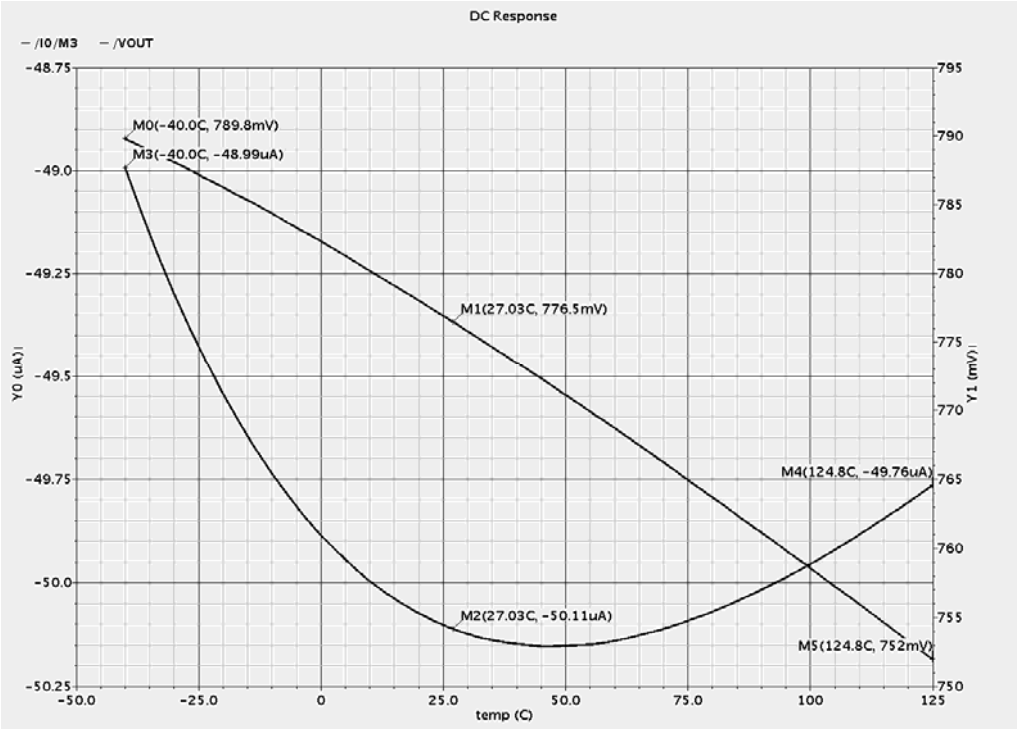


Figure 4.16: Post-Simulated behavior of the CMOS Combined Reference with Temperature Variation

4.4.3 Simulation Results at Different Process Corners

A process corner is an example of a design-of-experiments technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer.

Process corners represent the extremes of these parameter variations within which a circuit that has been etched onto the wafer must function correctly. If the circuit does not function at all or any of these process extremes, then the design is considered to have inadequate design margin. Therefore, the designer has to take into account these process corners while designing a circuit. If the circuit works well at all the process corners, then it will be sent to the foundry for the fabrication. Since the purpose of corners is to accept the extreme of extreme results, so one can define lowest supply voltage with highest temperature for slow-slow simulation and highest supply voltage with lowest temperature for fast-fast simulation.

The Table 4.5 shows the different corners with particular temperature and supply value for the simulation of a CMOS Combined Reference Circuit. There is ±10% variation in supply voltage is taken into account i.e. 1.98V is used for FF corner and 1.62V is used for SS corner.

Table 4.5: Corners Simulation Table

Corners	Supply Voltage	Temperature
TT	1.8V	27 °C
FF	1.98V	–40 °C
FS	1.8V	27 °C
SF	1.8V	27 °C
SS	1.62V	125 °C

The Table 4.6 shows the Pre-Simulation results at different process corners. While Table 4.7 shows the Post-Simulation results at different process corners.

Table 4.6: Pre- Simulation results at different process corners

Parameters	TT	FF	FS	SS	SF
Voltage (mV)	777.4	769	798.9	773	754.3
Current (µA)	50.72	47.93	52.63	52.86	48.68
Temperature Dependency					
For Current Reference	98	128	22	428	183
For Voltage Reference (ppm/°C)	293	360	278	235	307
Supply Dependency					
For Current Reference	285	46	264	414	316
For Voltage Reference (ppm/V)	348	237	352	397	344

Table 4.7: Post-Simulation results at different process corners

Parameters	TT	FF	FS	SS	SF
Voltage (mV)	776.4	751.4	797.8	793.5	753.4
Current (µA)	50.11	47.34	52	52.19	48.07
Temperature Dependency					
For Current Reference	93	141	16	267	178
For Voltage Reference (ppm/°C)	295	361	280	251	310
Supply Dependency					
For Current Reference	285	71	261	411	316
For Voltage Reference (ppm/V)	347	228	350	395	343

Chapter 5 Conclusion and Future Scope

5.1 Conclusion

The Proposed CMOS Combined Reference Circuit has been designed in standard 180 nm CMOS process that exhibits excellent supply and temperature independency. The design of CMOS Current Generator is by simply subtracting two current outputs with the same dependencies on the supply voltage and temperature. While for Voltage Generator we used the Active load, which gives the fix value of voltage with variations in supply voltage and temperature. Achieved results show that developed Architecture of combined reference can be easily used for oscillators and many other mixed signal integrated circuits.

This circuit achieves a nominal value of 50 μA and 777 mV for current and voltage respectively, from a 1.8 V supply voltage. The line sensitivity of 285 ppm/V and 348 ppm/V for current and voltage is achieved respectively, under the ±10 % variation in supply voltage. The temperature coefficient for current and voltage are 98 ppm/° C and 293 ppm/° C respectively in temperature ranges −40 ° C to 125 ° C.

The Proposed Architecture has been compared with the existing ones as shown in Table 5.1 and here a lot of improvement can be seen in Temperature and Supply dependency for a very wide Temperature range.

5.2 Future Scope

Still a lot of work has to be carried out in the upcoming years by improving the compensation of Supply and Temperature of CMOS Combined Reference Circuit and many other Process Parameters. Also, Reference Circuit is the most versatile Analog building block of many Analog applications, so it's various active blocks such as start-up circuit, Current Generator and Voltage Generator can be further improved, so that the overall performance of CMOS Combined Reference Circuit will be improved.

Table 5.1: Summary of Reference Circuits

References / Parameters	[13] (VDD-based)	[13] (Ground-based)	[14]	[7]	[8]	[10]	[11]	[15]	[6]	[16]	This Work
Year	2010	2010	2011	2009	2004	2007	2005	2009	2004	2007	2013
Technology(µm)	0.13	0.13	0.50	0.13	0.50	1.5	0.25	0.5	0.13	0.25	0.18
Temperature Range(°C)	–20~80	–20~80	–20~85	20~120	–10~80	–20~80	–20~100	0~70	0~80	0~120	–40~125
Supply Voltage(V)	0.7	0.7	1.7	1.0	5.0	2.1		2.6~5.0	1.2	1.1	1.8
V_{REF}(mV)	620.5	87.9	1271	490.0	2660	1184	727	1210	393	–	777.4
I_{REF}(nA)	–	–	–	–	–	–	97.7	6380	–	10.45	50.2
Temperature Coefficient Current Reference Voltage Reference (ppm/°C)	5.39	3.4	5.54		32.0	100.0	–	–	–	720	98 293
Supply Dependency Current Reference Voltage Reference (ppm/V)	–	–	–	–	–	–	–	–	–	1700	285 348

Paper Published / Presented

- A Paper entitled as "A Combined CMOS Reference Circuit with Supply and Temperature Compensation" is published in VDAT 2013 as a regular paper.

- Participated in the Present Around The World (PTAW) Competition-2013 conducted by IET (The Institution of Engineering and Technology) in Delhi and also Presented a Seminar on "A Supply and Temperature Compensated Combined Reference Circuit".

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