LOW POWER MEMORY CELL DESIGN

A THESIS

SUBMITTED IN FULFILLMENT OF THE REQUIREMENT

FOR THE AWARD OF DEGREE OF

DOCTOR OF PHILOSOPHY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

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2013

CERTIFICATE

I, **Shyam Akashe** hereby declare that the thesis entitled, **"LOW POWER MEMORY CELL DESIGN"** submitted to Thapar University, Patiala, in partial fulfillment of the requirement for the award of the Degree of **Doctor of Philosophy in the Electronics and Communication Engineering** is a record of original and independent research work carried out by me during 2008-2013 under the supervision and guidance of **Dr. Sanjay Sharma**, Professor, Department of Electronics and Communication Engineering, Thapar University, and it has not formed the basis for the award of any Degree/Diploma/Associateship /Fellowship or other similar title to any candidate of any university.

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ABSTRACT

Static Random Access Memory (SRAM) has been widely utilized as the representative memory for very large scale integrated (VLSI) circuits. This is because SRAM belongs to faster technology in comparison with the previously reported technologies. However, the power consumption in SRAM is relatively high. Therefore, it is important to reduce the power consumption in SRAM cell as it plays a significant role in the memory design.

The main objective of this thesis is to provide new and efficient ways to design a low power SRAM cell. This work proposes the new techniques for SRAM cell design based on seven transistors (7T) and introduces various circuit topologies and techniques to calculate leakage current, delay and power.

The area and cell stability of SRAM are taken care of while optimizing the power reduction. During the research, the Half-selected cell stability of 7T SRAM cell was found to be in between 5T and 6T SRAM cells using the Wordline Voltage Control Technique. The use of an additional transistor in 7T SRAM cell structure allows read operation without disturbance as compared to the previously proposed SRAM cells. The 7T SRAM cell has very low power consumption with high Static Noise Margin (SNM) and enhanced read/write stability under large variations. With the process variation methods the gate leakage current of 1.154pA and sub-threshold current of 13.139 pA are obtained whereas read and write SNM of 520mV and 545mV are respectively achieved.

In this research work, three techniques are proposed for reducing the gate leakage currents and sub-threshold leakage currents in 7T SRAM cell. In all the methodologies, a dynamic Self Controllable Voltage Level Switch (SVL) is used to reduce the effective voltage across the SRAM cell in stand-by mode. The first method uses the Lower Self Controllable

Voltage Level (LSVL) technique to reduce the supply voltage and achieves a gate leakage current of 467.05 fA and total sub-threshold current of 33.08 pA in 7T SRAM cell which is much less as compared to the total sub-threshold current of 33.6 nA in 6T SRAM cell. The second method uses an Upper Self Controllable Voltage Level (USVL) technique without changing bit-line voltage. With this technique, the gate leakage current significantly reduces to 437.52 fA in 7T SRAM cell from 25.51 nA in 6T SRAM cell. The technique also reduces the effective supply voltage across the 7T SRAM cell from 7V to 0.582V. The third method combines both the USVL and LSVL techniques and is found to be very effective in reducing all significant components of leakage currents. In this approach, the access transistors are put in off state during stand-by mode. Further, reductions in gate leakage current and total sub-threshold current are obtained. The total sub-threshold current reduces to 11.92pA and the gate leakage current shows a decline of 437.791fA from 5.49nA in 6T SRAM cell.

Finally, 8 kb SRAM memory is designed using 4 X 4 array with single ended 7T cell to show the feasibility of the proposed SRAM cell. A 16-Bit SRAM operating at 1V supply voltage is demonstrated in 45nm CMOS process. It is observed that the total power consumption is reduced by more than 90% in comparison to the conventional design. This 7T cell has lower leakage current due to single-bit line and transmission gate at feedback. As a result, it is suitable for low power consumption application.

The circuit simulations have been done using Cadence Virtuoso tool and specture in 45 nm technology. Post-layout simulations have been verified by running Layout Versus Schematic (LVS) design rule check. An analysis of average dynamic power dissipation with respect to the frequency and the load capacitance is made for showing the amount of power dissipated by the SRAM memory cell.

ACKNOWLEDGEMENT

First and foremost, I am indebted to the **ALMIGTHY**. I bow before Him for His blessings and bestowing upon me the will power and confidence to carry out this research work.

I extend my thanks to our Hon'ble Director, **Dr. K.K. Raina** and **Dr. P.K. Bajpai**, distinguished Professor & Dean (Research) for giving me the opportunity to carry out this Ph.D.

I would like to place my heartfelt thanks and sincere gratitude to my research guide **Dr. Sanjay Sharma,** Professor, Electronics and Communication Engineering, Thapar University, Patiala. I feel it a pleasure to be grateful to him for his valuable support, guidance advice and encouragement.

I owe my gratitude and profound thanks to all the doctoral committee members **Dr. Rajesh Khanna,** Professor and Head of Department, Electronics and Communication Engineering, **Dr. A. K. Chatterjee**, Professor, Electronics and Communication Engineering and **Dr. Kulbir Singh**, Associate Professor, Department of Electronics and Communication Engineering, Thapar University, Patiala, Punjab.

I would like to greatly acknowledge, with a deep sense of gratitude the continuous motivation, moral & technical support of all the faculty members and office assistants in the Department of Electronics and Communication, during the research work. My special thanks go to **Dr. Rajesh Khanna**, Professor and Head of Department,

Electronics and Communication Engineering, Thapar University, Patiala for his valuable suggestions for the journal work.

I would like to extend my special thanks to all my colleagues of Department of Electronics and Instrumentation Engineering, Institute of Technology and Management, Gwalior, Madhya Pradesh, India, for their valuable suggestions, support and encouragement.

I also thank the Management of Institute of Technology and Management, Gwalior, Madhya Pradesh, India, for sponsoring me to pursue Ph.D at Thapar University, Patiala.

I am privileged to express my profound gratitude, deep love and affection to my dear wife, **Ms. Esha Akashe** and my son **Soham Akashe**, who have always been with me in all the difficulties that came during the course of this research. Their love, patience, persistent encouragement, good understanding and prayers enabled me to complete this research work successfully. Finally, I am highly obliged to my parents, sister, brother and all the family members for their love, affection, sacrifices, endurance and prayers all through my life.

Shyam Akashe

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ACRONYMS AND ABBREVIATIONS

4T	4 Transistors
5T	5 Transistors
6T	6 Transistors
7T	7 Transistors
8T	8 Transistors
LSI	Large Scale Integration
VLSI	Very Large Scale Integration
RAM	Random Access Memory
SRAM	Static Random Access Memory
EEPROM	Electrically Erasable Programmable Read only Memory
FRAM	Ferroelectric RAM
PMOS	Positive Metal Oxide Semiconductor
NMOS	Negative Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
V_t	Threshold Voltage
Nm	Nanometer
V_{os}	Offset Voltage
SP	Single Port
DP	Dual Port
SPRAM	Spin Transfer Torque RAM
MB	Mega Byte
CRSRAM	Charge Recycling Static Random Access Memory
ADWLUD	Adaptive Dynamic Word Line Under Drive

DAFC	Data Aware Feedback Cutoff
DRD	Dynamic Read Decoupled
WL	Word Line
DNM	Dynamic Noise Margin
HCA	Hierarchical Cell Architecture
CMOS	Complementary Metal Oxide Semiconductor
V_{min}	Minimum voltage
SOI	Silicon on Insulator
DVFS	Dynamic and Voltage Scaling
LV-TTL	Low Voltage Transistor-Transistor Logic
RSNM	Read Static Noise Margin
MBLC	Marginal Bit line Leakage compensation
DVC	Dynamic Voltage Collapse
PD	Partial Depleted
BATT	BIST-Assisted Timing Tracking
BIST	Built-in Self Testing
IOT	IO Transistors
ECC	Error Correcting Codes
FBB	Forward Body Bias
SRBL	Single Read Bit Line
SOC	System on Chip
DRAM	Dynamic Random Access Memory
TSRAM	Tunneling Static Random Access Memory
QOB	Quality of Bit
RD	Reversible Decoder

IC	Integrated Chip
L_g	Gate Length
T_{ox}	Oxide Thickness
W	Width
BL	Bit Line
BLB	Bit Line Bar
WS	Word select Signal
CR	Cell Ratio
PR	Pull-up Ratio
NMH	Noise Margin High
NML	Noise Margin Low
VIH	Input High Voltage
VIL	Input Low Voltage
VOH	Output High Voltage
VOL	Output High Voltage
WSNM	Write Static Noise Margin
CS	Chip Select
INV	Inverter (Not gate)
VTC	Voltage Transfer Characteristics
i_{act}	Effective Current
C_{DE}	Output node Capacitances
V_{INT}	Internal Power Supply Voltage
I_{DC}	DC Current
∇t	Activation time
C_{pt}	Total Capacitance

I_{DCP}	Total Static (DC) or Quasi Static Current
fA	Fampto Ampere
SVL	Self Controllable Voltage Level
USVL	Upper Self Controllable Voltage
LSVL	Lower Self Controllable Voltage
MTCMOS	Multi Threshold Voltage Complementary Metal Oxide Semiconductor
P_{st}	Static Power
V_{thp}	Positive Threshold Voltage
V_{thn}	Negative Threshold Voltage
EDT	Edge Direct Tunneling
I_{sub}	Subthreshold Current
nA	Nano Ampere
I_{gate}	Gate Leakage Current
pA	Pico Ampere
PDA	Personal Digital Assistant
UDVS	Ultra Dynamic Voltage Scaling
WBL	Write Bit Line
RBL	Read Bit Line
RTL	Register Transfer Logic
GND	Ground
VTN	Threshold Voltage of NMOS
V_{gs}	Gate to Source Voltage
V_{ds}	Drain to Source Voltage
L_{eff}	Effective Length

V_T	Thermal Voltage
C_{OX}	Oxide Capacitance
μ_o	Permittivity of Silicon
$I_{diffusion}$	Diffusion Leakage Current
RBDL	Reverse Bias Diffusion Leakage
STI	Shallow Trench Isolation
ST	Store node
STB	Store Bar node
τ_p	Propagation Delay
P_{av}	Average Power Dissipated
PVT	Process Voltage and Temperature
RWM	Read Write Memory
PROM	Programmable Read only Memory
EPROM	Erasable Programmable Read only Memory
FN	Fowler Nordhein
UV	Ultra Violet

CHAPTER 1
INTRODUCTION

1. INTRODUCTION

Excessive demand of Electronic gadgets has led to a new revolution in the field of VLSI technology. These devices are replacing the basic amenities of human life and therefore need to be upgraded for various improvements with the passage of time. Application of VLSI technology is widely spread to various electronic devices from a simple mobile to smart phones, GPS positioning systems, defense and military operations, global communication systems, radars, satellites, medical services and is still not limited. Most of the applications in VLSI possess memories as their integral part to perform various functions and to store the data wherever it is required. Memories play a vital role in making the system intelligent. There are numerous categories of memory to be used in various operations and may possess permanent storage or temporary storage with static or dynamic operations.

New circuits and technologies are developing every year and there are many types of memories that become redundant with time but for SRAM applications in advanced microprocessor, only few are worthy. The DRAM was considered strong with its small size one transistor cell. It was, however, not used due to the specialised process steps needed, and associated prominent increase in manufacturing cost. Planar DRAM which used a standard CMOS process, on the other hand, did not prove to be a viable device for high yield and high volume production. The conventional six-transistor (6T) SRAM, is the main choice for today's applications, meeting the demand of high performance microprocessors.

SRAM is a critical component in almost all digital systems from high performance processors to low power mobile-phone chips. In order to achieve high performance, SRAM must have a

very high density and low power consumption while maintaining high performance of the conventional 6T structure. This research explores a new approach towards a fully Static RAM which can be used to replace a standard 6T [1-2]. The low power VLSI design of SRAM has been widely used as the representative memory for logic. This is because SRAM array operates at a faster rate, and consumes a little power at standby mode. While designing an SRAM, these features are central to digital circuits as they are capable of operating at extremely low supply voltages. The SRAM memory arrays are vital building blocks of the digital circuit. Fabrication of SRAM cell by the same process is another advantage as it needs no extra processing cost. SRAM cannot be obtained by other memories, such as DRAM and Flash memories. Now-a-days, SRAM memory cell array normally occupies around 40% of the logic circuit in VLSI design. Since the characteristics of VLSI circuits, such as operating speed, power, supply voltage and chip size are limited by the characteristics of SRAM memory array. Therefore, a good design of SRAM cell and SRAM array is suitable to obtain high performance, low power, low cost and the reliable VLSI circuits [3].

Low power nano-scale SRAMs are becoming meritoriously important to meet the needs of an extremely fast growing mobile market, to offset the sky-rocketing prices and for increasing the power dissipation of high-end microprocessor units, while ensuring the reliability of miniaturized devices [4]. Information is needed to be saved in high-speed memories for fast access. Memories in mobile devices often contribute to a large extent to the total power consumption. Hence, sub-1V SRAMs have been actively researched and developed. To design such low power SRAMs, the following challenges according to the characteristics, concern the features of memory cell and must be accomplished [1]. Firstly, in SRAM cell leakage current must be reduced, for example, the sub-threshold current increases

exponentially while reducing the threshold voltage (V_t), eventually dominating the active current of SRAM chip. Secondly, the noise margin of SRAM cell must be improved by increasing the signal-to-noise-ratio (S/N) of the design, as it dramatically decreases with device as well as the voltage scaling, causing the degradation in the soft-error characteristic and sensing margin. Thirdly, the performance variations of memory cells caused by variations in processes, voltages and temperature (PVT variations) must be reduced. For example, when we have to look at the ever-increasing variations in $V_{t,}$ an increase in leakage and a degradation in the voltage margin of SRAM cells due to device scaling, is quite disappointing. After that, to accomplish the challenges discussed above, the management of internal power-supply voltages with on-chip voltage converters is required. Lastly, the memory cell size, especially for low power memories, must be reduced otherwise the memory block will dominate the chip size of various VLSI design circuits.

1.1 MEMORY ORGANIZATION

The organization of a memory system is shown in figure 1.1. This organization is known as random-access architecture. The name is derived from the fact that memory addresses can be accessed in random order at a fixed rate, independent of the physical location for reading or writing. The simple cell circuits are arranged in order to share connections in horizontal rows and columns in the storage array or core. The horizontal lines, which are driven only from the outside storage array, are called word-lines, while the vertical lines, along which the data flows in and out of the cells, are called bit-lines. The particularly selected row and column in a cell is accessed for reading or writing. Each cell can store either ‘0’ or ‘1’. Memories may simultaneously select 4, 8, 16, 32, or 64 columns in each row depending on the application.

The rows and columns to be selected are determined by decoding the binary address information [1].

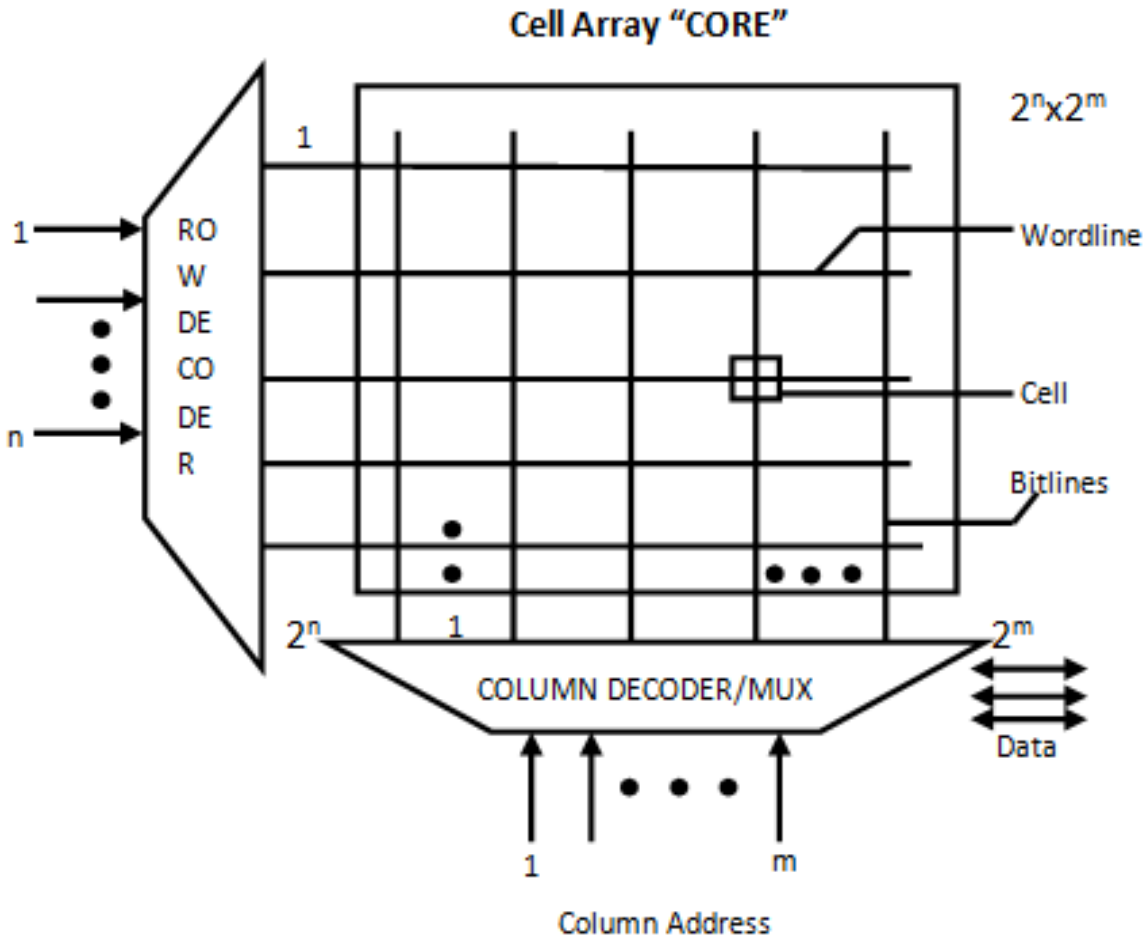


Figure 1.1- Organization of memory system

1.2 TYPES OF MEMORY

The information which is stored in flip-flop circuits or simply as charge on capacitors is called Read-Write Random-Access Memory (RAM). The reading or the writing data encounters approximately an equal delay because it is volatile. Read-Write memories store data in active circuit, i.e. stored information is lost if the power supply is interrupted. The term RAM is commonly used for Read-Write Random-Access Memory, so the natural abbreviation for Read-Write memory should be RWM.

The static RAM (SRAM) and the dynamic RAM (DRAM) are the two most common types of RAMs. As long as the power is on, the static RAM holds the stored value in flip-flop circuits. For the clock cycles in the range of 5 to 50 ns, SRAMs tend to be high-speed memories. Dynamic RAM stores the values on the capacitor. They are slower than SRAMs and vulnerable to noise and leakage problems. However, DRAMs are much denser than SRAMs which are approximately four times in a given generation of technology.

As shown in figure 1.1, ROMs also employ this organization and have a read speed comparable to those for read-write memories. Each ROM uses a different method to write data but they are all non-volatile in nature. The subsequent changes in the stored data are impossible in mask-programmed ROMs because the simplest form of ROM is programmed when it is manufactured by formation of physical patterns on the chip. To exhibit the difference, when manufactured, the programmable read-only memories (PROMs) have a data path present between every row and column corresponding to store '1' in every data position. By providing appropriate electrical pulses to selectively open the row-column data paths, storage cells are chiefly switched to '0' state once manufacturing is over and '0' cannot be written as'1', once programmed or blown.

Erasable Programmable Read-Only Memories (EPROMs) are programmed electrically similar to PROM but all bits may be erased by the exposure of ultraviolet (UV) light. Initially, they have all bits in one binary state. These components have a transparent window over the chip to permit the UV radiation to fall on the packages. Electrically Erasable Programmable Read-Only Memories (EEPROMS) are the most advanced and most expensive forms of PROM. They, too, can be written and erased by electrical means. Unlike EPROMs, E^2PROMs may be either selectively erased or totally erased and can be rewritten to change

even a single bit. All PROMs can retain the stored data when power is turned off, so they are termed as non-volatile. Writing and erasing operations for all PROMs require a time period ranging from microseconds to milliseconds.

A flash memory is the recent form of EPROM and E^2PROM. In flash memory, the blocks of memory can be erased simultaneously. The data in flash memory of the EPROM form is written, using the hot electron effect and these electrons can be created by applying a high field in the channel region, which enter the oxide region and consequently raise the threshold voltage of the device. The device with higher threshold voltage is viewed as stored '1' and the device with lower threshold voltage represents stored '0', whereas, the data in E^2PROM flash is written using Fowler Nordheim (FN) tunneling. This tunneling occurs through a thin insulating material such as, thin-oxide associated with the gate. A current flows across the oxide by tunneling through the energy barrier.

Memories, like FRAMs or FeRAMS, are based on ferroelectric materials. When the power is off, they can also be used to retain information. In this type of RAM, the Perovskite crystal material is used to design the memory cells and they can be polarized in one direction or the other to store the desired value. This results into a non-volatile memory structure, where polarization is secured even when the power supply is switched off. Thus, semiconductor memories are advantageous in terms of cost, operating speed, low power and physical size and eventually, they are preferred over ferroelectric memories for most of the VLSI based applications.

1.3 TRENDS OF SRAM MEMORY CELL

Static Random Access Memory (SRAM) has extensively been used as the representative memory for VLSI circuits. This is because SRAM array consumes a little power at standby

mode and operates as fast as logic circuits operate. The SRAM cell is fabricated by same process as logic circuits, which inherently gives another advantage that of not requiring extra processing cost. These features of SRAM cannot be attained by the other memories such as DRAM and Flash memories. Now-a-days, it occupies around 40% of logic VLSI SRAM memory cell array, so that the nature of VLSI circuits such as supply voltage, operating speed, power and chip size is limited by the traits of the SRAM memory array. Therefore, a good design of SRAM cell and SRAM cell array is expected to have low power, high performance, low cost and reliable VLSI circuits [3].

The 4K SRAM of High-R cell was first proposed as low power [7]. The designing of High-R cell does need bulk PMOS due to which the memory cell size was smaller than the conventional 6T SRAM. For inverter, poly-silicon layer of high-resistivity was used as a load in the SRAM of the High-R cell. The resistivity of poly-silicon layer is around 10^{12} per cell. The memory cell standby current is surprisingly decreased to 10^{-12}. The high-R cell was generally used for high density and low power SRAM memory in VLSI circuits from 4K to 4M bit [7-9]. The operation of the High-R cell at low voltage is discouraged. High-R cell cannot operate at supply voltage of less than 1.5 V. Taking the supply voltage into account, the voltage at cell node needs to be charged to 1.5 V less during read operation while the voltage at cell node should be charged to supply voltage level during write operation. Since the resistivity at the poly-silicon load is high, the time required to charge up node to supply voltage level is also relatively quite long. Instead of High-R cell, six-transistor (6T) cell memories are widely used as memory for logic VLSI circuits, which are sometimes called full CMOS cell.

Although, the 6T cell uses two PMOS transistors and four NMOS transistors, the two PMOS transistors cell area becomes larger than High-R cell. Therefore, the cell does not need an extra processing in the logic process. In addition, the PMOS transistors provide a surge to the voltage at cell nodes so fast, that 6T cell operates at minimum lower supply voltages as compared to High-R cell. Thus, the conventional 6T cell was extensively used for memories for logic VLSIs even when stand-alone SRAM the high-R cell was most popular. Therefore, in additional technologies, a recent supply voltage reduction technique has made the 6T cell predictable for logic VLSI circuits.

The five-transistor (5T) cell is also known as five-transistor SRAM cell that retains its data with leakage current and positive feedback, without refresh cycle. Although, the 5T SRAM cell uses one word-line, one bit-line and an extra read control, the cell size of 5T SRAM cell is smaller than a conventional six-transistor SRAM cell. In addition, it uses the same design rules with no degradation in performance characteristics [10].

The seven-transistor (7T) cell is also known as CMOS seven-transistor cell. To improve the read margin of an SRAM, also called the Static Noise Margin (SNM), additional transistors are used to control the storage node during the read operation efficiently. This 7T SRAM cell uses one word-line, one bit-line and NMOS transistor to control the operation. The delay in this cell is smaller as compared to a six-transistor SRAM cell. The 7T SRAM cell is used for very high density and low power applications. This cell holds its data with leakage current and positive feedback without refresh cycle to perform the read and write operation of the cell. Its leakage current and power consumption with respect to the 6T SRAM cell during read and write operation is less than the conventional 6T memory cell [11].

The eight-transistor (8T) cell is widely used for advanced CMOS device. It uses PMOS device as cell passes the transistors, controlled by the write word-line signal. Complementary write bit-line pairs (WBL, /WBL) are used just as in the 6T SRAM cell. This type of memory cell has two additional NMOS transistors, each for single read bit-line (RBL), for read operation and for write operation [12].

The ten-transistor SRAM (10T) cell is also known as CMOS ten-transistor cell. Just like the 8T SRAM cell, a read buffer within this type of memory cell is available to achieve a pre-chargeless RBL structure using the pull-up transfer PMOS transistors and a complementary read word-line pair (RWL, /RWL). Although, this 10T SRAM cell has a larger area penalty than that of 8T SRAM cell and conventional 6T SRAM cell, depending on the toggle rate of read out data, the active power can be reduced further. Thereby, under the low voltage operation, it becomes more effective in power reduction.

However, this single ended bit-line structure operates at a full voltage swing for RBL. The former 8T SRAM cell requires a keeper circuit for RBL, incompatible to the readout data while due to local V_t operation, large transition time verification of RBL becomes a disadvantage. Where weak drive strength of the serially connected pull-up PMOS takes the rising time RBL into consideration in 10T SRAM, ladder cell is another disadvantage.

1.4 DESIGN OF SEVEN TRANSISTOR SRAM CELL WITH DIFFERENT TOPOLOGIES

1.4.1 Device Parameters

Both device and technology parameters are central to the design of a circuit. Before designing any circuit, we must assign the values to the various parameters as we have done in the first step.

S.No.	Device Parameters	Memory cell (7T SRAM cell)
1.	Technology	45 nm
2.	Supply Voltage	0.7 V
3.	Precharge Voltage	1 V
4.	Temperature	27^0C
5.	S/D Metal width	60 nm
6.	Gate Spacing	160 nm
7.	Source Drain Length (left)	140 nm
8.	Source Drain Length (right)	140 nm
9.	Source Diffusion Periphery	520 nm
10.	Drain Diffusion Periphery	520 nm
11.	Source Diffusion Area	16.8 fm^2
12	Drain Diffusion Area	16.8 fm^2

Table-1.1: Device Parameters for 7T SRAM cell

The 7T SRAM cell has an area penalty (defined as cell area between 6T and 7T) as compared to 6T SRAM cell. The area penalty which is due to the functionality constraint of 7T SRAM cell has been overcome, since other transistors used for design are of minimal size. Device parameters used in Cadence tool for the designing of 7T SRAM cell are shown in Table 1.1.

1.4.2 Seven Transistor SRAM Topologies

In recent years, low power applications have gained a lot of attention. Due to continuous scaling of CMOS and low leakage, SRAM will continuously be in demand due to the rise in battery-operated portable applications. Therefore, a new approach should be evolved to reduce the leakage constraint. Device optimization is a must for low leakage of SRAM to further reduce the power and to enhance the performance. Both, area and cell stability should be taken care of while optimizing the power reduction. The 7T SRAM cell is used to enhance

the read/write stability under large variations. It uses a low overhead read/write assist circuitry to increase the noise immunity. The use of an additional transistor and a floating ground allows a read operation without any disturbance [13].

1.5 MEMORY CELL DESIGN TECHNIQUES AND ARRAY DESIGN TECHNIQUES

There are enormous different paths to obtain reliable, low power and small size 7T memory cell. As per the Moore's law, scaling size of 6T SRAM cell and the feature size of transistors in 6T cell are reduced. Supply voltage of 6T cell reduces as the feature size is reduced. Due to scaling, variations in the threshold voltage transistors and leakage in transistors have increased. Therefore, the supply voltage of 7T memory cell array has been reduced by scaling. Recent low power circuit techniques such as, Dynamic Voltage Frequency Scaling (DVFS) also need further low voltage operation for the memory cell arrays.

The 7T SRAM cell must be designed in such a manner that it is electrically stable at low supply voltage despite large variation in transistors. The memory cell size must be as small as possible to attain small chip size VLSI circuits. The leakage of 7T SRAM cell array must be less instead of large leakage in transistors in the cell. In addition, immunity of soft errors due to alpha particles or neutrons must be minimized to obtain reliable VLSI circuits.

SRAM cell array design technique plays a vital role in reducing the power consumption. Dummy cell design techniques provide an extra edge to adjust the activation timing of sense amplifier so that stable SRAM operation is achieved with PVT variation-circumstances. Reliability concerns are inevitable to the SRAM memory cell and cell array design. Various reliability issues such as soft errors caused due to alpha particles and neutron particles are serious issues [3].

1.6 PROBLEM FORMULATION

From the extensive literature being reviewed on the topics that relate to low power memory cell design, it has been observed that different types of memories exist today. Also new technologies and circuits are developed every year. But for, SRAM applications in advanced microprocessors, few have been proven worthy. This, together with the high performance demands of microprocessors, has resulted in the conventional six-transistor (6T) SRAMs being the main choice for today's applications. The purpose of this thesis is to show a new and a fresh approach to a fully static SRAM that can be used to replace the standard 6T. For this, it has to be low powered while maintaining the high performance of the 6T. It is also an important issue in the design of a 7T SRAM cell using various techniques, circuit topologies, process and material parameter combinations for low power memory cell design.

The usage of SRAM is continuously increasing in system on chip design in the present era. Process technology scaling has contributed remarkably in improving the performance and area density of system on chip design. The SRAM cell typically contains the minimum sized transistor in order to realize high density. With the resultant effect of increased intra die variations with the technology, scaling is more pronounced on the SRAM cells. The SRAM scaling has become extremely difficult in the advanced technology nodes (e.g. 65, 45, 32 nm LP CMOS technology).

The lowest operation VDD for embedded memories SRAM is limited by either SNM_{read} (Cell Stability) or write ability [write margin (WM)]. For low VDD values, the read SNM becomes negative (bistability loss). This is because of the reduced signal levels at the low VDD levels and also because of the effect of V_t variations. The SRAM cell ratio is defined as the (W/L) of the NMOS pull down transistor of inverter to the (W/L) of the NMOS pass transistor. The

cell ratio manages stability and performance of the cell. For stability, the increment in the cell ratio reduces the risk of data flip during the read operation.

However, for sturdy performance pass transistor is required. The conventional 6T SRAM cell topology has an inherent disadvantage that it requires a very complex trade-off between cell stability (SNM_{read}) and performance (I_{read}). The higher value of cell ratio fulfils the cell stability requirement but has a negative impact on Iread. Similarly, lower value of cell ratio increases Iread requirement but also increases the risk of data flips (less stable).

There is another problem associated with the write ability which causes write failures in the SRAM cell. A failure to write occurs when the pass transistor is not strong enough to overpower the pull up PMOS transistor and pull the internal node to ground node (Writing "0"). This dissertation describes the 7T SRAM cell topology which solves the issues like degraded SNMread, Iread and WM for low VDD SRAM.

In 7T SRAM cell, one extra transistor is inserted into the 6T SRAM cell structure for loop cutting. It enables differential write operation and single ended read operation. During an idle mode when the cell is not accessed, an extra transistor is turned on and the data retention process is exactly same as that of 6T cell. During read operation, the extra transistor is deactivated. The logical threshold voltage of the CMOS inverter driving node Q or QB becomes very high. Power supply voltage modulation is an important aspect which changes the stability of SRAM cell. Static Noise Margin of SRAM cell also depends on power supply (VDD), during read and write mode and has been widely accepted in nanometer technologies. When we increase the value of power supply (VDD), the value of SNM linearly increases with the increase in leakage current. Bit-line voltage modulation is observed to calculate the requirement of pre-charging bit-lines at a full power supply voltage. The SNM can be slightly

improved by decreasing the bit-line voltage compared to VDD during read operation. This technique increases the cell stability and is suitable with voltage modulation. The reduced bit-line voltage move may allow for a read-mode SNM improvement without the need of any changes in the SRAM cell array design.

The word-line voltage modulation is another technique to improve the stability of cell at low power supply voltage levels suitable with recommended cell layout ($\alpha \approx \beta \approx 3$). This technique is based on minimizing the maximum voltage swing of the word-line to sustain the cell access transistor during the read operations. The SNM can be improved by reducing the word-line voltage during read operations with respect to VDD. This approach may allow a great improvement of SNM.

1.7 OBJECTIVE OF THE THESIS

The following are the objectives of the thesis:

- To study the various techniques (Circuit topologies and process & material parameter combinations) for low power memory cell design, through their modeling and simulation.
- To design a memory array using cells and assess its performance.

1.8 THESIS OUTLINE

This thesis is organized in the following manner: Chapter 1 is Introduction. Chapter 2 deals with the literature survey and related works. Chapter 3 presents High density low leakage current based SRAM cell. Leakage current techniques are discussed in Chapter 4. Chapter 5 includes the design trade-off and material parameters. Chapter 6 describes design of SRAM cell based memory array. Finally, in Chapter 7, the conclusion of the research work has been presented. Thesis organization is given in figure 1.2.

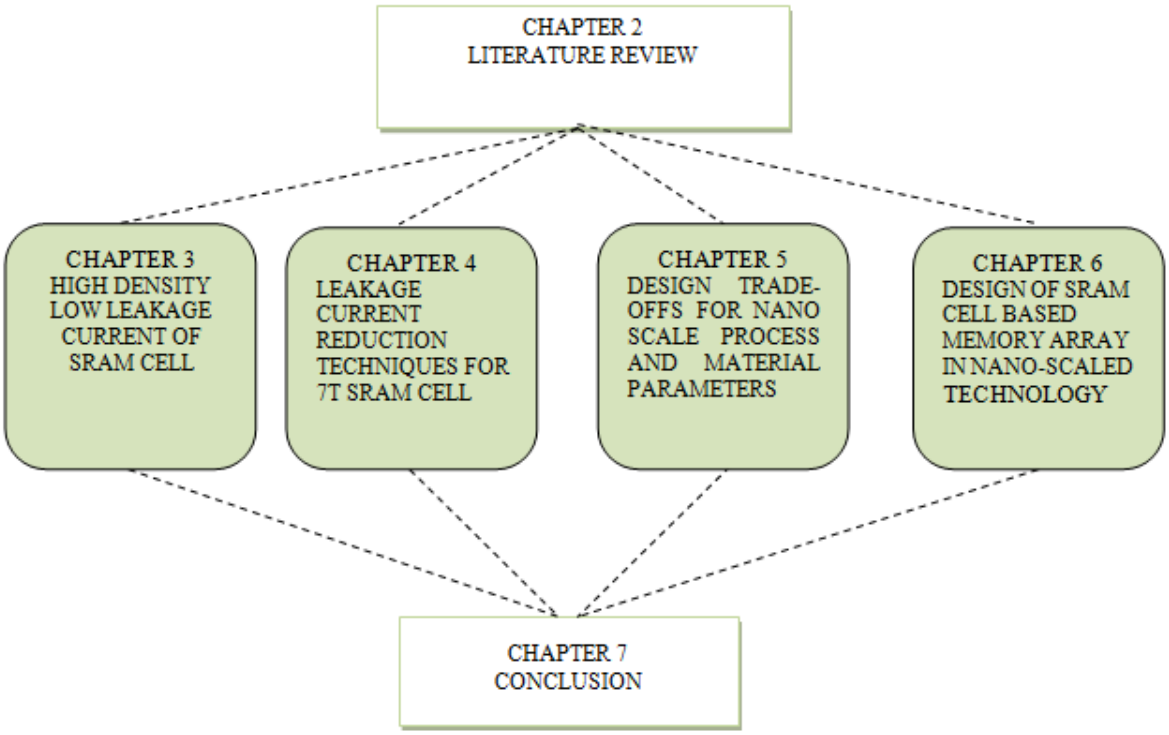


Figure 1.2- Thesis outline

Chapter 1 gives the introduction of the thesis. It describes the SRAM Cell array with its components, leakage reduction techniques and different parameters which affect the array performance.

Chapter 2 presents the literature survey about the SRAM Array, FinFET Array, cells with improved schemes, parameters and sense amplifier. This chapter focuses on various leakage current and power reduction techniques. It also includes the temperature variation effects on array and its simulation.

Chapter 3 describes a high density low leakage current based SRAM cell, its components and shows the simulation results. It also has the corresponding process parameters.

Chapter 4 deals with the leakage current reduction techniques. Performances of these techniques have been compared with the previous one.

Chapter 5 describes the design trade off for nano scale process and material parameters. This chapter focuses on some design techniques of SRAM cell and the useful material for the low power design, as technology and material greatly impact the power consumption.

Chapter 6 presents SRAM cell base Memory Array. In this chapter 8kb SRAM array is constructed using 7T SRAM cell to show the feasibility of the SRAM cell and this array must operate at low voltages operation to reduce the operating power.

Finally chapter 7 concludes the research work and gives future scope which can be used to extend the work in this field of research.

CHAPTER 2
LITERATURE REVIEW

2.1 SRAM CELL ARCHITECTURES

2.1.1 Six-Transistor (6T) Memory Cell

SRAM cell is designed in such a way that it provides a non-destructive read operation and a reliable write operation. In the conventional 6T SRAM cell, this condition is fulfilled by appropriately sizing all the transistors in the SRAM cell. Sizing is done according to the cell ratio (CR) [17]. Traditional SRAM cells are symmetrically composed of transistors with identical leakage and threshold characteristics as shown in figure 2.1

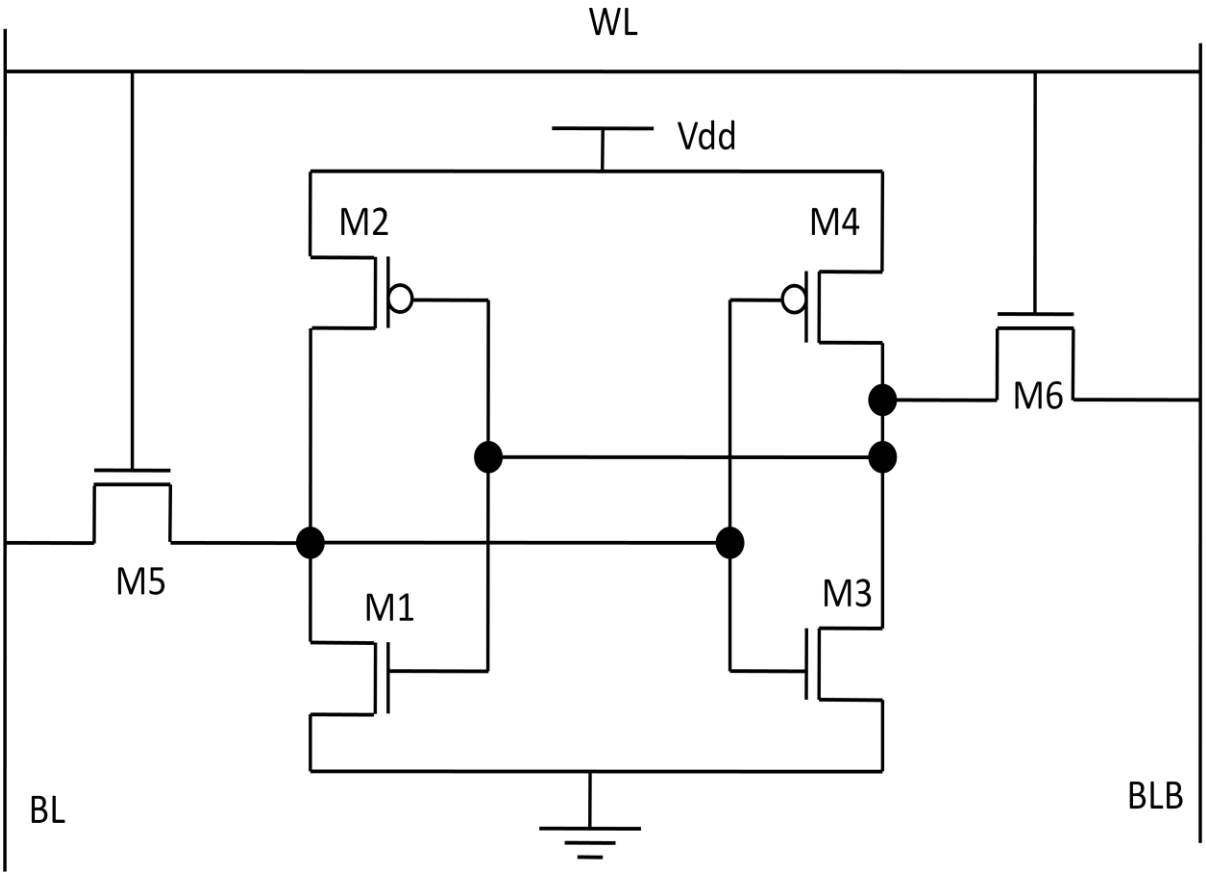


Figure 2.1 Basic Memory Cell

2.1.2 Sub-threshold 6T SRAM Design

The limitation of traditional six-transistor (6T) SRAM cell lies with its low voltage operation. It proposes an alternative bit-cell that functions for small voltages. Using the measurements, it confirms that a 256-kb, 65 nm SRAM test chip of proposed bit-cell operates below sub-threshold which can be upto 400 mV [18]. This low voltage SRAM memory provides substantial power and energy savings at the cost of speed and other energy-constrained well-suited application.

2.1.3 Dual V_t SRAM Design

The proposed Low-Leakage asymmetric Dual V_t Static Random Access Memory cell design reduces the leakage power in cache so as to keep the existence of low access latency. This design exploits the strong bias towards zero at the bit level exhibited by the memory value stream of ordinary programs. As compared to other conventional symmetric high-performance cell, this cell presents an acceptance for significant leakage reduction in the zero state as well as one state of some other cases [19].

2.1.4 SRAM in threshold Region

A new 6T SRAM design is the design which can work in threshold region to minimize the leakage power and speed. A negative word-line is added for the calculation of reducible leakage current and a latch-type voltage sense amplifier to increase the read speed of given SRAM cell [20]. This SRAM is simulated at 45 nm technology and achieves near about 50% of power reduction and leakage reduction upto 68%, write delay reduction upto 90% and read delay upto 78%.

2.1.5 Different Schemes for SRAM Architectures

A new scheme has been presented here to reduce the deterioration of the read speed and cell stability at low power supply voltage for utilizing a small offset-voltage (Vos) sense amplifier. By using this new concept for realizing a low-voltage-operation, SRAM with a small area is used and also the transistor threshold voltage shift caused by hot carrier injection is used for small offset-voltage trimming after chip fabrication. This scheme has been observed to be more effective when applied as a repeated trimming [21]. Anker Goel et al, proposed the negative bit-line based write-assist scheme for SRAM design in the nanometer technologies [22]. This technique can be used to improve the write ability of 6T single port (SP) and 8T dual port (DP) and of other multiport SRAM Cells also. On-chip using capacitive coupling, the negative voltage is generated during the write operation, only the bit-line on which a '0', is to be written on negative. This technology does not affect the read operation for bit-interleaved architecture enabling high-speed operation. Wen-Tsong Shiue et al, developed heuristic based procedure for multi-port, multi-module design that satisfied the area and/or energy timing constraints. The heuristic algorithm is supported through the understanding of the area-energy/timing tradeoffs by using the grouping of same bit arrays width which causes reduction in the area of the design but an increase in the energy. Similarly, splitting of already grouped bit arrays causes a reduction in the energy but as a result an increase in the area occurs [23].

2.2 SRAM WITH VARIOUS DESIGN TECHNIQUES

2.2.1 SPRAM Design

A 32-mb spin-transfer torque RAM (SPRAM) with 2TIR memory cell, an access time of 32 ns and cell write-time of 40 ns at a supply voltage of 1.8V. This SPRAM has three circuit technologies used for the design of large-scale array [24]. 1) Two transistors and one resistor

(2T1R) type memory cell are used to design a small size memory cell at sufficiently large write current despite. 2) A separate read/write compact hierarchy of bit/source-line structure is used with a localized bi-directional write driver for the efficiency of distribution write current. 3) It is used for the performance of stable read operation to design a scheme of '1'/ '0' dual- array equalized reference.

2.2.2 Charge-Recycling SRAM Design

A low-power SRAM using bit-line can be used for charge-recycling, and for performing read and write operation. This charge-recycling SRAM (CR-SRAM) technique reduces the power of read/write by recycling the charge in bit-lines. When N-bit-lines recycle their charge, the voltage of bit-lines is reduced to 1/N and the power of bit-lines is reduced by $1/N^2$ respectively. Byung-Do Yang et al, proposed Charge-recycling SRAM. This technique utilizes hierarchical bit-line architecture to perform charge-recycling without using static noise margin degradation in memory cell [25].

2.2.3 Adaptive Dynamic Word-Line under Drive Design

A 32 nm high-K metal gate SRAM with adaptive dynamic stability enhancement for low-voltage operation on word-line under drive (ADWLUD) scheme uses a bit, cell-based sensor to dynamically optimize the strength of WLUD for each die. Pramod Kolar et al, introduced sensor tracks process corners and temperature shifts allowing dynamically adjusting WLUD. The sensor area overhead is limited to 0.02% and power overhead is limited to 2% for a 34 mb SRAM array [26].

2.2.4 Data-Aware-Feedback-Cutoff Design

A 9T-SRAM cell with a data-aware-feedback-cutoff (DAFC) scheme is used to increase the write margin and a dynamic-read-decoupled (DRD) scheme in order to prevent read-disturb,

for achieving the deep sub-threshold operation. Upto 30 mV, a negative-pumped voltage is applied to the unselected word lines to suppress the bit-line leakage current. The 32 kb, 9T SRAM cells are stable for performing read and write operation at 105 mV. The shorter bit-line length overcomes the bit-line leakage issue [27]. This 9T SRAM cell is enabled at low-VDD_{min} sub-threshold chip feasibility for ultra-low-power application as well as energy harvesting based low-voltage systems.

2.3 NOISE COMPENSATION SENSE AMPLIFIER

This is a new scheme of bit-line sense amplifier for improving the performance in the presence of data-pattern-dependent sensing noise. Myoung Jin Lee et al, also suggests that there would be A 81.5% reduction in the amplitude of available data-pattern-dependent sensing noise. Simulation measurement shows the sensing scheme improvement of sensing noise over a conventional bit-line sense amplifier. Finally, an optimum data pattern noise, insensitive sense amplifier and a driver are also proposed [28].

2.4 HIGH DENSITY MEMORY

Multi-step word-line control technology in hierarchical cell architecture is used for scaled-down high density SRAMs with no area penalty controlling WL voltage, so as to keep DNM close to zero. The write cycle operation can be performed successfully through half-select. The multi-step word-line control is used at $0.248\mu m^2$ cells while maintaining sufficient DNM and WM upto 2.98 mb/mm^2 bit density and upto 78 % cell-area efficiency. Using this technology, hierarchical cell architecture (HCA) has been developed to minimize the speed problem. Koichi Takeda et al, fabricated a 2 Mb SRAM with a single-power supply macro using a 40 nm CMOS technology and also by joining the hierarchical cell architecture with multi-step word-line control technology [29]. A 4ns access time can be achieved by designing

a 2 mb SRAM. Takashi Ohsawa et al, generated an accurate reference current for data sensing in high-density memories by averaging the multiple pairs of dummy cells of a large scale memory with resistance change cell [30]. These special characteristics are confirmed by comparing with the footing body random access memory on the basis of their functionalities and the retention time distributions. The ways are found to be especially effective in situations where degraded signals are absolutely suitable for the sensing of the signals until bit-cells are in retention time distributions thus improving the FBRAM retention time performance drastically. By using the sense amplifier circuit which has positive feedback loop for sensing, data cannot be joined with dummy cell on averaging schemes. Elaine Ou et al, explores the design and quality of being capable for an array structure of a non-volatile three-dimensional cross-point resistance change memory. Using this resistance-change, memory cell serves for both of communicating with the element as well as with the memory element to be obtained by separating the need for individual selection devices. He also presents minimized leakage current effects while maintaining a high effective bit density circuit technique of specific architecture. The memory cell device characteristics become increasingly absurd with large memory layers and for large opportunities leakage current, a vertical connection establishes between memory array layers on the memory. Finally, a four-layer cross-point memory can be fabricated significantly with a greater bit density than Nand-flash memories [31].

2.5 SRAM NOISE MARGIN ESTIMATION

2.5.1 Read margin

Improvement of read margin and its distribution by V_{TH} mismatch self-repair the 6T SRAM with asymmetric pass gate transistor which is formed by post-process local electron injection.

Pass gate transistor increases the margin for each cell without following up its characteristics and the local electron injection is automatically and simultaneously achieved. The asymmetric V_{TH} shift is twice as maximum as the conventional by applied scheme without process and cell area penalty. The self- repair function is proposed by Kousuke Miyaji et al [32]. This scheme enhances the maximum read margin upto 70% and decreases read margin distribution upto 20%. Vibhu Sharma et al, developed the wireless sensor applications at ultra low energy, A 128 Kbit 6T SRAM low power CMOS with energy consumption of 4.4 PJ/access is achieved in 90 nm technology, operating at 80 MHz [33]. The architecture of SRAM memory cell for performing read/write operation has been developed for high variability resilient and low power techniques. The low swing global bit-lines also include the energy-efficient herarchichal bit-lines structure. The variability resilience as well as the maximum energy reduction compared with the existing calibration technique is added with multi-sized SA redundancy calibration technique for the global read sense amplifiers of the SRAM.

2.5.2 Asymmetric Sizing for Read Stability

Here, five-transistor (5T) memory bit-cell is displayed with asymmetric sizing for improved read stability and to provide an efficient knob for trading of the aforementioned metrics. Satyanand Nalam et al, compares the 5T to show that it can be a flexible, intermediate alternative between the two conventional 6T and 8T SRAM [34]. The simulation results are obtained at 45 nm technology to test the chip and to investigate that the 5T SRAM is single-ended sensing. The 5T can be demonstrated through figure 2.2 and the comparable write ability down to 0.7V while showing no read errors down to 0.5V through a combination of write assists.

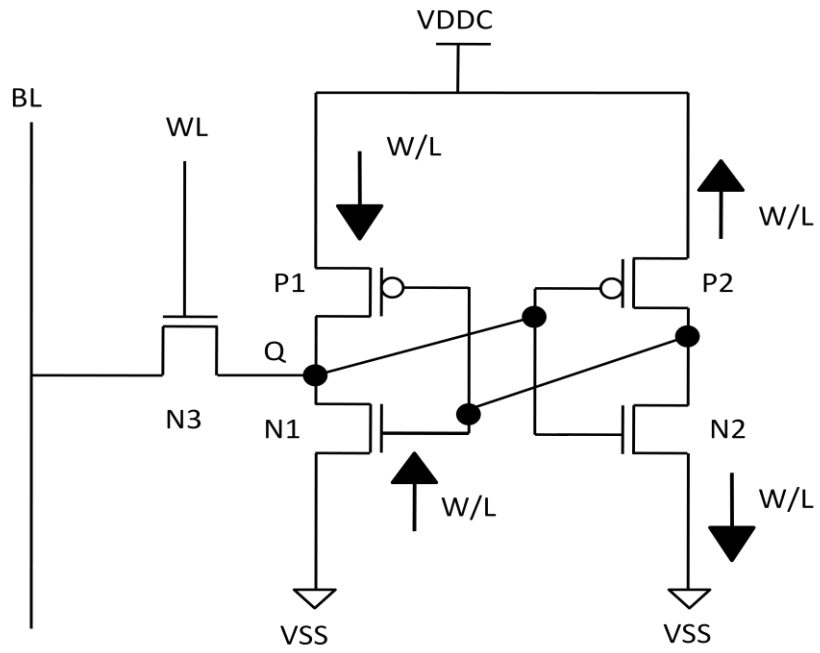


Figure 2.2 Asymmetric 5T Memory Cell

2.6 PERFORMANCE AND AREA SCALING BENEFITS FOR SRAM DUE TO SUB-MICRON TECHNOLOGY

2.6.1 A 28 nm Dual-Port SRAM

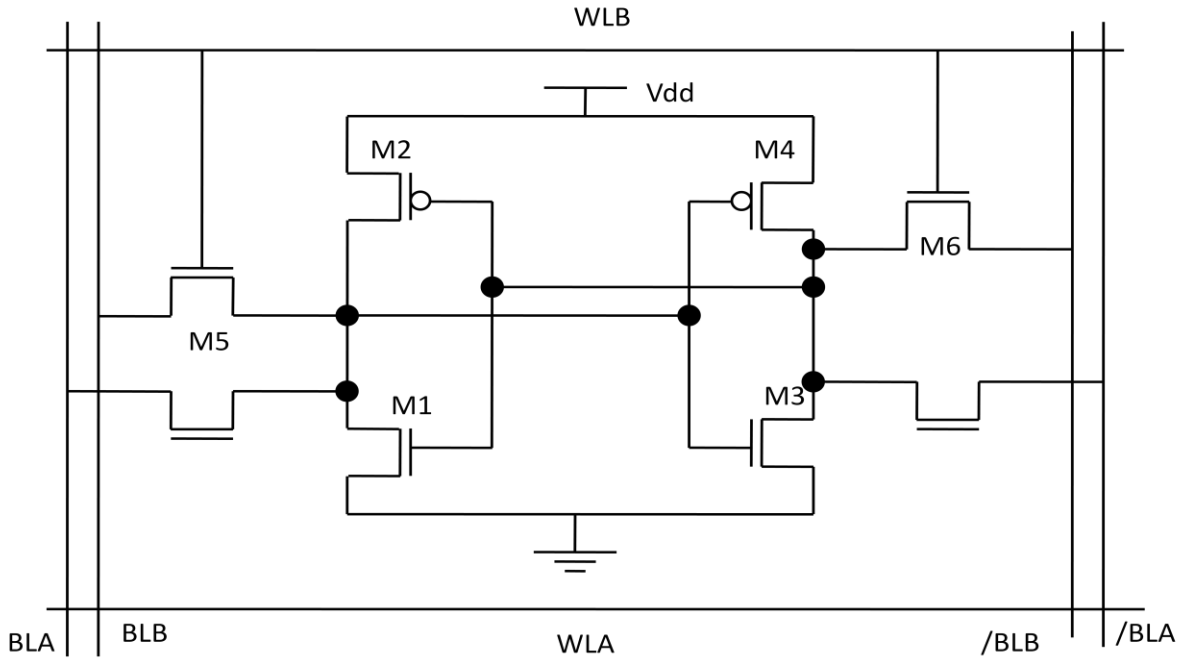


Figure 2.3 Dual Port Memory Design

It is a circuit technique to detect the worst Vmin in asynchronous clock operation. As shown in figure 2.3 the write/read-disturbing condition with a finite clock skew is determined by the worst minimum operating voltage (Vmin) of an 8T dual-port (DP) SRAM. This circuitry allows the circuit to screen the worst bit in an array which is conventionally obtained by a costly and a time-consuming test procedure. He proposed a circuit that is designed and fabricated in a 512-kb DP-SRAM macro using 28 nm low power CMOS technology, successfully reproducing within 6% discrepancy, which is confirmed experimentally that the worst V_{min} to be screened is without using asynchronous clock [35].

2.6.2 The 40 nm CMOS technology

It is a digitized replica of a bit-line delay technique for the generation of random-variation-tolerant timing of SRAM memory sense amplifiers. A sufficient count of replica cells and replica bit-line delay is digitized and multiplied to adjust it to the target timing for SA which is reduced by the random variation of transistor threshold voltage (V_{TH}) through the timing variation of sense amplifiers attribute.

By using this scheme, as shown in figure 2.4 at 40 nm CMOS technology, the variation of the generated timing was 41% less than the conventional technique and also the cycle time was reduced to 20% at supply voltage (VDD) of 0.6V as given by Yusuke Niki et al [36]. Adam Teman et al, presents a novel 9T SRAM bit-cell which describes implementing a supply feedback concept to internally weaken the pull-up current during write cycle thus enabling the low-voltage write operations. The full range of supply voltage is as low as 250 mV applied to the proposed bit-cell providing the robust functionality under global and local variations. The cell provides, in its stable state the internal leakage suppression, resulting in a 15%-16% reduction of static power as compared to an 8T SRAM cell, depending on the

implementation of same supply voltage. At voltages from 250 mV to 1.1V, the proposed bit-cell is fully functional under global and local variations [37].

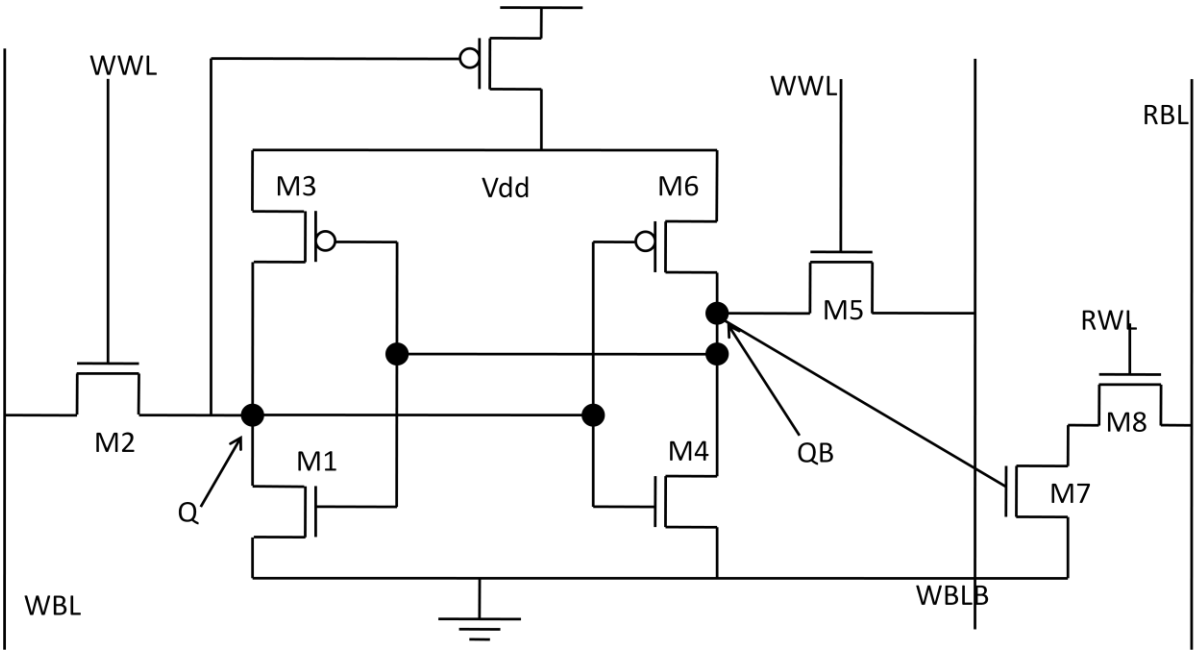


Figure 2.4- 8T Memory Design with bit line delay technique

2.6.3 The 45 nm CMOS technology

Seng Oon Toh et al, evaluated the past to ensure continued scaling of bit-cell size and supply voltage in future technology nodes for the optimization of SRAM yield using dynamic stability metrics. These dynamic stability metrics are proposed but they have not been used in practical failure analysis and are compared with conventional static margin. The 45 nm CMOS technology implemented the stability characterization architecture using pulse word-line to identify the source of variability and their impact on SRAM stability [38]. The static write margins failed to predict outliners in critical writability and static read margins were calculated to overcome the failures by 10-100X. The low frequency RTN signaling of large amplitude in SRAM transistors causes shift in dynamic stability of similar magnitude that depends on bit-cell access patterns. The temporal variability in transistor characteristics and

the critical writeability magnifies the impact of process-induced, compared to static write margins.

2.6.4 A 64 Mb SRAM in 32 nm

A 64 Mb SRAM macro has been fabricated in 32 nm high-k metal gate SOI technology at 0.7V, operation enabled by stability, write-ability and read-ability enhancements. In a bit-line regulation system, the stability is improved and does not degrade the write margin, using a scheme of bit-line boost and boost control, that features a 40% improvement in bit-line. Boost voltage is achieved by low voltage write-ability as compared to the previous design. Lastly, to improve both performance and yield across the process, space is implemented by Harold Pilo et al, using a bit-cell-tracking delay circuit [39].

2.7 BENEFITS OF INTEGRATED LINEAR REGULATOR TECHNOLOGY FOR DUAL SUPPLY SRAM

Chun-Yen Tseng et al, presented an integrated linear regulator with fast output voltage transition for dual-supply voltage of a SRAM cell to improve the read and write margins in a DVFs System. For system-level power saving is an effective way of dynamic voltage and frequency scaling (DVFs), so as to minimize the timing overhead during the mode transitions and adopt the two separate feedback loops for reference tracking and load regulations. The simulation result shows a good performance on both the steady-state and dynamic behaviour [40].

2.8 A HIGH-SPEED LOW- POWER MULTI-VDD SRAM WITH WRITE/READ ASSIST TECHNIQUES

A high-speed low power SRAM using three power supplies with different output voltages has a great advantage of making it makes it possible for high performance ULSI with low power

dissipation. The SRAM core, to save the standby and/or active power, is mainly used for 1V power supply. The critical components are used to realize the high performance using 2V power supply. Upto 2.2V, each MOSFET voltage is applicable because of the use of a 5 nm ultra thin gate oxide and maximum of 3.3V power supply is used only for LV-TTL level and I/O buffers. The six-transistor memory cell is guaranteed by using a new switched power line impedance scheme which is a secure write operation for 1V. A segmented bit-line scheme is adopted by Nobutaro shibata et al, and long global bit-lines are assigned for the topmost layer to reduce the dynamic power dissipation [41]. During standby mode, the power dissipation of the maximum 3.3V input/output buffers is less than 0.3mW and the values for 100 MHz operation are 5.8 mW (write) and 11.0 mW (read). Zheng Guo et al, presents a method for using direct bit-line measurement of large-scale characterization of read stability and writeability in functional SRAM arrays at 45 nm technology node [42]. The excellent correlation near failure of SRAM DC RSNM and I_W is conducted in small SRAM macros with all-internal node. Access measurement shows the large-scale read/write margins and V_{MIN} in a functional SRAM array and then direct correlation between them is established. Finally, the result shows the direct connection between the large-scale read/write metrics and $V_{MIN,}$ exceptionally at lowest read/write margin and high V_{MIN} regions. This states that large-scale read/write metrics can be used for V_{MIN} position. The SRAM V_{MIN} impact of four conventionally used read assist and write assist techniques is evaluated and compared.

2.9 A RESILIENT SELF-VDD-TUNNING SCHEME FOR LOW-POWER SRAM

On-chip self-V_{DD}-tuning scheme with speed-margin for low-power SRAM automatically adjusts each SRAM macro manufactured to a minimal voltage near its $V_{minf.}$ Finally, the simulation results of 64 Kb SRAM design indicate that when the fabrication of the chip is

done, the temperature ranging between 25^0C and 125^0C can well tolerate the doubtful practices. Ya-Chun Lai et al, presented a self-V_{DD} tunning scheme in which maximum 40%, power reduction is achieved for an 8 Kb SRAM macro operating at 150 MHz and the supply voltage is reduced from 1.8V to 1.08V on the chip [43]. Tae-Hyoung Kim et al, proposed new circuit techniques for lowering V_{min} and minimising the leakage. A voltage scalable 0.26V, 64 Kb 8T SRAM with 512 cells per bit-line is achieved with 130 nm CMOS technology. The write cell margin and read performance improve without the aid of any peripheral circuits using the reverse short channel effect in SRAM cell design. The bit-line leakage current which becomes similar to read current at a sub-threshold supply voltage can be compensated by using a marginal bit-line leakage compensation (MBLC). This MBLC permits lower V_{min} upto to 0.26V and also removes the need for precharged read bit-lines. This short term, read bit-line and write bit-line scheme reduces the leakage power consumption. The read word-line pulse with control scheme automatically improves the readability and reduces the wasted read power by tracking the PVT variations [44]. Muhammad Khellah et al, presented two approaches to enable the V_{MIN} reduction of DNF 6T SRAM cells. The first approach is a new WL under-drive (WLUD) circuit that enables a read stable DNF cell with all minimal sized devices. The WLUD of 6T SRAM cells circuit is used for both PT and supply noise tolerant, improving write stability through dynamic voltage collapse (DVC) scheme that trades the large dynamic cell retention margin. The second approach introduces the new idea of DNF P-cell with pMOS pass device and highly charged bit-lines. Using this cell through upsizing, the nMOS PD without creating a notch as in conventional cell, is inherently read ratioed and an extra read margin can be obtained similar to the M-cell with WLUD [45]. Yen Huei Chen et.al, describes an adaptive mechanism to generate cell-VDD (CVDD) which tracks a certain

voltage offset with respect to the logic-VDD. This dual-rail SRAM circuit works at a minimum voltage lower than the VDD i.e. 0.6V. The bit-line (BL) is precharged to VDD, instead of CVDD. The application of this design is to oscillate the IR-drop constraints for P & R flow on the CVDD. Power mesh routes and exits the leakage saving mode and precharges to full-rails for quick recovery time for the BL. Finally, 1-M bit compiler SRAM can be measured upto 45 nm data and it successfully pushed the VDD_min upto minimum 0.6V [46].

2.10 DYNAMIC STABILITY METRICS OF SRAM

Rajiv V. Joshi et al, studied the impacts of floating body effect, device leakage and gate oxide tunneling leakage on the read and write-ability under V_t, L, W variations in sub-100 nm technology of a PD/SOI CMOS SRAM cell. The read stability is degraded while improving the write-ability using floating body effect and using the gate-to-body tunneling and the current increases the read stability while degrading the write-ability. The improvement in leakage, read and write-ability is attained without causing any significant performance degradation using a high V_t and thick oxide cell transistors [47].

2.11 HIGH-DENSITY 2RW DUAL-PORT 8T-SRAM

A new access scheme for a synchronous ultra-high density Dual-Port (DP) SRAM minimises the 8T-DP and maintains cell stability and cell area. Using this scheme, the smallest 8T-DP-cell and the highest bit-density has already been noticed in the 65 nm era. Koji Nii et al, opined that the speed penalty was negligible and standby leakage was reduced upto 27% because of the cell design size [48].

2.12 APPROACHES FOR MEMORY STABILITY

2.12.1 Static Noise Margin (SNM)

The dynamic criterion of cell data stability by conscious design of the cell operates between access and non-access conditions alternating in a dynamic environment. Launched a new bound for the cell static noise margin (SNM) using the dynamic data stability criteria. It is thus evident that the true noise margin of the cell can be much higher than the conventional SNM. Once the cell access time is self sufficiently less, the cell-time does not alter. This technique can be used to increase the noise margin in sub-threshold SRAM. Finally, to maintain the data stability with proper choice of access and recovery time constant, the sub-threshold operation of the cell is developed. Mohammad Sharifkhani et al, introduced extended read/write noise margin to realize a low leakage current of segmented virtual grounding architecture. The AR operational modes are introduced to the SRAM cells for read/write operations and are performed by accessed row but they are neither selected nor they discharge their bit-lines, hence they save energy. The read and write operation, by controlling the cell, access time and cell supply voltage, enhance the stability of the cells. Finally, the result shows that upto 28% of noise margin can be enhanced using this scheme [49-50].

2.12.2 Robust SRAM Design via (BATT) scheme

A BIST-assisted timing-tracking (BATT) scheme as shown in figure 2.5 is used to make robust read operation easy without giving any circuit performance in an SRAM design.

This scheme has a very low area overhead for tracking the worst-case silicon speed of the bit-lines. It commonly uses the existing memory BIST circuit. The SRAM compiler needs to support a wide & varied range of configurations of this scheme and, thus, it is more suitable

because it is highly scalable. The measurement result from the test chip shows that this scheme can rescue one chip that may have failed using the traditional timing-tracking scheme given by Ya-Chun et al [51].

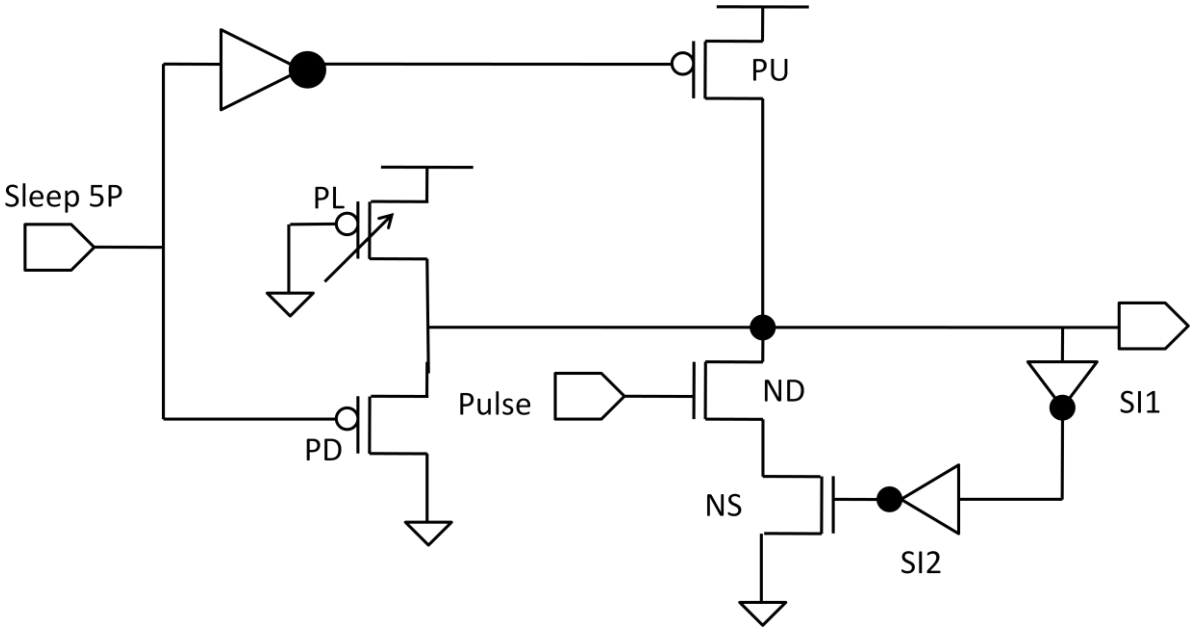


Figure 2.5 SRAM design using BIST-assisted timing-tracking scheme

Ik Joon Chang et al, deduced a differential 10T bit-cell that effectively separates read and write operations thereby achieving high cell stability [52]. Soft error tolerances with conventional error correcting codes (ECC) are also achieved using the proposed bit-cell thus supplying efficient bit-interleaving. The dynamic DCVSL scheme compensates for bit-line leakage noise, thereby improving bit-line swing for read access. A 10T SRAM cell allows the bit interleaving with the column-wise write access control while having differential read path. Finally, a 32 Kb array of the proposed 10T bit-cell is fabricated in 90 nm CMOS technology. Fatih Hamzaoglu et al, developed a 153 Mb SRAM, a high performance 45 nm high-k metal gate technology. The standby leakage and the lower active- VCC_{min} in the design are an integration of active-controlled SRAM VCC in sleep mode and dynamic SRAM PMOS forward-body-bias (FBB). Dynamic FBB is used to improve the SRAM active-VCC_{min} upto

75mV and active- controlled SRAM VCC distribution tightened by 100mV. The VCC_{min}, performance, leakage and area are optimized through a 0.346 μm^2 area of 6T SRAM Cell [53].

2.12.3 PMOS Forward Body Bias Technique

Naveen Verma et al, 2009 presented a high-density 45 nm SRAM using small-signal non-strobed regenerative sensing so that the array performance is limited by sense-amplifier offset. The performance degradation of sense-amplifier that targets simple offset compensation of high-speed node, reduces the sensitivity to a variation while imposing minimal load. Stable internal voltage references serve as an integral means to self-trigger the regeneration so as to avoid the tracking mismatch in an external strobe-path. The bit-cell parameters can be optimized by using a precise small-signal detection to withstand small read-currents. A 64-Kb high density array is composed of 0.25 μm^2 using 6T bit-cells [54]. Giby Samson et al, presented a dynamic word-line decoder which is fast, has reduced active and leakage power dissipation and also enables faster race-free sense timing. The energy-delay product of the dynamic decoder is 66% lower than a low-power static version in a multi-bank memory with 16 decoders. The significant decoder leakage reductions in unselected banks provide the design leverages of the predictability of dynamic circuits. The proposed dynamic decoder with active power characteristics and its improved leakage as well as race-free sense timing can enable the robust memories for highly scaled future technologies [55]. Bo Zhai et al, suggested a deep sub-threshold 6T SRAM and also fabricated it in an industrial 0.13 µm CMOS technology. The implication of variability on a specific emphasis of the detailed simulation is to explore the challenges of ultra-low-voltage memory design. They also proposed a single-ended 6T SRAM design with a gated-feedback

write-assist that remains robust deep in the sub-threshold regime. Finally, the proposed design randomly halves the size of the multiplexer design and consumes 36% less energy per access [56].

2.12.4 SRAM using Hierarchical Replica Bit-line Technique

A new 2-port 8T-SRAM with a single read bit-line (SRBL) memory cell is used for 45 nm system-on-chip (SOC). Due to threshold voltage (V_t), random variations in the access time tend to be slower as the fabrication is scaled down. The fast access time can be felt on a divided read bit-line scheme with shared local amplifiers (DBSA) without increasing area penalty. Using DBSA with the SRBL-8T cell, the simulation results show a read and write (R/W) access by the same row. The 64 kb 2 port SRAM was fabricated in the 45 nm LSTP CMOS process proposed by Satoshi Ishikura et al [57].

2.13 ARRAY STRUCTURE SRAMs

2.13.1 4x4 SRAM Design

The design and implementation of FinFET based 4 X 4 SRAM cell array by means of one bit 6T SRAM is given by Lourts Deepak A. et al. The dynamic random access memory (DRAM) and central processing unit communicate between the cache memory of SRAM. Also for low power application, the SRAM technology acts as a driving force since SRAM is portable as compared to DRAM and no refresh current is required for SRAM. Finally, all the sub blocks are integrated and 4 X 4 SRAM cell array is developed [58].

2.13.2 TSRAM Memory Array Design

Anisha Ramesh et al, designed a low power high-speed tunneling SRAM (TSRAM) memory array including pre-charge circuit blocks and sense amplifiers operating at 0.5 V and simulated at MOSIS CMOS 90 nm [59]. The memory array assigns 0.5 V as logic ‘1’ and 0 V

as logic ‘0’. To ensure the high sensing speed concurrently with low operating and standby power is designed using dual supply voltages of 0.5V, 1V and threshold voltage. The 3T memory cell with a read access time of 1 ns and write access time of 2 ns is achieved. Finally, the technology node simulated on 0.5 ns write access time and 1ns read access time is obtained with a standby power consumption of 6 X 10^{-5} mW/cell and dynamic power consumption of 1.8 X 10^{-7} mW/MHz per cell.

2.13.3 A 7T/14T Memory Array

As shown in figure 2.6, the novel dependable 7T/14T SRAM cells and their array structure avoid a half-selection problem. The memory has three modes-normal mode, high-speed mode and dependable mode in 65-nm process technology.

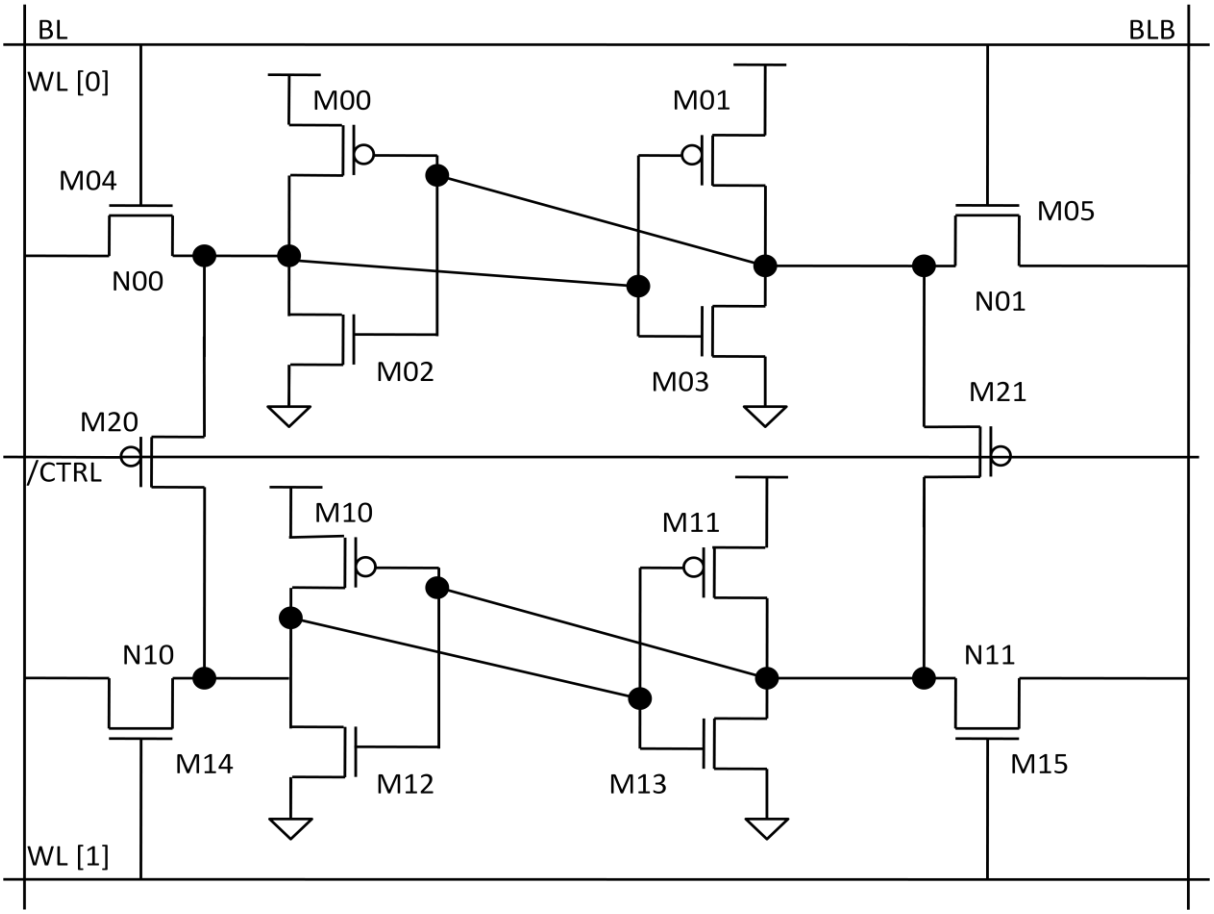


Figure 2.6-Dependable 7T/14T SRAM cells

The speed and dependability of proposed SRAM can be dynamically changed as based on the concept of "quality of bit (QOB)". Finally, the Monte-Carlo simulations are performed by Hidehiro Fujiwara et al, at minimum voltages in read and write operations which are improved by 0.20 V and 0.26 V respectively [60].

2.13.4 A 6T Dual Port memory Array

Hiep Tran describes new circuit techniques of single bit-line SRAM cell design for robust operations of five transistors. Using these techniques, an array of six transistor memory cells is operated as a dual-port SRAM. A high performance custom application in an ASIC environment, is practically embedded in both 5T SRAM and 6T dual-port cells [61].

2.14 DESIGN OF MEMORY ARRAYS USING NOVEL REVERSIBLE LOGIC GATE AND DECODER

A novel 4 X 4 MLMR gate is used to control the read/write logic of a SRAM cell. A novel 4 X 4 reversible decoder (RD) gate is implemented as a 2:4 decoder with low delay, cost and its implementation is shown in the construction of a 4 X 2 reversible SRAM array. A synchronous n-bit reversible dual-port SRAM array was designed by Matthew Morrison et al, using reversible logic structure [62].

2.15 GAPS IN PRESENT STUDY

Many types of memories exist today and new technologies and circuits are developed every year. But, for SRAM applications in advanced microprocessors, only a few have been proven to be worthy. The DRAM with its small, one-transistor cell would be a strong candidate. It has, however, not been used due to the specialized process steps needed and associated prominent increase in manufacturing cost. Planar DRAMs using a standard CMOS process, on the other hand, have not been proven viable for high-yield and high-volume production.

This, together with the high performance demands of microprocessors, has resulted in the conventional six-transistor (6T) SRAMs being the main choice for today's applications. The purpose of this thesis is to show a new approach to a fully static SRAM that can be used to replace the standard 6T. To do that, it has to have low power consumption while still maintaining the high performance of the 6T. The low-voltage operation for memories is attractive because of lower leakage power and active energy, but the challenges of SRAM design tend to increase at lower voltage. The limits of low-voltage operation for traditional six-transistor (6T) SRAM and alternative bit-cell that functions to much lower voltages. Measurements confirm that a 256-kb 65 nm SRAM test chip using the bit-cell operates into sub-threshold to below 400 mV. At this low voltage, the memory offers substantial power and energy savings at the cost of speed, making it well-suited to energy-constrained applications [18]. Aggressively scaling the supply voltage of SRAMs, greatly minimizes their active and leakage power, a dominating portion of the total power in modern ICs. Hence, energy constrained applications where performance requirements are secondary, benefit significantly from an SRAM that offers read and write functionality at the lowest possible voltage. However, bit-cells and architecture achieving very high density conventionally operate at low voltage [54]. A 2 µW, 100 kHz, 480 kb sub-threshold SRAM operating at 0.2V is demonstrated in a 130 nm CMOS process. A 10-T SRAM cells allows 1 k cells per bit-line by eliminating the data-dependent bit-line leakage. A virtual ground replica scheme is displayed for logic, "0" level tracking and optimal sensing margin in read buffers. Utilizing the strong reverse short channel effect in sub-threshold region improves cell writeability and row decoder performance due to the enhanced current driveability at a longer channel length. The sizing method leads to an equivalent write word-line voltage boost of 70 mV and a delay

improvement of 28 % in the row decoder compared to the conventional sizing scheme at 0.2 V. A bit-line writeback scheme was used to eliminate the pseudo-write problem in unselected columns [44]. Sub-threshold logic circuits are becoming increasingly popular in ultra-low-power applications where minimal power consumption is the primary constraint. Sub-threshold static CMOS logic can operate while consuming roughly an order of magnitude less power than in the normal strong-inversion region. Characteristics of MOS transistors in the sub-threshold region are significantly different from those in strong inversion region, The MOS saturation current, which is a near-linear function of the gate and threshold voltages in that region, becomes an exponential of those values in the sub-threshold region. This leads to an exponential increase in MOS current variability under process-voltage-temperature fluctuations.

However, due to parameter variations in scaled technologies, stable operation of SRAMs is critical for the success of low-voltage SRAMs that fail to achieve reliable sub-threshold operation. A different configuration SRAMs for sub-threshold operations having, single-ended 8T or 10T bit-cells, were proposed for improved stability. While these bit-cells improve SRAM stability in sub-threshold region significantly, the single-ended sensing methods suffer from reduced bit-line swing due to bit-line leakage noise [52]. The single-ended SRAM can reduce the power consumption significantly. In addition, the single-ended structure will reduce the complexity of RAM cells, thus simplifying the possible fault models. Traditionally, a half-swing pulse-mode gate family uses reduced input signal swing without sacrificing performance. These gates are well suited for decreasing the power in SRAM decoders and write circuits by reducing the signal swing on high-capacitance predecode lines, write bus lines and bit-lines. Charge recycling between positive and negative half-swing

pulses reduces the power dissipation. SRAM cell read-stability and write-ability are major concerns in nanometer CMOS technologies, due to the progressive increase in intra-die variability and Vdd scalling of the read stability N-curve metrics and comparing them with commonly used static noise margin (SNM).

CHAPTER 3

HIGH DENSITY AND LOW LEAKAGE CURRENT OF SRAM CELL

3.1 INTRODUCTION

Fast low power SRAMs have become a critical component of many VLSI chips. This is especially true in case of microprocessors where the on-chip memory cell sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. Power dissipation has become an important factor due to the increased integration, operating speeds and the explosive growth of battery operated appliances. The leakage current of the memory will be enhanced with such a capacity that more power will be consumed even in the standby mode. These on-chip memory cells are usually implemented using arrays of densely packed SRAM cells for high performance [63]. A six transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell [Akira Kotabe et al, 2005]. However, the 6T SRAM cell produces a cell size of a magnitude larger than that of a DRAM cell, which results in a low memory density. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty in meeting the growing demand for a larger memory capacity in mobile applications [64].

A novel asymmetric sizing approach is used to achieve increased read stability using a five-transistor (5T) SRAM bit-cell. Below 0.5 V, the measurements of a 32 kb 5T SRAM in a 45 nm bulk CMOS technology validate the design, showing read functionality [81]. Studies show that the power dissipated by the cell is usually a significant part of the total chip power [63]. Cell access consumes a significant fraction (30-60%) of total power dissipation in modern microprocessor. A large portion of the cell energy is dissipated in driving the bit-

lines, which are heavily loaded with multiple storage cells [65]. Clearly, the memory cells are the most attractive targets for power reduction. Besides, in cell accesses, an overwhelming majority of the write and read bits are '0', whereas, in the conventional SRAM cell one of two bit-lines must be discharged to low, regardless of written value. The power consumption in both writing '0' and '1' is generally same [63]. Also in conventional SRAM cell differential read bit-line is used during read operation and consequently, one of the bit-lines must be discharged regardless of the stored data value [65]. So there are always transitions on bit-lines in both writing '0' and reading '0'. Since in cell accesses a majority of the write and read bits are ‘0’, these cause high dynamic power consumption during read/write operation in conventional SRAM cell.

The read Static Noise Margin (SNM) is an important parameter of SRAM cell. The read SNM of cell shows its stability during read operation, further degraded by supply voltage scaling and transistor mismatch. The read operations at the low read SNM levels result in storage data destruction in SRAM cells [66]. In response to these challenges in conventional SRAM cell, our objective is to develop a high read-static-noise margin SRAM cell with five transistors to reduce the cell area size with importance to performance and power consumption. In designing of this new cell, we exploit a strong bias towards ‘0’ at the bit level exhibited by the memory value stream of ordinary programs.

3.2 READ STATIC NOISE MARGIN AND SRAM CELL CURRENT IN CONVENTIONAL SRAM CELLS

The SRAM cell current and read Static Noise Margin (SNM) are two important parameters of SRAM cell. The read SNM of cell shows the stability of cell during read operation. SRAM cell current determines the delay time of SRAM cell.

Figure 3.1 and 3.2 show the SRAM cell current in the conventional SRAM cell. Although SRAM cell current degradation simply increases bit-line (BL) delay, Read SNM degradation results in data destruction during read operations. Both Read SNM and SRAM cell current values are highly dependent on the driving capability of the access NMOS transistor: Read SNM decreases with increase in driving capability, while SRAM cell current increases, i.e., the dependence of the two is in cross coupled manner [66]. Thus, in conventional SRAM cell, the read SNM of cell and cell current cannot be adjusted separately.

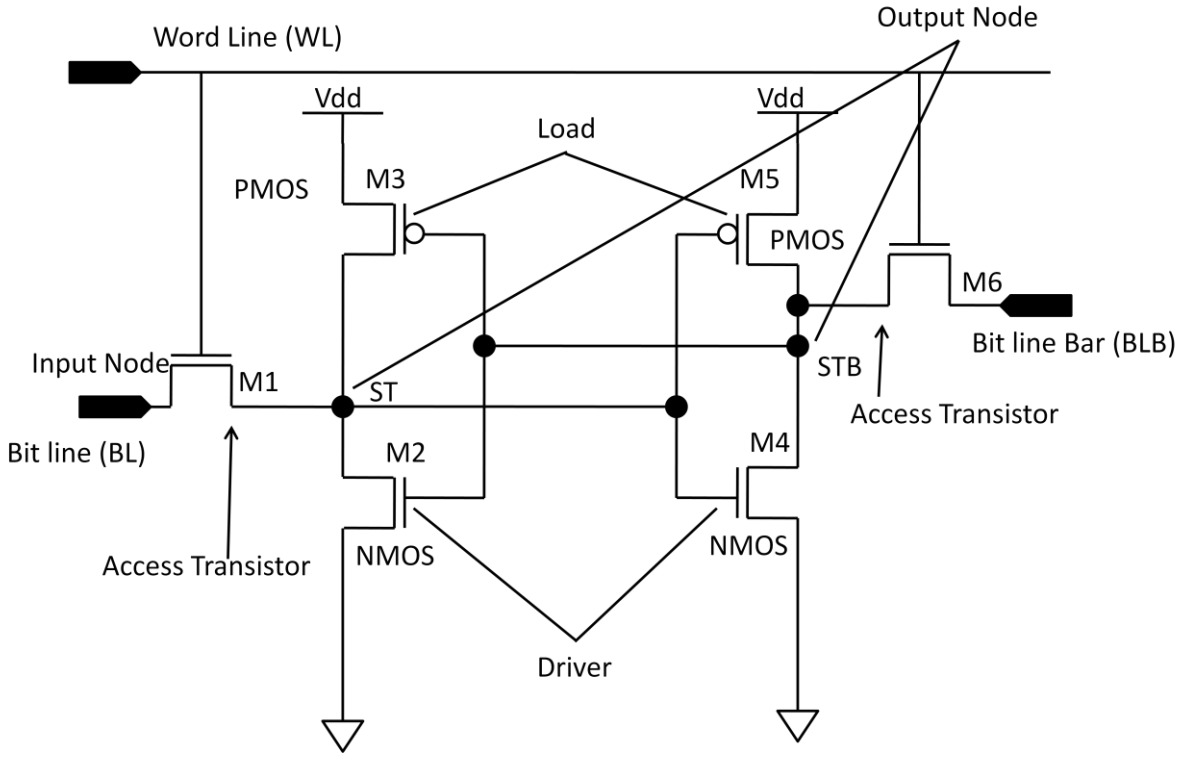


Figure 3.1-SRAM cell current in 6T SRAM cell

One strategy for solving the problem of inverse correlation between SRAM cell current and read SNM is separation of data retention element and data output element. Separation of data retention element and data output element means that there will be no correlation between Read SNM and SRAM cell current. Based on this strategy, [67] a dual-port SRAM cell is

considered. But this cell is composed of eight transistors and has 30% larger area than that of a conventional 6T SRAM cell [66]. Another strategy is loop- cutting during read operation. Based on this strategy, a read-static-noise-margin-free SRAM cell for low-VDD and high speed application is presented.

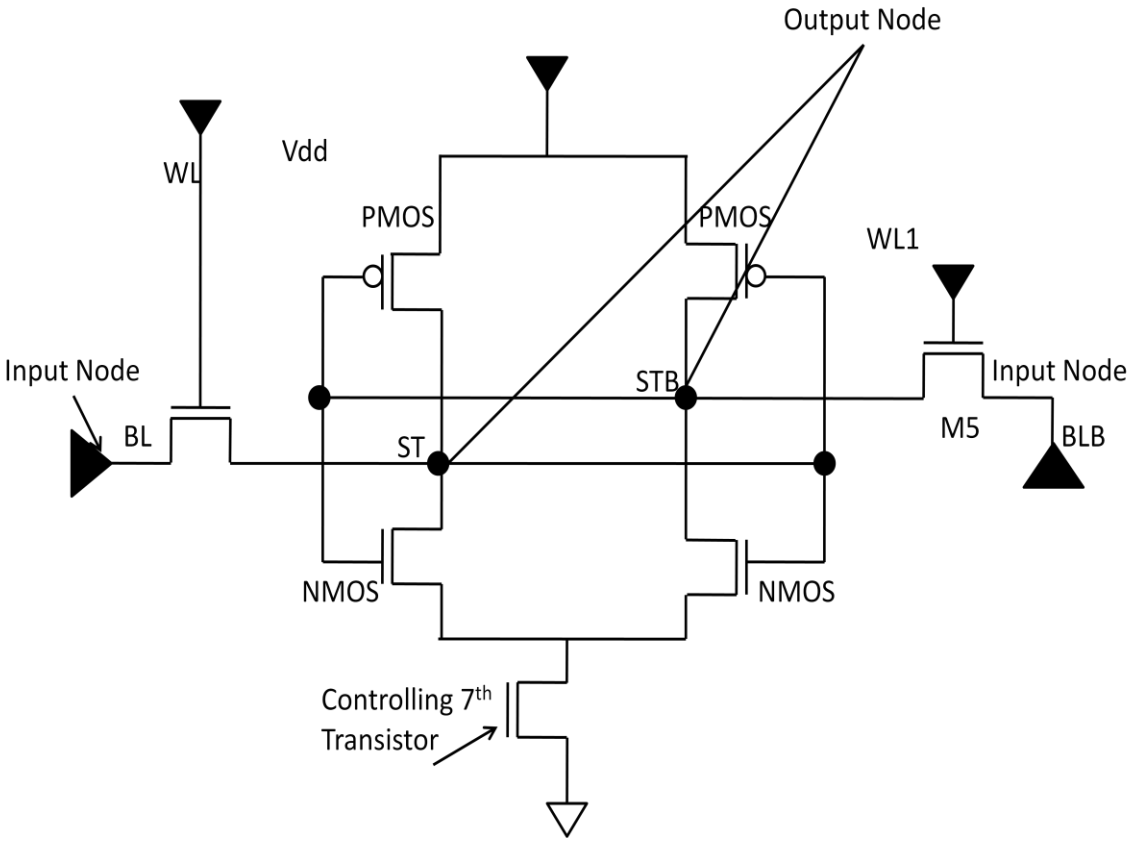


Figure 3.2-SRAM cell current in 7T SRAM cell.

To avoid inverse correlation between SRAM cell current and read SNM, I propose new five transistor SRAM cell. Our proposed cell is based on loop-cutting strategy and the observation in the ordinary programs. Most of the bits in memory cell are zeroes for both the data and instruction streams. This new cell makes it possible to achieve both low-VDD and high-speed operations with no overhead area.

3.3 CELL DESIGN CONCEPT

In the state-of-the-art Static Random Access Memory (SRAM) design, SRAM cells are always optimized to meet the desired performance and stability requirement. However, the targeted performance and stability at the initial state will be affected by the stability degradation over time and eventually lead to circuit failure. The proposed WL voltage control technique improves the degraded stability of the half-selected cell without using boosted supply voltage and increasing the power and energy consumption.

$$IDS{-}M1 > ISD{-}M\,2 + I\,gate{-}M\,4 + I\,gate{-}M3 \qquad (3.1)$$

Figure 3.3 shows the schematic of an 5T SRAM cell with Q storing data '0' and QB storing data '1'. The 5T SRAM cell consists of five transistors.

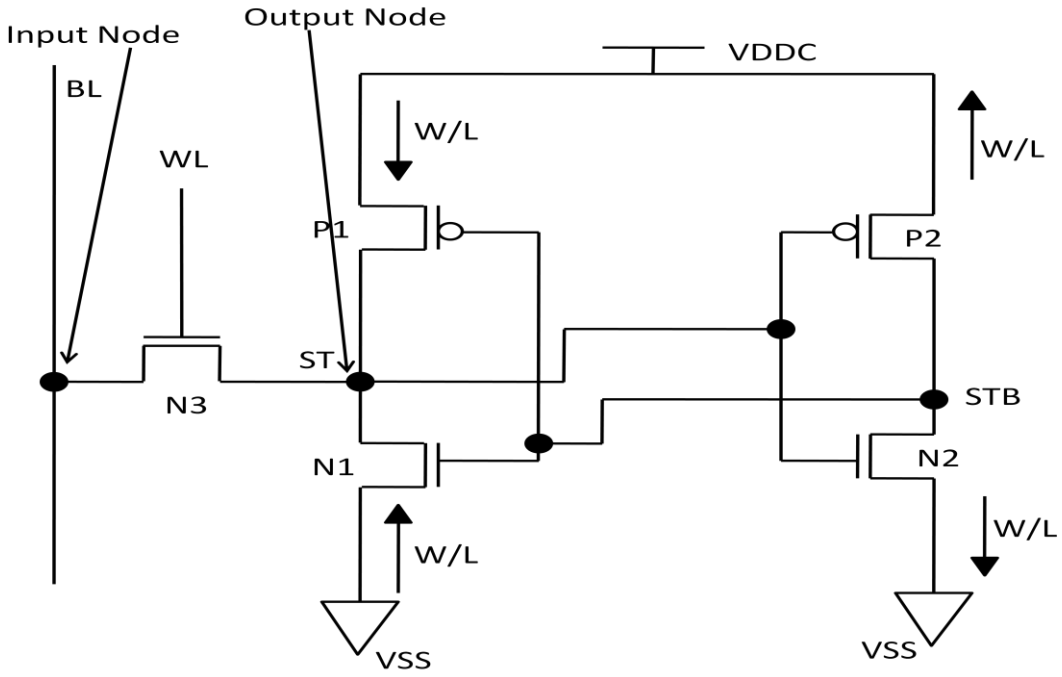


Figure 3.3- 5T SRAM cell in 45 nm technology node

3.3.1 Read Operation

I started the read operation by enabling the wordline of the selected row and pre-charging the bitline conditionally because this bitline was discharged through the access transistors and

pull down transistors. In this proposed design I have considered two critical parameters i.e. stability and delay. To limit the stability degradation caused by the disturbing current from the bit line to the cell node (storing data '0'), the access transistors are designed to be weaker than the pull down transistors [68].The read delay is determined by the series resistance formed by the access transistors and the pull-down transistors.

3.3.2 Write Operation

During a write operation, data is loaded into a bitline and the wordline of the selected row is enabled. The current strength of the access transistors should be greater than that of the pull-up transistors for pulling down the node storing '1' below the trip point of the other inverter. Once this condition occurs, the positive feedback of the cross-coupled inverters shifts the cell nodes from weak '0' and '1' to strong '0' and '1'. This completes the write operation. Write margin is defined as the highest bit line voltage that can successfully flip the stored data from storing node '0' to storing node '1'. This flipping of data is characterized by write margin. The write margin is determined by the strength ratio of the access transistors to the pull-up transistors [69].

3.3.3 Half-Select Cell Stability:-

As we know that during write operation, all the write access transistors are turned on by WL in the selected row. In unselected columns, bit line (BL) is floating at VDD. Thus, the half selected cells in the unselected columns are under an unwanted disturbance condition in 5T SRAM cell. Half Selected Static Noise Margin (HS-SNM) is the parameter which is used to define the stability of the half-selected cells due to the unwanted read-like operation. It can be defined as the highest disturbing voltage at the node storing data '0' that can flip the data during write operation [70-71]. A typical way of compensating the cell stability degradation is to raise the supply voltage but it significantly increases the power consumption and

additional circuits for boosted supply generation. In the following section, I have presented a circuit technique that can improve the stability of the half-selected SRAM cells without performance degradation and the boosting of supply voltage is not required.

3.3.3.1 Wordline Voltage Control Technique for Improving Half-Selected Cell Stability:-

I have used word line (WL) voltage control technique to improve the half selected cell stability. As discussed in the previous section, the stability of 5T SRAM is dominated by the HS-SNM. Once the degraded HS-SNM becomes negative, data flipping will occur in the half-select cells during write operation. In order to prevent this flipping, supply voltage is to be increased. But for low power applications it is not possible where energy and power consumption are the main constraints [72].

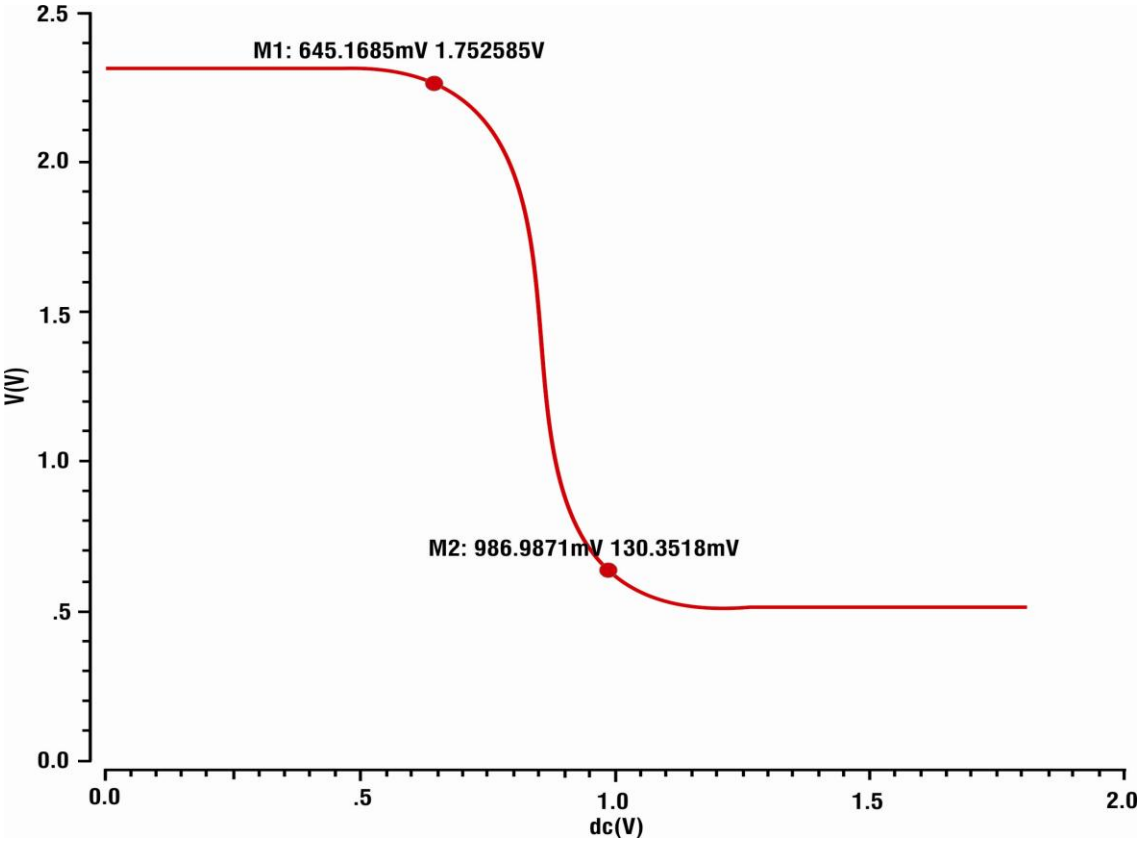


Figure 3.4- 5T SRAM cell Stability during read cycle

To address the above problem, I have reduced the WL voltage to improve HS_SNM. This is because the strength of the write access transistors is reduced with a lower WL voltage applied at its gate terminal. Hence, the disturbance current (write bit line to the cell nodes storing data '0') flowing through the write access transistors is reduced [73]. Thus, the original cell stability can be maintained by choosing a proper WL voltage level.

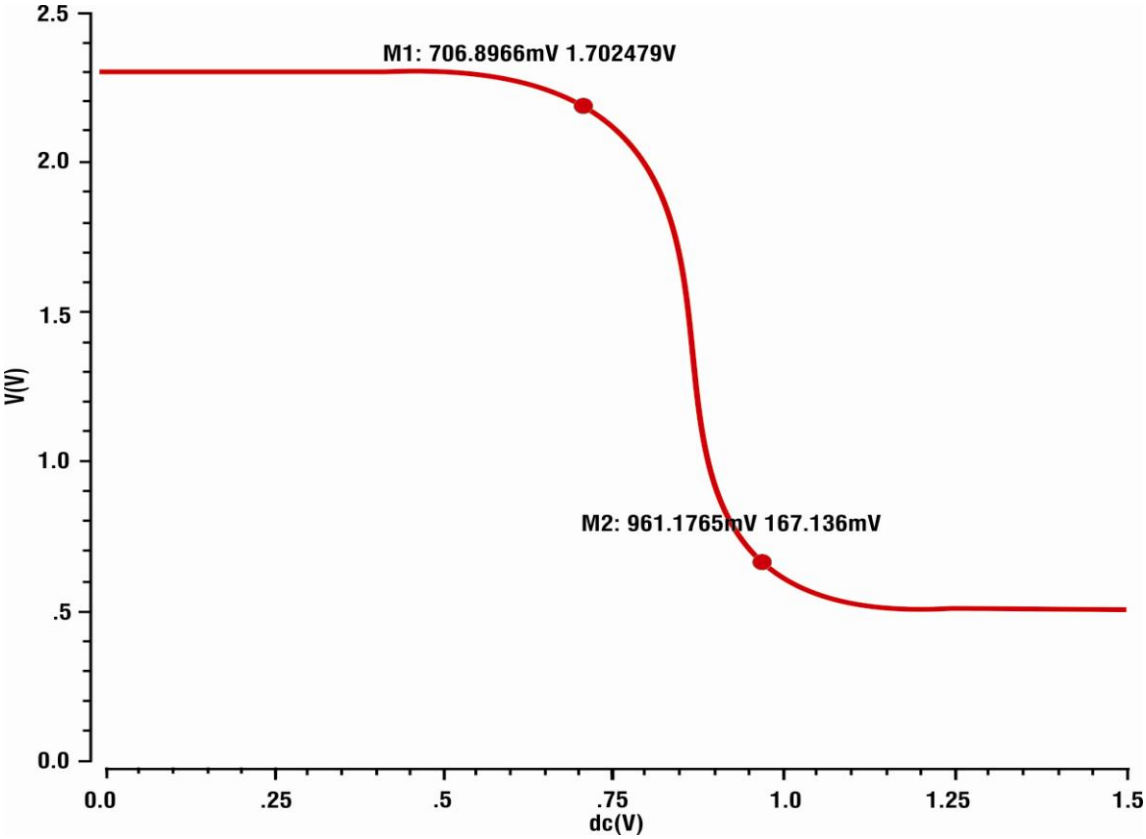


Figure 3.5- 5T SRAM cell Stability during write cycle

Fig (3.4) and fig (3.5) show the stability of the SRAM cell during read and write cycle.

Calculation for Stability of 5T SRAM cell

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

$$HSSNM = \sqrt{(NM_H{}^2) + (NM_L{}^2)}$$

$$\text{HSSNM} = \sqrt{(342)^2 + (255)^2}$$

$$\text{HSSNM} = \sqrt{(116964) + (65025)}$$

$$\text{HSSNM} = \sqrt{181989}$$

HSSNM=426 mV

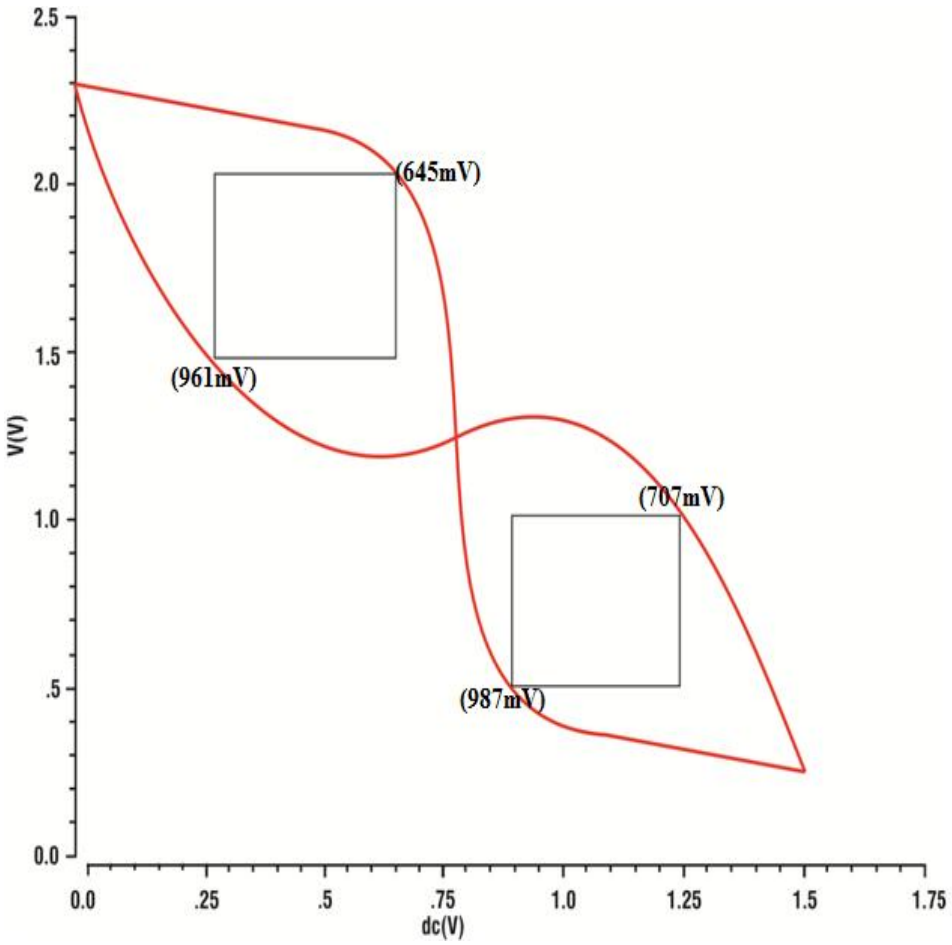


Figure 3.9- HS-SNM for 5T SRAM cell

Similarly fig (3.6) and fig (3.7) show the stability of the conventional SRAM during read and write cycle and fig (3.8) shows the comparison chart of the HS-SNM for different SRAM.

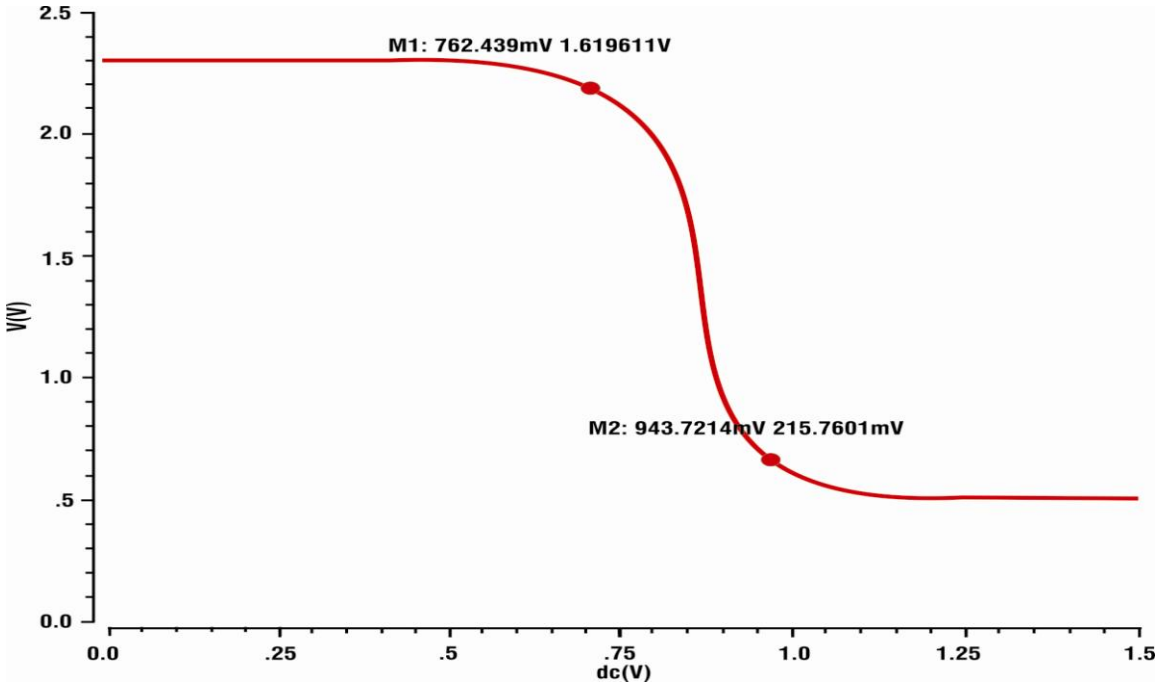


Figure 3.6- 6T SRAM cell Stability during read cycle

Fig (3.9) and fig (3.10) show the HSSNM curve for 5T and 6T SRAM cell. The result shows that a lower WL level improves HS-SNM.

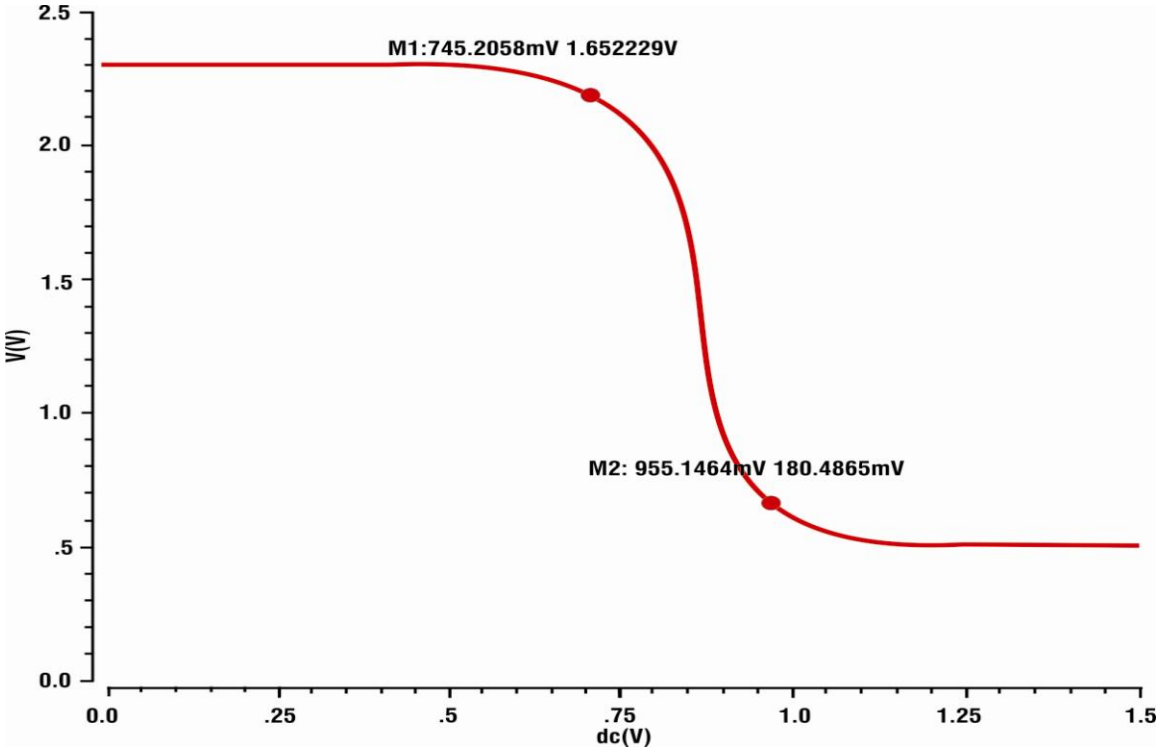


Figure 3.7- 6T SRAM cell Stability during write cycle

Calculation for Stability of 6T SRAM cell

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

$$HSSNM = \sqrt{(NM_H{}^2) + (NM_L{}^2)}$$

$$HSSNM = \sqrt{(182)^2 + (210)^2}$$

$$HSSNM = \sqrt{(33124) + (44100)}$$

$$HSSNM = \sqrt{77224}$$

HSSNM=278 mV

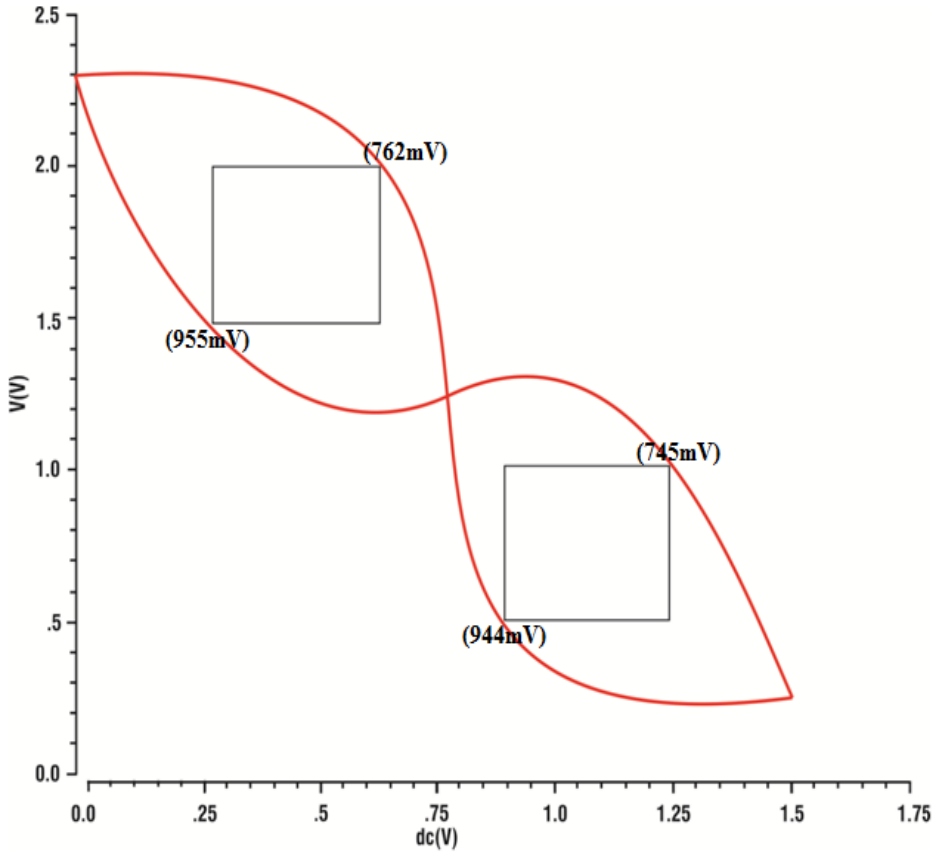


Figure 3.10- HS-SNM for 6T SRAM cell

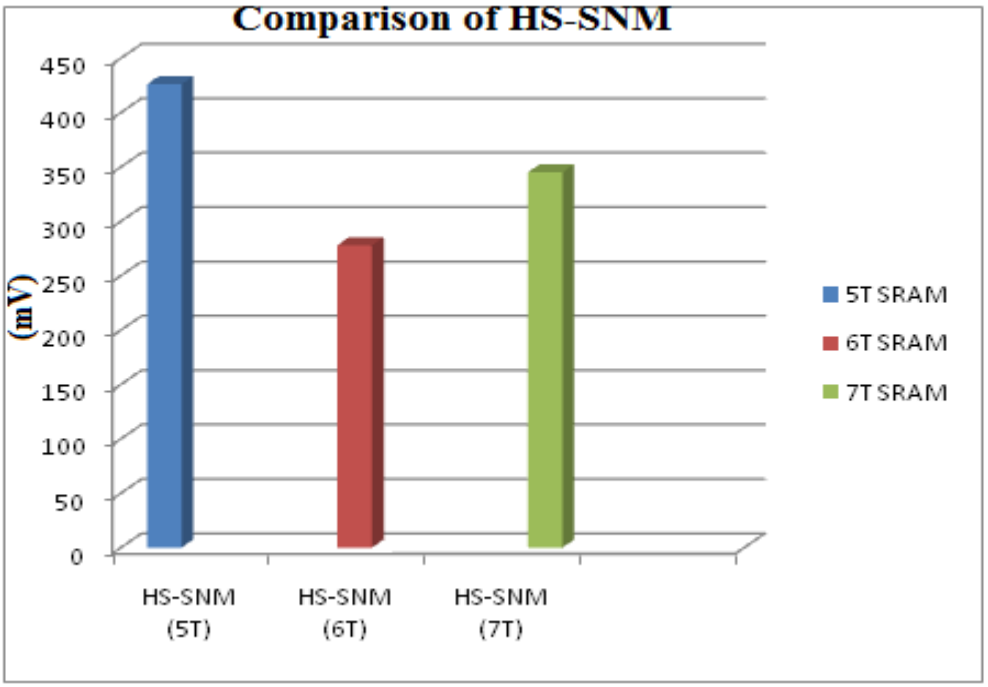


Figure 3.8- Comparison of HS-SNM

3.4 CELL AREA

As the CMOS process technology in SoC has advanced, its minimum feature size is scaled down, which enables a higher density and lower chip cost. Since a chip area of 80% or more is supposed to be occupied by the memories like large-capacity SRAMs for storing data, small area SRAMs are required in terms of chip cost and yielder.

Figure 3.11 shows information about the layout analysis at 45 nm technology. Consideration of making this layout depends on the area which is covered by the components of different orientations or different parameters like nmos, pmos and the layers.

In figure 3.11 seven transistors are used. Two transistors are PMOS and remaining five transistors are NMOS. Blue colour strip shows the metal 1 layer. With the help of layout, we can calculate the area of the cell. We can see in figure 3.11 that the length and width of the

cell is 2.1 µm. So the area of the cell is 2.1 * 2.1 μm^2. This area is very less as compared to 180 nm technology.

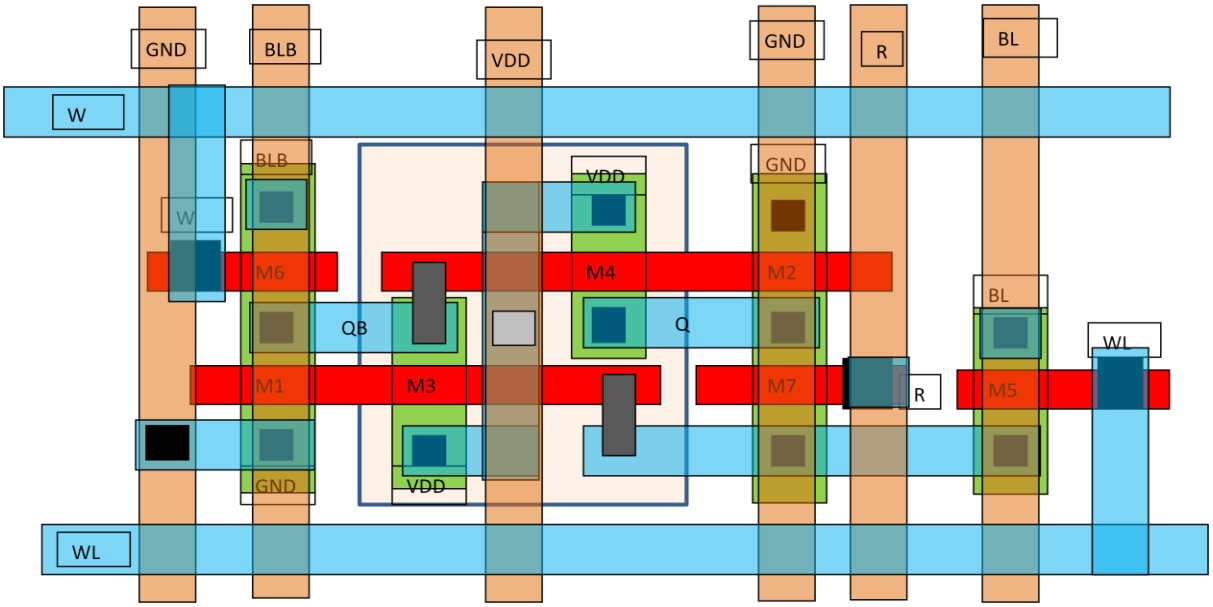


Figure 3.11-Layout of 7T SRAM cell using 45 nm technology

Figure 3.12 shows the layout of 6 transistors SRAM cell in 45 nm technology. Upper two transistors are PMOS and remaining four transistors are NMOS. The area of the 6 transistors SRAM cell is less as compared to 7 transistors SRAM cell.

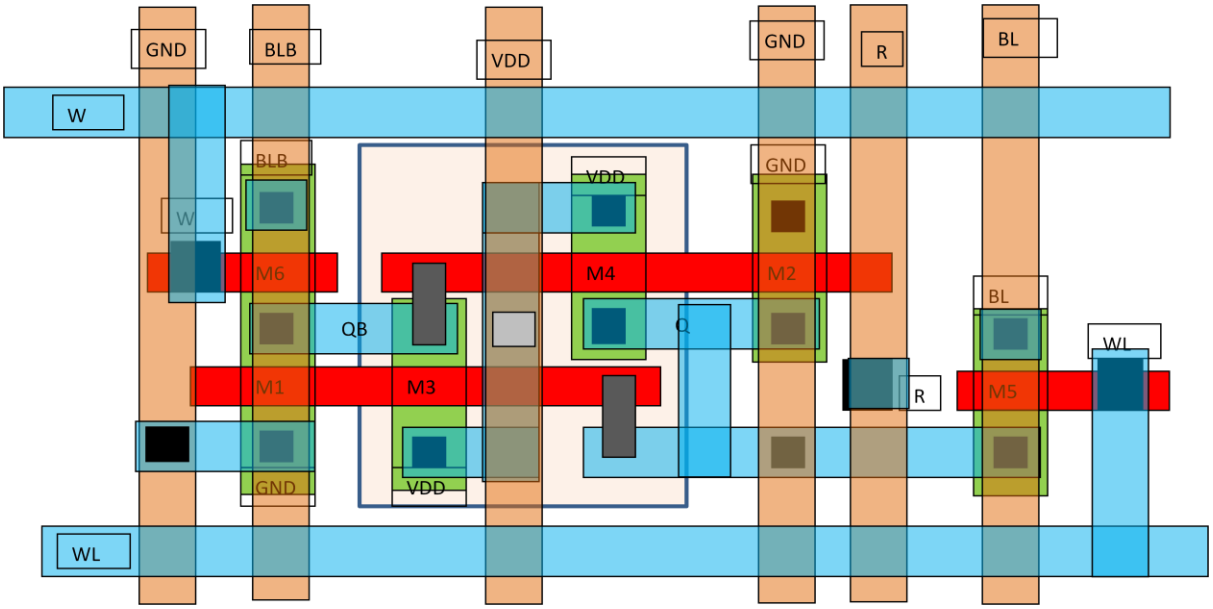


Figure 3.12 - Layout of 6T SRAM cell using 45 nm Technology

Drain and source connections are done with the help of metal 1 layer. Gate connections are made with the help of poly layer. All input pins are connected to the gate terminal with the help of via. Supply and ground strips are made with the help of metal 1 layer. The length and width of the 6 transistors SRAM cell is 1.8 µm and 1.91 µm. So the area of the cell is 1.8 * 1.91 μm^2.

Figure 3.13 displays the layout of 5 transistors SRAM cell using 45 nm technology. In this cell, upper three transistors are PMOS and two transistors are NMOS. Upper blue strip is supply strip and bottom blue strip is ground strip. Drain and source connections are made with the help of metal 1 layer. Input pins are connected to gate terminal with the help of via. The length and width of the cell is 1.755 µm and 1.535 µm respectively. So the area of the cell is 1.755 * 1.535 μm^2.

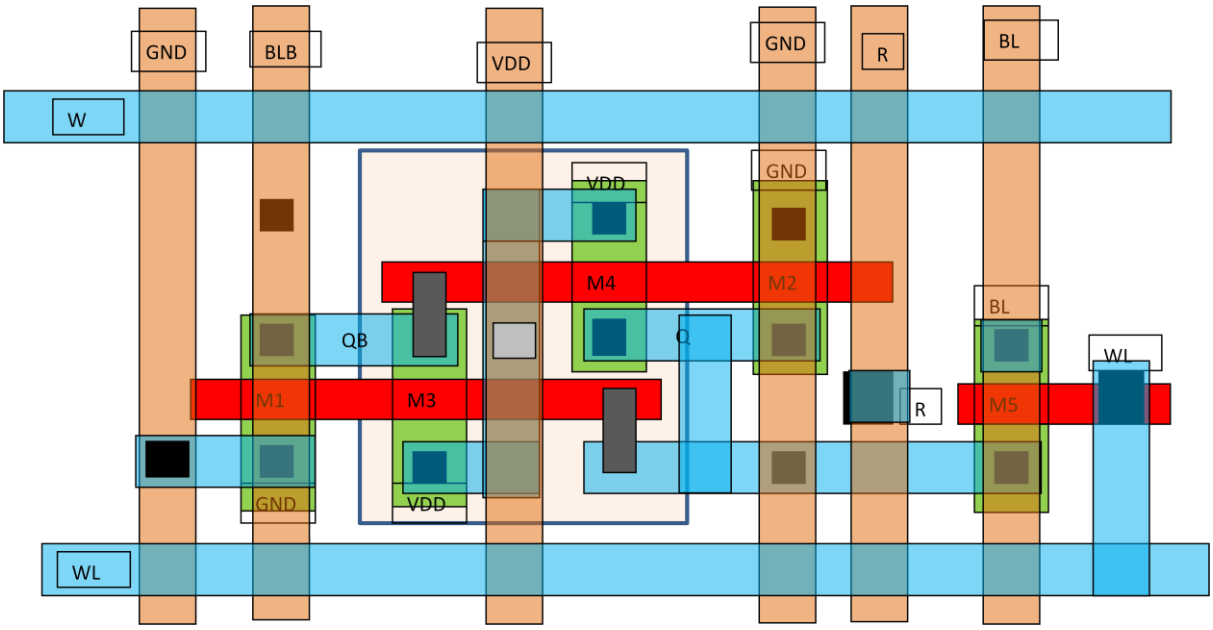


Figure 3.13-Layout of 5T SRAM cell using 45 nm technology

After the completion of the different transistors in different technologies, following results are shown in table 3.1.

S.No.	Parameters	7T	6T	5T
1	Read cycle time	84.45ps	34.39ps	22.87ps
2	Write cycle time	303.19ps	74.20ps	46.28ps
3	Leakage Current	22.63nA	9.20nA	3.60nA
4	Power during read ’0’	61.36nW	22.47nW	13.23nW
5	Power during read ’1’	15.84nW	6.44nW	2.52nW
6	Power during write ’0’	5.98nW	0.1603nW	6.87nW
7	Power during write ’1’	39.66nW	65.87nW	3.85nW

Table-3.1Comparison among 5T, 6T and 7T cell area

3.5 LEAKAGE CURRENT

In one state, novel 5T SRAM cell must retain its data using the leakage current of the access transistor (when ‘0’ is stored) and in the other state the 5T SRAM cell must retain its data using positive feedback (when ‘1’ is stored). Thus, in idle mode when '1' is stored in the cell, there is a positive feedback and transistors M2, M3 and feedback cutting (M5) transistors are turned ON and access transistors are maintained in sub-threshold region. In this state, there is a path from supply voltage to ground which results in power dissipation.

Leakage current will be calculated as per the following equation (2) at the time when transistor is in OFF condition [80]

$$I_{sub} = \mu_0 C_{ox} \frac{W}{L_{eff}} V_T^2 e^{1.8} \exp\left(\frac{V_{gs}-V_{th}}{nV_T}\right).\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right) \qquad (3.2)$$

Figure 3.8 shows this path when '1' is stored in cell. In ordinary programs, most of the bits in memory cell are zeroes for both data and instruction streams. It has been shown that this behaviour persists for a variety of programs under different assumptions about the memory cell size, organization and instruction set architectures [74]. Thus, most of the bit values residing in data and instruction memory cell are zero. Based on these observations, we simulated an average leakage current in idle mode of 5T SRAM cell and conventional 6T SRAM cell by using 45 nm technology.

3.5.1 Diffusion Leakage

Although the diffusion leakage current ($I_{diffusion}$) does not pose a significant technical challenge or the ULP technology leakage goals, some experimental optimization was required to reach such goals. Reverse-Bias Diffusion Leakage (RBDL) is a function of defected population within the depletion region and thus the local stresses arise from the sources such as STI (Shallow Trench Isolation) processing parameters and the silicide processing [79]. This leakage can be characterized as

$$I_{diffusion} = A_2 \exp (E_a / K_T) \quad (3.3)$$

Where, E_a is roughly equal to $E_g / 2$ in the typical junction environment and A is defined as

$$A_2 = T^{3/2} \times V^{1/2} \quad (3.4)$$

The diffusion leakage was minimized by optimizing the source/drain energy, so that the junction depth becomes deep enough to avoid the silicide defects. The relationship between the deep p-well retrograde implant and the area diffusion leakage leads to a reduction of the deep retrograde implant dose for the ULP technology.

$$J_{diffusion} = qD_n \frac{n_i^2}{N_A L_n} [\exp(\frac{qV}{kT})\text{-}1] \quad (3.5)$$

Where q is the electron charge, D_n is the diffusion constant of electrons, n_i is the intrinsic carrier density, N_A is the acceptor density, and L_n is the diffusion length of electrons.

3.5.2 Process of calculating leakage current

Leakage current is calculated from the transistor which is in OFF condition at the time of operation. In the leakage current calculation, there are four operations performed which are described below:-

a) For writing '1' in STB node

For writing '1' in STB node, transistor M3 will be in OFF condition so we will take the leakage current from the node of M3 transistor,

Leakage current at STB node for writing '1' = leakage at M3 transistor = -9.824 nA.

b) For writing '0' in STB node

For writing '0' in STB node, transistor M4 will be in OFF condition so we will take leakage current from the node of M4 transistor,

Leakage current at STB node for writing '0' = leakage at M3 transistor = 5.51 nA.

c) For writing 1 in ST node

For writing '1' in ST node, transistor M4 will be in OFF condition so we will take leakage current from the node of M4 transistor,

Leakage current at STB node for writing '1' = leakage at M3 transistor = 18.9 nA.

d) For writing '0' in ST node

For writing '0' in ST node, transistor M2 will be in OFF condition so we will take leakage current from the node of M2 transistor,

Leakage current at ST node for writing '0' = leakage at M3 transistor = 3.60 nA.

Comparison of 5T, 6T and 7T for leakage current:-

S. No.	Parameter	Leakage current in 5T		Leakage current in 6T		Leakage Current in 7T		Better Performance
		At 25°C	At 35 °C	At 25°C	At 35°C	At 25°C	At 35°C	
1	For writing '1' in STB node	-9.824 nA	-19.648 nA	-0.229 nA	-0.458 nA	-8.546 nA	-16.84 nA	6T
2	For writing '0' in STB node	5.51 nA	11.02 nA	94.11 nA	188.22 nA	56.67 nA	178.67 nA	5T
3	For writing '1' in ST node	18.90 nA	37.80 nA	-32.10 nA	-64.20 nA	87.67 nA	145.30 nA	5T
4	For writing '0' in ST node	3.60 nA	7.20 nA	9.20 nA	18.40 nA	22.63 nA	34.11 nA	5T

Table-3.2: Comparison among 5T, 6T and 7T leakage current

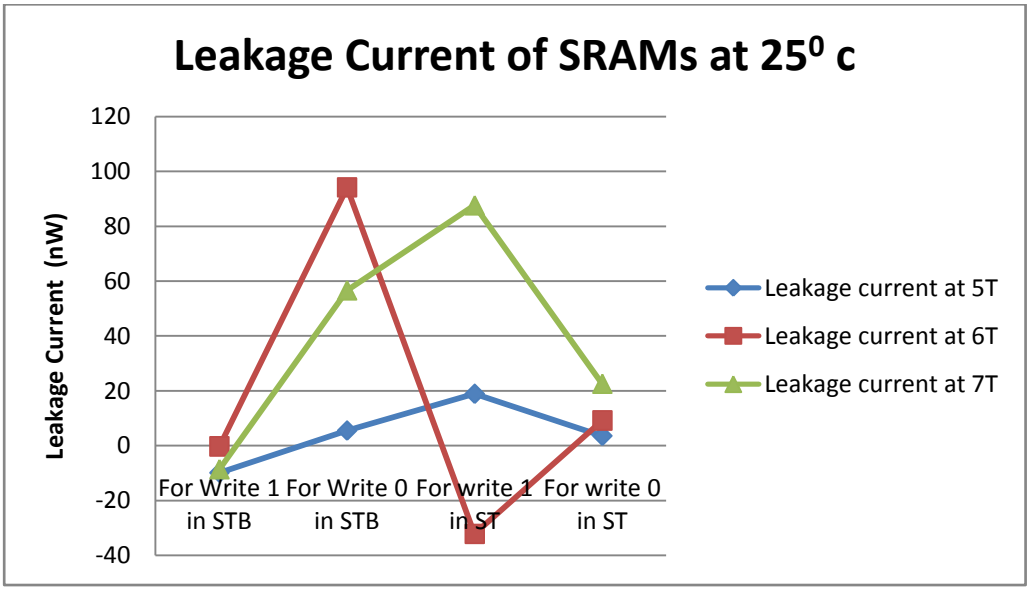


Figure 3.14 Leakage current of SRAMs at 25°c

Comparison of 5T, 6T and 7T for gate leakage current:-

Table 3.2 and 3.3 shows that cell leakage of 5T SRAM in write 0 STB node, write '1' ST node and write '0' ST node is less than the 6T SRAM cell. It shows that 5T is better than 6T to write the data in SRAM cell.

S. No.	Parameter	Gate Leakage current in 5T		Gate Leakage current in 6T		Gate Leakage current in 7T		Better Performance
		At 25°C	At 35 °C	At 25°C	At 35°C	At 25°C	At 35°C	
1	For write '1' in STB node	1.778 nA	2.4672 nA	90.76 pA	8.084 pA	476 fA	4.34 pA	6T
2	For write '0' in STB node	5.361 nA	1.947 nA	27.4 pa	33.6 pA	4.33 pA	178.67 nA	5T
3	For write '1' in ST node	3.1584 nA	2.2938 nA	6.856 pA	8.916 pA	1.48 pA	37.3 nA	5T
4	For write '0' in ST node	1.5895 nA	1.9345 nA	251 pA	25.6 pA	3.581 pA	3.589 pA	5T

Table-3.3: Comparison among 5T, 6T and 7T Gate leakage current

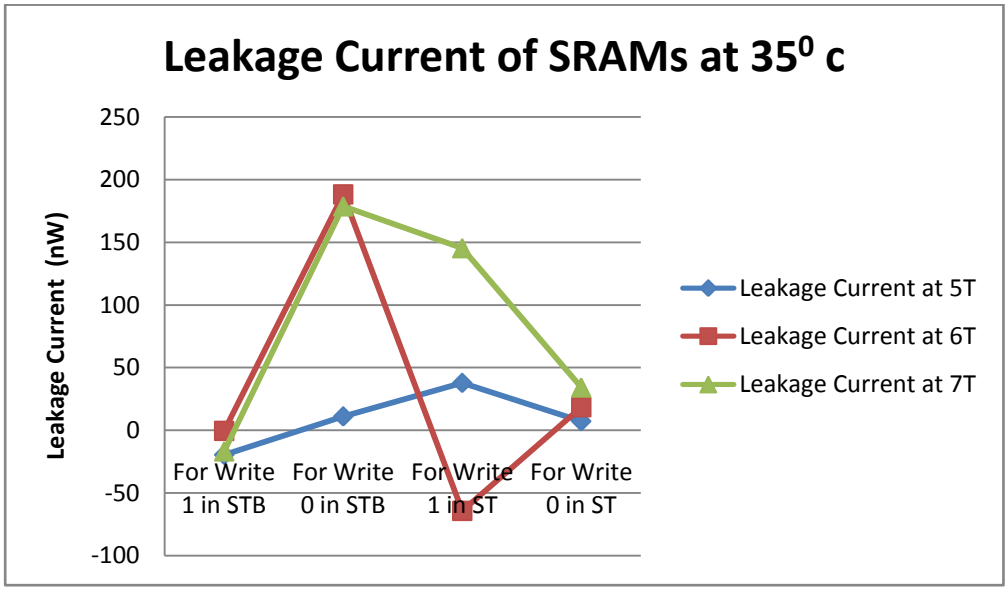


Figure 3.15-leakage current of SRAMs at 35°c

3.6 CELL DELAY

The propagation delays τ_{PHL} and τ_{PLH}, determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively [78]. Going by the definition, τ_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\ \%}$ transition of the rising output voltage. To simplify the analysis and the derivation of delay expressions, the input voltage waveform is usually assumed to be an ideal step pulse with zero rise and fall times. Under this assumption, τ_{PHL} becomes the time required for the output voltage to fall from V_{OH} to the V_{150s} level and τ_{PLH} becomes the time required for the output voltage to rise from V_{OL} to the $V_{50\%}$ level. The voltage point $V_{50\%}$ is defined as follows:-

$$V_{50\%} = V_{OL} + ½ (V_{OH} - V_{OL}) = ½ (V_{OH} + V_{OL}) \qquad (3.6)$$

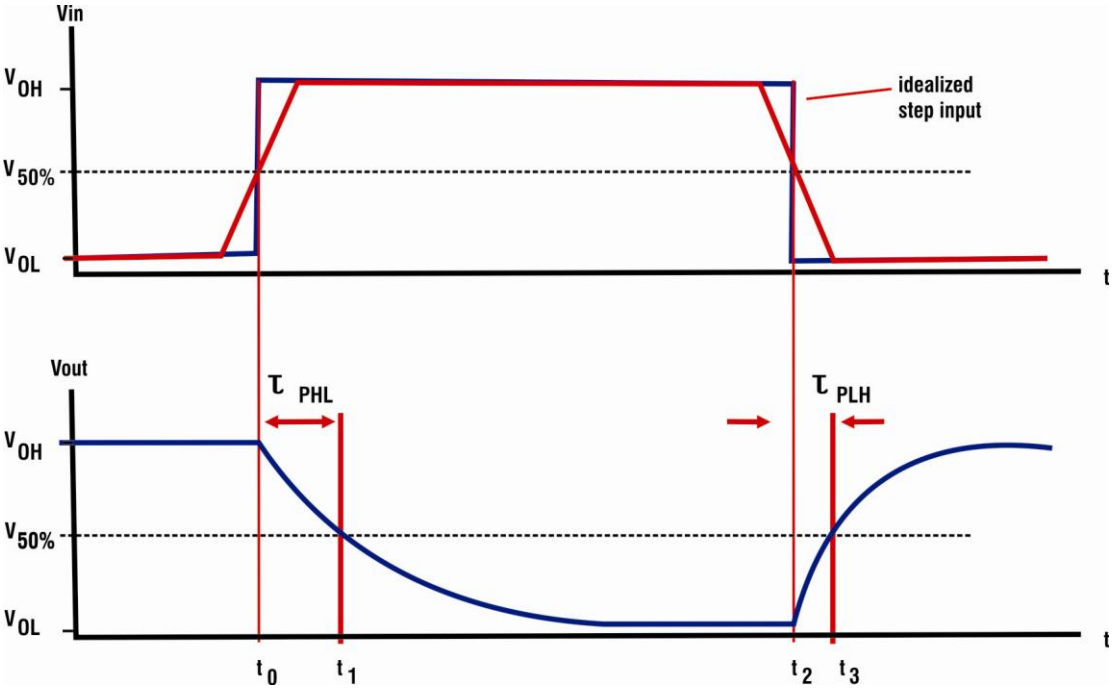


Figure 3.16-Input and output voltage waveforms of a typical inverter

Thus, the propagation delay τ_{PHL} and τ_{PLH} are found to be,

$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

The average propagation delay τ_p of the inverter characterizes the average time required for the input signal to propagate through the inverter as-

$$\tau_p = \frac{\tau_{PHL}+\tau_{PLH}}{2} \quad (3.7)$$

Cell delay will be calculated directly using the cadence virtuoso tool. By using the calculator after the simulation of the circuit like 5T SRAM cell, we can calculate the delay for both ST node and STB node. The delay will be calculated [77], by using the basic idea which is shown in figure 3.16.

There is a speed penalty for a Vdd reduction, with the delays drastically increasing as VDD approaches the threshold voltages of the devices. Even though the exact analysis of the delay is quite complex, if the nonlinear characteristic of a CMOS gate is taken into account, it is found that a first simple derivation adequately predicts the experimentally determined dependence and is given by

$$T_d = \frac{C_L \times V_{dd}}{I} = \frac{C_L \times V_{dd}}{\mu C_{ox}(W/L)(V_{dd}-V_t)^2} \quad (3.8)$$

Delay of the cell depends on the consumption of time between the cells from input (BL) to output [76]. The table 3.4 shows the comparison of the cell delay between 5T, 6T & 7T.

S. No.	Parameters	Delay of 5T	Delay of 6T	Delay of 7T	Better Performance
1	Delay at STB	14.24 ps	47.72 ps	55.21 ps	5T
2	Delay at ST	2.453 ns	0.839 ns	1.491 ns	6T

Table -3.4: Comparison among 5T, 6T and 7T cell delay

This table shows that 5T cell delay in STB node is less than 6T cell delay in STB node. It means 5T is better than 6T because the output is taken from the STB node and the cell delay for 5T in STB node is less than that of 6T in STB node. Information about the comparison between 5T, 6T & 7T SRAM cell delay is graphically represented in figure 3.17.

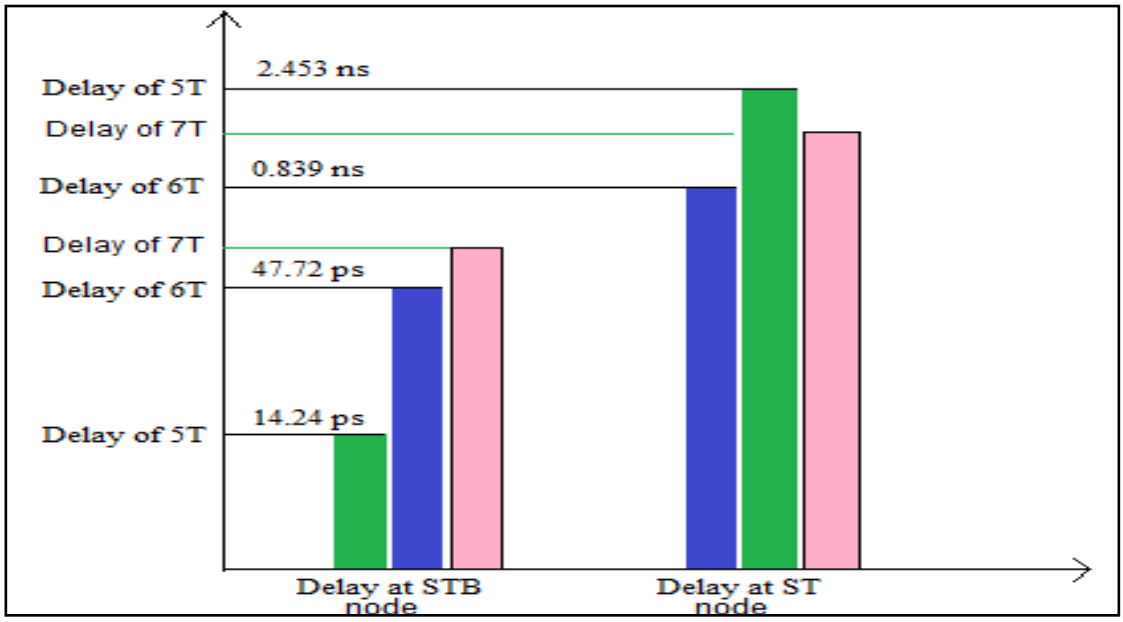


Figure 3.17- Delay Comparison among 5T, 6T and 7T

3.7 POWER CONSUMPTION

Power consumption of the SRAM memory cell depends upon the power consumption of the transistors used for the operation [75]. Assuming the periodic input and output waveforms, the average power dissipated by any device over a unit period can be found as follows:-

$$P_{av} = [(1/T) \int_0^T I\, dt] \times V \qquad (3.9)$$

By using this phenomenon, we can calculate power consumption during four operations for the 5T SRAM cell.

a) Power consumed at STB node for writing '1'

For writing '1' in STB node, M1-M4-M5 transistors are turned ON and by consuming power which is calculated by multiplying voltage and current of the respective transistors.

$P_{consumed\text{-}STB\text{-}writing\ 1} = P_{M1} + P_{M4} + P_{M5} = 9.8$ nW.

b) Power consumed at STB node for writing '0'

For writing '0' in STB node, M1-M3 transistors are turned ON and by consuming power which is calculated by multiplying voltage and current of the respective transistors.

$P_{consumed\text{-}STB\text{-}writing\ 1} = P_{M1} + P_{M3} = 67.3$ nW.

c) Power consumed at ST node for writing '1'

For writing '0' in STB node, M2-M3 transistors are turned ON and by consuming power which is calculated by multiplying voltage and current of the respective transistors.

$P_{consumed\text{-}STB\text{-}writing\ 1} = P_{M2} + P_{M3} = 85.01$ nW.

d) Power consumed at ST node for writing '0'

For writing 1 in STB node, M1-M4-M5 transistors are turned ON and by consuming power which is calculated by multiplying voltage and current of the respective transistors.

$P_{consumed\text{-}STB\text{-}writing\ 1} = P_{M1} + P_{M4} + P_{M5} = 9.8$ nW.

Power consumption of the cell is shown in the table 3.5.

S. No.	Parameters	Power consumption of 5T	Power consumption of 6T	Power consumption of 7T
1	Power consumed at STB node for writing '1'	9.8 nW	0.011 pW	11.24 nW
2	Power consumed at STB node for writing '0'	67.3 nW	30 pW	80.61 nW
3	Power consumed at ST node for writing '1'	85.01 nW	0.003 pW	82.44 nW
4	Power consumed at ST node for writing '0'	9.8 nW	28 pW	22.07 nW

Table-3.5: Comparison among 5T, 6T and 7T power consumption

3.8 SUMMARY OF THE CHAPTER

With the aim of achieving high density, half-selected cell stability and low leakage current, the SRAM memory cell has been developed using 5T, 6T and 7T circuit topologies. The half-selected cell stability of 5T, 6T and 7T SRAM cell is 426 mV, 278 mV and 345 mV respectively. The key observation in these designs is that the cell leakage current is determined by the node whose transistor is 'off'. With the same design rules, proposed cell area is 21.66% smaller than 6T SRAM cell with 28.57% speed improvement. The proposed cell has been simulated at 45 nm technology and its robustness is calculated during the correct read/write operations, and also the delay of a new cell is 70.15% smaller than a six-transistor SRAM cell. The leakage current during memory cell access of a new cell is 72.10%, lesser than 6T SRAM cell and with every 10°C rise in temperature, leakage current gets double in its value.

CHAPTER 4
LEAKAGE CURRENT REDUCTION TECHNIQUES FOR 7T SRAM CELL

4.1 INTRODUCTION

In this chapter, the impact of gate leakage on 7T SRAM is described and the three techniques for reducing the gate leakage currents and sub-threshold leakage currents are examined. In first technique, the supply voltage is decreased. In the second, the voltage at the ground node is increased. While in the third, the effective voltages across SRAM cell Vd which is 0.348V and Vs which is 0.234V, are observed. In all the techniques, the effective voltage across SRAM cell is decreased in stand-by mode, using a dynamic self controllable voltage level (SVL) switch. Simulation results based on cadence tool at 45 nm technology show that the technique in which supply voltage level is reduced, is more efficient in reducing gate leakage than the one in which ground node voltage is increased. Results obtained show that 437 fA reduction in the leakage currents of 7T SRAM can be achieved.

4.2 LOW POWER TECHNIQUES

Design techniques for low power circuits, for example, to use in battery-driven mobile phones, are not only needed for logic circuits (such as extremely fast adders and multipliers) but also for storage circuits (such as flip-flops, register files and memories). An integrated static random access memory (SRAM) compiler is proposed to reduce both leakage and dynamic power at circuit and architectural level [96]. There are several techniques for reducing the standby power Pst [82]. One is by using a multi-threshold-voltage CMOS (MTCMOS). This technique reduces Pst by disconnecting the power supply through the use of pMOSFET switches with higher threshold voltage Vthp and nMOSFET switches with

higher threshold Vthn voltage. However, it also has serious drawbacks, such as, the need of additional fabrication processes for higher Vthp and higher Vthn and the fact that storage circuits based on this technique cannot retain data. To overcome this drawback, a self-controllable voltage level switch is used which can significantly decrease the stand-by power, while maintaining the high speed performance [89]. There is a significant increase in sub-threshold leakage due to its exponential relation with the threshold voltage and gate leakage due to the reduction in gate-oxide thickness [92]. The sub-threshold leakage current exponentially depends on the gate-to-source voltage of a MOSFET [13]. When the SRAM circuit is in active mode, the SVL switch generates maximum supply voltage (e.g. Vd which is 0.7V) and the minimum ground level voltage (Vs which is 0V) to it through switches that are turned on, so that SRAM circuit can operate quickly. On the other hand, when the SRAM circuit is in stand-by mode, it generates slightly lower supply voltage and relatively higher ground level voltage. The present work describes analysis which shows the use of SVL switch for reducing the supply voltage to yield the maximum reduction in leakage currents especially when the pre-charge transistors are put in cut-off state during the stand-by mode. An SVL switch can be used either to reduce the supply voltage to the SRAM cell or to increase the potential of ground level and the two approaches can be combined as well. Although, a technique similar to SVL can be used for raising the ground potential which has already been observed to yield the significant reduction in gate leakage current [85]. A detailed comparison of these alternative approaches has not yet been undertaken. An analysis of leakage currents in 7T SRAM cell has been carried out and the techniques for suppressing it, are compared. It reduces the sub-threshold leakage current by increasing the ground level during the idle (inactive) mode [95]. Out of several techniques which have been proposed to

reduce the sub-threshold leakage current in SRAM cells [86]-[88], the use of a self-controllable switch (SVL) [89] is significant which allows full supply voltage to be applied in active mode and reduces the supply voltage in stand-by mode. This appears to be particularly promising for reducing gate leakage currents as well. A number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-VDD scheme [87], Dual-V_t SRAM, etc. As a result, even though the supply voltage has also been reduced with new generations of technology, the magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than sub-threshold leakage current for the future CMOS devices [88]. The SRAM unstability and the leakage dissipation in scaled-down technologies present a novel design flow for simultaneous power minimization, performance maximization, process variation and tolerance optimization of nano-CMOS circuits [91]. The 7T SRAM cell consumes higher hold power due to its extra cell area, required for its functionality constraint [94].

In this chapter, a 7T SRAM cell in 45 nm technology, whose channel length is 45 nm and width is 120nm has been proposed. The 7T SRAM cell consists of seven transistors in which two inverters (M1, M3 and M2 and M4) are connected in cross-coupled manner. Transistors M5 and M6 are write-access transistors and transistor M7 is the read-access transistor. This is designed in 45 nm technology because it occupies less chip area density as compared to other nanometer technologies.

4.3 READ AND WRITE OPERATION OF CIRCUIT

The proposed write concept depends on cutting off the feedback connection between the two inverters, inv1 and inv2, before the write operation. The connecting and disconnecting of feedback is performed by an extra NMOS transistor M7, as shown in Figure 4.1, and the cell

only depends upon the BLB (Bit-line bar) to perform a write operation. The write operation starts by turning M7 ‘off’ to cut off the feedback connection. BLB carries the complement of the input data, M5 is turned ‘on’, and M6 is kept ‘off’. The SRAM cell looks like two cascaded inverters, inv2 followed by inv1. BLB transfers the complement of input data to the input of another inverter which drives inv2, M2 and M4 to develop output, cell data which drives inv1 and develops QB. The proposed cell can be applicable to the more advanced CMOS technology provided that each process and the device parameter is scaled to the same degree [93]. Lower supply voltages due to increased device variations have enforced the usage of write-assist circuits in static random access memory (SRAMs) in the nano-complementary metal oxide semiconductor (CMOS) regime [22].

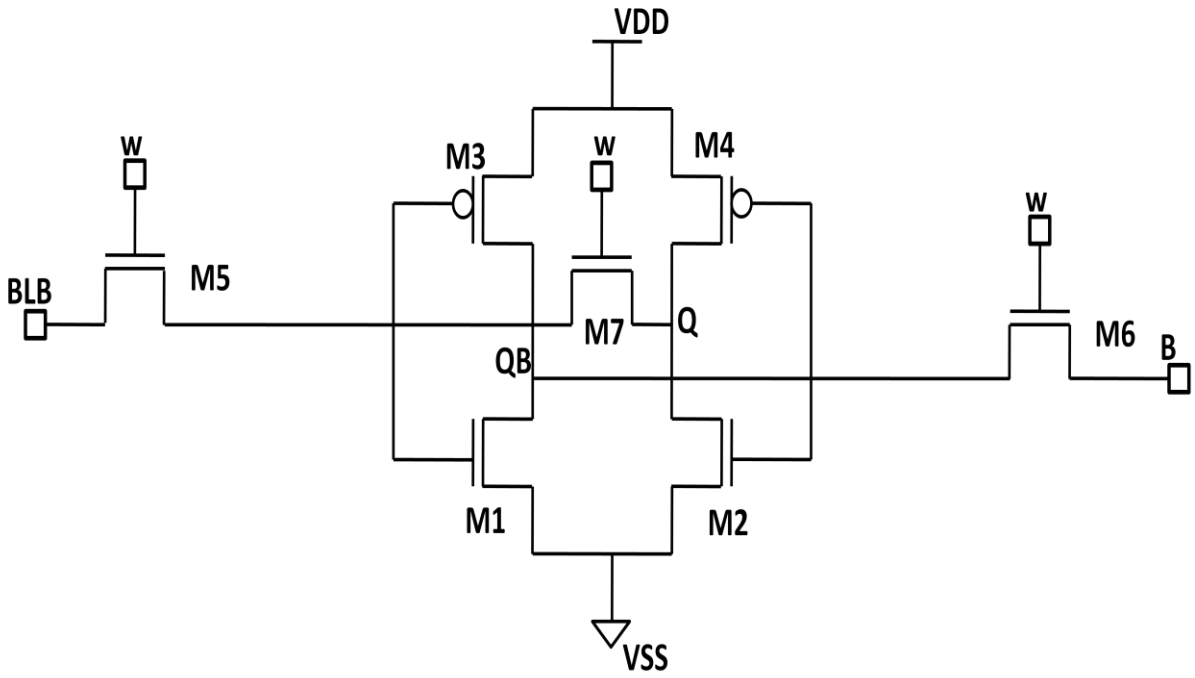


Figure 4.1-Schematic of Conventional 7T SRAM Cell

Figure 4.1 is the schematic of 7T SRAM cell. In this, four transistors (M1, M2, M3 and M4) make two inverters which are connected in cross-coupled manner. Transistors M5 and M6 are

write access transistors and transistor M7 is read access transistor. The layout of conventional 7 transistor SRAM using cadence tool is shown in figure 4.2, which is designed in virtuoso layout editor tool.

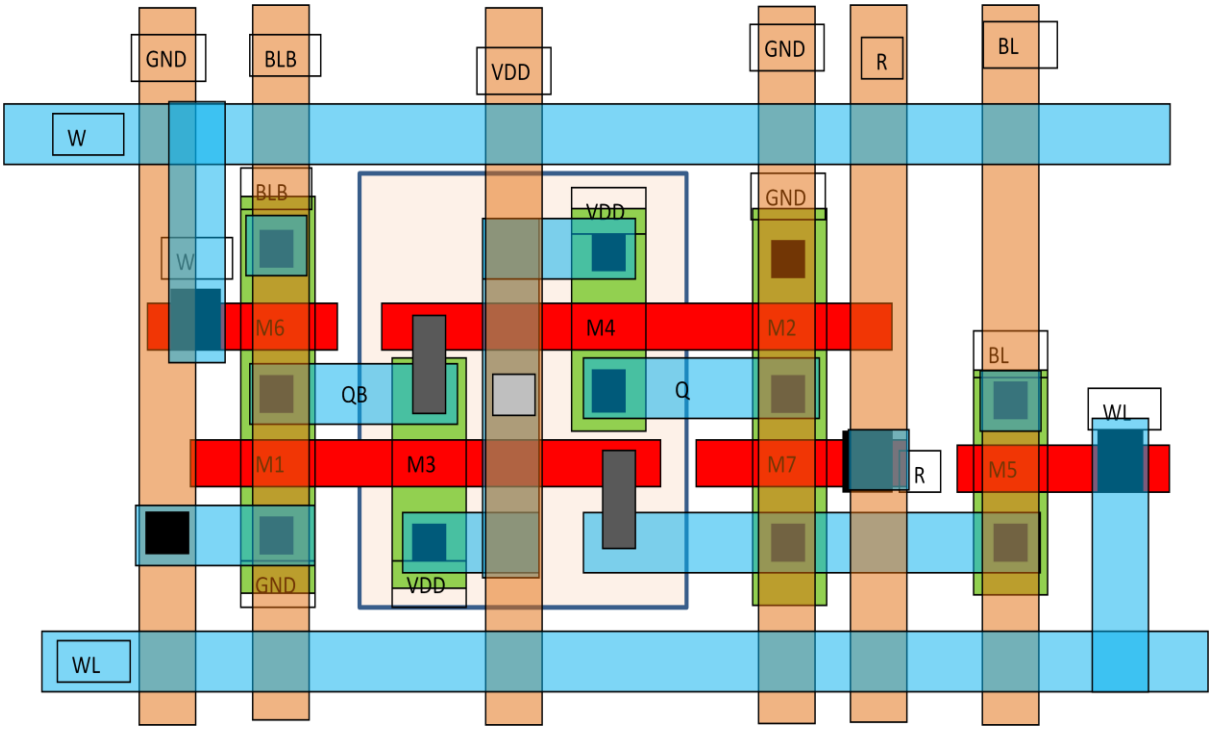


Figure 4.2-Layout of Conventional 7T SRAM Cell

In figure 4.2, two transistors are PMOS and remaining five transistors are NMOS. Blue colour lines are metal 1 and red colour line is metal 2. Yellow lines are polysilicon. Top horizontal line is used for power supply and bottom horizontal line is ground terminal. Metal 1 and poly is joined by via (metal1-poly). Here minimum width of metal 1 is 65 nm. We cannot take width of metal 1 to be less than 65 nm. Metal 1 to metal 1 spacing should be greater than 65 nm. The width of poly should be greater than 50 nm. The width of via should be greater than 65 nm. The minimum spacing between via and via, should be greater than 75 nm.The output waveform of read and write operation are shown in figure 4.3.

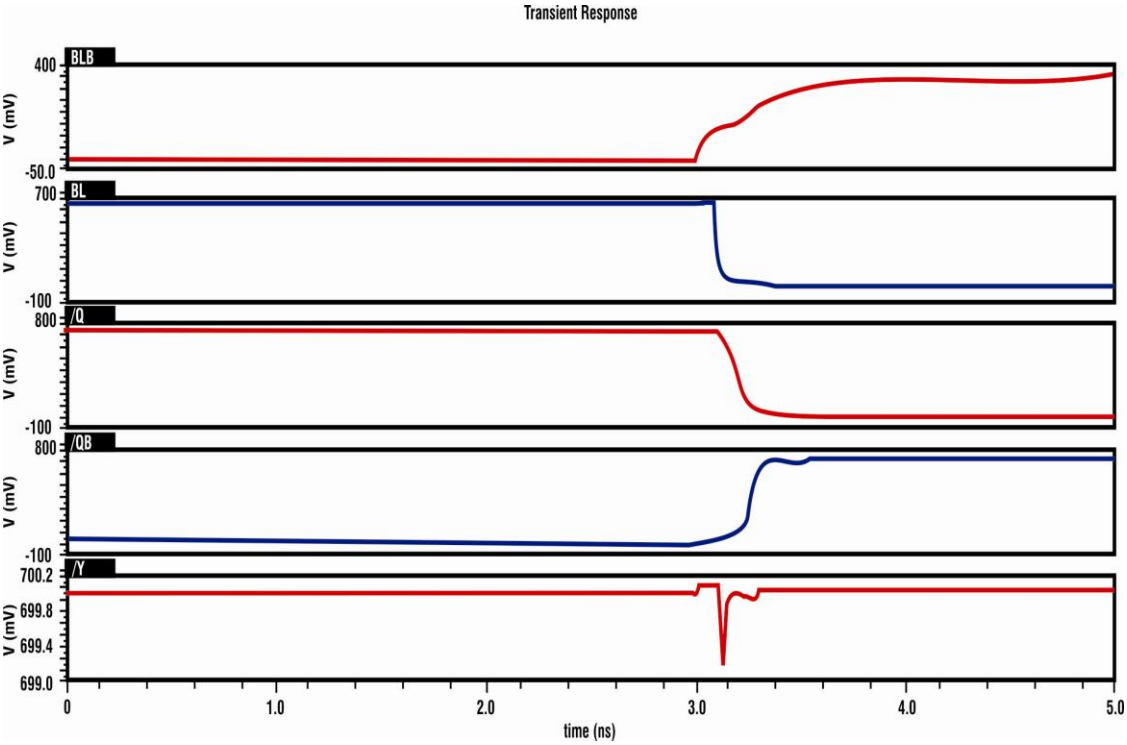


Figure 4.3-Read and Write waveform of Conventional 7T SRAM Cell

4.4 LEAKAGE CURRENT IN 7T SRAM BIT-CELL

In 45 nm technology, the physical oxide thickness is 0.7 nm and channel length is 45 nm. Both gate leakage and sub-threshold leakage currents are important in 7T SRAM bit-cell. In the stand-by mode, the bit-lines are charged to 'VDD' and the word-line is held at 'low' voltage. The leakage current flowing through the transistor depends upon the value stored in the cell. When '0' is stored, there is significant gate leakage current through N-type transistors M1, M5 and M6. Although a similar mechanism operates in transistor M3 as well, the gate leakage here is negligible because of its P-type nature. Gate leakage is maximum in transistors M2 and M7. Sub-threshold currents originate in transistors that are in OFF state and that include transistors M1 and M4 in the cross-coupled inverter pair and the access transistors M5, M6 and M7, except for transistors M6 and M7 whose drain-source voltage is zero. All other three transistors have a significant sub-threshold leakage current. To

summarize, there are five dominant components of gate leakage current through transistors M1, M2, M5, M6 and M7. It has been calculated by equation (4.1).

$$I_{gate} = W.L.A\left(\frac{v_{ox}}{t_{ox}}\right)^2 \exp\left[\frac{-B\left(1-\left(1-\frac{V_{ox}}{\emptyset_{ox}}\right)^{3/2}\right)}{\frac{Vox}{t_{ox}}}\right] \quad (4.1)$$

Where, W and L are the effective transistor width and length respectively.

A= $q^3/16\pi^2 h\emptyset_{ox}$, B= $4\pi\sqrt{2m}_{ox}\ \emptyset_{ox}^{3/2}/3hq$, where m_{ox} is the effective mass of the tunneling particle, $\emptyset_{ox}$ is the tunnelling barrier height, t_{ox} is the oxide thickness, h is 1/2 π times Planck's constant and q is the electron charge.

The gate leakage current of conventional 7 Transistors SRAM is shown in figure 4.4.

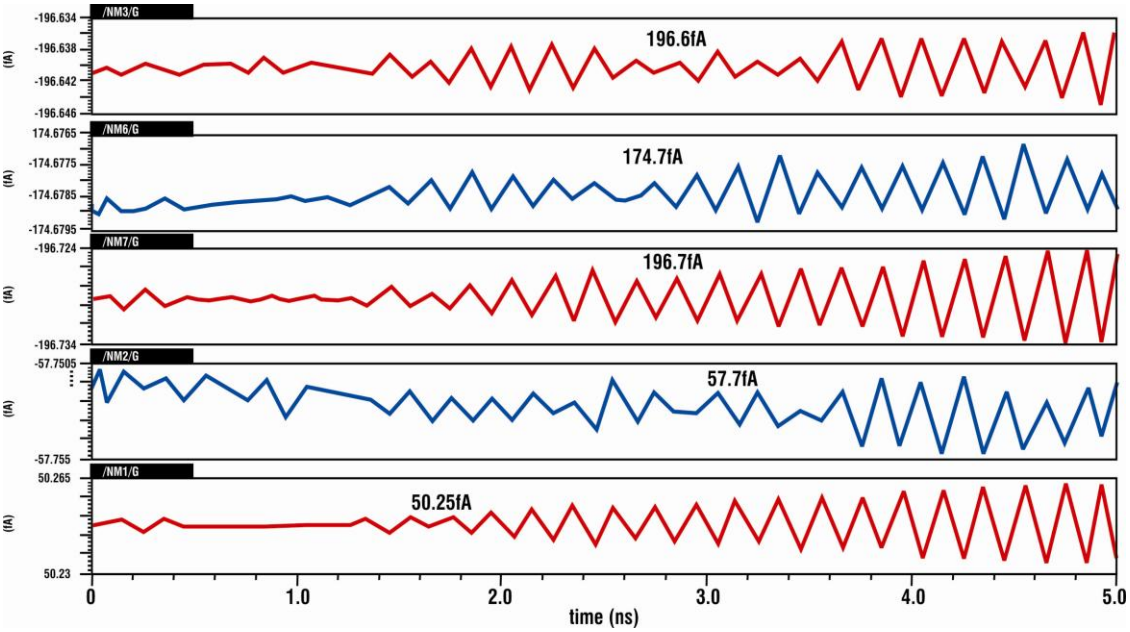


Figure 4.4- Gate Leakage Currents in Conventional 7T SRAM Cell

There are three sub-threshold leakage current components through transistors M1, M4 and M5. It has been calculated by equation (4.2).

$$I_{SUB} = \frac{W}{L}\ \mu v_{th}^2\ c_{sth}\ e^{\frac{V_{GS}-V_T+\eta V_{DS}}{nV_{th}}}\left(1-e^{\frac{-V_{DS}}{V_{th}}}\right) \quad (4.2)$$

Where W and L are width and length μ denotes the carrier mobility. V_{th} = KT/q is the thermal voltage at temperature T.

C_{sth} is the summation of the depletion region capacitance and interface trap capacitance. η is the drain induced barrier lowering capacitance and n is the slope shape factor.

$$n = 1 + \frac{C_{sth}}{C_{ox}}$$

C_{ox} is the gate input capacitance per unit area.

4.5 LEAKAGE CONTROL IN 7T SRAM BIT-CELL

It has been mentioned earlier that self- controllable switch can be used either at the upper end of the cell to reduce supply voltage (USVL technique) or at the lower end of the cell to raise the voltage of the ground node (LSVL technique). The switching energy, the short-circuit energy and the leakage current are assumed to remain constant under the same power supply [94] .The impact of these techniques on leakage currents is described in the next sections.

4.5.1 Leakage control using USVL

An SRAM cell consisting USVL techniques is shown in figure 4.5. In this technique, a full supply voltage is applied to SRAM cell in active mode, while the supply voltage level to SRAM is reduced to voltage level 'Vd' in stand-by mode. Since transistor M3 is in on state, voltage at the drains of M1 and M3 is also reduced to 'Vd'. As before, let us first consider the impact on gate leakage currents. As a result of a decrease in gate voltage of transistor M2, gate leakage current through it, is sharply reduced. A decrease in drain voltage of transistor M1 results in lower gate-drain voltage across it and thus gate leakage current through it, is also reduced. A decrease in source voltage of M6 results in a decrease of one component of EDT (Edge direct tunnelling) leakage across it, while leaving the other unchanged. Gate leakage across transistor M5 remains unchanged.

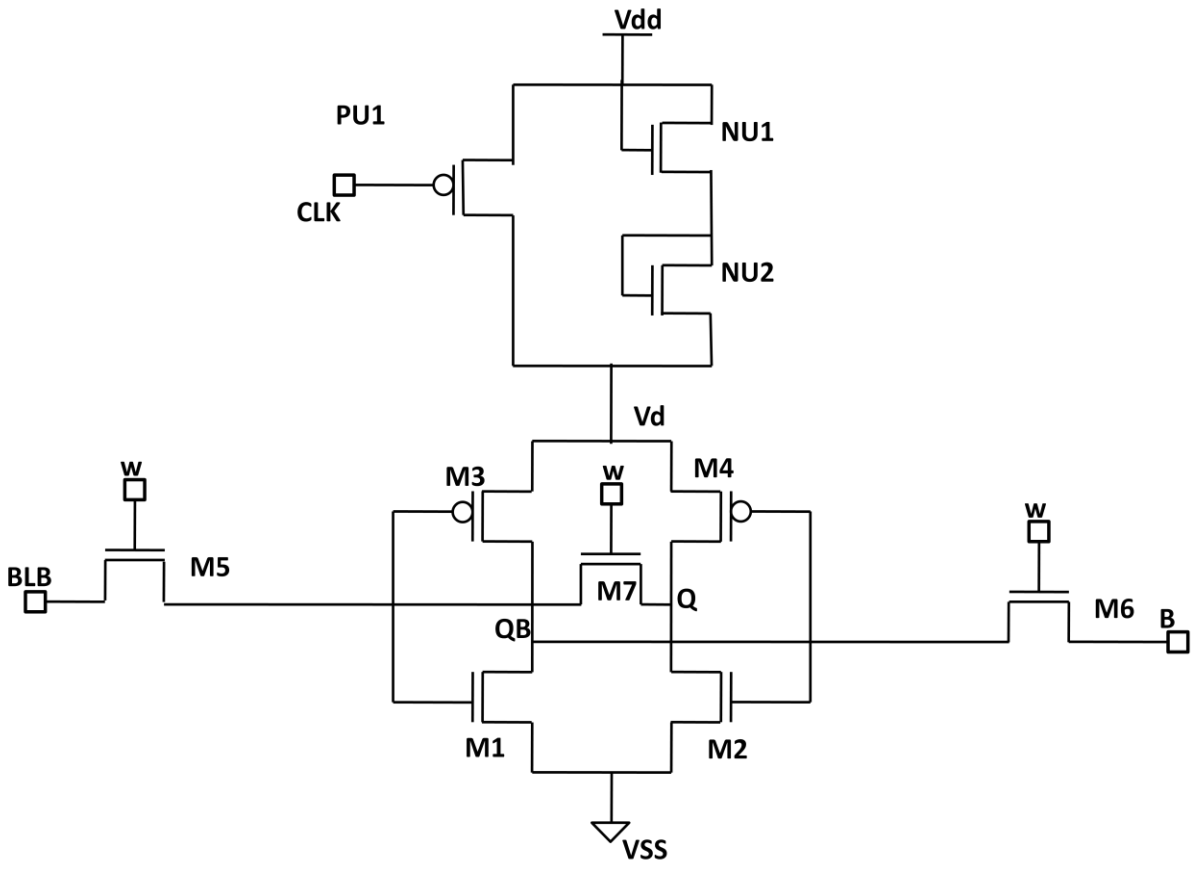


Figure 4.5-Schematic of 7T SRAM Cell after applying USVL Technique

When the clock of the PMOS transistor is '0', the PU1 is 'on', this transistor will behave like a short circuit and the whole current will pass through this branch. This condition is called active mode. In this case,

$$Vd = VDD \tag{4.3}$$

When the clock of the PMOS transistor is '1', then the PU1 is 'off' and this transistor will behave like an open circuit. In this case transistor NU1 and NU2 will weakly on. So there is some voltage drop in this branch. Due to this voltage drop, Vd will be reduced as compared to Vdd. This condition is called standby mode. In this case,

$$Vd = VDD\text{-}Vn \tag{4.4}$$

Where, Vn is the voltage drop of the two NMOS transistors.

Transistor PU1 being a PMOS transistor does not result in any significant added leakage current as a result of transistors used in UVSL circuit. Gate leakage current is shown in figure 4.6.

USVL technique has a better effect on gate leakage current reduction. However, this technique is inferior with respect to sub-threshold leakage current. While, sub-threshold leakage through transistors M1 and M4 is reduced, leakage across transistor M5 remains unchanged, as shown in figure 4.7. Further, a new sub-threshold leakage current appears in transistor M6 as a result of reduction in its source voltage.

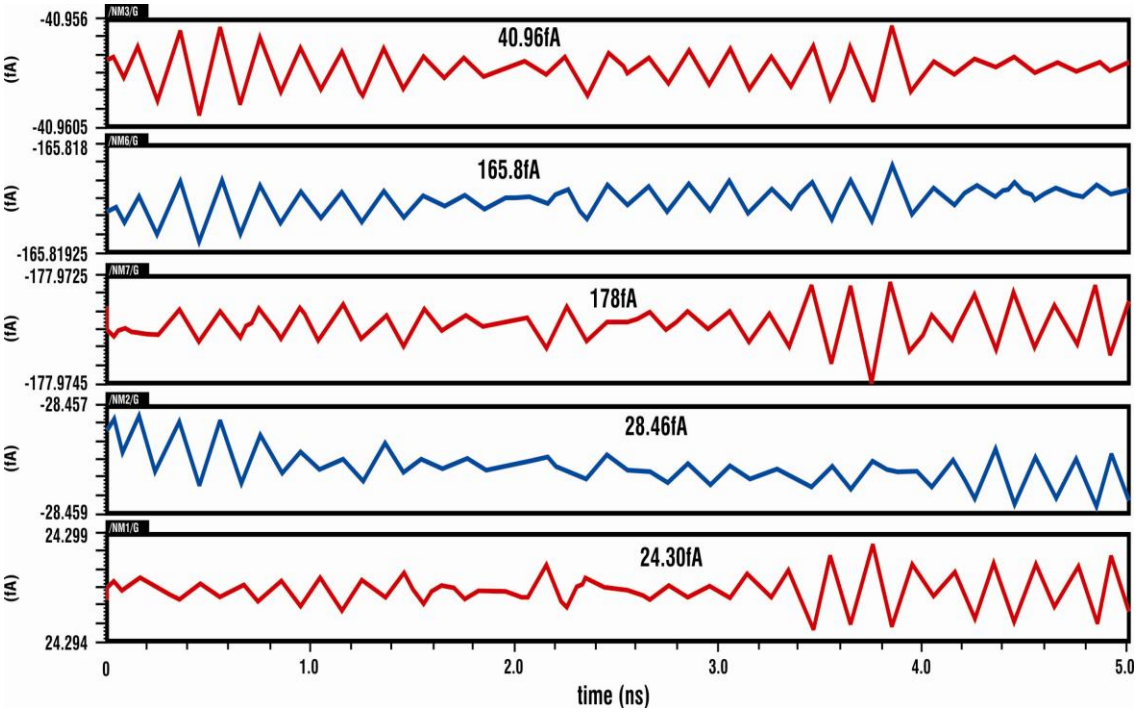


Figure 4.6-Gate leakage currents in 7T SRAM Cell after applying USVL Technique

To summarize, the USVL technique which reduces the gate leakage current, the two components of gate leakage current left in access transistors, remain unchanged. The left sub-

threshold current component in access transistor remains unchanged and results in an additional sub-threshold leakage current across the other access transistor.

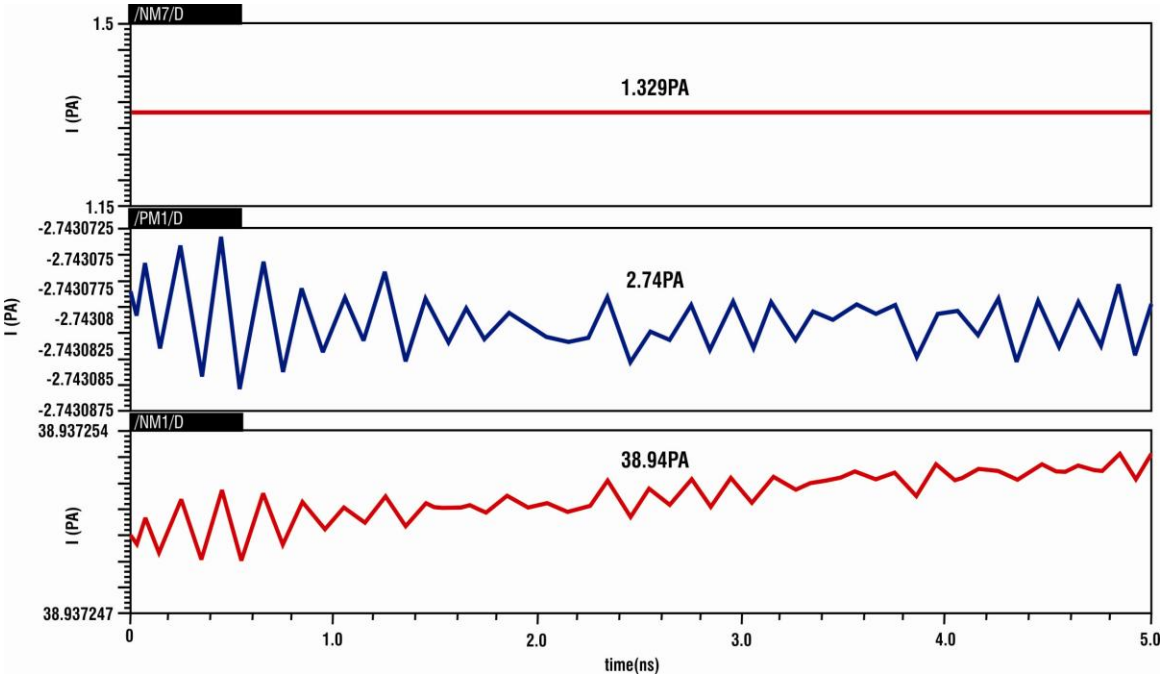


Figure 4.7- Sub-threshold leakage current in 7T SRAM Cell after applying USVL Technique

4.5.2 Leakage control using LSVL

Figure 4.8 shows a schematic of 7T SRAM cell in which LSVL technique is applied. The switch provides '0' Volt at the ground node during the active mode and an increased ground voltage (virtual ground) during the inactive mode. When the clock of the NMOS transistor is '1', then the NL1 is 'on' and this transistor will work like a short circuit and the whole current will pass through this branch. This condition is called active mode. In this case,

$$Vs = VSS \qquad (4.5)$$

When the clock of the NMOS transistor is '0', then the NL1 is 'off' and this transistor will behave like an open circuit, in this case transistor PL1 and PL2 are weakly 'on'. So there is some voltage drop in this branch. We know that the threshold voltage of the PMOS transistor

is negative. Due to this voltage drop, Vs will be increased as compared to VSS. This condition is called standby mode. In this case,

$$Vs = VSS - (-Vp) \quad (4.6)$$

Where Vp is the threshold voltage of the PMOS transistor.

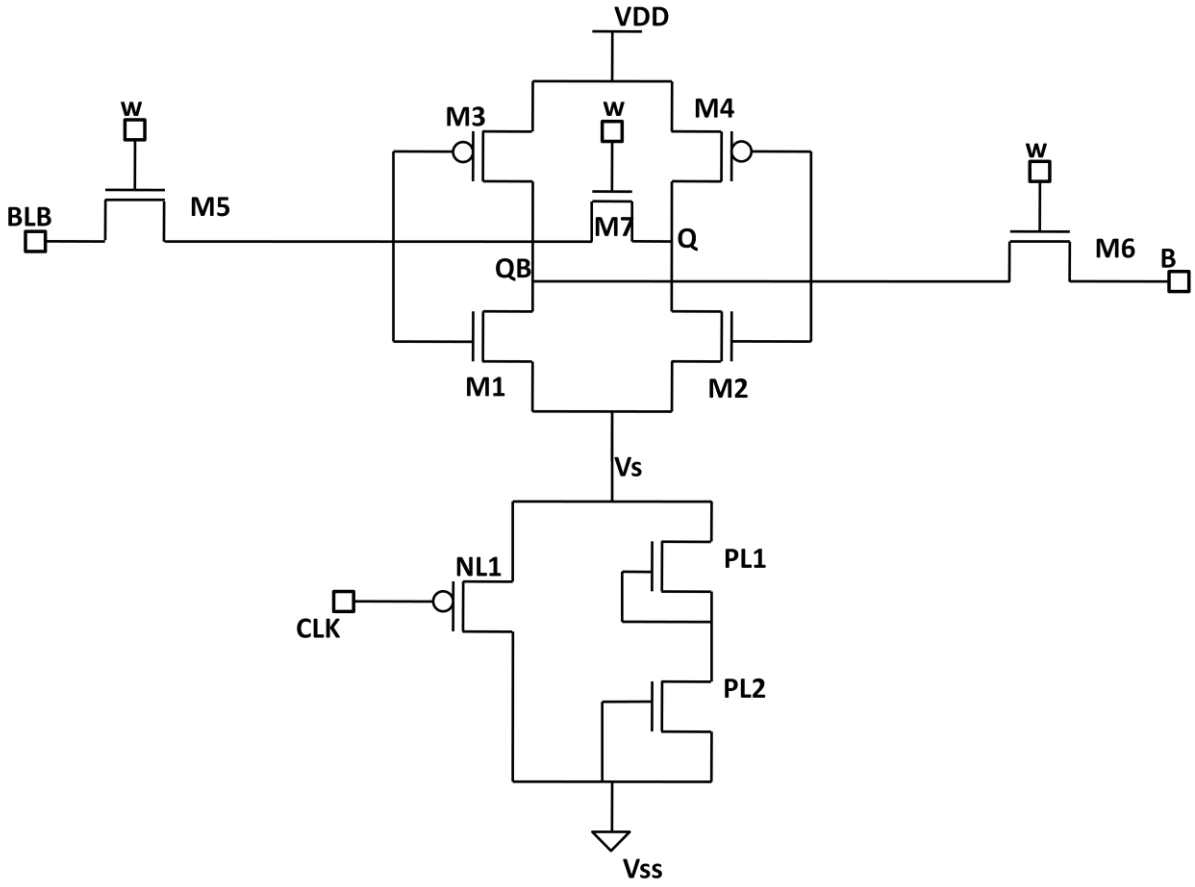


Figure 4.8-Schematic of 7T SRAM Cell after applying LSVL Technique

This technique is similar to the diode footed cache design scheme proposed to control the gate and sub-threshold leakages in SRAM cell, in which a diode designed with high V_t MOS transistors was used to increase the ground voltage of SRAM in the standby mode [87].

Let us consider the effect of this technique on gate leakage. An increase in the virtual ground voltage (Vs) (as shown in figure 4.8), results in reduction of gate-source and gate-drain voltages of transistor M1 and gate-drain voltage of transistor M2 which results in sharp

reduction in gate leakage currents of these two transistors. However, there is no improvement in gate leakage currents for transistors M5 and M6. In fact, as a result of increase in drain voltage of M2, a new gate leakage current appears at transistor M7 as indicated in figure 4.9.

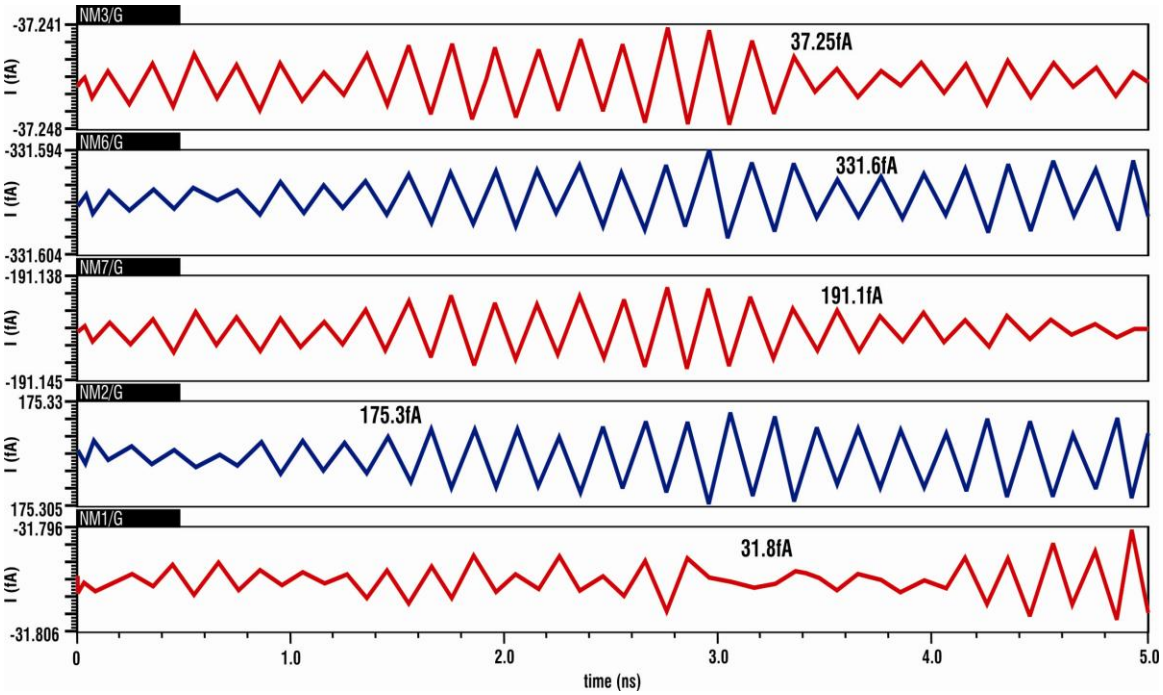


Figure 4.9-Gate leakage currents in 7T SRAM Cell after applying LSVL Technique

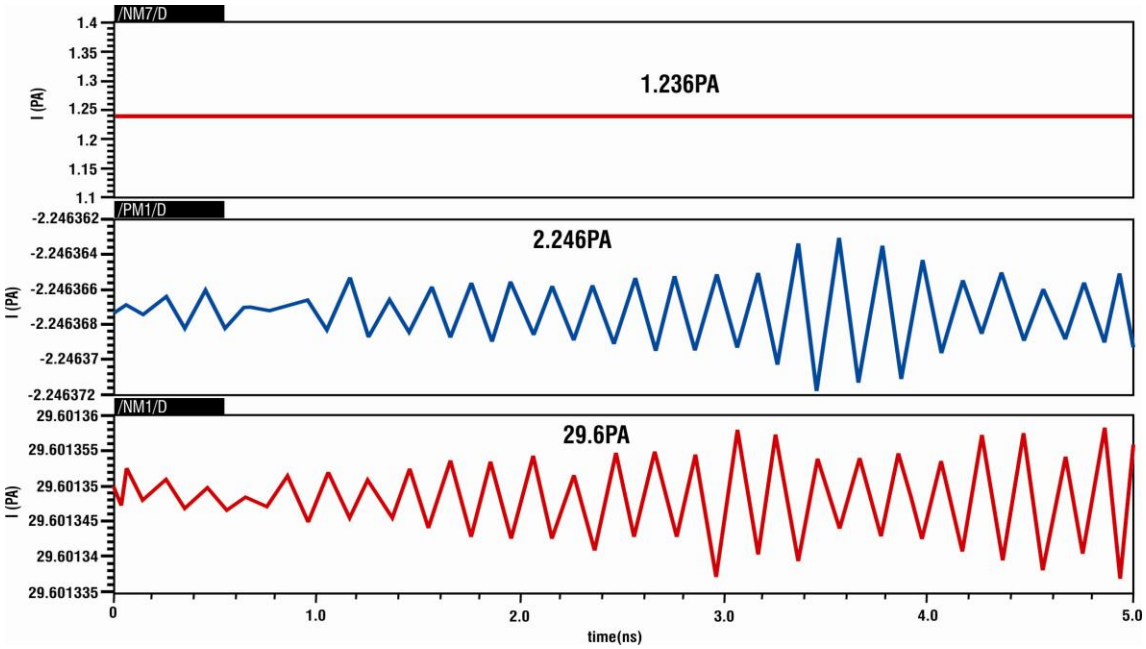


Figure 4.10- Sub-threshold leakage currents in 7T SRAM Cell after applying LSVL Technique

Incorporation of SVL results in another new gate leakage current through NMOS transistor NL1 in the SVL switch. As far as sub-threshold leakage currents are concerned, LSVL approach is successful in reducing the currents through M1, M4 and M5 as well.

To summarize, one has to note that while reducing all sub-threshold currents using LSVL approach, it is only partially successful in reducing gate leakage currents. Sub-threshold leakage current waveform is shown in figure 4.10.

4.5.3 Leakage Control Using Combined Technique (USVL combined with LSVL)

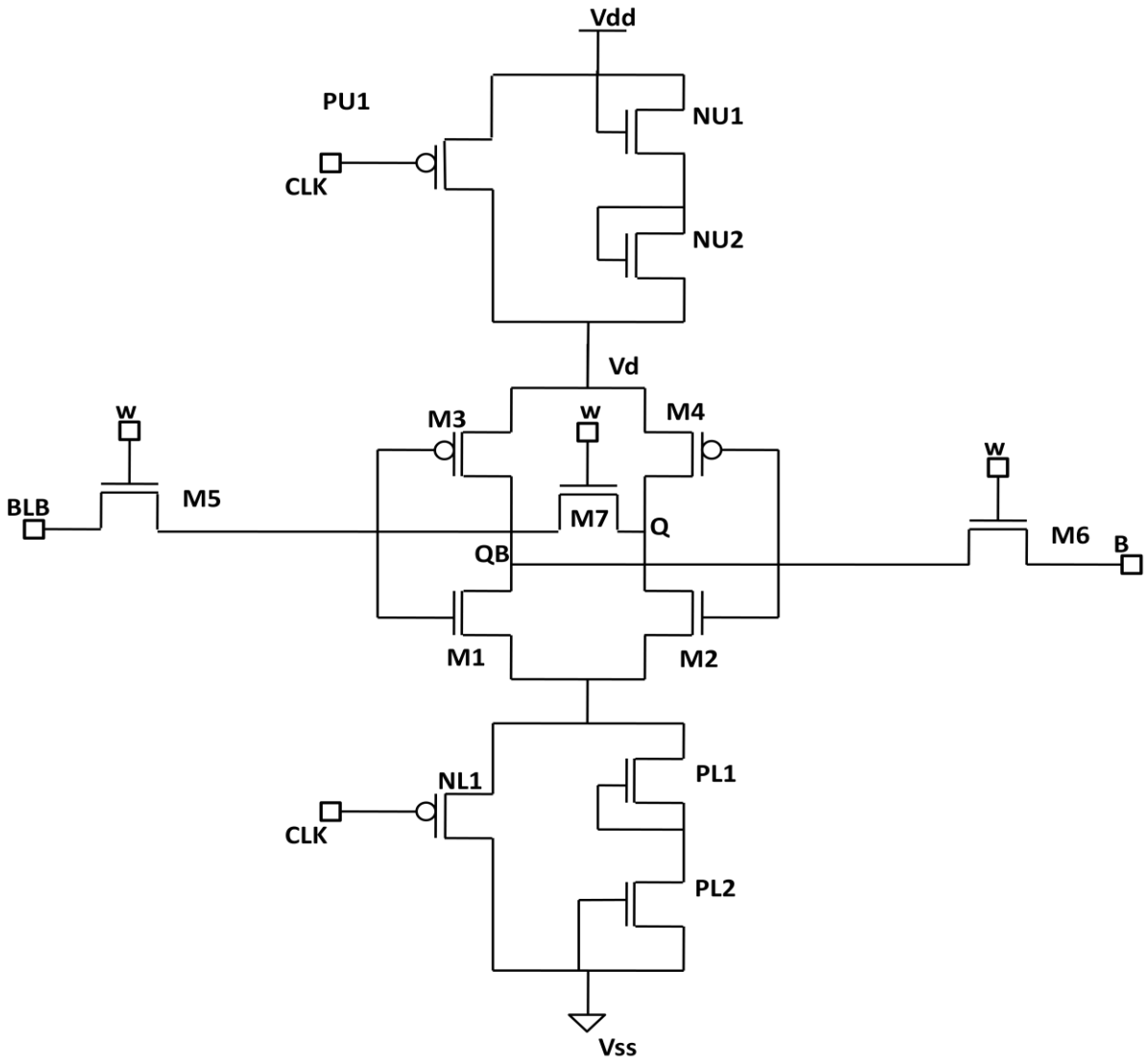


Figure 4.11-Schematic of 7T SRAM Cell after applying both techniques

Figure 4.11 shows the schematic of mixed technique (e.g. LSVL plus USVL). In this technique, both LSVL and USVL are connected to the conventional 7 transistors SRAM.

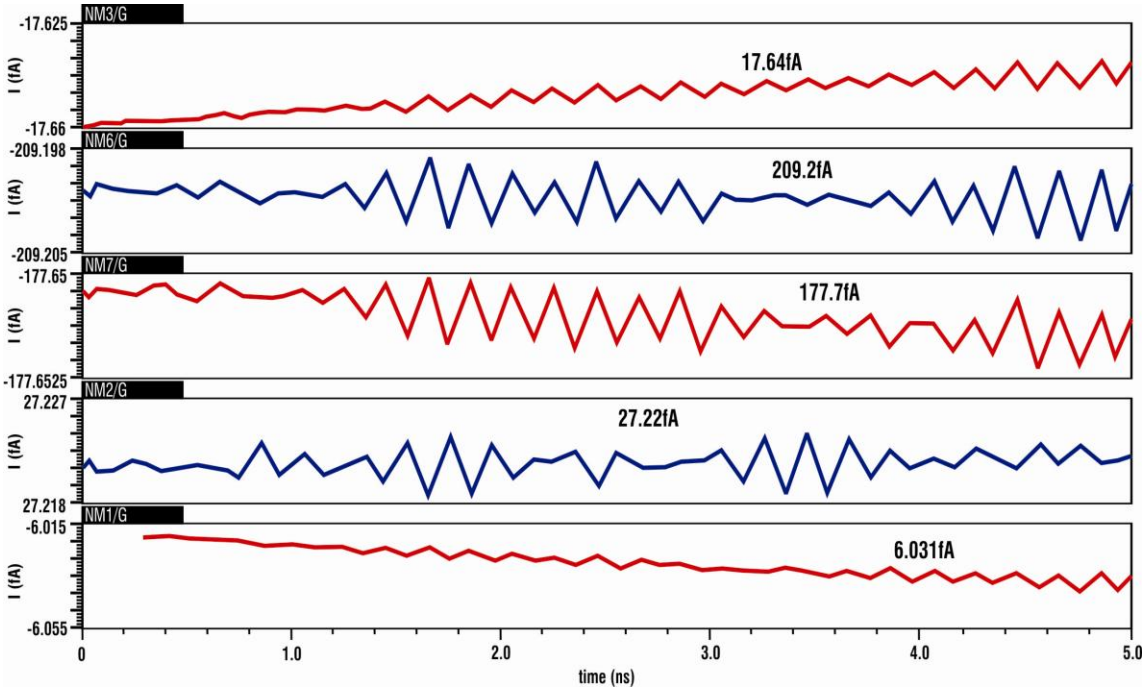


Figure 4.12-Gate leakage currents in 7T SRAM Cell after applying both Techniques

By using this technique, supply voltage is reduced to 0.348 V and ground voltage is enhanced up to 0.234 V. Due to this technique, gate leakage current of the SRAM bit-cell is reduced up to 437 fA as shown in figure 4.12. Sub-threshold leakage current of the SRAM bit-cell is reduced up to 11.92 fA, which is shown in figure 4.13.

The combined technique is connected to both the technique (USVL and LSVL) simultaneously. So the overall voltage of the circuit will be reduced and we will get this value by equation.

$$Vdsn = VDD – (Vd + Vs) \quad (4.7)$$

where Vdsn is the overall voltage of the circuit.

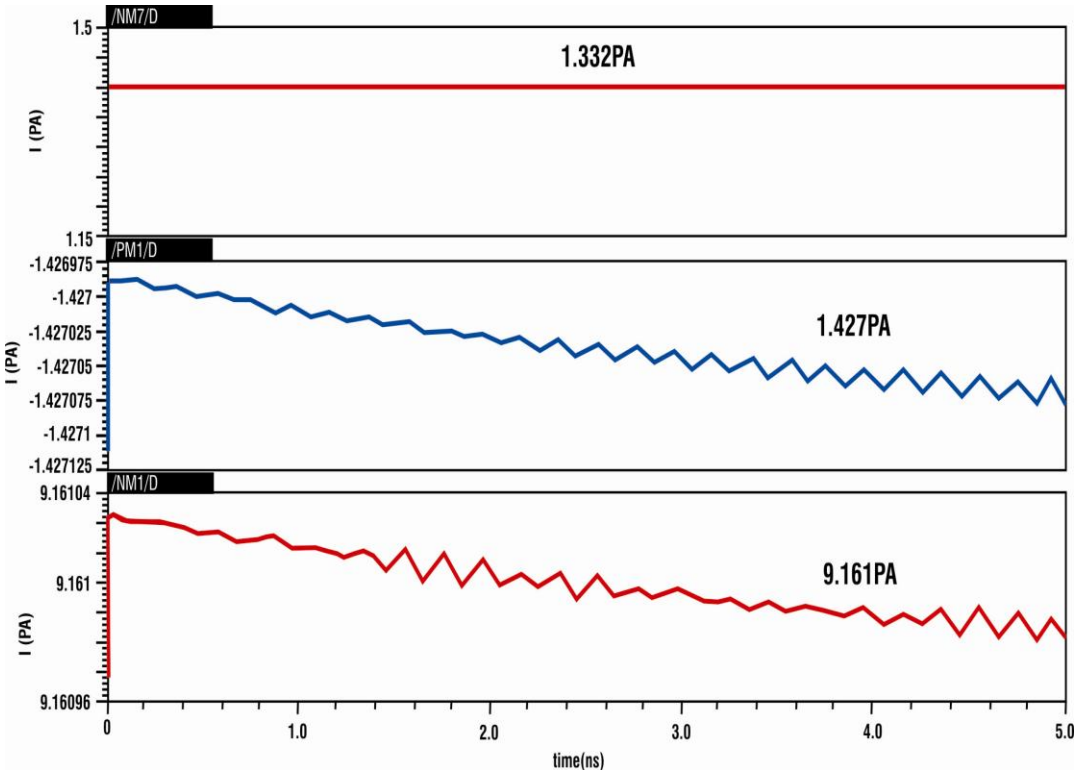


Figure 4.13- Sub-threshold leakage currents in 7T SRAM Cell after applying both Techniques

4.6 ADVANTAGE OF SVL TECHNIQUES

There are numerous advantages of the SVL circuit. When the SRAM circuit is in active mode, the SVL circuit supplies maximum drain- source voltage Vds to the MOSFET which is ON, through 'on' switch. Thus, the SRAM circuit can operate swiftly. On the other hand, when the SRAM circuit is in stand-by mode, it supplies slightly lower Vd and slightly higher Vs to MOS transistor through "weak on switch". Thus, the SVL circuit not only retains data but also produces high noise immunity with minimal overheads in terms of silicon area. Furthermore, the V_t increases and consequently sub-threshold current (I_{sub}) of the "off MOS" transistor decreases. So, stand-by power Pst is greatly reduced.

4.7 SIMULATION RESULTS AND DISCUSSION

The simulation of 7T SRAM cell has been done using Cadence Virtuoso tool at 45 nm technology. Although the circuit is simulated under ideal condition, there are various constraints on simulation parameters like transistor length, width, temperature effect, etc., in the 7T SRAM cell. The leakage currents in conventional 6T SRAM cell and 7T SRAM cell as per the techniques suggested in section A, B and C at a temperature of 27 ^{0}C are shown in table 4.1 and table 4.2, the gate leakage being the only prevailing mechanism at room temperature, LSVL techniques achieve a gate leakage current of 467.05 fA and a total leakage current in 7T SRAM is 33.08 pA and 33.6nA in 6T SRAM cell, while USVL technique without changing bit-line voltage provides a leakage reduction of 437.52 fA in 7T SRAM cell and 25.31nA in 6T SRAM cell. The effective supply voltage across the 7T SRAM is reduced from 0.7 V to 0.582 V.

The combined technique provides 437.791 fA of gate leakage current (I_{gate}) with maximum reduction in sub-threshold leakage current (I_{sub}) 11.92 pA.

Techniques	**M1**		**M2**	**M4**	**M5**		**M6**	**M7**	**Total I_{gate} (fA)**	**Total I_{sub} (pA)**
	I_{gate} (fA)	**I_{sub} (pA)**	**I_{gate} (fA)**	**I_{sub} (pA)**	**I_{gate} (fA)**	**I_{sub} (pA)**	**I_{gate} (fA)**	**I_{gate} (fA)**		
Conv.	50.25	26.46	57.75	910.3	196.7	1.207	174.7	196.6	676	27370.67
USVL	24.30	38.94	28.46	2.74	178	1.329	165.8	40.96	437.52	43.009
LSVL	31.8	29.6	175.3	2.246	191.1	1.236	31.6	37.25	467.05	33.082
USVL + LSVL	6.031	9.161	27.22	1.427	177.7	1.332	209.2	17.64	437.79	11.92

Table- 4.1 Leakage Current in 7T SRAM cell for different SVL techniques at temperatures of 27^{0}c

At the elevated temperature, sub- threshold leakage current increases considerably and gate leakage current almost remains constant. USVL technique is more efficient in gate leakage suppression whereas LSVL technique is better for sub-threshold leakage reduction.

Techniques	**M1**	**M2**		**M3**	**M5**		**M6**	**Icell**
	I_{gate} (nA)	**I_{gate} (nA)**	**I_{sub} (nA)**	**I_{gate} (nA)**	**I_{gate} (nA)**	**I_{sub} (nA)**	**I_{gate} (nA)**	**(nA)**
Conv.	37.1	13.92	0.86	0.56	9.84	0.6	19.56	83.6
USVL	2.38	1.14	0.58	-	9.84	0.6	10.64	25.51
LSVL	2.35	1.08	0.17	0.29	10.68	-	19.44	33.6
USVL Combined with LSVL	2.78	1.14	0.58	-	0.32	0.32	1.2	5.49

Table -4.2 Leakage Current in 6T SRAM cell for different SVL techniques at temperatures of 27^0c

4.8 SUMMARY OT THE CHAPTER

An analysis of gate leakage currents in 7T SRAM cell at 45 nm technology shows that both gate and sub-threshold leakage currents significantly contribute to leakage power dissipation in stand-by mode. Reduction in the supply voltage and an increase in ground voltage using self-controllable voltage level switches for reducing leakage currents in 7T SRAM cell is examined in detail. It is found that the LSVL approach reduces sub-threshold leakage current (I_{sub}), while the USVL approach reduces gate leakage currents (I_{gate}) more effectively. However, both techniques are found to be inadequate for reduction of leakage currents through access transistors. A modified USVL combined with LSVL approach in which access transistors are put in ‘off’ state during the stand-by mode, is found to be very effective in reducing all significant components of leakage currents. The result shows that 437.791 fA

and 11.92 pA reductions in the total sub-threshold leakage currents are achieved at 27^{o}C. In 6T SRAM cell, we have got total leakage current of 5.49nA which shows that 7T SRAM cell is better as compared to 6T SRAM cell.

CHAPTER 5
DESIGN TRADE-OFFS FOR NANO SCALE PROCESS AND MATERIAL PARAMETERS

5.1 INTRODUCTION

Low power memory is need of the hour today with high priority and high stability. Now-a-days, power is the most important factor for the technological advancement. So the power reduction for one cell has a significant role in memory design techniques. In this chapter, some design techniques and useful material for low power design have been introduced. The leakage current reduction, to ground the transistor body for the junction current reduction, gate current and the leakage power, latching between Drain and Source of the transistors, Bit-line and word-line modulation, Mutual flux effect, capacitance effect, VDD and supply voltage modulation and the processing of read/write data for power reduction have been covered in this chapter. The technology and the materials have main impact on power consumption. The material parameters like the ratio adding of impurity and wafer index play a vital role in power reduction. 7T SRAM cell is a very low power consumption cell with high SNM and good read/write stability. In the 7T SRAM cell, high Static Noise Margin is achieved when applied bit-line and word-line modulation have lower VDD results. In 7T SRAM cell, power reduction and enhanced stability is in the same manner with some limitations.

The integration of an entire electrical circuit on a single piece of silicon significantly lowers the cost and intensifies the reliability as compared to the circuits with discrete components. The growth of the semiconductor industry driven by the advancements of the integrated circuit (IC) technology and the market dynamics was predicted by Gordon Moore in 1965

[98]. A new process technology with significantly higher integration density and enhanced speed has been introduced by the semiconductor industry in every two to three years since the early 1970s [102].

The size of the transistors is reduced with technology scaling, thereby increasing the integration density and the operating speed of the circuits [103]. The increasing number and the higher operating speed of transistors lead to a broader functionality and enhanced performance in an integrated circuit. These benefits associated with technology scaling, however, come at a cost of elevated power consumption and improve sensitivity to parameter variations [104]. Developing low power and variation tolerant, integrated circuit techniques have become indispensable for the semiconductor industry. The trends in the evolution of microprocessor technologies are reviewed in this section [103]. The feature sizes of the transistors and the wires have been continually scaled, enhancing the integration density for each new process-technology generation. The minimum critical feature size (channel length) of the transistors in the lead Intel microprocessors has decreased from 10μm in 1971 to 45 nm in 2008. The total number of transistors in the lead Intel has increased by more than a thousand times in less than two decades.

High leakage current in deep-sub micrometer regimes is becoming a valuable contributor to power dissipation of CMOS circuits as the threshold voltage, channel length and the gate oxide thickness are reduced. CMOS devices have been scaled down significantly in each technology generation to achieve the higher integration density and performance. With the continuing trend of technology scaling, leakage power has become a substantial contributor to the power consumption. Moreover, the increasing statistical variation in the process parameters has emerged as a serious obstacle in the nano-scaled circuit design [105] and can

cause a significant increase in the transistor leakage current [106].Design with the worst case leakage may cause excessive guard banding resulting in a lower performance [107]. Hence, accurate estimation of the total leakage current, considering the effect of random variations in the process parameters, is extremely important for designing CMOS circuits in the nano-meter regime. By the process variability of transistor, mismatch becomes a major limitation of overall performance of low-voltage SRAM in nanometer CMOS process. Different leakage mechanisms contribute to the total leakage in a device. The two major ones which are calculated can be identified as sub-threshold leakage and gate leakage. Each component depends differently on the transistor geometry i.e. gate length (Lg), oxide thickness (Tox), and width (W). Hence, variation in each of these parameters results in a large variation in each of the leakage components, thereby, causing a significant increase in the overall leakage. In this research, the leakage components with respect to different process parameters have been analyzed and modeled.

5.2 DESIGN OF SEVEN-TRANSISTOR (7T) SRAM CELL

Figure 5.1 represents the cell schematic of a 7T SRAM cell design. The cell consists of 7 transistor-2 PMOS and 5 NMOS. It consists of a cross-coupled inverter pair known as active transistor that stores the data and there are two transistors which are known as pass transistors to load/retrieve data on bit-lines, BL and BLB. There are two word-lines which are used for read and write operation. The read and write operations are controlled by the last transistor which is the most important transistor for the whole circuit operation. During a write operation, the data is loaded on the bit-lines and the word selects signal WS turned ‘high’. A successful write operation occurs if the data is correctly latched in the cell. The bit-lines are

pre-charged to the supply voltage and the word select line is turned ‘high’ to retrieve the data during a read operation.

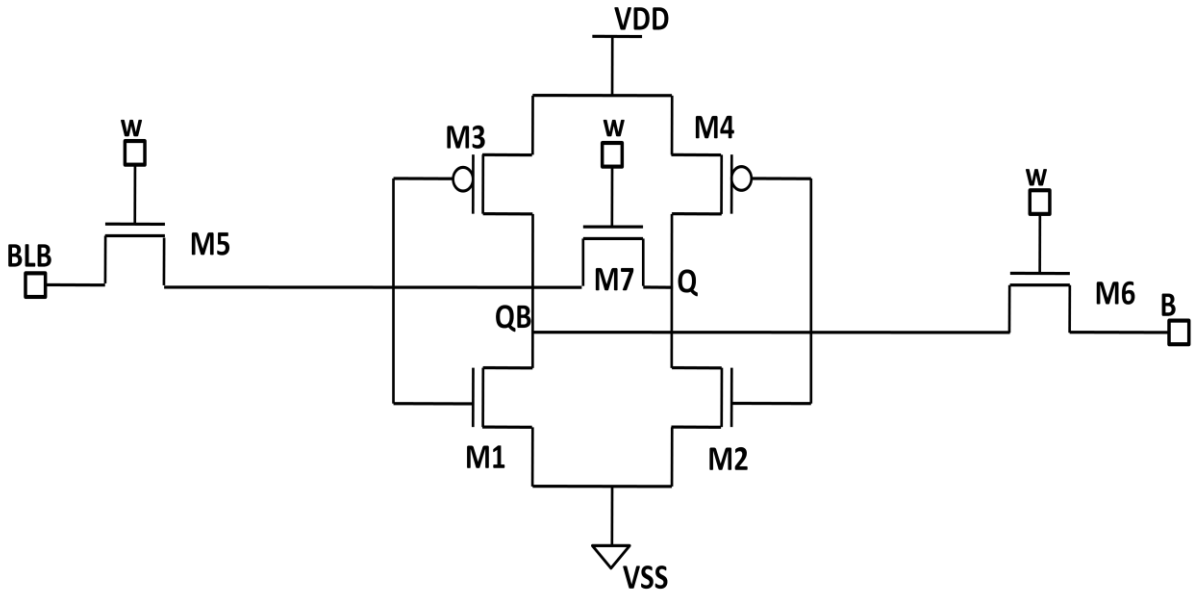


Figure 5.1-Schematic of 7T SRAM Cell

A read failure can occur if drop in the voltage is higher than the threshold voltage of the cross coupled inverter pair. Figure 5.2 shows the layout of 7 transistors SRAM cell. The waveform of read and write operation of 7 transistors SRAM cell is shown in figure 5.3

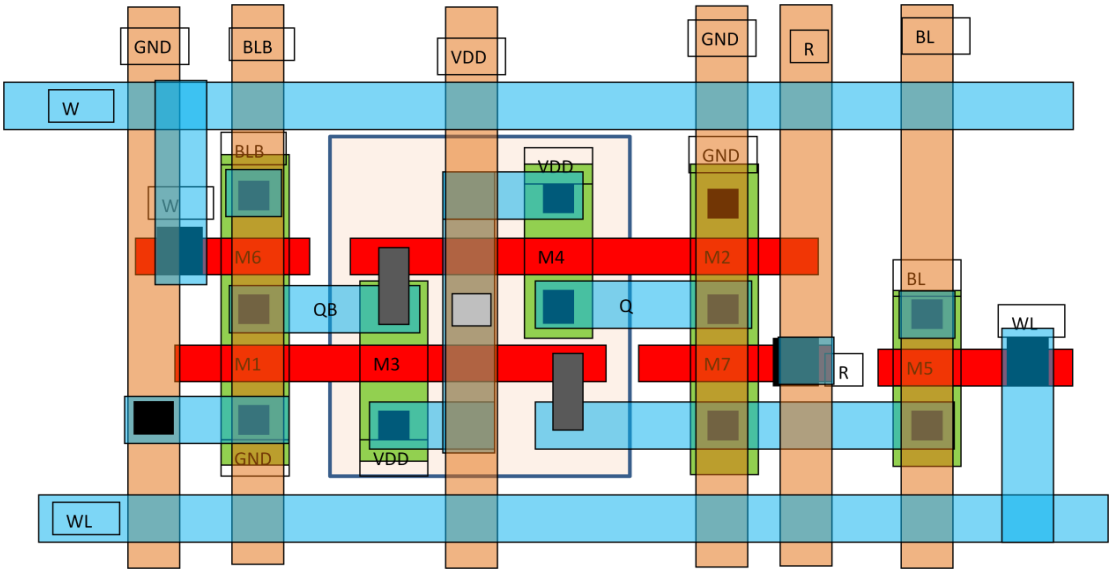


Figure 5.2- Layout of 7T SRAM Cell

The layout of 7T SRAM cell is shown in figure 5.2. The above blue horizontal line is used for supply pin and bottom blue horizontal line is used for ground pin. In this layout two PMOS transistors and five NMOS transistors are used. The blue colour lines are metal 1 and red colour line is metal 2. Metal 1 to Metal 1 spacing should be greater than 65 nm. The width of poly should be greater than 50 nm. The minimum spacing between via and via should be greater than 75 nm.

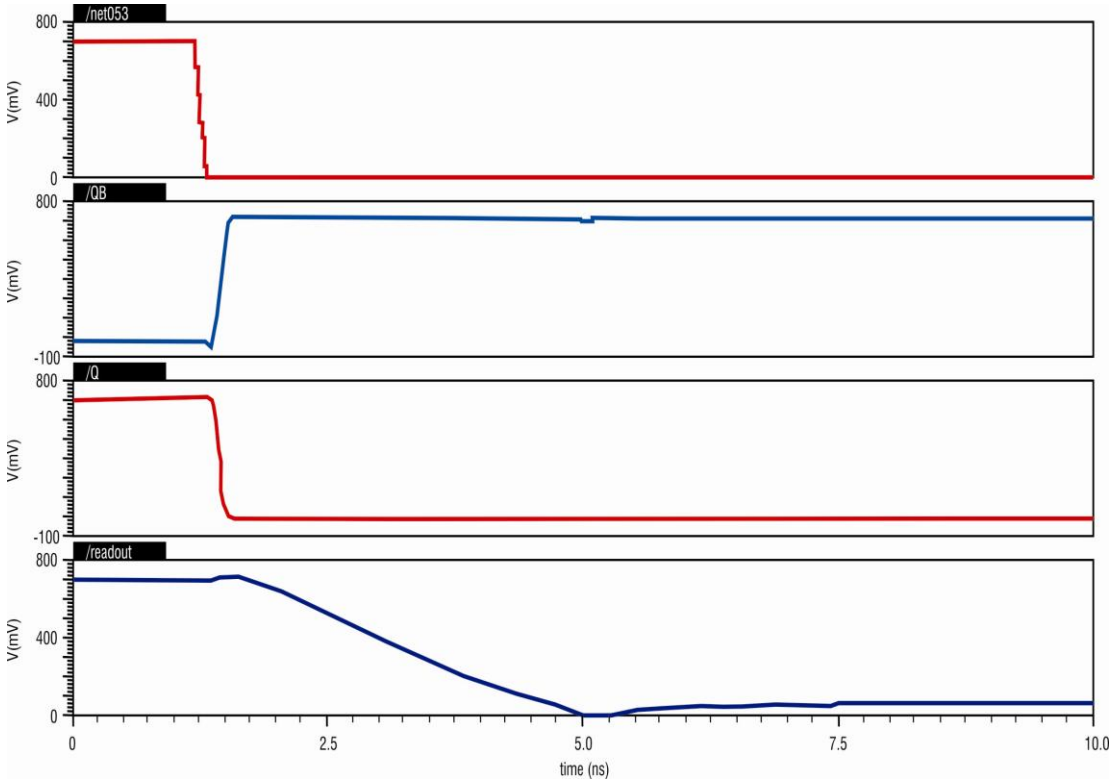


Figure 5.3- Read and Write waveform of 7T SRAM Cell

5.3 MATERIAL PARAMETER OF DEVICES

Material Parameters are very important for the analysis as well as designing of any analog or physical devices. Material parameters of physical devices such as carrier concentration, scattering and leakage current are dependent on doping and temperature etc. Although technical consideration such as gate and ohmic metallization as well as dopant profiles are an

inextricable component of device behaviour at elevated temperatures, here analysis is done with varying temperature (99).

5.3.1 Carrier mobilities

The mobility of charge carriers determines the performance of the device and these mobilites are expected to change with an increase in operating temperature. There are various carrier scattering mechanisms for semiconductor materials that limits the carrier mobility principle as can be seen in acoustic phonon scattering phenomenon. This phenomenon refers to the columbic interaction between the charge carriers with the ionized dopant that give rise to the free carriers first approximation of given material mobility limitation from ionized impurity scattering scales with temperature as $T^{3/2}$ .While that from acoustic phonon scattering scales as $T^{3/2}$, however mobility also depends upon factors such as density of ionized impurities which in particular varies with the temperature. In addition, polar semiconductor such as GaAs optical phonon scattering phenomenon becomes more important, Also, the critical current carrying area of some devices comprises a thin sheet of charge near a hetro interface, this characterizes the inversion layer change at the interface of silicon and SiO2 in MOSFET.

5.3.2 Intrinsic Carrier concentration

There are mainly two factors which influence the intrinsic carrier concentration of any device namely energy bandgap of the semiconductor material and the operating temperature. Thermal energy KT is generally sufficient to promote electrons from the valence band to the conduction band giving rise to the thermally generated current, which is not affected by explicit device operation. In fact at sufficiently high temperature the thermally generated intrinsic carrier concentration can exceed the density of the dopant which results in the loss of

control over the concentration of the charge carriers in the device. The intrinsic carrier density for a material is given as

$$ni = (\frac{2\pi KT}{h^2})^{\frac{3}{2}}(Mdh\ Mde)^{\frac{3}{2}} \exp\ (-\frac{Eg}{2KT}) \quad (5.1)$$

Where, k= Boltzmann constant,

h= Plank constant,

T= Absolute Temperature,

Mdh, Mde= Hole and electron effective mass.

In intrinsic semiconductor ni=p=n. Above equation reflects the effect of increase in temperature on the intrinsic density. An increase in temperature results in the increase in the ni density. Also larger the band gap of the material, larger is the current density.

5.3.3 Schottky Leakage

A MOSFET device that utilizes the schottky barrier junction property such as the reverse leakage current which increases at an elevated temperature acts as a limitation to the device operation. The reverse leakage current of an ideal schottky barrier diode is approximately given as

$$Js = A^{*}T^{2}\exp\ (-\frac{qp_b}{KT}) \quad (5.2)$$

Where, A*= An effective Richardson constant and

Pb= Schottky Barrier height for thermionic emission.

For a MOSFET device the schottky junction reverses the gate electrode potential. Thus it is desired that carrier injection across the barrier under the forward biased condition must be minimized. Also the reverse leakage current under the forward biased conduction is increased at an elevated temperature in both schottky junction and pn junction.

5.3.4 Threshold Voltage Shift

The intricate coordinate interaction of devices within a circuit depends on the control of the threshold voltage of the component devices while Fermi level changes with the temperature. The magnitude of the threshold voltage gets reduced as the temperature is increased. The threshold voltage equation is given as

$$V_{T=2\varphi_f} \; -\frac{Q_{ss}}{C_{ox}} + \frac{(2\epsilon qN2\varphi_b)^{\frac{1}{2}}}{C_{ox}} + \varphi_{ms} \qquad (5.3)$$

Where, $\varphi_{ms} =$ Metal semiconductor work difference,

$Q_{ss=}$ Fixed charge located at the silicon SiO2 interface,

C_{ox} =Gate oxide capacitance per unit area and

N= Substrate doping density

5.4 IMPACT OF OPERATING/PROCESS AND MATERIAL PARAMETERS VARIATION

(a) Access Time: The access time is resolute by the time it takes for the cell to extend a minimum required voltage drop on the bitline. The worst case condition for the impact of the BTI aging on the access time is when the cell residue in a fixed state (Q='1'; Q='0').Due to device scaling, there are numerous design challenges for nanometer SRAM design. To ease the power consumption, supply voltage has been scaled down which has accordingly reduced the threshold voltage. Reduction of threshold voltage and ultra–thin gate oxide have increased sub threshold leakage and gate leakage current rising standby power consumption. Besides this, read access time (TRA) and write access time (TWA) also get considerably affected.

(b) Leakage Power: Leakage in the SRAM cell is mainly caused by the sub threshold leakage which occurs on the OFF transistors. Hence, the BTI induced Vth enhance which

happens on the ON transistors does not contact the leakage of the cell unless the cell changes state and the ON transistors become OFF.

5.4.1 DESCRIPTION OF VARIOUS OPERATING PARAMETERS USED IN 7T SRAM CELL

(a) Operating Current: This is the maximum amount of current that SRAM consumes while it is in operation with the Vcc at the maximum, the chip select pin active and output at high impedance.

(b) Standby Current: This is the maximum amount of current that the SRAM consumes while it is deselected, i.e. while the chip pin select is disabled.

(c) Output Leakage Current: This is the maximum amount of current flowing through an I/O pin when chip is deselected.

(d) Read Cycle Time: This is the minimum amount of time needed to complete one read cycle from one memory address to another.

(e) Chip Select Access Time: This is the maximum amount of time needed for data read from memory address & becoming valid as referenced from the time the chip select pin is enabled.

(f) Write Cycle Time: This is the minimum amount of time needed to complete one write cycle from one memory address to another.

(g) Chip Select To End of Write Time: This is the minimum amount of time that write enable pin must be active for successful write cycle as referenced from the time chip select pin is enabled

(h) Write Pulse Width: This is the minimum amount of time write enable pin must be in active mode for the write cycle to be successful.

(i) Output Active from End of Write Time: This is the minimum amount of time it would take the I/O pins to go into the output mode again after the write enable pin is deactivated,

5.4.2 DEVICE GEOMETRY VARIATION

The first set of process variations of concern relate to the physical geometric structure of MOSFET and other devices (Resistors and capacitors) in the circuit. These typically include:

(a) FILM THICKNESS VARIATIONS-: The gate oxide thickness is significant but usually with moderately well controlled parameters. A variation tends to take place primarily from one wafer to another with good across wafer and transversely die control.

(b) LATERAL DIMENSION VARIATIONS-: Lateral dimensions (Length, Width) typically arise due to photolithography immediacy effects (a symmetric pattern dependency); mask, lens or photo system deviations (a repeated die dependent variation, though not directly the purpose of the layout density or other layout parameters).

5.4.3 DEVICE MATERIAL PARAMETER VARIATIONS

(a) DOPING VARIATION-: Deviation arising due to insert amount, energy, or angle can affect junction depth and doping profile (and thus may also impact effective channel length) as well as other electrical parameters such as threshold voltage. Depending on the gate technology used, these deviations can lead to some loss in the matching of NMOS versus PMOS devices (101).

(b) DEPOSITION AND ANNEAL-: Additional material parameter variations are observed in the silicide formation and in the grain structure of poly or metal lines. These variations may depend on the deposition and anneal processes, and thus experience from substantial wafer to wafer and within wafer deviations, and may also have large random device to device constituent.

5.4.4 DEVICE ELECTRICAL PARAMETER VARIATIONS

(a) V_T VARIATIONS-: A key concern is the threshold voltage (V_T) variation. In accumulation to geometric sources, mobile charge in the gate oxide can initiate a bias dependent variation.

(b) DISCRETE DOPANT VARIATION-: Another source of V_T variations that is just established becomes important in SRAM and other circuit is related to random dopant fluctuations. The implication is that such random discrete dopant fluctuations will likely be tolerable for logic, but may pose a problem for narrow and intense devices such as SRAM blocks containing large numbers of devices that must be well matched.

(c) LEAKAGE CURRENT -: Other electrical constraint variations can also be of concern in circuit design. Leakage current is a key factor for any SRAM cell. The leakage current is straightforwardly associated to the electric field of the device.

5.4.5 INTERCONNECT GEOMETRY VARIATION

Vertical and lateral dimensions as well as material property deviations can be the sources of variation in interconnect structures. Key geometry concern includes:

(a) LINE WIDTH AND LINE SPACE-: Variations in width of patterned lines again arise due to photolithography and etch dependencies. Variation in line width can directly impact line resistance, as well as the capacitance from one layer to layers above or below. Deviations in line width can also result in line space differences affecting the level of line to line coupling within the layer (and can impact not only capacitance but also cross talk and signal integrity).

(b) METAL THICKNESS -: In conventional metal interconnect, the thickness of sputtered or otherwise deposited metal film and liners or barriers is usually well controlled, but can vary from wafer to wafer and across wafer.

(c) DIELECTRIC THICKNESS-: The thickness of deposited and polished oxide can also suffer substantial deviations. While wafer level deposition can be differ (typically on the order of 5%), more difficult are pattern dependent characteristic of such deposition.

(d) CONTACT AND VIA SIZE-: Contact and via sizes can be exaggerated by etch process deviation, as well as symmetric layer thickness dependencies.

5.4.6 INTERCONNECT MATERIAL PARAMETER VARIATION-:

(a) CONTACT AND VIA RESISTANCE-: Contact and via resistance associated to good ohmic contact can be susceptible to etch and clean processes, with extensive wafer to wafer and random component.

(b) METAL RESISTIVITY AND DIELECTRIC CONSTANT-: While metal resistivity variation can take place (and include a small random element), resistivity usually varies significantly on a wafer to wafer basis and is frequently well controlled.

5.5 LEAKAGE COMPONENTS

The leakage current of a deep submicron CMOS transistor consists of three major components: junction tunneling current, sub-threshold current and gate tunneling current. In the following points, each of these three factors are briefly discussed.

5.5.1. Junction Tunneling Leakage

The reversed biased p-n junction leakage has two main components: one is minority carriers' diffusion near the edge of the depletion region and the other is due to electron-hole pair generation in the depletion region of the reverse biased junction. The junction tunneling current is an exponential function of the junction doping and the reverse bias voltage across the junction. Since, junction tunneling current is a minimal contributor to the total leakage

current, so no attempt has been made to measure this component of leakage in an SRAM in this chapter.

$$I_D = I_s\left(e^{\frac{V_D}{V_T}} - 1\right) \quad (5.4)$$

Where, $I_{D,}$ is the diode current,

$I_{s,}$ is the reverse saturation current which depends on the doping levels and area of diffusion regions, typical value is < 1fA/um^2.

$V_{D,}$ is the reverse bias diode voltage and

$V_{T,}$ is the volt equivalent of temperature.

5.5.2 Sub-threshold Leakage

Sub-threshold leakage current is the drain-source current of a transistor when the gate-source voltage is less than the threshold voltage. More precisely, sub-threshold leakage happens when, the transistor is operating in the weak inversion region. The sub-threshold current depends exponentially on threshold voltage which results into a large sub-threshold current in short-channel devices.

$$I_D \approx I_{D0} e^{\frac{V_{GS} - V_{th}}{\eta V_T}} \quad (5.5)$$

Where, $I_{D0,}$ is the leakage current,

$V_{GS,}$ Gate to source voltage,

V_{th}, Threshold voltage of MOSFET,

η, is the material constant and

$V_{T,}$ is the volt equivalent of temperature.

When $V_{GS} \leq V_{th}$ then:

$$I_D \approx I_{D0}$$

This proves that when gate to source voltage is less than or equal to threshold voltage, the drain current is nearly equal to the leakage current of the MOSFET.

5.5.3 Gate Tunneling Leakage

Gate leakage is the oxide tunneling current due to the low oxide thickness and the high electric field which increases the possibility of carrying the tunnel through the gate oxide. Gate tunneling current is composed of three major components: gate to source and gate to drain overlap current, gate to channel current, part of which goes to source and the rest goes to drain, and the third is gate to substrate current.

$$J_g \approx A\left(\frac{V_g V_{aux}}{t_{ox}}\right)^2 e^{-t_{ox}B(\alpha-\beta|V_{ox}|)(1+\gamma|V_{ox}|)} \quad (5.6)$$

Where, A and B are constants,

α, β *and* γ are physical parameters defined by the device technology,

$t_{ox,}$ oxide thickness,

$V_{aux,}$ indicates density of carriers and

$V_{ox,}$ unknown quantity.

5.5.4 Leakage Current

Leakage current is a main factor for any SRAM cell. The leakage current is directly related to the electric field of the device.

SRAM/PARAMETER	Without Process Variation	After Process Variation
Gate Leakage Current	61.78FA	1.154pA
Sub-threshold Current	1.125nA	13.139pA

Table- 5.1 Leakage Current and Leakage Power of 7T SRAM cell

By reducing the supply voltages, the leakage current can be decreased. An analysis has been done on leakage current saving by controlling the different nodes of 7T SRAM cell (WL, BL, VDD, VSS, VNMOS, and VPMOS) [108]. Table (5.1) shows the study of 7T SRAM cell on the basis of their leakage current and leakage power, respectively.

5.6 STATIC NOISE MARGIN

Static Noise Margin can be defined as the minimum dc noise voltage necessary to flip the cell state. SNM is used to measure the stability of the cell [109].SNM affects both read and write margin which is related to the threshold voltage of the PMOS and NMOS devices in SRAM cells. Static noise margin (SNM) of SRAM cell depends on cell ratio (CR), supply voltage and pull up ratio (PR). The value of SNM should be high for the consistency of SRAM cell. Cell ratio is the ratio between sizes of the driver transistor to the access transistor during read operation. Pull-up ratio is defined as the ratio between sizes of the access transistor to the load transistor during write operation.

$$\text{Cell Ratio} = \frac{M1}{M5} \text{ or } \frac{M2}{M6} \tag{5.7}$$

$$\text{Pull Up Ratio} = \frac{M5}{M3} \text{ or } \frac{M6}{M4} \tag{5.8}$$

5.6.1 Read Static Noise Margin (RSNM)

Read Static Noise Margin is a measure of the voltage required at the node store ‘0’ to flip the state of a SRAM cell during reading cycle. Figure 5.4 shows the waveform of the RSNM of 7T SRAM. The read Static Noise Margin (SNM) deteriorates with decrease in supply voltage [106] and increase with transistors mismatch. This mismatch occurs due to the variations in physical quantities of identically designed devices like their body factor, current factor and the threshold voltages. Though, at low voltage SNM will decrease and the overall SRAM delay will increase.

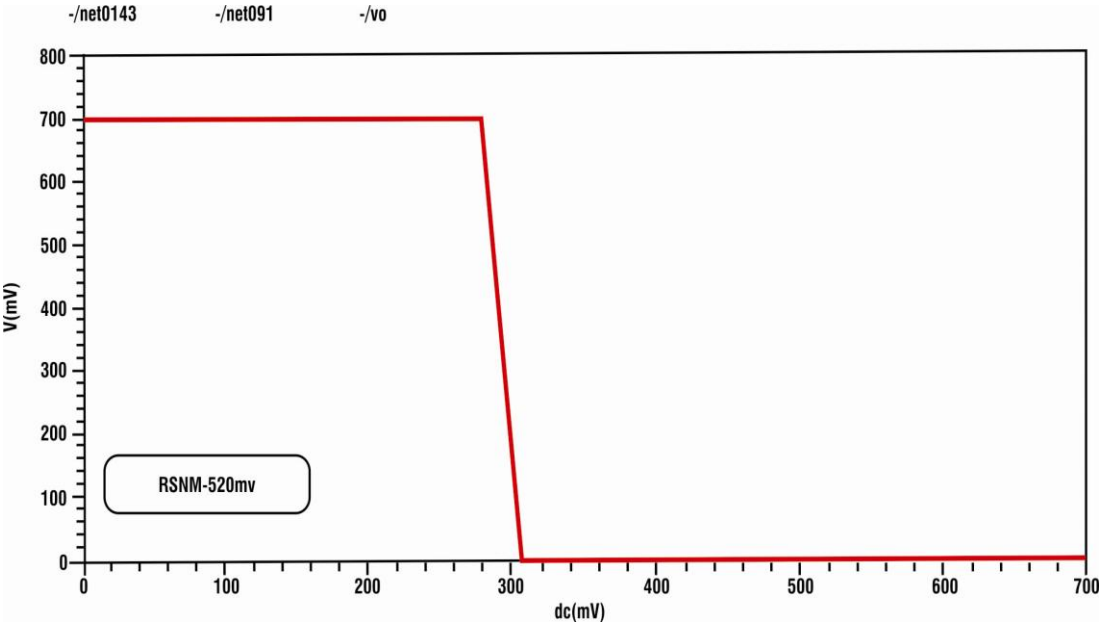


Figure 5.4- Read SNM of 7T SRAM

As shown in above figure, NM_H and NM_L are defined as equations (1) and (2) respectively.

$$NM_H = V_{OH} - V_{IH} \tag{5.9}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - \frac{K_{s-n(sat)}\left(V_{IL} - V_{TH\_n(sat)}\right)^{\alpha\_n(sat)}}{K_{l-p(lin)}\left(\left|-V_{DD} - V_{TH\_p(lin)}\right|\right)^{\alpha\_n(lin)/2}} - \left(\frac{K_{l-p(lin)}}{K_{s-p(sat)}}\frac{2}{\alpha_{n(sat)}}\right)^{\frac{-2}{\alpha_{n(sat)+2}}}$$

$$\left(\left|-V_{DD} - V_{TH_{p(lin)}}\right|\right)^{\frac{2\alpha_{p(sat)}}{\alpha_{n(lin)+2}}} + V_{TH\_n(lin)} \tag{5.10}$$

$$NM_L = V_{IL} - V_{OL} \tag{5.11}$$

$$NM_L = V_{IL} - V_{OL} = \left(\frac{K_{l-p(lin)}}{K_{s-p(sat)}}\frac{2}{\alpha_{n(sat)}}\right)^{\frac{1}{\alpha_{n(sat)-1}}} \left(\left|-V_{DD} - V_{TH_{p(lin)}}\right|\right)^{\frac{\alpha_{p(lin)}}{2\left(\alpha_{n(sat)-1}\right)}} + V_{TH\_n(sat)} -$$

$$\frac{K_{s-p(sat)}\left(\left|-V_{DD} - V_{TH\_p(sat)}\right|\right)^{\alpha\_p(sat)}}{K_{l-p(lin)}\left(V_{IH} - V_{TH\_n(lin)}\right)^{\alpha\_n(lin)/2}} \tag{5.12}$$

Where V_{IL} is the maximum, input voltage level is recognized as logical '0', V_{IH} is the minimum, input voltage level is recognized as logical '1', V_{OL} is the maximum logical '0' output voltage, and V_{OH} is the minimum logical '1' output voltage. Therefore, the required SNM expression can be defined as:

$$V_{OH} = -\frac{K_{s-n(sat)}(V_{IL} - V_{TH\_n(sat)})^{\alpha\_n(sat)}}{K_{l-p(lin)}(|-V_{DD} - V_{TH\_p(lin)}|)^{\alpha\_n(lin)/2}} + V_{DD} \quad (5.13)$$

$$V_{IL} = \left(\frac{K_{l-p(lin)}}{K_{s-n(sat)}}\frac{1}{\alpha_{n(sat)}}\right)^{\frac{1}{\alpha_{n(sat)}-1}} \left(|-V_{DD} - V_{TH\_p(lin)}|\right)^{\frac{\alpha_{p(lin)}}{2(\alpha_{n(lin)}-1)}} + V_{TH\_n(sat)} \quad (5.14)$$

$$V_{OL} = \frac{K_{s-p(sat)}(|-V_{DD} - V_{TH\_p(sat)}|)^{\alpha\_p(sat)}}{K_{l-n(lin)}(V_{IH} - V_{TH\_p(lin)})^{\alpha\_n(lin)/2}} \quad (5.15)$$

$$V_{IH} = \left(\frac{K_{l-p(lin)}}{K_{s-p(sat)}}\frac{2}{\alpha_{n(sat)}}\right)^{\frac{-2}{\alpha_{n(sat)}+2}} \left(|-V_{DD} - V_{TH_{p\_(sat)}}|\right)^{\frac{2\alpha_{p(sat)}}{\alpha_{n(lin)}+2}} + V_{TH\_n(lin)} \quad (5.16)$$

$$SNM = \sqrt{(NM_H{}^2) + (NM_L{}^2)} \quad (5.17)$$

As shown in figure 5.4, the SNM of 7T SRAM cell during read operation is 520mV.

5.6.2 Write Static Noise Margin (WSNM)

WSNM implies the write stability of any SRAM during the operation. It is one of the different SRAM's cell design metrics.

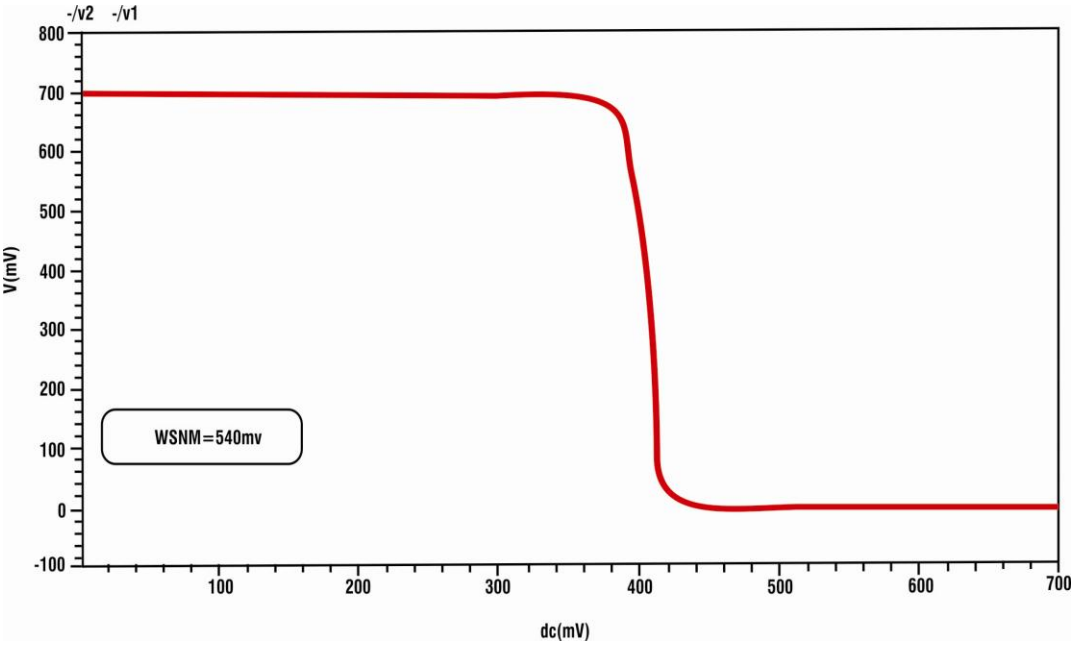


Figure 5.5 Write SNM of 7T SRAM Cell

It is a measure of an ability of an SRAM cell to pull down the node which stores '1' to a voltage which is less than the switching threshold voltage of the inverter which stores '0'.

It means WSNM measured during '1' is written from the simulation. As shown in figure 5.5, the SNM of 7T SRAM during write operation is 545 mV.

5.7 SIMULATION RESULT

In this study, proper simulations on the 7T SRAM cell were done and were calculated. As shown in table (5.1), the leakage currents of 7T SRAM cell design are 1.154pA and 13.139pA. It appears that SNM decreases with decreasing voltage supply. However, if a time limit is set (word-line is active only for a finite amount of time), the SNM increases as voltage supply decreases. This is because at a lower voltage supply, the current drawn from the BL is smaller during '0' read. Therefore, whatever is the charge stored at storing node, it will be less, thus lower voltage at storing node is reached after some delay which means increase in the static noise margin before the cell state is changed.

SRAM CELL/SNM	RSNM (mv)	WSNM (mv)
7T SRAM CELL	520	545

Table - 5.2 Read SNM and Write SNM of 7T SRAM Cell

5.8 SUMMARY OF THE CHAPTER

In this research, a process variation method is presented to improve the characteristics of leakage current and increase the stability of the proposed SRAM. With the help of process variation method, better outcomes have been achieved compared to without process variation. The value of gate leakage current and sub-threshold current after process variation are 1.154pA and 13.139pA. A 7T SRAM cell with higher SNM and higher speed at a supply

voltage less than 0.7V was presented. The value of read and write SNM is 520 mv and 545 mv respectively.

CHAPTER 6
DESIGN OF SRAM CELL BASED MEMORY ARRAY IN NANO-SCALED TECHNOLOGY

6.1 INTRODUCTION

In this chapter, the aim is to reduce the read time as well as to increase the SNM and stability of the SRAM cell during read operation. A different 7T cell with single bit-line is proposed to increase the SNM and stability within the memory core. A 4 X 4 array is constructed using single ended 7T cell to show the feasibility of the proposed SRAM cell. A 16 Bit SRAM operating at a supply voltage of 1V is demonstrated in 45 nm process technology. Its total power consumption is reduced by more than 90% as against the conventional design. This 7T cell has a lower leakage current due to the single-bit-line and transmission gate at feedback. As a result, it is suitable for low power consumption application especially for battery operated gadgets.

6.2 SRAM MEMORY

SRAM memory cell array normally occupies around 40% of logic LSI nowadays, so that the nature of logic LSI such as operating speed, power, supply voltage and chip size is limited by the characteristics of SRAM memory array [112]. Therefore, the good design of SRAM cell and SRAM cell array is inevitable to obtain the high performance, low power [132], low cost and reliable logic LSI. The SRAM cell array must operate at low voltages operation to reduce the operating power. It must retain data with low leakage at standby mode. Many low power techniques for obtaining low power SRAM have been proposed. SRAM cell array design also plays an important role in reducing the power consumption. Large SRAM arrays are widely used as cache memory in microprocessors and the application-specific integrated circuits can

occupy a significant portion of the die area [119]. In an attempt to optimize the performance/cost ratio of such chips, designers have faced so much dilemma. Large arrays of fast SRAM help to boost the system performance. However, the area impact of incorporating the large SRAM arrays into a chip directly converts it into a higher cost chip. Balancing these requirements drive, the effort is to minimize the footprint of SRAM cells. As a result, millions of minimum-size SRAM cells are tightly packed making SRAM arrays the thickest circuitry on a chip. Such areas on the chip can be especially susceptible and sensitive to the manufacturing defects and process variations. Conventional symmetric 6-transistor (6T) SRAM failed to perform the reliable operation in sub-threshold region because of read current disturbance inducing the Static Noise Margin (SNM) degradation [118].

Figure 6.1 shows the basic SRAM block structure for 16 bit array which is designed in Cadence Virtuoso software. A row decoder gated by an appropriate timing block signal decodes 4 row address bits and selects one of the word lines WL 0–WL 4. The SRAM core consists of a number of arrays of NXM, where N is the number of rows and M is the number of bits. SRAM core is organized as a number of arrays in a page manner which requires an additional column-decoder to select the accessed bits. The figure shows an illustration of an SRAM with four pages of 4x4 arrays with the corresponding I/O blocks. SRAMs can be organized as either bit-oriented or word-oriented. In a bit-oriented SRAM, each address accesses a single bit, whereas in a word-oriented memory, each address directs a word of *n* bits (where the popular values of *n* include 8, 16, 32 or 64). Column decoders are directed by 4 address bits that allow the sharing of a single sense amplifier among 2, 4 or more columns. The majority of modern SRAMs are self-timed i.e., all the internal timings are generated by the timing block within an SRAM instantaneously, which are internally given with inputs. An

additional Chip Select (CS) signal introducing an extra decoding hierarchical level can often be provided in multi-SRAM chip architectures [52].

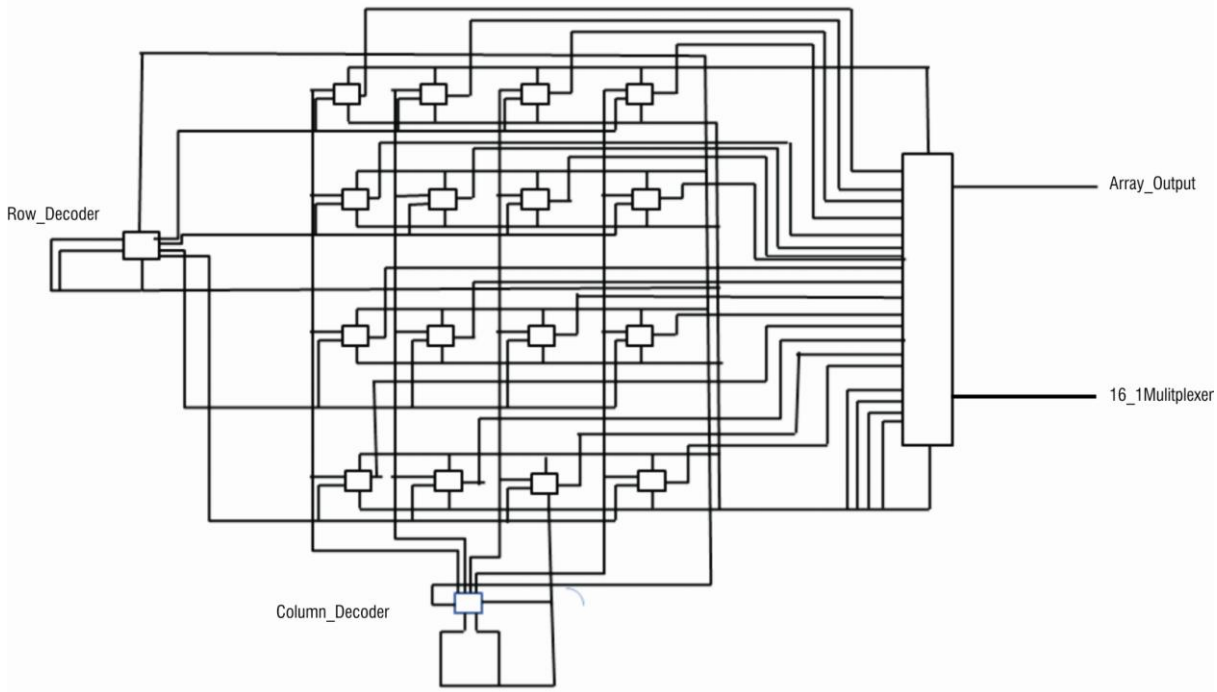


Figure 6.1-16-bit SRAM Array

6.3 DESIGN OF SEVEN-TRANSISTOR (7T) SRAM ARRAY

6.3.1 SRAM Topologies

As a major memory component, SRAMs occupy large area and dissipate high energy in system-on chips (SoCs). In the near-threshold or sub-threshold region, conventional 6T SRAMs are not reliable due to severely degraded cell stability including half-selected problem.

Decoupled SRAM cells have been verified to work in the sub-threshold or near-threshold region. While decoupled SRAM cells improve the cell stability substantially during read operation, the stability of the half-selected cells is still a challenging issue. Pulsed word lines and hierarchical bit lines mitigate the stability degradation of the half-selected cells, but they degrade the write margin, demanding write margin improvement techniques Therefore,

design parameters and assisting circuits have to be carefully selected by tradeoffs. In ultra-low voltage SRAMs, leakage current occupies a substantial percentage of power and energy. Thus, energy aware leakage reduction is also important for the better energy efficiency.

The Seven-transistor (7T) SRAM cell topologies, the extra one transistor are used to increase the read/write stability under large variations. There are four circuit topologies of 7T SRAM cell for low power application.

6.3.1.1 Novel Basic 7T SRAM cell

The proposed 7T SRAM cell and its operation is depicted in Fig. 6.2(a). Higher-Vth devices are employed in the pull-up PMOS transistors (P1 and P2) to improve stability and reduce leakage. A single-ended 1T read port is proposed for minimizing the area overhead. This is achieved by removing the read access transistor in the traditional 8T SRAM cell [120].

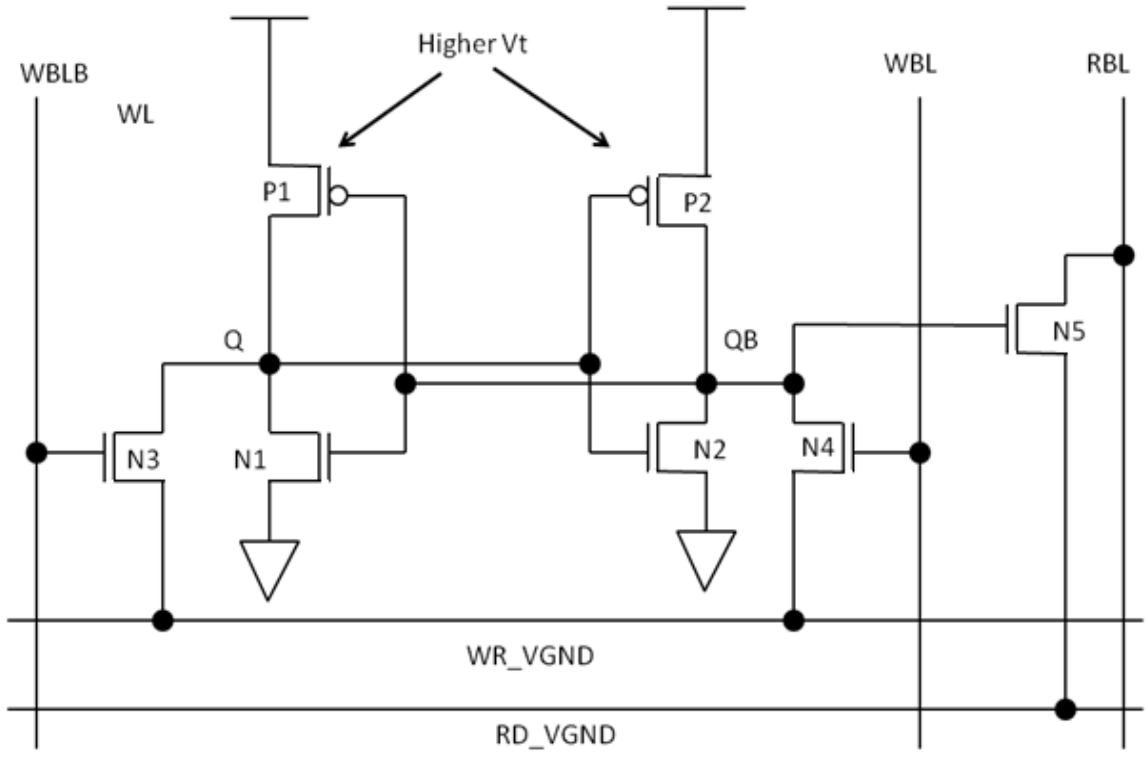


Figure 6.2(a) - Basic 7T SRAM cell

When read is enabled (RD_VGND = GND), the read bit line (RBL) is pre-charged which was earlier conditionally discharged by QB. When QB = ‘1’, the pull-down cell current fights with the pull-up leakage current from unselected RD_VGNDs through N5, it results in DC offset at storing node ‘0’. However, near threshold region, the DC offset imposes body effect on N5 in unselected rows and N5 starts to operate in the sub-threshold region. With this, the RBL swing becomes large enough to be sensed without needing the access devices. [121]. During non-read cycles, RD_VGND and RBL are held to VDD, thus eliminating the bit line leakage through N5. Write operation starts by applying WR_VGND at GND and then loading write data at write bit lines (WBL and WBLB). Either of the N3 or N4 will be storing ‘0’ into the selected node.

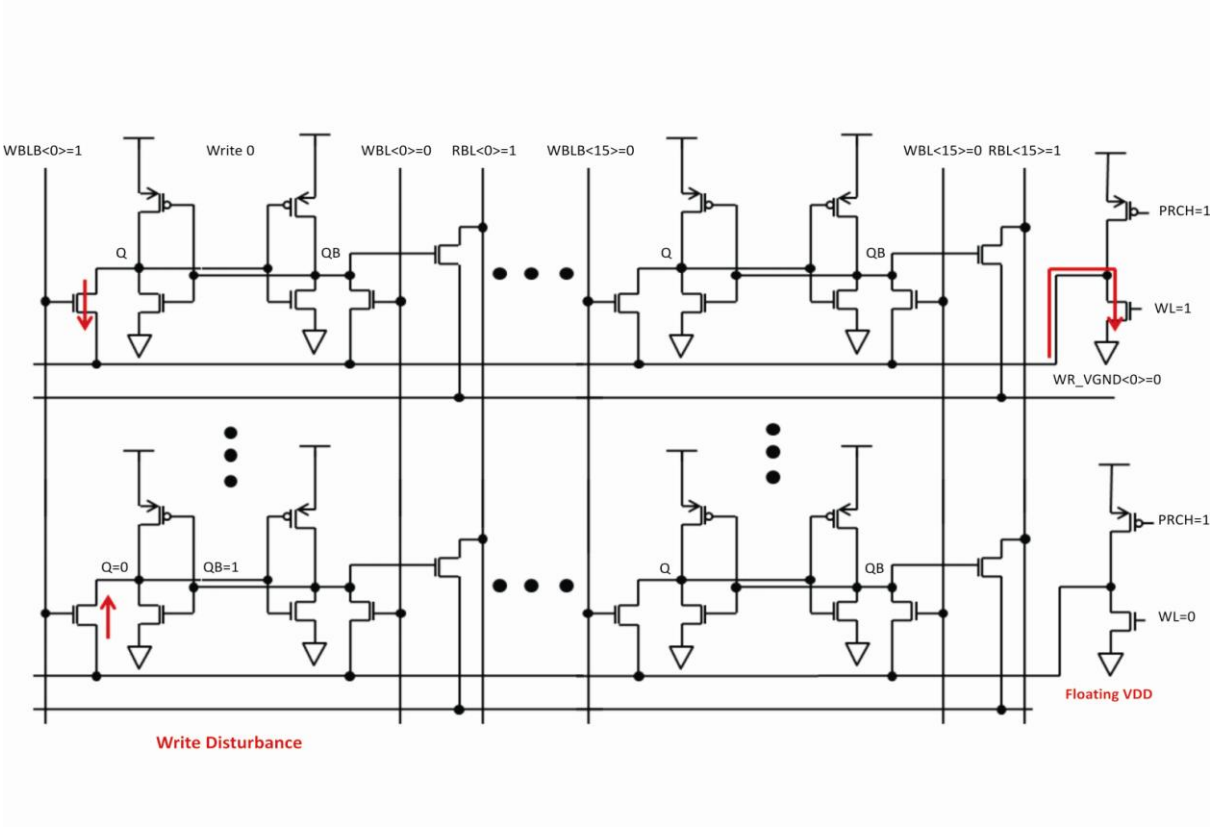


Figure 6.2(b) - Basic 7T SRAM cell array

In unselected rows due to pre-charging at VDD, WR_VGND becomes floating. Due to this floating, disturbing current starts flowing for a short time. This is one of the reasons that both WBL and WBLB are GND in unselected columns to prevent the conventional half-select issue [122-123].

Write Through Virtual Ground Scheme

In the proposed SRAM array, the unselected cells in the selected row are free from disturbing current due to grounded WBLs/WBLBs. But the selected column still has a disturbing condition as shown in Fig. 6.2(b). For example, when write operation is executed, cell located at the first row and the first column, WR_VGND<0>, is grounded while other WR_VGNDs are all floating. The write driver loads data '0' to the first column, making WBL<0> = '0' and WBLB<0> = '1'. Q becomes '0' along the WBLB<0>. With this, disturbing current starts flowing from floating WR_VGND (e.g. WR_VGND<255>) to Q node (Fig. 6.2(b)).

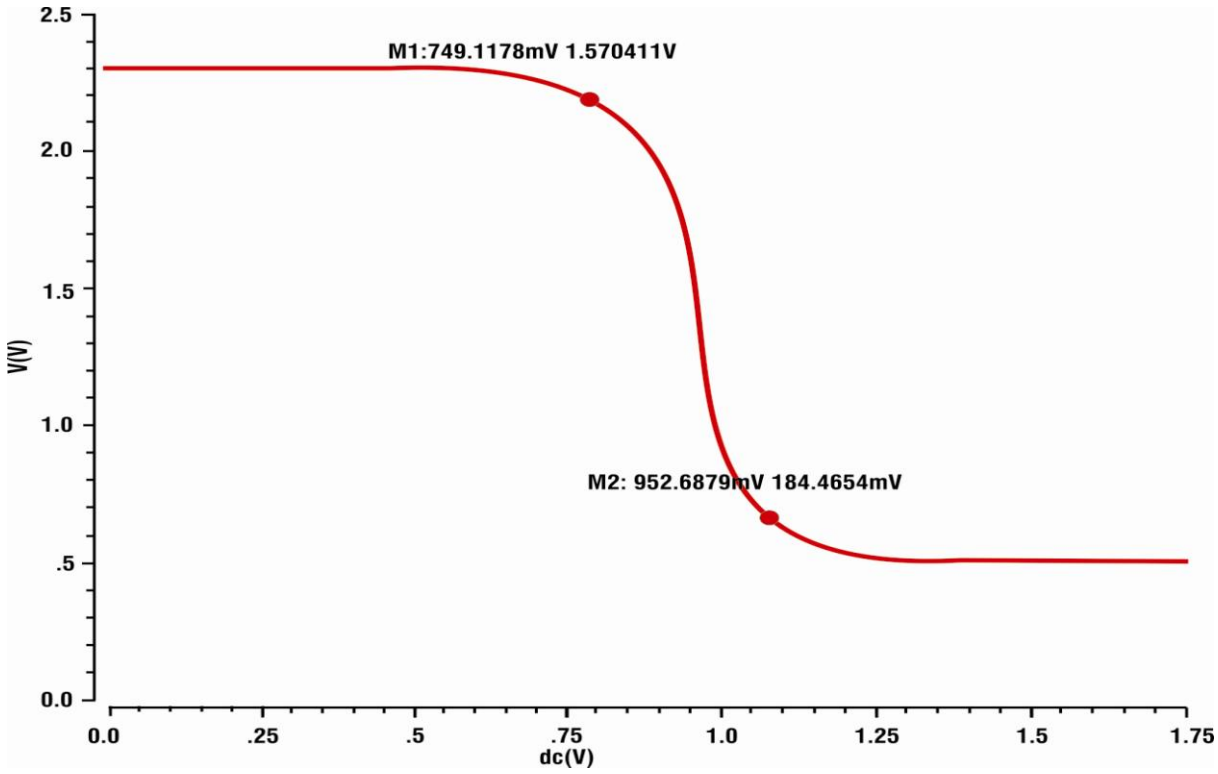


Figure 6.2 (c)- 7T SRAM cell Stability during read cycle

However, if compared to 8T SRAM cells, the write disturbance in the proposed cell is remarkably ameliorated due to smaller parasitic capacitance. This is because conventional 8T write disturbance is determined by capacitance at WBL/WBLB while the proposed SRAM depends on the capacitance at WR_VGND [124-125].

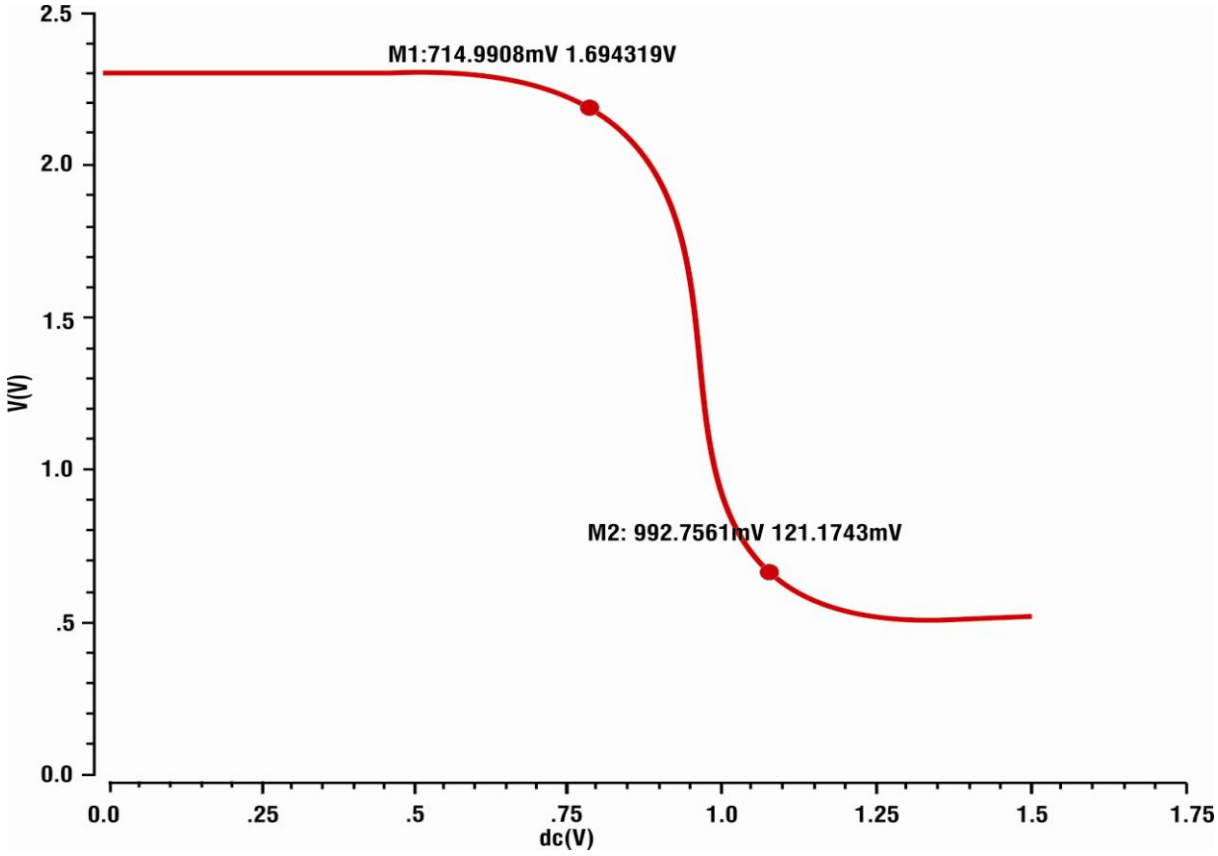


Figure 6.2(d)- 7T SRAM cell Stability during write cycle

Since the number of devices connected to WR_VGND is much smaller than that of conventional bit lines, this is why floating WR_VGNDs quickly discharges and accordingly improves the cell stability as illustrated in Fig. 6.2(c) and fig. 6.2(d). Similarly fig 6.2 (e) shows the HSSNM curve for the 7T SRAM cell.

Calculation for Stability of 7T SRAM cell

$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

$$\text{HSSNM} = \sqrt{(\text{NM}_\text{H}{}^2) + (\text{NM}_\text{L}{}^2)}$$

$$\text{HSSNM} = \sqrt{(204)^2 + (278)^2}$$

$$\text{HSSNM} = \sqrt{(41616) + (77284)}$$

$$\text{HSSNM} = \sqrt{118900}$$

HSSNM=345 mV

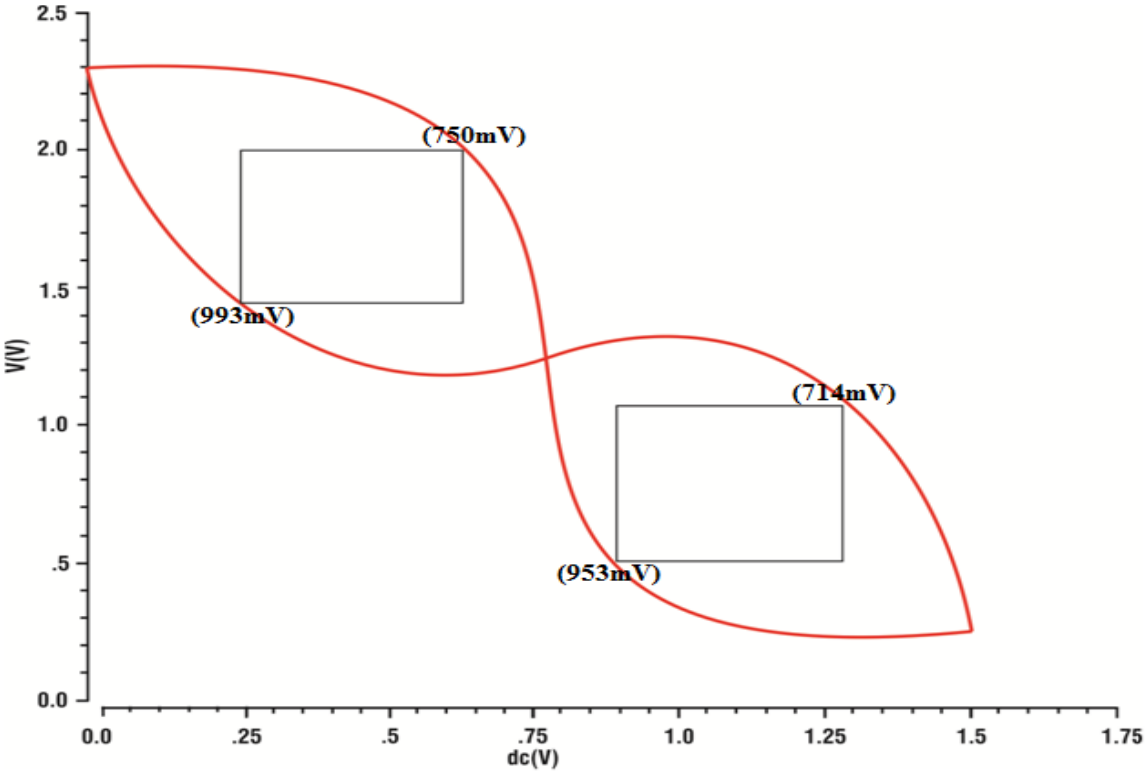


Figure 6.2 (e)- HS-SNM for 7T SRAM cell

6.3.1.2 Gated ground 7T SRAM cell

A gated ground 7T SRAM cell provides a high read stability. Figure 6.3 shows a proposed cell. The reading and writing paths of the cell are independent of each other and they never interfere mutually. Transistors N1 and N2 form a latch and hold the data. The transistors N3, N4 and N5 are read access transistors and PMOS transistors P1 and P2 are write-access transistors [14].

BL and BLB charge and discharge to write ‘1’ to the storage node V_Q and ‘0’ to V_{QB} respectively. The word-line write WL_W is set ‘low’ to turn transistor P1 and P2 ‘on’, while word-line right WL_R is maintained at a low voltage to keep N5 in ‘off’ state. For writing‘1’, V_Q is charged up to high-level by BL through P1, while BLB discharges V_{QB} to low-level through P2.

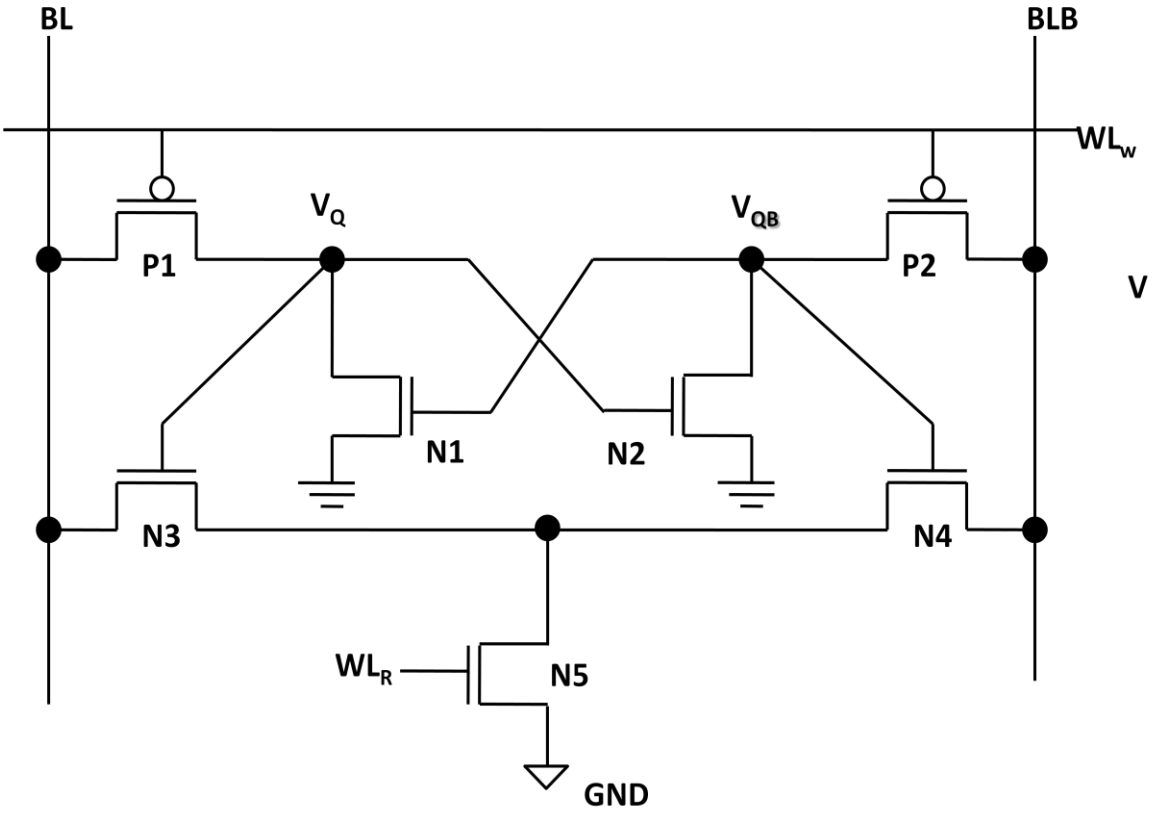


Figure 6.3-Gated ground7T SRAM cell

When V_Q charges sufficiently, word-line WL_W is set to ‘high’ state and then P1 and P2 are turned to ‘off’ state. In contrast, to write ‘0’to the node V_Q and ‘1’ to V_{QB}, BL and BLB discharge and charge respectively.

During the read operation, the storage nodes V_Q and V_{QB} completely decouple the datum from the BL. When WL_W is set to ‘high’, it puts the transistors P1 and P2 in ‘off’ state and V_Q stores ‘1’, while WL_R is maintained at a high voltage to keep N5 ‘on’. BL then discharges

through N3 and N5. On the other side, BLB remains high as N4 insulates BLB from the GND. In gated ground 7T SRAM cell, the read path is separated from the write path. Data in read operation does not interfere with the storage node which is closely maintained at the ground level during read operation.Thus, the 7T SRAM cell has higher endurance against the external noise [14].

6.3.1.3. SOI-7T-SRAM with Look Ahead Body-Biasing Word/Bit Line Signals

Adopting active body-biasing control on PD-SOI in SOI-7T-SRAM cell, V_{th} of each transistor can be dynamically controlled through a direct body contact.

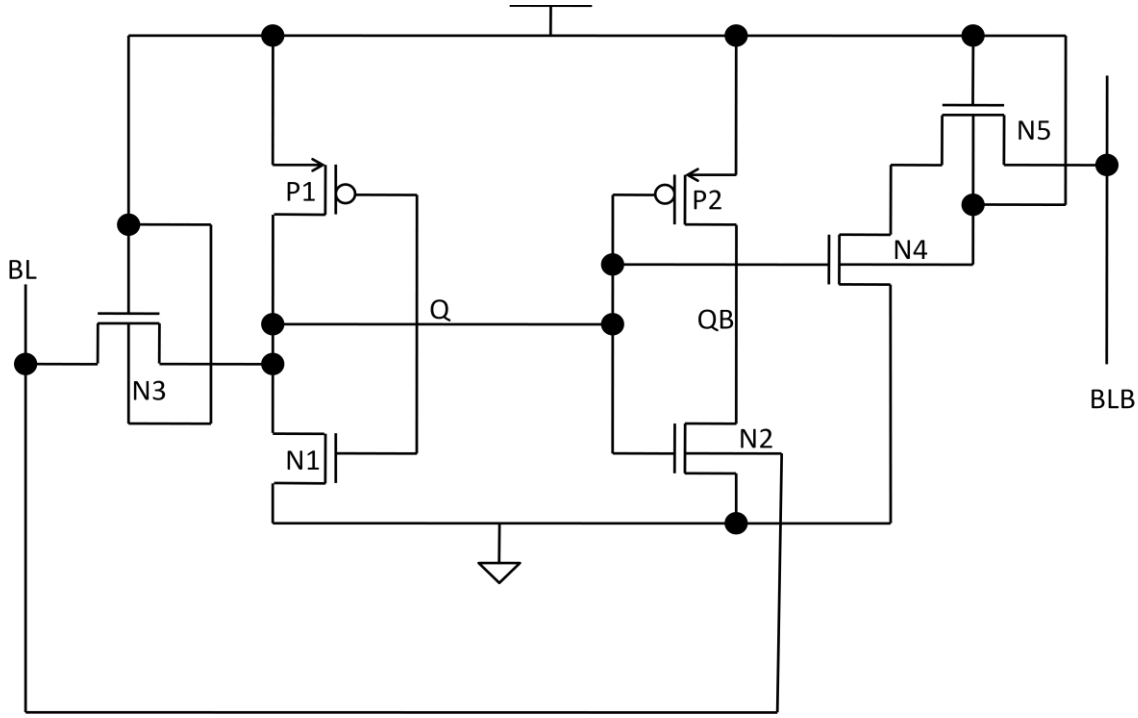


Figure 6.4-Schematic of SOI-7T-SRAM with Look-Ahead Body-Biasing with Word / Bit Line Signals

As shown in figure 6.4, in this type of 7T SRAM cell topology, the write and read word-lines (WWL and RWL) control the body access transistors and the driver transistor. The write bit-line (WBL) provides the body-bias for INV (R).Here, the body voltage of PMOS and NMOS in INV (L) is fixed to VDD and GND, respectively, which corresponds to the zero body bias. In write '0' operation, the V_{th} of PMOS(P1) in INV (R) is set to low by the forward body-bias

when WBL is equal to ‘low’ which accelerates the charging speed of node V_2. In addition, during the write‘1’ operation where the WBL is equal to ‘high’, the V_{th} of NMOS goes to a ‘low’ state. Hence, discharge current from node V_2 increases. Namely, the V_{th} of PMOS and NMOS in INV(R) can be controlled by the write data of WBL, before hand, in order to assist the write operation. Moreover, the body bias employing the WWL and RWL improves the read and write current owing to lower V_{th} of access and driver transistor which, therefore, shortens the access time in both read and write operations.

6.3.1.4 Single ended 7T SRAM Cell

In single ended, 7T SRAM cell, as shown in figure 6.5, the word-line is asserted high, prior to the read and write operations similar to the standard 6-transistor SRAM cell [133].

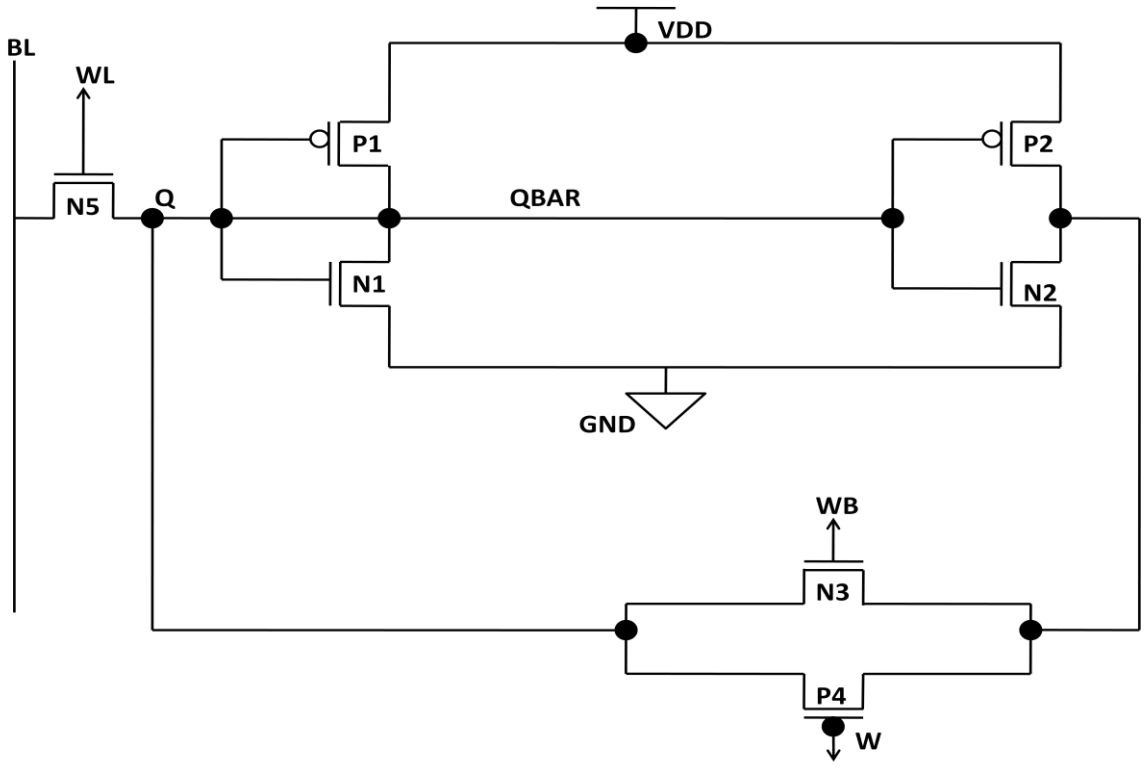


Figure 6.5-Schematic of Single ended 7T SRAM cell

In the hold mode, transmission gate provides a strong feedback to the cross coupled inverters, and the word-line (WL) is set to a ‘low’ state. In order to read a value, when WL and BL are

in ‘high’ state, Q node is set to‘1’and corresponding NMOS goes in ‘off’ state, carrying the gate-oxide leakage current and sub-threshold leakage current. When Q_b is ‘0’, the PMOS and NMOS transistors are in ‘on’ state. These transistors keep dynamic current along with gate oxide leakage current. To write ‘0’ on the SRAM cell, Q is set to‘0’, the bit-line to‘0’ and WL is precharged to level ‘1’.

The corresponding transistor reaches the ‘on’ state so that it keeps both dynamic as well as gate oxide currents. Other PMOS and NMOS transistors now conduct sub-threshold leakage and gate-oxide leakage current as they are in ‘off’ state [129].

Figure 6.6 shows the layout of 7 transistors SRAM cell in 45 nm technology. In this figure, three transistors are PMOS and remaining four transistors are NMOS. Blue coloured lines are for metal 1 and yellow lines are for polysilicon. In the above figure, horizontal line is used for power supply and bottom horizontal line is for ground terminal. Metal 1 and poly is joined by via (metal1-poly).

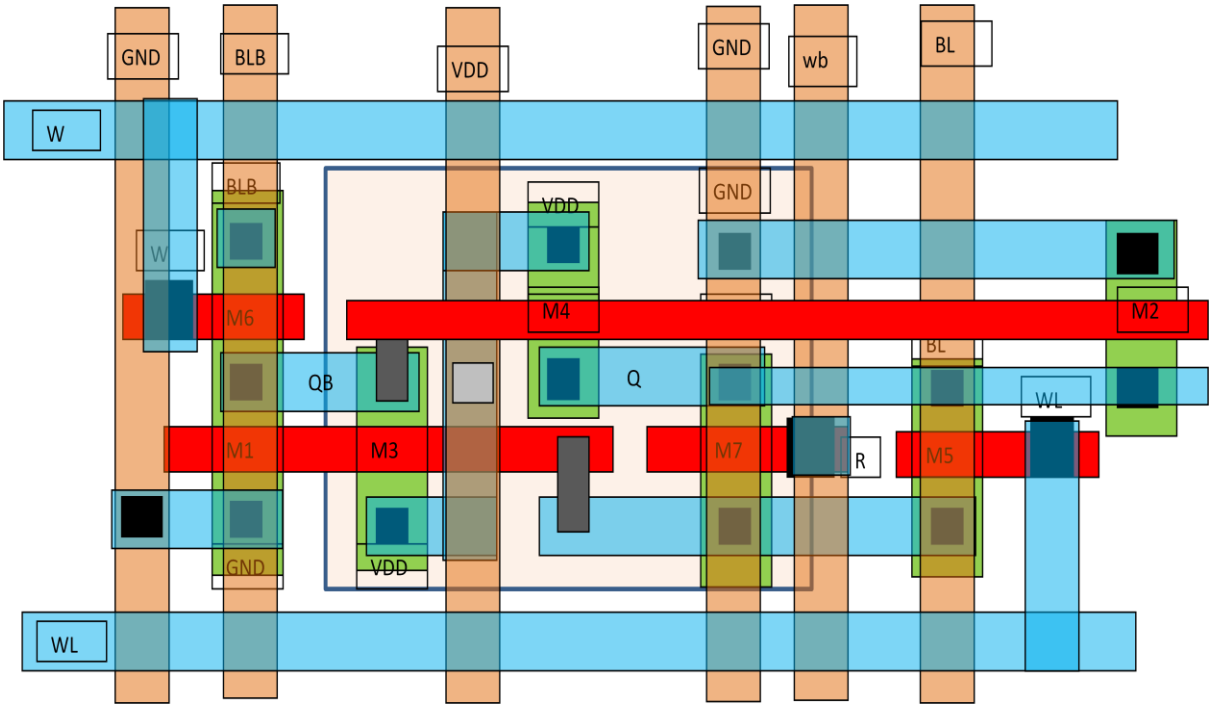


Figure 6.6- Layout of 7T SRAM Cell

The area in 45 nm technology is very less as compared to 180 nm technology. Here minimum width of metal 1 is 65 nm. We cannot take the width of metal 1 less than 65nm. And metal 1 to metal 1 spacing should be greater than 65 nm. The width of poly should be greater than 50 nm. The width of via should be greater than 65 nm. The minimum spacing between via and via should be greater than 75 nm.

6.3.2 Sense Amplifier

The read access time of SRAM is a vital performance parameter. Furthermore, the sense amplifier delay usually becomes a bottleneck for read access time in SRAM. The sensing and amplifying of the data signal transmitted through a memory cell to a bit-line are the most important functions of a sense amplifier. However, to sense the data correctly and swiftly, it becomes more and more difficult when the working voltage scales down with the gate oxide thickness. Because the bit-lines are always loaded with a large number of memory cells, the loading of bit-lines is usually pretty large [115]. Thus, the signal swing distributed on bit-line will be on inverse ratio of the loading of bit-line (about 50mV~200mV). So, the sensing delay becomes one of the threatening elements of memory read access time. With a decrease in working voltage, the input signal swing of sense amplifier is becoming smaller. This result leads to a challenge for sense amplifiers to work at lower operating voltages [116].

Generally, the parameters characterizing a sense amplifier include:-

(I) Gain A= V_{out}/Vin,

(II) Sensitivity S= V_{in_min} – minimum detectable signal,

(III) Offset V_{offset} and I_{offset} – the difference at outputs with the common mode signal at the inputs,

(IV) Common Mode Rejection Ratio CMRR=A_{diff}/Acm ration of amplification for a differential and a common mode signals,

(V) Rise time $t_{rise,}$ fall time t_{fall} – 10% to 90% of the signal transient,

(VI) Sense delay $t_{sense} = t_{50\%\_WL} - t_{50\%\_Vout.}$,

(VII) Where $t_{50\%\_WL}$ -the 50% point of the word-line enables signal and $t_{50\%\_Vout}$ -the 50% point of SA output is transient.

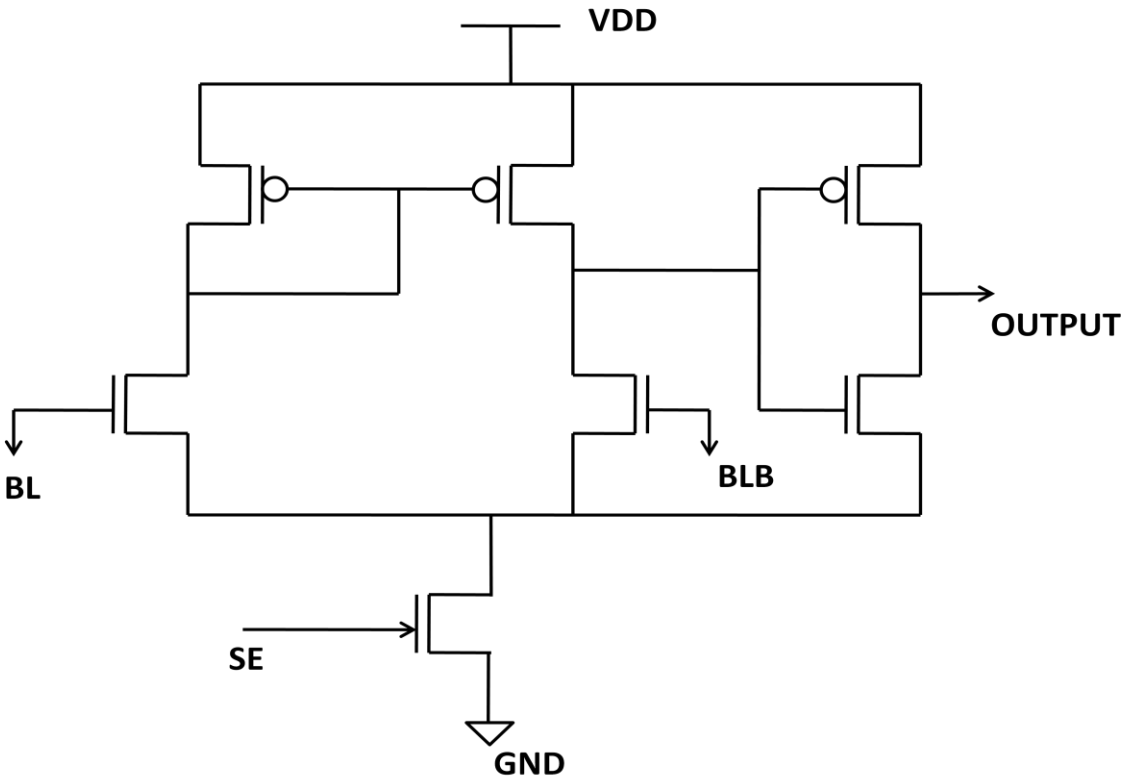
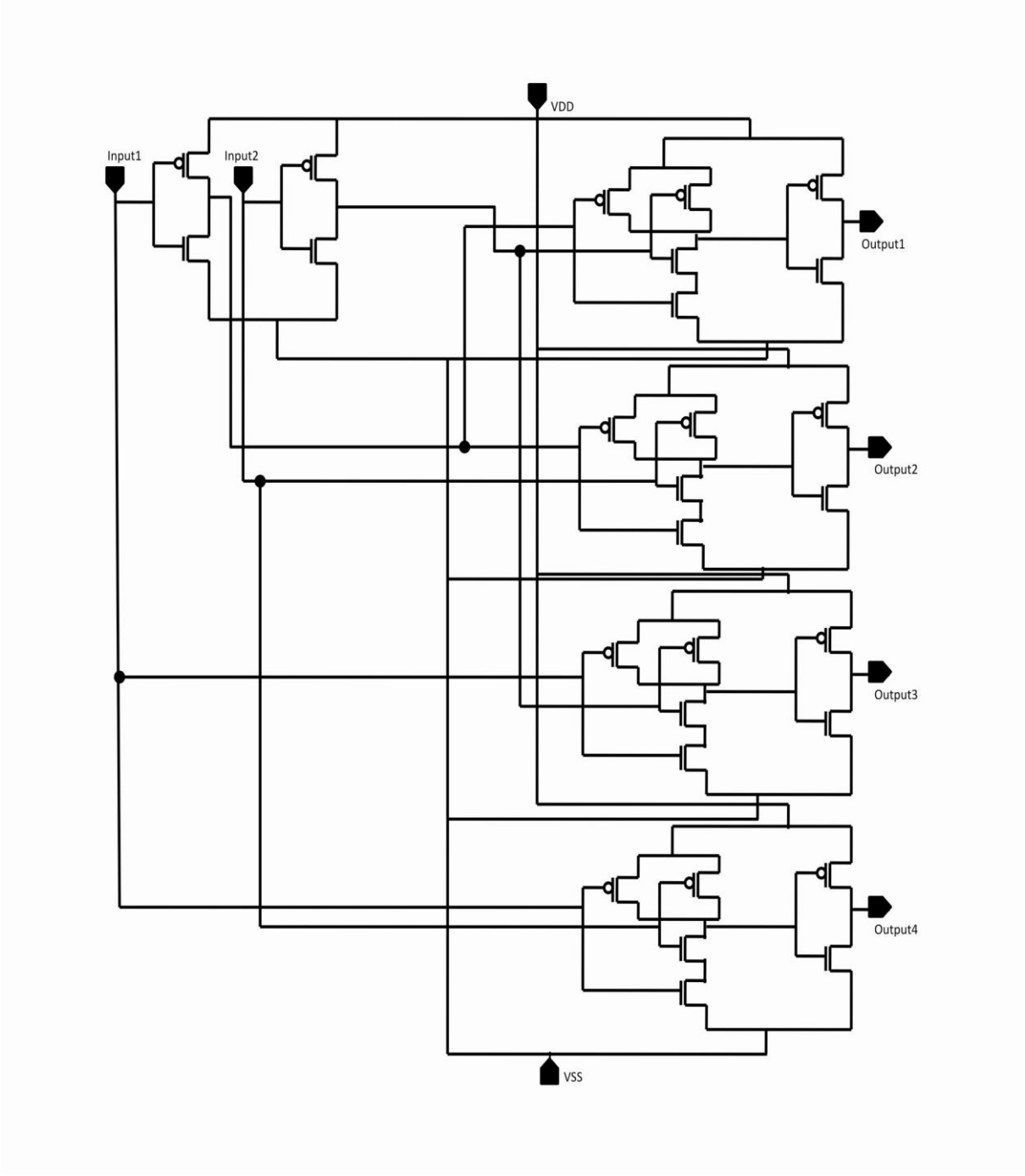


Figure 6.7-Sense amplifier

6.3.3 Decoder

The designed 2:4 decoder is shown in figure 6.8 (a) and (b). The INV and NAND parts of the circuit have been presented which are used in this work as the building blocks of the 2:4 decoder.



6.8 (a)- Schematic of 2:4 decoder

The outputs are taken from the corresponding output islands of each NAND gate, D0, D1, D2 and D3 respectively.

Equation for 2:4 Decoder is:-

D0 = A’B (6.1)

D1 = A’B (6.2)

D2 = AB’ (6.3)

D3 = AB (6.4)

The presence of a positive charge on one of these islands corresponds to the logic ‘1’, whereas the absence of positive charge corresponds to logic ‘0’. The two inverters produce the complementary of the inputs and each of the four NAND gates produces the maxterms. As shown, the outputs are independent which means that only one output is equal to 1 at an instant time. The output line which is equal to 1 symbolizes a maxterm which corresponds to the binary number in the output line

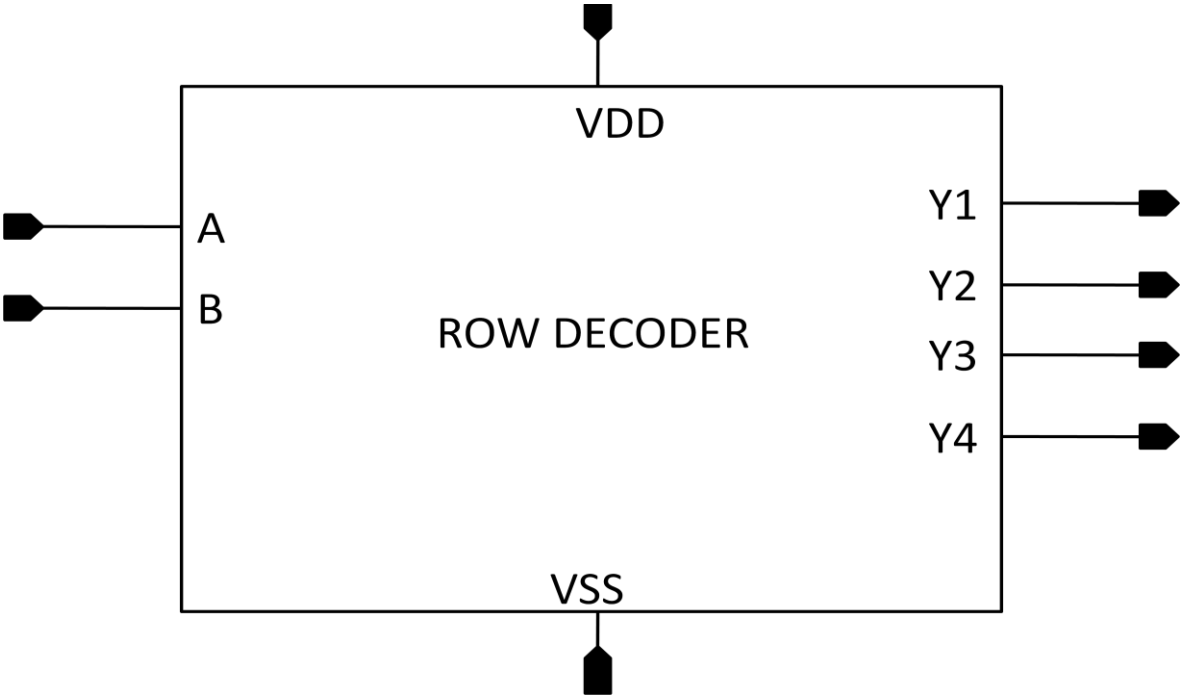


Figure 6.8 (b)-2:4 Decoder

Hence, the circuit operation is complete [128]. The input/output waveforms of the Row Decoder are shown in figure 6.9.

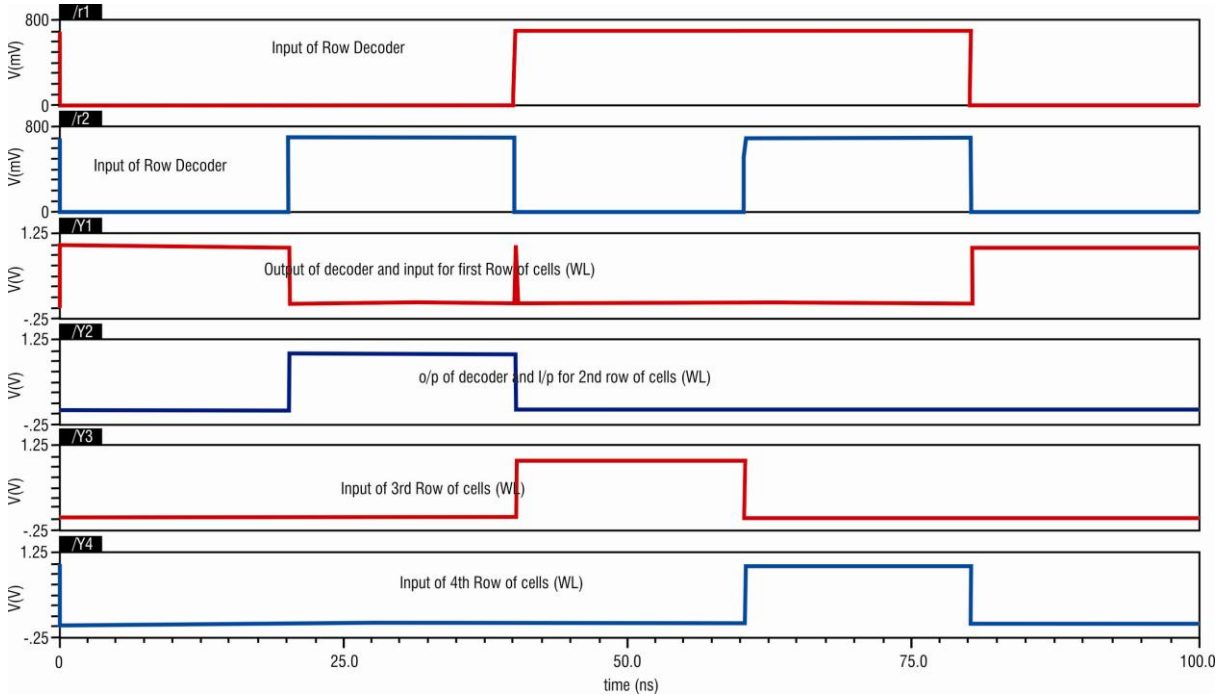


Figure 6.9- Input/output Waveforms of Row decoder

The input/output waveforms of Column Decoder are shown in figure 6.10. At particular selection of the column decoder, the output waveform will be displayed in the figure.

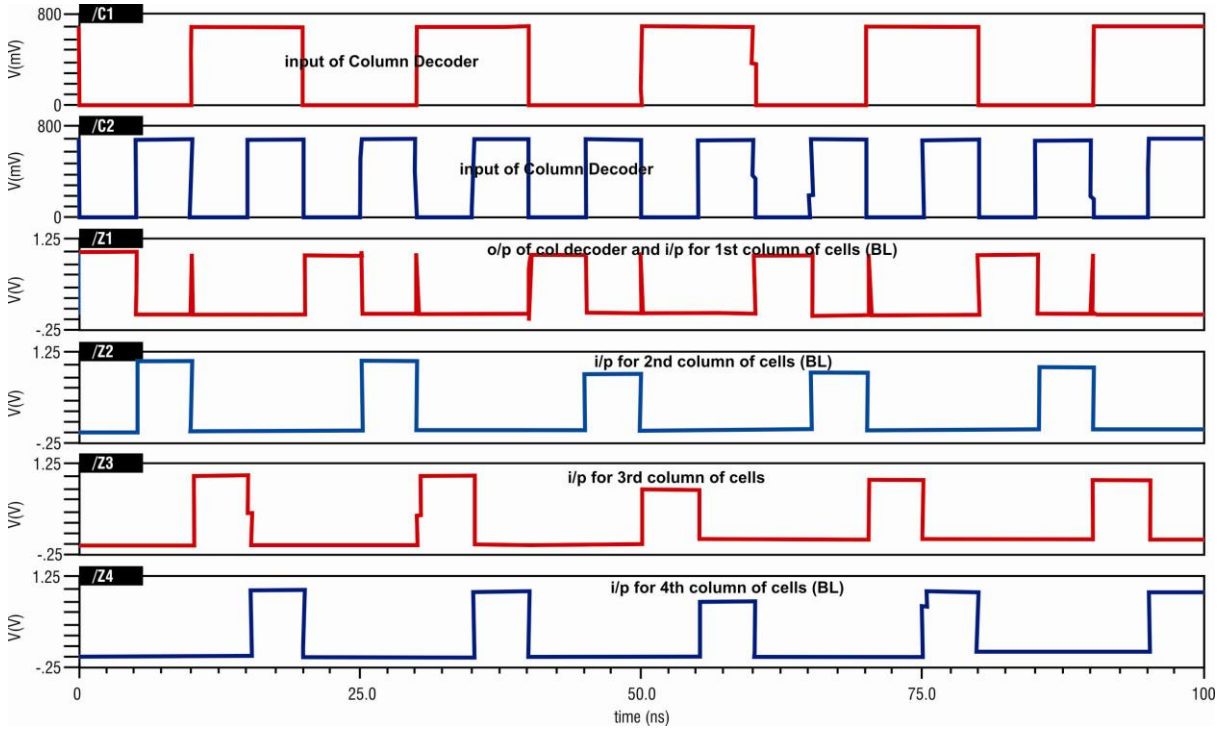


Figure 6.10- Input/output Waveforms of column decoder

6.3.4 Multiplexer

A multiplexer is a combinational circuit that selects binary information from one of the many input lines and directs it to a single output line.

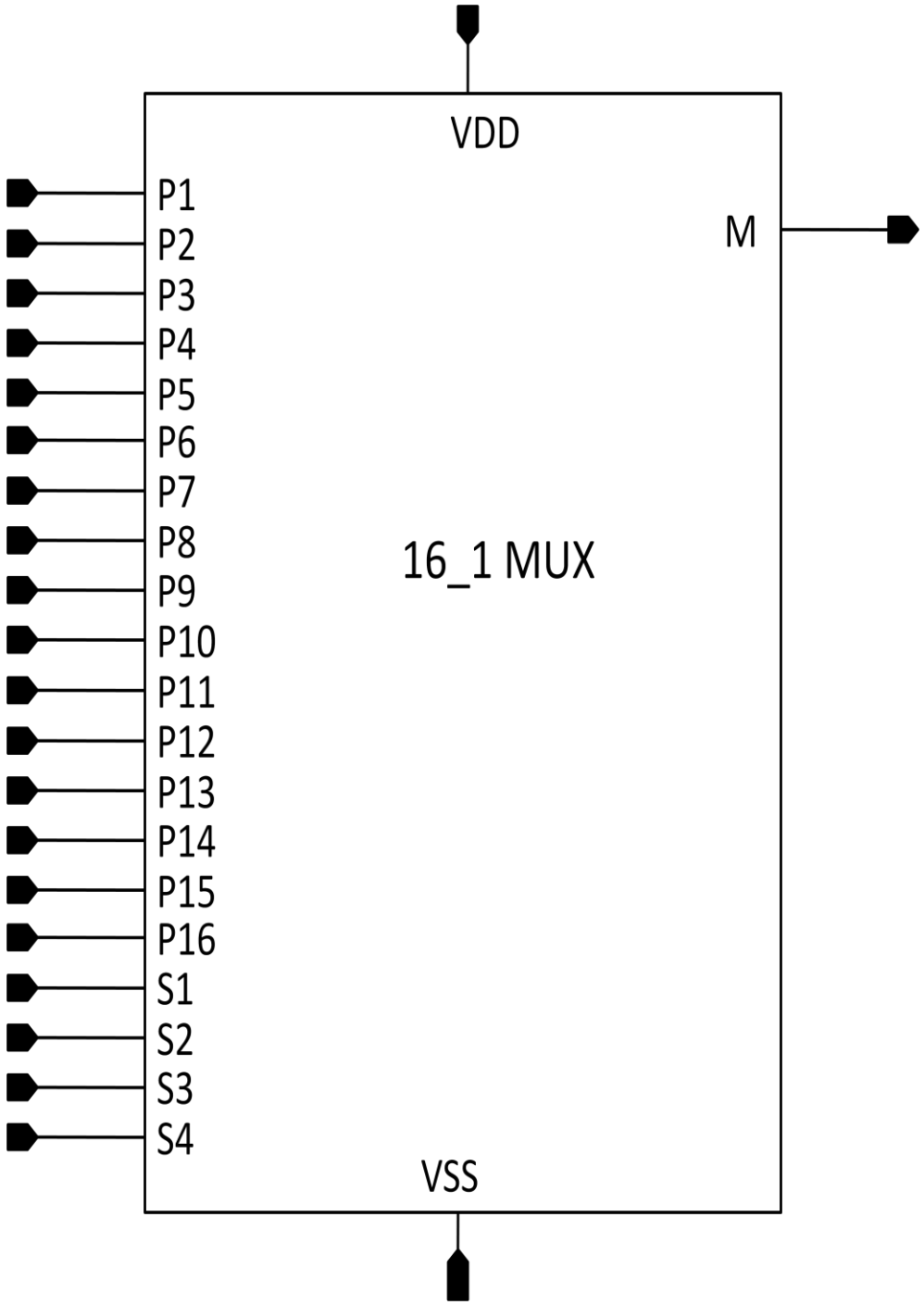


Figure 6.11 -Symbol of 16:1 multiplexer

The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^N input lines and N selection lines whose bit combination determines input node [115]. I have designed a 16X1 multiplexer in our circuit. A 16X1 multiplexer is a combinational circuit that uses four select lines (S1, S2, S3 and S4) to connect one of sixteen input data lines (output of cells) to a single output (Y). Only one of the input data lines can be produced at the output of the multiplexer at any given instance [127].

Multiplexer gets the output of each cell as 16 inputs, so that the operation it provides is an appropriate output (M) as shown in figure 6.11.

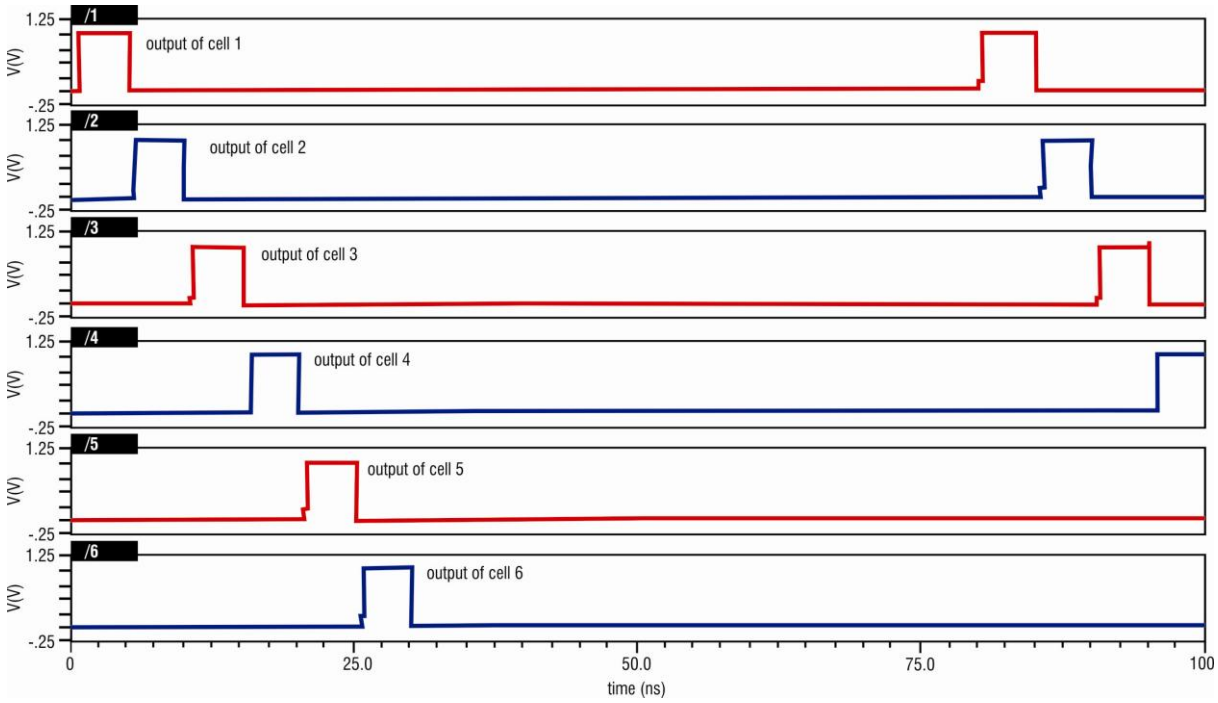


Figure 6.12(a)-Output of individual Cell

Every time one of the cells is selected according to the select line (cell 1, cell 2 and so on) and Multiplexer produces the output corresponding to the selected cell at all times.

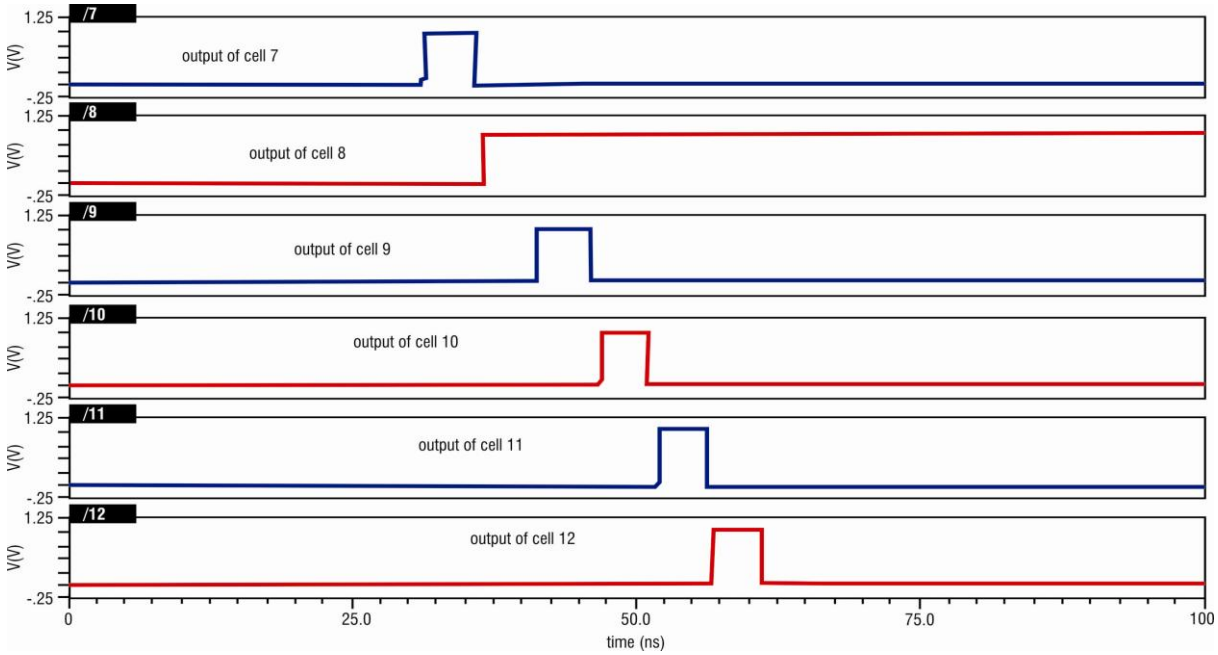


Figure 6.12 (b)-Output of individual Cell

Figure 6.12- (a), (b) and (c) show the output of individual cells according to decoder and fed to the multiplexer for the output.

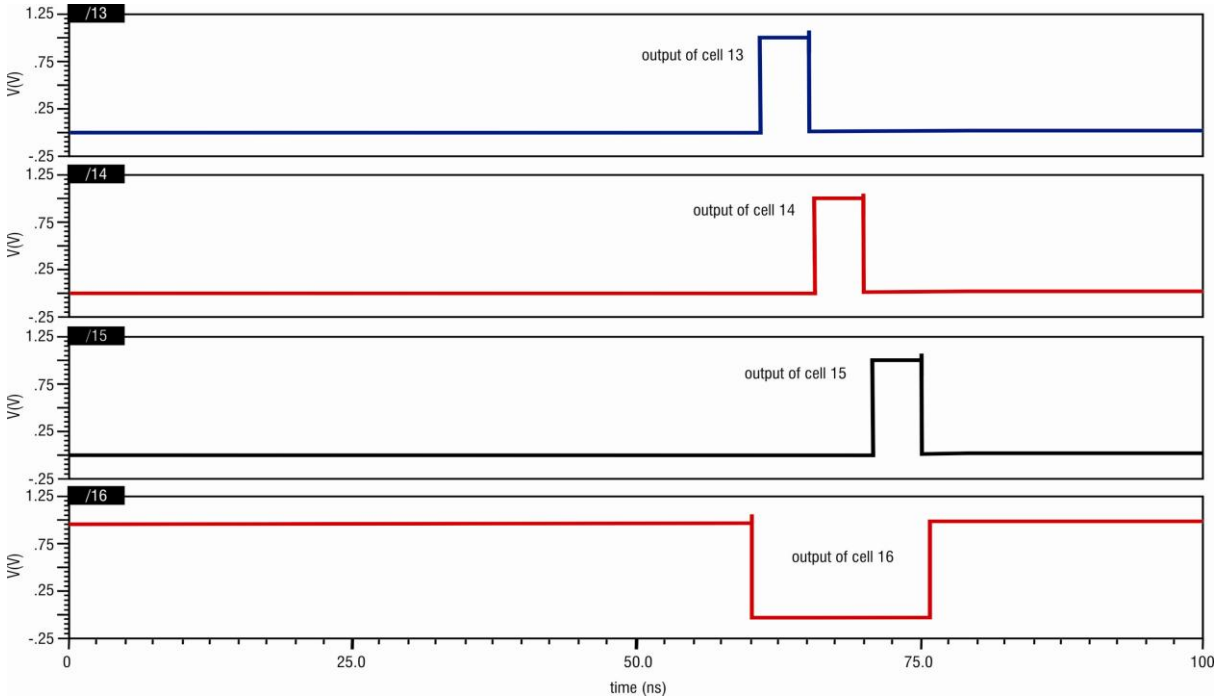


Figure 6.12(c)-Output of individual Cell

Figure 6.13 shows select lines and the corresponding output of a 16 bit array.

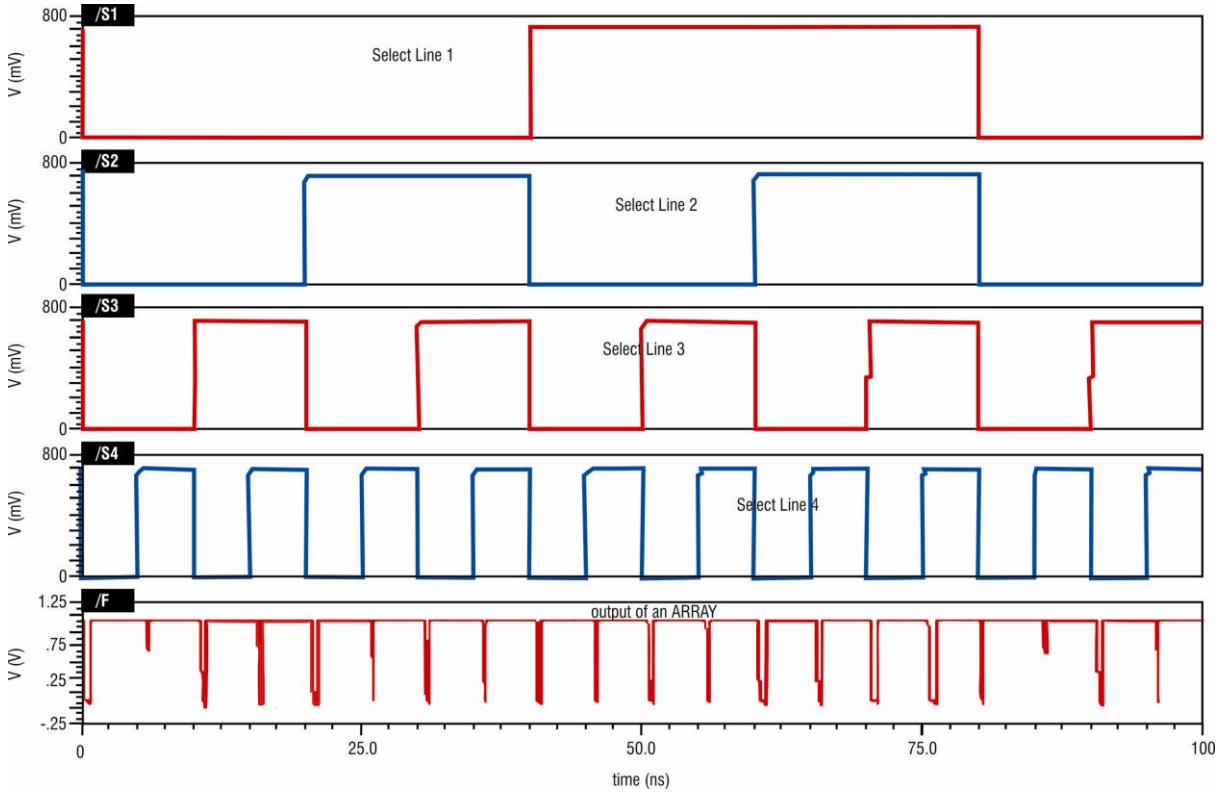


Figure 6.13-Select lines of 16:1 Mux and Output of 16-Bit Array

6.4 STATIC NOISE MARGIN

The Static Noise Margin (SNM) value can be determined easily from the simulation, by forcing the voltage on one of the internal nodes of the cell (ST) from ground to the power supply and by recording the response of the other node (STB). The SNM is defined as the smallest diagonal of the two maximum squares that can be fitted into the cross section of the VTC diagrams of the cross-coupled inverters [113]. The SNM of the SRAM cell is calculated, given by 0.324V, as shown in figure 6.14.

$$SNM = \sqrt{(NM_H{}^2) + (NM_L{}^2)} \quad (6.5)$$

$$NM_H = V_{OH} - V_{IH} \quad (6.6)$$

$$NM_L = V_{IL} - V_{OL} \quad (6.7)$$

V_{OH} = 660.36mV , V_{IH} = 336.79mV

From equation (6.6),

NM_H = 660.36 - 336.79

NM_H =323.57mV

V_{IL} = 373.48mV, V_{OL} = 4.6336mV

From equation (6.7),

NM_L= 373.48 – 4.6336

NM_L =368.8464mV

From equation (6.5), we get

$$SNM = \sqrt{(323.57)^2 + (368.84)^2}$$

$SNM = \sqrt{((323.57)^2+(368.8464)^2)}$

SNM = 324.139mV

SNM = 0.324V

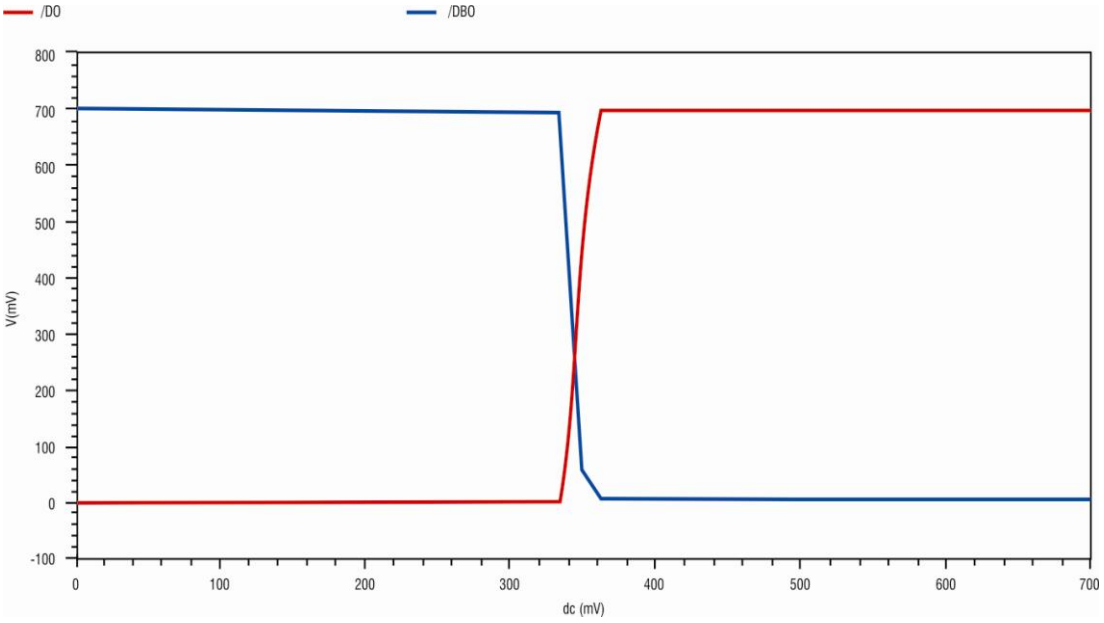


Figure 6.14- Static noise margin of SRAM cell

6.5 POWER CONSUMED BY 16-BIT SRAM ARRAY

There are different sources of active and standby power present in SRAMs. The active power is the sum of power consumed by the following components: - decoders, memory array, sense amplifiers and peripheral circuits [132]. The total active power of an SRAM with 4x4 arrays of cells can be summarized by the expression:

$$P_{act} = (mi_{act} + m\,(n-1)\,i_{leak} + (n+m)\,f\,C_{DE}V_{INT} + mi_{DC}\,\nabla t\,f + C_{PT}\,V_{INT}f + I_{DCP})*V_{dd} \quad (6.8)$$

Where i_{act} is the effective current of selected cells, i_{leak} is the effective data retention current of the unselected memory cells, C_{DE} is the output node capacitance of each decoder, V_{INT} is the internal power supply voltage, i_{DC} is the DC current consumed during the read operation, ∇t is the activation time of the DC current consuming parts (i.e. sense amplifiers), f is the operating frequency, C_{PT} is the total capacitance of the CMOS logic and the driving circuits in the periphery and the I_{DCP} is the total static (DC) or quasi static current of the periphery [124].

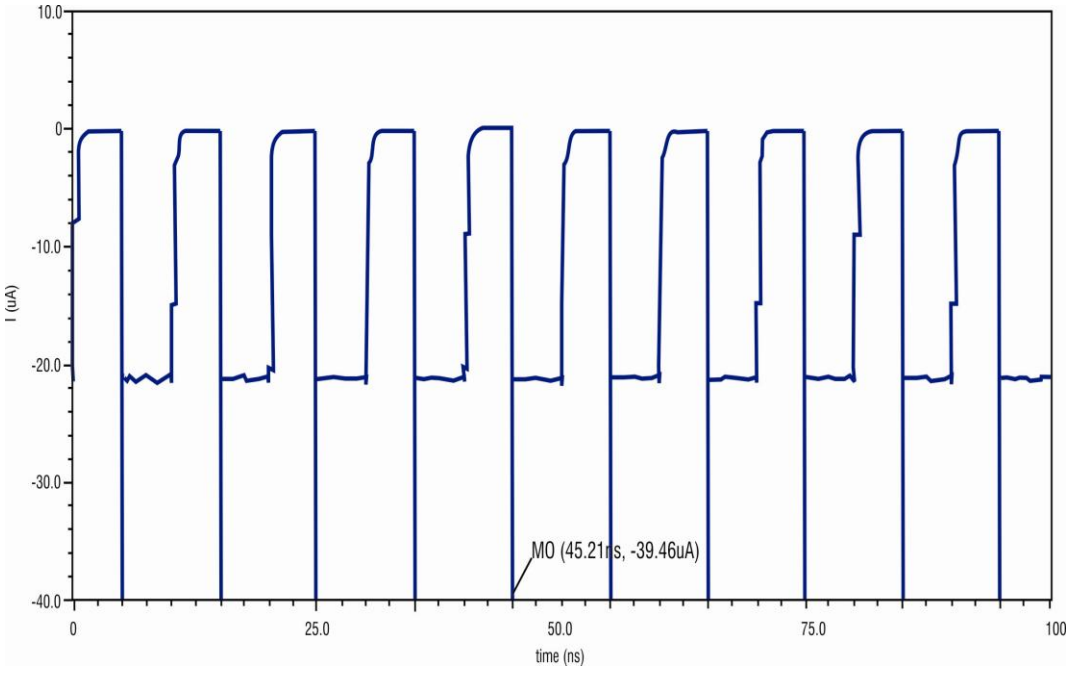


Figure 6.15-Current by cell

The standby power of an SRAM source is represented by i_{leak}mn because the static current from other sources is almost negligible. Therefore, the total standby power can be expressed as [133].

$$P_{stndby} = mn\ i_{leak} * V_{dd} \quad (6.9)$$

After simulation, I gets a consumed power by a single cell which is 39.46µw, and for 16- bits, it is 414.09µw.

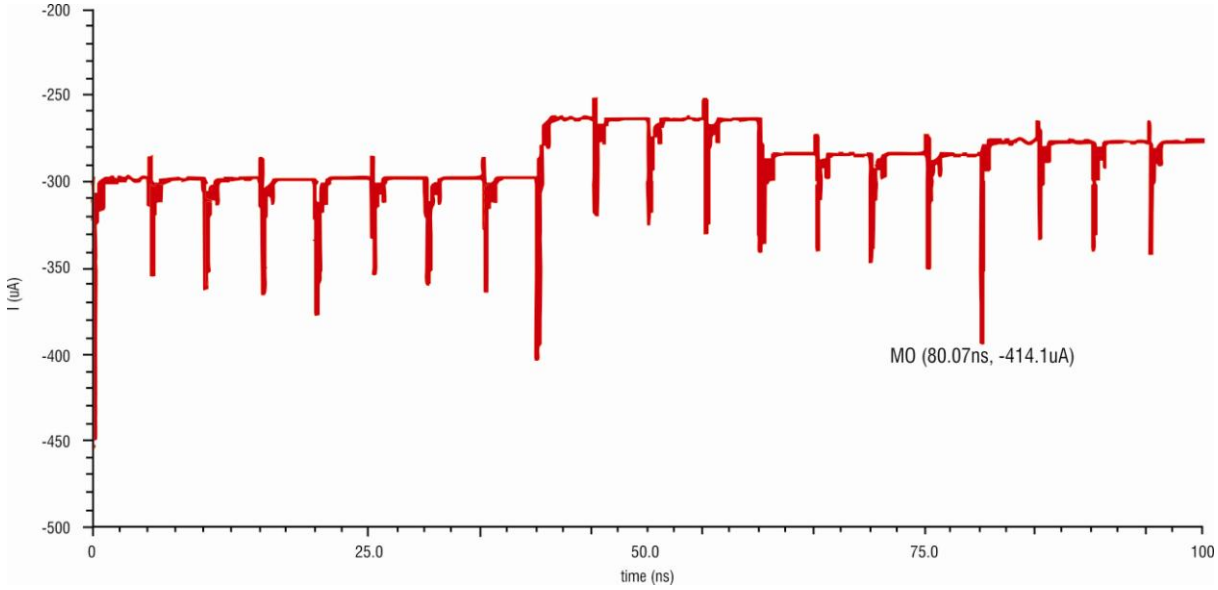


Figure 6.16-Current by Array

6.6 Result Analysis of 16-bit SRAM Array

I have done proper simulation of the 7T SRAM cell in cadence virtuoso tool and found some remarkable results. As shown in table (6.1), the leakage current of 7T SRAM cell design during the read operation is 21.355 µA and the leakage current during the write operation is 653.06µA. I think that SNM decreases with decreasing the voltage supply. However, if a time limit is set (word-line is active only for a finite amount of time), the SNM increases as voltage supply decreases. This is because, at a lower voltage supply, all currents drawn from the BL are less during '0' read. Therefore, the charge stored at storing node will be less.

Thus, the lower voltage at storing node is reaches after some delay which means an increase in the Static Noise Margin before the cell state is changed. The total power consumed by a cell is 39.46µW and the total power consumed by array is 414.09µW.

S.No.	Parameter	16-Bit Array
1	Clock Speed	500MHz
2	Leakage Current during Read	21.355µA
3	Leakage Current during Write	653.06µA
4	Write Access Time	0.578ns
5	Read Access Time (Array)	1.0513ns
6	Supply	1V
7	Leakage Power	653.06µw
8	Total Power Consumed by a Cell	39.46µw
9	Total Power Consumed by Array	414.09µw
10	SNM	0.324V

Table- 6.1 different parameters of 7T SRAM Cell

6.7 32b sub Array-:

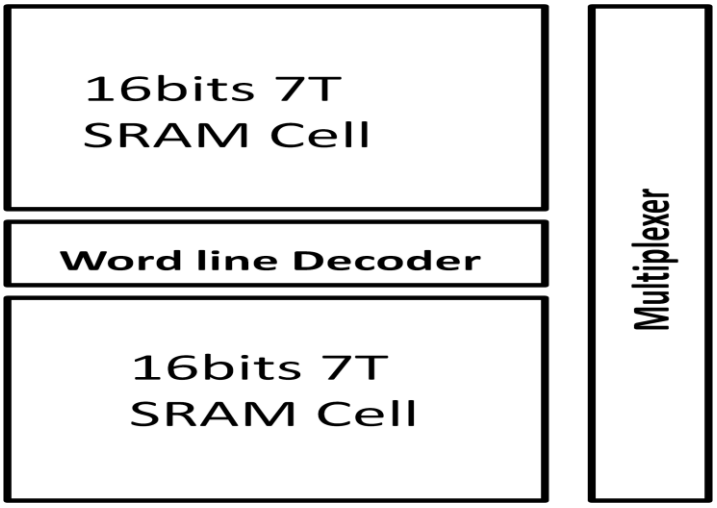


Figure 6.17-32b Sub Array.

A 32b sub Array is constructed by using 16 bit 7T SRAM cells. This sub Array has the capability to store 2^5 bits. This can be accomplished by using an (1-2) wordline decoder and (2-1) Multiplexer. 32b Sub Array is exhibited in figure 6.17. Memory reading is achieved by probing the resistance between the drain and source electrodes, which has an ideally large ratio between ON (resistance: RON) and OFF (resistance: ROFF) states. This is of key importance to attain reasonable memory density [122].

$16b = 2^4b$

$32b = 2^4 b \times 2^1 b = 2^5b$

6.7.1 1-kb Sub-Array-:

A 1-kb Sub-Array can be built as 8 rows X 4 columns. An SRAM 1-kb Sub-Array is designed with the help of 32 bit Sub-Array. In order to address one row out of 16, the row address decoder needs 5 address bit i.e. 2^5 bits =32 bits.

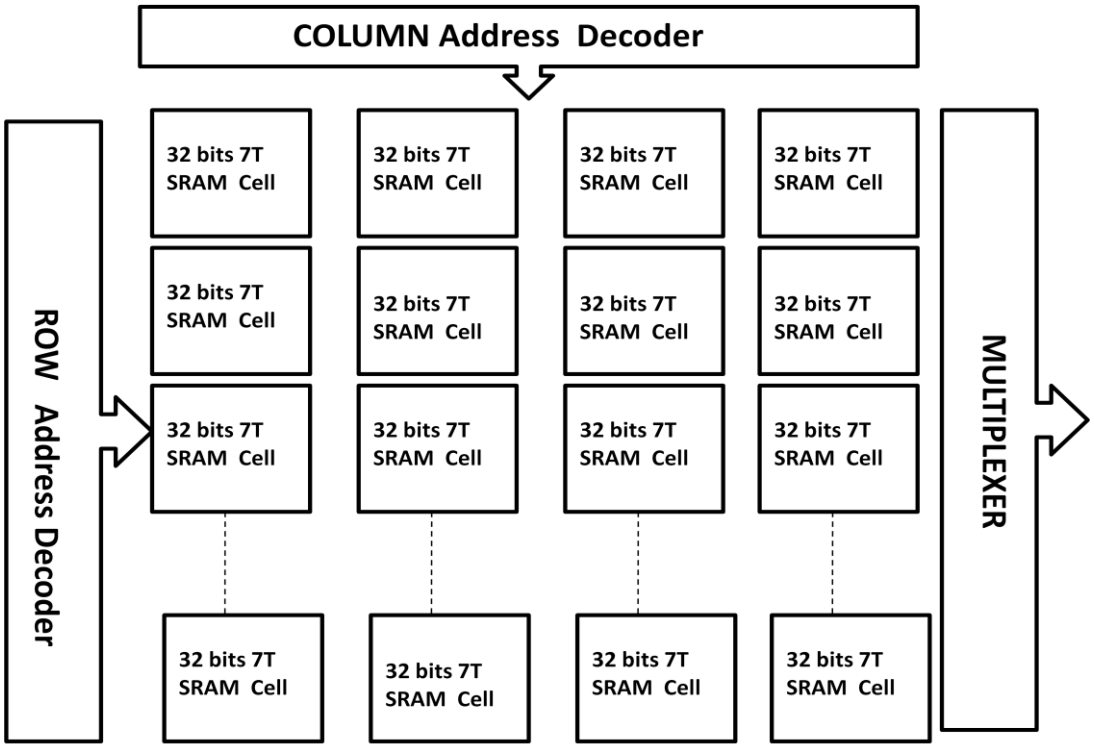


Figure 6.18-1kb sub-Array

This can be accomplished by using (3-8) row address decoder and (2-4) column address decoder. 1kb Sub-Array is shown in figure 6.18. The 8T array with 1024 cells per bitline generates negative bitline swing at 80°C and VDD = 0.3V [73].

32 bits = 2^5 bits

1kb = 2^5 x 2^3 x 2^2 bits = 2^{10} bits

6.7.2 8-kb SRAM array-:

The 8-kb SRAM array is organized with 4rows × 2 columns. In this array, we are using 4x2 matrixes with the help of 1kb sub-Array. Therefore this array has the capability to store 2^{13} bits. 8-kb SRAM Array is shown in figure 6.19.

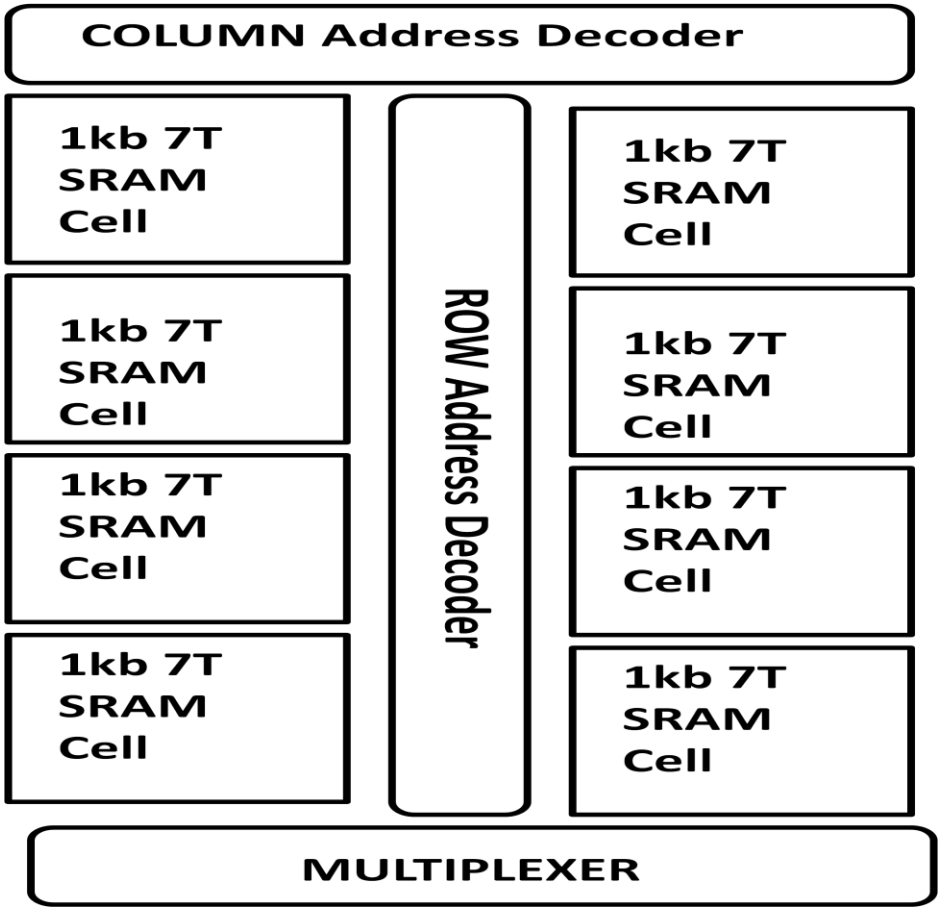


Figure 6.19-8kb SRAM Array

For an array structure with a fixed density (8 kbit), the optimal number of rows for minimum energy consumption is 128 at higher supply voltages (> 0.7 V), which is larger than the number of columns (= 64). On the other hand, the optimal number of rows decreases at lower supply voltages (0.3–0.7 V) [136].

1kb = 2^{10} bits

8kb = 2^{10} x 2^{2} x 2^{1} = 2^{13} bits

Bit store in 8-kb SRAM Array is shown in Table 6.2

Array	**SRAM Cell**	**Row address decoder**	**Column address decoder**	**Bit store**	**Total bits stored in 8kb Array**
16 bits	1-bit 7T	2^{2}	2^{2}	2^{4} bits	16 bits
32 bits	2^{4} bits 7T	2^{1}	-	$2^{4}x2^{1}$ bits	32 bits
1kb	2^{5} bits 7T	2^{3}	2^{2}	$2^{5}x2^{3}x2^{2}$ bits	2^{10} bits
8kb	2^{10} bits 7T	2^{2}	2^{1}	$2^{10}x2^{2}x2^{1}$ bits	2^{13} bits

Table- 6.2 Bit store in 8-kb SRAM Array

6.7.3 Result Analysis of 8-kb SRAM Array

This work is done using Cadence Virtuoso tool for the 8-kb 7T SRAM Array under temperature variation from 100C to 1250C.The analysis is based on access time 8ns, frequency 0.125GHZ and the optimum supply voltage 0.7V for the active and standby region developed on 45 nm CMOS technology.

Active Region:-

Parameters	**Active Region**						
Temperature	10^0C	11^0C	25^0C	27^0C	30^0C	75^0C	125^0C
Leakage current	49.80nA	49.89nA	51.32nA	51.54nA	52.08nA	56.32nA	60.06nA
Leakage Power	1.27pW	1.29pW	1.95pW	2.08pW	2.25pW	8.4pW	29.05pW
Operating Current	8.105mA	8.159mA	8.181mA	8.232mA	8.312mA	8.625mA	8.817mA
Operating Power	40.30µW	39.81 µW	39.75 µW	39.74 µW	40.25 µW	41.69 µW	42.11 µW
Optimum Current	2.37 µA	2.37 µA	2.35 µA	2.34 µA	2.31 µA	2.28 µA	2.21 µA
Optimum Power	83.86Pa	84.68pA	88.10pA	88.72pA	89.72 pA	91.96pA	96.09pA
Delay	405.5 ps	406.1 ps	414.5 ps	415.8ps	417.7ps	445.3ps	490.4ps

Table-6.3 Simulation Result of 8-kb SRAM Array in Active Region

The results for different temperatures are shown in Table 6.3 and Table 6.4. It could be clearly seen from Table 6.3 and Table 6.4 that the Leakage current and Leakage Power of these CMOS circuits increases as the temperature rises. Maximum Operating power and Maximum Operating current and Daley of the 8-kb SRAM Array are also estimated.

Standby Region:-

Parameters	Standby Region						
Temperature	10^0C	11^0C	25^0C	27^0C	30^0C	75^0C	125^0C
Leakage Power	1.271pW	1.319pW	1.976pW	2.076pW	2.274pW	8.482pW	28.76pW
Leakage Current	30.29nA	30.36nA	31.31nA	40.24nA	40.48nA	43.79nA	47.38nA

Table- 6.4 Simulation Result of 8-kb SRAM Array in Standby Region

6.7 SUMMARY OF THE CHAPTER

The process technology scaling and push for a better performance enabled the embedding of millions of Static Random Access Memories (SRAM) cells into contemporary ICs. In several applications, the embedded SRAMs can occupy the majority of the chip area and contain hundreds of millions of transistors. As the process technology continues to scale deeper into the nanometer region, the stability of the embedded SRAM cells becomes a growing concern. As a consequence, large SRAM arrays can impact all aspects of chip design and manufacturing because they become the yield-limiters in modern high-performance ICs. Here, it has been tried to design 16-bit array which will further be used in larger bit array and SRAM memory has been designed having capability to store 2^{13} bits using 4 X 4 array with 7T SRAM cell.

CHAPTER 7
CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

Static Random Access Memory (SRAM) cell is integrated on the same die with the microprocessor and it also occupies a large percentage of the die size and, therefore, it influences the design metrics significantly. Due to leakage current in SRAM, it also consumes large amount of static power which can have significant impact on the performance of the chip. To reduce this static power dissipation, various power reduction techniques and circuit topologies of seven-transistor (7T) SRAM cell have been proposed. The merits and demerits of the proposed designs have been investigated in detail and compared with the existing approaches. The detailed parametric analysis has been performed in terms of leakage current, silicon area and delay.

With the aim of achieving high density, half-selected cell stability and low leakage current, the SRAM memory cell has been developed using 5T, 6T and 7T circuit topologies. The half-selected cell stability of 5T, 6T and 7T SRAM cell is 426 mV, 278 mV and 345 mV respectively. The key observation in these designs is that the cell leakage current is determined by the node whose transistor is 'off'. At 25^0C, the leakage current in 5T SRAM cell is 3.60 nA and 18.90 nA, at the time of writing '0' and '1' on ST node, respectively. For the same operation, at 35^0C, the leakage current is 7.20 nA and 37.80 nA. In 6T SRAM cell, at 25^0C, the leakage current is 9.20 nA and -32.10 nA at the time of writing '0' and '1', on ST node respectively and at 35^0C, the leakage current is 18.40nA and -64.20 nA for the same operation. While in 7T SRAM cell, at 25^0C the leakage current is 22.63 nA and 87.67 nA at the time of writing '0' and '1', respectively, on ST node and at 35^0C is 34.11 nA and 145.30

nA for the same operation. In the same design, the silicon area for the proposed cell is found to be 21.66% lesser than 6T SRAM cell with 28.57% speed improvement. It is also found that the leakage current during memory cell access of a new cell reduces to 72.10% than 6T SRAM cell.

At every 10°C rise in temperature, leakage current approximately doubles which results in further cell power consumption penalty. An analysis of gate leakage current in 7T SRAM cell for a 45 nm technology has been performed and it clearly depicts that both gate and sub-threshold leakage currents contribute significantly to the overall leakage power dissipation in stand-by mode. The techniques of reduction in supply voltage and the increment in ground voltage using self-controllable voltage level (SVL) switches for reducing the leakage current in 7T SRAM cell have been examined in detail in this research work. It has been found that the lower self-controllable voltage (LSVL) approach is better in reducing sub-threshold leakage current (I_{sub}) while the upper self-controllable voltage (USVL) approach performs better with respect to gate leakage current (I_{gate}). However, both these techniques are found to be inadequate for reduction of leakage currents through access transistors. A USVL combined with LSVL approach, in which access transistors are put in 'off' state during the stand-by mode, is found to be very effective in reducing all significant components of leakage currents.

In several applications, the embedded SRAMs occupy majority of the chip area and contain hundreds of millions of transistors. As the process technology continues to scale deeper into the nanometer region, the stability of embedded SRAM cells is a growing concern. As a consequence, large SRAM arrays put an impact on all aspects of chip design and manufacturing because they are the yield-limiters in modern high-performance ICs. The 8 kb

SRAM memory has been designed having capability to store 2^{13} bits using 4 X 4 array with 7T SRAM cell, which can further be used in larger bit arrays for minimum leakage current and low power consumption. The leakage current of 16-bit array during read and write operation has been found to be 21.355 µA and 653.06 µA, respectively. The read and write access times of 16-bit array are found to be 1.051 ns and 0.578 ns, respectively. The total power consumed by a cell is 39.46 µW and the total power consumed by array is 414.09 µW. Therefore, in this research work, a low power 7T SRAM cell design, using self controllable voltage level techniques has been proposed and the gate leakage current and sub-threshold leakage current have been found to be 437.79 fA and 11.92 pA while in 6T SRAM cell it is found to be 1.2 nA and 5.49 nA, respectively. Therefore, a significant reduction in static power consumption is observed. Finally, 16-bit memory array design, using 7T SRAM cell has been proposed which may be used to design low power memory applications.

7.2 FUTURE SCOPE

This thesis analyzes, explores and simulates the groundwork for various continued research areas in low power memory cell design and more specifically memory applications. The research not only focuses on the design techniques to reduce static and dynamic power dissipation, but it also prompts to overcome the process and temperature variations for applications such as portable electronic systems where battery run-time is to be improved. Further analysis of the optimal operating points for each of the modules is suggested, as it is very likely that different system level blocks will have different optimal supply voltages and clock frequencies which will further complicate the interface between the blocks. The analysis would be enhanced by further fabricating SRAM array circuits for multiple supply voltage, quit bit-line and threshold voltage in various activity factors to verify the energy-

performance contours. Multiple threshold CMOS is needed in order to achieve wider range of threshold voltages. An SRAM array with multiple instances and back biasing can obtain a large threshold voltage range, however, transistor models with triple well processes are needed. Further, research work could also be beneficial in low voltage memory design which operates at low voltage process corners which will include a sub-threshold memory layout generator for SRAMs and ROMs.

The future of this work is Statistical Optimization of DG SRAM which is one of the possible extensions of DG SRAM to minimize the mean of leakage power dissipation under process variations, such as, variations in the number of dopants in the channel, variations in the line width and variations in the oxide thickness. By modeling the sub-threshold and tunneling gate leakage currents as functions of these variations, it is possible to minimize the mean of leakage current, subject to a fixed voltage potential between the power supply and ground rail in the standby mode and then by applying various new power reduction techniques. FinFET-based SRAM has to be very effective in reducing the short channel effects. One interesting extension of our research on low-leakage SRAM design is to evaluate the efficiency of heterogeneous cell SRAM and DG SRAM solutions on the FinFET-based designs.

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LIST OF PUBLICATION

Refereed to International Journals:

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Vitae

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