Design and Analysis of Some Studies on Low Power Hybrid Adder

A Thesis

Submitted in fulfillment of the requirement for the award of degreeof

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by

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Patiala-147004, India

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DECLARATION

I hereby certify that the work which is being presented in the thesis entitled, "**Design and analysis of some studies on Low Power Hybrid Adder**", for the award of degree of **Doctor of Philosophy** in Electronics and Communication Engineering Department (ECED), Thapar Institute of Engineering and Technology, Patiala, is an authentic record of my own work carried out under the supervision and guidance of Dr. Sanjay Sharma Professor, ECED, Thapar Institute of Engineering and Technology, Patiala.

The results presented in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma.

Priyank Sharma
Candidate

Date: 27.02.2024.

This is to certify that the above statement made by the candidate is correct to the best of my knowledge and belief.

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ABSTRACT

The mitigation of leakage current is of utmost importance in contemporary CMOS circuits, which are very susceptible to power loss, in order to get optimal performance. CMOS devices consume power in two distinct manners, namely statically and dynamically. As the feature sizes of MOS transistors continue to drop, there has been a corresponding reduction in the lengths of CMOS gates. As a result of this technological progress, integrated circuits may now be densely packed into smaller areas, leading to an increase in package density. The issue of power loss has emerged as a significant design constraint in light of the rapid and exponential growth in system complexity. In addition, the utilization of embedded memories is more prevalent in System-on-Chip (SoC) designs. Consequently, it is vital to possess a satisfactory memory power profile to accurately anticipate the overall power consumption of the system. Nevertheless, the memory power model used in commercial Electronic Design Automation (EDA) tools lacks sophistication, hence hindering its ability to provide accurate estimations of power usage. As the field of technology progresses towards the nano scale, the research and development of intricate logic circuits necessitate careful consideration of several factors such as leakage current, active power, delay, and space. To further enhance energy conservation, this work proposes the utilization of low loss one-bit full adder cells across many applications. The optimal dimensions of sleep transistors for one-bit Full Adder cells have been established by the application of a distinctive approach for resizing transistors. The use of this technology resulted in a substantial reduction in both power leakage and delay.

This study also analyzed and comprehended the nano scale characteristics of a CMOS transistor in the entire adder circuit to determine its most efficient operation. The source voltage, band-to-band tunneling of transistors, layer thickness, and cutoff voltage were all decreased for optimal high-speed performance. By employing various techniques, this resulted in a reduction of the loss of both moving and stationary capabilities. In that instance, when the device was in its sleep mode, leakage current was quite little to spare. The 45nm complete 10-transistor adder offered the lowest delay time across all loads, making it suitable for high-speed applications. The 45nm CMOS technology utilized in the design operated at an input voltage of 0.7V and a temperature of 27°C under standard atmospheric conditions. Implemented an optimal method resulted in a significant reduction in both the power consumption and leakage current of an entire adder cell.

Especially for usage in Low Power VLSI Circuits, the hybrid full adder was created. A low power hybrid full adder was created with XNOR and Transmission Gate (TG) logic, combining the two logic models—CMOS and TG based full adder. In terms of power, noise, and delay, the 10T hybrid full adder performed better. The hybrid full adder that was designed achieved a power reduction of 55.9% compared to the static CMOS full adder (28T) and 13% compared to the TG-based full adder (20T). The delay was reduced by 62% and 28.1%, respectively, in comparison to the TG-based full adder and the Static CMOS (28T). The simulation is executed on the Cadence Virtuoso with GPDK at 45nm.

Moreover, the Ultra-Low Power Techniques (ULPT) of Multi Threshold Complementary Metal Oxide Semiconductors (MTCMOS), Tri-Mode MTCMOS, and Self Controllable Voltage Level (SVL) Techniques were used to investigate the 10T Junction-Less Double Gate Hybrid Full Adder (10T JLDGHFA) cell. The leakage characteristics of an idle circuit decreased with standard circuit fabrication techniques. Simulation results have demonstrated that the leakage power reduced by 24.09% while the leakage current is reduced by 24.11%. Relative to MTCMOS and SVL technologies, Tri Mode MTCMOS offered a 98.55% higher power density and current concentration. It was implemented with a smaller number of transistors and CMOS could be replaced with Fin FET in the future.

Furthermore, downscaling the CMOS technology was identical to Moore’s principle, moved with greater functionality, low power, long lifespan, and VLSI circuits that persisted in the need for more integration. When this deterioration expanded to the nano size, many challenges were propagated and had physical changes. We proposed some reliability parameters to an 8T full adder at 45nm CMOS technology. The reliability parameters NBTI and HCI were evaluated at various operating conditions for a 1 year span. The major techniques in reliability were implemented such as Negative Bias Temperature Instability (NBTI) under PMOS and Hot Carrier Injection (HCI) under NMOS degradation and aging were compared and evaluated. The simulated results indicated that the NMOS under HCI degradation and aging was high at low voltage operation at 0.7V and very high at 1.2V operation to NM2. PMOS deterioration and aging were highly influenced by PM1 and PM2 at all observed voltages.

This study examined several design architectures and evaluated their individual merits in the context of multiple bit full adder design using the Modified Gate Diffusion Input (m-GDI) approach, based on relevant data analysis. The findings of this study enhanced the design of forthcoming ALU full adder implementations. As a first step towards further investigation, a thorough examination and subsequent optimization of the design's voltage swing was undertaken.. In conclusion, this study provided a comprehensive analysis of the TG, hybrid, static CMOS, and forthcoming m-GDI full adder, enabling a comparative evaluation of their respective performance characteristics. The transient power of the planned hybrid full adder exhibited a much lower average, with an absolute value approximately equal to 16.65μW. The delay in the sum and carry output was denoted as 50.81ps and 51.19ps respectively. Consequently, a determination was made on the optimal design for a complete adder circuit that minimizes both die area and power consumption.

The analysis was based on a predetermined set of factors that were consistently maintained throughout the analogy. The interim operational hours and conditions were same across all three locations. The factors included in the analysis were transistor count, Power Delay Product (PDP), Cout delay, SUM delay, and average transient power.

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List of Abbreviations

Sr. No.	Abbreviations/Symbols	Full Form/Meaning
1.	SOC	System on chip
2.	CMOS	Complementary Metal Oxide Semiconductor
3.	V_O	Output Voltage
4.	GND	Ground
5.	V_{TH}	Threshold Voltage
6.	CLK	Clock
7.	VTC	Voltage Transfer Curve
8.	V_{REF}	Reference Voltage
9.	V_{IN}	Input Voltage
10.	V_m	Switching Voltage
11.	V_p	Voltage at Positive input
12.	V_n	Voltage at Negative Input
13.	W_p	Width of PMOS Transistor
14.	W_n	Width of NMOS Transistor
15.	L_p	Channel Length of PMOS Transistor
16.	L_n	Channel Length of NMOS Transistor
17.	F_{MAX}	Maximum Sampling Frequency
18.	LSB	Least Significant Bit
19.	SAR	Successive Approximation Resistor
20.	SNR	Signal to Noise Ratio
21.	ENOB	Effective Number of Bits
22.	SFDR	Spur Free Dynamic Range
23.	DNL	Differential Non Linearity
24.	INL	Integral Non Linearity
25.	MODL	Multiple Output Domino Logic

26.	A_V	Gain
27.	ΔV	Input voltage change
28.	ICR	Input Common Mode Range
29.	SR	Slew Rate
30.	V_{out}	Output Voltage
31.	I	Current
32.	C	Capacitance
33.	dV	Voltage
34.	V^+	Positive Input
35.	V^-	Negative Input
36.	Io^+	Positive Current
37.	Io-	Negative Current
38.	RC	Resistor Capacitor
39.	VLSI	Very Large Scale Integration
40.	SVL	Self Controllable Voltage Level
41.	MOSFET	Metal Oxide Semiconductor Field Effect Transistor
42.	SCE	short Channel Effects
43.	LSVL	SVL at Ground
44.	USVL	SVL at Supply
45.	AVL	Adaptive Voltage Level
46.	AVLG	AVL at Ground
47.	AVLS	AVL at Supply
48.	PLL	Phased Lock Loop
49.	VCO	Voltage Controlled Oscillator
50.	SOI	Silicon on Insulator
51.	FET	Field Effect Transistor
52.	P_{total}	Total Power
53.	P_{static}	Static Power
54.	$P_{dynamic}$	Dynamic Power

55.	I_{static}	Current flowing through the device
56.	$P_{transien}$	Transient Power
57.	P_{cap}	Capacitive Load Power
58.	C_L	Load Capacitance
59.	C	Capacitance
60.	f	Frequency
61.	i	Current
62.	v	Voltage
63.	q	Charge
64.	φ	Flux linkage
65.	dv	Differential of voltage
66.	di	Differential of current
67.	dφ	Differential of flux linkage
68.	dq	Differential of charge
69.	M	Memresistance
70.	L	Inductance
71.	D	Length of the Memristor
72.	W	State variable of the Memristor
73.	V(t)	Voltage with respect to time
74.	I(t)	Current with respect to time
75.	P(t)	Power with respect to time
76.	R_{on}	High doped region
77.	R_{off}	Low doped region
78.	ns	Nanosecond
79.	M1-M5	NMOS Transistors
80.	P_{total}	Total Power
81.	P_{dyn}	Dynamic power consumption
82.	P_{sc}	Short Circuit Power
83.	$P_{st/static}$	Static Power Consumption

84.	I_{sc}	Short-circuit current
85.	C_L	Switching Capacitance
86.	α	Switching activity of output node
87.	f	Operating frequency of the system.
88.	TiO_2	Titanium Di-Oxide
89.	Pt	Platinum Contacts
90.	Hz	Hertz
91.	$I_{leakage}$	Leakage Current
92.	SL	Sleep signal
93.	SLB	Sleep Bar signal
94.	$V_{ss}v$	Virtual Ground
95.	$V_{dd}v$	Virtual Supply Voltage
96.	nm	Nanometer
97.	SOP	Sum of Products
98.	POS	Products of Sum
99.	CAM	Content Addressable Memory
100.	SVL	Self-Controllable Voltage
101.	LSVL	Low Self controllable voltage level
102.	pW	Pico-watt
103.	pS	Pico-second
104.	µW	Micro-watt
105.	nW	Nano-watt
106.	t_{pd}	Propagation Delay
107.	P_{Peak}	Peak Power
108.	E	Energy
109.	t_{dr}	Rise Time
110.	t_{df}	Fall Time
111.	R	Resistance

CHAPTER 1

INTRODUCTION

The popularity of portable, battery-operated devices has increased dramatically in recent years. In portable electronics, the combination of efficient computing and low consumption of batteries is becoming increasingly vital. Considering the recent demand for specially designed chips, designers have been putting much effort into integrating as many practical features as possible within each chip. Challenges like temperature variations, manufacturing processes, packaging and cooling arise when the density of chips develops. Power dissipation can be reduced at the design level by varying the voltages at which different device parts operate or by scaling supply voltages. Lowering thresholds and device sizes are among the prevalent transistor-level techniques. Logic-level procedures are also the primary objective in the quest for modern design.Reducing thresholds and device sizes are among the prevalent transistor-level techniques. Logic-level operations are a focus of contemporary design efforts as they strive to create novel designs with increased efficiency and lower power usage. The provided information is necessary to synthesize VLSI CMOS logic.

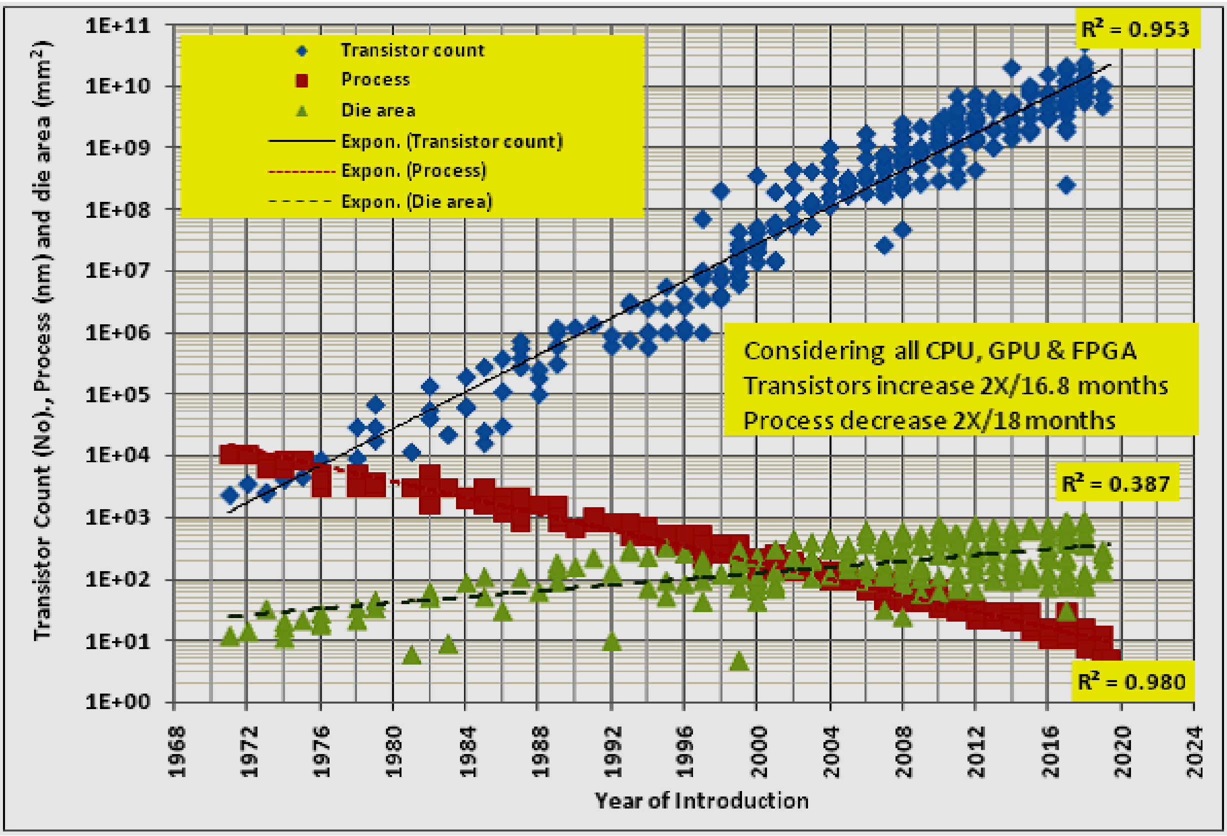


Figure 1.1: Microprocessor Chip Trends in Transistor Cout[3]

The majority of technologists nowadays work on VLSI technology. Small Scale Integration (SSI) systems, a subset of low-density manufacturing processes, were developed in the early 1960s. There were just ten different types of transistors available in SSI. This accelerated the development of Medium Scale Integration (MSI), which relies on a single chip that contains a large variety of transistors—up to 100.

Other IC households like ECL have been outlasted employing Transistor-Transistor Logic (TTL), which gives excessive integration densities and has become the foundation of the first integrated circuit revolution. The early 70s are known for developing around 1000 transistors on a single chip, called Large Scale Integration (LSI). 1970 VLSI began when complicated semiconductor and communication technology changed into advanced, Very Large Scale Integration. It is a framework in which several transistors surpass 1000 transistors created on a single chip. With VLSI, all these additives were introduced on a single chip. Before VLSI appeared on the scene, the extent of the transistor was one of the real issues. With the growth of technological invention, the device dimensions are downsizing, and the complexity and performance evaluation of VLSI ICs is enhanced [36]. With the first microprocessor, 4004 transistors by using Intel in 1972, and 8080 transistors in 1974, the second phase of revolution in the technology of Integrated Circuits began. Companies like Cadence, Alliance Semiconductor, Texas Instruments, Synopsys, Infineon, Celox Networks, Cisco, National Semiconductors, Lucent, Micron Tech, ST Microelectronics, Philips, Qualcomm, Mentor Graphics, Intel, Analog Devices, Motorola and other industries are keen to know of a variety of fields in “VLSI” like Hardware Descriptive Language (HDL), Programmable Logic Devices (PLD), layout equipment, Embedded Systems and so on. To accomplish superior and coordinated thickness in each era of innovation, CMOS circuits have scaled downwards unyieldingly. Reading the patterns in the current nanoscale innovation under CMOS circuits, successful arrangements must be made to diminish spillage control since it is expected that in not so distant future, spillage power will command the chips, adding to control utilization. In each level of outline reflections, these arrangements can be connected. The deliberation level includesthe framework, structural, circuit, and gadget/process levels.

CMOS innovation is utilized for the usage of coordinated circuits. For advanced circuits, CMOS innovation is utilized for microcontrollers, microchips, SRAM, etc. For simple circuits, the CMOS innovation is utilized for picture sensors, exceedingly incorporated handsets, information converters, and different sorts of correspondence. CMOS, i.e. Complementary Metal Oxide Semiconductor, is a mix of PMOS and CMOS. The CMOS gadget has fundamental attributes, which include high commotion invulnerability and low static power.

One of the upsides of utilizing CMOS gadgets is that they do not squander much warmth when contrasted with other rationale like transistor-transistor-rationale (TTL) or NMOS rationale because these rationales envelop some current standing, notwithstanding the time when they do not change the state. The CMOS gadget additionally permits the high thickness of the rationale work on a chip. Due to this reason, CMOS gadgets are generally used to actualize VLSI chips.

1.1 Context of Research

Transistor density on chips has increased dramatically during the last decade. Moore's law [1] predicts that the number of transistors that can be manufactured on a single die will rise at an exponential pace with time. Despite the fact that a chip's complexity doubles every two years, strong law [2] continues to hold. Figure 1.1 [3] shows a graph showing the number of transistors on microprocessor chips and how they have changed over the last four decades. The rising number of transistors proves Moore's law.

The instance of microprocessors shows a tremendous rise in complexity and performance expectations [4]. Clock frequencies have increased from the 1970s 0.1 MHz to 1 GHz [5]. The number of transistors on a chip has increased from a low of only 2,000 in 2000 to over a billion. Intel 4004 microprocessor [6] was an initial computer that required careful placement of every transistor and design optimization for its specific working environment. Time-to-market efficiency is critical for such components but cannot be optimized when millions of transistors must be integrated [7]. As there are so many moving pieces in contemporary circuit design, several design automation tools have been developed to help keep track of them all.

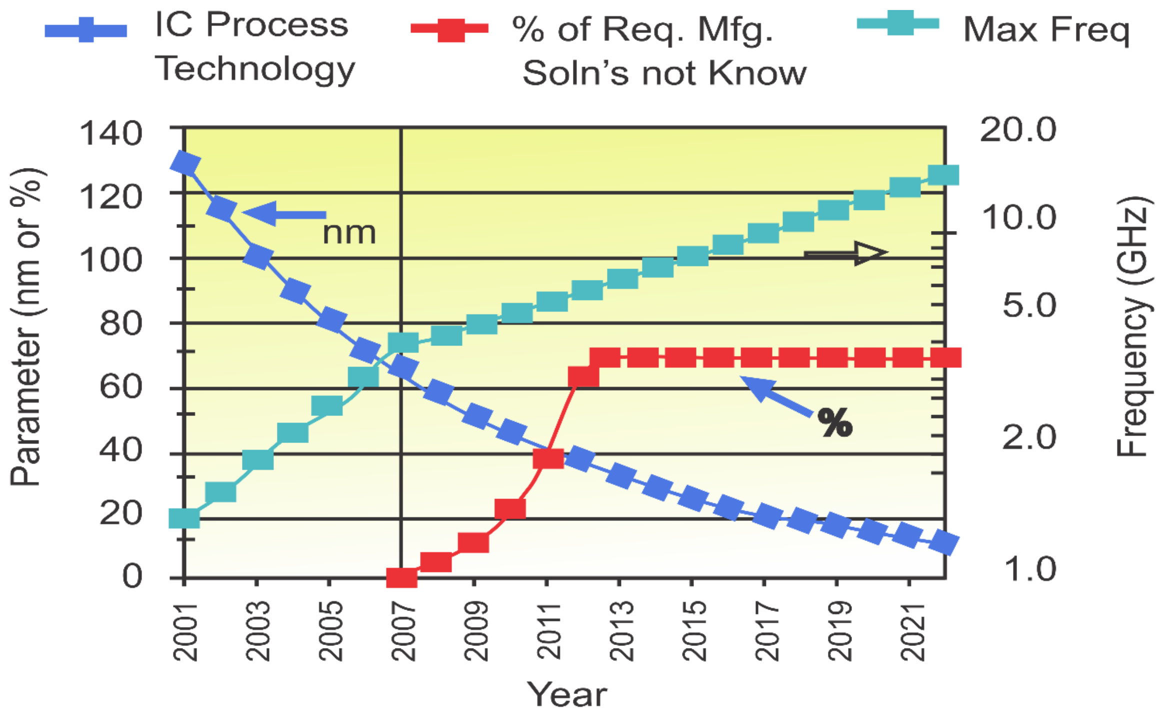


Figure 1.2: Microprocessor Update Cycles and Technological Trends [11]

By expanding the channel's bandwidth, we may improve the performance of a circuit. However, its impact on power density is tremendous [8]. Attempts to save expenses often drive one to a greater degree of integration. While low-cost technology innovations to continually improve power conservation are becoming scarcer, they are not extinct. Available system-on-chip (SOC) architectures [9-10] need a higher power supply. As electronic devices continue to shrink, there is a corresponding increase in the need for static and dynamic power in logic and memory. Figure 1.2 [11] depicts the shifting correlations between device size and clock frequency. The amount of lithographic needs for which no viable production alternatives were identified has been highlighted in red. These features suggest that power density inside the chips will grow considerably when processor rates improve. Regarding portability, battery life is the major bottleneck [12]. There is a growing need for cheaper products with more functionality and more extended run periods. Starting at the 120nm node, the processing performance only slightly improves while the dynamic and leakage current density increases [13]. This necessitates highly integrated silicon in modern manufacturing techniques but at the expense of a higher leakage current [14]. So, it is essential to reduce power loss by bearing the considerations mentioned above in mind.

Table 1.1: Methods on several Hierarchical Scales

S. No	Rank in a hierarchy	Approach
1	System	Power down, partitioning
2	Algorithm	Regularity complexity, concurrency
3	Architecture	Redundancy, data encoding parallelism, pipelining
4	Circuit Logic	Energy recovery, transistor sizing, logic styles,
5	Technology	Multi-threshold devices, threshold reduction

Several strategies for lowering power consumption and enhancing performance may be adopted at various points in the digital design hierarchy. Instead of designing circuits piecemeal, designers are now utilizing a hierarchical framework [15] that makes it simple to include automation. This hierarchical designing method is advantageous for highly large-scale design in digital circuits, offering significant advantages over analogue design. The digital design uses several abstraction levels: system, module, RTL (Register Transfer Level), gate, and transistor. System-wide measures may be taken to fight the power minimization issue, including shutting down and partitioning. The latter facilitates sequential execution of the modules, reducing power consumption. The use of regularity in algorithms may drastically cut down on unnecessary calculations [16]. Encoding data, pipelining, and parallelism are only some methods that may be employed to conserve the clock cycle and cut down on duplicate processing [17]. These methods make the circuit more usable. Table 1.1 summarizes several approaches that may be used with varied degrees of abstraction. In this thesis, we concentrate on improving performance from a logical perspective, aiming to invent novel logic approaches that may be utilized to design efficient circuits while also using little power. For this reason, we have chosen to concentrate on the logical level, where advances may be integrated with those gained at higher levels of abstraction. The following section concisely explains the causes that led us to pursue study in this field [18].

1.2 Overview of CMOS VLSI Design

Complementary metal oxide silicon has been an essential technology in the integrated circuit industry during the last several decades. Based on the theoretical foundation laid by Julius Lilienfeld for the first field-effect transistor in 1925 [19], Oskar Heil patented the first metal-oxide semiconductor field-effect transistor in 1935. Following him, Bell Laboratories' John Bardeen, Walter Brattain, and William Shockley developed the first practical point-contact transistor in 1947. In 1958 [20], Jack Kilby of Texas Instruments developed the first flip-flop using an integrated circuit. These circuits could not be built until Fairchild's Frank Wanlass introduced the first Complementary Metal Oxide Silicon (CMOS) logic gate in 1963. (nMOS and pMOS) when everything else failed [21]. Because of their low power consumption, these circuits are poised to become the standard. The first MOS calculator wasn't displayed until 1965, and by 1967, a broad variety of MOS devices with real-world applications in industry, were on display. As time has progressed, nMOS-based procedures have become the norm [22]. Concerns about power use first surfaced in the 1980s. The CMOS approach is widely used nowadays [23]. Thin-film transistor technology was made possible due to this concept. The inverter, the NOR gate, and the NAND gate were the first three logic circuits to be created. Integrated circuits may be created using CMOS (Complementary Metal-Oxide-Semiconductor) technology [24]. A square relationship exists between the supply voltage, capacitive loading, and switching activity in CMOS circuits' power usage [25]. All contemporary digital logic circuits, such as microprocessors, microcontrollers, static RAM, and more, adopt CMOS technology. Charge-coupled device (CMOS) image sensors, data converters, and highly integrated transceivers are all examples of analogue circuits that rely on CMOS technology [26]. As a result, CMOS has become the de facto standard for Very Large-Scale Integration (VLSI) devices, displacing bipolar technology. In order to create an Integrated Circuit (IC), Very Large-Scale Integration (VLSI) combines many transistors onto a single chip. The advent of VLSI coincided with advances in semiconductor complexity and communication protocols.

Before the advent of VLSI advancement, most ICs had a well-guarded strategy for potential failure sites. VLSI allows IC facilitators to integrate them on a single chip.

In the mid-1920s, a few early adopters tried out devices that would eventually be used to regulate the current in solid-state diodes and convert them into triodes. Specialists eventually returned to the strong state device revolution after focusing on the radar movement for a while. Transistors allowed the hardware industry to transition from vacuum tubes to solid-state devices.Armed with the tiny transistor, the electrical designers of the 1950s foresaw the consequences of creating increasingly complex circuits internally and externally. Problems arose as a result of the disorganized construction of circuits. The circuit's compass was one potential problem. A complicated circuit, like a personal computer, needs speed to function. Thefirst mixed circuit was set up in September 1958 [27]. The thought was substantial, even though the originally worked out circuit was harsh and had a few difficulties. There is no longer a need to manually assemble wires and splits, reduce the size of the circuits and automate the data collection infrastructure. Small-Scale Integration (SSI), Medium-Scale Integration (MSI), Large-Scale Integration (LSI), and Very Large-Scale Integration (VLSI) all emerged as a result of this, with progressively more transistors packed onto a single silicon wafer as time passed (from thousands to millions to billions) (10^9).

At present, most of the technologists use VLSI technology. In the early 60s,falling inside the category of the low-density fabrication process, Small Scale Integration (SSI) system came into existence. In SSI, the variety of transistors became restricted to 10, thus giving an upward push to Medium Scale Integration (MSI) inside the final 60s, in which a wide variety of transistors depending on a single chip quickly changed into 100.

Other IC households like ECL are outlasted utilizing Transistor-Transistor Logic (TTL). This logic gives excessive integration densities and has become the basis of the first integrated circuit revolution. The early 70s is known for developing around 1000 transistors on a single chip called Large Scale Integration (LSI). In 1970, VLSI began when complicated semiconductor and communication technologies changed into advanced VLSI, i.e. Very Large Scale Integration. It is a framework in which several transistors surpassing a thousand are created on a single chip. A digital circuit contains CPU, RAM, ROM and different glue good judgment. With the advent of VLSI, all these additives were introduced on a single chip. Before VLSI appeared, the extent of the transistor was one of the significant issues. With each technological advancement, device dimensions are downsizing, and the complexity and performance evaluation of VLSI ICs are enhanced [28]. With the first microprocessor, 4004 were added using Intel in 1972, and 8080 in 1974, the second technology of the Integrated

Circuits revolution started taking shape. Companies like Cadence, Alliance Semiconductor, Texas Instruments, Synopsys, Infineon, Celox Networks, Cisco, National Semiconductors, Lucent, Micron Tech, ST Microelectronics, Philips, Qualcomm, Mentor Graphics, Intel, Analog Devices, Motorola and other industries have shown their keen interest in a variety of fields in “VLSI” like Hardware Descriptive Language (HDL), Programmable Logic Devices (PLD), layout equipment, Embedded Systems and so on. To accomplish superior and coordinated thickness in every era of innovation, CMOS circuits have scaled downwards unyieldingly. With the existing patterns in the current nanoscale innovation for CMOS circuits, successful arrangements must be taken to diminish spillage control since it is expected that shortly, spillage power will command the chips to add up to control utilization. These arrangements can be connected with the following deliberation levels: framework and structural level, circuit level, and gadget/process level. CMOS innovation is utilized for the usage of coordinated circuit while for advanced circuits, this innovation is applied for microcontrollers, microchips, SRAM and so on. For simple circuits, the CMOS innovation is used for picture sensors, exceedingly incorporated handsets, information converters, and different sorts of correspondence. CMOS, also called Complementary Metal Oxide Semiconductor, is a mix of PMOS and CMOS. A CMOS gadget has essential attributes like high commotion invulnerability and low static power. One of the upsides of utilizing a CMOS gadget is that it does not squander much warmth when contrasted with other rationale like transistor-transistor-rationale (TTL) or NMOS rationale. These rationales are disadvantaged as they envelop some standing current even when they do not change the state. The CMOS gadget additionally permits high thickness of the rationale work on a chip. In light of this reason, CMOS gadget is generally used to actualize VLSI chips [29].

1.3 Evaluation of Hybrid Adder

Further developments in this field included more transistors, and more individual termination points or frameworks were eventually joined. Initially, integrated circuits contained only a few components, perhaps up to ten diodes, transistors, resistors, and capacitors, making creating multiple logic gates on a single device possible. Medium-Scale Integration (MSI) is the reorganization of framework-initiated devices with various systems for thinking entrances, formerly known as Small-Scale Integration (SSI). Additional redesigns prompted LSI, or frameworks with fewer than a thousand entries, for strategies of thought. Current technological advancement has far surpassed this imprinting, and today's semiconductor has a variety of doors and billions of individual transistors. Midway through 2008, billion-transistor processors will be fiscally available. This became more prevalent as semiconductor production advanced from the then-current 65 NM outline. Current designs are not at all like conventional contraptions, as far-reaching procedure mechanization and electronic support combine to design transistors, empowering more extraordinary measures of the multifaceted nature in subsequent methods of calculating value. Specific massive pondering components, for example, the SRAM (Static et al.) cell, are still hand-drawn to ensure the best quality. With the introduction of NEMS advancement, VLSI development may move towards further radical reduction[30].

1.4 Need for Hybrid Adder

Carver Mead and Lynn Conway's plan to restrict the spectrum of connecting fabrics with an aim to increase microchip area which was the impetus behind VLSI architecture. This is consummated by a time-consuming process of creating rectangular, large-scale squares that may be wired together through projection [31]. In this illustration, a snake's cellular architecture is divided into a few tiny pieces. Multilevel nesting may seem to be the master of this sorting in sophisticated minds. While the mid-1980s understood the fundamentals of organized VLSI architecture, this understanding has faded as designers have learned to limit the closeness of arrangement and the power of controlling devices to exploit the increasing range made possible by Moore's Law. To echo Edsger Dijkstra's made-up programming framework of the system settling to keep up a key partition from the ramshackle spaghetti-created assignment, Reiner Hartenstein introduced the term "sorted out VLSI plan" (previously known as "formed LSI configuration") while presenting the apparatus depiction vernacular KARL in the mid-'70s.

1.4.1 Challenges

As a result of progress in scaling, microchips are becoming more complicated. In contrast, chip developers have encountered a few challenges that have caused them to reframe their strategy and begin planning for a post-silicon era.

As photolithography frameworks converge on the fundamental rules of optics, achieving high accuracy in doped focuses and scratched wires becomes more complex and error-prone because of the organization of the processes involved. Before a chip can be guaranteed an orchestrated theme, creators must repeat their efforts across many corners of the creation framework.

Thus, it becomes imperative that coordinators consider at least one of these standards while planning out unique circuits.

• Initial pass success: With passing time, sizes decrease (due to scaling), and wafer sizes increase (due to reduced collection costs). In addition, the number of kicks the bowl gets per wafer rises, and the flexibility with which acceptable photo masks may be made increases rapidly. The price of a shroud for a propelled helicopter might easily reach several millions. This one-time fee encourages first-pass silicon success and reroutes the traditional iterative speculation that often requires a few "turn cycles" to find blunders in silicon. Many information-planning methodologies such as Design for Manufacturing (DFM), Design for Testing (DFT), and Design for X have been developed to aid the usage of this new method. [32].

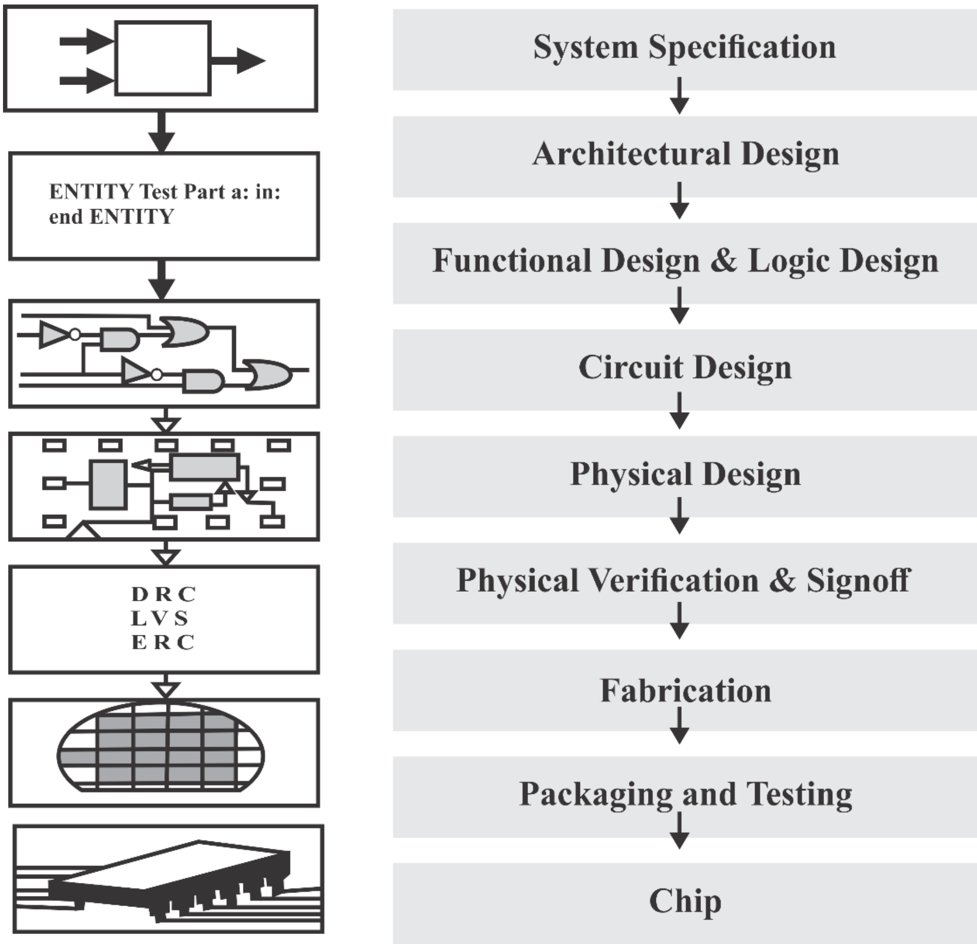


Figure 1.3: Integrated Circuit Design Flow

1.4.2 Hybrid Full Adder

There is a flood of portable battery-powered gadgets such as computers, notebooks, mobile phones, etc. These devices' Ultra-Large-Scale Integration (ULSI) and Low-Power Delay (LPD) requirements necessitate the use of VLSI architectures. Full Adder being the fundamental element of all circuits, must be optimized to use less power and execute faster. As the most fundamental building block from which all other circuit applications are created, the complete Adder has been the exclusive focus of researchers for many years. Several logical approaches were explored for realizing the 1-bit full Adder, each with its own set of advantages and drawbacks. So far, two different layouts have been explored. The following list depicts them: [33].

1) Static style

2) Dynamic style

Static adders are the most reliable and efficient kind due to the merits of basic construction and low power consumption. However, the chip area is massive in comparison to dynamic adders.

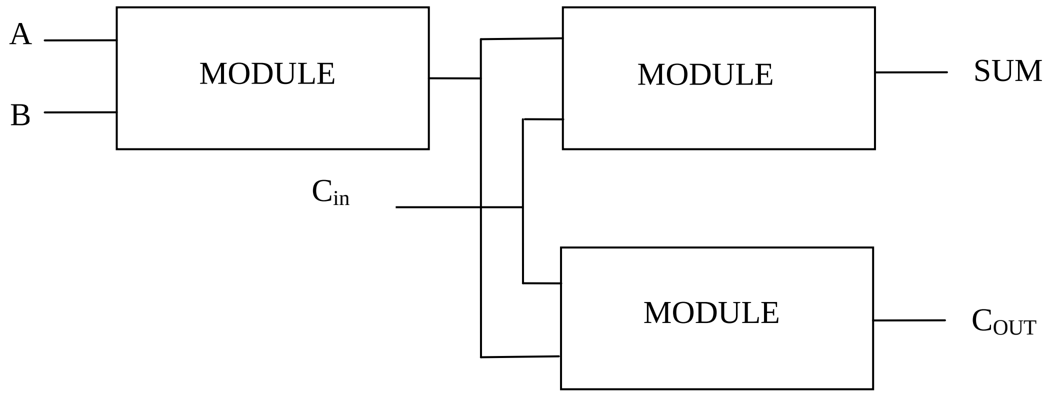


Figure 1.4 Block Diagram of Full Adder

As per Fig. 1.4, three squares represent the whole adder circuit that is being suggested. The XNOR pieces are square 2 and block 1. Piece 3 generates the C_{out} (yield convey flag), and these two squares are responsible for making the SUM (sum flag). Each individual square is constructed in such a manner that the complete adder circuit operates at a high level of efficiency. The outcomes of waiting, exercising control, and staying inside a certain area are always favorable. Below, we provide a detailed discussion of each component: Block XNOR, (Type A), XNOR module in our suggested complete adder circuit may dissipate the amount of energy needed to run the whole circuit. This square is designed in such a way that it consumes electricity in the most efficient way possible without reducing the voltage in any way. The adapted XNOR circuit is introduced in Fig.1.5. Due to the use of a weak inverter, this circuit has a low power consumption. The transistors used in such inverters often have narrow channels. These devices use Mp and Mn1 transistors.

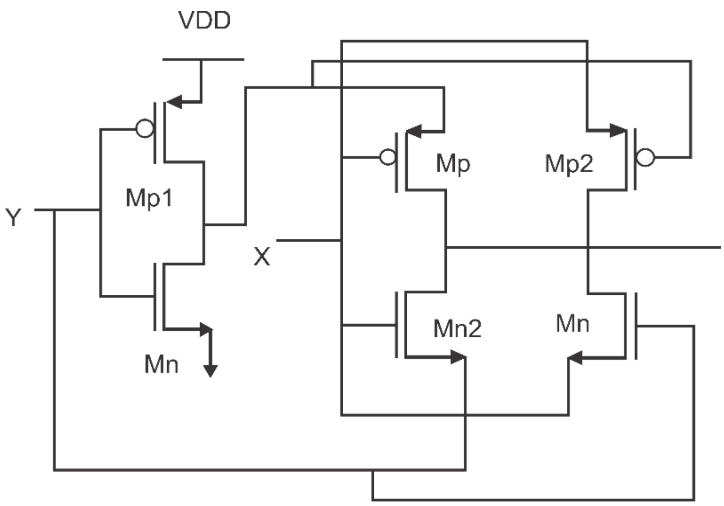


Figure 1.5 XNOR Block of Full adder

Our XNOR block uses six transistors, but they are arranged in a different way than is typical. When compared to the standard 6-T XOR-XNO implementation [34], this XNOR consumes exceptionally little power while providing impressive throughput.

To transport transistors Mn8, P8, P7, and Mn7,generation block, is used which also generates the circuit's carry signal at the output. The input carry signal, C_{in}, propagates via a single transmission gate, Mp7, and the Mn7. In this manner, the length of the whole carry propagation channel is drastically shortened. Then, the wider channel and more robust transmission gates are employed to further minimize the latency in the carry signal's propagation. Mn7, Mp7, Mn8, and Mp8 transistors are used here.

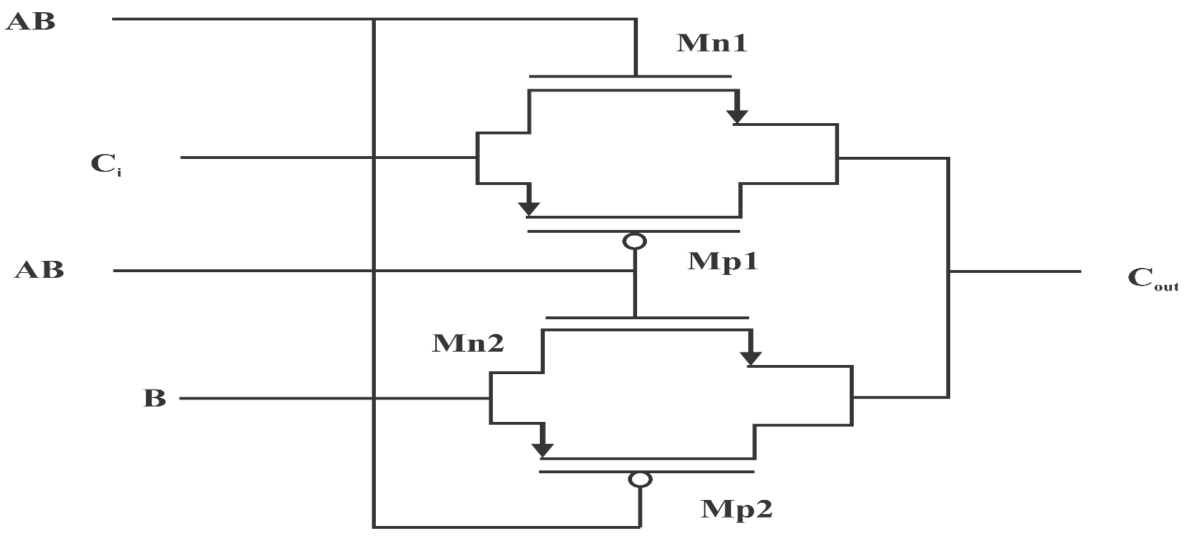


Figure 1.6 Carry Generation Block of Full Adder

1.4.3 Hybrid Adder Design

The design of the Adderfollows the standard practice of employing just transistors. With its modified low-power XOR and XNOR circuits, the Chang adder is designed with only 26 transistors. The delay issue can be addressed by employing additional transistors, but this design results in high power utilization. On the other hand, Goel adder with XOR-XNOR circuit produces a fully balanced swing output. Cross-coupling in these circuits makes them ideal for use in high-speed applications. Agarwal adders compute full swing output voltage based on the logic of complementary pass transistors. The "SUM" and "CARRY OUT" signals are generated by this hybrid Adder [35].

1.4.4 Full-Adder Categorization

a) Adder strategy and the ages of the Sum and Carry are separated into three distinct groups. The structure of the circuit may be deduced from these yields using a variety of reasoning lines. There are only three distinct families of complete adder architectures. There are three overarching categories into which the many conceivable structures for complete adders may be placed. The Sum and Count were derived from the following inputs: A, B, and C_{in},

$$A \oplus B \oplus C_{in} = SUM \quad A . B + C_{in}(A \oplus B) = C_{out}$$

b) Adder featuring XOR and XNOR logic gates-

The resulting Sum and Carry are the result of the subsequent condition [36], where H is A⊕B and H' is the supplement of H.

$$A \oplus B \oplus C_{in} = H \oplus C_{in} = SUM \quad A . H' + C_{in} . H = C_{out}$$

c) Complete Adder layout with XNOR-XNOR circuit-

The Sum and Carry outputs are generated by the expression shown below.

$$(C_{in} \oplus B) \oplus (C_{in} \oplus A) = SUM = H . A . H' + C_{in} . H = C_{out}$$

d) Automated Full-Sum Adder with a Central Location

The corresponding articulation produces the Sum and Carry-

$$\mathbf{H \oplus C_{in} = H . C'_{in} + H' . C_{in} = SUM \; A . H' + C_{in} . H = C_{out}}$$

1.4.5 Effect of Leakage Current and Power on Hybrid Full adder

Dynamic power dissipation is the result of load capacitances being charged and discharged. Bits that change from "0" to "1" or "1" to "0" use more dynamic power than bits that stay the same. It allows the transistors to function at their active and cutoff regions when the current is at its maximum. [37]:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}{}^2}{2}\right) \quad (1.1)$$

For active region, the current equation is:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{th})V_{DS}\right) \quad (1.2)$$

For saturation region, the current equation becomes:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left(\frac{V_{DS}{}^2}{2}\right) \quad (1.3)$$

Leakage characteristics due to lower threshold voltage and high packing density indicate that total power consumption does not lessen to any significant degree even if performance increases with scaling down of technology to a relevant level. In 2014, ITRScame to the conclusion that the average yearly drop in feature size was 13%. As more and more memory is manufactured in large quantities, its per-unit price drops. As feature size decreases, gate oxide thickness decreases, increasing gate tunneling leakage current [38].

There are four parts to power dissipation in digital circuitry:

$$P = P_{ds} + P_{sc} + P_{sb} + P_{leakage} \quad (1.4)$$

Where P is the whole power lost, P_{ds} switching mechanism a dynamic, P_{sc} is the short circuit, P_{sb} is the static-biasing and $P_{leakage}$ is the leakage power.

In dynamic-switching, the dissipated power is a function of switching frequency, capacitance value, and supply voltage (i.e).

$$P_{ds} = CV^2 f \quad (1.5)$$

The power dissipated in a short circuit varies with the clock frequency f and the rise or fall time.

The formula is:

$$P_{sc} = K(V_{dd} - 2V_{th})^3 \tau f \quad (1.6)$$

Leakage power is the amount of power lost when Vdd is drained away in the form of a static current flowing to ground.

Leakage may occur in three different ways: below the threshold, through band-to-band tunneling (BTBT), or via the gate oxide. [39].

$$I_s = I_o W e^{\frac{V_{gs} - (V_{t0} - \eta V_{ds} - \gamma V_{bs})}{n V_T}} \left[1 - e^{\frac{-V_{ds}}{V_T}}\right] \quad (1.7)$$

Sub-threshold slope coefficient n, gate oxide capacitance C_{ox}, and sub-threshold leakage current I_s are all accounted for in this formula.

Band-to-band tunneling is insignificant and may be ignored, but sub-threshold leakage current and gate tunneling leakage currents are considered. When we supply V(t) or I(t) to a Hybrid Full adder, which may indeed be utilized as a switch, the resistance varies dramatically. The voltage is considered to be constant while computing the power dissipation throughout a single switching operation [40]. The charge adjustment that must be done in order for a resistor to change from Ron to R_{offas} well as from time ton to toff is provided by [41]

$$E_{switch} = \int P_{switch} = \int \frac{\mathcal{V}^2}{R(t)} dt = \mathcal{V}^2 . \int_{t_{off}}^{t_{on}} \frac{dt}{M(q(t))} \quad (1.8)$$

Consider that $dq = \imath t$, can be rewritten as:

$$\mathrm{E_{switch}} = \mathcal{V}^2 . \int_{\mathrm{Q_{off}}}^{\mathrm{Q_{on}}} \frac{d\mathrm{q}}{\mathrm{I(q)M(q)}} \quad (1.9)$$

Inputting $V = \imath(q)M(q)$ and then $\int \frac{dq}{V} = \frac{\Delta Q}{V}$ yields:

$$E_{switch} = \mathcal{V}^2 . \int_{Q_{off}}^{Q_{on}} \frac{dq}{V(q)} = V.\Delta Q \quad (1.10)$$

where $\Delta Q = Q_{on} - Q_{off}$. So, to change from R_{on} to R_{off} in a resistor, the charge must be changed by ΔQ.

The voltage is considered to be constant while computing the power dissipation throughout a single switching operation [42].

1.4.6 Technology Scaling

In the course of recent decades, CMOS innovation scaling has been an essential driver of the gadgets business and has shown a way toward both denser and speedier mix. The transistors produced today are 20 times speedier and involve less than 1% of the territory of those assembled 20 years back.

The quantity of gadgets per chip and the framework execution has been enhancing exponentially during the recent two decades. As the channel length is diminished, the execution enhances, the power per exchanging occasion diminishes, and the thickness progresses. Yet, the power thickness adds up to circuits per chip, whereas the aggregate chip control utilization has been expanding.

The requirement for more execution and joining has quickened the scaling patterns in practically every gadget parameter, such as lithography, powerful channel length, entryway dielectric thickness, supply voltage, gadget spillage, etc.

Some of these parameters are moving toward key points of confinement and other options to the current material. Similarly, maybe structures ought to be distinguished with a specific end goal to keep scaling. The primary coordinated circuit flip flounder was imagined by J Kilby in

1958 at Texas and in 1963 the main CMOS rationale door was portrayed by Frank Wanlass at Fairchild [43].

Moore's law is known for the headway of CMOS development. As indicated by this law, the transistor check gets multiplied due to the consistent scaling downat regular intervals. Gordan Moore watched that the quantity of parts for the most complex coordinated chip gets multiplied every year for the following ten years.

1.4.7 Latest trends in Hybrid Full Adder

In electronics, there are a lot of developments in trend because every day, new gadgets and devices come into the world, providing better performance. The latest technology has a better performance than what we are now using. The circuit's power consumption is the single most important parameter and all the more as engineers are running on the power consumption. They all have reduced the transistor size, replaced the circuit with a new one, and then tried to make it more than good to back.

1.4.8 Application of Hybrid Full Adder

So many applications utilize the characteristics of hybrid full Adder for design simplification or enhanced performance. These are some applications which perform with the help of Full Adder.

Circuit complexity: -A full adder is a circuit which reduces the size and makes the circuit easier.

Ripple carry: - It can be utilized to develop a ripple carry counter for including a n-bit number. Subsequently, it is utilized as a part of the ALU too.

1.4.9 Advantages and Disadvantages of Hybrid Full Adder

1.4.9.1 Advantagesof Full Adder

First, the suggested hybrid GDI approach yields better power, latency, and area performance in simulations of various digital circuits than the status quo or industry standard.

Developing highly efficient and easily transportable electronic gadgets would benefit significantly from real-time implementation.

The traditional CMOS approach and various parallel methods like PTL, TG, and the current GDI methods are used to design elementary gates like AND, OR, and XOR doors with two inputs. While GDI is quickly becoming a viable alternative to CMOS for complex circuit configurations, it still struggles with a limiting decrease in voltage.

The static CMOS approach and the GDI process with swing reclamation buffers are compared with the help of shown circuits. Power, latency, and transistor Cout are utilized as comparison criteria.

1.4.9.2 Disadvantages of Full Adder

The switching power created by charging and discharging capacitances is a significant component in CMOS's low yet rapid power consumption. Firstly, as the speed of the circuits rises, so does the frequency and the power consumption. Secondly, tiny transistors made the dense architecture of the circuit possible, but interconnectivity still puts a cap on density.

Thirdly, using a pass transistor lowers the logic level. The gate will eventually find its logical equilibrium if noise stays below acceptable bounds.

Fourthly, the Adder circuit's main flaw is its lack of robustness against voltage scaling and transistor estimation.

Fifthly, a N fan-ingate may be achieved using 2N transistors. This may lead to an enormous implementation zone.

Last but not the least, it needs pMOS and nMOS transistors on each input, and the pMOS transistors add much capacitance. [44]

1.5 Gap in Conventional Full Adder Cell of 1-Bit

A typical CMOS adder cell for 1 bit of data consists of 28 transistors, as shown in Fig. 1.7. Throughout the rest of the essay, we will assume this situation always occurs. The "Base case" is utilized in all of the calculations. One technique to aid in creating low-power, high-performance systems is to use fast adders in multiplier circuits [45]. Adders are the foundation of any multiplier architecture; therefore, they must be considered early on. When it comes to the static CMOS design philosophy, transistor size plays a pivotal role. In CMOS circuits, MOSFETs (Metal-Oxide-Semiconductor et al.) of both p-type and n-type are employed [46]. Polysilicon and diffusion combine to form complementary metal-oxide-semiconductor transistors (devices), with N diffusion for N devices and P diffusion for P devices. Every product is a connected pair of metals. Contacts may generate either metal-polysilicon or metal-diffusion interactions [47].

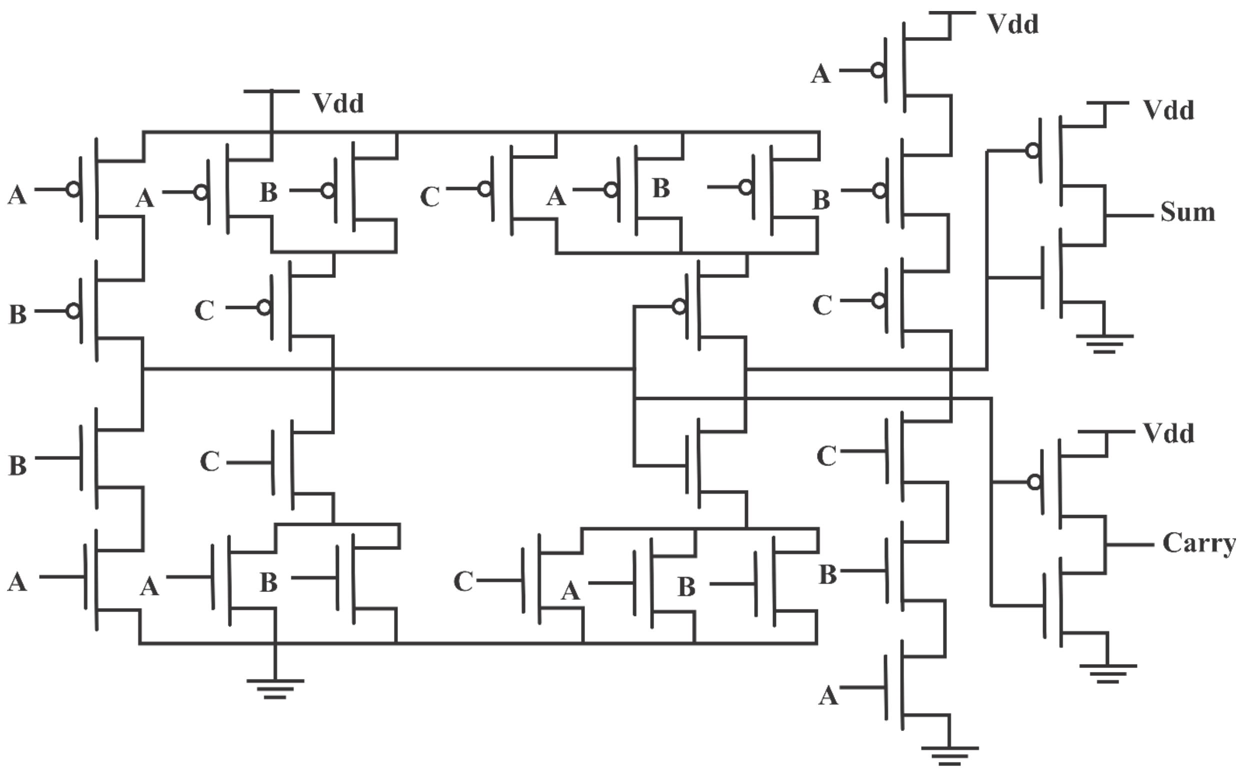


Figure 1.7 Schematic of Conventional 1-Bit Full Adder [49]

The CMOS architecture combines the pull-up features of PMOS with the pull-down features of NMOS for optimum performance. In this layout, each kind of transistor (PMOS or NMOS) has its own branch, and some of those branches may further split off into even more sub-branches. Yet leakage current has increased dramatically and currently constitutes a considerable proportion of total energy consumption [48]. This method has become the de facto benchmark for most 1-bit full adder cell enhancements [49]. Numerous approaches are proposed for constructing a full adder, each of which involves giving something up in terms of noise margin, area, or something else. The design procedure needs to be revised since this gain comes at the expense of parasitic effects like load sharing. When it comes to longevity and dependability, no other design method stands in comparison to the CMOS design method [50].

1.5.1Full-Scale Static Adder

Using static CMOS logic approaches, low-power 1-bit adder cells were realized. Complementary CMOS and Pass-Transistor are the two most common forms of logic circuits. 32 transistors are used to implement CPL's swing restoration using complementary pass logic [51]. Because of its robustness against voltage scaling and transistor sizing, the complementary CMOS architecture is preferred for applications requiring reliable operation at low voltage and arbitrary transistor sizes. Constructing a complementary CMOS circuit is straightforward and space-saving because of the use of paired complementary transistors and fewer connecting wires. Figure 1.9: Typical Static Full Adders

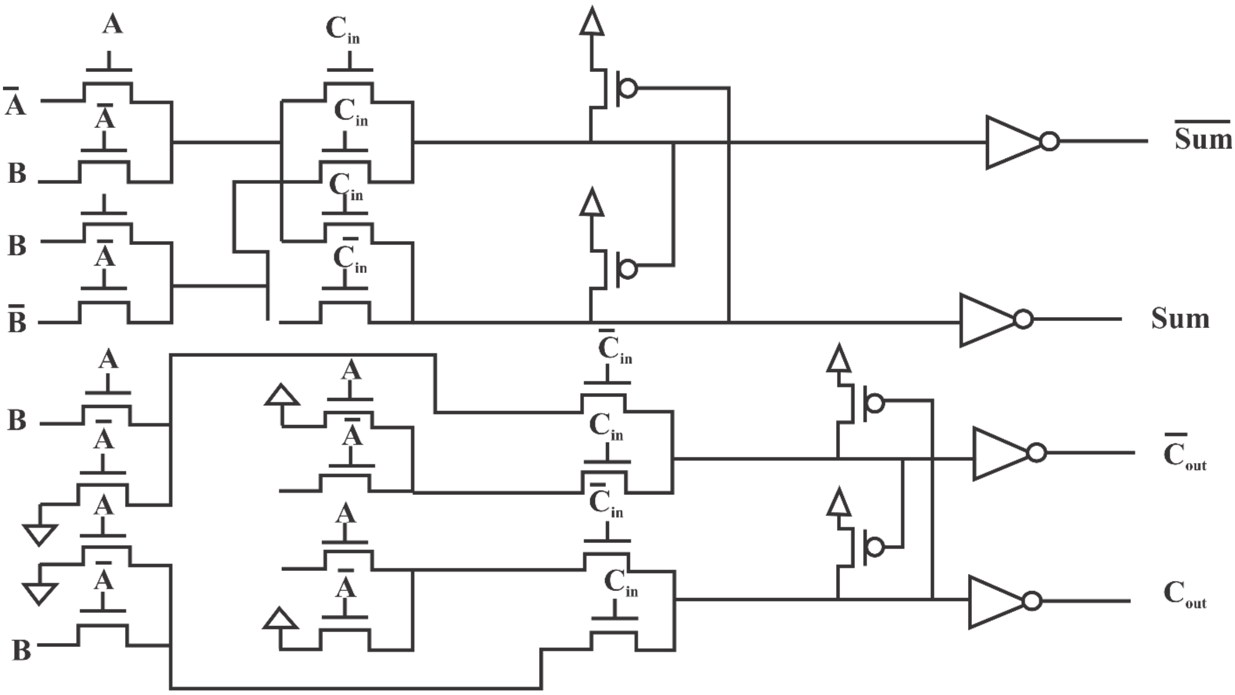


Figure1.8 Conventional Static Full Adders in CPL Full Adder Cell

This Research used standard topologies for implementing full-adder cells as a reference point. Complementary CMOS (C CMOS) full adders employ 28 transistors for addition, whereas Complementary pass-transistor logic (CPL) full adders require 32 transistors [52].

1.5.2DYNAMIC FULL ADDER

In most cases, there are two steps to dynamic logic. If your design has an output node connected to VDD through a precharged PMOS transistor, you'll need a pull-down network made up of NMOS transistors. Setting Clock to 0, starts the charging phase, while setting it to 1 initiates the testing phase of the circuit. All input values must be adjusted during the pre-charge phase to avoid the charging sharing problem and incorrect operation. This is because there will be no way to recharge the output once it has been depleted during the evaluation phase until the pre-charge phase starts. The Sum output function is defined by the following equation [53].

$$Sum = Carry\,(A + B + C) + A.B.C \tag{1.11}$$

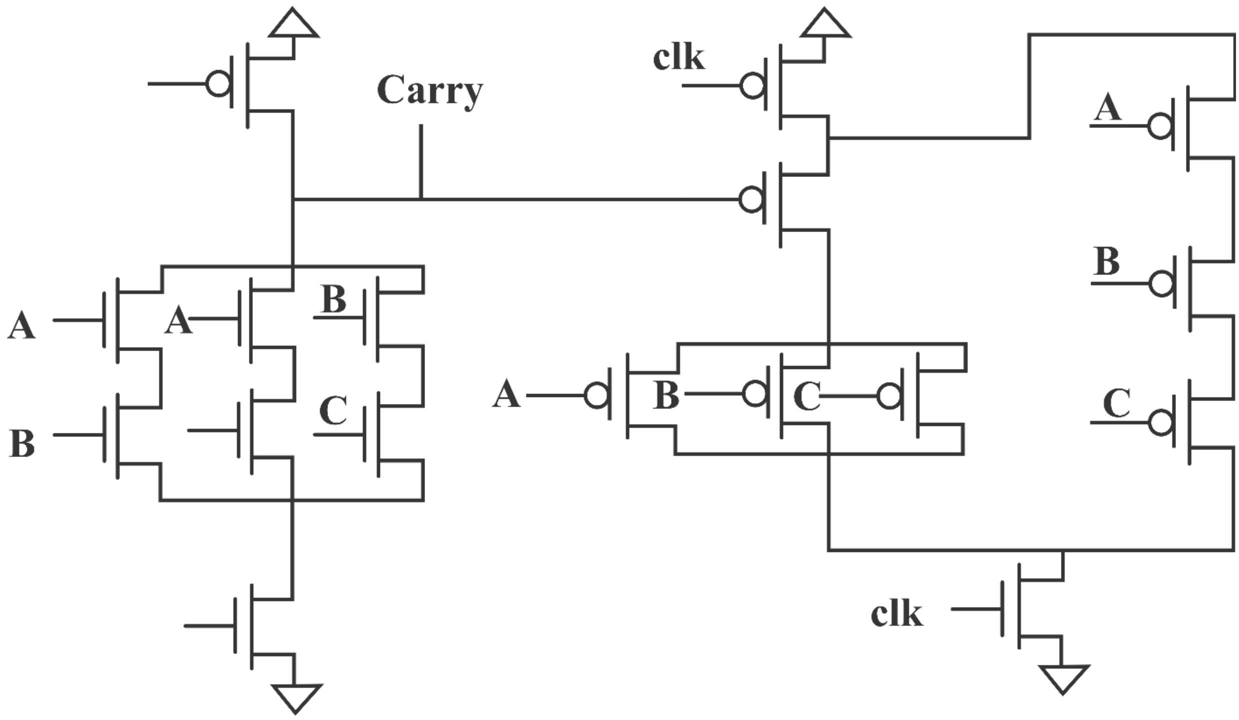


Figure1.9 Conventional Static Full Adders in CPL Full Adder Cell

Figure 1.9 depicts the design of a conventional NP CMOS full adder. The NP-complete dynamic full adder [54], as shown in Figure 3, is constructed in a complementary CMOS circuit. This design uses the standard two-stage Zipper (NP) method to develop dynamic design CMOS circuits. NP complementary dynamic CMOS systems have the advantage in performance but use much power.

1.5.3 Research Gap

Several studies on low-power, high-speed full adders with output dynamic capabilities have been published [55]. The 28-transistor complete Adderwas the first of its kind in this list. The pull-down and Pull-up networks of this Adder were implemented using just Complementary Metal Oxide Semiconductor (CMOS) elements. This Adderhad a high noise margin but with certain drawbacks, such as a larger footprint and higher power requirements. To solve this shortcoming of 28T full adders, 20T transmission gate full adders were released. The circuit for this transmission gate adder comprised 2 sets of 8T XOR connected by two inverters. Before then, this Adder had the reputation of being the quickest of its kind. With this, although the power-consumption drawback of a larger chip was mitigated, the disadvantage of a larger chip's footprint stayed on. After some time, a second 14T complete adder entered the electronic market. Even then, the drawback of power consumption still lingered, despite this complete Adder. Up to that point, 14T speed was sufficient, but power was an issue [56]. Therefore, eventually, a complete adder capable of reviving 10T of static energy was made available. It used less power than a standard CMOS full adder since it recycled the charge for efficiency gains. One of the benefits of the circuit, in terms of energy efficiency, was that it did not have a direct connection to the earth. Reapplying the charge held in the load capacitance to the gates increased the leakage and delay of the whole circuit, affecting the transistors' threshold voltage.

Afterwards, a 10T complete adder was created, utilizing the gate diffusion method. Thus, GDI XNOR and XOR were used to resolve the circuit's high power consumption issue, and it has now switched to operating on low power [57]. Nevertheless, the need for dual well CMOS in GDI for manufacture or silicon on insulators reduced the driving capacity of complete adders. Moreover, GDI infrastructure was costly. The subsequent development of the 9A and 9B full adders modified the 10T full adder, allowing it to function at higher frequencies while still using very little energy.

Thanks to this development, an 8T complete adder is now the standard. For SUM and Cout, it utilizes a pair of 3T XOR gates and a pair of 2T MUXs. Compared to a complete adder implemented in 28T CMOS technology, this Adder demands far less space on the device and uses much less energy. This circuit began to create a short circuit current after being supplied electricity for an extended period, which eventually raised the circuit's minimal power consumption. Considering the benefits of both full adders and hybrid adders, it is decided to concentrate on developing a low-power hybrid adder that could achieve higher processing speeds using less energy [58].

1.6Source of Power Dissipation in CMOS

1.6.1Oxide Tunneling Current (IG)

The field across the oxide increases when gate oxide thickness is decreased. As the oxide is very thin and the electric field is extremely high, electrons are able to tunnel from the substrate to the gate and back again, causing the tunneling current [59-64].

1.6.2Short-Circuit Power Dissipation

Under certain switching conditions, CMOS gates may cause a short circuit between the power supply and ground. This happens if the CMOS gate only allows current to flow from the supply to the ground. This kind of power loss is referred to as short-circuit power dissipation. Since input waveforms at the gate have distinct peak and fall phases, power is dissipated during these times. The value may be reduced by decreasing the supply voltage [65]. When dynamic logic circuits' pre-charge and evaluation stages run in parallel, no power is wasted due to a short circuit. Adder modules extract power in proportion to the capacitive load they experience at their inputs. Even worse, when the module lacks direct power supply connections, the inverters connected at the total adder inputs deliver the power required to charge and discharge the full adder internal nodes. Since the full Adder is given flawed signals from the associated buffers rather than perfect ones from voltage sources, it will eventually short-circuit and consume itself. Short circuits and static dissipation are more likely to occur in inverters that are attached to the entire Adder's output signals due to the signals' shallow slopes and less voltage swing [66].

1.6.3Dynamic power

In CMOS VLSI circuits, dynamic power consumption is responsible for the majority of power loss. Power is dissipated whenever the load capacitors in a circuit are connected to or disconnected from the supply. The input pattern determines the frequency of transistors switching (so use dynamic power) within a given clock cycle. In other words, the dynamic power loss originates in the charging procedure. It is possible for dynamic power to be wasted even if the output net's logic state does not change due to a voltage change on the input net. This component of the dynamic power dissipation is caused by the charging and discharging of parasitic capacitances in the circuit. [67].

1.7Motivation of the Research

Multiplication, a simple but common mathematical action, slows down many Very Large Scale Integrated Circuits (VLSI) like DSP designs, microprocessors, and so on. The main job of an adder cell is to add two binary numbers. This shows the importance of adder speed is in VLSI systems. The goal of this thesis is to undergo a thorough study of how single-bit full adder cells work in terms of time delays and power use in situations where low power-delay products are very important.

Leakage power can be curtailed in several ways in different single-bit full adder cell designs. The best way to look at the cells is in a 45-nm CMOS setting. Performance data can be used to develop cell designs with low leakage power, leakage current, and delay. Microprocessors and Digital Signal Processors (DSPs) can't be made without full adders. In this Research, we combine new XOR and XNOR by-gates with existing ones to demonstrate 41 new 10-transistor complete adders. Over ten thousand Cadence simulations of various adders have been conducted. Different inputs, frequencies, and capacitances were used for each simulation. Three of the new adders are consistently 10% more efficient and quicker than the previous 10-transistor full Adder and the conventional 28-transistor CMOS adder, despite most of the new adders consuming less power at higher frequencies. Leakage current could be slashed greatly if the structure is stacked while the device is in sleep mode. What does this mean for the age of low-V_{th} transistors and the nanoscale size regime? Traditional power control schemes need a new design to cut leaking current a lot during rest.

Two NMOS transistors connected in series provide the ground link in a logic circuit. Design variables, such as leakage current, leakage power, and delay, for frequency virtuosity at 45nm technology were discovered after our analysis of the 1-bit full Adder and the full Adder using the power gating approach and the stacking power gating method. It is worth mentioning that fewer transistors are required to create a 1-bit full adder, which is equally effective. Low-V_{th} devices assist in reducing the clock time on critical delay lines because they switch ON and OFF rapidly. However, this results in a significant increase in static loss power in low V_{th} devices. On the non-critical line, devices with a high V_{th} are used to cut down on static electricity leakage without consuming more time. Static power can be reduced by a factor of 10 with most high-V_{th} devices. Nanoelectronics circuit devices are becoming more common as they use less power and have fewer leaks. This makes it hard to build VLSI circuits and systems today. By changing the cutoff voltage, source voltage can be lowered. This makes the power quieter and the control circuits most accurate. We provide a novel 10T Hybrid Full Adder (HFA) cell that utilizes a compact Junction-Less Double Gate (JLDG) MOSFET architecture on Silicon on Insulator (SoI). It employs a Negative Differential Forbearance (NDF) mechanism in addition to a dual logic approach. A 10T Junction-Less Double Gate Hybrid Full Adder (JLDGHFA) cell was evaluated using a number of Ultra-Low Power methods (ULPT), including MTCMOS, Tri-Mode MTCMOS, and SVL. Using the normal ways to build circuits makes sure that an idle circuit's leaking characteristics will be reduced. For low power, the analysis results show that the leakage current is curtailed by 24.11 percent while the leakage power is expurgated by 24.09 percent. Tri-mode MTCMOS is 98.5 percent better than MTCMOS and SVL at reducing the amount of power and current that is wasted. The Cadence Virtuoso Tool was used to make the suggested circuit layouts and low-power methods work. Lastly, we talked about the safety features that need to be built into a 45nm CMOS 8T full adder. For low-power circuits, lowering the source voltage until it meets the cutoff voltage is a good idea, but it shortens the life of the circuit. This study examines this event by adding different voltages (0.7V, 1V, and 1.2V) over the course of a year.More functionality, low power, extended lifetime, and the requirement for increased integration in VLSI circuits are the elements that drive the trend towards downscaling CMOS technology, which is equivalent to Moore's principle. Several difficulties multiply and undergo physical alterations as this degradation grows to the micro scale. An electrically active interface trapping resulting in the dissociation of passivity Si-H bonds at the gate oxide, NBTI in PMOS and HCI in NMOS, has become one of the most notable concerns in reliability during aggressive down scaling of CMOS transistor. As a result, the device's efficiency drops and eventually breaks. There is a comparison between the 6T and 5T SRAM cells that was suggested by ShyamAkashe et al. This work details the reliable study of PMOS transistors subjected to NBTI deterioration, NMOS transistors subjected to PBTI degradation, and HCIs subjected to both types of transistor degradation, among other models. We compute the NBTI, PBTI, and HCI methods, assess the leakage parameters and the average noise margin. Whole adders have been built using logic gates by Walid Ibrahim et al. Whole device reliability estimates are extrapolated from gate-level evaluations of dependability. It helps in evaluating the potential cause for failure. An adder is a crucial part of any computing or logic system. VLSI design is shifting in response to a growing need for low-power devices. Low-power applications may benefit from adiabatic logic-based circuits. Predictive technology characteristics for 180nm technology are used in the design of complete adders. A comparison is made between different complete adders developed. With the number of transistors needed to build a complete adder, the time it takes for signals to travel through them, and the average amount of power they use at various input frequencies and capacitance loads. A complete adder built using static CMOS is also evaluated and compared to the findings. It has been discovered that complete adders constructed using adiabatic logic methods need much less energy than those crafted with static CMOS logic. It has been noted that the cost of reducing power consumption leads to increase in propagation latency. One adiabatic design of a full adder delivers up to 89% power savings compared to a full adder developed using static CMOS circuitry under specific operating circumstances. It's safe to say that the system's performance is mostly dependent on how the critical path transistors act.

In conclusion, the adders' performance is critical to the VLSI system's capability of functioning with the current battery technology; however, researchers are torn between two competing design challenges: (1) exploring high-performance design and implementation techniques that can meet the stringent speed constraints for real-time systems, and (2) thinking about low-power design approaches to lengthen the operating time of portable devices. You may quickly evaluate fundamental differences between the various building-block designs by comparing their power-dissipation and leakage current. The complementary pass-transistor logic is yet another standard adder (CPL). Large power dissipation may be attributed to a high number of static inverters and internal nodes. Transmission Function Full Adders (TFAs) and Transmission Gate Full Adders (TGFAs) are two further examples of full adder architectures

(TGA). The primary drawbacks of these logic types are their lack of driving capabilities and a radical drop in performance that occurs when TGA and TFA are cascaded. It is possible to divide these Full adder architectures into three sections.

1.8Research Methodology

Here are some of the main things this study will add to the field:

1. To explore various logic styles for designing hybrid Adder for low power.
2. To propose a novel architecture of a one-bit hybrid adder.
3. To demonstrate the proposed design for multi-bit Adder.
4. In order to evaluate the suggested designs,we will look at their speeds, power consumption, and transistor-equivalent Couts.

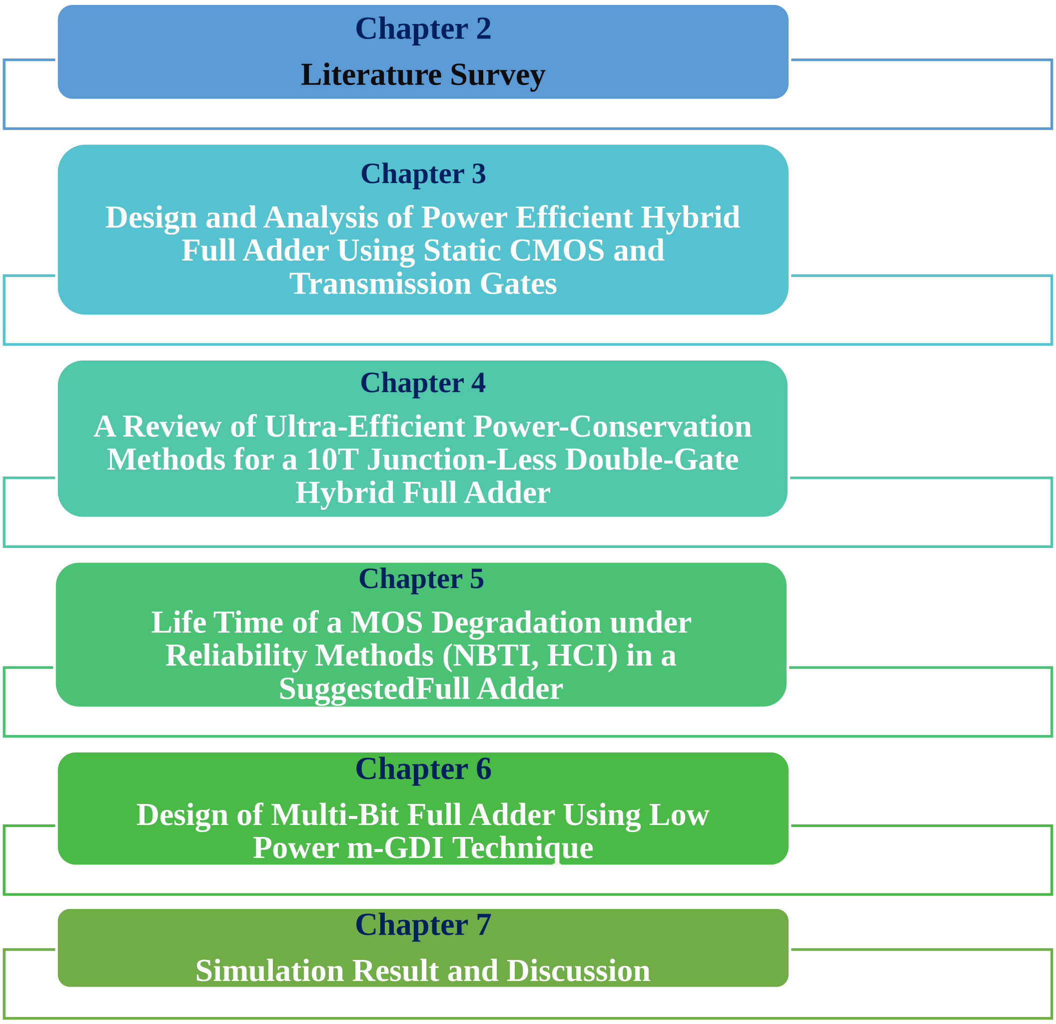


Figure 1.10Organization of Thesis

1.9 Organization of The Thesis

Figure 1.10 shows the structure used to divide the Research in this thesis into seven sections.

Chapter 1 In this chapter, we'll learn about hybrid models, why they're useful, how many hybrid models are available, and how they're related to the construction of Full adder models. The thesis covers a wide range of topics, from the need of Hybrid models in VLSI circuit design to the transistor C_{out} in VLSI design to the description of non-volatile developing technologies and power challenges. Additionally, it demonstrates thesis structure.

Chapter 2: Provides an exhaustive literature review on cooperative diversity in Hybrid models and different resource allocation techniques in Full adders. Hybrid models resource allocation in cooperative Full adders is also discussed. Further, limitations in the existing studies, problem formulation and research objectives are also presented.

Chapter 3: By analyzing the power consumption of a 1-bit full adder, a full adder using the Power Gating technique, and a full adder using a stacked power gating methodology, we can estimate a number of design characteristics, including leakage current, leakage power, and latency, in cadence virtuoso at 45nm technology. Implementing a 1-bit Full Adder with the same functionality and fewer transistors has several uses. In order to shorten the clock time, low Vth devices are preferable on critical delay lines due to their faster switching speed. Low Vth devices have a lot more static leakage power to make up for it.

Chapter 4: This section has introduced Junction Less Double Gate (JLDG), MOSFET and 10T Hybrid Full Adder (HFA) using ultra-low power approaches (Multi-Terminal Complementary Metal Oxide Semiconductor Logic) such as MTCMOS, Tri-Mode MTCOMS, and SVL.

Chapter 5: We look at how the NBTI and HCI dependability characteristics fare under different operation conditions and over a year.We compare and contrast the degradation and aging of NMOS to that of PMOS, namely the occurrence of Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI). Simulation results indicate that the NM2 transistor's HCI impact is significantly hindered at low voltages and gradually reduces at high voltages but that the NM2 transistor will ultimately cause circuit damage.

Chapter 6: The evolution of full Adder from CMOS logic to hybrid logic design has taken a significant step in ALU's smaller and compact design. This chapter uses a principle concept of m-GDI logic to build a low power and relatively less area whole adder block. Different design structures are compared according to the corresponding input bits in the chapter. This study helps realize a better design structure for implementing the full Adder in ALU.

Chapter 7 Provides the conclusions drawn from the Research and outlines the possible extensions of this work in the future. The thesis concludes with a list of publications and references found useful throughout the research work.

CHAPTER 2

LITERATURE SURVEY

The research and development of high-performance arithmetic circuits has long been attracted ASIC processor designers. Due to this, there have been several attempts to lessen the circuits' need for power and delay time. This section provides a literature review of the past research in this topic.

2.1Single Bit Full Adder Cell Topology

2.1.1. Transmission Gate Full Adder

Microprocessors and Digital Signal Processor (DSP) designs are among the applications that need the utilization of complete adders. The primary use of cardinal numbers is to denote addition, however they also hold significance in subtraction, multiplication, division, and the computation of addresses, among other mathematical operations. In many instances, the adder is situated along the critical pathway that governs the overall throughput of the system. Therefore, enhancing the efficacy of the essential constituent of the adder is imperative, and the 1-bit full adder cell necessitates low-power consumption. In response to the growing demand, a unique complete adder was developed [68]. This innovative design aims to minimize power consumption while ensuring efficient processing of numbers, making it particularly suitable for implementation in tree-based architectures. A unique full adder is built by utilizing a buffer inverter at the output and a complementary signal at the input. This newly developed adder has exceptional driving capability and little power consumption, while being constructed with a mere 20 transistors. The utilization of this adder facilitates the realization of high-performance circuits, such as quick and low-power multipliers. The authors of [69] conducted a comparison between CPL logic and logic circuits including 20 transistors. The study determined that the design of a Transmission Gate Full Adder circuit is comparatively simpler when compared to that of a conventional CMOS Full Adder. Although this design has the advantage of generating SUM and CARRY outputs with buffers, it is accompanied by the disadvantage of using a significant amount of power.

2.1.2. Complementary Pass-Transistor Logic (CPL)

Using static CMOS logic and pass transistor logic, we developed a high-speed, low-power complete CMOS adder with three exclusive OR (XOR) inputs [89]. He also paid close attention to the entire adder's capacity to drive. Using 0.35 nm TSMC CMOS technology, he found that power consumption could be reduced by 35.6%, time delays by 11.7%, and power delay products by 91.4%. His study and design of the circuit prove that the suggested adder is fast, uses little power, has a negligible impact on latency, and can be implemented entirely on a single chip (SoC) [70].

The simulation of a 1-bit half adder using 90-nanometer, 70-nanometer, and 50-nanometer CMOS technology yields comparisons of power consumption and chip size as performance metrics [71-73]. The analysis reveals that adopting 70 nm CMOS technology reduces power consumption by 67.15 percent and surface area by 50.94 percent compared to the suggested 1 bit adder implemented in 50 nm CMOS technology, which reduces power consumption by 94.9 percent and surface area by 75.09 percent.

Parasitic capacitance, transistor size, and delay were determinants limiting the switching speed of the circuit [74]. He analyzed and compared the entire adder's driving capacity, power consumption, chip size, and latency as it went from 28 to 8 transistors.With recuperation of Static Energy in addition to a complete adder (SERF), his paper has a GDI full adder, anAdder 9A full adder, and aAdder 9B full adder. He found that the GDI type full adder used the least amount of power, while the TG based full adder had the shortest average latency but the smallest power delay product of any full adder. In conclusion, the 8T full adder outperforms the competition.

2.1.3. 14 Transistor Full Adder Cell Design

Many arithmetic operations, including addition, subtraction, multiplication, and division, rely on adder as their principal building component. Hence, developing a fast full-adder is a very valuable and crucial endeavor. Yet, with the development in popularity of mobile devices like smartphones, PDAs, and laptop computers, there has been a corresponding increase in the need for VLSI circuits that are both small in size and low in power consumption. [75] advocated an FA based on 14 transistors and 3 capacitors, all built using carbon nanotube field effect transistor technology. In addition to the new design, seven additional schemes are used, such as the Hybrid scheme and three Full Adder schemes that are not based on the results of past majorities.

Reduced delay times are only one indicator of the success of the simulation. [76] used pass transistors to build a generic full adder circuit using exclusive OR and NOR circuits. In the conventional complete adder, we propose a CMOS XOR circuit with six transistors that also generates an XNOR output. A full adder circuit is produced with only 14 MOSFETs,with complete voltage-swing at all circuit nodes. By reducing the number of MOS transistors, [77] suggested a novel low power adder cell that significantly outperforms the static energy recovery complete adder in terms of speed and efficiency.

2.1.4. Static Energy Recovery Full Adder Cell

Non-energy recovering logic requires more power than energy recovering logic since the former wastes less energy. An innovative static energy recovery complete adder with low power consumption and transistor count was created in [78]. The SERF adder is then compared to a standard full adder in terms of its power requirements and other general properties. As compared to complete adder cells, the energy consumption and number of transistors in the proposed low power energy recovery logic are both lower. An innovative complete adder architecture with as little as 10 transistors per bit was presented in [79]. It has been shown that the suggested cell can function within the supply voltage of reduced transistors. He employed six transistors to get a low threshold voltage drop in the MOS transistor and a low supply voltage operating cell.

Zimmermannet al. [80] compared standard CMOS to a newer technology called Complementary Pass Transistor Logic (CPL) and found that the latter was much more energy efficient. Nonetheless, he also concluded that CMOS is superior than CPL in terms of speed, power dissipation, area, and power delay products. Instead of using the more power-hungry CPL version, he switched to a 32-bit adder CMOS. He also established that CMOS offers other benefits, including resilience with regard to transistor size and voltage scaling. Based on his findings, CMOS logic is 20% slower than CPL logic, but it uses 29% fewer circuit nodes and 41% less transistors on the device.

Twenty distinct kinds of 1 bit full adders were analyzed by A. Shams et al. [81]. Each adder has unique characteristics in terms of speed, drive capacity, area, power consumption, and power delay product. In conclusion, he offered the most suited cell for improved driving power and the other characteristics after comparing every innovative module of the adder cell.

The power delay product, driving capabilities, power consumption, and speed of several one-bit hybrid adder topologies were examined and contrasted by M.Aranda et al. [82]. Simulation work was carried out using TSMC 180nm CMOS technology. We found that whereas Chang adder performed best for PDP, Aguirre adder excelled in terms of driving ability and low power consumption.

M.Vesterbacka [83] showed how to build a complete adder circuit using OR and NOR gates with pass transistor logic. We were able to create a complete adder using just 6T of CMOS technology by using an XOR circuit. Only 14 T, at full voltage, dangles from each of the circuit's nodes. Technology with a feature size of 0.34 nm was used for simulation. He tested the suggested adder's performance to that of a 16T adder and found that it had the same or better results, while using fewer transistors and taking up less space.

2.1.5. Gate Diffusion Input Logic (GDI)

As a means of catering to the expanding interest, [84] created a low-power 1-bit complete adder cell that uses GDI to generate XOR and XNOR operations in parallel. The 0.18-m CMOS technology used in the simulations was preferred because it delivered the best results. A novel low-power complete adder with just 24 transistors has been shown, that can function at voltages as low as 0.5V. In contrast to the first cell, which failed at supply voltages of 0.5V at 10MHz, the new one functions consistently down to 0.8V. In terms of power consumption, the recently suggested complete adder cell is far and away the winner. Figure 2.1 displays the fundamental GDI cell.

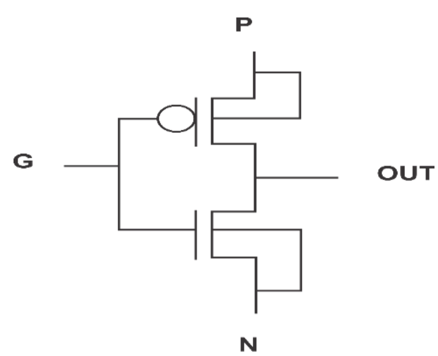


Figure 2.1 Schematic of GDI Logic

The low power 1-bit complete adder circuit design presented in [85] is presented with improvements. The circuit is known as a 10-T cell since it is built using a top-down methodology with a total of 10 transistors. After the circuit was simulated, its performance in terms of power, latency, and area could be seen clearly. A power reduction of around 60% was seen when the suggested circuit's performance was compared to that of other circuits published in different literatures. Since a complete adder is a ubiquitous part of digital circuits, its design has been refined repeatedly throughout the years. [86-88] by using a newly suggested design process known as GDI, four distinct kinds of 10-transistor (10-T) based complete adders presented (Gate-Diffusion Input). Using the GDI scheme, the XOR, XNOR, and MUX gates have been rethought. According to Figure 2.2, we can see that just 4 transistors are required to implement the GDI XOR gate. As compared to a traditional CMOS XOR gate, the GDI variant's reduced transistor count is immediately apparent. Hybrid adder based on carry look ahead and carry select adder combination was introduced by A.Husseinet al. [89]. The suggested circuit was realized in 0.18 m CMOS technology, with the majority of its sub circuits employing domino logic. At 125^{o}C, i.e., he was in the worst condition imaginable. As it was developed using dynamic logic, the architecture is pipelined and uses an average of 787.2w of electricity while delaying 100 mega operations by 876.7ps.

A Parallel Feedback Carry Adder (PFCA) was presented by P.Prashanthet al. [90] to reduce the computational time and space required by complete adders like the carry look ahead adder and the ripple carry adder. Furthermore, he noted that the PFCA complete adder would be most beneficial as it became bigger: low-power, full-bit, ten-digit adder (1-bit). When comparing the original ULP full adder to the BBL-PT full adder, it was found that the BBL-PT design offered four times the static performance and PDP of the CPL design. Delay and leakage power were also reduced, by 30% and 50%, respectively.

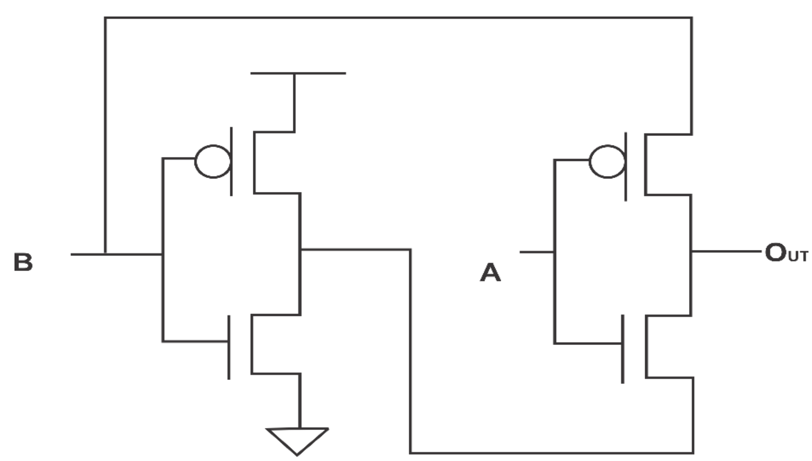


Figure 2.2 XOR Gate using GDI

2.2. Transistor Full Adder Cell (8T)

Clearly, when comparing the 8 transistor full adder to the 9 transistor full adder cell in [91], the 8T full adder has significant issues, particularly when Cin=0 and the circuit works in sub threshold areas. With just four input vectors, the logic level of the outputs is rather high. There is a significant drop in output voltage for the remaining input vectors, which may result in functional failure and higher power consumption that may be mitigated by the use of power reduction strategies. The silicon area and power-delay product have been significantly improved over previously suggested 4T and 6T XOR gates, thanks to this design. The suggested three-transistor XOR gate was used in the construction of an eight-transistor complete adder, and its performance was studied in 0.15- and 0.35-micron technologies.

In continuation, K.Naviet al. [92] developed a low-voltage MOS capacitor construction for a one-bit complete adder. The suggested circuit helped do away with the XOR gate that was adding latency. The recommended adder was compared to novel adders in PDP, power consumption, speed, and space efficiency. The results showed a 30% power saving compared to CMOS adders and a 1.11-fold speed gain compared to TFA adders.

When considering time, energy, and power delay product, M. Linares et al. [93] explored Topologies for one-bit hybrid full adders that are most likely to be useful. On a mentor graphics backdrop and with the help of TSMC's 180 nm CMOS technology, the investigation was completed with a precise replica setup and input prototype. Several supply voltage standards were also tested for the presentation. The simulation findings demonstrated that the Aguirre adder excels in driving capabilities even at low power supply, whereas the Alter adder excels in PDP figure of merit. Powered by 0.8v, the Aguirre adder has improved piece-even in a 10-level tree architecture. This finding is important because tree-structured equivalent multipliers are widely employed in modern high-speed applications.

M. Zhang et al. [94] recommended a novel architecture for a 1 bit full adder cell using hybrid CMOS logic. The pass logic method has been used to expertly generate the XOR and XNOR roles simultaneously, and the outcomes are superior in terms of drivability, thanks to the use of a novel complementary CMOS process with a standard structure. Over a large supply voltage range, this circuit has been found to be power delay frugal, making it an excellent choice for designing low power, high performance arithmetic logic components for embedded applications.A 1 bit complete adder was suggested by M. Zavarei et al. [95], which would use a hybrid CMOS logic design and would be composed of XOR/XNOR, SUM, and CARRY sub-circuits. Using Complementary Pass Transistor Logic (CPL) and transmission gate logic, the XOR/XNOR circuit may perform logical operations with a minimum number of gates (TG).

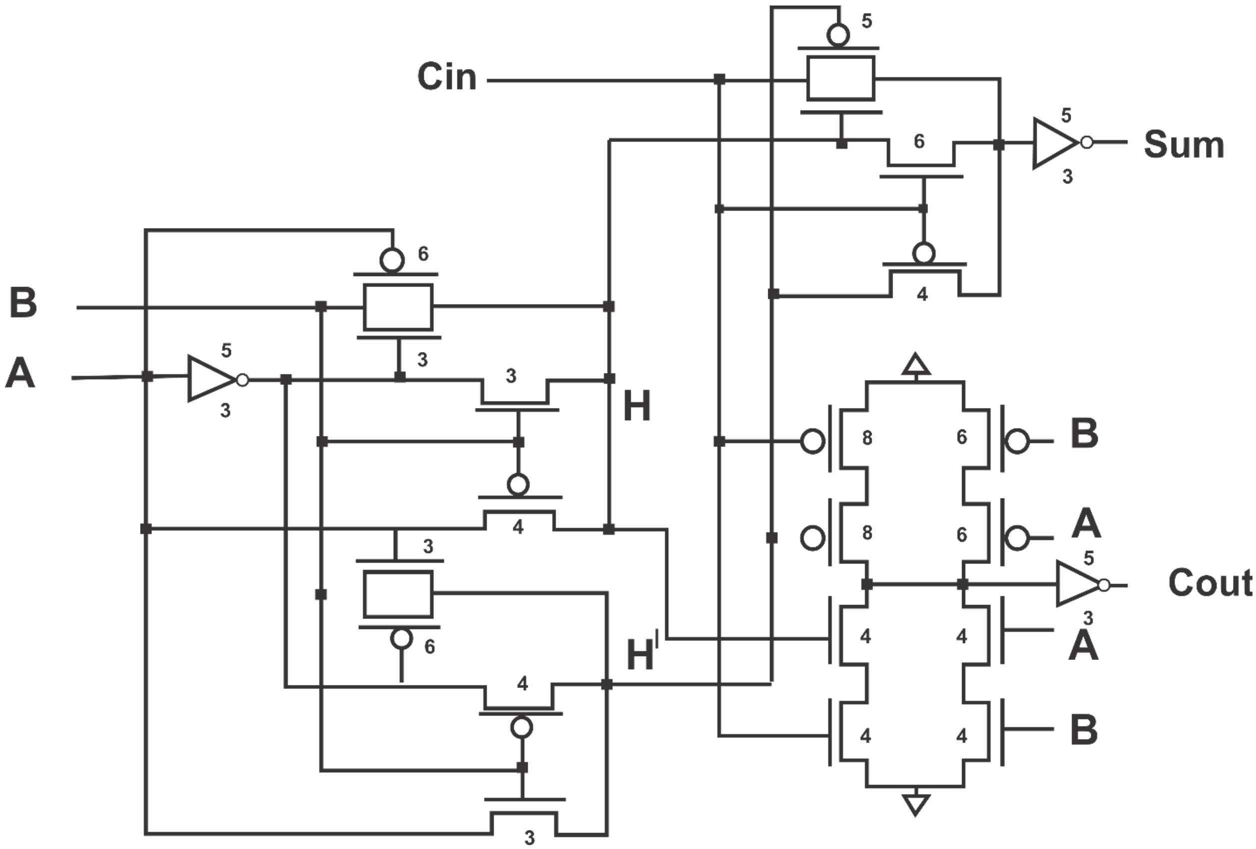


Figure 2.31 bit complete adder was suggested by M. Zavarei et al. [95]

Low-power operation can be achieved by combining various logic techniques. As compared to other recent full adder circuits, the new XOR/XNOR circuit uses the least amount of power. Results from a simulation show that the expected complete adder has low PDP under a variety of load scenarios. Hence, the expected full adder concert is satisfactory, since it maintains embed as a 4- or 8-bit full adder [96].

2.2.1Dynamic Domino Full Adder

For proper function, the Dynamic Domino [97] circuits go through a pre-charge phase followed by an evaluation phase, all of which is coordinated by the system clock signal. To get around the standard dynamic Domino full adder's well-known constraint in the gate implementation of inverting logic functions [98], the Dual-rail Domino circuit uses a differential version of the adder's logic. High performance circuits often use it due to its low latency [99]. The gate enters a precharge or an evaluation mode through a PMOS pair operated by the clock and an NMOS pull-down network. By using output inverters, we can eliminate the possibility of a race condition, and by using weak feedback PMOS transistors, we may decrease the charge-redistribution issue and thus, increase the noise immunity [100].

2.2.2Transmission Function Full Adder

This is a comprehensive adder based on the theory of Transmission Functions (TFA) [101]. This device, which was built using 16 transistors and uses transmission function theory, was conceived by an engineering team. The absence of driving ability is the primary drawback of TGA and TFA reasoning approaches. The efficiency of TGA and TFA decreases drastically when they are chained together. There are three inputs (A, B, and C_{in}) and two outputs (Sum and C_{out}). Although there is no issue with voltage loss, twice as many transistors are needed for the design function.

Two complementary transistors, one PMOS and one NMOS, are connected in parallel to form the device. When both PMOS and NMOS transistors are activated, they provide a route to either the logic "1" or "0" of the input. This means that passing "1" or "0" through it, causes no voltage drop. In this process, twenty transistors [102] are included. The performance of a complete adder with a majority function is lower than the performance of any other adders when TGA or TFA are cascaded. In comparison to other adders, however, it consumes much less power, has a significantly smaller latency, and has a smaller power delay product. The majority-function full adder uses fewer transistors than any other kind of an added.

Using the more common NOT gate, the author presents two innovative low-power 1-bit complete addersbyK. Naviet al. [103]. The design of every individual cell is built using an innovative technique. While the second cell benefits from a high concert CMOS bridge circuit, the first cell only has a CMOS inverter and a capacitor at its input. Our designs are geared around using as little electricity as possible. The planned complete adders in 0.18 m CMOS technology are modelled with all four supply voltages, from 2.4v down to 0.8v. Our research has shown that our circuits have the lowest Power Dissipation Potential (PDP) among all existing full adder designs.

A novel low-power inverter based on a one-bit full adder was proposed by K.Naviet al. [104]. A 1-bit full adder cell's efficiency, performance, and usefulness may be greatly enhanced by only adopting a simple 16-transistor configuration. Total adder cell size was calculated using

Synopsys, H-Spice, and cadence spectra simulations. Development of full-size, low-power, high-performance VLSI system is a good fit for the inverter-based full adder.

J. Wanget al. [105] offered two novel configurations of CMOS devices for exclusive OR and exclusive-NOR functionalities. Proposed solutions eliminate the need for complimentary signal inputs and limit the output end of a four-transistor arrangement to a single low-level signal. The suggested designs for all the 6 transistor types offer non complementary inputs, high quality signal outputs, and superior driving power. The simulation (HSPICE) results for 4 transistors and 6 transistors categories show that our designs are superior and more assertive than the competition.

2.2.3Pass-Transistor Logic Adder

In nMOS logic, pass transistor logic is a well-known approach used to accomplish a variety of functions. It's a vital aspect of a wide variety of other operations, including subtractions, multiplications, divisions, address calculations, and more. Most of the time, the adder is located on the crucial route that determines the system's total throughput. Theprincipal objective, therefore, is to improve the efficiency of adder's fundamental building component, the 1-bit complete adder cell. As a rule, selecting the control variable and the pass variable from the functional description is the first step in creating the pass transistor logic diagram for a function. Complementary PL (CPL) is predicated on the idea that logic operations may be implemented with a single nMOSFET network [106-110]. As a consequence, the input capacitance is kept small whereas the operating speed is kept high.

2.2.4Hybrid Full Adder

The goal of every hybrid design is to create a low-power full-adder cell [111-112], and to do so, the researchers combine the best modules available with those available but are implemented using different logic styles. To minimize power consumption, adder cells often include fewer transistors. This is made possible by the use of pass transistors or other low-power logic architectures such as TGA or TFA. With the Hybrid full adder, massive tree-structured arithmetic circuits may achieve ideal area efficiency without sacrificing VLSI power and time, thanks to the adder's balanced outputs, which set it apart from conventional adders. The overall performance of a large-scale multi-bit adder is greatly enhanced by the adder core due to the huge reduction in delay brought about by its implementation. It takes three main components [113] to make a hybrid full adder circuit. We have the options of XOR and XNOR, as well as a carry and sum generators.Subsequent developments included more transistors, and consequently, more individual termination points or frameworks were eventually joined. Initially, integrated circuits contained only a few components, perhaps up to ten diodes, transistors, resistors, and capacitors, making it possible to create multiple logic gates on a single device. Medium-Scale Integration (MSI) is the reorganization of framework-initiated devices with various systems for thinking entrances, which was formerly known as Small-Scale Integration (SSI). Additional redesigns prompted LSI, or frameworks with fewer than a thousand entries, for strategies of thought. Current technological advancement has far surpassed this imprinting, and today's semiconductor has a variety of doors and billions of individual transistors. Midway through 2008, billion-transistor processors were fiscally available. This became more prevalent as semiconductor production advanced from the then-current 65 NM outline. Current designs are not at all like conventional contraptions, as far-reaching procedure mechanization and electronic support combine to design transistors, empowering greater measures of the multifaceted nature in the subsequent method of calculating value. Certain massive pondering components, for example, the SRAM (Static Customary Access Memory) cell, are still hand-drawn to guarantee the best quality. With the introduction of NEMS advancement, VLSI development may move towards further radical reduction. The 26 transistors in the Hybrid Full Adder cell run a modified low-power XOR/XNOR circuit. By connecting two PMOS and two NMOS transistors in series, we can eliminate the worst-case delay issues that occur during transitions from 01 to 00 and 10 to 11. This circuit has a power use of 2.22% w [114].

2.2.510 Transistor Full Adder (10T)

In the 10T adder cell, pass transistor logic is used to perform XOR and XNOR of A and B, and an inverter is used to supplement the input signal [115-116]. This approach guarantees that there is a fair distribution of delays at the output of the XOR and XNOR gates and also makes their outputs quicker. As a result, there will be fewer false SUM and CARRY messages. When designs with fewer transistors and lower power usage are explored, maintaining full output voltage swing functioning becomes all the more difficult, if not impossible. If a driver is connected to the output, the output voltage swing will be the same as VDD. As illustrated in Figure 2.1, 10 T adders are represented by a specific circuit configuration.

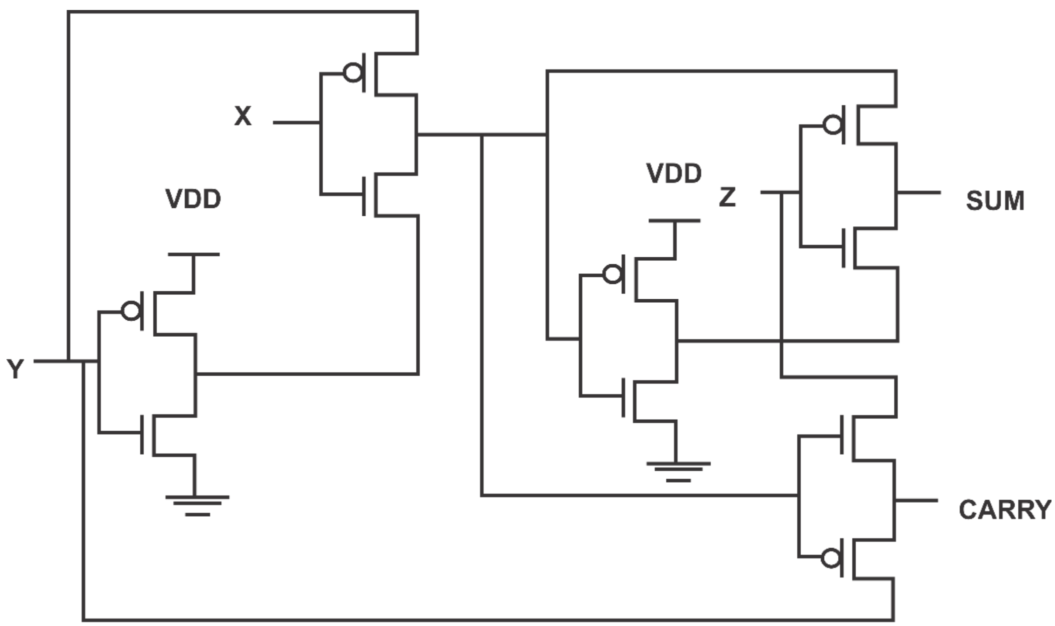


Figure 2.4 Schematic of 10T Full Adder 45nm Technology

The threshold voltage setback issue may impair the output voltage swing in pass transistor logic. While reducing the voltage swinghelps save energy, it may cause slower switching in cascaded operations like ripple carry adders. As the inverter is not used to load the XOR and XNOR gates, the capacitance at their outputs is likewise lowered. Drivers may be utilized to mitigate signal deterioration at the SUM and Carry if it is very severe, for deep sub-micron circuits.After the circuit was simulated, its performance in terms of power, latency, and area could be seen clearly. With the support of the driver, outputs with uniform rise and fall timings may be produced. As a result, the system's speed, power consumption, and acceleration are enhanced.

2.2.6Complementary Pass-Transistor Logic

CPL's central tenet is that logic operations may be performed with a network of only NMOS pass transistors. Each factor is used in a complimentary manner and each input signal and its complement must be supplied. The circuit also generates a complementary output that may be fed into a future cascade of CPL. Using a different circuit called CPL may drastically reduce the complexity of complete CMOS pass gate logic. Complementary static CMOS outperforms complementary programmable logic (CPL) and other pass-transistor logic designs where low power is a priority, as shown by the reported research findings for all basic and complicated logic gates apart from the full-adder and under actual circuit circumstances. When comparing circuit speed and layout efficiency, CMOS also performs well. When it comes to submicron VLSI, where every bit count, the fact that it just requires a single rail for power and data is a game changer for conserving valuable routing resources. It facilitates effective power optimization of noncritical signal nets and complete circuit components, and is resilient to transistor shrinking and voltage scaling. In fact, circuit resilience is prominently escalating as a primary concern in deep-submicron VLSI. When it comes to submicron VLSI, where space is at a premium, the ability to save on routing resources is of paramount importance, and its single-rail characteristic is essential for performing only that. Since it can withstand changes in transistor size and supply voltage, it may be used for effective power optimization of both noncritical signal networks and complete circuit subsystems. As compared to other designs, this one makes more use of transistors. The reason for this is because producing complement signals requires seven inverters [117]. Nevertheless, the input complementary signals may be generated from the outputs of preceding stages when this adder is employed in designs like the multiplier. This decreases the total number of transistors. Additionally, this multiplier may be driven effectively even without inverters. The pull-up functionality of PMOS transistors is to blame for this effect. Similarly, the output inverters used to generate SUM and CARRY may be employed in different stages of complicated designs like the multiplier, resulting in gains, both in terms of speed and size. CPL uses less power than conventional static CMOS circuits because the output voltage swing is less as a result of one Vt loss in the output. This circuit has a 2.5w power requirement[118].

2.2.7Transistor Full Adder

The 14-transistor (14T) adder is fast and uses much less power (on the order of microwatts) than its 10-transistor counterpart. As compared to other kinds of transistor adders, the 14T adder significantly improves upon the threshold loss issue. It is evident that the future applications of the digital FIR filter and its design will make use of this kind of low power, high speed adder cell. Yet, with the development in popularity of mobile devices like smartphones, PDAs, and laptop computers, there has been a corresponding increase in the need for VLSI circuits that are both small in size and low in power consumption. [119] advocated an FA based on 14 transistors and 3 capacitors, all built using carbon nanotube field effect transistor technology. Only 14 MOSFETs are required to create a full adder circuit with full voltage-swing at all circuit nodes. [120] provided an explanation of how a generic full adder circuit may be built using pass transistors and the exclusive OR and NOR circuits. We present a CMOS XOR circuit with six transistors that creates an XNOR output, replacing the standard full adder. Seven other schemes, such as the Hybrid scheme and three Full Adder schemes that are not grounded on the outcomes of previous majorities, are employed in addition to the new design. The simulation results [121] show that there are benefits in waiting. A novel low-power adder cell is made by lowering the number of MOS transistors, which makes it significantly quicker and consumes much less power than the static energy recovery full adder. The result of this study is a cutting-edge l-bit complete adder cell implemented in 14T CMOS.

This 1 bit hybrid complete adder was designed by M. Kaur et al. [122] and realized in 180 nm technology using CMOS and pass transistor logic. The new design reduces the static power consumption to 477.3pw and the average power consumption to 3.617w for a 1.8-volt supply compared to the prior design, which included components like CPTL and TGA (Transmission Function Adder). The suggested design is an advancement over the existing one, both in terms of efficiency and organization. Future complete adders have a critical route delay of 18.745ns and an average power consumption of 3.61w. The proposed design has an advantage that it requires fewer metal wires than the current standard. This circuit is in its regular operating range from 1.25V to 1.8V.

The energy consumption of three different adders and the total number of transistors were recommended to be made available by M. Jayaprakash et al. [123]. The hybrid adder offers superior power performance compared to both multiplexer-based adders and traditional CMOS 28-transistor adders. It is shown that the power consumption of the circuit may be reduced by using logic rearrangement methods when the MOSIS 90 nm technology is used for the overall architecture's design. The planned method is expected to provide low power consumption and fast speed compared to existing full adder designs.

Performance of a one-bit full adder was provided by P. Kumar et al. [124] based on an analysis of its internal logic design. This cadence tool equates the new design to the old design using 90nm and 55 nm technologies. As compared with other full adder cells, the suggested design offers highest performance and best PDP. It has been determined that this new design works well at low voltages and produces satisfactory results. This demonstrates that the suggested architecture has potential as a viable option for nanoscale or future-scaled technologies. The suggested design is validated using simulation results to ensure it will function properly under the anticipated fluctuations in supply voltages and temperature.

K. Katiyar et al. [125] demonstrated a practical approach to increase the GDI gates' output swing. In order to do so, new designs have been introduced, employing single pass transistors for the most fundamental digital gates (AND, OR, XOR). The propagation latency of the proposed circuit's OR gate is smaller than CMOS, but it is more in AND and XOR, when compared to other static CMOS approaches such as 28T, SERF,8T, and 6T. As a result, it was found that the OR gate had the lowest power delay product value.

2.2.8Gate Diffusion Input Logic (GDI)

Lowest power design approach is a GDI cell, which may be found in the literature [126]. This circuit just requires two transistors but can perform a broad range of logic operations. The GDI procedure, as seen in Figure 2.2, makes use of a basic cell. Notably, a GDI cell's PMOS source is not linked to VDD, and its NMOS source is not connected to GND. This function provides the GDI cell with two additional input pins, expanding the design's capabilities beyond those of a standard CMOS cell. Its main drawback, the need for a specialized CMOS process, is a direct result of this property. Specifically, the GDI technique can't be implemented using the cheaper ordinary p-well CMOS process but rather necessitates the costlier twin-well CMOS or silicon on insulator (SOI) technology. This is comparatively simpler than NAND and NOR, needing just two transistors to perform the same function. In contrast to NAND and NOR gates, these operations may be employed to efficiently synthesis new operations [148]. In order to repair the voltage, drop at the outputs and restore the logic levels, a buffer circuit is added (SUM & CARRY) [127].

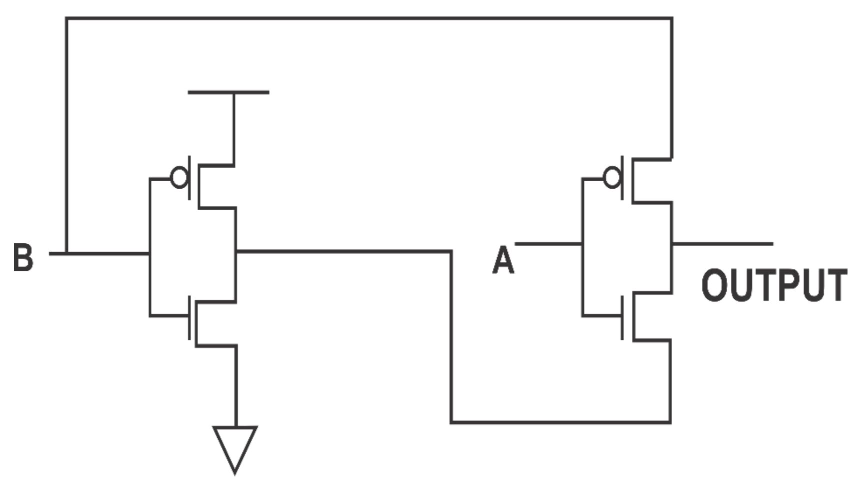


Figure 2.5 XOR Gate Using GDI

G is connected to the common gate input of the nMOS and pMOS, P is connected to the source/drain of the pMOS, and N is connected to the source/drain of the nMOS in the GDI cell. Unlike a CMOS inverter, an nMOS or a pMOS may be arbitrarily biased since their bulks are linked to N or P. Although the majority of functions (6-12 transistors) in CMOS and typical PTL implementations are challenging, the same functions are greatly simplified by the GDI design approach.

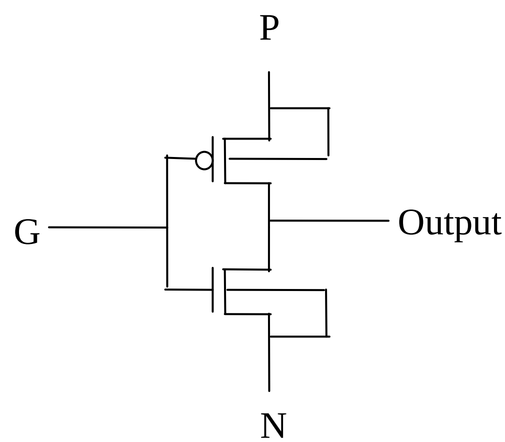


Figure 2.6 Schematic of Gate Diffusion Input Logic

More versatile than a standard CMOS design, the GDI cell now has two more input pins, thanks to this addition. Its main drawback, the need for a specialized CMOS process, is a direct result of this property. Specifically, the GDI technique can't be implemented using the cheaper ordinary p-well CMOS process but rather necessitates the costlier twin-well CMOS or Silicon on Insulator (SOI) technology. Just 4 transistors are required to implement the GDI XOR gate. By comparing GDI XOR to its CMOS equivalent, it becomes clear that the GDI XOR gate uses less transistors.

New FA topology implementations in GDI, TG, and C-CMOS are compared and contrasted by M. Hasan et al. in [128-135]. To further demonstrate the performance improvements brought about by the proposed FA, this research provides a comparison between the proposed design and 13 existing state-of-the-art FAs. Additionally, a 4-bit, 8-bit, 16-bit, and 32-bit adders have been built using a cascade of the proposed and existing FAs, assessing the performance and feasibility of the FAs in large-scale situations. The recommended design performed quite well in both single-cell and cascaded tests.

With 65 nm technology at 1 GHz with 1.2 V supply voltage, the intended FA showed 4.48 W average power and 70.29 ps delay. A PDP of 314.9 pJ was measured. As an added bonus, the suggested method for FA design employs C-CMOS logic at the output terminals, thereby rectifying the voltage degradation inherent in the GDI method and the lack of drivability in the TG-based design. The simulation results produced in this study provide significant support to the disagreement that the FA design provided here is suitable for use in wide adder design in state-of-the-art VLSI systems.

Using a mixed logic approach, J. Kandpal et al. [136] researched and developed a high-performance complete adder. Here the output from a simulation runs in the cadence programmed using 90 nm CMOS technology and 1.2V. The suggested layout works well regardless of the supply voltage and with a variety of loads. The findings reveal a 53% reduction in latency and 57% reduction in PDP compared to the optimum alternative. In addition to its reliability with the suggested supply voltage, the proposed circuit is also useful with other voltages. By considering both delay and power delay product, the suggested circuit provides the optimal solution (PDP). It's possible that high-performance circuits might benefit from a hybrid design approach.

The effects of the power delay product, driving capability, power consumption, and speed on the performance of the XOR-XNOR circuit have been investigated and compared across a number of different one-bit hybrid adder topologies by J. Kandpal et al. [137]. It is possible to develop low-power circuits using fewer transistors through gate diffusion input and redesigning GDI cells. Two new NOR gates based on the MGDI cell were used to produce this FA. Next, using either the aforementioned adder or MGDI XOR-XNOR gates, we offer two low-power and energy-efficient complete adders that meet full-swing property. To discover how effective our freshly built full adders are, we compare them to certain already-existing full adders. Post-layout simulations utilizing Cadence Virtuoso tools in TSMC 0.18 m CMOS process technology show that the power consumption of the features may be decreased by approximately 24%-56% (22%-56%), while the power-delay product (PDP) can be lowered by around 36%-66% (28%-62%).

S. Hussain et al. [138] developed a full adder (FA) cell with 18 transistors using the full swing hybrid logic architecture. After the first stage, which employs the XOR-XNOR module, the SUM and CARRY outputs are generated by pass transistors and inverters, respectively. The performance of the intended FA cell was compared to that of eight existing FAs throughout a supply voltage range of 0.4 V to 1.0 V using an HSPICE simulator at the 16 nm manufacturing node. When compared to a regular 0.8 V CMOS Mirror adder, the proposed adder shows significant improvements in propagation latency (34.77%), average power (48.8%), and power delay product (66.58%).

M.Hasan et al. proposed a full-swing Full Adder (FA) that makes use of the XOR-XNOR module. Eleven current FAs have been utilized to test the effectiveness of the new design. The proposed FA has a smaller Silicon area (19.35%), average power consumption (33.59%), propagation delay (36.15%), area delay product (ADP) (56.22%), and power delay product (57.59%) than a conventional CMOS FA. It was shown that FA's 32-bit simulations generated superior performance. The proposed hybrid FA has the potential to replace conventional FAs due to its superior properties.

2.2.9Transistor Full Adder Cell

A full adder is required in the design of any kind of processor, whether it a microprocessor, a DSP, or anything else. The rapid development of design approaches to substantially lower power consumption and this has been spurred by demands for the low power VLSI. The adder is on a crucial route that slows down most digital systems. The performance of the suggested 8T full adder cell was shown to be the best during comparison analysis. Of all full adders documented till date in the literature, the 8T full adder cell uses the least amount of silicon area on chip. The suggested complete adder cell has a tiny silicon area, which might be beneficial for implementing compact VLSI circuits on a limited amount of chip real estate. All current adders are outperformed by the proposed full adder cell in terms of threshold loss, latency, and power dissipation. This clearly indicates that the 8T full adder cell, proposed by us, significantly exceeds any prior adders.

S. Mishraet al. [139] examined and compared two high-performance full adder circuits. The proposed circuits' power consumption, delay, and Power Delay Product (PDP) were compared to those of current 10 transistor full adders using simulation in the Cadence VIRTUOSO environment in 0.18 m UMC CMOS technology.

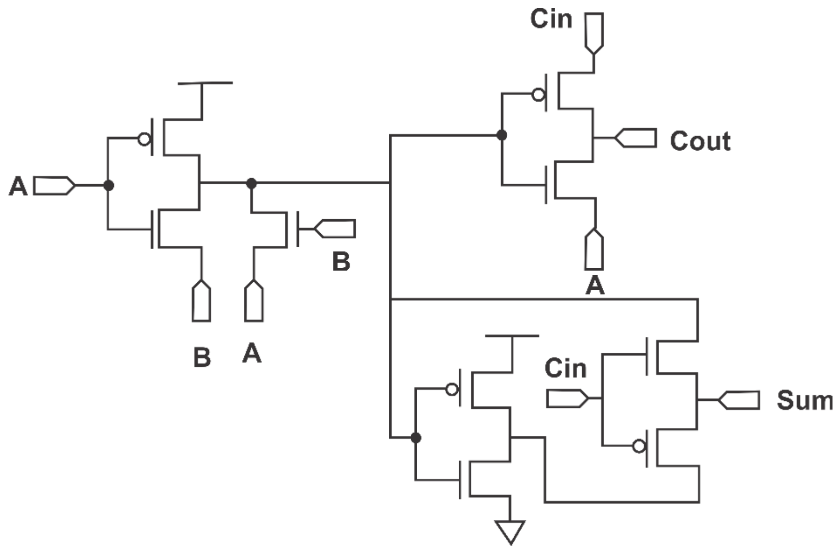


Figure 2.7 8T full adder cell suggested by S. Mishra et. al. [139]

Many researchers (including Deepa Sinha) came to this conclusion in 2011. When comparing an 8-transistor full adder cell to a 9-transistor full adder cell, it is distinctively seen that the 8-transistor full adder has significant issues, particularly at Cin=0 and also when the circuit works in sub-threshold areas. With just four input vectors, the logic level of the outputs is rather high. There is a significant drop in output voltage for the remaining input vectors, which may result in functional failure and higher power consumption that may be mitigated by the use of power reduction strategies. The silicon area and power-delay product have been significantly improved over previously suggested 4T and 6T XOR gates, thanks to this design. The suggested three-transistor XOR gate was used in the construction of an eight-transistor complete adder, and its performance was studied in 0.15m and 0.35m technologies.In the course of recent decades, CMOS innovation scaling has been an essential driver of the gadgets business and has given a way toward both denser and speedier mix. The transistors produced today are 20 times speedier and involve less than 1% of the territory in comparison to those assembled 20 years back.

The quantity of gadgets per chip and the framework execution have been enhancing exponentially after the recent two decades. As the channel length is diminished, the execution enhances, the power per exchanging occasion diminishes, and the thickness progresses. Yet, the power thickness, adds up to circuits per chip, and the aggregate chip control utilization has been expanding.

The requirement for more execution and joining has quickened the scaling patterns in practically every gadget parameter, like lithography, powerful channel length, entryway dielectric thickness, supply voltage, gadget spillage, and so forth.

Some of these parameters are moving towards key points of confinement, and other options to the current material. Probably, structures ought to be distinguished with a specific end goal to keep scaling. John Bardeen, Walter Brattain and William Shockley developed the fundamental transistor at Bell Laboratories in 1947. The primary coordinated circuit flip flounder was imagined by J Kilby in 1958 at Texas and in 1963, the main CMOS rationale door was portrayed by Frank Wanlass at Fairchild. Moore's law is known to be the headway of CMOS development. As indicated by this law that at regular intervals, the transistor check gets multiplied due to the consistent scaling down. Gordan Moore watched that for the most complex coordinated chip, the quantity of parts gets multiplied every year for the following 10 years.

2.3Leakage Power Reduction Techniques

2.3.1Power Gating Technique

The suggested unique approach, with better staggered phase damping, may reduce leakage significantly with little effect on performance, in addition to reducing the peak of ground bounce noise. Both the "sleep" transistor and the extra cycles spent waiting for functional units to wake up may have an effect on performance when power gating is used. There may be a little reduction in cycle time due to the inclusion of the "sleep" transistor. A little increase in VDD to compensate for the voltage drop across the "sleep" transistor, will prevent this from happening. In order to implement power gating, a "sleep" transistor must be included in the header (or footer) of each circuit that can be switched off, allowing the supply voltage to be set to ground (or VDD level for footer) during idle periods. In addition, control logic is wanted for power gating in order to foresee when it would be most beneficial to gate the circuit's power supply. The sub-threshold leakage current may be greatly reduced by turning off the sleep transistor while the low-Vth logic block is idle. Fig. 2.4. presents a power-gating sleep transistor. Using data from the decoding stage or issue queue to proactively wake up required units may significantly reduce the effect from the second source on performance. The disadvantages of an inadequately sized sleep transistor may be mitigated by a capacitance, but it would have to be enormous. As a low pass filter, the RC circuit ensures that the virtual ground voltage never exceeds a small percentage of its maximum dc value.

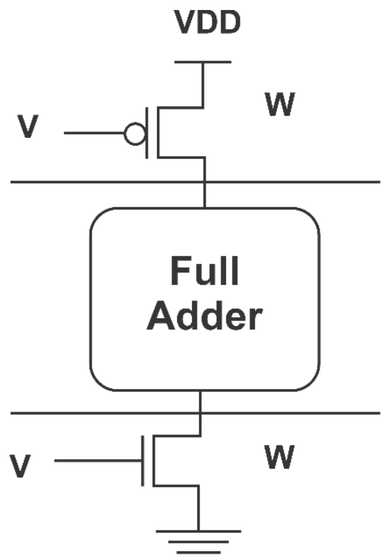


Figure 2.8 Fine-Grained Power Gating(term we've coined for this strategy)

There are two major leakage mechanisms in scaled devices: sub threshold leakage and gate leakage [140-143].

2.3.2Multi Threshold CMOS (MTCMOS) Technique

Most circuits nowadays employ a technology called Multi-Threshold Voltage Complementary Metal-Oxide-Semiconductor (MTCMOS) to reduce leakage currents below the threshold. In this research, we suggest using dynamic forward body bias to reduce ground bouncing noise in sequential MTCMOS circuits, without impacting their capacity to store information. The half-micron technology ushered in a period of linear scaling between supply voltage and feature size. The speed of the circuit, however, is affected by the scale of the power supply [144]. Disabling a VLSI circuit's power supply is the most direct technique to reduce the leaky power dissipation it generates while in the STANDBY mode. In order to achieve both low leakage and great performance, Multi-Threshold Complementary Metal-Oxide-Semiconductor (MTCMOS) technology uses high-speed, low-Vt transistors for logic cells and low-leakage, high-Vt devices as sleep transistors. In order to decrease leakage while the system is sleeping, sleep transistors temporarily cut power to logic cells. In MTCMOS, high-speed low-voltage-to-temperature (LVT) transistors are used for logic cells, while low-leakage high-voltage-to-temperature (HVT) devices are used for sleep. In order to reduce leakage while the device is dormant, sleep transistors isolate logic cells from power and ground. Wake up latency and power plane integrity are major concerns in this technique, also known as power gating. Figure 2.5 is a schematic depicting the MTCMOS power gating technology.

Due to silicon breakdown mechanisms including electro migration, significant power dissipation severely reduces the chip's dependability. In [145], a method for reducing leakage power consumption during operation via gate-length biasing was disclosed. In [146], we see the proposed method to reduce sub-threshold voltages and leakage currents in domino circuits using a single PMOS sleep transistor.

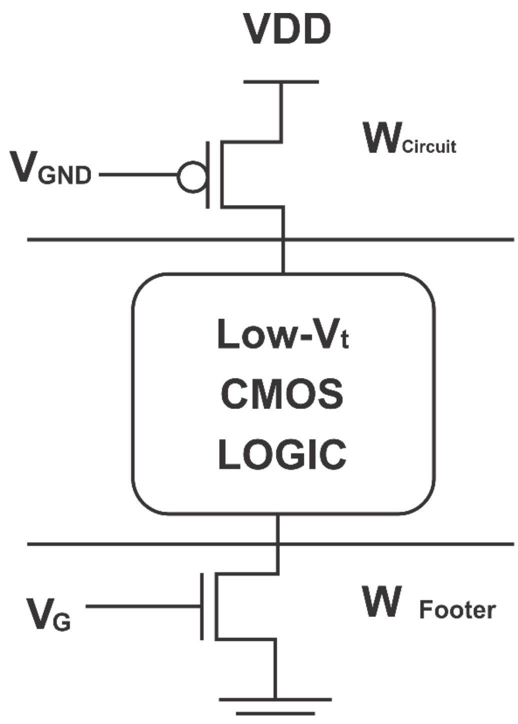


Figure 2.9 Multi Threshold CMOS (MTCMOS) Technique

In [147], a method is described for determining when and where to use leakage control transistors. For optimal leakage suppression, this strategy combines input vector control with sleep-transistor techniques.

2.3.3 Multi Threshold (MVT) Voltage Technique

Low Vt and High Vt cells are used in multi-threshold voltage methods including lower-threshold gates along the crucial route and higher-threshold gates elsewhere. This technique boosts functionality without necessitating more energy use. Nevertheless, the difficulty of manufacture increases when using Multi Vt cells, which is the technique's downside. As a result, it takes more time to get the design right. If the design isn't optimal, more Low Vt cells will be used, which might result in greater output. The challenges of optimizing both dynamic and static power consumption while working with numerous supply voltages and different threshold voltages have been highlighted by RuchirPuri et al. [148]. They found that Multi Vt optimization has several positive effects. Position-preserving transformation is the goal of multi-Vt optimization. Low Vt and high Vt cells have the same footprint and area as nominal as Vt cells. Because of this, low Vt cells may be readily substituted into time-critical pathways. Devices in a double Vth process may now be assigned using a novel approach provided by Frank Sill et al. [149]. They created Vth gates that work in tandem. They demonstrated a 25% decrease in leakage. They compiled low-, medium-, high-, and multi-volume tapestries. They tested each layout's LVT variant and compared the simulated results. When compared to the LVT approach, the mixed Vth methodology resulted in a 65% reduction in the average leakage power dissipation. MeetaSrivatsav et al. [150] looked at several methods for reducing leakage power and proposed the Multi Vt strategy. They have looked at both 90 nm and 130 nm technologies. They used a wide variety of target libraries in their design synthesis. Combinations of Low Vt cells alone, High Vt cells solely, High Vt cells with incremental compile using Low Vt library, nominal (or normal) Vt cells, and Multi Vt were used to accomplish multiple variant targeting (Hvt and Lvt concurrently). With just Low Vt, we were able to get a leakage power of 469 w. High Vt cells were used to decrease power usage, however deadlines were missed (-1.13 slack). For a low leakage power at standard Vt, 263 w was calculated. The most efficient methodwas targeting the Hvt library for synthesis and utilizing the Lvt library for incremental compilation.

The following are examples of Xiaodong Zhang's [151] use of Synopsys EDA tools throughout various low leakage synthesis processes.:

2.3.4 Variable Threshold CMOS (VTCMOS) Circuits

Using a low supply voltage and low threshold voltage without sacrificing speed performance is an effective way for lowering power consumption. On the other hand, as the threshold voltage of these devices rises, so does the subthreshold leakage and the standby power consumption.

Devices based on variable threshold complementary metal-oxide-semiconductor technology (VTCMOS) have been developed to deal with this problem. In the VTCMOS process, the threshold voltage of low-threshold devices is modified by modifying the substrate bias voltage [152].

While the VTCMOS approach is very efficient in lowering power consumption, it does have significant disadvantages associated with its use in practical devices. In order to adjust the substrate bias voltage in VTCMOS, either twin well or triple well technology is required. The IC substrate bias control circuitry has a very small footprint. The Relationship Between Voltage

Scaling and DVFS. The most efficient method to decrease dynamic power while incurring just a little performance hit is to lower the voltage of the power source. If the power is reduced while all other elements remain the same, the time it takes for a signal to travel will rise. However, a decline in threshold voltage boosts noise and increases leakage current. It enables for effective power optimization of noncritical signal nets and complete circuit components, and is resilient to transistor shrinking and voltage scaling [153]. In fact, circuit resilience is rising to prominence as a primary concern in deep-submicron VLSI. When it comes to submicron VLSI, where space is at a premium, the ability to save on routing resources is of paramount importance, and its single-rail characteristic is essential for doing just that. Since it can withstand changes in transistor size and supply voltage, it may be used for effective power optimization of both noncritical signal networks and complete circuit subsystems. As compared to other designs, this one makes more use of transistors. The reason for this is because producing complement signals requires seven inverters. Nevertheless, the input complementary signals may be generated from the outputs of preceding stages when this adder is employed in designs like the multiplier. This decreases the total number of transistors. Additionally, this multiplier may be driven effectively without inverters. The pull-up functionality of PMOS transistors is to blame for this effect. Similarly, the output inverters used to generate sum and carry may be employed in different stages of complicated designs like the multiplier, resulting in gains in both speed and size. CPL uses less power than conventional static CMOS circuits because the output voltage swing is less as a consequence of the one Vt loss in the output. This building has a 2.5w power requirement [154].

2.3.5 Dynamic Voltage and Frequency Scaling (DVFS)

If the supply voltage can be lowered by a factor of four, the decrease in power usage should be around the cube of that number. It's important to remember, though, that lowering the frequency slows down the process. While energy and voltage are often correlated, this is not always the case. The authors in [155] demonstrated that when Vdd is reduced below the sub threshold voltage level, the linear connection between energy and Vdd breaks down. The leakage current below the sub-threshold rises exponentially with increasing supply voltage. As the on current in sub threshold operation is a sub threshold current, the delay grows exponentially with increasing voltage. When the voltage drops extremely low, the dynamic power decreases by a factor of four. Yet, because leakage energy is proportional with circuit delay, it grows as supply voltage drops.

According to Bo Zhai et al. [156], dynamic voltage and frequency scaling is a viable low power strategy. Increases in power efficiency are not seen with wider voltage ranges, though. They demonstrated that "just in time completion" loses energy efficiency below the threshold supply voltage due to leakage energy. In addition, they demonstrated that lowering the minimum voltage to half of Vdd improves energy efficiency for most CPU architectures, whereas lowering the minimum voltage to sub-threshold operations is only helpful in a few cases. One key takeaway from their research is that DVFS is never energy efficient while operating at voltages below the threshold.

2.3.6 Power Gating

Requiring their former functionality once again, circuit blocks are switched back to "active mode" when this occurs. The optimal time and way for switching between these two modes maximizes power performance while minimizing performance effect. Thus, the purpose of power gating is to restrict power to non-essential blocks when the system is in a certain mode, thereby reducing leakage power consumption. When comparing power gating to clock gating, the former has a much greater impact on the overall structure of a device [157]. The time required to enter and leave power-gated states securely is increased. Where can I find instructions on how to disable the barriers? Software or hardware may be used to make this happen. The power-down processes may be pre-scheduled by the driver software. There are hardware timers that can be used. It is also possible to use a specialized controller for power management. Long-term leakage power reduction may be accomplished using the most basic kind of power gating: an externally switched power source. Internal power gating is ideal for briefly turning off the block.

2.4Leakage Reductions at Circuit Level

At the circuit level we can reduced leakage by some technique they self-reverse biasing, multiple threshold voltage, gated Vdd /Ground**.** In the course of recent decades, CMOS innovation scaling has been an essential driver of the gadgets business and has given a way toward both denser and speedier mix. The transistors produced today are 20 times speedier and involve less than 1% of the territory of those assembled 20 years back [158].

The quantity of gadgets per chip and the framework execution has been enhancing exponentially finished the most recent two decades. As the channel length is diminished, the execution enhances, the power per exchanging occasion diminishes, and the thickness progresses. Yet, the power thickness, add up to circuits per chip, and the aggregate chip control utilization has been expanding.

The requirement for more execution and joining has quickened the scaling patterns in practically every gadget parameter, for example, lithography, powerful channel length, entryway dielectric thickness, supply voltage, gadget spillage, and so forth.

Some of these parameters are moving toward key points of confinement, and other options to the current material and maybe structures ought to be distinguished with a specific end goal to keep scaling. John Bardeen, Walter Brattain and William Shockley developed the fundamental transistor at Bell Laboratories in 1947. The primary coordinated circuit flip flounder was imagined by J Kilby in 1958 at Texas and in 1963 the main CMOS rationale door was portrayed by Frank Wanlass at Fairchild [159].

2.4.1Self Reverse Biasing

Due to the body effect in CMOS transistors, a narrower depletion layer result in less threshold voltage (VT). To raise VT while using a CMOS transistor's reverse bias, and to reduce VT when using a COMS transistor's forward bias, just apply a bias in the opposite direction. Furthermore, in CMOS, the threshold voltage rises with increasing channel doping and falls with applied bias. As reverse biasing may reduce the current in the sub threshold zone, it is useful for reducing it. Provides a numerical value for the back gate bias parameter as a function of oxide capacitance and substrate doping. [160].

$$\gamma = \frac{t_{ox} \cdot \sqrt{2N_{SUB}\ q\epsilon_{Si}}}{\epsilon_{ox}} \qquad (2.1)$$

Where t_{ox} is gate oxide thickness, N_{SUB} is substrate doping level q is unity electron charge ϵ_{ox} is gate oxide permittivity and ϵ_{Si} is Silicon permittivity.

2.4.2Multiple Threshold Voltage

One simple strategy for lowering static power is to use a combination of high- and low-value transistors on the same chip, in addition to a sleep control mechanism. With higher transistors placed outside the critical route, static power may be decreased without sacrificing performance.

2.4.3Multiple Oxide CMOS

The threshold voltage of a transistor may be adjusted by varying the thickness of its gate oxide. You may make a dual by applying oxides of various thicknesses. The performance may be maintained despite the reduced oxide thickness (and thus, threshold voltage) in key pathways. In addition to decreasing sub-threshold leakage, increasing the oxide thickness also has a positive effect on lowering the dynamic power consumption by decreasing the gate capacitance. This is because the oxide tunneling current drops exponentially with increasing oxide thickness [161].

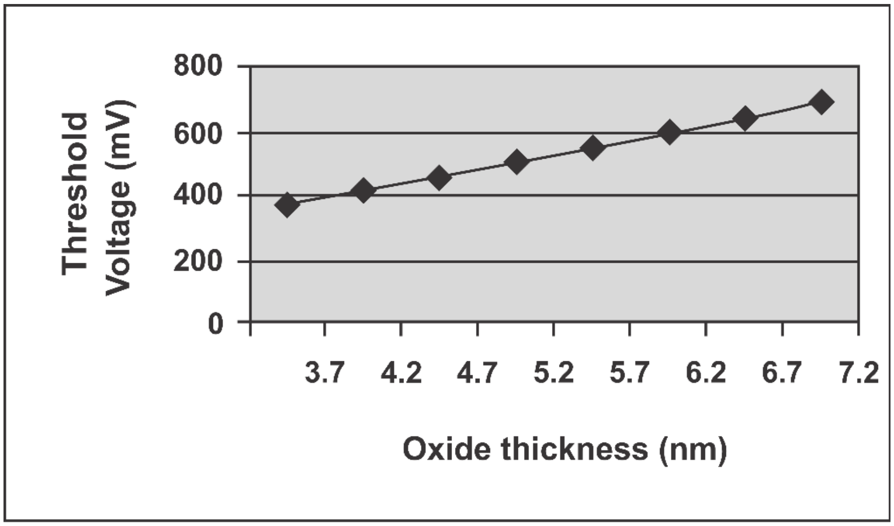


Figure2.10 V_{TH} at different oxide thicknesses

2.4.4Multiple V_{th} Design

By combining high- and low-threshold transistors on the same chip, multiple-threshold CMOS technologies are able to solve the leakage issue with great efficiency. When it comes to sub-threshold leakage current, high-threshold transistors may help to reduce it to some extent, but low-threshold transistors are preferred when excellent performance and stability are required. To get multiple threshold voltages, the following techniques may be used [162].

2.5Various Clock Gating Approaches

Clock gating is an important technique for lowering the power consumption of Boolean operations [163-168]. Domino logic circuits depend heavily on this technique to lessen their overall power consumption. In this article, we will discuss some of the most significant advancements in the field of clock gating research.

Nilanjan et al. [169] detail a fine-grained clock gating approach for dynamic logic systems. The proposed strategy enhanced switching efficiency in addition to reducing the time spent on computations. Domino/skewed logic forms are added to this Shannon-based approach. Energy was conserved by gating the clock in unused parts of the device's logic circuitry on a dynamic basis. The approach uses Shannon decomposition to establish that just a single cofactor is useful for doing computations for each given Boolean function. Several of the other co-factors' computations are recycled here. This might potentially save time by avoiding the need for further computations. It is ensured that all procedures take place when the circuit is live. The method is scaled up hierarchically such that it may handle several levels of development while still respecting the aforementioned time and space constraints. Due to the fact that the shared logic among the co-factors is not gated, the process ran indefinitely. In order to optimize the logic in gate cofactors, the governing variable is chosen. Since common logic is constantly active and hence cannot be gated by the clock, its usage was minimized.

Safeenet al. [170] provide a method for evaluating clock gating-compatible FPGA clock network designs. Time-based gating for a wide variety of device regions with disparate clock requirements is also a part of the strategy. We begin our research by presenting a number of novel clock gating topologies. They want to make some easy adjustments to the hardware to let an enable signal control some of the clock signals. In this work, we explore a range of fine-grained clock gating topologies that may be implemented inside clock distribution frameworks that are analogous to those found in consumer electronics. Similar alternatives exist for gates: The FG COLUMN gate type may be used to put gates where clock signals enter a sub-region and where horizontal half-spines cross with vertical quarter-spines. The opposite of a CG Region or CG column is also specified. The clock power term is the sum of the power used by all clock signals in the design and is determined at a given location. Due to the well-structured nature of the clock network, a clock routing could be quickly computed during installation, making it considerably easier to estimate clock capacitance and power.

Shen et al. [171] offer a new way to make gated clock trees that use less power. A concerted attempt was made to exploit the logical and physical information contained in shared registers.

This might affect how far other signals go and how long their wires are. For this reason, we used a net weighting method that took slack and switching activity into account. Next, an improved approach is utilized to insert gates and route clocks with zero skew at the same time, cutting down on unnecessary logic gates. It is not necessary to assume that each leaf (or register) has a gate in front of it for this technique to work.

The gating cover may be expanded by increasing the gating of devices, as described by Lin et al. [172]. This technique is an implementation of an interpolation-based satisfiability (SAT) based algorithm. SAT proofs are generated from clock gating signals. The problem with the clock gating is considered to be a sat issue. This research provides further detail on the CRAIG interpolation method [173] for creating fresh gating signals. There were three procedures involved in putting the clock gating technique into action. In the first stage, good candidates are chosen for gating. A logic simulation of the tested circuit is run to find and remove the invalid net-register combinations. The SAT engine then verifies that the remaining net-register combinations are satisfied. After that, we apply interpolation techniques to locate possible gate candidates of different types (I type, Gtype). Interpolants and any additional logic are constantly monitored to guarantee that timing requirements are satisfied. Finally, we estimate how much energy might be saved by using each of the gates that met our requirements. The overlap effect, which occurs when several signals gate the same set of registers [174], was included into the final power savings estimates.

In [175], Khaturia et al. provide a comprehensive overview of existing clock gating methods. The simulations of different approaches were also analyzed in the study. The clock signal and the control signal are sent into a two-input AND gate to provide the logic for clock gating. However, much like traditional gating, this kind of gating is vulnerable to risks and malfunctions, which may lead to unintended outcomes. To avoid issues with the enable signal, latch-based AND clock gating is employed. During timing verification, it is important to account for the delay introduced by the addition of logic, even while this does not reduce the effect of a defect. While latch-based NOR clock gating eliminates safety concerns, glitches continue to be a problem. Power consumption is higher because to the additional MUX per bit, even if the end circuit is reliable and synchronously constructed. Changing the time on the device you're attempting to control will not cause the controlled device to turn on [176]. Keeping the same gadgets on at all times helps save energy. Using this technique, we can eliminate both bugs and threats.

The proposed method of simultaneous gate/buffer insertion may reduce power consumption and enable the construction of a binary tree topology. An approach based on finding the nearest neighbors is used to construct the tree topology. As a result, both the wire length and the enable signals may be optimized. Node activity inside the network is monitored and updated in real-time. As a result of simplifying the code, the software now executes in a fraction of the time it used to [177]. The PSACTS synthesizer features more restrictive restrictions, such as a maximum clock slew that cannot be changed.

In order to minimize the disruption to the net list, Hurst et al. [178] provide a technique for the automatic synthesis of clock gating conditions. The new method considers both time and space. There are a number of benefits to employing this method, including the fact that it is scalable, that it makes use of simulation and satisfiability testing, and that it does not need symbolic representation. Each node on the hypergraph represented a single bit register or combinational logic node with a single output, which was used to simulate the circuit. To meet the multiple clock domain scenario, register groups are managed individually. The gating algorithm found the disjunction of literals that satisfied the gating conditions for each register. After that, in the "candidate identification" step, a set of possible literals is determined according to the gating signals for each register. Time, space, and material constraints are ultimately exploited to make them better [179]. The next step, candidate trimming, involves making sure each literal meets the gating requirement. The heuristic of greedy addition is employed to get to the bottom of things. A gated clock signal is produced as a consequence of using each candidate set to drive a clock gate [180-182].

CHAPTER 3

Hybrid Full Adder with Low Power Consumption: Analysis and Design in Static CMOS and Transmission Gates

3.1 Aim of the Chapter

The primary goal of any designer planning such a gadget is to make it both energy-efficient and highly effective. Any controller or processor relies heavily on its arithmetic logic unit. Adding is the most fundamental and obligatory activity for a gadget to function. Both static CMOS and transmission gate implementations of this entire adder circuit are available. The first of its kind, this Hybrid Full Adder was explicitly developed for use in low-power VLSI Circuits. The advantage of combining these two techniques is that it requires fewer transistors. This study chapter compares and contrasts the suggested complete adder with the two widely used TG and Standard CMOS adders with respect to power consumption, noise, and delay. In the cadence virtuoso, we model all three entire adder circuits using GPDK at 45nm.

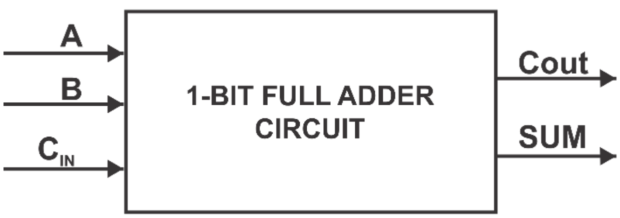
3.2Introduction

The field of electronics is sought to be the most versatile and evolving. Nowadays, the growth of silicon chips is taking place very rapidly. It is always a hurdle to design a portable system with high-performing capability. Moreover, that system has to be less power-consuming. Power utilization can be curtailed by scaling the input voltage. However, scaling can lead to propagation delay and deteriorate the driving capabilities. So, it is crucial to improve power delay characteristics while designing the Full Adder circuit [183]. The number of transistors in cascade, size of the transistor, number of inversion levels, and wiring capacitances of the intra-cell are the terms which determine the circuit delay.

Among all the ALUs, addition is the most used and is an essential operation of any controller or processor. So, for the sake of improving the system performance, it is indispensable to improve the performance strength of the adder. Choosing a suitable adder for any system is compulsory for its performance. In the process, many full adder circuits were implemented using different logic styles or a combination of different logic styles; each has its own advantages and disadvantages to make the full adder circuit. These logic styles are static and dynamic. Static comes up with high reliability and less power consumption, whereas dynamic adders have fewer area requirements. Some common logic styles are static CMOS, Transmission-Gate (TG), and

Pass-Transistor Logic (PTL)—conventional CMOS with pull-up and pull-down transistors. To improve the power, area, and delay, hybrid technologies are used by combining two or more standard logic styles [184].

The full adder performs addition, having three inputs and two outputs for SUM and CARRY. The block diagrams and the FA circuits' truth table are given below in Figures3.1(a) and (b).



(a)

INPUT			OUTPUT	
A	B	C_{IN}	SUM	C_{OUT}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(b)

Figure3.1(a) 1-bit Full Adder (b) Full Adder Truth Table

The equation for SUM and C_{OUT} is stated below.

$$SUM = A(XOR)B(XOR)C \tag{3.1}$$

$$C_{OUT} = C_{IN}(A + B) + AB \tag{3.2}$$

This chapterwill closely discuss performance and parameter analysis of the standard CMOS, Transmission Gate (TG) full adder with a hybrid full adder as suggested. The parameters of concern here are propagation delay, power dissipation and noise [185]. This chapter is furcated into sections where Section 2 includes power calculation and its consideration in the full adder circuit; Section 3 comprises the study of different logic styles used full adder; Section 4 includes a discussion of the proposed full adder; Section 5 includes results and Section 6 includes conclusions.

3.2.1Power Analysis

It is an unambiguous work to design a system and requires a lot of effort, such as fabrication, packing, and behavioral description of the IC. So, the consideration of power consumption is apparent from the beginning, and the aim is to design the circuit with low power consumption. The three sections of power-dissipation in a circuit are, Switching-Power, Short-Circuit Power and Static Power [186]. The first two are dynamic powers responsible for bulk dissipation from these three sections.

The given equation formulates the dynamic power,

$$P_{dynamic} = \Sigma\left(C_{i\,swing} \,.\, V_{i\,swing} \,.\, \alpha_i\right). f_{clk} \,.\, V_{dd} + \Sigma(K_i . \alpha_i)(V_{dd} - 2V_t)^3 . f_{clk} \quad (3.3)$$

And

$$K_i = \beta\tau/12 \quad (3.4)$$

Where,

$C_{i\,load}$ *is load capacitance at node i.*

$V_{i\,swing}$ *is voltage swing.*

α_i *is the switching activity factor.*

f_{clk} *is system clock frequency.*

V_{dd} *is the power supply voltage.*

V_t *is the transistor threshold voltage*

β *is the gain factor of the transistor*

τ *is the rise and fall time of the signal*

On reducing any of these components, the power consumption decreases. Improving the speed without compromising the power is of more significant concern [187]. Power calculation becomes easier when large circuits are fragmented into smaller modules by calculating the power of each module individually.

3.2.2 Study of Full Adder Design

3.2.2.1 Static CMOS Full adder

Static CMOS Full adder uses a total of 28 numbers of transistors with 14 PMOS and 14 NMOS transistors altogether. It is easy to implement this due to the symmetry of the schematic topology. The presence of 28 transistors, which is relatively high, led to more power and area consumption. A greater number of PMOS results in steep input capacitances, so steep delay and power, can be seen in this logic state full adder [188]. It has an edge of sturdiness against a scaling of voltage and sizing of transistors [189]. Its circuit is given in Fig. 3.2.

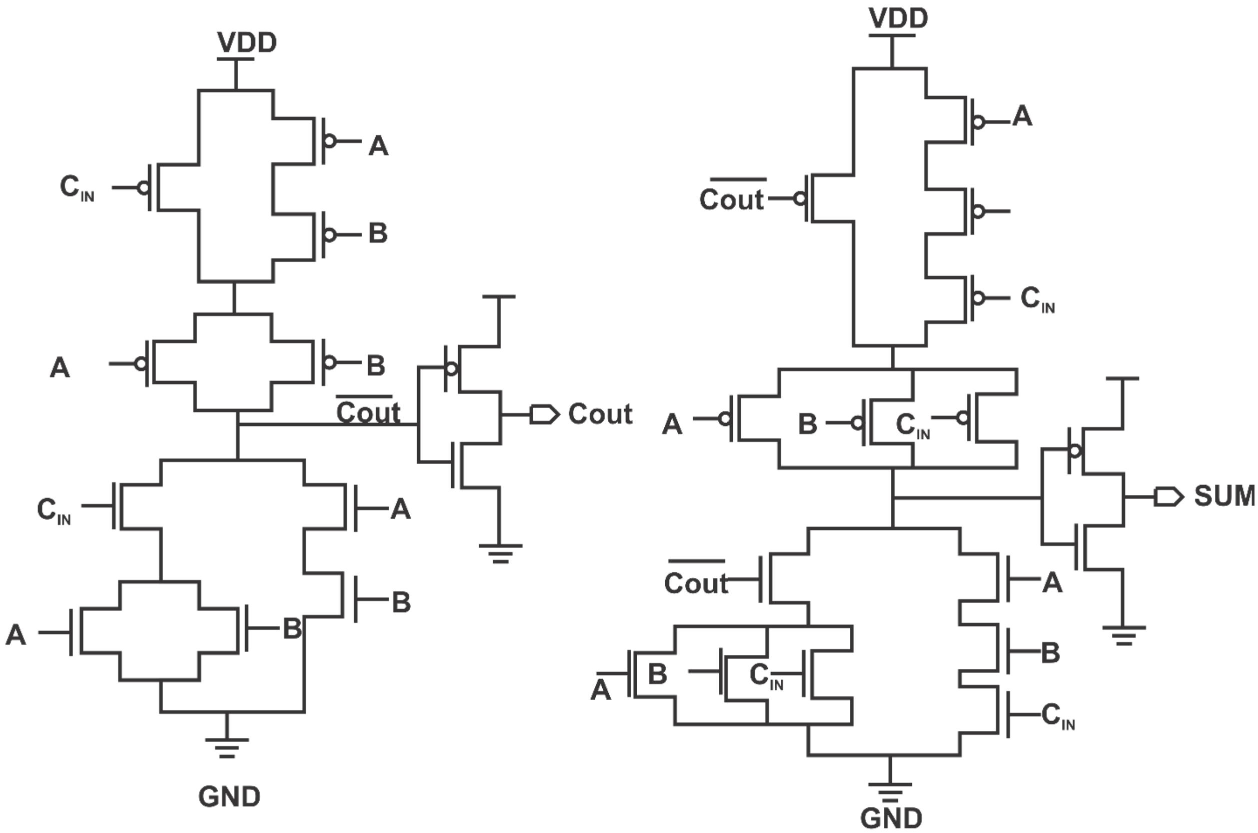


Figure3.2 Conventional CMOS Full Adder

3.2.3 Transmission-Gate Full Adder Circuit

Pass Logic is another name for this line of thinking. One pull-up and one pull-down transistor are connected in parallel in this design. The number of transistors may be reduced by using this logic. This logic acts as a bidirectional switch between A and B and is swayed by control signal C, as shown in Fig 3.3.

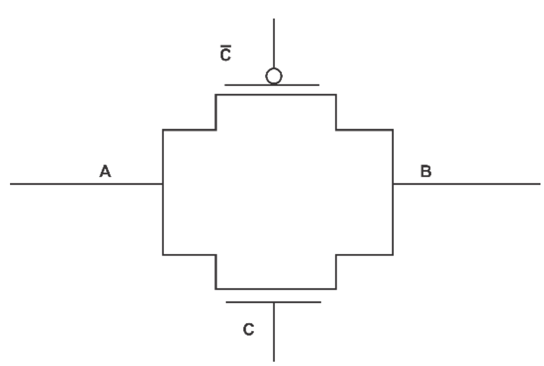


Figure. 3.3 Representation of Transmission Gate

It works under the high impedance state, i.e. if C is low, both the transistors are in the OFF state, and the path between A and B is an open circuit. If C is high, the path between A and B is short-circuit as both the transistors are in the ON state [190]. This can be termed as a special type of Pass Transistor Logic as it uses both the NMOS and PMOS. In PTL, either PMOS or NMOS can be used [191]. As it needstwice the transistor count than that of PTL, this became the main drawback of this circuit. By implementing this logic style, one can lower the power consumption and speed up the circuit execution because of the fewer transistors than the standard full adder [192]. With 20 transistors, this full adder has two XOR gates and a MUXto initiateSUM and CARRY, respectively.

In Fig. 3.4, this full adder can be seen.

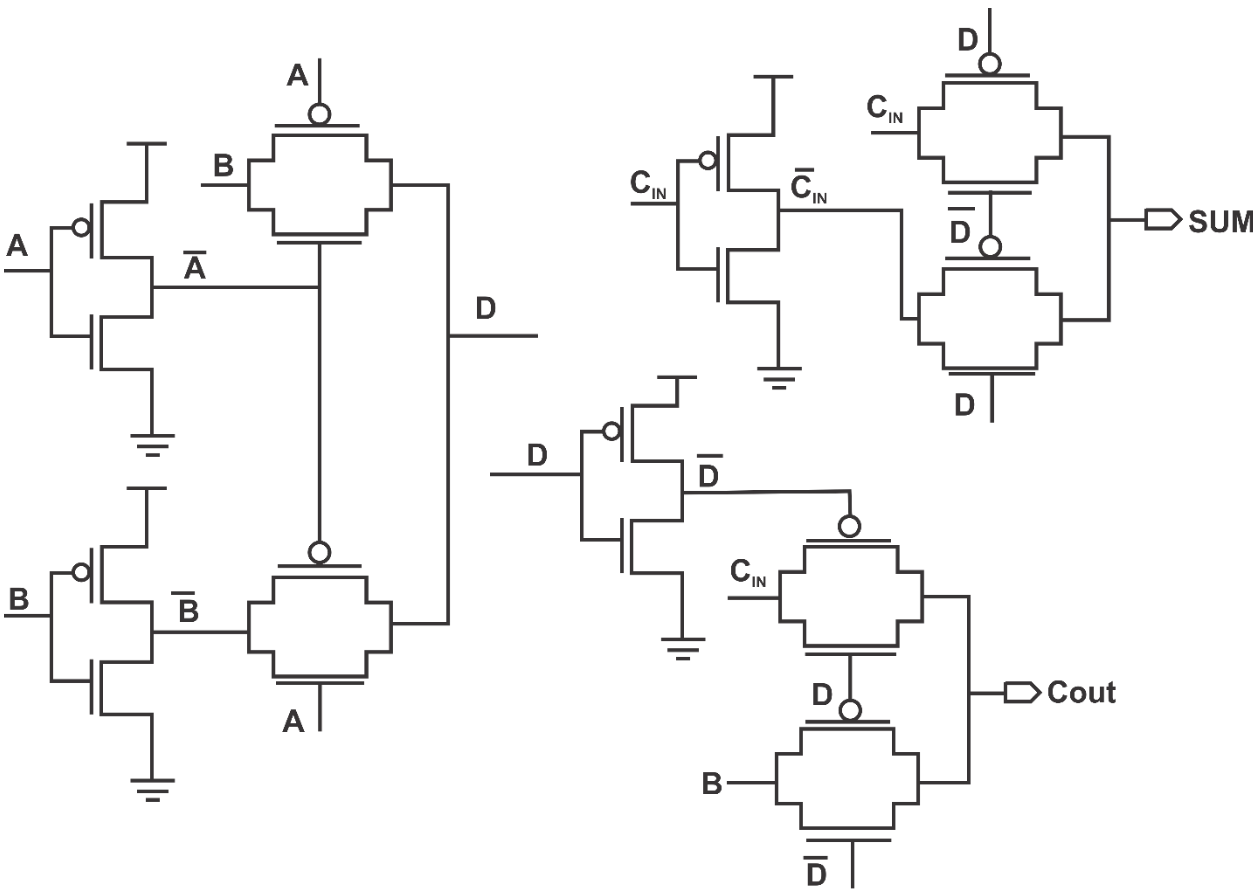


Figure. 3.4 Full Adder using Transmission Gate

3.2.4 HybridFull Adder Circuit

The suggested hybrid adder here has three blocks, each named Block1, Block2, and Block3, respectively. As shown in Fig. 3.5, the first two blocks, namely Block1 and Block 2, are XNOR gates, and the last block, Block 3, is used for C_{OUT} signal generation [193].

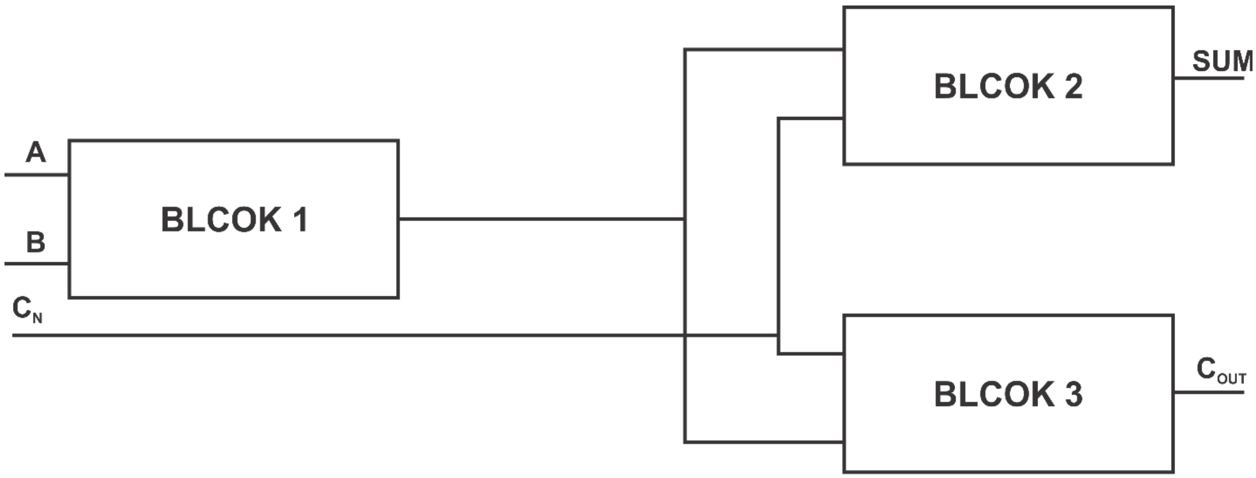


Figure. 3.5 Schematic Structure of Hybrid FA

3.3 Hybrid Full Adder Block Description

Here, the XNOR circuit has been amended to consume less power without any deterioration in voltage because it can consume most of the circuit's power. Though there are many existing XNOR gates present here in this hybrid adder, the XNOR gate is used to consist of the total number of transistors, and this XNOR topology provides high speed and low power to that of the existing XNOR gate[194]. Restoring the transistor makes full swing of the output signal and low power dissipation achievable. In Fig. 3.6(a), this XNOR circuit is shown. The transmission gate style is used to lower the transistor count for the carry generation. This logic style also led to the deduction of the propagation delay. Notably, the carry propagation path has seendeduction because the C_{IN} signal only passes via one transmission gate. The C_{OUT} generation circuit is given in Fig. 3.6(b).

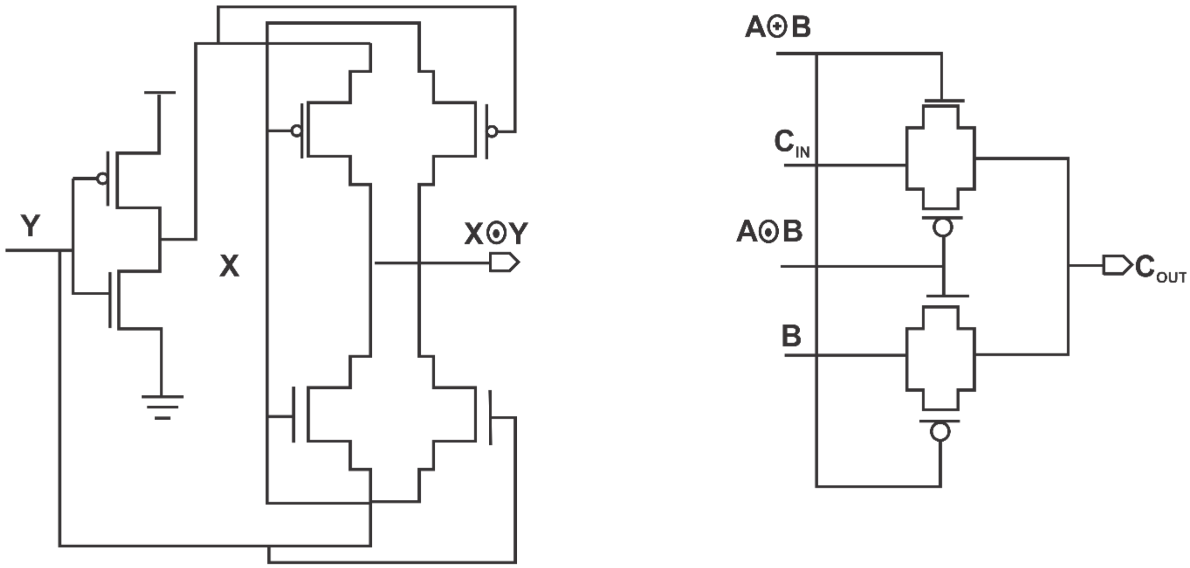


Figure 3.6 (a) XNOR block (b)CARRY generator block

3.4 Operation of Proposed Hybrid Adder

The SUM of the adder is calculated using the two XNOR gates, as was previously mentioned. As shown in Fig. 3.7, transistor P1 and N1 make an inverter to generate the B and helps to implement the controlled inverter having P2 and N2. The XNOR of A and B are getting as the output of this controlled inverter. This XNOR possesses a voltage deteriorating problem, which is further solved with the help of the transistors P3 and N3. Further, this XNOR output is taken as one of the inputs along with C_{IN} to generate the SUM signal. The second stage XNOR of the SUM signal.

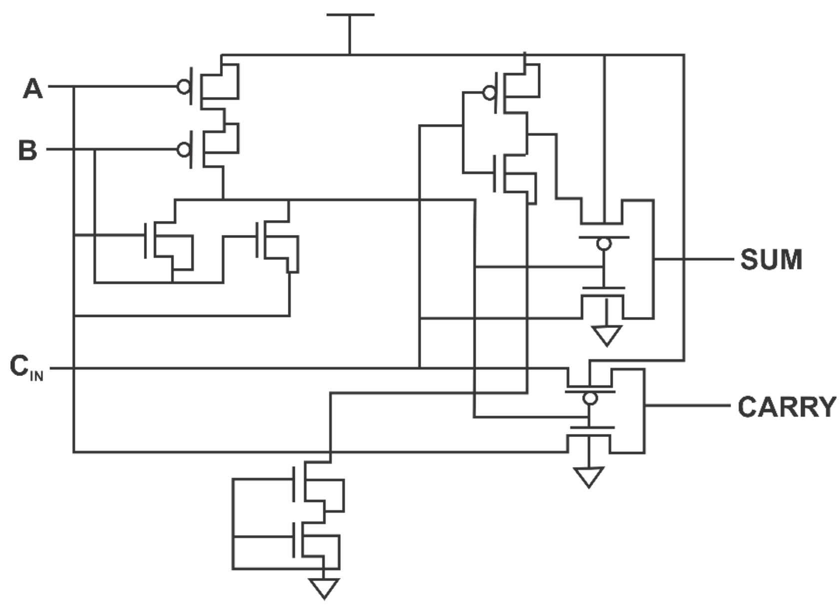


Figure. 3.7Proposed Hybrid Full Adder

The transmission gate (TG) technique is used for the carry generation, as stated earlier. This block is being implemented with the help of the transistor shown in the figure. It has four inputs present: input from the first TG is XOR of A and B, C_{IN} , XNOR of A and B, and B are the inputs given to the second TG. The XOR of A and B is used to check the parity betwixt inputs A and B, and if it is equal, then C_{OUT} is the same as that of B; otherwise, C_{IN} will show at the output of C_{OUT} [195].

This hybrid adder is realized with just 12 transistors as that of the above-discussed 20T TG adder. The suggested hybrid full adder is given in Fig. 3.7.

3.5 Average Power Dissipation

Talking about power dissipation for the above-discussed full adder circuit, the TG full adder offers a better power reduction than CMOS. The proposed hybrid full adder power dissipation is categorized into two parts: dynamic and static power dissipation [196]. It has high static power dissipation due to the charging-discharging of CLOAD in the transistor, and it can be formulated by the given equation as,

$$C_{LOAD} = C_{FIX} + C_{VAR}. \tag{3.5}$$

Where fixed capacitance, C_{FIX} can be reduced by proper design. Similarly, power dissipation can be appropriately controlled depending on the size of the transistor. One thing can be examined: most of the power dissipation comes from the SUM block. Overall, the average power consumption is less than that of the two discussed full adders.

3.5.1 Delay Propagation

A delay in the adder decides the execution or speed of the adder circuit. The CARRY signal propagation is mainly accountable for the speed response of the adder. So, to reduce this issue, this signal's path length must be minimized. The CARRY signal passes through only one transmission gate, while the CARRY path minimizes, leading to delay propagation reduction [197]. Overall, the propagation delay can be reduced by the power selection of transistor sizing and using an efficient TG.

Because of reduced delay and power, PDP will also improve compared to another mentioned full adder [198-199].

3.6 Result

The above-discussed two full adders based on static CMOS and TG-based full adders, respectively, are compared with the suggested hybrid FA. This comparison is mentioned in atabular form in Table 3.1. From the below table, it is evident that the suggestedFA is better in power consumption anddelay. The chopping in these two parameters means that the suggested adder has better PDP.

Table 3.1 Comparison between designed Full Adder Circuits

Parameter	Conventional Static-CMOS FA	Transmission-Gate FA	Proposed Hybrid FA	Percentage Improvement
Technology(nm)	45	45	45	
No. of Transistor	28	20	12	
Average Power(W)	5.590E-05	2.836E-05	2.465E-05	13%
Carry Noise(V^2)	1.373e-17	1.396e-17	1.598e-17	
Sum Noise(V^2)	1.870e-17	2.453e-17	1.747e-17	28%
Carry Delay(s)	83.26E-12	43.83E-12	36.11E-12	17%
Sum Delay(s)	93.30E-12	49.27E-12	35.41E-12	28%

3.7Summary of the Chapter

A full adder is anintegral part of any digitalcircuit. Nowadays, demand for portable devices leads us to long for better devices having good speed, reliability, and less power consumption. A low-power hybrid FA implemented using XNOR and TG logicis collated with the two logic styles, CMOS and TG based FA. The simulation is done on the Cadence Virtuoso with GPDK at 45nm. The 10T hybrid full adder performs better in power and delay. It can be implemented with a smaller number of transistors, and CMOS can be replaced with FinFET in future.

CHAPTER 4

A Comprehensive Analysis of High-Performance Power-Saving Techniques for a 10T Junction-Free Double-Gate Full Adder

4.1 Aim of the Chapter

Due to the proliferation of Nano-electronic circuit components, the reduction of power and leakage have become a significant challenge for modern VLSI circuit and system design. By modifying the threshold voltage, it is possible to reduce the supply voltage, resulting in silent power and precise control circuits. By integrating a dual logic strategy and a Negative Differential Forbearance (NDF) device into a greatly downsized Silicon on Insulator (SoI) Junction-Less Double Gate (JLDG)MOSFET architecture, this research presents anexceptional 10T Hybrid Full Adder (HFA) cell. The 10T JLDGHFA 10T Junction-Less Double Gate Hybrid Full Adder cell (10T JLDGHFA) was studied using the Ultra-Low Power Techniques (ULPT) of MTCMOS, Tri-Mode MTCMOS, and Self Controllable Voltage Level(SVL). Using standard circuit fabrication techniques, the leakage features of an idle circuit are guaranteed to reduce. In low-power simulations, the leakage power and current decreased by 24.09% and 24.11%, respectively. Tri Mode MTCMOS has 98.55 percent greater power density and current concentration than MTCMOS and SVL technologies, respectively. Cadence Virtuoso Tool has been used to realize the proposed circuit layouts and low-power methods.

4.2 Introduction

4.2.1 Overview of CMOS VLSI Design

Complementary Metal Oxide Silicon has been asignificant technology in the integrated circuit industry during the last several decades. Julius Lilienfeld developed the theoretical groundwork for the first field-effect transistor in 1925 [200], and in 1935, Oskar Heil patented the first metal-oxide semiconductor field-effect transistor. In 1947, John Bardeen, Walter Brattain, and William Shockley of Bell Laboratories invented the first commercially viable point contact transistor. The first flip flop using an integrated circuit was created by Jack Kilby of Texas Instruments in 1958. These circuits couldn't be built till Fairchild's Frank Wanlass introduced the first Complementary Metal Oxide Silicon (CMOS) logic gate in 1963. (NMOS and PMOS). When everything else failed. Because of their low power consumption, these circuits are poised to become the standard. The first MOS calculator wasn't displayed until 1965, and by 1967, a broad variety of

MOS devices with real-world applications in industry were on display. Time progressed and by 1970, nMOS-based procedures have become the norm. Concerns about power use first surfaced in the 1980s. The CMOS approach is widely used nowadays [201]. Thin-film transistor technology was made possible due to this concept. The inverter, the NOR gate, and the NAND gate were the first three logic circuits to be created. Integrated circuits may be created using CMOS (Complementary Metal-Oxide-Semiconductor) technology. There is a square relationship between the supply voltage, capacitive loading, and switching activity in CMOS circuits' power usage. All contemporary digital logic circuits, such as microprocessors, microcontrollers, static RAM, and more, utilize CMOS technology. Charge-coupled device (CMOS, image sensors, data converters, and highly integrated transceivers are all examples of analog circuits that rely on CMOS technology. As a result, CMOS has become the de facto standard for Very Large-Scale Integration (VLSI) devices, displacing bipolar technology. In order to create an integrated circuit (IC), Very Large-Scale Integration (VLSI) is used to combine many transistors onto a single chip. The advent of VLSI coincided with advances in semiconductor complexity and communication protocols.

Before the advent of VLSI advancement, most ICs had a well-guarded strategy of potential failure sites. VLSI allows IC facilitators to integrate them on a single chip. After focusing on the radar movement for a while, specialists eventually returned to the strong state device revolution. Transistors allowed the hardware industry to switch from vacuum tubes to solid-state devices [202]. The electrical designers of the 1950s, armed with the tiny transistor, could foresee the consequences of creating internally and externally increasingly complex circuits. Problems arose as a result of the disorganized construction of circuits. The circuit's compass was one potential problem. A complicated circuit, like a personal computer, needed speed to function. His first mixed circuit was set up in September 1958. The thought was substantial, despite the fact that the originally worked out circuit was harsh and had a few difficulties. There is no longer a need to manually assemble wires and splits. It also reduced the size of the circuits and automate the data collection infrastructure.

In the present day most of the technologists use VLSI technology. In early 60s,Small Scale Integration (SSI) system came into existence, which falls under the category of the low-density fabrication process. In SSI, the variety of transistors became restricted to 10 which gave upward push to Medium Scale Integration (MSI) inside the final 60s in which wide variety of transistors depend on a single chip quickened to 100 [203].

Other IC households like ECL are outlasted by means of Transistor-Transistor Logic (TTL) which gives excessive integration densities and has become the basis of first integrated circuit revolution. Early 70s are known for the development of around 1000 transistors on a single chip known as Large Scale Integration (LSI). In 1970, VLSI came into being when complicated semiconductor and communication technology changed into advanced VLSI termed as Very Large Scale Integration [204]. It is a framework in which assortment of transistors surpassing thousand are created on a single chip. A digital circuit contains of CPU, RAM, ROM and different glue good judgment. With use of VLSI, all these additives are introduced on single chip. Before VLSI appeared, the extent of a transistor was one of the real issues. With progressive technological innovation, the device dimensions are downsizing the complexity whereas performance evaluation of VLSI ICs is enhanced. With the first microprocessor, 4004 by using Intel in 1972, and 8080 in 1974, the second technology of Integrated Circuits revolution started taking shape. Companies like Cadence, Alliance Semiconductor, Texas Instruments, Synopsys, Infineon, Celox Networks, Cisco, National Semiconductors, Lucent, Micron Tech, ST Microelectronics, Philips, Qualcomm, Mentor Graphics, Intel, Analog Devices, Motorola and other industries are keen about a variety of fields in “VLSI” like Hardware Descriptive Language (HDL), Programmable Logic Devices (PLD), layout equipment, Embedded Systems and so on [205-210]. To accomplish superior and coordinated thickness in every innovation era, CMOS circuits have scaled downwards unyieldingly. With the patterns in the current Nano scale innovation for CMOS circuits, successful arrangements must be taken to diminish spillage control, since it is normal that in not so distant future spillage power will command the chips add up to control utilization. In every one of the levels of outline reflections, these arrangements can be connected with deliberation levels as: framework and structural level, circuit level, and gadget/process level. CMOS innovation is utilized for the usage of coordinated circuit. For advanced circuits, CMOS innovation is utilized for microcontrollers, microchips, SRAM and so on. For simple circuits, the CMOS innovation is utilized for picture sensors, handsets that are exceedingly incorporated, information converters and different sorts of correspondence. CMOS which stands for Complementary Metal Oxide Semiconductor is a mix of PMOS and CMOS. The CMOS gadget has fundamental attributes like high commotion invulnerability and low static power. One of the upsides of utilizing CMOS gadget is that they don't squander much warmth when contrasted with other rationale like Transistor-Transistor-rationale (TTL) or NMOS rationale in light of the fact that these rationales envelop some standing current, notwithstanding when they don't change the state. High thickness of the rationale work on a chip is additionally permitted by the CMOS gadget. In light of this reason, CMOS gadget generally used to actualize VLSI chips [211]

4.2.2 Evaluation of Hybrid Adder

Following developments included more transistors, and consequently, more individual termination points or frameworks were eventually joined. Initially, integrated circuits contained only a few components, perhaps up to ten diodes, transistors, resistors, and capacitors, making it possible to create multiple logic gates on a single device. Medium-Scale Integration (MSI) is the reorganization of framework-initiated devices with various systems for thinking entrances, which was formerly known as Small-Scale Integration (SSI). Additional redesigns prompted LSI, or frameworks with fewer than a thousand entries, for strategies of thought. Current technological advancement has far surpassed this imprinting, and today's semiconductor has a variety of doors and billions of individual transistors. Midway through 2008, billion-transistor processors will be fiscally available. This became more prevalent as semiconductor production advanced from the then-current 65 NM outline [212].

Current designs are not at all like conventional contraptions, as far-reaching procedure mechanization and electronic support combine to design transistors, empowering greater measures of the multifaceted nature in the subsequent method of calculating value. Certain massive pondering components, for example, the SRAM (static customary access memory) cell, are still hand-drawn to ensure the best quality. With the introduction of NEMS advancement, it is expected that VLSI development may move towards further radical reduction.

4.2.3 Need of Hybrid Adder

Carver Mead and Lynn Conway's planned to restrict the spectrum of connecting fabrics with a view towards increased microchip area,which was the impetus behind the VLSI architecture. This is accomplished by a time-consuming process of creating rectangular, large-scale squares that may be wired together through projection [213]. In this illustration, a snake's cellular architecture is divided into a few tiny pieces. Multilevel nesting may be the master of this sorting in sophisticated minds. While the fundamentals of organized VLSI architecture were understood by the mid-1980s, this understanding has faded as designers have learned to limit the closeness of arrangement and the power of controlling devices in order to exploit the increasing range made possible by Moore's Law. To echo Edsger Dijkstra's made-up programming framework of the system, settling to keep up a key partition from ramshackle spaghetti-created assignment, Reiner Hartenstein introduced the term "sorted out VLSI plan" (previously known as "formed LSI configuration") while presenting the apparatus depiction vernacular KARL in the mid '70s.

4.2.4 Challenges

As a result of progress in scaling, microchips are becoming more complex. Consequently, chip developers have encountered a few challenges that have caused them to rethink their strategy and begin planning for a post-silicon era.

As photolithography frameworks converge on the fundamental rules of optics, it becomes more difficult and error-prone to achieve high accuracy in doped focuses and scratched wires because of the organization of the processes involved. Before a chip can be guaranteed to have an orchestrated theme, creators now have to reiterate their efforts across many corners of the creation framework. As a result of complications with scale in lithography and engraving, requirements for layout have become stricter. When constructing distinctive circuits, coordinators should consider a multitude of these requirements. The advancement of nanoscale transistors, low-level voltages, and weak electrostatic control channels has led to an increase in the power available in digital integrated circuits. However, this progress is not without its notable hurdles. The delays seen in low-power and high-speed design networks due to power supply scaling are unfortunate. Low-power alternatives to standard complementary metal-oxide-semiconductor (CMOS) technology encompass several options such as multi-threshold CMOS (MTCMOS), Tri Mode MTCMOS, and SVL Technology. These alternatives are characterized by the inclusion of high-speed logic circuits [214]. The Tri Mode MTCOS utilizes low voltage and high threshold transistors in its designs, resulting in exceptional performance and reduced power consumption. By employing this technique, it is possible to diminish inactive approach currents to a level that is lower than the threshold, while ensuring that the circuit's functionality remains unaffected.

4.3 Full Adder 10T Hybrid

The Junction-Less Dual-Gate Metal Oxide Semiconductor Field-Effect Transistor links the drains of two transistors together and connects them in parallel to the supply. Based on the

MOSFET Gate bias, Junction-Less Dual-Gate devices fall into one of two categories [216]. Connecting the unit's front and back gates yields the earliest results and is represented by the three terminal devices in Figure.4.1. This setup is used as a multi-gate transistor replacement. The second kind requires separate control over the gate. The power and leakage consequences of HFA may be mitigated with JLDGMFET's [217] improved execution and operation.

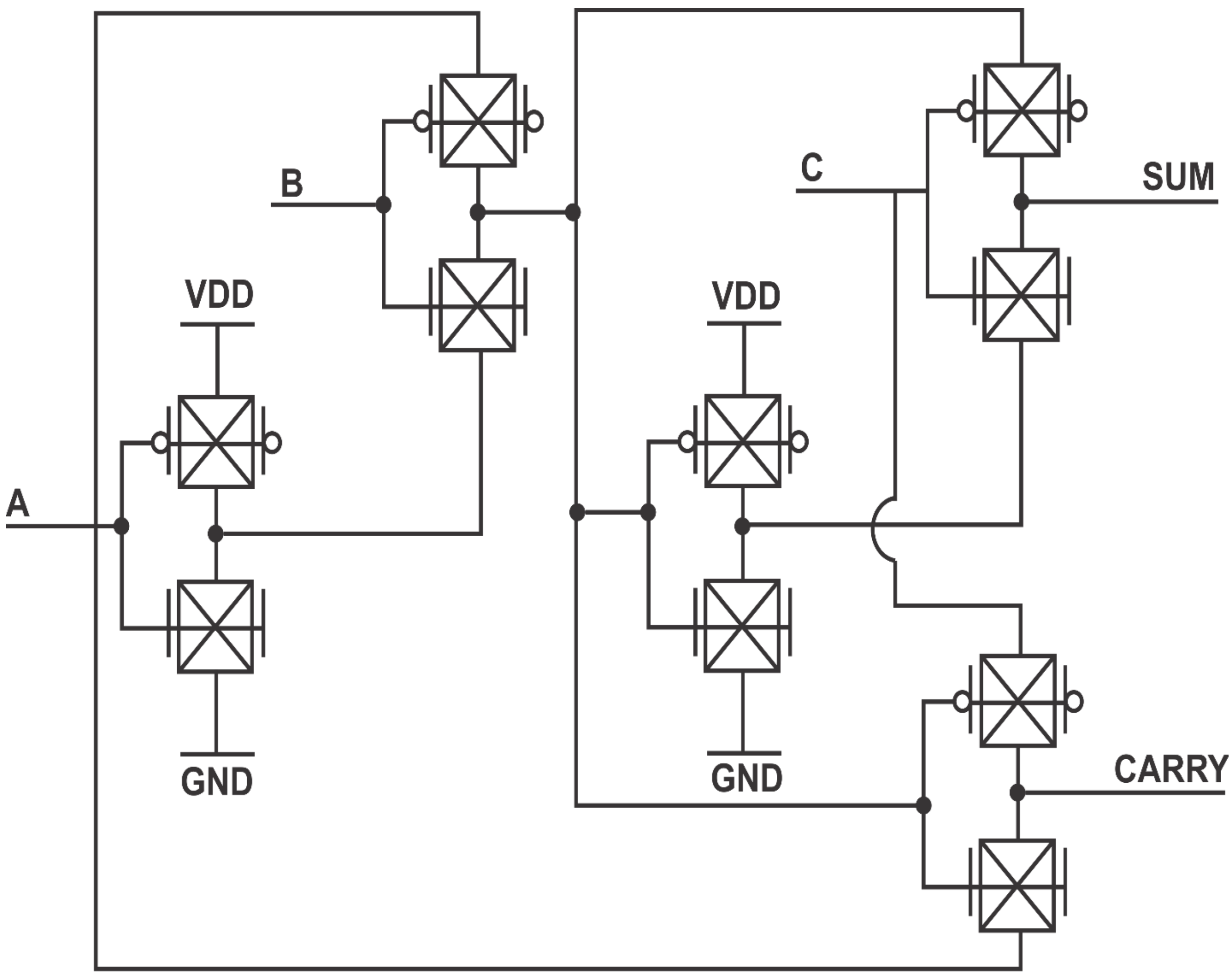


Figure 4.1 Junction Less Full Adder Double Gate Hybrid (10T)

where JLDG is derived as [217]:

$$V_{th_p} = V_{fb_p} + A_p V_T \ln\left(\frac{Q_{th_p} N_{si}}{n_i^2 t_{si}}\right) - B_p \left[V_{bi_p} - V_T \ln\left(\frac{Q_{th_p} N_{si}}{n_i^2 t_{si}}\right)\right]^{\frac{1}{2}} \left[V_{bi_p} + V_{ds} - V_T \ln\left(\frac{Q_{th_p} N_{si}}{n_i^2 t_{si}}\right)\right]^{\frac{1}{2}} - C_p \left(2V_{bi_p} + V_{ds}\right) \quad [4.1]$$

4.4 MTCMOS (Multi Threshold Complementary Metal-Oxide-Semiconductor)

Because of electro migration in the wire, it is crucial that the current through the transistors be stopped in active modeduring the fabrication of the MTCMOS circuit's physical structure.

Sincethe power is so unlimited, the channel width is also crucial. When deciding between global and local standby devices, a middle ground must be found. While the MTCMOS strategy does not present any challenge when used to combinational systems, but may be challenging when applied to sequential ones. Any data stored in the circuit will be erased if power is suddenly cut. With MTCMOS circuits, this is the prime issue. An elaborate synchronization mechanism or auxiliary circuit is used to solve this concern [218]. The circuit's performance suffers as a result of these extra elements. In addition to a significant loss of power, this also necessitates a large terminating surface.

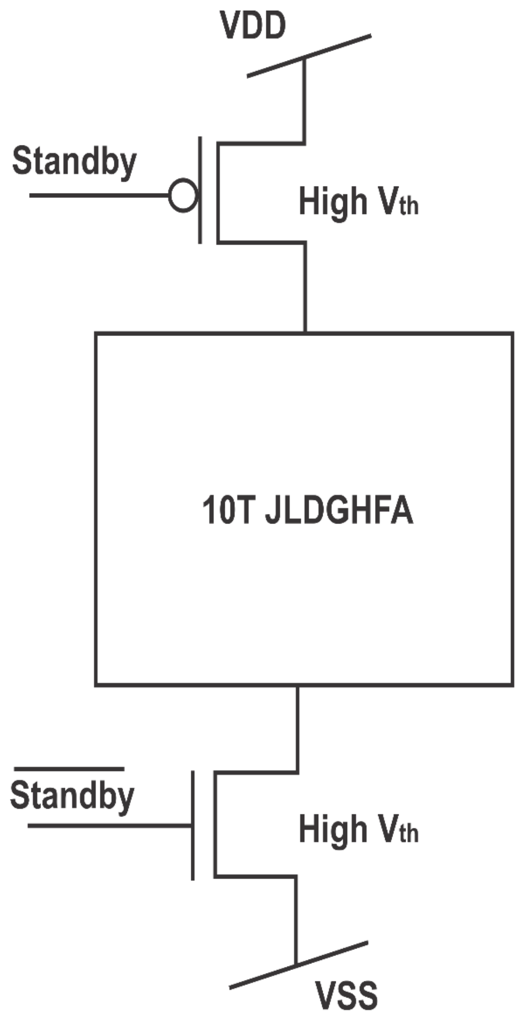


Figure 4.2Block Diagram of a 10T Hybrid Full Adder implemented in a Metal Oxide Semiconductor Metal Oxide Semiconductor Field Effect Transistor Array

When it comes to controlling leakage, MTCMOS Logic is unparalleled in its effectiveness. Power needs for low and high levels are met by MOS Vth and Vth transistors in multi-level logic. High-speed Vth transistors are employed in the logic circuit and power supply rails. Standby signals turn on these standby transistors, which are then utilized by high-level transistors to save energy when in standby mode. To boost active-mode performance, a logic circuit incorporates Vth transistors. The basic layout of an MTCMOS circuit is seen in Figure.4.2 [219]. Connecting the Vth Logic circuit's feed rails to the PMOS and NMOS transistors is a series of high-power transistors. High-level transistors activate a logic-on mode for real-world computation of high-level signals. To disrupt the logic circuit at the feed rails, three-volt transistors are held in a suspended state. There would be less leakage below the sub-limit when the device is in sleep mode. Low-power and high-speed applications both benefit from MTCMOS's efficient technology. In Figure.4.2, a 10T JLDGHFA is linked in series using MTCMOS approach with a combination of PU PMOS as Vdd and PD NMOS as Vss to analyze the circuit design's MTCMOS architecture [220].

$$I_{SUB} = I_0 e^{\frac{V_{gs} - V_{th} - \eta V_{ds} - \gamma V_{sb}}{\eta v\theta}} \left(1 - e^{-V_{ds}/v\theta}\right) \qquad [4.2]$$

4.5 Power Gating Technique

Scaling CMOS technology decreases supply and threshold voltages. In general, the sub threshold leakage current increases exponentially with decreasing threshold voltages [221]. Modern high performance ICs may waste over 40% of their active mode energy through leakage currentswhich will soon account for the vast majority of high performance ICs' overall energy usage as more transistors are integrated on-die. Power gating, commonly known as the Multi threshold Voltage CMOS (MTCMOS) method, is a well-liked approach of reducing leakage in electronic circuits.

The problem of power leakage is seen as particularly difficult in low power systems. By adding high-threshold sleep transistors to low-threshold circuits, the leakage may be reduced using the Multi-threshold CMOS (MTCMOS) method. By using high-speed, low-Vth transistors for logic cells and low-leakage, high-Vth devices as sleep transistors, Power Gating Method ensures low leakage and high performance operation. When the system is in sleep mode, leakage is minimized, thanks to sleep transistors that cut power to logic cells. The wake up latency and power plane integrity are major factors in this technique, also known as power gating. The term "power gating" refers to a method of controlling power to logic gates by cutting their supply and the ground line using high threshold voltage (high-Vth) sleep transistors. Figure 5.4 depicts a schematic of the power-gating approach. Low-threshold-voltage transistors are employed to implement the logic. In order to avoid leakage dissipation from occurring during standby (sleep) mode, high threshold voltage transistors are employed to electrically separate the low threshold voltage transistors from the power supply and the ground. [222].

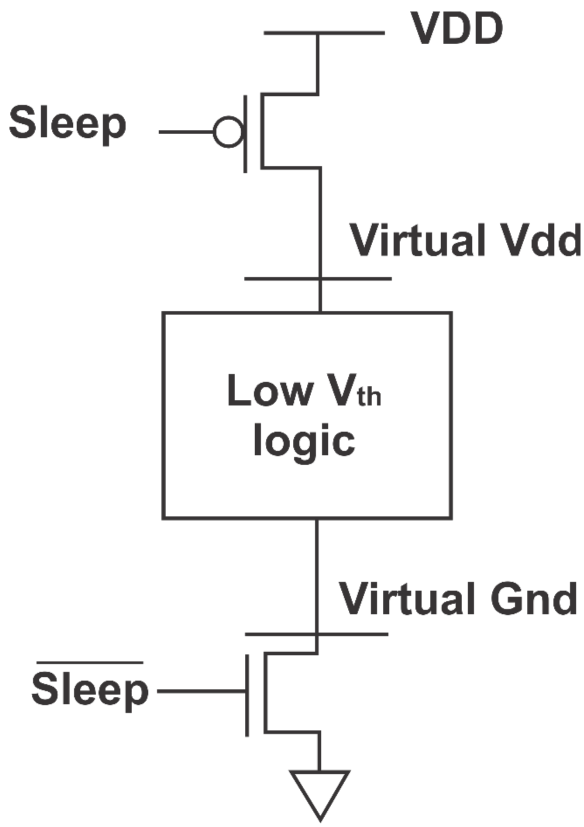


Figure 4.3PowerGating Technique

4.5.1 Stacking Power Gating Technique

The current tendency is to use transistors with a lower Vth, and nanoscale technology is being developed to accommodate this. The present, standard power gating design does not adequately reduce leakage current in standby mode, hence a new approach is required. This leakage may be greatly reduced by using a stacking structure and by incorporating a third operating mode into a power gate that is stacked

One: Operate in "active mode"

Two: with the "standby" setting

In standby mode, the leakage current is minimized by physically isolating the power supply rail from the ground rail and turning off the sleep transistors. Sleep transistors M1 and M2 are turned off by maintaining a logic zero value on the sleep signal SL.

To decrease ground bounce noise, we have used a sleep-to-active mode transition in which we first turn on transistor M1 and then turn on transistor M2 after a brief delay. Based on our design needs, we will choose values for the parameters T and capacitance C2. Figure 4.4 is a schematic representation of the stacked power gating method [223].

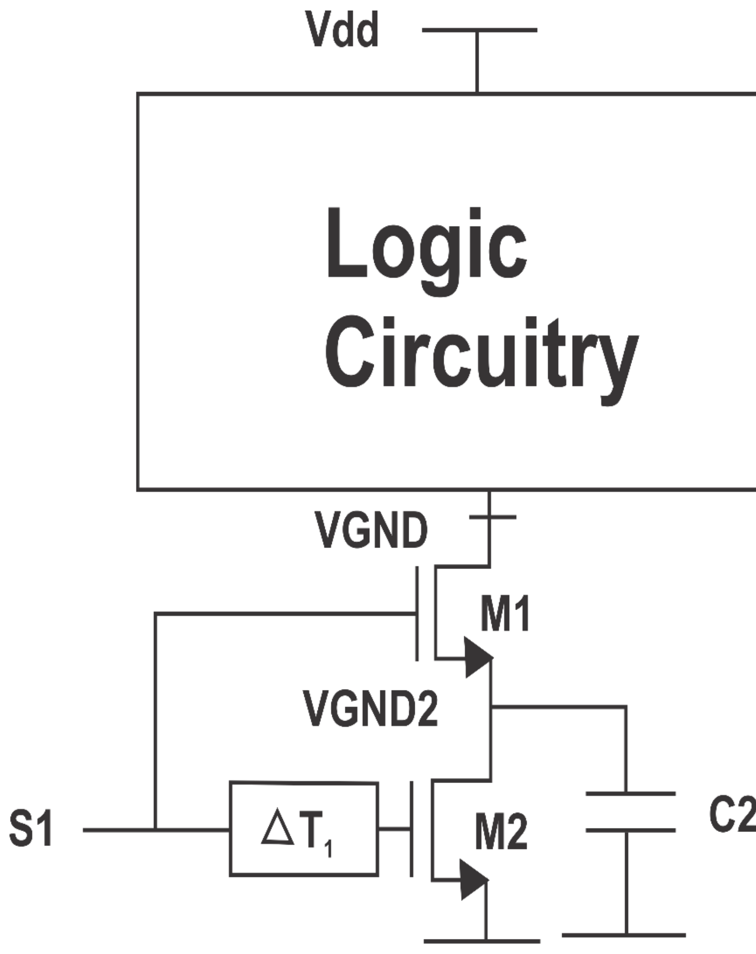


Figure 4.4Stacking Power Gating Technique

4.6Multiple Threshold Complementary Metal Oxide Semiconductor (TRI MODE MTCMOS)

Tri-mode MTCMOS refers to a low-noise MTCMOS technology that has three operational modes; SLEEP, PARK, and ACTIVE for a tri mode MTCMOS circuit. This is required in order to maintain the low drain state of the three-mode Metal-Oxide-Semiconductor-Metal-Oxide-Semiconductor-Oxide-Semiconductor (MTCMOS) circuit SLEEP setting.

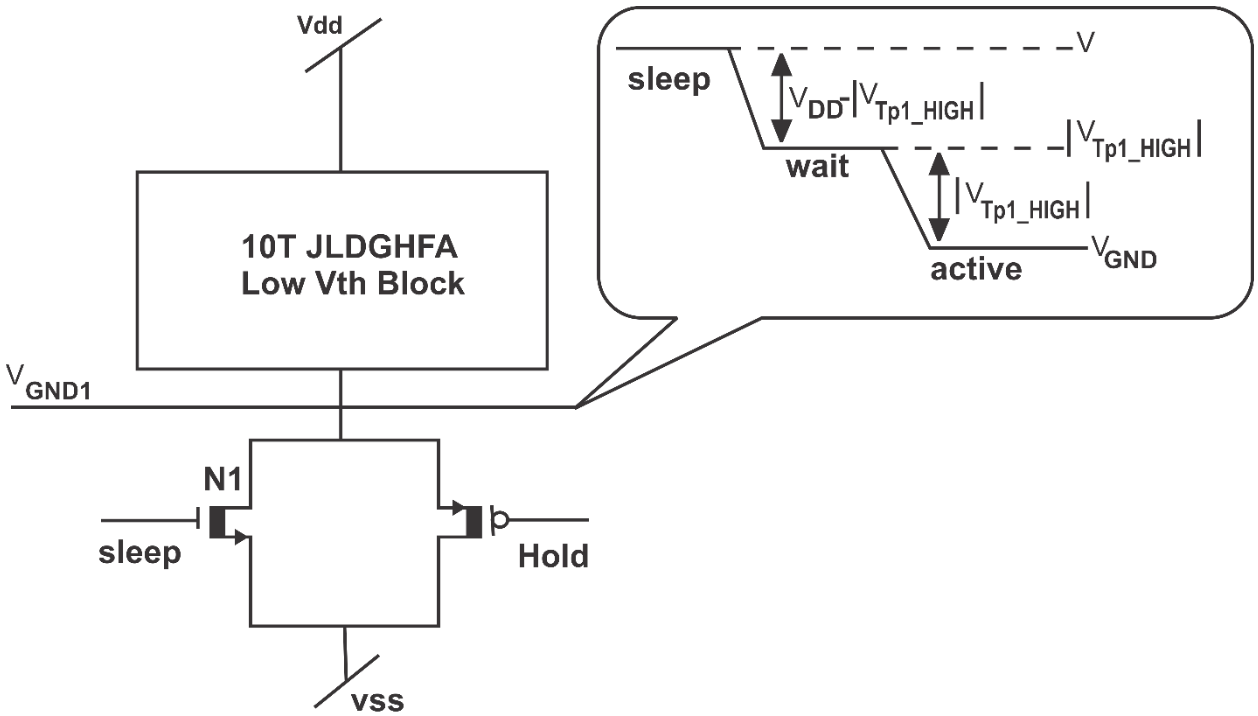


Figure 4.5 10TJLDGHFA's Block Diagram using the Tri Mode MTCMOS Process

When the supply voltage (VDD) approaches its maximum in base SLEEP mode, the virtual line voltage at the base rises. At a voltage of 0V [224], the real source competent in an MTCMOS circuit becomes completely wrinkled. In SLEEP mode, the leakage problem caused by the low voltage in the block circuit is mitigated. Figure 4.5 shows a block schematic of a Tri mode metal oxide semiconductor junction field effect amplifier.

4.7 SVL (Self Controllable Voltage Level) Technique

Using an SVL methodology, the charge circuit is split up with the highest possible voltage from the power supply in active mode, but the flow is slowed down by decreasing the leakage current via the gate. The voltage is thus somewhat reduced but still rather high while it is in standby mode. Switching off MOSFETs by charging the voltage will cause Vsub to decrease as V escalates as a current sub-limit drop [225]. In SVL, you may use one of three methods here: 1) USVL 2) LSVL 3) ULSVL.

Figure.4.6 illustrates this method, which combines Upper and Lower SVL approaches. When it comes to decreasing leakage power while a device is dormant, the ULSVL is better than other available solutions. Upper SVL provides Vdd to a series combination of PD NMOS transistors, but connects the PU PMOS in parallel. Lower SVL is about linking the PD NMOS transistors in parallel with the PU PMOS transistors in series. Upper and Lower SVL are used to serially connect a 10T JLDGHFAwhich show how prevalent is the usage of Vss.

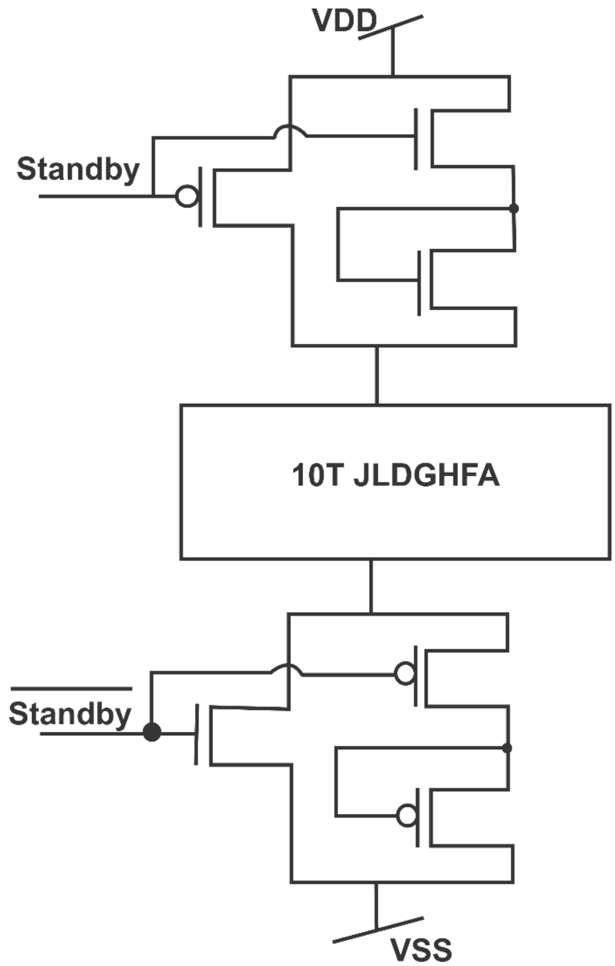


Figure4.6SVL Technique 10T JLDGHFA Block Diagram

4.8 The Outcome of Ten-Teraflop Computing on Low-Power Methods and Parameters

This work demonstrates that leakage power in MTCMOS technology may be reduced to 30% of the leakage current, and in Tri mode MTCMOS technology to 29% of the leakage current.

	Leakage Power	**Leakage Current**
SVL	4.18E-07	5.97E-07
TRI MODE MTCMOS	3.15E-07	4.50E-07
MTCMOS	4.15E-07	5.93E-07

Table 4.1 Parameters for 10T JLDGHFA Leakage in a Number of Low-Power Schemes

Using the SVL method, the leakage power may be reduced to 30% of the total current dissipation. Under typical conditions of use, Tri mode MTCMOS technology is also much more energy-efficient than MTCMOS and SVL techniques.

Static power, or power dissipation, causes leakage current and voltage in a CMOS transistor. While reducing static power consumption is preferable, minimizing transistor size remains a priority when dealing with power dissipation, even if static power may be an issue. Power dissipation may be significantly lowered using MTCMOS, Tri Mode MTCMOS, or SVL methods.

Energy Loss occurs when:

$$P(W) = C_L {V_{DD}}^2 f + V_{DD} I_{max} \left(\frac{t_r + t_f}{2}\right) f + V_{DD} I_{leak}$$

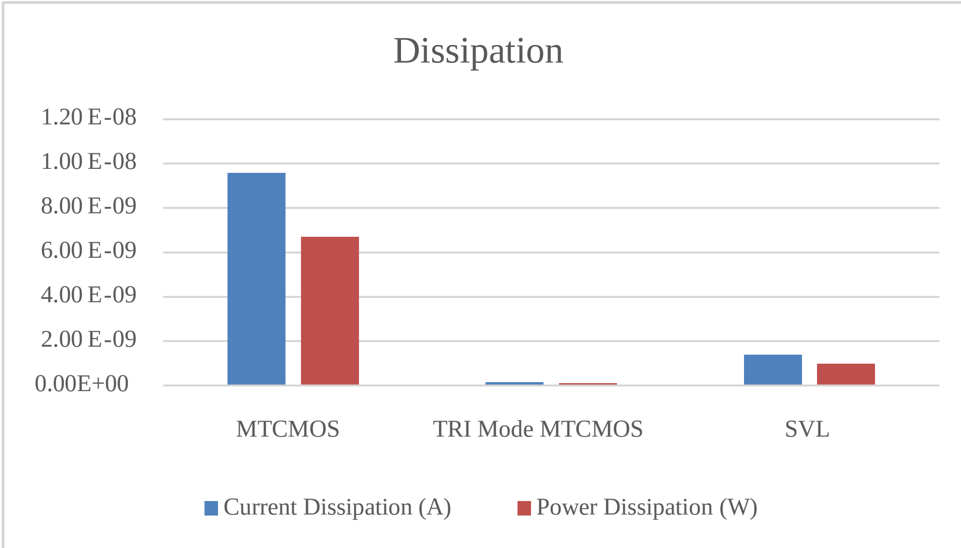
Instances when Dissipation of Current is achieved:

$$I(A) = \frac{P(W)}{V_{int}}$$

	Current Dissipation (A)	**Power Dissipation (W)**
SVL	$1.39e^{-09}$	$9.73e^{-10}$
TRI MODE MTCMOS	$1.38e^{-10}$	$9.69e^{-11}$
MTCMOS	$9.58e^{-09}$	$6.71e^{-09}$

Table 4.2 10T JLDGHFA Dissipation Parameters for a Variety of Du Methods

The findings display that the MTCMOS technique decreases power dissipation by 29.9 percent. With Tri mode MTCMOS, power consumption is cut down to only 29.78% of the total current dissipation. With SVL, power loss is cut to 30% of typical levels.



Graph 4.1Dissipation Parameters of Low-Power Methods asVisualized

4.9 Summary of the Chapter

Ultra-low power techniques (Multi-Terminal Complementary Metal Oxide Semiconductor Logic) like MTCMOS, Tri-Mode MTCOMS, and SVL have been presented in this area, along with Junction Less Double Gate (JLDG) MOSFETs and 10T Hybrid Full Adders (HFAs). Once these techniques were decided upon, we looked at the characteristics of leakage current & voltage and power dissipation. From this, we conclude that the Tri Mode MTCOMS method is more effective than MTCOMS and SVL in minimizing leakage current and voltage as well as power dissipation.

CHAPTER 5

MOS Degradation Lifetime in a Full Adder Predicted Using Reliability Methods (NBTI, HCI)

5.1 Aim of the Chapter

Keeping our purpose in sight, we propose some robustness parameters for a CMOS 8-Transistor Full Adder at 45 nm in this section. During a period of one year, researchers applied voltages of 0.7V, 1V, and 1.2V to the system in question in this study. We compare and contrast Hot Carrier Injection (HCI) in deteriorating and ageing NMOS with Negative Bias Temperature Instability (NBTI) in PMOS. Even if the HCI impact is considerably mitigated at low voltages and progressively declines at high voltages, modeling results show that the NM2 transistor will hurt the circuit at some point. The NBTI effect at PM1 and PM3 transistors is severely worsened at all adjustable voltages and causes the adder circuit to fail miserably. In this 8T complete adder circuit, NM2, PM1, and PM3 transistors are stressed. These recommended schematics and reliability characteristics are accomplished using the cadence virtuoso instrument.

5.2 Introduction

More functionality, low power, extended lifetime, and the requirement for increased integration in VLSI circuits are all factors that drive the trend towards downscaling CMOS technology, which is equivalent to Moore's principle. Several difficulties multiply and undergo physical alterations as this degradation grows to the micro scale [226]. An electrically active interface trapping caused due to the dissociation of passivated Si-H bonds at the gate oxide, NBTI in PMOS and HCI in NMOS, has become one of the most notable concerns in reliability during destructive down scaling of CMOS transistor. As a result, the device's efficiency drops and eventually breaks.

There is a comparison between the 6T and 5T SRAM cells that were suggested by ShyamAkashe et al. [227]. This work details the reliability study of PMOS transistors subjected to NBTI deterioration, NMOS transistors subjected to PBTI degradation, and HCIs subjected to both types of transistor degradation, among other models. The threshold voltage losses for the low-power 8T full adder built by Tripti Sharma et al. [228] are reduced by 45% compared to the prior work for the 16T full adder. For example, Seelam V S V Prabhu Deva Kumar et al. [229] have constructed a comparator circuit and analyzed its performance across a variety of reliability metrics including NBTI, PBTI, HCI, and Aging. The researchers in this study assessed the performance of the suggested circuit using simulations run at 1, 5, and 10 year lifetimes with applied voltages of 0.7V and 1.2V. At several micro scales, Hee Je Kim et al. have presented a 3-input CMOS LUT (90nm-45nm-22nm-11nm). Their study's practical application is analysing and improving the performance of a custom-made CLUT circuit. We compute the NBTI, PBTI, and HCI methods, and assess the leakage parameters and the average noise margin. Whole adders were built by Walid Ibrahim et al using logic gates. Whole device reliability estimates are extrapolated from gate-level evaluations of dependability. It helps in evaluating the potential for failure [230]. An adder is a crucial part of any computing or logic system. VLSI design is fluctuating in response to the growing need for low-power devices. Low-power applications may benefit from adiabatic logic-based circuits.

For 180nm technology, predictive technology characteristics are used in the design of complete adders. A comparison is made between several developed complete adders with regard to the number of transistors needed to build a complete adder, the time it takes for signals to travel through them, and the average amount of power they use at various input frequencies and capacitance loads. A complete adder built using static CMOS is also evaluated and compared to the findings. It has been discovered that complete adders constructed using adiabatic logic methods need much less energy than those crafted with static CMOS logic. It has been noted that the cost of reducing power consumption leads to increase in propagation latency. One adiabatic design of a full adder delivers up to 89% power savings compared to a full adder developed using static CMOS circuitry under specific operating circumstances. It is safe to say that the system's performance is mostly dependent on how the critical path transistors act. To sum up, the adders' performance is crucial to the VLSI system's ability to function with the current battery technology; however, researchers are torn between two competing design challenges:

(1) investigating high-performance design and implementation techniques that can meet the stringent speed constraints for real-time systems, and

(2) thinking about low-power design approaches to lengthen the operating time of portable devices.

You may quickly evaluate fundamental differences between the various building-block designs by comparing their power-dissipation and leakage current. Complementary pass-transistor logic is yet another standard adder (CPL). Large power dissipation may be attributed to the high number of static inverters and internal nodes. Transmission function Full Adders (TFAs) and Transmission Gate full adders (TGFAs) are two further examples of full adder architectures (TGA). The primary drawbacks of these logic types are their lack of driving capabilities and the drastic drop in performance that occurs when TGA and TFA are cascaded[331]. It is possible to divide these Full adder architectures into three sections. Each and every one of the circuits in Part I is either an XOR or an XNOR. Multiplexers and logic gates like XOR and XNOR predominate in Part II and III. Part I generates intermediate signals, which are then sent to Part II and III, which provide the SUM and CARRY outputs, respectively. One of the most important parts of a microprocessor or other complicated device is the full-adder. So, it stands to reason that the full-performance adders would have far-reaching consequences for the system as a whole [232]. Zipper CMOS domino full-adders are widely used in contemporary high-performance microprocessors and cache architecture because of its better speed and area characteristics as compared to static CMOS full-adders.

5.3 Performance Analysis

5.3.1 Reverse-Biased Junction Leakage

For example, think of a CMOS inverter that has a very high input voltage. In a circuit with no switching activity, sub threshold leakage current may still flow through a pMOS transistor because of the reverse potential difference of VDD between the drain and the n-well [233].

5.3.2 Sub threshold Conduction Leakage

The sub threshold Conduction current contributes to leakage current because carriers diffuse between the source and drain regions of the transistor during weak inversion. Sub threshold leakage current may flow even if no switching is happening in the circuit [234].

5.3.3 Leakage Power

Leakage power refers to the total power used by a CMOS transistor, including that used by sub-threshold currents and reverse biased diodes. When applied to a logic cell, the leakage power of a CMOS logic gate is independent of the input transition and load capacitance [235].

5.3.4 Sub threshold Current

However low the gate-to-source voltage is, the sub threshold current will always flow from source to drain. This is because in weak inversion, the CMOS transistor's source and drain regions undergo carrier diffusion. Sub threshold current is important when the voltage from gate to source is less than the threshold voltage of the device [236].

5.3.5Average Power

The total amount of power used by a CMOS logic gate's output switch may be calculated as P_{load} + P_{short} + P_{statc}. When the output load (CL) is equal to the supply voltage (VDD), the power dissipation (P_{short}) is 1, and the power consumption (P_{static}) is 0. The dynamic power consumption of a logic gate is denoted as P_{load}+P_{short}, where P_{short} is the power used while the output is not being switched. In a CMOS gate, P_{load} (output load charging and discharging) accounts for the vast majority of power consumption whereas static P (often ignored in power computation) accounts for just a tiny fraction. The output load of a gate is composed of the source/drain capacitance at the driver's output node, the interconnect capacitance, and the gate capacitance of the driven circuits. In a CMOS logic gate, it is important to minimize both the gate capacitance and the source/drain capacitance. When two logic gates are connected with wires, a capacitance known as interconnect capacitance is introduced and must be reduced. At the point in time t when the output state is changing, the power dissipation due to the short circuit is I(t) Vdd short.

As per the definition of short circuit time T, it is time spent in a state where there is continuity between the power source and ground.

The short P is directly related to the short circuit time, which should be minimized if possible. Widening the pMOS and nMOS transistors may decrease the latency of a CMOS gate for a given output loading and input rise/fall period (or input slew). The downside is that this would make CMOS logic gates even more power famished. While designing a CMOS logic gate, it is important to carefully consider the trade-off between power and latency. When given the output load CL and supply voltage VDD, Pload can be simply calculated, but Pshort is much more difficult to acquire. A b power meter may be used to determine Pshort. In Figure 1, we see a power meter [244] consisting of a Voltage-Controlled Current Source (VCCS) and a parallel RC circuit, both of which are used to measure the average power consumption of a specified circuit. The addition of the power meter to a simulated circuit doesn't significantly alter the results. If you have a circuit and want to know how much power it is dissipating on average, the power meter can do the job. Its operation is explained below [236].

5.4 8T Full Adder Structure and NBTI, HCI Mechanisms

Both Tripti Sharma et. al. [237] and Shubhajit Dutta Chowdhury et. al. [238] deliberate over the experimental principle features and performance of an 8T full adder. The authors of this study devote considerable attention to the proposed 8T Full Adder's reliability parameters, namely those of the NBTI in PMOS and the HCI in NMOS. The NMOS transistors (N1, N2, N3, and N4) are strongly impacted by HCI after the transmission of each NMOS gate source [239]. Different electrical fields propel carriers in the channel from source to drain. The drain's high voltage field may cause the hot carrier's accuracy to degrade until it reaches the drift speed's thermal limit (heat conductor). The gate oxide contact receives several electron holes from the heat carriers which generate electrons and the Si contacts a little more quickly. The threshold voltage is raised as a result of this event. Eq. 5.1 calculates how much of a change in starting voltage may be attributed to HCI. The hot-carrier trade-off of the MOSFET is associated with the present N-channel Isub. The substrate is linked together through the electric field in the channel that generates the most heat and the same heat flow connection that ultimately leads to the exhaust side. Gate degradation and power-driven force are regulated for Ig current in the p-channel of the MOSFET. [240].

$$\Delta V_{th} = A_{HCL} * \alpha * f * e^{\frac{v_{dd} - v_{th}}{t_{ox} E_i}} * t^{0.5} \qquad [5.1]$$

where, A_{HCL} is a technical consistency, α refers to the factor of action and f is the operation frequency. v_{th} and v_{th} represent the initial voltage and supply voltage. Thickness of t_{ox} oxide, the E_i affixed 0.8v / nm and t total operating time.

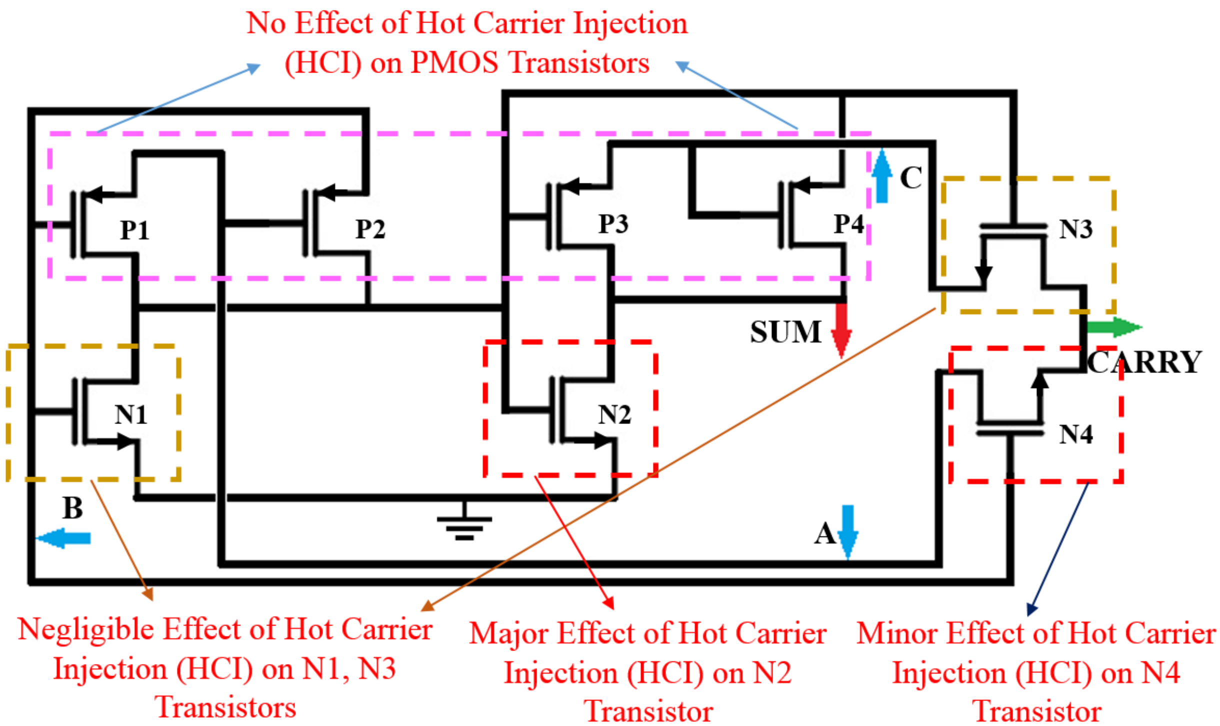


Figure 5.1 Effect of Hot Carrier Injection (HCI) on the Transistors

Vgs is a negative gate-source voltage for PMOS transistors (P1, P2, P3, P4), and NBTI is an early ageing equipment that generates experimental voltage intensity [241]. It is becoming hotter and hotter. The drain current and trans-condensation in a MOSFET both increase as a result of NBTI. The afflicted devices are P-channel when operating in NBTI with a negative gate to the source voltage. While the manufacturing technique involves oxidation, hydrogen transition is used to capture the Si molecules. The major roles of the timeline voltage of the device are the formation of donors, that is, interpersonal traps, and the breaking of these weak Si-H bonds at stages at high temperatures. The oxide in the H molecule shows fast variation in contrast to the H neutral molecule, which shows moderate variation. Hence, NBTI is a constant computation of trap waves at the Si/SiO2 interface of a single PMOS transistor. Interface traps under NBTI pressure are proportional to the total positive charges in the oxide group.

PMOS transistors include an NBTI process in which species of H molecules or H2 molecules spread. If the uniform band voltage is altered, the NMOS transistors' feed will reduce the number of available holes, leading to a decline in NBTI [242].

$$Si_3 \equiv SiH + H^+ \leftrightarrow Si_3 \equiv Si + H_2 \qquad (5.2)$$

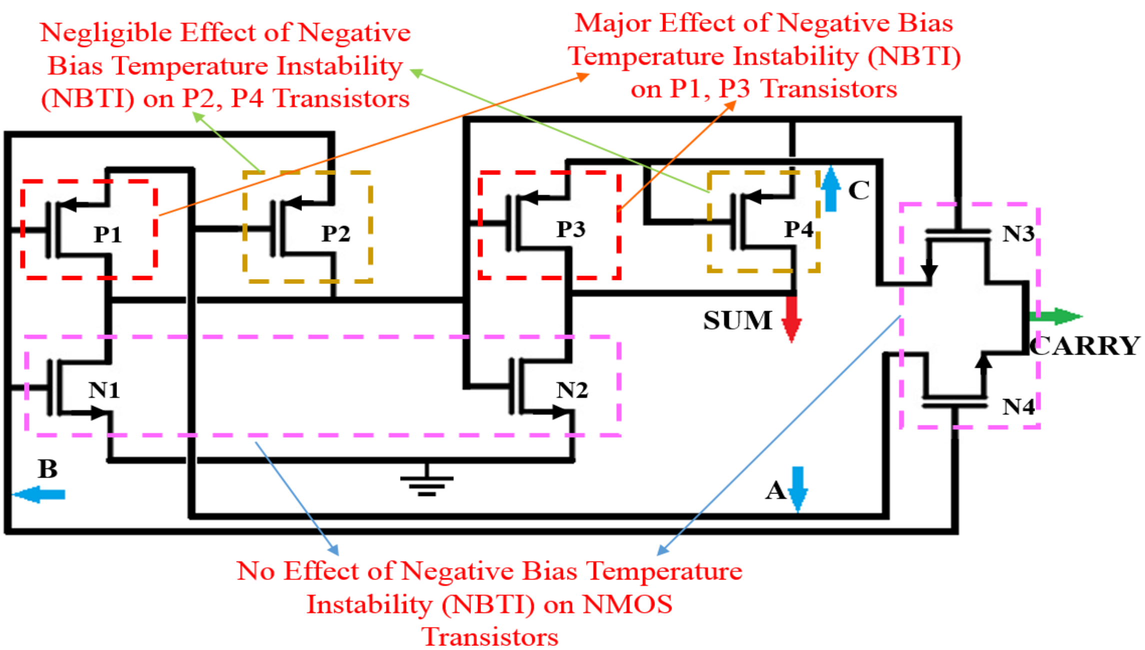


Figure 5. 2 Effect of Negative Bias Temperature Instability (NBTI) on the Transistors

5.5 Results and Discussion

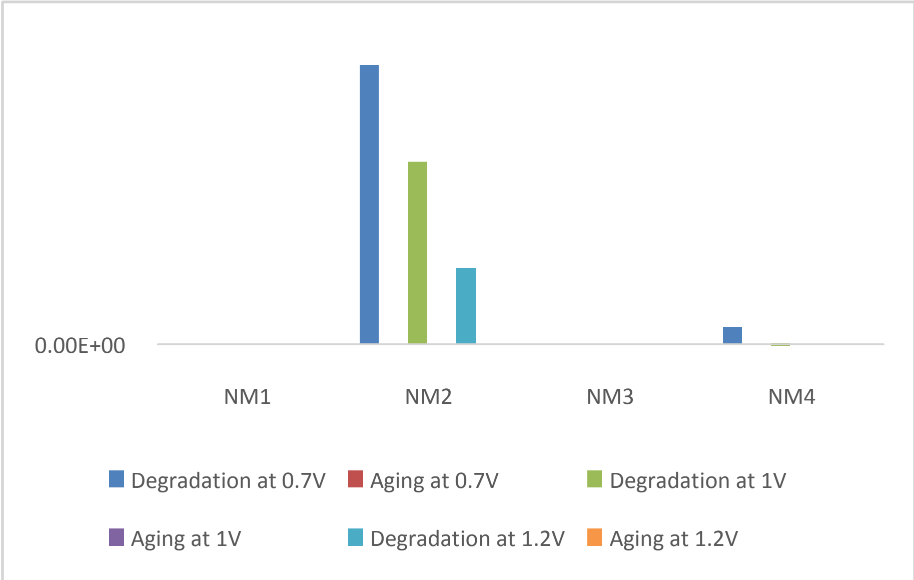
This study includes an 8-transistor complete adder circuit in 45nm CMOS technology, and analyses its dependability in terms of the NBTI and HCI. The transistor's capacity to function reliably at 0.7V, 1V, and 1.2V voltages is essential. Tab. 1. Compares the performance of individual NMOS transistors in a complete adder after one year of exposure to HCI deterioration and ageing.

Table 5.1

Shows the Comparison of HCI Effect on NMOS at 0.7v, 1v 1.2v in a Duration of a Year

Transistor	Degradation	Aging	Degradation	Aging	Degradation	Aging
	1 Year		1 Year		1 Year	
	0.7 V		1 V		1.2 V	
NM1	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NM2	7.32E-28	2.38E-70	4.79E-28	8.02E-71	2.00E-28	8.50E-72
NM3	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NM4	4.47E-29	1.82E-73	2.66E-30	1.31E-76	0.00E+00	0.00E+00

The deterioration of NMOS transistors is shown graphically in Figure 5.1, with NM2 damaged more severely than NM1, NM3, or NM4. Degradation of NM2 is three times as great at 0.7V as it is at 1.2V, and it is twice as great at 1V. It has been noted that the NM4 deteriorated only a little bit from its minimal state. The degree of deterioration of NM1 and NM3 is zero.



Graph 5.1 NMOS under HCI Degradation and Aging

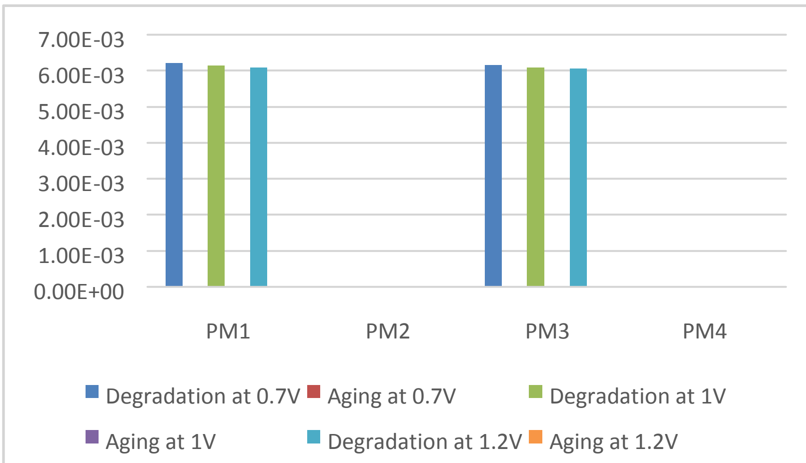
The transistor has to be reliably operated at voltages of 0.7V, 1V, and 1.2V. This table compares the performance of individual PMOS transistors in a complete adder as they age and degrade due to exposure to NBTI over a year.

Table 5.2
Shows the Comparison of NBTI Effect on PMOS at 0.7v, 1v 1.2v in a Duration of a Year

Transistor	**Degradation**	**Aging**	**Degradation**	**Aging**	**Degradation**	**Aging**
	1 Year		**1 Year**		**1 Year**	
	0.7 V		**1 V**		**1.2 V**	
PM1	6.21E-03	1.23E-11	6.14E-03	1.16E-11	6.10E-03	1.12E-11
PM2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
PM3	6.16E-03	1.18E-11	6.09E-03	1.11E-11	6.06E-03	1.08E-11

PM4	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

Highest deterioration of PMOS transistors is seen in Graph 5.2, with PM1 and PM3 being much more damaged than PM2 and PM4. Both PM1 and PM3 exhibit identical deterioration at 1V (0.7V) and 1.2V (1.2V), respectively. Similarities between PM1 and PM3 may be seen in its degradation. The degradation level of PM2 and PM4 is zero.



Graph 5.2 PMOS under NBTI Degradation and Aging

5.6 Summary of the Chapter

With low power CMOS devices, the longevity is a big issue when transistor sizes are reduced to 45nm. In this work, we examine the performance of the NBTI and HCI reliability characteristics across a range of operational settings and over a period of 1 year. The simulated findings show that the NMOS is very susceptible to deterioration and ageing due to HCI at low voltages of 0.7V and extremely so at high voltages of 1.2V, yielding NM2. Degradation and ageing of PMOS have a substantial impact on PM1 and PM2 throughout the board, as assessed by the measured voltages. The intrinsic MOS transistors of the 8T complete adder, however, are vulnerable to degradation. Certain corrective measures, essential for optimal performance and stability, must be taken to counteract this degeneration.

CHAPTER 6

Multiple Bit Full Adder Design Using m-GDI Technique

6.1 Aim of The Chapter

To meet strict power and space constraints, the most recent advancements in VLSI circuits necessitate the continuous modification of adder circuits through the use of many logic families. Whole adder circuits have decreased from 28T to as low as 13T to fit the low-power technology nodes. This article offers a novel approach for constructing an entire adder circuit using just twelve transistors. The study also includes an assessment of the proposed hybrid-based full adder logic architecture against traditional CMOS and TG full adders. The first, fourth, and eighth bits of the input data form the basis of the analysis. The above research makes use of Cadence virtuoso and GDPK 90nm technology. Parametric analysis aids in understanding the circuit's benefits and shortcomings, allowing for the creation of a superior complete adder block.

6.2 Introduction

6.2.1 CMOS VLSI Design

The integrated circuit industry has relied heavily on complementary metal oxide silicon technology for decades. When all other methods had failed, in 1963(nMOS and pMOS), Frank Wanlass of Fairchild created the first Complementary Metal Oxide Silicon (CMOS) logic gate. These circuits are likely to become the norm due to their low power consumption. Not until 1965 was the first MOS calculator shown, and by 1967 a wide range of MOS devices with practical applications in industry had been shown. By 1970, nMOS-based methods had become the standard. It was the 1980s when cloud cover over electricity use became a concern. The complementary metal oxide semiconductor (CMOS) strategy is largely responsible for the development of thin-film transistors. First developed were inverters, then NOR gates, and finally NAND gates, the three fundamental building blocks of modern computing. Technology based on Complementary Metal Oxide Semiconductor (CMOS) may be used to build integrated circuits[243]. CMOS technology is used in all modern digital logic circuits including microprocessors, microcontrollers, static RAM, and more. Analogue circuits that use CMOS technology include image sensors, data converters, and highly integrated transceivers. Because of this, CMOS has largely replaced bipolar technology as the go-to for VLSI devices. Very large-scale integration (VLSI) is used to fit a huge number of transistors onto a single chip, allowing for the creation of an IC. The development of VLSI followed developments in both the complexity of semiconductors and communication systems. Most integrated circuits (ICs) had a well-guarded strategy of probable failure spots until the advent of VLSI development. VLSI enables IC enablers to combine them all onto a single chip.

An exclusive group of inventors tested devices in the mid-1920s that would regulate the current in solid-state diodes and turn them into triodes. After a period, specialists turned their attention back to the radar movement and returned to the strong state gadget revolution. The transition from vacuum tubes to solid-state components in the hardware industry was made easier by the development of transistors. The little transistor allowed electrical designers of the 1950s to anticipate the consequences of building ever-more complex circuits, both inside and outside the house. Numerous problems resulted from the circuits' haphazard construction. One potential cause of problems in the circuit is the compass. Complex circuits like computers have to operate quickly. In September 1958, he designed and built his own mixed circuit.Putting together cables and splices is now unnecessary [244].

Most modern-day engineers employ VLSI technology. The low-density manufacturing technology known as Small Scale Integration (SSI) was developed in the early 1960s. Starting with just 10 transistors in Small Scale Integration (SSI), the number of transistors on a single chip rapidly increased to 100 in the late 1960s with the advent of Medium Scale Integration (MSI).

Transistor-transistor logic (TTL) has been the foundation of the first integrated circuit revolution, supplanting other IC families like ECL because of its high integration densities. Large Scale Integration (LSI), which involved the placement of about a thousand transistors on a single chip, was pioneered in the early 1970s. Very Large-Scale Integration (VLSI), a term coined in 1970, emerged as a result of the simplification of previously complex semiconductor and communication technology. It's a setup where more than a thousand different types of transistors may be manufactured on a single silicon chip. VLSI allows for the integration of a digital circuit's central processing unit, random access memory, read-only memory, and various glue logic components onto a single chip. The size of the transistor was one of the main problems that needed solving before VLSI was developed. The complexity and performance assessment of VLSI ICs are improving as a result of the shrinking device dimensions brought on by technological progress [245]. The first Intel 4004 microprocessor appeared in 1972, and its successor, the 8080, appeared in 1974, ushering in the second technological revolution brought about by integrated circuits. Some examples of companies interested in "VLSI" include Cadence, Alliance Semiconductor, Texas Instruments, Synopsys, Infineon, Celox Networks, Cisco, National Semiconductors, Lucent, Micron Tech, ST Microelectronics, Philips, Qualcomm, Mentor Graphics, Intel, Analogue Devices, Motorola, and others. CMOS circuits have relentlessly shrunk in size in order to achieve better and coordinated thickness in each successive generation of technology. Given the trends in today's Nano size technology for CMOS circuits, effective preparations must be made to reduce spillage control; otherwise, spillage power would eventually command the chips, which will contribute to control utilisation. These arrangements can be linked at the framework and structural level, the circuit level, and the device/process level of design reflections. Coordinated circuits are utilised by means of CMOS technology. The CMOS technology is used in microcontrollers, microchips, SRAM, and other sophisticated circuits. CMOS technology is used for basic circuits like those used in cameras, highly integrated mobile phones, data converters, and many forms of communication. Complementary Metal Oxide Semiconductor, or CMOS for short, combines the best features of complementary metal oxide semiconductors. The CMOS device's primary characteristics are great noise immunity and low static power. Compared to other rationales like Transistor-Transistor-Rationale (TTL) or NMOS rationale, which enclose some standing current even when they don't change the state, CMOS devices have the advantage of producing less waste heat. The CMOS device also makes it possible to pack a lot of logic into a single chip. For this reason, very large-scale integrated circuits (VLSIs) are often produced using CMOS equipment. [246].

6.2.2Evaluation of Hybrid Adder

As technology progressed, more transistors were introduced, leading to the union of more distinct terminals or structural elements. Integrated circuits were first able to build several logic gates on a single device since they only had a few components, potentially up to ten diodes, transistors, resistors, and capacitors. The reorganisation of framework-initiated devices with diverse systems for thinking entrances is known as Medium-Scale Integration (MSI), formerly known as Small-Scale Integration (SSI). As a result of further redesigns, LSI (Low-Entry-Models) were developed to organise different ways of thinking. Modern semiconductors have many gates and billions of discrete transistors, vastly beyond the imprinting of the past. There was a commercially viable option for billion-transistor processors by the middle of 2008. As transistor technology progressed beyond the then-current 65 NM boundary, this became increasingly commonplace. Transistors are a prime example of how modern designs deviate from traditional devices by allowing for more precise measurements of the complex nature of the value calculation that follows. To ensure the highest quality, some large-scale thinking components, like as the SRAM (Static Customary Access Memory) cell, are still drawn by hand. VLSI innovation may proceed towards even more extreme reduction as NEMS technology advances. [247].

6.2.3Need of Hybrid Adder

The motivation for the VLSI design came from Carver Mead and Lynn Conway's intention to limit the variety of linking fabrics in order to maximize the usable space on microchips. Creating the big, rectangular squares needed to be linked together via projection is a time-consuming procedure [248]. This diagram shows the cellular structure of a snake broken down into its constituent parts. This categorization may be ruled by multilevel nesting in complex brains. However, by the mid-1980s, designers had learnt to restrict the proximity of arrangement and the strength of regulating devices in order to take use of the growing range made available by Moore's Law, and their knowledge of the foundations of organized VLSI architecture had eroded. In the mid-1970s, Reiner Hartenstein presented the apparatus depiction vernacular KARL, coining the term "sorted out VLSI plan" (originally as "formed LSI configuration") to echo Edsger Dijkstra's fabricated programming framework of the system settling to keep up a key partition from ramshackle spaghetti-created assignment.

6.2.4 Challenges

The complexity of microchips is increasing as a consequence of scaling improvements, and this has prompted chip makers to reevaluate their approach and begin making preparations for a post-silicon world.

High precision in doped focuses and scratched wires becomes increasingly challenging and prone to mistake when photolithography frameworks converge on the basic principles of optics. It is now necessary for producers to re-execute their work in several areas of the creation framework before a chip can be assured to have an orchestrated theme.Scale issues in lithography and engraving have led to stricter criteria for layout. Coordinators should consider at least one of these guidelines while laying up novel circuits.

There are many subfields of computer architecture within the VLSI field. The Arithmetic Logic Unit (ALU) is a crucial component of modern computers. The power efficiency and small size of the ALU are the results of many different kinds of work. Binary addition and subtraction are just two of the fundamental building elements of ALU architecture. In recent years, many different approaches and strategies have been integrated into the readily accessible technology in order to construct a useful and efficient addition block. The researchers' end objective is to create a Full Adder (FA) that uses less die space and generates less power consumption. The FA also has to have dependable driving ability and a decent output swing in addition to the aforementioned qualities. It all has to do with the FA's construction technique [249].

Twenty-eight transistors are required to construct a conventional CMOS FA block. This method of design is scalable, robust against changes in device size, and has high driving capability. The inefficiency of the layout worsens as the number of transistors used in the design increases. Buffers may need to be implemented in the system if there are significant delays in sum and carry blocks. A 32-transistor, modified FA design was created to enhance the voltage swing of the system utilising CPL logic. As a result, more switching power was available in the design. Because of this, the number of transistors in the circuit was reduced by the study team. The die size might be drastically reduced by using XNOR logic, as previously proposed [250].

The FA circuit is implemented in the study utilising the m-GDI approach at 90nm technology nodes, which reduces the number of transistors to twelve(8T), resulting in much lower average power consumption. Cadence Virtuoso's GDPK 45 library is used to compare the design against preexisting TG,CMOS and hybrid designs for 8-bit, 4-bit, and 1-bit adders.

6.3 Design Structure ofFull Adder

To create a complete adder, the transistor must be oriented in three distinct blocks. A and B are supplied into the first XOR gate. The sum logic of the FA [251] is satisfied by the second cascaded XOR block receiving the output of the matching block. Table 6.1 depicts the truth table that must be satisfied before the carry output may be formed using the first XOR block and the carry input port. The block diagram is represented in Figure6.1.

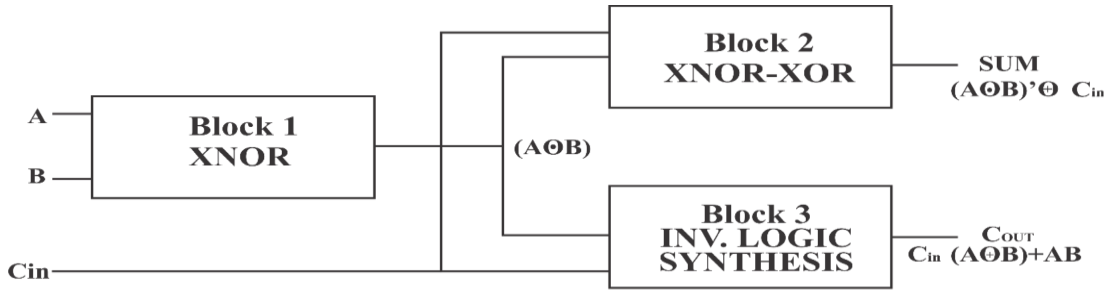


Figure 6.1 Functional diagram of Full Adder

6.4 Static CMOS Full Adder (1-BIT)

One-bit full adder CMOS circuit diagram is shown in Figure 6.2. There is a total of 28 transistors in this layout [252], 14 NMOS and 14 PMOS. The building may be sectioned up into the aforementioned three sections. The truth table in Table 6.1 is used to guide a transient analysis.

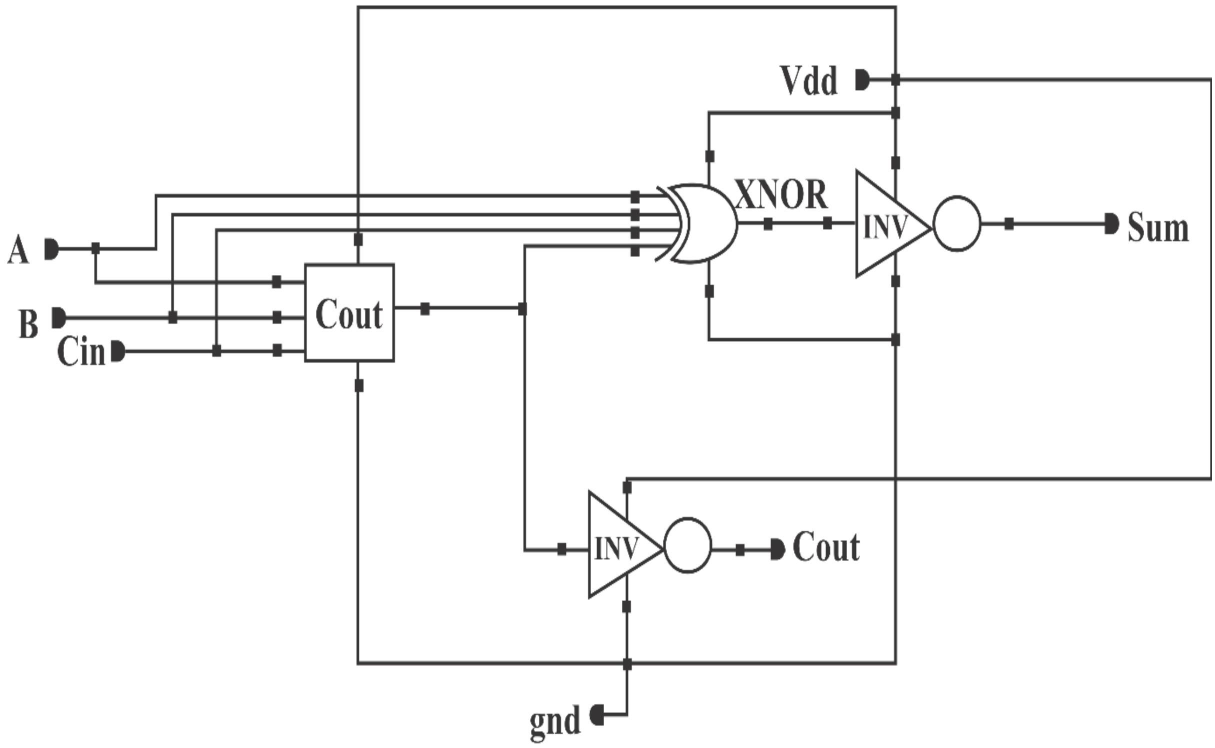


Figure 6.2. The 1-bit Full Adder Circuit Diagram in Static CMOS was produced in Cadence Virtuoso.

6.5 TG Full Adder (1BIT)

Using the principles of the transmission gate, these 20 transistors have effectively integrated the functions of a Full Adder. By arranging 12 transistors into 6 transmission gates and employing the remaining 8 as inverters, we may achieve the necessary logical function of an FA [253]. The basic layout of a 20T TG FA is seen in Figure 6.3.

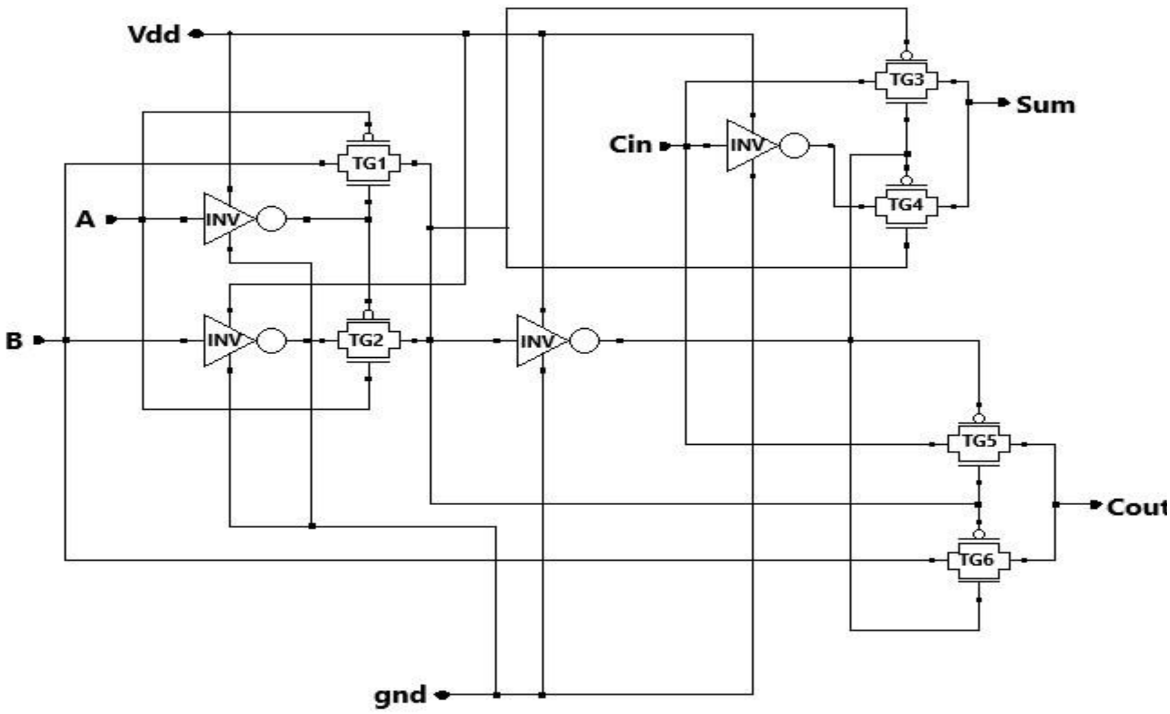


Figure 6.3Using a Transmission Gate (TG), this circuit is a 1-bit full adder.

6.6 Hybrid Full Adder (HFA-1BIT)

A variety of hybrid designs for use in a Full Adder circuit have been created by the authors cited in references 20–23. A plan for constructing a practical FA out of 12T is proposed in this chapter. A transmission gate coupled with static CMOS can be used to generate the logic functionality. This building is made up of three separate units [254].

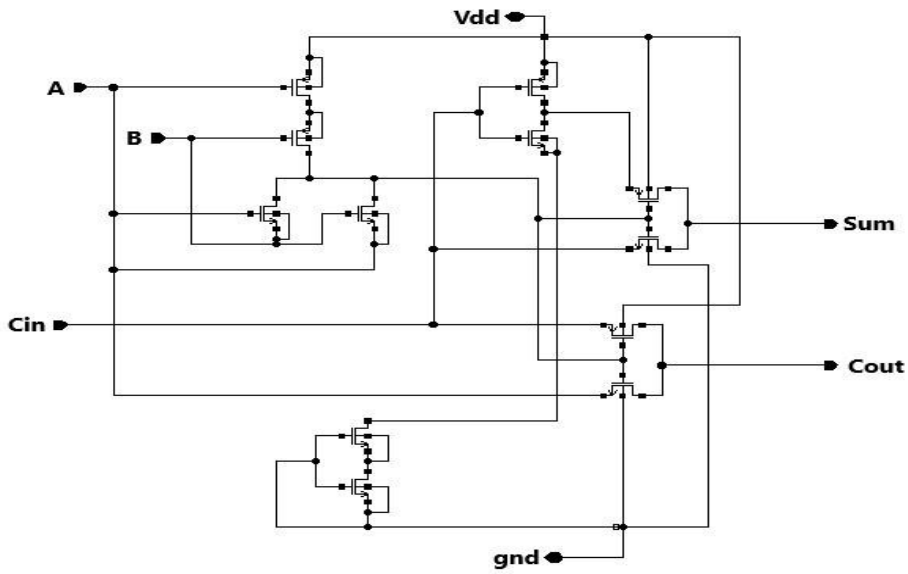


Figure 6.4An Integrated Circuit with a Hybrid Full Adder Using 12T

The first step is to combine signals A and B to form the XNOR block. The Sum block is addressed by this XNOR in logical conjunction with the input carry (C_{in}) port. Similarly, the XNOR and the required logical link drive the carry output (C_{out}). Figure 6.1 depicts a modular method to proposing this structure, and Figure 6.4 depicts the schematic design for implementing the suggested structure as HFA [255].

6.7 Proposed GDI Implemented Full Adder (1-BIT)

It is possible to realise a whole adder circuit by using a modified Gate Diffusion Input. Cascading the XOR logic deduced from reference 24 allows for the creation of the Sum block. However, pass transistor logic may be used to provide a parallel log version of C_{out}. The output swing voltage suffers as a result of this method, but the effective number of transistors is considerably reduced. More significant reductions in power usage are achieved compared to the hybrid FA design [256]. Figure 6.5 depicts the m-GDI logical layout for XNOR implementation. Figure 6.6 depicts the suggested technique's schematic.

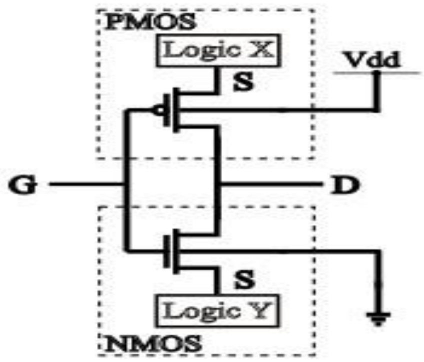


Figure 6.5The PMOS and NMOS Source, Drain, and Gate Connections

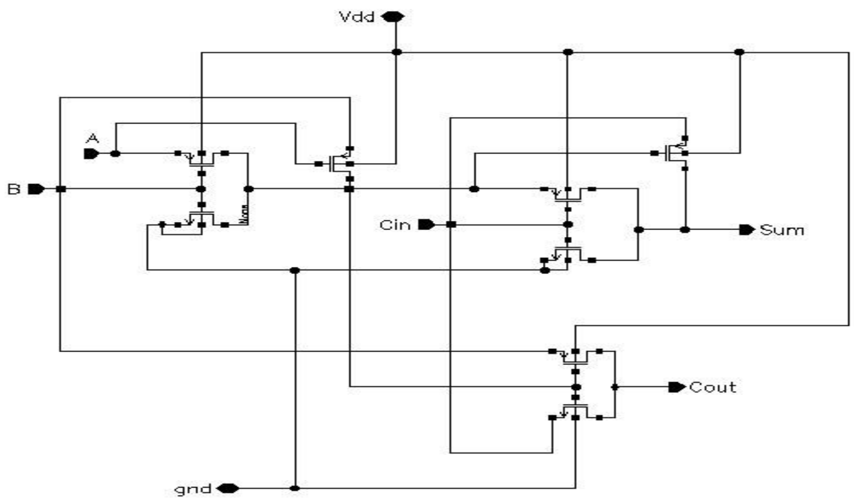


Figure 6.6Full Adder Structure Layout with the m-GDI Method

6.8 4-BIT and 8-BIT Structure

Four- and eight-bit FA are structurally similar to their one-bit counterparts. The various bit properties of the FA are identified using a symbolic model technique [257].

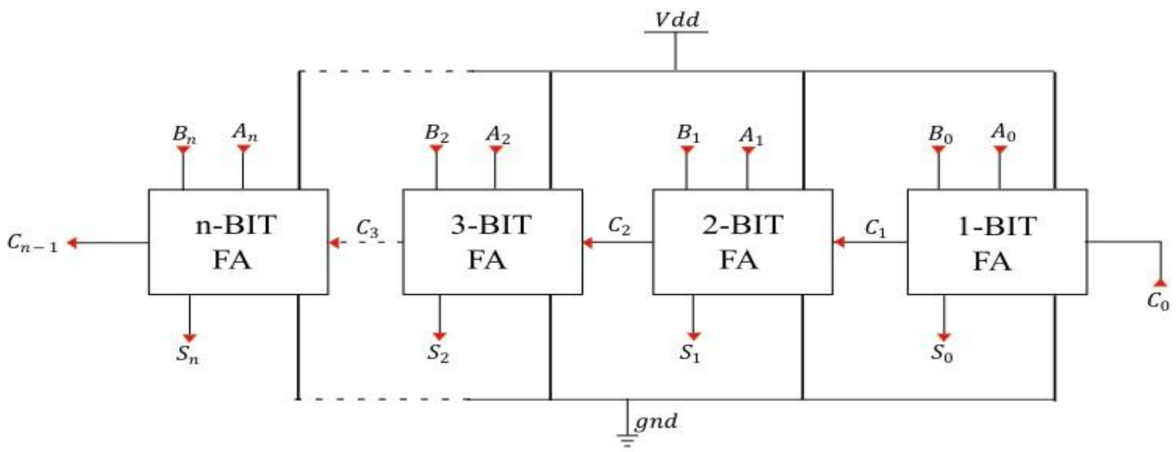


Figure 6.7Structure of n-bit Full Adder

Assuming an n-bit architecture, n such 1-bit blocks would be cascaded so that the C_{out} of the first block would be the C_{in} of the second. It must be emphasised that the first block's C_{in} must be grounded for proper logic operation.

The inputs, SUM, and CARRY pins of a 4-Bit and 8-Bit FA structural architecture are depicted in a block diagram in Figure 6.1.

6.9 Results and Analysis

Figure 6.6 depicts a potential architecture for a single-bit m-GDI full adder. In order to limit dissipation in the structural design, the suggested design takes into account the power constraint. When the number of transistors employed decreases, the amount of space required on the die also decreases. In this work, a 1-bit m-GDI FA adder circuit is simulated in cadence to ensure proper operation. The 1, 2, and 8-bit Static CMOS, TG, and Hybrid designs are also simulated for study. First, the aforementioned data bits undergo a transient analysis with a time window of 100ns. The data bits are then supplied into a pulse voltage that ranges from 1V at the top to 0V at the bottom. By applying various pulse voltages to each input bits, it is possible to maintain a constant pulse voltage while achieving the necessary pulse width variations. The analysis of the SUM and C_{out} output pins involves comparing the simulation graph's input signal to the required output values. The circuit verifies the FA's functional behaviour if the levels of the simulated graph's output agree with the truth table shown in Table 6.1. The simulation results are depicted in Figures 6.8, 6.9, 6.10, and 6.11 for the 1-bit static CMOS, TG, Hybrid, and proposed m-GDI FA.

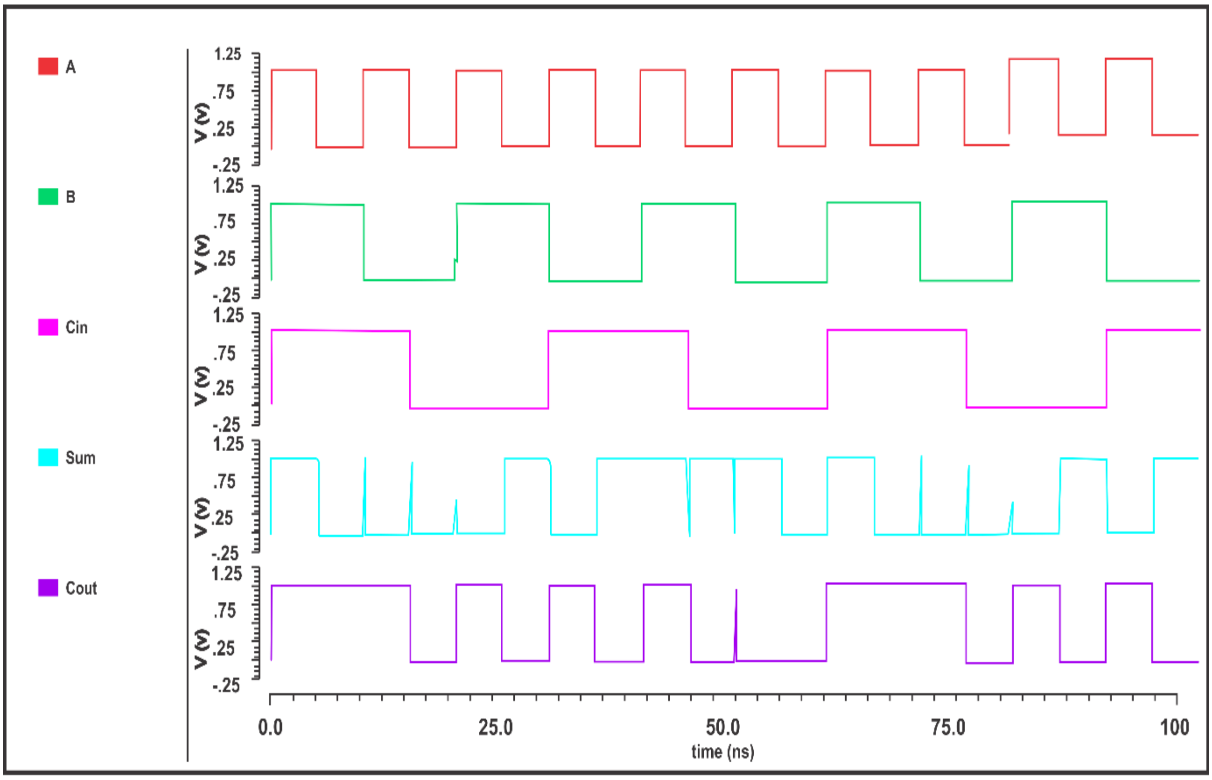


Figure 6.8One-Bit Static CMOS Full Adder's Transient Response

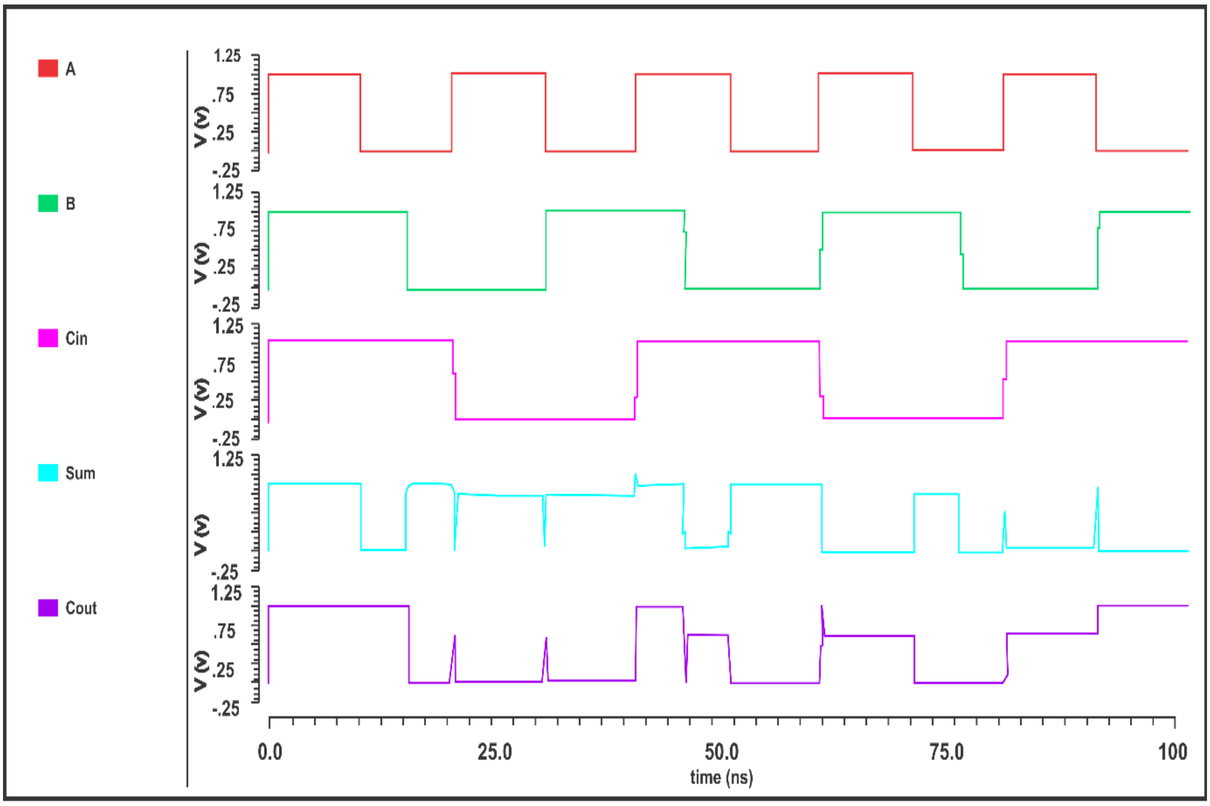


Figure 6.9The Transient Behavior of a Full Adder Based on a Transmission Gate with 1 Bit of Memory

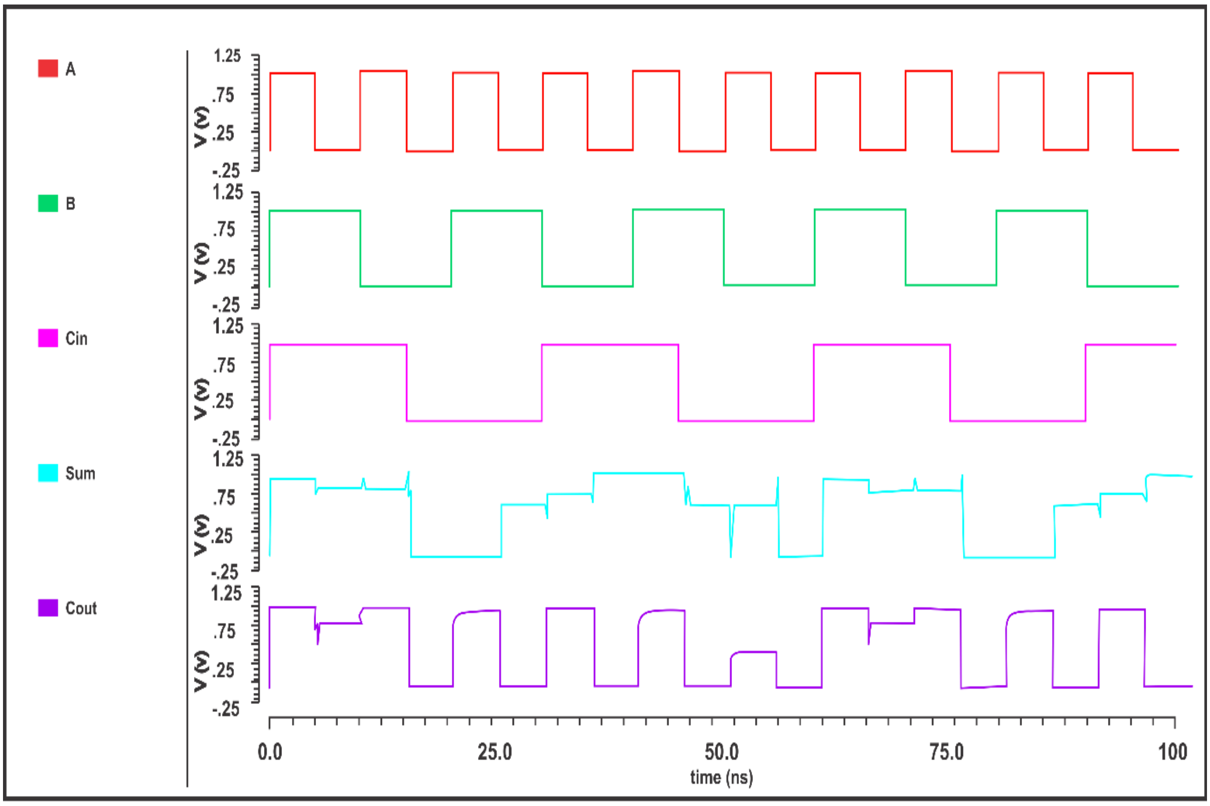


Figure 6.10One-Bit Hybrid Full Adder's Transient Response

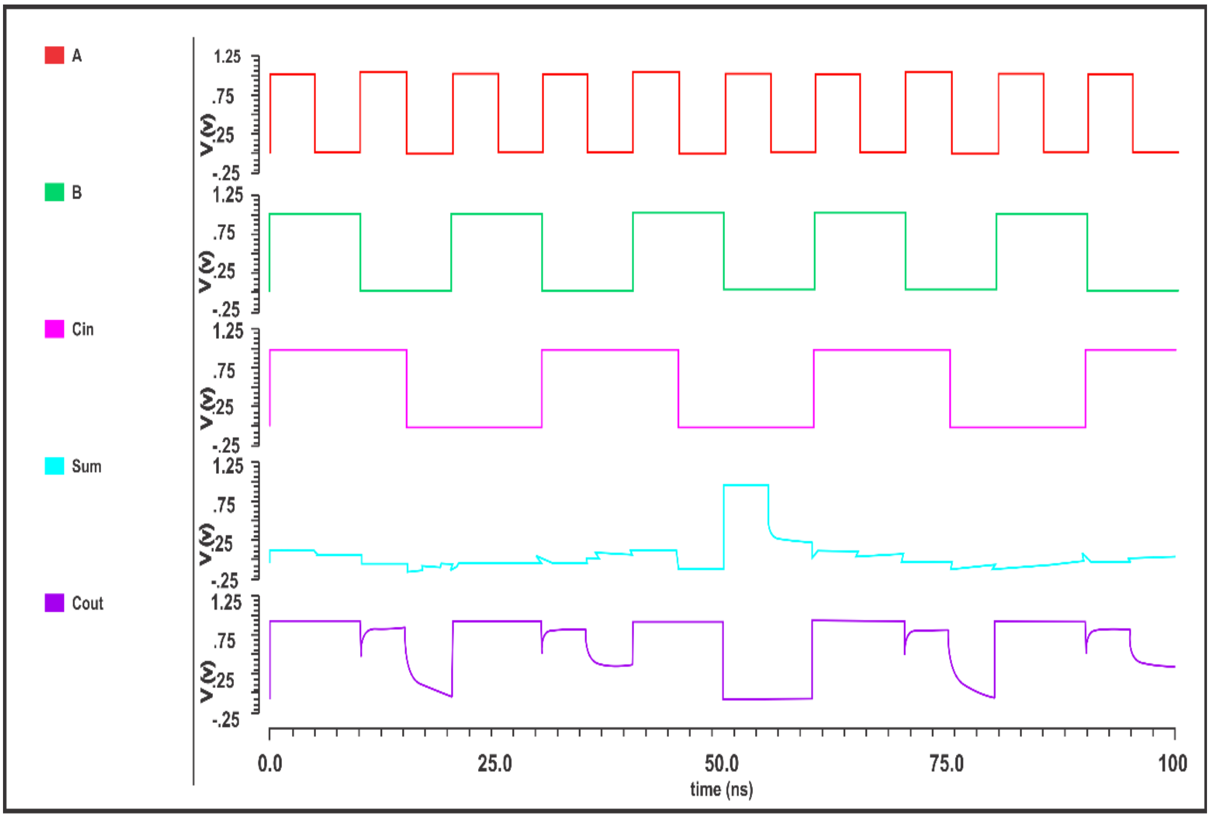


Figure 6.11Proposed GDI Full Adder with a Bit-Level Transient Response

6.10 Comparison

A comparison of Static CMOS, TG, hybrid, and the planned m-GDI FA forms the backbone of this section. Certain factors are held constant throughout the analogy and form the basis of the analysis. All three buildings have the same temporary operating time and conditions. For the DC analysis used in the computation of the comparison study, Vdd is held constant at 1V for all the structures. All simulations in Cadence Virtuoso use the 90nm technology node from the GDPK library. The study is simplified if we assume there is no increase and fall period to compare. The comparison of the aforementioned circuits and designs may be seen in Tables 6.1, 6.2, and 6.3.

Average transient power, C_{out} delay, SUM delay, Power Delay Product (PDP), and transistor count are some of the factors under consideration.

	Static CMOS	**TG**	**Hybrid**	**Proposed GDI**	**Percentage improvements**
Transistors count	28	20	12	8	35%
Average power	47.31E-6	28.71E-6	30.01E-6	17.65E-6	38%
Carry delay	57.60E-12	38.32E-12	50.048E-12	51.19E-12	19%
Sum delay	50.51E-12	46.02E-12	41.92E-12	50.81E-12	2%
PDP	2.38	1.32	1.25	0.896	28%

Table 6.1Table showing the differences between the aforementioned 1-bit FA structures

	Static CMOS	**TG**	**Hybrid**
Transistors count	28*4	20*4	12*4
Average power	89.49E-6	66.87E-6	60.4E-6
Carry delay	84.33E-12	80.5E-12	68.1E-12
Sum delay	95.05E-12	65.69E-12	51.38E-12
PDP	8.50	4.39	3.10

Table 6.2Table showing the differences between the above 4-bit FA structures

	Static CMOS	TG	Hybrid
Transistors count	28*8	20*8	12*8
Average power	127.26E-6	116.0E-6	96.95E-6
Carry delay	184.3E-12	159.4E-12	127.6E-12
Sum delay	194.6E-12	161.0E-12	128.2E-12
PDP	2.47	1.86	1.24

Table 6.3Table showing the differences between the aforementioned 8-bit FA structures

6.11 Discussion

The simulations outlined above offer a convenient means of doing functional validation. An evaluation of the SUM and CARRY outputs is performed. Subsequently, a comprehensive study is conducted, whereby several bits are examined, and a comparative chart is presented including all the designs. In order to maintain analytical simplicity, the available bits are limited to 1, 4, and 8 bits. The suggested 1-bit GDI FA is used as a benchmark to evaluate all existing full adder designs. By employing a mere 8 transistors, the dimensions of the object are significantly diminished. Upon careful examination of the simulations, one may observe a trade-off in the output voltage swing. The reduction in voltage swing is accompanied by a consistent PDP need of 0.9 pJ. In comparison to all alternative circuit designs for a comprehensive adder, this numerical value is comparatively lower than that of any other design. Additionally, there is a significant decrease in the average transient power consumption associated with this approach, which is approximately 16.65 micro Watts. The sum and carry output exhibit a respective delay of 50.81 picoseconds and 51.19 picoseconds. Hence, it is possible to arrive at a determination on the most efficient configuration for a comprehensive adder circuit, taking into account considerations of both die area and power consumption.

6.12 Conclusion

Full Adder's cutting-edge ideas are an integral element of the vast majority of modern electronics. Smaller and more space-efficient ALU designs have been made possible by the transition of the Full Adder from CMOS logic to hybrid logic architecture. In this research, we employ an m-GDI logic paradigm to create a Full Adder block with low power consumption and small footprint. The study compares several design structures by using the corresponding bits of information to draw conclusions about their relative merits. The results of this research can be used to improve the architecture of future implementations of the Full Adder within ALU. The voltage swing of the design may be examined more thoroughly and optimised as a starting point for further investigation. This layout may be studied in the future to determine the best possible net list and layout design.

CHAPTER 7

SIMULATION RESULT AND DISCUSSION

Cadence IC 6.1.5 version is used to create the first suggested Low Power Full Adder. For output simulation, a spectral cadence threshold (spectre) simulator is utilized.

7.1 Power Consumption

The total power dissipation of a digital circuit consists of two parts and may be stated as [258]. This is the most pressing technological issue now confronting the semiconductor industry.

$$P_{total} = P_{dyn} + P_{static} \tag{7.1}$$

WhereP_{dyn} = dynamic power dissipation

P_{static} = static power consumption

7.1.1 Dynamic power

The average dynamic power consumption is equatedas [263]-

$$P_{dyn} = (1/2)\, C_L V^2_{dd} \alpha . f \tag{7.2}$$

Where,$\mathbf{C_L}$is the switching capacitance,

$\boldsymbol{\alpha}$ is the switching activity of output node and

f is the operating frequency

7.1.2 Static power

The static power consumption can be expressed as [264]-

$$P_{static} = V_{dd} * I_{static} \tag{7.3}$$

where, t_{avg} = Average gate delay, t_{dr} = Rise time delay and t_{df} = fall time

The FinFET-based Priority Encoder was simulated using Cadence Virtuoso at a 45 nm technology node. The simulation allowed us to evaluate the device's average power consumption, leakage power, and leakage current across various voltage levels. After conducting a comprehensive analysis of the data, it was determined that the Priority Encoder using FinFET technology has significantly improved performance at a voltage of 5V. Various circuit approaches were used in our study, such as metal-oxide-semiconductor-metal-oxide-semiconductor (MTCMOS) and silicon-controlled-metal-oxide-semiconductor (SCL) logic.

7.1.3 Leakage Power

The utility of devices is reduced as a result of power loss and leakage. Furthermore, it is important to note that the charge of any electronic device will progressively diminish over time as a result of leaking power. This phenomenon, quantified in Watts, persists even while the device is in an inactive state.This is quantitatively expressed as [259]-

$$P_{leakage} = I_{leakage} \times V_{dd} \tag{7.4}$$

where $P_{leakage}$ is the leakage power, $I_{leakage}$ is the leakage current and V_{dd} is the power supply voltage.

7.2 Stacking Power Gating Technique Applied on 10T Full Adder Cell

By using the stacking architecture, it becomes possible to effectively reduce the magnitude of leakage current during the standby mode. There is a prevailing trend in the field to use transistors characterized by a reduced threshold voltage (Vth), and efforts are on to advance nanoscale technology to accommodate this development. The reduction of leakage current in standby mode is imperative, necessitating a substantial improvement over the existing conventional power gating approach. The design of the power gating approach is shown in Figure 7.1. The image clearly illustrates the arrangement of two NMOS transistors connected in series to provide a connection between the logic circuit and the ground. Furthermore, it is worth noting that both M1 and M2 sleep transistors are arranged in a stacked configuration in this context.

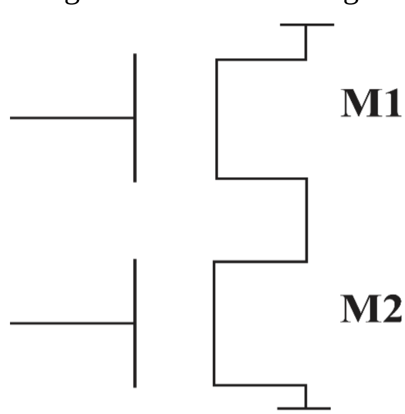


Figure 7.1: Stacking Structure

The determination that the system is in standby mode is made when both M1 and M2 are deactivated. The stacking effect is used in this arrangement to effectively reduce leakage current by simultaneously deactivating both M1 and M2 sleep transistors. Consequently, the minimal drain current induces a rise in voltage at the intermediate node, VGN, leading to positive values. [260]. The implementation of the stacking power gating approach on a 10-transistor full adder cell results in a reduction in both leakage current and latency in the cell's standby state. The input-output waveform of a 10T full adder cell using the stacking power gating technique in standby mode is seen in Figure 7.2.

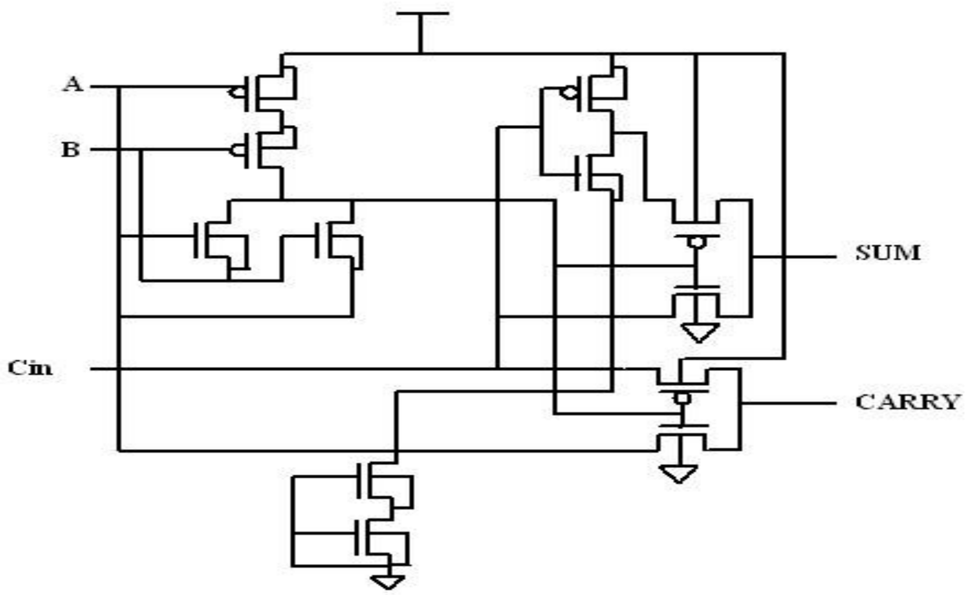


Figure 7.2. Schematic of Full Adder using Stacking Power Gating Technique

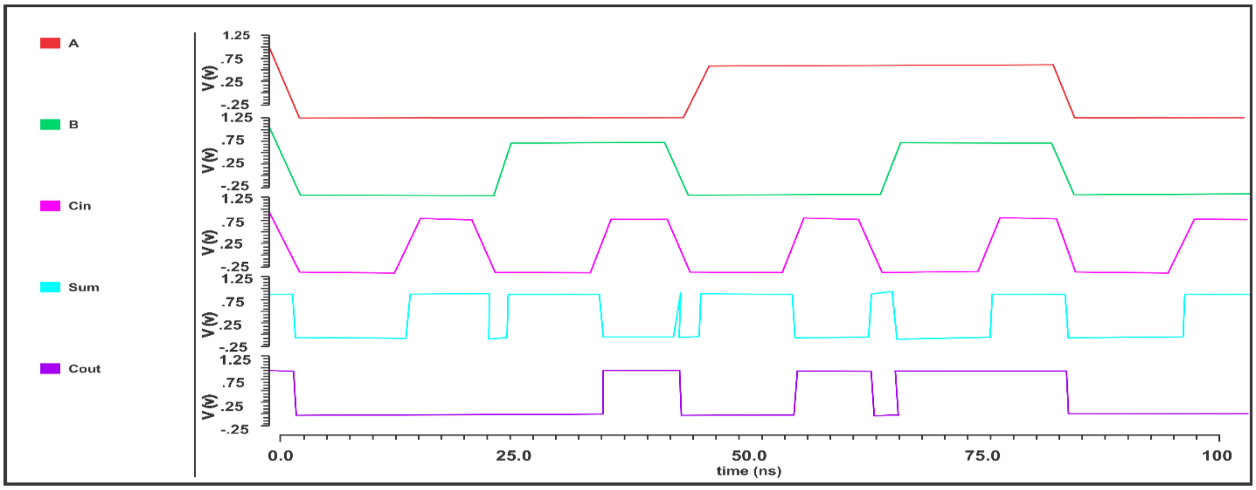


Figure 7.3 Input Output Waveform

What happens to a circuit's power supply while it's idle?

In the context of a 1-bit full adder circuit, the sleep transistor is connected to the NMOS pull down network and its functionality is deactivated when a voltage of 0V is supplied to the network. The dimension of a sleep transistor is determined by the size of the largest transistor in the network (either pull up or pull down) that is connected to the sleep transistor [261]. The waveform of the leakage current during sleep is shown in Figure 7.4, with a magnitude of 9.51nW.

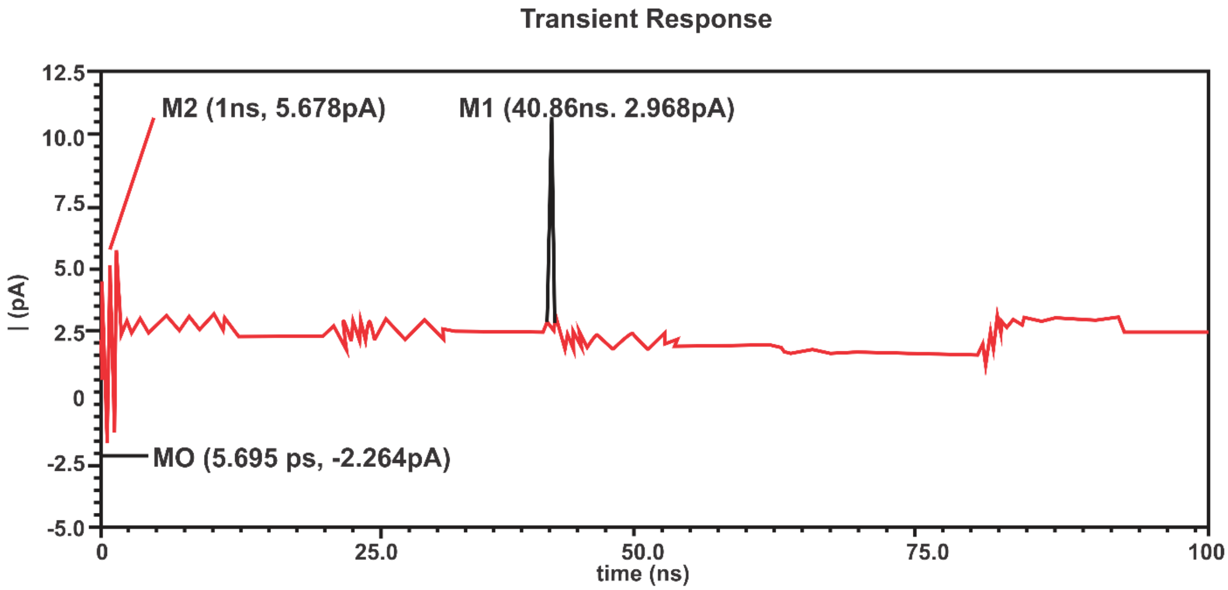


Figure 7.4 Leakage Current Waveform of Full Adder using Stacking Power Gating

7.3 Leakage Control Using Low Power Technique

Several experts in the field have proposed that a 1-bit Full Adder be built utilizing the Power Gating technique.

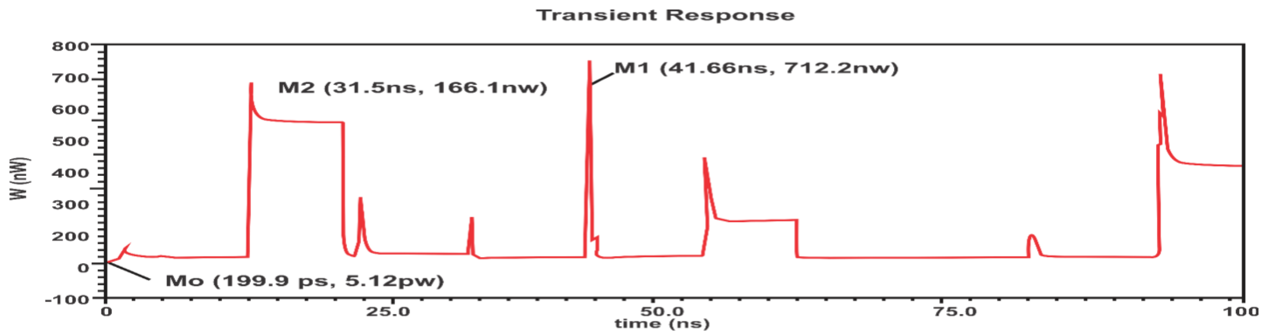


Figure 7.5 Active power in 10 T Full Adder by using Stack Power Gating Technique

The practicality of this method in complete adder design is shown by simulation results, which indicate a considerable reduction in power dissipation by 60-70% as compared to CMOS technology, with a supply voltage of 0.7V. Power Gating Adders have a somewhat larger physical footprint compared to CMOS adders, but, significant strides have been made in reducing power consumption to unprecedented levels. The CANDENCE VIRTUOSO Tool is used for the evaluation of simulation effectiveness. By using the Power Gating Method, we successfully reproduced the leakage current (271.6nA) and leakage power (121.21nW) characteristics of a 10-transistor full adder cell. The leakage current and power of a 10T complete adder have been determined to be 7.59pA and 4.54nW, respectively.

7.4 Delay and PDP of Full Adder Cell

The latency of a cell is determined by the input transition and output load. The delay of a complete adder cell in this section may be determined via the use of Power gating and Stacking power gating techniques. The delay values for the Sum and Carry signals in a Complementary Metal-Oxide-Semiconductor (CMOS) 1-bit complete adder are measured to be 10.44 picoseconds (ps) and 7.45 ps, respectively. The use of the stacking power gating technique on a 10-transistor CMOS full adder cell resulted in an observed augmentation in the transistor count, thereby leading to increased delays for both the sum and carry operations, namely 17.12 ps and 12.52 ps, respectively.

7.5 Results in Various Low Power Techniques and Parameters (10T)

The results mentioned earlier indicate that the leakage power in MTCMOS technology has the potential to be diminished to around 30% of the leakage current. Similarly, in Tri mode MTCMOS technology, the leakage power may be decreased to approximately 29.9% of the leakage current. [262].

Device	Leakage Current	Leakage Power
SVL	5.97E-07	4.18E-07
TRI Mode MTCMOS	4.50E-07	3.15E-07

MTCMOS	5.93E-07	4.15E-07

Table 7.1Parameters for 10T JLDGHFA Leakage in a Number of Low-Power Schemes

When a CMOS transistor is subjected to static electricity, it loses energy in the form of heat, which increases the leakage current and the threshold voltage. Although reducing static power consumption is desirable, minimizing transistor size is still important since static power might be an obstacle when it comes to power dissipation.

Power dissipation may be drastically lowered by using MTCMOS, Tri Mode MTCMOS, or SVL technology[263]. It is obtained as:

$$P(W) = C_L {V_{DD}}^2 f + V_{DD} I_{max} \left(\frac{t_r + t_f}{2}\right) f + V_{DD} I_{leak}$$

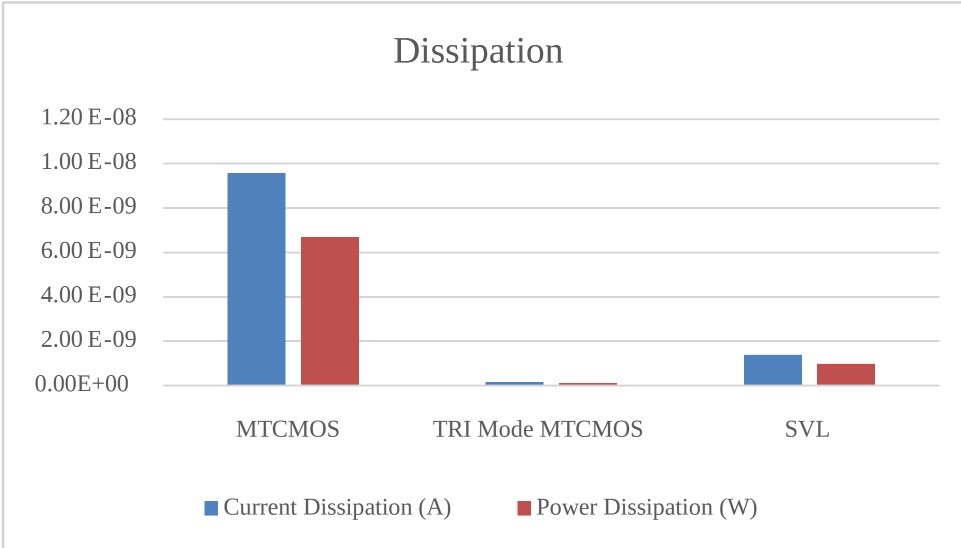
where Current Dissipation is gained as:

$$I(A) = \frac{P(W)}{V_{int}}$$

Device	Current Dissipation (A)	Power Dissipation (W)
SVL	1.39E-09	9.73E-10
TRI Mode MTCMOS	1.38E-10	9.69E-11
MTCMOS	9.58E-09	6.71E-09

Table 7.2 Dissipation Parameters of 10T JLDGHFA Utilizing a Wide Range of Du Methods

The findings demonstrate a 29.9% decrease in power dissipation in MTCMOS as compared to the current state of the art. Using the Tri mode MTCMOS method, power dissipation is reduced to only 29.78% of the current dissipation. The SVL method reduces power loss to 30% of the standard level. Moreover, under normal circumstances, Tri mode MTCMOS technology is far more effective than MTCMOS and SVL technology. [264].



Graph 7.1Compared to the Present State, power dissipation in MTCMOS

7.6 Full Adder Structure and NBTI HCI Mechanisms Results and Discussion (8T)

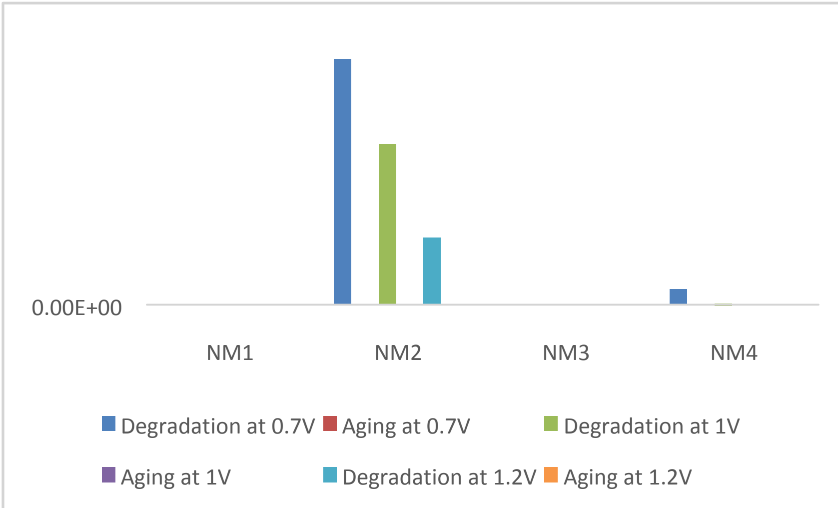
Reliability study of the NBTI and HCI in 45nm CMOS technology is used to propose a complete adder circuit with 8 digits of precision. The transistor has to be reliably operated at voltages of 0.7V, 1V, and 1.2V. To illustrate the effects of HCI deterioration and ageing over the course of a year, the table below compares individual NMOS transistors in a whole adder.

Transistor	**Degradation**	**Aging**	**Degradation**	**Aging**	**Degradation**	**Aging**
	1 Year		**1 Year**		**1 Year**	
	0.7 V		**1 V**		**1.2 V**	
NM1	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NM2	7.32E-28	2.38E-70	4.79E-28	8.02E-71	2.00E-28	8.50E-72
NM3	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
NM4	4.47E-29	1.82E-73	2.66E-30	1.31E-76	0.00E+00	0.00E+00

Table 7.3 Comparison of HCI Effect on NMOS at 0.7v, 1v 1.2v in a Year

The deterioration of NMOS transistors is shown graphically in Figure 7.4. NM2 is affected more severely than NM1, NM3, and NM4 with its degradation three times as great at 0.7V as it is at

1.2V, and it is twice as great at 1V. It has been noted that the NM4 has deteriorated only a little bit from its minimal state. The degree of deterioration of NM1 and NM3 is zero.



Graph.7.2 NMOS under HCI Degradation and Aging

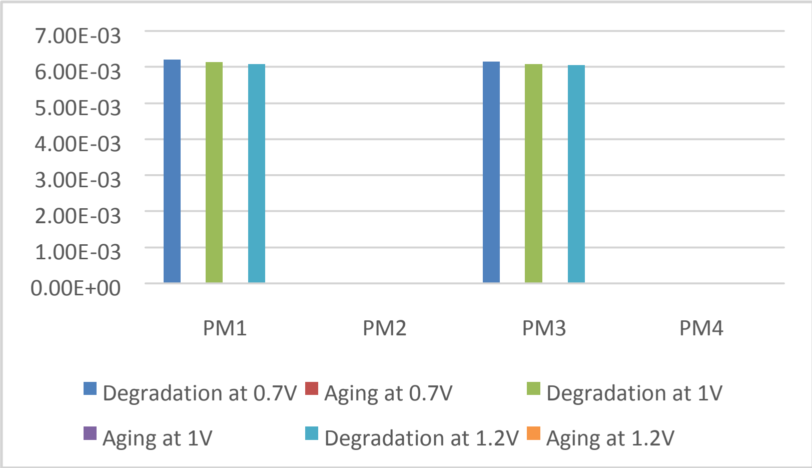
The transistor has to be reliably operated at voltages of 0.7V, 1V, and 1.2V. Where we're sitting: at the table. 7.4 Displays a comparison of PMOS transistors in a complete adder as they degrade and age over the course of a year due to NBTI deterioration and ageing.

Transistor	Degradation	Aging	Degradation	Aging	Degradation	Aging
	1 Year		1 Year		1 Year	
	0.7 V		1 V		1.2 V	
PM1	6.21E-03	1.23E-11	6.14E-03	1.16E-11	6.10E-03	1.12E-11
PM2	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
PM3	6.16E-03	1.18E-11	6.09E-03	1.11E-11	6.06E-03	1.08E-11
PM4	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00

Table 7.4Shows the Comparison of NBTI Effect on PMOS at 0.7v, 1v 1.2v in a duration of a Year.

The deterioration of PMOS transistors is shown graphically in graph 7.3, with PM1 and PM3 being hit much harder than PM2 and PM4. Both PM1 and PM3 exhibit identical deterioration at

1V (0.7V) and 1.2V (1.2V), respectively. Similarities between PM3 and PM1 may be seen in its degradation but the degradation level of PM2 and PM4 is zero.



Graph.7.3PMOS under NBTI Degradation and Aging

7.7Evaluation of a Low-Power Multi-Bit Full Adder Implemented with the m-GDI Technique

The modified Gate Diffusion Input (m-GDI) technique is used for the implementation of a complete adder circuit. The suggested configuration exhibits the capacity to mitigate power losses inside the system, while also adhering to the imposed power limitation. Due to the reduced number of transistors, more space is created on the integrated circuit. The present work involves the simulation of a 1-bit m-GDI FA using Cadence software in order to ensure the accurate functioning of the adder circuit. The static complementary metal-oxide-semiconductor (CMOS), transmission gate (TG), and hybrid designs, with respective bit widths of 1, 2, and 8, are also subjected to simulation. Initially, a transient analysis is conducted on the aforementioned data bits using a time frame of 100 nanoseconds. The input bits are subjected to a pulse voltage with a range of 1V to 0V for the purpose of processing. The necessary modifications to the pulse width may be accomplished by using a consistent pulse voltage and applying distinct pulse voltages to each input bits. It is important to conduct a comparison between the input signal and the simulation graph in order to analyze the Sum and C_{out} output pins. The functioning of the complete adder is verified by comparing the output levels of the simulated graph with the truth table that is provided. The figures presented in this study illustrate the outcomes obtained from simulations conducted on several full adder designs, including the 1-bit static CMOS, TG, Hybrid, and suggested m-GDI FA. These results are displayed in Figures 7.6, 7.7, 7.8, and 7.9.

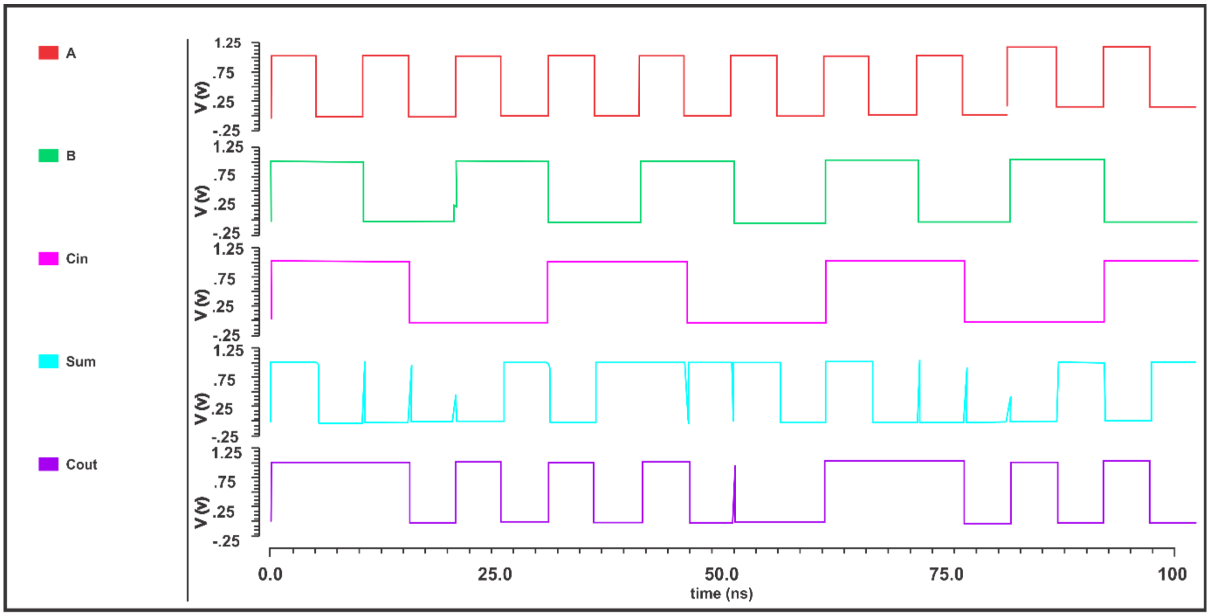


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Figure 7.6 One-Bit Static CMOS Full Adder Transient Response

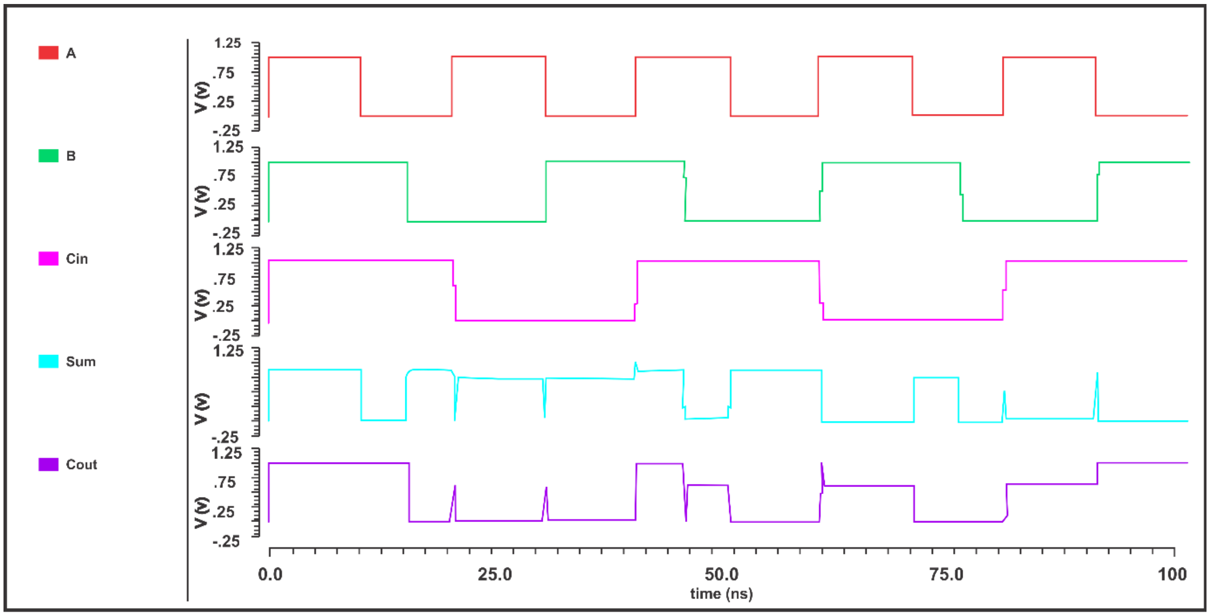

Figure 7.7 One Bit Full Adder Circuit Transient Response

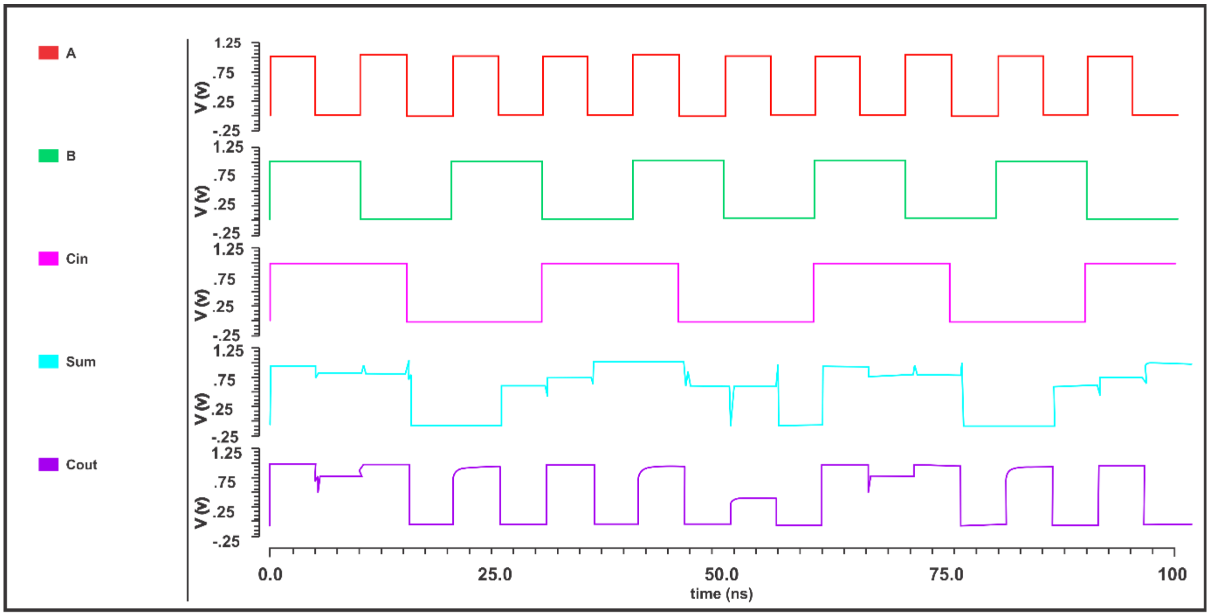

Figure 7.8 One-Bit Hybrid Full Adder Transient Response

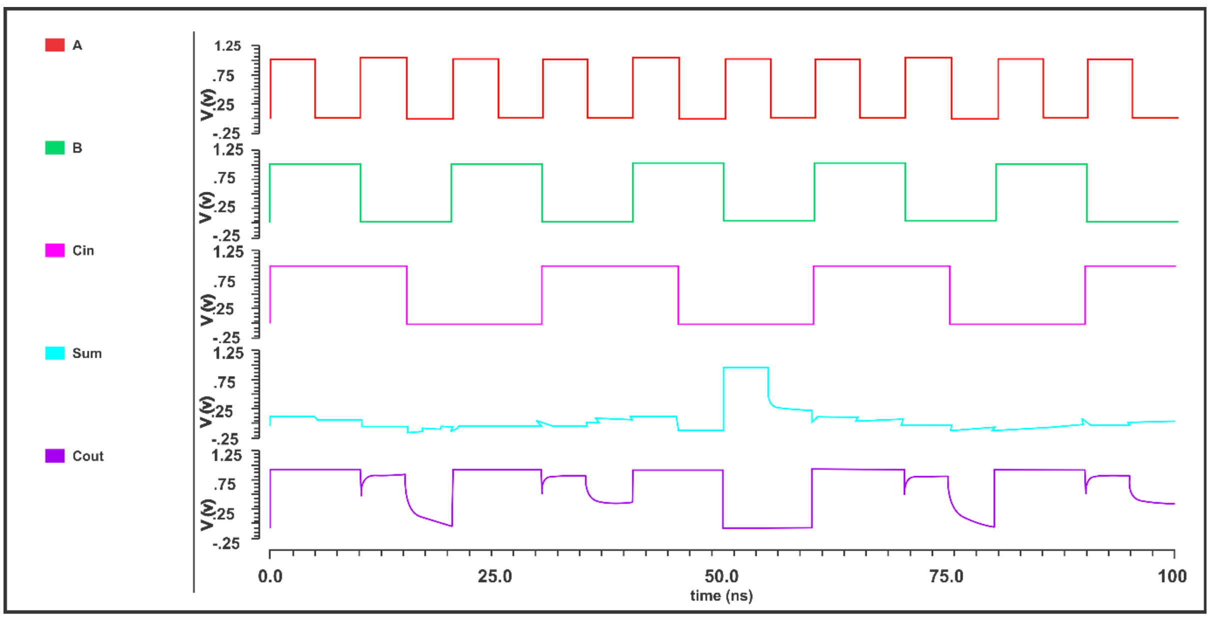

Figure 7.9The Proposed GDI Full Adder Transient Response

7.8 Comparing Multi-Bit Full Adder Using Low Power m-GDI Technique

The primary objective of this part is doing a comprehensive analysis of the differences and parallels among the Static CMOS, TG, hybrid, and projected m-GDI FA. The methodology used in this study is based on the premise that some variables remain consistent throughout the process of comparison. The operating duration and circumstances for all three buildings are limited in duration. In the DC analysis conducted for the comparison research, the Vdd voltages of all the structures are maintained at 1V. The simulations conducted by CAEDENCE VIRTUOSO consistently use the 90nm node of the GDPK library. If there is no variation in the levels of rise and decrease to compare, the research may be simplified. The results of the tests conducted on the circuits and designs discussed earlier are shown in Tables 7.5, 7.6, and 7.7.

Parameter	Static CMOS	TG	Hybrid	Proposed GDI
Transistors count	28	20	12	8
Average power	47.31E-6	28.71E-6	30.01E-6	17.65E-6
Carry delay	57.60E-12	38.32E-12	50.048E-12	51.19E-12
Sum delay	50.51E-12	46.02E-12	41.92E-12	50.81E-12
PDP	2.38	1.32	1.25	0.896

Table 7.5 The differences between the aforementioned 1-bit FA structures

Parameter	Static CMOS	TG	Hybrid
Transistors count	28*4	20*4	12*4
Average power	89.49E-6	66.87E-6	60.4E-6
Carry delay	84.33E-12	80.5E-12	68.1E-12
Sum delay	95.05E-12	65.69E-12	51.38E-12
PDP	8.50	4.39	3.10

Table 7.6 The differences between the previously mentioned 4-bit FA structures

	Static CMOS	TG	Hybrid
Transistors count	28*8	20*8	12*8
Average power	127.26E-6	116.0E-6	96.95E-6
Carry delay	184.3E-12	159.4E-12	127.6E-12
Sum delay	194.6E-12	161.0E-12	128.2E-12
PDP	2.47	1.86	1.24

Table 7.7 The differences between the previously mentioned 8-bit FA structures

7.9Discussion

The simulations discussed above provide a simple means of verifying functioning. This paper investigates the underlying reasoning behind the concepts of sum and carry. Ultimately, a comparative chart and comprehensive analysis of several bits of data demonstrate the relative merits and shortcomings of different designs when evaluated in relation to each other. The process of analysis is significantly streamlined when limited to the use of either 1, 4, or 8 bits. The proposed 1-bit GDI full adder is being evaluated in comparison to existing full adder designs. A minimum of eight transistors are used, resulting in a significant reduction in size. A thorough analysis of the simulations should unveil a trade-off in the amplitude of the output voltage. The compromise of the 0.9 pJ voltage swing is made in order to achieve energy savings. The numerical value associated with this particular figure is lower in comparison to the values seen in other designs for complete adder circuits. Furthermore, it is worth noting that the mean transient power associated with this methodology is much reduced, measuring around 16.65 µW in absolute magnitude. The carry and total delays are measured to be 50.81 picoseconds and 51.19 picoseconds, respectively. Hence, it becomes imperative to make a decision on the optimal configuration for a complete adder circuit with the objective of reducing resource use, including power consumption and silicon area.

CHAPTER 8
CONCLUSION AND FUTURE WORK

8.1 Conclusion

This thesis advances our knowledge of the behavior of single-bit whole adder cells, which are crucial for their high performance, low leakage current, fast speed, and low power consumption. In light of this, whole adder cells with 10 transistors have been simulated using 45 nm CMOS technology and implemented in the Cadence tool suite to determine the cells' minimal power dissipation performance. Several methods have been shown in this study, which in turn lowers leakage power and current and enhances the functionality of the Full Adder circuit—a crucial part of any digital circuit.

Nowadays, our need for durable, fast, and low-power gadgets is fueled by the need for portable electronics. Thus, in this work, TG logic is combined with the two logic types, CMOS and TG-based FA, and a low-power hybrid FA has been created utilizing XNOR. The Cadence Virtuoso with GPDK at 45 nm is used for the simulation, and the outcome is a 10T hybrid Full Adder that has improved power and delay performance. In comparison to a CMOS-based full adder, it delays 10% and decreases leakage power by up to 40%. MTCMOS has a little delay increase but a 35% reduction in leakage power. We are also using the tri-mode MTCMOS, SVL approach to reduce the delay while achieving 37% and 43% reductions in leakage power and current, respectively, in full adder cells. The performance of the full adder cell was improved by implementing three leakage mitigation strategies. Following circuit modeling, a design is chosen for low-power application scalability and usage. The chosen design is changed, and the variables are scaled, to further enhance the performance of the whole adder cell. It is discovered that the leakage current and leakage power of the circuit decrease with voltage scaling and power supply reduction. When transistor sizes are down to 45 nm, lifespan becomes a significant concern for low-power CMOS devices. This study investigates the performance of the HCI and NBTI reliability characteristics over a one-year period in various operating circumstances. The simulated results demonstrate that at low voltages of 0.7V and excessively so at high voltages of 1.2V, the NMOS is very vulnerable to degradation and aging owing to HCI, producing NM2. The aging and degradation of PMOS have a significant effect on PM1 and PM2 across the board, as seen by the voltage measurements. However, the built-in MOS transistors of the 8T complete adder are prone to damage. Adopting precise remedial steps to improve performance and stability is necessary to stop future degradation.

This study has led to a comprehensive knowledge of the power and time behavior of full adder cells as well as the advantages of 45 nm CMOS technology in the field of full adder cells. The study also revealed which full adder cell designs work best in terms of power and current. In a later part, the proposed 1-bit GDI FA is compared to various Full Adder designs. Its size is considerably decreased using as few as eight transistors. Upon further inspection of the simulation data, we can observe that a tradeoff in output voltage swing is made in order to preserve the lowest PDP of 0.9 pJ. Compared to other full adder circuit designs, this value is lower. Additionally, the average transient power needed for this approach is far lower, at about 17.65μW. The sum and carry outputs are behind by 50.81 ps and 51.19 ps, respectively. Consequently, the circuit design for a full adder that minimizes die area and power consumption is the optimal.

8.2 Future Scope

The process developed and used to identify the best high-speed and low-power full-adder cells produced findings that were comparatively good. For even better outcomes, though, the upcoming researchers must further scale down the device. This thesis examines many circuit-level leakage reduction strategies that considerably decreased leakage current and power for a single-bit full adder cell using 45 nm technology. Given the tremendous importance of leakage in 45 nm technology, this study ought to be expanded to 32 nm, 22 nm, and beyond. In addition to the approaches used here, a number of other leakage reduction strategies must be used in subsequent work to enhance performance. Although unfinished, this work offers a route to follow in order to investigate novel approaches.

List of Publications

1. P. Sharma and S.Sharma, “Design and Analysis of Power Efficient Hybrid Full Adder Using Static CMOS and Transmission Gates” International Journal of Nanotechnology, Inderscience Pub. ISSN 1475-7435,April 2022. (Impact Factor=0.346).
DOI: https://www.inderscience.com/info/ingeneral/forthcoming.php?jcode=ijnt

2. P. Sharma and S.Sharma,“Life Time of a MOS Degradation under Reliability Techniques (NBTI, HCI) in Proposed 8T Full Adder” International Journal of Nanotechnology, Inderscience Pub. ISSN 1475-7435,Nov. 2022. (Impact Factor=0.346).
DOI: https://www.inderscience.com/info/ingeneral/forthcoming.php?jcode=ijnt

3. P. Sharma and S.Sharma, “Evaluation of Ultra-Low Power Techniques to 10T Junction Less Double Gate Hybrid Full Adder (10TJLDGHFA),” IEEE VLSI Circuits and System Letter, vol. 4, No. 4, PP. 01-05, Nov.2018. (IEEE System Letter).
DOI:https://ieeecs-media.computer.org/media/technical-activities/tcvlsi/newsletters/2018/VLSI_Circuits_and_Systems_Vol-4_Issue-4_2018-Nov.pdf

4. P.Sharma,J.Sutradhar,S.Akashe and S.Sharma, “Design of Multi-Bit Full Adder Using Low Power m-GDI Technique” IEEE World Conference on Applied Intelligence and Computing (AIC 2023), Publisher IEEEPage 834 – 838,29-30 July 2023.
DOI: https://ieeexplore.ieee.org/xpl/conhome/10263804/proceeding

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