

An Investigation of Flipped Voltage Follower Cells for Analog VLSI Circuits

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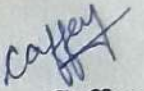
February, 2022

CERTIFICATE

I, Caffey, hereby certify that the research work presented in the thesis entitled "**An Investigation of Flipped Voltage Follower Cells for Analog VLSI Circuits**" being submitted by me with **Registration No. 901706029** to the Department of Electronics and Communication Engineering, Thapar Institute of Engineering and Technology, Patiala, India in the fulfilment of the requirements for the award of the degree of "**Doctor of Philosophy**". It is an authentic record of bonafide research work carried out under the guidance and supervision of **Asst. Prof. (Dr). Rishikesh Pandey, ECED, TIET, Patiala**.

The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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CAFFEY

*Dedicated to my
Parents*

ABSTRACT

Nowadays, the use of battery-operated portable electronic devices has been rapidly increasing. The portability requirement demands low power dissipation to increase the battery's life and minimize the size of the battery. Low power becomes the major design constraint in the designing of battery-operated devices. These devices consist of analog and digital circuits integrated on a chip. The density of integrated circuits has been continuously increasing with the scaling down of complementary metal-oxide-semiconductor (CMOS) technology. To reduce the power dissipation and maintain the reliability of the integrated circuits, the supply voltage needs to be scaled down. In integrated circuits, the small-channel length and low supply voltage operation enhance the performance of the digital circuits in terms of speed, power, and integration. However, short channel effects and low supply voltage degrade the performance of analog circuits in terms of non-linearity in the output, which becomes the bottleneck of the system. This has forced the analog designers to switch from conventional analog circuit architectures to new low-voltage/low-power transistor implementation techniques.

In the thesis, analog cells called flipped voltage follower (FVF) cells have been investigated to regain circuit performance in a low voltage environment. However, the conventional FVF cell shows class-A behaviour such that either the quiescent bias current is high or the settling time is poor, thus showing an asymmetrical slew rate. The output resistance of the class-A FVF cell is also not low enough. Class-AB biasing employed in the FVF cell can reduce its power consumption as the quiescent bias current can be kept at low value and symmetrical slew rate can be achieved with low output resistance. The thesis proposes four class-AB FVF cells namely class-AB FVF cell-I, class-AB FVF cell-II, class-AB FVF cell-III, and class-AB FVF cell-IV, which offer several improved electrical features such as current sourcing/sinking capability, output resistance, slew rate, input/output voltage swing, etc. as compared to existing FVF cells available in the literature. The analyses of proposed class-AB FVF cells have been performed using small-signal modelling. The proposed class-AB FVF cell-I uses the replica-biased scheme to eliminate the DC level shift between input and output voltages where the input voltage is applied at the bulk terminal. The class-AB FVF cell-I can provide approximately unity voltage gain with high current driving capability but it shows limited bandwidth because the input voltage is applied at the bulk terminal. In the proposed class-AB FVF cells (II and III), the input voltage is applied at the gate terminal and bulk driven transistor is used as an adaptable current source to enhance the current sourcing capability. The current sinking capability has been increased using an extra transistor and

quasi-floating gate technique in class-AB FVF cells II and III, respectively. The class-AB FVF cell-IV uses the folding transistor to provide an alternate path for sourcing currents while reducing the output resistance. A level shifter has also been employed to increase the input/output voltage swing. The class-AB FVF cell-IV shows significantly better results in terms of various performance parameters than the other three proposed class-AB FVF cells and FVF cells available in the literature.

To demonstrate the working of proposed class-AB FVF cells, these FVF cells have been used as the building blocks in designing a basic analog VLSI circuit, i.e. current mirror. The current mirrors I, II, III, and IV have been proposed using class-AB FVF cells I, II, III, and IV, respectively at the input stages and thus offer low input resistance due to class-AB FVF cells. The proposed current mirrors offer various improved electrical features such as input resistance, output resistance, current mirroring range, error, minimum input voltage, and minimum output voltage.

All the proposed circuits have been designed using BSIM3V3 180 nm CMOS technology and simulated using spectre in the Cadence Virtuoso Analog Design Environment. The physical layouts of the proposed circuits have been designed using Cadence Virtuoso Layout XL editor in 180 nm CMOS technology.

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LIST OF ABBREVIATIONS

BDSBCM	Bulk-Driven Self-Biased Cascode Mirror
CCII	Second-Generation Current Conveyor
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
DC	Direct Current
DFVF	FVF Differential Structure
DIBL	Drain Induced Barrier Lowering
DTMOS	Dynamic Threshold MOSFET
FGMOS	Floating-Gate MOSFET
FOM	Figure of Merit
FVF	Flipped Voltage Follower
FVFCS	FVF Current Sensor
FVFDP	FVF Pseudo-Differential pair
GBW	Gain-bandwidth product
INSD	Input-referred Noise Spectral Density
JFET	Junction Field-Effect Transistor
KCL	Kirchoff's Current Law
LP	Low-Power
LV	Low-Voltage
MOSFET	Metal Oxide Semiconductor Field-Effect Transistors
NMOS	N-type Metal-Oxide-Semiconductor
OTA	Operational Transconductance Amplifier
PMOS	P-type Metal-Oxide-Semiconductor
SR	Slew Rate
THD	Total Harmonic Distortion
VLSI	Very Large-Scale Integration

CHAPTER-1

INTRODUCTION

1.1 Introduction

The invention of transistors in the late 1940s has begun the era of low power microelectronics [1]. Over the past few decades, microelectronics has become an important part of modern life. One cannot imagine a world without the low power microelectronics as it has been used mostly in various battery-operated equipments such as hearing aids, wristwatches, cell phones, implantable cardiac pacemakers, calculators, camcorders, hand-held multimedia terminals, etc. Nowadays, in the market of portable electronic devices, consumers look for a good battery life offered by the device. With the increase in demand for smaller size and longer battery life of portable applications, low power dissipation has become one of the most critical factors in complementary metal-oxide-semiconductor (CMOS) very large-scale integrated (VLSI) circuits and systems [2]. Also, to enhance the performance and integration of the portable applications, single-chip implementation of both analog and digital circuits by decreasing the feature size in mixed-signal integrated circuits is recommended. As a result, the magnitude of power per unit area increases which creates the problem of heat removal. The common practice to decrease the power dissipation of any circuit is to scale down the power supply voltage. However, single-chip systems also face a critical constraint due to voltage scaling in sub-micron CMOS processes. Because in digital circuit design, static and dynamic powers are directly proportional to supply voltage, so low power consumption can be achieved by low supply voltage but this is not always in the case for analog circuit design. In analog circuit design, there are other problems associated such as the voltage swing and bandwidth getting decreased at the low supply voltage [3]. Also, the delay in the circuit increases when the supply voltage is scaled down to reduce power. The performance loss (low voltage swings, decreased bandwidth, increased delay, etc.) can be compensated if the threshold voltage is scaled-down along with the supply voltage and device size. The scaling of the threshold voltage is also restricted as the components of the threshold voltage due to the bulk charge in the channel and built-in-junction potential do not scale as preferred. There is a limitation in scaling down the threshold voltage because the devices suffer from short channel effects, parasitic effects, and increased leakage currents [4]. Therefore, threshold voltage scaling is tightly constrained. The scaling improves the performance of digital circuits but it marginally benefits the analog circuits [5]. Although, in a mixed-signal circuit design there are different approaches to design analog circuits at low supply voltage. The first

approach is to use the lower direct current (DC) supply voltage and then multiply it to larger values that need special interface circuits. This is not a suitable solution because it increases the complexity. In the second approach, the existing CMOS technologies can be changed to accommodate the low-voltage analog circuits, which is an expensive process. The third approach is to apply transistor implementation techniques in the existing CMOS technology to obtain low voltage operation without the need for costly process development [6].

1.2 Background

The recent trends in the design of mixed-signal circuits aroused a need to switch from conventional analog circuit architectures to new low-voltage/low-power (LV/LP) transistor implementation techniques that can be used without the need for costly process development. The various LV/LP transistor implementation design techniques for low supply voltage operation of analog circuits are bulk-driven metal oxide semiconductor field-effect transistors (MOSFETs) [7-8], level shifter technique [8], sub-threshold MOSFETs [7-8], self-cascode MOSFETs [7-8], floating-gate MOSFETs (FGMOS) [7-10] and flipped voltage follower [10]. The basic structure and operation of different LV/LP design techniques are discussed as follows:

1.2.1 Bulk-driven MOSFETs

When MOSFETs perform any signal processing task, there should be biasing current flowing through its drain. In the conventional gate-driven MOSFETs, the drain current flows when applied gate voltage overcomes the threshold voltage. The bulk-driven MOSFETs biased in the saturation region provide a continuous drain current and avoid the threshold voltage requirement in the signal path. This is because the fixed bias voltage (V_b) is applied at the gate terminal which is sufficient to form the inversion layer between source and drain terminals while the input signal is given at the bulk terminal in bulk-driven MOSFET as shown in Figure 1.1. This either reduces or removes the threshold voltage requirement. The behaviour of bulk-driven MOSFET is like a junction field-effect transistor (JFET), so it can work under negative, zero, or slightly positive bias voltages due to the availability of conducting channel [11]. The width of the conducting channel changes by varying the voltage at the bulk terminal, so the drain current also changes due to the body effect of MOSFET. The various low-voltage analog circuits using the bulk-driven technique have also been reported [12].

However, the limitation of bulk-driven MOSFET is that it needs to be fabricated in different wells to have an isolated bulk terminal.

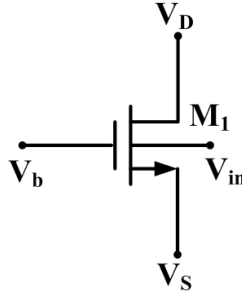


Figure 1.1 Bulk-driven MOSFET

The other shortcoming of bulk-driven MOSFET is that the transconductance of bulk-driven MOSFET is lesser than the gate-driven MOSFET. This generates larger input-referred noise and a lesser gain-bandwidth product than the gate-driven MOSFET when used for low-voltage applications. Also, the bulk-driven MOSFETs are process dependent i.e. N-channel bulk-driven MOSFETs can be implemented only in the P-well process and P-channel bulk-driven MOSFETs can be implemented only in the N-well process. This limits the use of bulk-driven MOSFETs in low-voltage applications.

1.2.2 Level shifter technique

Another technique to reduce the required supply voltage for operation is a level shifter. DC level shifting technique is used to reduce the effective threshold voltage of MOSFETs. In this approach, MOSFETs operate in sub-threshold or saturation regions [13]. To show the usefulness of the level shifter, conventional current mirror and current mirror using level shifter are shown in Figure 1.2 (a) and (b), respectively. The drain current flowing in Figure 1.2 (a) is $I_D = \frac{1}{2} \mu_n C_{ox} W/L (V_{GS1} - V_{th})^2$ where μ_n is the mobility of electrons, C_{ox} is the gate-to-oxide capacitance per unit area, W/L is the aspect ratio, V_{th} is the threshold voltage. In this case, the minimum input voltage required for the operation of the current mirror is V_{th} . The conventional current mirror cannot operate at a voltage less than V_{th} . But, the required input voltage decreases by using a level shifter (transistor M_3) between the drain and gate terminals of the current mirror. Now, the minimum input voltage required is $V_{GS1} - V_{SG3}$. The input and output resistances remain the same in both the mirrors whereas the level shifter decreases the minimum input voltage. The advantage of a level shifter circuit is enhanced bandwidth at low voltage. The level shifter circuits provide rail-to-rail operation, both at input and output ends.

However, the number of MOSFETs increases by using a level shifter which increases the power dissipation and silicon area. Another drawback is that the offset current starts flowing through

the output transistor even when the input current is zero. So, this is more problematic and degrades the performance of the circuit when the input current is in the order of offset current.

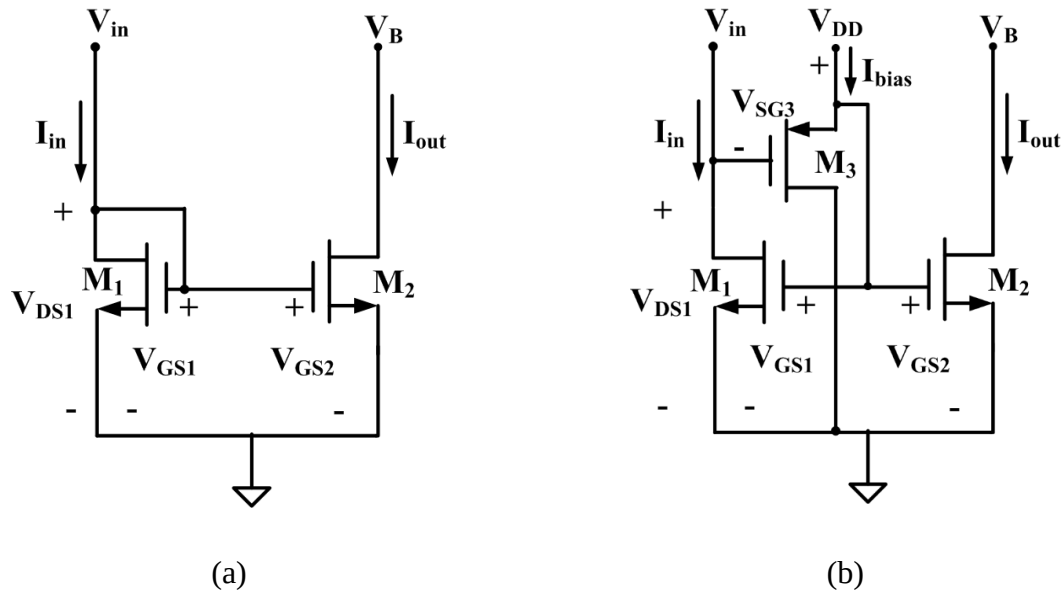


Figure 1.2 (a) Conventional current mirror (b) Current mirror using level shifter

1.2.3 Sub-threshold MOSFETs

In recent years, the sub-threshold region has gained prominence due to the use of low-voltage and low-power circuits in human implantable biomedical instruments. Generally, we assume the device turns off abruptly when gate-to-source voltage is less than the threshold voltage but actually in MOSFETs, when gate-to-source voltage is less than the threshold voltage, then drain current flows due to the diffusion of minority charge carriers. This is called the sub-threshold or weak inversion region. The drain current exhibits an exponential relationship with gate-to-source voltage in the sub-threshold region. The sub-threshold MOSFETs have low saturation voltages i.e. 100 mV which gives large voltage swings at low supply voltages. Due to the operation in low supply voltage, the circuits designed using sub-threshold MOSFETs consume less power. The input-referred noise of MOSFETs operating in the sub-threshold region is also lesser than the saturation region MOSFETs.

But the frequency response of devices in the sub-threshold region is poor. Also, the leakage currents flowing due to reverse-biased drain/source substrate currents become non-negligible as compared to sub-threshold currents. The devices operating in the sub-threshold region are poorly matched which limits their use in current precision circuits. The linearity is also degraded in sub-threshold MOSFETs which makes the design of low-voltage circuits complicated.

1.2.4 Self-cascode MOSFETs

The output impedance of MOSFET decreases with the scaling down of technology due to channel length modulation. In addition to channel length modulation, drain induced barrier lowering (DIBL) causes the current to increase with drain bias, lowering the output impedance of MOSFET. The gain is also dependent on the output impedance so short-channel MOSFETs cannot provide high gain. To achieve high gain and high output impedance, the cascode structures can be used where MOSFETs are stacked one above the other in a common-source/common-gate configuration. However, it provides high gain but the output signal swing gets reduced by using the conventional cascode structure. The alternative technique is to use self-cascode structure where both the MOSFETs are connected with the same gate voltage.

The self-cascode structure shown in Figure 1.3 consists of two MOSFETs where transistor M_2 operates in the saturation region and transistor M_1 operates in the ohmic region. The self-cascode structure can be considered as a single composite transistor M_s operating in the saturation region. The aspect ratio of transistor M_2 is larger than transistor M_1 and transistor M_1 acts as a resistor. The composite transistor M_s shows a large effective channel length and output impedance. The drain-to-source voltage of transistor M_1 is small so the self-cascode structure can be used in the low voltage operation. The conventional cascode structure operates at a much higher voltage than self-cascode structure. So, the self-cascode is advantageous as it provides high output impedance similar to conventional cascode while operating at lesser supply voltage.

However, the output impedance of the self-cascode structure can be increased by choosing the threshold voltage of transistor M_1 greater than that of the threshold voltage of transistor M_2 . But, this is possible using multiple threshold technology, which is very expensive.

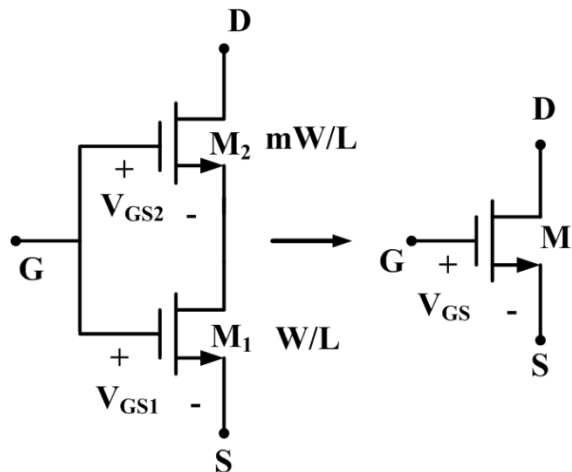


Figure 1.3 Self-cascode MOSFET

1.2.5 Floating-gate MOSFETs

Recently, in the number of analog applications, the floating-gate MOSFET (FGMOS) shown in Figure 1.4 (a) has been used. It has also been used in digital circuits and is compatible with the standard CMOS technology. The FGMOS devices allow tuning of the threshold voltage due to which it can be used in the design of low-voltage analog circuits and reduces the voltage headroom [14]. The polysilicon gate of conventional MOSFET is floating in the FGMOS device as it is surrounded by an insulating oxide layer on all sides. The electrical charge resides at the floating gate and discharges very slowly due to the insulation property of SiO_2 . The polysilicon gate is called floating because there is no DC path to the ground. The inputs are applied through the second polysilicon gate which is present over the floating gate. In the two-input FGMOS transistor shown in Figure 1.4 (b), a bias voltage (V_b) is applied at one gate and input voltage (V_{in}) is applied at the second gate. The capacitances C_{G1} and C_{G2} are the capacitances between the floating gate and control gate. The bias voltage and the input capacitances adjust the threshold voltage to a lower value. Thus, the FGMOS transistors can be used in low-voltage analog circuit design.

The fabrication of floating-gate cannot be done using conventional technology which increases the cost. Also, the charge gets trapped during fabrication of floating-gate which leads to DC offsets. The FGMOS transistor shows low output impedance which limits its use in high gain circuits.

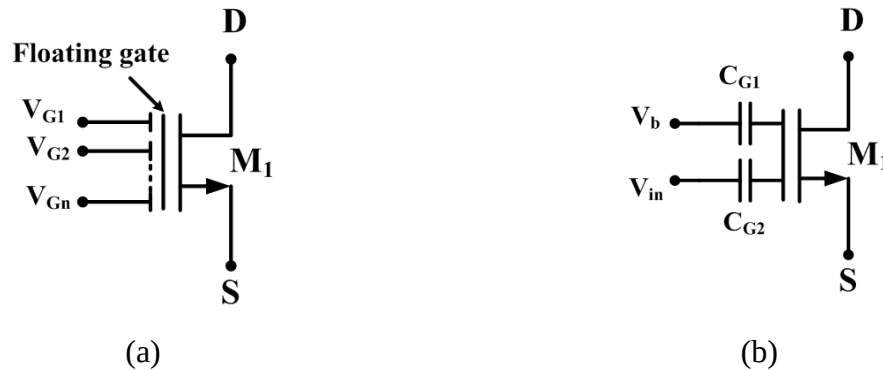


Figure 1.4 (a) Multi-input FGMOS transistor (b) Two-input FGMOS transistor

1.2.6 Flipped voltage follower

Voltage follower which is used as a voltage buffer is a fundamental building block of analog VLSI circuits. It is characterized by high input impedance, low output impedance, high bandwidth, and approximately unity voltage gain. The voltage follower depicted in Figure 1.5 (a)

is used to avoid the loading effect as it transfers the voltage from the circuit having high output impedance to the circuit with low input impedance. In the voltage follower biased at the source terminal, the output voltage follows the input voltage with the dc level shift of gate-to-source voltage ($V_o = V_{in} - V_{GS}$). But, voltage follower suffers from certain drawbacks as the current through transistor M_1 depends on the output current, and output current is a function of input voltage. So, the gate-to-source voltage of the voltage follower does not remain constant, this results in less than unity voltage gain for resistive loads and capacitive loads at high frequencies. The output resistance inversely proportional to the transconductance of transistor M_1 is also not low enough. To decrease the output resistance, the transconductance of transistor M_1 needs to be increased which requires a large aspect ratio (W/L). Another problem is a limited current sinking capability which leads to an asymmetrical slew rate.

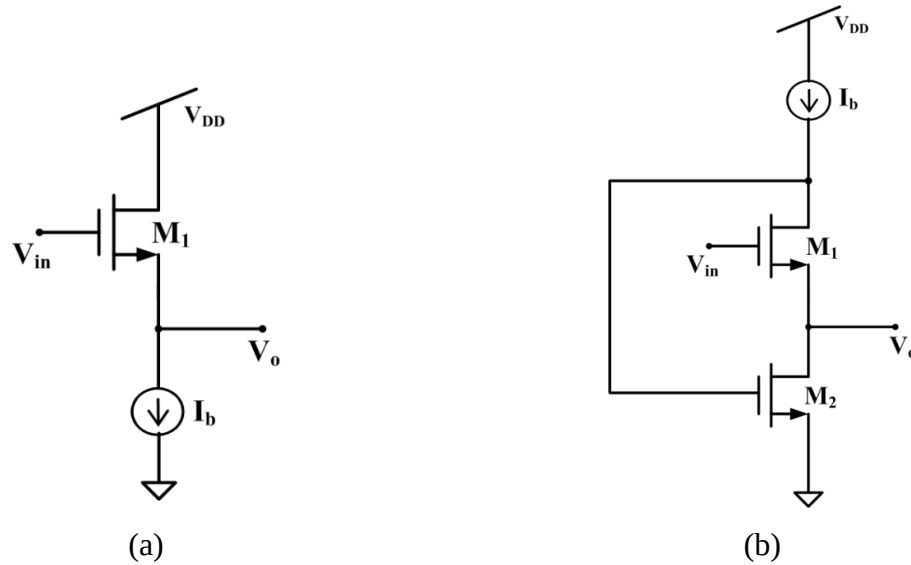


Figure 1.5 (a) Voltage follower (b) Flipped voltage follower

Flipped voltage follower (FVF) cell is an improved version of the voltage follower as shown in Figure 1.5 (b) [15-16]. Its name is based on the fact that it is biased at the drain terminal instead of the source terminal. It is a cascode amplifier where input is given at the gate terminal of transistor M_1 and output is taken from the source terminal of transistor M_1 . The transistor M_2 provides shunt feedback which decreases the output resistance of FVF cell. Unlike voltage follower, the gate-to-source voltage of transistor M_1 remains constant and voltage gain is approximately unity. This is because the current through transistor M_1 remains constant, independent of output current as the variations in output current are absorbed by current sensing transistor M_2 . The characteristics of FVF cell are low output impedance, high gain-bandwidth product, low supply voltage requirements, and low static power dissipation. However, the FVF

cell shows limited input/output voltage swing due to the gate-to-source voltage of transistor M_2 and the swing does not increase with the increase in supply voltage. FVF cell can sink a large amount of current, but the sourcing capability of FVF cell is limited by bias current I_b , thus it shows asymmetrical slew rate [17]. This is because the conventional FVF cell shows class-A behaviour, so the modification of conventional FVF cell which can provide class-AB behaviour with both large current sourcing and sinking capabilities is required. FVF cell has been used widely in various low-voltage analog circuits such as current mirrors, current conveyors, operational transconductance amplifiers, low-dropout regulators, multipliers, filters, comparators, etc.

1.3 Motivation

In real-time signal processing, analog signal processing is an essential element as all the naturally occurring signals are analog in nature. The advancement in CMOS technology and increased market demands have aroused a great interest in analog system design. The desire for portability in electronic devices needs the development of analog circuits to operate at low supply voltage levels in standard CMOS technology. The scaling down of process technology allows the circuits to operate at high frequency with less power consumption. But, in analog circuits, this fact is partially applied because it needs the additional current to maintain the same performance when the supply voltage is reduced. Moreover, in sub-micron technology, voltage doublers also cannot be used to enhance the performance of analog circuits due to the low breakdown voltage of transistors. Analog designers face difficulties and challenges as the threshold voltage and drain-to-source voltage of MOS transistors do not scale at the same rate as supply voltage which results in limited voltage headroom. The circuits which can only operate under high supply voltage with high performance lost their properties in low supply voltage. The analog circuit design for low voltage differs considerably from high supply voltage design. So, the alternative design techniques or circuit structures to suit the low voltage environment need to be investigated. The various LV/LP transistor implementation techniques for low supply voltage operation of analog circuits are bulk-driven technique, level shifter technique, sub-threshold MOSFETs, self-cascode MOSFETs, and FGMOS. Although these techniques work efficiently to reduce the supply voltage but offer certain limitations such as bulk-driven technique is a process dependent, level shifter technique increases the silicon area, sub-threshold MOSFETs degrades the linearity and frequency response, self-cascode MOSFETs require multiple threshold technology, and charge gets trapped during fabrication of floating-gate which leads to DC offsets

in FGMOS. FVF cell is another LV/LP technique that has been efficiently used in the design of various low-voltage and low-power analog integrated circuits. It offers advantages of low supply voltages, low power dissipation, and hence it increases device portability. Therefore, this technique can effectively replace the other LV/LP techniques which suffer from significant drawbacks, and also it provides a new area of research for the investigation.

1.4 Organization of thesis

The thesis is organized into five chapters as follows:

Chapter 1 introduces the requirement of LV/LP circuit design techniques. The various LV/LP transistor implementation techniques and the advantages of FVF cells over other LV/LP techniques have been discussed. This chapter addresses the motivation of the proposed work and the organization of the thesis.

Chapter 2 presents the research work that has been carried out on FVF cells and various analog circuits based on FVF cells in the literature. Based on the literature survey, the research gaps are identified. To overcome the limitations of the reported structures, the objectives of the work are proposed. Finally, the research methodology followed to fulfill the proposed objectives is discussed.

Chapter 3 proposes four different structures of FVF cell with class-AB behaviour and these structures offer different improved electrical features such as current sourcing/sinking capability, slew rate, input/output voltage swing, output resistance, etc. This chapter also includes the large-signal and small-signal analyses of proposed FVF cells. The physical layout and post-layout simulation results of the proposed FVF cells have been presented to validate their performance.

Chapter 4 presents current mirrors as applications of proposed class-AB FVF cells discussed in chapter 3. The small-signal analyses of these proposed current mirrors have been discussed to determine input resistance, output resistance, transfer function, and bandwidth. The physical layout and post-layout simulation results of the proposed current mirrors have been presented to demonstrate their performance in terms of input resistance, output resistance, current mirroring range, error, minimum input voltage, and minimum output voltage.

The conclusion of the research work has been given in Chapter 5. The future work which can be done in this domain has also been discussed.

CHAPTER-2

LITERATURE SURVEY

The name flipped voltage follower (FVF) was coined by J. Ramirez Angulo *et al.* [15] to describe a class of pre-existing and new low-voltage/low-power (LV/LP) analog circuits. The operation of FVF cell is based on class-A and class-AB topologies. To achieve high-performance FVF cells many modifications of the conventional FVF cell have been reported in the literature. Some of the authors have reported class-A FVF cells which are characterized by a non-symmetrical slew rate. The class-A FVF cells show either large current sourcing capability or current sinking capability. Several authors have also presented modified conventional FVF cell to show class-AB behaviour which provide both large current sourcing and sinking capabilities. FVF cells have also been used to design various analog VLSI circuits in the literature. The chapter discusses the research work which has been carried out on the FVF cell reported by various authors in recent years. A review based on the study of papers is as follows:

2.1 FVF cells based on class-A operation

The basic FVF cell used for designing LV/LP analog circuits has been reported by R. G. Carvajal *et al.* [16] which overcome the limitations of the conventional source follower. The different structures derived from FVF cells such as FVF current sensor, FVF differential structure, and FVF pseudo-differential pair have been reported. The variety of applications based on the suggested cell such as current mirrors, differential pairs, and operational transconductance amplifiers are also discussed.

A comparison of different structures of FVF cells is reported by J. Ramirez Angulo *et al.* [17]. The different FVF structures are FVF with level shifter, folded FVF (super source follower), FVF with floating gate, and cascoded FVF. However, the conventional FVF cell offers low output impedance, but it suffers from input/output voltage swing limitation. FVF with level shifter overcomes this limitation and increases the input/output voltage swing. But due to the addition of level shifter MOSFET, the power dissipation is increased and bandwidth is degraded. The other structure is folded FVF which also increases the voltage swing but shows the additional power dissipation. The other two FVF structures namely FVF with floating gate and cascoded FVF provide better characteristics in terms of voltage swing, slew rate, bandwidth, and power dissipation.

C.I. Lujan *et al.* presented FVF cell based on a cascode transistor with dynamic biasing and local feedback [18]. Due to the cascode transistor, the circuit overcomes the linearity problem of conventional FVF cell and the circuit shows better gain and linearity. The cascode transistor is biased with a floating battery connected between its gate and the input terminal of the circuit. The static and dynamic implementations of floating batteries using a resistor and quasi-floating gate technique are presented.

The wideband FVF cells using bandwidth extension techniques are reported by M. Gupta *et al.* [19] and U. Singh *et al.* [20]. The FVF cell reported in [19] uses resistance in the feedback path and it offers wider bandwidth and lower output impedance as compared to the conventional FVF cell. Another technique to enhance the bandwidth is discussed in [20] by using an inductor or by using a series combination of resistor and an inductor in the feedback path. It is observed that large bandwidth has been achieved using an inductive element in the feedback path of the conventional FVF cell.

U. Singh *et al.* [21] use the resistive compensation technique in the FVF cell based on level shifter [17] and FVF cell based on floating-gate technique [17]. In both circuits, the resistor has been used in the feedback path to enhance the bandwidth of the circuits without affecting the gain.

H. Dingchyan [22] presented a level shifted version of FVF cell to eliminate the limitation of input/output voltage swing. The level shifter transistor has been used in the feedback path of the FVF cell. But this level shifter transistor increases the power consumption of the circuit.

V. Niranjana *et al.* [23-24] use the gate-body-driven technique in the conventional FVF cell. The bulk and gate terminals of the input transistor are tied together and used to give input voltage. The gate-body-driven technique allows low voltage operation due to the body effect. Also, this technique improves the bandwidth and output resistance of the circuit without the requirement of any additional circuit and passive components.

U. Singh *et al.* [25] presented the various g_m -boosted FVF cells. The g_m -boosting technique is applied to the different structures given in [17] by using a high-gain amplifier in such a way that the output of the amplifier is given to the input of FVF cells. This contributes towards enhancing the bandwidth and decreasing the output resistance.

The class-A FVF cell improves the properties of conventional single transistor voltage follower due to the negative feedback present in FVF cell. The negative feedback reduces the output resistance and enhances the bandwidth of the cell. However, in both the voltage follower and class-A FVF cell, the slew rate is asymmetrical, and settling time is also poor. Since the load current is limited by the quiescent bias current, there exists a trade-off between quiescent power consumption and slew rate in voltage follower and class-A FVF cells. To solve this design constraint, various class-AB implementations of FVF cells have been reported in the literature which provide load current not limited by the quiescent bias current.

2.2 FVF cells based on class-AB operation

A. Torralba *et al.* [26-27] presented a voltage buffer consisting of two differential FVF cells that provide low power operation and a high slew rate. The input swing of the buffer has been increased by adding a DC level shifter. The buffer is suitable for transferring voltage to high capacitive loads due to its high output driving capability.

M. Jimenez *et al.* [28] reported class-AB FVF cell with increased current driving capability where a transistor is connected in parallel to the input transistor to provide additional current when input transistor is unable to provide current more than the bias current. But, the gate-to-source voltage of the additional transistor increases when it provides a large current. So, the output voltage shows deviation from the input voltage.

I. Padilla-Cantoya *et al.* [29] overcome the limitation of FVF cell [28] as the current through an additional transistor is maintained by using control circuitry. The output voltage follows the input voltage but, the output voltage is a DC level shifted from the input voltage and the voltage swing of the FVF cell is also limited. The folded version is also presented to increase the output voltage swing of the circuit. The reported circuits show improved sourcing and sinking capability at the output but the increased number of transistors increases the power dissipation as compared to other class-A and class-AB modifications of the FVF cell.

Two low-voltage unity-gain buffers are presented by A. Torralba *et al.* [30] by combining FVF cell and folded FVF cell. In the proposed circuits, the floating-gate technique is employed which allows low voltage and low power operation. The circuits maintain a high slew rate and good linearity.

The differential FVF cell based on the quasi-floating gate technique is reported by J. Ramirez Angulo *et al.* [31]. The differential FVF cell inherits the advantages of the FVF cell and output voltage is not DC level shifted from the input voltage. Unfortunately, the presented circuit has no high impedance node which prevents miller compensation and increases the area.

J. Ramirez Angulo *et al.* [32] have modified the conventional FVF cell using the quasi-floating gate technique and the introduced circuit offers the good current driving capability and slew rate without additional power dissipation. The presented FVF cell shows improved bandwidth and lower total harmonic distortion as compared to the conventional FVF cell.

Y. Haga *et al.* [33] introduced a replica-biased bulk-driven FVF cell. The replica-biased bulk-driven MOSFET is used for the input transistor to remove the DC level shift between input and output voltages. But, the sinking capability is poor since it is a class-A type, therefore the capability to drive large loads at high speed is poor. To overcome this problem, the circuit is modified to class-AB type by using a diode-connected current source instead of a constant current source. This change significantly improves the capability to sink large output currents while retaining various advantages such as low power consumption and high-power driving capability.

A. Lopez Martin *et al.* [34] utilized the quasi-floating gate technique in super source follower to achieve class-AB behaviour to solve the slew rate limitation problem of the conventional super source follower. The proposed class-AB super source follower does not require additional supply voltage and power consumption as compared with conventional source follower. However, the reported class-AB super source follower shows the DC level shift between input and output voltages.

Y. Haga *et al.* [35] presented a power-efficient voltage buffer by combining the bulk-driven replica biased topology discussed in [33] with super source follower [34]. The bulk-driven replica biased scheme is used for the input transistor to eliminate the DC level shift of super source follower. The quasi-floating gate technique allows class-AB operation in the suggested FVF cell.

Y. Haga *et al.* [36] modified the previously reported FVF cell [35] by using the quasi-floating gate technique. The quasi-floating gate technique is applied along with the bulk-driven technique

at the input transistor to allow low voltage operation. The proposed circuit is capable to drive large output currents but the circuit shows a poor power supply rejection ratio.

S. Wangtaphan *et al.* [37] suggested the modification of FVF cell [34] without using a replica biased scheme. The suggested FVF cell overcomes the problem of voltage shift between the input voltage and output voltage of FVF cell [34] by employing bulk-driven and quasi-floating gate technique at the input transistor instead of replica biased scheme.

J. de la Cruz-Alejo [38] presented the FVF cell using floating-gate MOS transistors both at the input transistor and feedback transistor to enhance the operation of the FVF cell in a low voltage environment. But, the floating gate transistors trap the initial charges at the gate which leads to DC offsets.

F. Centurelli *et al.* [39] proposed a class-AB buffer using the non-inverting gain stage in the feedback path which assures negative feedback and reduces the output resistance. The proposed buffer has a high slew rate and less setting time than the conventional FVF cell. The circuit is capable to handle large-swing signals. But, the non-inverting gain stage in the feedback path consisting of two branches creates two poles at a high frequency that reduces the phase margin and bandwidth of the feedback loop. Also, additional power is consumed by these additional branches.

F. Centurelli *et al.* [40] proposed a class-AB FVF cell to overcome the limitations of the reported FVF cell [39]. The proposed topology avoids the formation of an additional pole by using a common-gate auxiliary amplifier instead of a non-inverting stage consisting of two branches. The resulting circuit consumes less power and shows an improved phase margin. However, both the FVF cells [39-40] show similar performance in terms of slew rate, linear behaviour, and output voltage swing.

M. Gupta *et al.* [41] presented two modified output stages based on FVF cells [39-40] with the floating-gate technique. The suggested structures show significant improvement in bandwidth, current driving capability, and output resistance as compared to previously reported structures of the FVF cells [39-40].

U. Singh *et al.* [42] presented the super source follower with improved output voltage swing. The performance is improved by using two floating gate transistors in super source follower

instead of MOS transistors. Also, the resistive compensation technique is used in the feedback path of super source follower to enhance the bandwidth and speed.

A. Lopez Martin *et al.* [43] presented a modified super source follower using the quasi-floating gate technique to offer class-AB behaviour. But the input voltage swing is limited in the presented circuit. To enhance the input voltage range, the floating-gate technique is also used in the presented circuit.

C. Muniz-Montero *et al.* [44] overcome the limitation of [31] and presented a differential FVF cell without using a quasi-floating gate technique. The proposed differential FVF cell offers good sourcing and sinking current capabilities and is able to drive large capacitive loads.

The different approaches used to implement class-AB FVF cells reported in [28-29, 32, 39] are compared by I. Padilla-Cantoya *et al.* [45] and it is concluded that the output resistances of reported FVF structures [28, 32, 39] are more than the conventional FVF cell. The reported FVF cell [29] is further improved to achieve high linearity and a large operational range by I. Padilla-Cantoya *et al.* [45]. The class-AB operational transconductance amplifier structure with high linearity and large operational range implemented using reported FVF cell is also presented.

J. E. Molinar-Solis *et al.* [46] presented a bulk-driven configuration of the FVF cell. The proposed FVF cell uses a bulk-driven transistor to implement a constant current source of conventional FVF cell which acts as an adaptable current source to achieve class-AB operation.

M. Piry *et al.* [47] presented a class-AB FVF cell with an improved slew rate by the combination of two FVF cells. In one of the FVF cells, input is given to the N-type metal-oxide-semiconductor (NMOS) transistor and in another FVF cell input is given to the P-type metal-oxide-semiconductor (PMOS) transistor. Both the FVF cells use DC level shifter and the resulting class-AB FVF cell offers improved slew rate while operating at low voltage.

M. Khanjani Moaf *et al.* [48] introduced two class-AB voltage buffers using FVF cells. The two circuits offer a high slew rate along with low output resistance.

J. J. Ocampo-Hidalgo *et al.* [49, 50] proposed super source followers using the quasi-floating gate technique. The proposed super source followers use quasi-floating gate MOSFET in a negative feedback loop which helps to achieve class-AB operation. The quasi-floating gate

technique is used to solve the problem of trapping of initial charges in the floating-gate MOSFETs.

C. Jindal *et al.* [51] introduced a class-AB FVF cell based on bulk-driven and level shifter techniques. The bulk-driven technique is used to implement an adjustable current source to enhance the current driving capability while the level shifter technique is used to increase the swing of the class-AB FVF cell. But, the current sinking capability of the reported FVF cell is limited.

A. Paul *et al.* [52] reported the class-AB FVF cell based on double cascoded flipped voltage follower which includes local feedback loop with cascode transistors to enhance the bandwidth and current efficiency, but it consumes large power.

I. Padilla-Cantoya *et al.* [53] presented two modified structures of class-AB FVF cell namely low output resistance version and low voltage version. By combining conventional FVF cell, folded FVF, and an additional resistor, the class-AB operation is achieved. In the conventional FVF cell, bidirectional output currents passing through the voltage following transistor degrades the output resistance. But, the low output resistance version of the proposed class-AB FVF cell allows the flow of large bidirectional output currents through two paths maintaining a constant current in the circuit. Therefore, the proposed class-AB FVF cell offers low output resistance as compared to other reported class-AB FVF cells. Further, the low voltage operation is achieved in the low voltage version of the proposed class-AB FVF cell by changing connections across the resistance.

A. Paul *et al.* [54] suggested the modified version of the class-AB FVF cell [32]. As the structure reported in [32] uses large resistance which limits its current sourcing capability and does not allow optimization of positive slew rate, negative slew rate, and bandwidth simultaneously. To overcome this limitation, an extra transistor connected in parallel with the resistor, and a quasi-floating gate MOSFET are used in the modified version of the class-AB FVF cell.

J. J. Ocampo-Hidalgo *et al.* [55] presented the class-AB voltage follower by merging the conventional FVF cell and super source follower. The presented circuit offers low output resistance and symmetrical slew rate. But, this circuit needs high supply voltage for the proper operation.

2.3 Applications of FVF cell

The various basic structures are derived from the FVF cell such as FVF current sensor (FVFCS), FVF differential structure (DFVF), and FVF pseudo-differential pair (FVFDP) [16, 56-57]. These basic structures such as FVF, FVFCS, DFVF and FVFDP are used to implement various analog and mixed-signal circuits like current mirrors, current conveyors, operational transconductance amplifiers (OTAs), multipliers, filters, comparators, etc.

The current mirror based on FVF cell input stage has been presented by A. Torralba *et al.* [58]. The shunt feedback at the input provides low input impedance and the super cascode structure connected at the output provides high output impedance. J. Ramirez Angulo *et al.* [59] uses the FVF cell with shunt feedback input stage to achieve low input resistance. The regulated cascode output stage is used to enhance the output resistance. A. Torralba *et al.* [60] reported class-AB current mirror based on FVF cell which offers wide bandwidth and good linearity. The comparison of cascode current mirrors and FVF based current mirrors has been presented by C. Koliopoulos *et al.* [61] and they concluded that FVF based current mirrors offer superior performance. M. Gupta *et al.* [62–64] and U. Singh *et al.* [65] presented FVF based current mirrors with resistive compensation technique between gates of the primary current mirror for the enhancement of the bandwidth. Further, the current mirrors [63, 65] use resistances in the feedback paths of the FVF cells and the current mirror [64] uses an inductive compensation technique. FVF based current mirror using dynamic threshold MOSFET (DTMOS) technique is presented by V. Niranjana *et al.* [66]. The supply voltage and threshold voltage are reduced due to the use of the body effect. B. Aggarwal *et al.* [67] reported FVF based current mirror, which copies the input current accurately at the output due to the nested feedback loops at the input and output sides of the presented current mirror. The high output resistance has been achieved by using the super cascode technique at the output side of the current mirror. The FVF cell based current mirror presented by S. Garg *et al.* [68] offers low input compliance voltage due to the FVF cell and accurate current mirroring due to the self cascode output stage. A. Shrivastava *et al.* [69] presented FVF based current mirror which operates at low supply voltage and bandwidth of the presented current mirror is enhanced using resistance in the feedback path of FVF cell. The level shifted FVF cell [17] based current mirrors have been reported by B. Aggarwal *et al.* [70]. The presented circuits offer a wide operating current range due to the level shifter in the feedback path of FVF cell. In the proposed current mirror [70], the resistive compensation technique is used to increase the bandwidth and the super cascode output stage is used to

enhance the output resistance. The high dynamic range current mirror structure based on the FVF cell is suggested by G. K. Chakravarthy *et al.* [71]. It has low input resistance, high output resistance but the bandwidth is not as high as required. B. Aggarwal [72] presented a current mirror based on folded FVF cell at the input stage and cascode configuration at the output stage which helps to achieve low input resistance and high output resistance, respectively. M. Bchir *et al.* [73] reported FVF cell based current mirror which utilizes bulk-driven and quasi-floating gate techniques. The bulk-driven technique increases input voltage swing and quasi-floating gate technique improves the frequency response. N. Raj *et al.* [74-75] presented current mirrors with low input resistance which is achieved due to the FVF cell. The FVF cell uses a PMOS transistor in the negative feedback path which gives a low resistance node where current is injected. Further, the current mirror [75] shows enhanced output resistance due to the negative feedback loop and super cascode structure at the output. N. Domala *et al.* [76] presented FVF cell based current mirror using super transistors both at the input and output terminals of the current mirror to improve the input and output resistances. The super cascode configuration is also connected at output which further improves the output resistance.

A. J. Lopez-Martin *et al.* [77] presented a current conveyor based on the FVF cell. The FVF cell provides high input impedance, low output impedance, accurate copying of voltage and high speed for a given current consumption. The presented current conveyor is better in terms of bandwidth, supply voltage, and power consumption as compared to conventional current conveyors. The universal bi-quad filter based on the presented current conveyor is also discussed. A. P. Naik *et al.* [78] designed a compact current conveyor by using a current mirror which is based on the FVF cell. The current conveyor consumes low power. A high-performance class-AB second-generation current conveyor (CCII) based on FVF cell is proposed by K. Moustakas *et al.* [79]. As compared to class-A CCII based on FVF cell, the proposed class-AB CCII has very low power consumption. A class-AB CCII based on class-AB FVF cell is presented by F. Centurelli *et al.* [80] and compared with class-A CCII based on the conventional FVF cell. The class-AB FVF cell is capable of driving larger capacitive loads and it shows improved power efficiency and settling time in the current conveyor. G. Barile *et al.* [81] reported a current conveyor consisting of two class-AB FVF cells. The class-AB FVF cells improve the performance of the current conveyor in terms of impedance, accuracy, and current driving capability.

J. Galan *et al.* [82] proposed the OTA using two cross-coupled class-AB pseudo-differential pairs biased by the FVF cells. It offers a wide transconductance range and high linearity while consuming low power. X. Zhu *et al.* [83] proposed an OTA using FVF cell and source degeneration technique. The power supply requirement of OTA is reduced due to the FVF cell while the linearity of OTA is improved due to the source degeneration technique. X. Zhao *et al.* [84] presented a class-AB bulk-driven OTA with an improved slew rate. To increase the slew rate, OTA uses bulk-driven FVF cell at the input stage and current mirror as an active load. The output node of the FVF cell is used for the frequency compensation in the recycling folded cascode structure. K. Garradhi *et al.* [85] reported an OTA using FVF cell based current mirror and source degeneration technique. The FVF cell based current mirror provides low input impedance and high output impedance. The source degeneration technique is used at the input differential pair to improve the linearity. N. Narang *et al.* [86] presented FVF cell based OTA using the DTMOS technique. In the proposed OTA, by effectively using the body effect of DTMOS, the performance has been enhanced in terms of transconductance, output current, linearity, and bandwidth. T. Sharan *et al.* [87] reported a two-stage OTA in which a bulk-driven source-degenerated class-AB FVF cell is used in the first stage that provides rail-to-rail linear input signal driving capability. The input stage load is a self-cascode structure which is followed by a common source stage having a load of current source and this increases the overall gain. The cascode compensation in the proposed OTA increases the phase margin. S. Pourashraf *et al.* [88] implemented an OTA using class-AB cascoded FVF cell at the input stage and dynamically biased cascode transistors at the output stage. The class-AB OTA offers enhanced slew rate, output current, gain bandwidth, and open-loop gain. A. Sarkar *et al.* [89] and X. Zhao *et al.* [90] reported OTA structures using FVF cells in the adaptive biasing of the amplifier. The reported OTA [90] shows a high slew rate at the expense of large power consumption. A class-AB bulk-driven OTA using adaptive biasing is reported by M. Akbari *et al.* [91]. Using the quasi-floating gate technique two bulk-driven FVF cells are reformed as non-linear tail currents to improve the slew rate and transconductance of the reported OTA. A low power fully differential OTA operating in weak inversion region with rail-to-rail linear input range is presented by T. Sharan *et al.* [92]. The input pair of OTA is designed using bulk-driven source degenerated class-AB FVF cell, in which a regenerative feedback loop has been inserted to boost its bulk transconductance. In the presented OTA self cascode current mirror as a load is used to enhance its open-loop gain. X. Lv *et al.* [93] presented bulk-driven folded cascode OTA based on the FVF cell. The proposed OTA uses bulk-driven FVF cell and quasi-floating gate MOSFET to design the class-AB input

stage and class-AB output stage, respectively. The input and output stages enhance unity-gain bandwidth and dynamic current. A fully differential structure of FVF cell is used to design multi-input OTA by P. Bansal *et al.* [94]. The reported OTA offers large output current and transconductance with the minimum use of the active and passive elements. T. Dubey *et al.* [95] presented OTA using FVF cells at the input stage. The OTA uses both the floating gate and bulk-driven techniques employed in the input transistors of FVF cells to obtain the low voltage operation and increased linearity but it suffers from poor common-mode rejection ratio (CMRR). A. S. Khade *et al.* [96] presented an OTA using DTMOS based differential pair with the class-AB operation. The adaptive biasing consisting of the FVF cell is used to achieve class-AB operation which also enhances the dynamic current and gain-bandwidth product.

The four-quadrant multiplier based on FVF cell is presented by A. Demosthenous *et al.* [97]. The proposed multiplier offers low total harmonic distortion due to the FVF cell. C. Sawigun *et al.* [98] introduced a compact multiplier by connecting four common source amplifiers and two differential FVF cells. The FVF cells decrease the supply voltage requirement of the reported multiplier. A. H. Miremadi *et al.* [99] reported a low-voltage multiplier consisting of four nullers, four voltage adders, and a multiplier core. The voltage adders are designed using FVF cells to offer low voltage operation. J. Mateus *et al.* [100] proposed a current-mode multiplier using FVFCS. The multiplier uses a very low impedance input node of FVFCS, suitable for sensing the current signals. To cancel the higher-order components in the output current, two differential pairs have also been used. C. Sakul *et al.* [101] reported a simple structure of multiplier composed of two FVF cells and a multiplier core. The reported circuit shows a wide input range and operates at low supply voltage due to FVF cell. A. Satapathy *et al.* [102] used a voltage adder consisting of FVF cell as a basic building block to design an analog multiplier. The FVF cell allows the low voltage operation of the reported multiplier. A four-quadrant voltage-mode analog multiplier, which can work under low voltage due to the use of FVF cell is presented by U. Gurram *et al.* [103]. A. Diaz-Sanchez *et al.* [104] presented a high-speed multiplier composed of a Gilbert cell and four FVF cells. The FVF cells are used at the input and output current mirrors due to the low impedance nodes to achieve high speed and high performance.

A second-order low-pass filter designed by combining the FVF cell with two capacitors is reported by C. Sawigun *et al.* [105]. The reported low-pass filter is able to operate at low supply voltage due to the FVF cell. The fourth-order Butterworth low-pass filter based on FVF cell presented by F. Fary *et al.* [106] gives large in-band linearity due to the presence of local loop in

FVF cell. S. Thanapitak *et al.* [107] also reported a fourth-order low-pass filter for electrocardiogram signals. The presented filter is designed using FVF bi-quads with the level shifter. The FVF cell allows cascading of FVF bi-quads for implementation of higher-order filters without the loss of gain. R. Bagavathiyammal *et al.* [108] and S. Bano *et al.* [109] presented fourth-order low-pass bi-quad filters by cascading second-order PMOS based FVF bi-quad and NMOS based FVF bi-quad operating in the sub-threshold region for biomedical applications. The reported filters are designed using FVF cells which make them compact and allow operation in a low supply voltage environment.

The design and characterization of a latched voltage comparator using FVF cell at the input stage is presented by H. J. Achigui *et al.* [110]. The FVF cell enhances the input common-mode range of proposed comparator. A. C. Paglinawan *et al.* [111] reported dual-modulation based current comparator to improve accuracy. It uses FVF cell at the input stage to achieve low input resistance. V. Kumar *et al.* [112-113] presented current comparators based on FVF cell which helps to achieve less delay, low area and large voltage swing. The low-voltage current comparators using FVF cell at the input stage are presented by J. E. Molinar Solis *et al.* [114] and M. Bchir *et al.* [115]. The FVF cell offers a very low input resistance, which is mandatory for current-mode applications.

2.4 Research Gaps

In the literature, various structures of FVF cells have been presented and compared. Based on the literature survey, the following gaps are identified:

- The output of the FVF cell follows the input signal but the voltage gain of FVF cell is less than unity due to the body effect of the input transistor.
- The current sourcing/sinking capability of FVF cell is limited which results in an asymmetrical slew rate. However, the symmetrical slew rate is required to achieve class-AB behaviour.
- The bandwidth of FVF cell is low which limits its use in high-frequency applications.
- The output resistance is not low enough which decreases its speed of operation.

Hence, it is required to re-design the FVF cell through a novel approach to overcome the limitations of the reported structures of the FVF cell in the literature.

2.5 Objectives of proposed work

Based on research gaps, the following objectives are being proposed:

- To propose efficient low-voltage FVF cells in terms of electrical parameters such as current sourcing/sinking capability, output resistance, slew rate, etc.
- The proposed FVF cells shall be used to design a basic analog VLSI circuit.
- To validate the performance of the proposed circuits using post-layout simulations.

2.6 Research Methodology

To meet the objectives, the following research methodology has been followed:

- First, specifications required for designing the proposed FVF cells and current mirrors for 180 nm CMOS technology are defined.
- The analyses of the proposed FVF cells have been performed to calculate input/output voltage swing, output resistance, and voltage gain.
- The analyses of the proposed current mirrors have been performed to calculate input resistance, output resistance, and transfer function.
- The proposed FVF cells and current mirrors are designed using BSIM3V3 180 nm CMOS technology and simulated using spectre in the Cadence Virtuoso Analog Design Environment.
- The physical layouts of all the proposed circuits are designed using Cadence Virtuoso Layout XL editor in 180 nm CMOS technology.

CHAPTER 3

PROPOSED CLASS-AB FLIPPED VOLTAGE FOLLOWER CELLS

3.1 Introduction

In sub-micron CMOS technology, the design of low-voltage analog circuits with high performance has become a challenging task. The flipped voltage follower (FVF) cell is an important low-voltage transistor implementation technique and therefore efficient design of FVF cell leads to improved performance of the overall analog circuit. The design of FVF cell with a high slew rate along with low power consumption is a challenging task. The conventional FVF cell (consisting of NMOS transistors) is biased using a constant current source, which provides a relatively high negative slew rate as compared to a positive slew rate. Since the large-signal speed is limited by the minimum value of positive and negative slew rates, the symmetrical slew rate is required for the proper operation of the circuit. The other disadvantages of conventional FVF cell are limited input/output voltage swing and not low enough output resistance. Hence, to provide large dynamic currents to the load while quiescent bias currents are kept at very low values, class-AB biasing techniques can be employed in the conventional FVF cell that allows symmetric slew rates without any increment in the static power consumption. To overcome the limitations of class-A FVF cells, it is necessary to develop class-AB design techniques for FVF cells that can enhance their performance at low supply voltage.

The various class-AB FVF cells have been reported in the literature with improved performance over conventional FVF cell and class-A FVF cells [31–33, 35, 39, 43–44, 46–47, 50–52]. The differential version of FVF cell based on the quasi-floating gate technique that provides no DC level shift between input and output voltage has been reported by J. Ramirez-Angulo *et al.* [31], but this circuit occupies a large area. Another class-AB FVF cell using the quasi-floating gate technique has been presented by J. Ramirez-Angulo *et al.* [32] with improved bandwidth and slew rate, but it has a limited current sourcing capability. The bulk-driven technique connecting the bulk terminal of the MOS transistor to a potential other than the source terminal has also attracted attention recently. The class-AB FVF cells [33, 35] use the bulk-driven transistor as an input transistor where the bulk terminal is used to feed the input voltage. The class-AB operation is achieved by replacing the constant bias current source with diode-connected transistor which provides the current larger than the bias current in the FVF cell [33] while a quasi-floating gate transistor is used to implement the current source to achieve class-AB behaviour in FVF cell

[35]. The class-AB FVF cell [39] uses a non-inverting gain stage in the feedback path to reduce output resistance at the expense of increased power dissipation and reduced bandwidth. The folded FVF cell also known as super source follower showing class-AB operation using quasi-floating gate technique has been reported by A. J. Lopez-Martin *et al.* [43]. The authors have used floating-gate MOS transistor to enhance its input voltage range, but trapping of initial charge at the floating gate leads to DC offsets. The differential FVF cell [44] is designed without using a quasi-floating gate technique and it overcomes the limitation of the large area of cell reported by J. Ramirez-Angulo *et al.* [31]. The class-AB FVF cells [46, 51] use the bulk-driven technique in which the bulk terminal is connected to the drain terminal of the transistor to implement the current source, which gives the ability to source large current at the output. But the current sinking capabilities of these circuits are limited. The class-AB FVF cell with an improved slew rate has been presented by M. Piry *et al.* [47] by combining two FVF cells at the expense of increased power consumption. The other super source follower based on the quasi-floating gate technique has been suggested by J. J. Ocampo-Hidalgo *et al.* [50], but its current driving capability is limited. The class-AB FVF cell [52] based on double cascoded FVF includes local feedback loop and cascode transistors to enhance the bandwidth and current efficiency but it consumes large power.

In this chapter, four different structures of class-AB FVF cells are presented to overcome the limitations of reported FVF cells. The class-AB FVF cells proposed here are namely class-AB FVF cell-I, class-AB FVF cell-II, class-AB FVF cell-III and class-AB FVF cell-IV, which offer various improved electrical features such as high current sourcing/sinking capability, high slew rate, large input/output voltage swing, low output resistance, etc.

This chapter is organized as follows. Section 3.2 describes the proposed FVF cells. In section 3.3, the large-signal and small-signal analyses of the proposed FVF cells have been discussed. The simulation results of the proposed FVF cells are presented in section 3.4. The conclusion of the chapter is addressed in section 3.5.

3.2 Proposed flipped voltage follower cells

Flipped voltage follower (FVF) cells are the important building blocks of low-voltage analog and mixed-signal circuits. FVF cell is considered as a current sensing cell which requires low output resistance. It is also used as an output stage to accurately copy the input voltage to a load with high input resistance and low output resistance. The high current driving capability, high slew rate, large voltage swing, low output resistance and low power consumption are the key

specifications of FVF cells. To reduce the power consumption, class-AB biasing needs to be employed which enables the driving of large capacitive loads while keeping the low quiescent bias current. This section proposes four class-AB FVF cells with improved performance which can be efficiently used to design low-voltage analog and mixed-signal circuits.

3.2.1 Proposed class-AB FVF cell-I

The proposed class-AB FVF cell-I shown in Figure 3.1 is the modified version of the conventional FVF cell where transistors M_1 , M_3 and M_4 form the conventional FVF cell. In the conventional FVF cell, the output voltage (V_o) follows the input voltage (V_{in}) with a DC level shift of source-to-gate voltage according to the relation $V_o = V_{in} - V_{GS}$ while showing voltage gain less than unity. The DC level shift between input and output voltages has been eliminated in the proposed FVF cell-I by using a replica-biased scheme suggested by B. Blalock *et al.* [116]. The bulk-driven transistor M_1 is used as an input transistor, where its bulk terminal is used to feed the input voltage. The transistors M_2 and M_5 are the replica devices for transistors M_1 and M_4 , respectively. The gate of transistor M_1 is biased by the diode-connected replica transistor M_2 to eliminate the DC level shift between input and output voltages. The bulk terminal of the transistor M_2 is connected to its source terminal, which is the output node of the FVF cell-I. Since the transistors M_1 and M_2 are perfectly matched, gate-to-source voltages and the drain currents (I_b) of both the transistors are also equal. The bulk and source terminals of transistor M_1 become virtually shorted ($V_{BS1}=0$), which results in $V_o = V_{in}$.

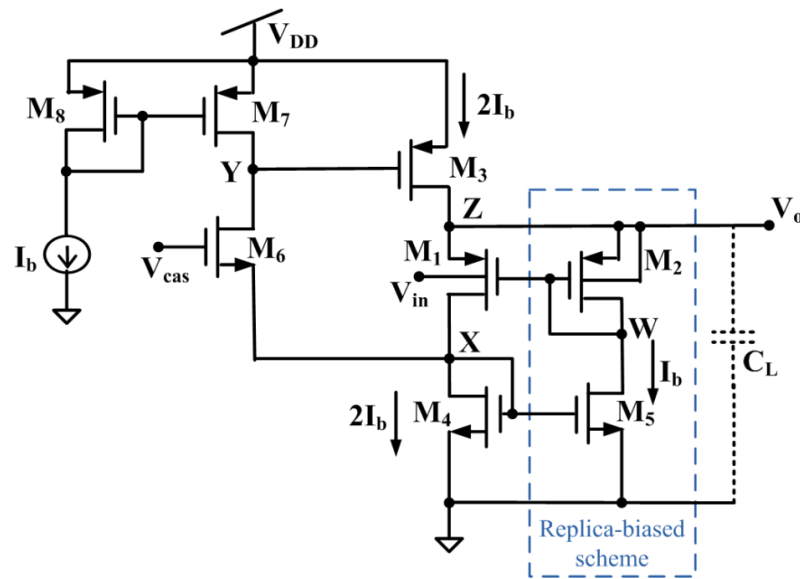


Figure 3.1 Proposed class-AB FVF cell-I

To achieve class-AB operation, the current sinking capability of FVF cell-I has been improved by using a diode-connected transistor M_4 instead of a constant current source of $2I_b$ while transistor M_3 allows the sourcing of large currents to the load capacitor (C_L). The gate-to-source voltages of transistors M_4 and M_5 are equal and aspect ratios of both the transistors are kept in such a way that the transistor M_5 copies the current I_b from transistor M_4 . In this way, the same current I_b is flowing through both the transistors M_1 and M_2 which validates the replica-biased scheme. Further, the cascoding transistor M_6 is connected between the gate terminal of transistor M_3 and the drain terminal of transistor M_4 to form shunt feedback. The transistor M_6 is biased using the current mirror formed by transistors M_7 and M_8 . The current source I_b can be implemented using a diode-connected transistor M_9 . The introduced transistor M_6 in the feedback path provides additional gain to the negative feedback loop, which results in low output resistance. Also, the inclusion of this cascoding transistor in the feedback path gives an additional advantage of very small variations at node 'X'.

The proposed class-AB FVF cell-I can provide approximately unity voltage gain with high current driving capability but it shows limited bandwidth because the input voltage is applied at the bulk terminal.

3.2.2 Proposed class-AB FVF cell-II

The proposed class-AB FVF cell-II overcomes the limitation of the proposed class-AB FVF cell-I by using a gate-driven transistor for the input voltage as shown in Figure 3.2.

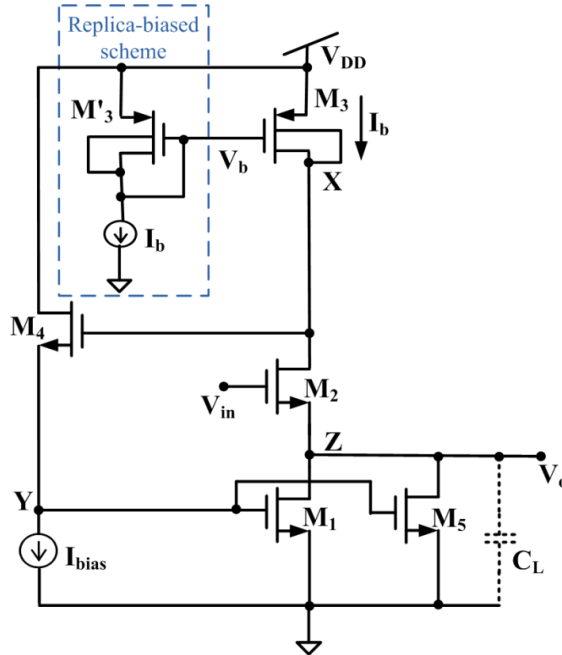


Figure 3.2 Proposed class-AB FVF cell-II

The gate terminal of transistor M_2 is used to give the input voltage (V_{in}) and its source terminal is used to draw the output voltage (V_o). Instead of using a constant bias current source I_b which limits the sourcing current, a bulk-driven transistor M_3 has been used to achieve class-AB operation in the proposed FVF cell-II. The bulk-driven transistor M_3 forms an adaptable current source in which bulk and drain terminals are connected to each other. The transistor M_3 allows the sourcing of current larger than the bias current as its source-to-bulk voltage varies with the change in input voltage which changes its threshold voltage. The DC voltage V_b applied at the gate terminal fixes the gate-to-source voltage of transistor M_3 (V_{GS3}) leading to constant bias current in the branch consisting of transistors M_{1-3} . The fixed DC voltage (V_b) is generated using the gate terminal of a diode-connected transistor M'_3 (replica of transistor M_3). The bulk and drain terminals of transistor M'_3 are also connected to each other and a sinking current source I_b is connected at the drain terminal. To increase the current sinking capability, the transistor M_5 is connected in parallel to the transistor M_1 . The transistor M_5 copies the equal amount of current flowing through transistor M_1 because these transistors are perfectly matched. The introduced transistor M_5 also improves the bandwidth and reduces the output resistance. The transistor M_4 connected in the feedback path between nodes 'X' and 'Y' acts as a DC level shifter which increases the swing of the proposed FVF cell-II. The level shifter is biased using a current source (I_{bias}) which can be implemented by a diode-connected transistor M_6 .

The proposed FVF cell-II is capable of sourcing and sinking currents larger than the bias current I_b , and hence it shows class-AB operation. In Figure 3.2, when the input voltage increases, the voltage at node 'X' is decreased. The decreased voltage at node 'X' increases the source-to-bulk voltage of transistor M_3 which allows it to provide positive output currents to the load capacitor (C_L) larger than the bias current, leading to an increase in the current sourcing capability. The transistor M_4 transfers the variations of voltage from node 'X' to node 'Y'. The decrement in voltage at node 'X' decreases the gate-to-source voltages of transistors $M_{1,5}$ and hence turns off the transistors $M_{1,5}$. When input voltage decreases, the voltages at nodes 'X' and 'Y' are increased. These increased voltages allow transistors $M_{1,5}$ to sink large negative output currents from the load capacitor. Thus, the current sinking capability of the proposed class-AB FVF cell-II is increased at the expense of an extra transistor.

3.2.3 Proposed class-AB FVF cell-III

The proposed class-AB FVF cell-III shown in Figure 3.3 avoids the requirement of an extra transistor for sinking the output currents used in the proposed class-AB FVF cell-II. The

proposed FVF cell-III uses quasi-floating gate and bulk-driven techniques to achieve class-AB operation. In the quasi-floating gate technique, a capacitor C_{bat} is included between two nodes ('X' and 'Y'), and a large valued resistance R_{large} is connected between gate terminals of transistors M_2 and M_5 to set the quiescent voltage at the gate of the transistor M_2 . The transistors M_{6-7} form a current mirror to copy the current $I_b (=I_{bias})$, and a diode-connected transistor M_5 provides the voltage V_b . The current source I_b can be implemented by using a diode-connected transistor M_8 . The resistance R_{large} is implemented by transistor M_4 operating in the cut-off region. There is no voltage drop across R_{large} due to which it establishes well-defined quiescent voltage V_b at the gate of transistor M_2 that maintains the bias current across transistor M_2 . This makes the gate of transistor M_2 as a quasi-floating gate under dynamic conditions. Under DC operating conditions, the voltages V_X and V_Y at nodes 'X' and 'Y' are independent of each other, whereas these nodes are connected under dynamic conditions. The capacitor C_{bat} and resistance R_{large} act as a high pass filter with cut-off frequency f_o ($1/2\pi R_{large}C_{bat}$) for signals passing from node 'X' to node 'Y'.

Using the bulk-driven technique, the transistor M_3 acts as an adaptable current source as the bulk terminal is connected to the drain terminal. The adaptable current source increases the current sourcing capability of the proposed class-AB FVF cell-III. The gate terminal of transistor M_3 is connected with fixed DC voltage (V_{bias}) and to generate this voltage, the gate terminal of a diode-connected transistor M'_3 (replica of transistor M_3) is used. The bulk and drain terminals of transistor M'_3 are also connected to each other and a sinking current source I_{bias} is connected at the drain terminal.

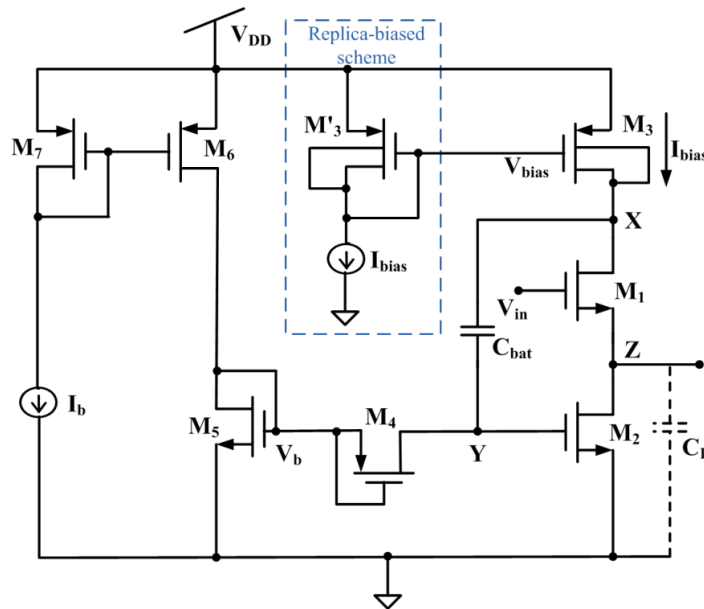


Figure 3.3 Proposed class-AB FVF cell-III

The gate voltage V_{bias} fixes the gate-to-source voltage of transistor M_3 and therefore, the bias current in the branch M_1 - M_3 . The voltage at node 'X' controls transistors M_2 and M_3 to preserve the bias current in the branch consisting of transistors M_1 - M_3 . The gate and source terminals of transistor M_1 are used to apply the input voltage (V_{in}) and draw the output voltage (V_o), respectively.

The transient variations in input voltage generate voltage V_X at node 'X' which is inverted with respect to the input voltage. Due to the large time constant ($\tau = R_{\text{large}}C_{\text{bat}}$), the capacitor C_{bat} cannot acquire charge rapidly at node 'X'. So, the capacitor C_{bat} acts as a floating battery and transfers the voltage variations from node 'X' to node 'Y'. When V_{in} increases, it leads to a decrease in voltage at node 'X' and an increase in source-to-bulk voltage of transistor M_3 . This allows bulk-driven transistor M_3 to supply large output positive current to the capacitive load (C_L) and thus increased current sourcing capability and increased positive slew rate are achieved. However, the decreased voltage at node 'Y' decreases the gate-to-source voltage and the drain current of transistor M_2 . When V_{in} decreases, the voltages at nodes 'X' and 'Y' are increased. The increased voltage at node 'X' decreases the current through transistor M_3 and increased voltage at node 'Y' increases the negative output current through transistor M_2 , and hence increased current sinking capability and increased negative slew rate are achieved. Therefore, it can be concluded that the proposed class-AB FVF cell-III has a symmetrical slew rate which confirms its class-AB operation.

The proposed class-AB FVF cell-III offers an improved symmetric slew rate as compared to the proposed class-AB FVF cell-II. However, the proposed class-AB FVF cell-III suffers from the certain limitation that sourcing current provided by transistor M_3 passes through transistor M_1 , affecting the gate-to-source voltage of transistor M_1 and varies the output voltage with respect to the input voltage which results in not low enough output resistance.

3.2.4 Proposed class-AB FVF cell-IV

To further improve the output resistance of the proposed class-AB FVF cell-III, the class-AB FVF cell-IV shown in Figure 3.4 is proposed. The proposed class-AB FVF cell-IV designed using level shifter, folding transistor and resistor R_b overcomes the limitation of output resistance and shows improved input/output voltage swing as compared to class-AB FVF cell-III. The transistors M_4 and M_5 are used as a level shifter and a folding transistor, respectively. The current source I_{bls} is used to bias the level shifter transistor M_4 . It can be implemented by using a diode-connected transistor M_6 which always remains in the saturation region to generate constant

current. The transistors M_5 and M_2 provide large sourcing and sinking currents, respectively to the capacitive load (C_L) to achieve class-AB operation. The transistor M_1 acts as a voltage following transistor. The input voltage (V_{in}) and output voltage (V_o) are applied at the gate and source terminals of transistor M_1 , respectively. The transistor M_4 introduced between the gate terminal of transistor M_2 and drain terminal of transistor M_3 allows the output voltage to follow the input voltage linearly for a large range and thus increases the input/output voltage swing. The folding transistor M_5 is driven through the drain of voltage following transistor M_1 . When the folding transistor M_5 is directly driven by input voltage then if the input voltage increases, the source-to-gate voltage of the folding transistor M_5 decreases, and therefore for the given input voltage range, the transistor M_5 will turn off and will not be able to provide sourcing current. When the folding transistor M_5 is driven through the drain of voltage following transistor M_1 then for the given input voltage range, in which output voltage follows the input voltage, the transistor M_5 remains in the saturation region. The bias voltage (V_{bias}) applied at the gate of transistor M_3 generates the bias current (I_b). This bias voltage (V_{bias}) is generated using the diode-connected transistor (replica transistor M'_3) with sinking current source I_b . A resistor R_b generates voltage $V_b (=I_b R_b)$ between gates of transistors M_4 and M_5 using the same biasing current I_b from M_1 and thus, it does not require additional power. The voltage V_b generated across resistor R_b provides complimentary voltage variations to the gates of M_4 and M_5 and therefore, their currents for the class-AB operation.

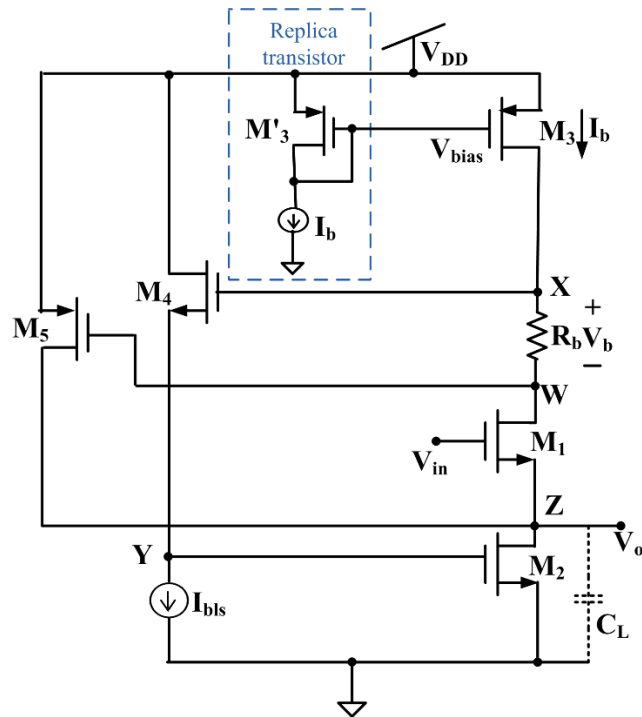


Figure 3.4 Proposed class-AB FVF cell-IV

The inclusion of resistor R_b gives a negative value for voltage V_b when the path consisting of transistors M_5 , M_4 and M_2 is considered to calculate power supply voltage requirement. Therefore, it reduces the minimum power supply voltage requirement of the proposed class-AB FVF cell-IV by the voltage V_b . The voltage variation at the gate of transistor M_4 is transferred to the gate of transistor M_2 through the level shifter. When input voltage increases, the source-to-gate voltage of transistor M_5 (V_{SG5}) increases and the gate-to-source voltage of transistor M_2 (V_{GS2}) decreases. During the rising edge of input voltage, the sourcing current through transistor M_5 increases, and sinking through transistor M_2 does not occur, whereas during the falling edge of input voltage V_{GS2} increases which increases the current sinking from the capacitive load. Therefore, the proposed class-AB FVF cell-IV provides large sourcing and sinking currents during the rising and falling edges of input voltage, which confirms its symmetrical slew rate and class-AB behaviour.

3.3 Analysis of proposed FVF cells

The analyses of all of the proposed class-AB FVF cells presented in section 3.2 are described in this section.

3.3.1 Analysis of proposed class-AB FVF cell-I

In this section, large-signal analysis, small-signal analysis and stability analysis of the proposed FVF cell-I are presented.

3.3.1.1 Large-signal analysis

The transistors of the proposed class-AB FVF cell-I are operating in the saturation region under equilibrium conditions. Using condition of saturation region operation for transistors M_1 and M_3 ($V_{SD1,3} \geq V_{SDsat1,3}$), the lower and upper limits of the output voltage (V_o) can be expressed as

$$V_o \geq V_{D1} + V_{SDsat1} \quad (3.1)$$

$$V_o \leq V_{G3} + V_{th3} \quad (3.2)$$

Using equations (3.1) and (3.2), the voltage range of the V_o is given as

$$V_{D1} + V_{SDsat1} \leq V_o \leq V_{G3} + V_{th3} \quad (3.3)$$

The transistor M_6 is also operating in the saturation region, so we can assume

$$V_{DSsat6} = V_{DS6} = V_{G3} - V_{D1} \quad (3.4)$$

Using equations (3.3) and (3.4), the output voltage swing (V_{osw}) can be written as

$$V_{osw} = V_{DSsat6} + V_{th3} - V_{SDsat1} \quad (3.5)$$

Since the bulk and the source terminals of transistor M_1 are virtually at the same potential, the input voltage swing (V_{isw}) of the proposed class-AB FVF cell-I can be expressed as

$$V_{isw} = V_{DSsat6} + V_{th3} - V_{SDsat1} \quad (3.6)$$

The supply voltage (V_{DD}) requirements of the paths through transistors M_1 and M_2 are given in equations (3.7) and (3.8), respectively.

$$V_{DD} = V_{SDsat3} + V_{SDsat1} + V_{GS4} \quad (3.7)$$

$$V_{DD} = V_{SDsat3} + V_{DSsat5} + V_{SG2} \quad (3.8)$$

When the path through transistor M_6 is considered, the V_{DD} is given as

$$V_{DD} = V_{DSsat6} + V_{SG3} + V_{GS4} \quad (3.9)$$

From equations (3.7), (3.8) and (3.9), it can be concluded that the minimum supply voltage (V_{DDmin}) requirement of the proposed class-AB FVF cell-I can be expressed by equation (3.9).

3.3.1.2 Small-signal analysis

In this section, output resistance and transfer function analyses of the proposed class-AB FVF cell-I using small-signal equivalent models are presented.

3.3.1.2.1 Output resistance

The proposed class-AB FVF cell-I overcomes the limitation of output resistance of FVF cell reported in the literature [33] by introducing cascoding transistor M_6 in the feedback path. So, the small-signal equivalent model shown in Figure 3.5 is used to analyze the output resistance of the proposed class-AB FVF cell-I, where the output terminal is connected to a voltage source (v_o) which supplies a current (i_o). In the model, g_{m1-6} are the transconductances of transistors M_{1-6} , $g_{mb1,6}$ are the transconductances of transistors $M_{1,6}$ due to body effect and r_{o1-7} are the output resistances of transistors M_{1-7} . Applying Kirchoff's Current Law (KCL) at node 'Y' and assuming $r_{o7} \gg r_{o6}$; $g_m r_o \gg 1$, we get

$$v_{d6} = (g_{m6} + g_{mb6})r_{o6}v_{d1} \quad (3.10)$$

Applying KCL at node 'W' and assuming $g_m r_o \gg 1$, we get

$$v_{g1} = v_o - \frac{g_{m5}}{g_{m2}}v_{d1} \quad (3.11)$$

Applying KCL at node 'X', we get

$$(g_{m1} + g_{mb1})v_o = g_{m1}v_{g1} + (g_{m4} + g_{m6} + g_{mb6})v_{d1} - \frac{v_{d6}}{r_{o6}} \quad (3.12)$$

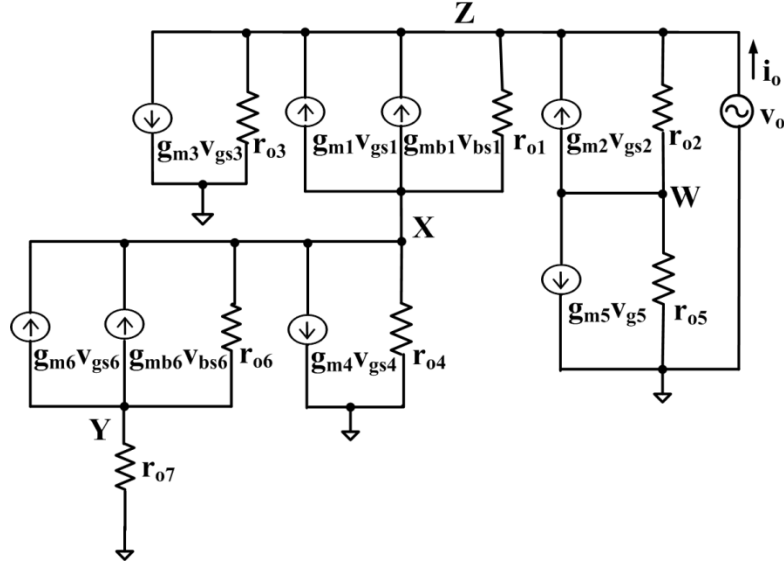


Figure 3.5 Small-signal equivalent model of the proposed class-AB FVF cell-I for the calculation of the output resistance

Using equations (3.10), (3.11) and (3.12), the value of v_{d1} can be written as

$$v_{d1} = \frac{g_{mb1}}{g_{m4}} v_o \quad (3.13)$$

In equation (3.13), it is assumed that $g_{m4}g_{m2} \gg g_{m1}g_{m5}$.

Applying KCL at node 'Z', we get

$$i_o = (v_o - v_{g1})(g_{m1} + g_{m2}) + g_{mb1}v_o + g_{m3}v_{d6} - \frac{v_{d1}}{r_{o1}} \quad (3.14)$$

Using equations (3.10), (3.11) and (3.13), the expression of output resistance (R_{out}) of the proposed class-AB FVF cell-I is given as

$$R_{out} = \frac{g_{m2}g_{m4}}{g_{mb1}g_{m2}g_{m4} + g_{mb1}g_{m5}(g_{m1} + g_{m2}) + g_{mb1}g_{m2}g_{m3}(g_{m6} + g_{mb6})r_{o6}} \quad (3.15)$$

In equation (3.15), it is assumed that $g_m r_o \gg 1$.

Also, the expression of R_{out} of the FVF cell proposed in [10] is given in equation (3.16).

$$R_{out} = \frac{g_{m2}g_{m4}}{g_{mb1}g_{m2}g_{m4} + g_{mb1}g_{m5}(g_{m1} + g_{m2}) + g_{mb1}g_{m2}g_{m3}} \quad (3.16)$$

By comparing equations (3.15) and (3.16), it is evident that the cascoding transistor M_6 reduces the output resistance because a factor $(g_{m6} + g_{mb6})r_{o6}$ is introduced in the denominator of equation (3.15).

3.3.1.2.2 Transfer function

To calculate the transfer function, a high-frequency small-signal equivalent model of the proposed class-AB FVF cell-I is shown in Figure 3.6. The input voltage is given at the bulk

terminal and output voltage is drawn from the source terminal of transistor M_1 . In the model, the capacitances at the nodes 'X', 'Y' and 'Z' are denoted by C_X , C_Y and C_L , respectively.

Applying KCL at node 'Y', we get

$$v_{d6}(s) = \frac{(g_{m6} + g_{mb6})r_{o6}v_{d1}(s)}{(1 + sC_Yr_{o6})} \quad (3.17)$$

In equation (3.17), it is assumed $r_{o7} \gg r_{o6}$ and $g_m r_o \gg 1$.

Applying KCL at node 'X', we get

$$(g_{m1} + g_{mb1})v_o(s) = g_{m1}v_{g1}(s) + (g_{m4} + g_{m6} + g_{mb6} + sC_X)v_{d1}(s) + g_{mb1}v_{in}(s) - \frac{v_{d6}(s)}{r_{o6}} \quad (3.18)$$

Using equations (3.11), (3.17) and (3.18), the value of $v_{d1}(s)$ can be written as

$$v_{d1}(s) = \frac{g_{mb1}(1 + sC_Yr_{o6})(v_o(s) - v_{in}(s))}{(g_{m4} + sC_X)(1 + sC_Yr_{o6}) + (g_{m6} + g_{mb6})sC_Yr_{o6}} \quad (3.19)$$

In equation (3.19), it is assumed that $g_{m4}g_{m2} \gg g_{m1}g_{m5}$.

Applying KCL at node 'Z', we get

$$(g_{m1} + g_{mb1} + g_{m2})v_o(s) + g_{m3}v_{d6}(s) + sC_Lv_o(s) = (g_{m1} + g_{m2})v_{g1}(s) + g_{mb1}v_{in}(s) + \frac{v_{d1}(s)}{r_{o1}} \quad (3.20)$$

Using equations (3.11), (3.17), (3.19) and (3.20), the transfer function ($A_v(s)$) of the proposed class-AB FVF cell-I is given in equation (3.21).

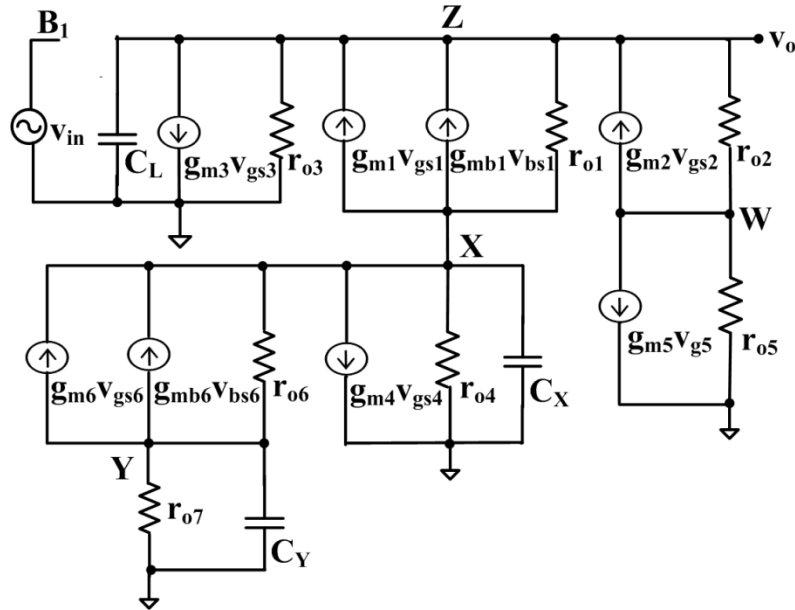


Figure 3.6 High-frequency small-signal equivalent model of the proposed class-AB FVF cell-I for the calculation of the transfer function

$$A_v(s) = \frac{v_o(s)}{v_{in}(s)} \quad (3.21)$$

$$\frac{C_X C_Y g_{mb1} r_{o6} s^2 + \left(\frac{g_{m4} g_{mb1} C_Y r_{o6} + g'_{m6} g_{mb1} C_Y r_{o6}}{g_{mb1} C_X + 2g_{m5} g_{mb1} C_Y r_{o6}} \right) s^1 + \left(\frac{g_{m4} g_{mb1} + 2g_{m5} g_{mb1}}{+g_{m3} g_{mb1} g'_{m6} r_{o6}} \right)}{C_X C_Y C_L r_{o6} s^3 + \left(\frac{g_{m4} C_Y C_L r_{o6} + g'_{m6} C_Y C_L r_{o6}}{g_{mb1} C_X C_Y r_{o6} + C_X C_L} \right) s^2 + \left(\frac{2g_{m5} g_{mb1} C_Y r_{o6} + g_{m4} g_{mb1} C_Y r_{o6}}{g'_{m6} g_{mb1} C_Y r_{o6} + g_{m4} C_L + g_{mb1} C_X} \right) s + \left(\frac{g_{m4} g_{mb1} + 2g_{m5} g_{mb1}}{g_{m3} g_{mb1} g'_{m6} r_{o6}} \right)}$$

where $g'_{m6} = g_{m6} + g_{mb6}$ and $g_m r_o \gg 1$.

From equation (3.21), it can be seen that the DC gain of the proposed class-AB FVF cell-I is unity when $s=0$.

3.3.1.3 Stability analysis

To calculate the open-loop voltage gain, the feedback path formed by transistor M_6 has been opened by using the method suggested in [16]. The open-loop voltage gain (A_{ol}) of the proposed class-AB FVF cell-I is given as

$$A_{ol} = -g_{m3} R_{olx} \quad (3.22)$$

where R_{olx} is the open-loop resistance at node 'X'.

The R_{olx} can be written as

$$R_{olx} = \frac{v_x}{i_x} = 1/g_{m4} \parallel (g_{m1} r_{o1} r_{o3}) \cong 1/g_{m4}; \text{ since, } 1/g_{m4} \ll (g_{m1} r_{o1} r_{o3}) \quad (3.23)$$

Using equations (3.22) and (3.23), the A_{ol} is given as

$$|A_{ol}| = \frac{g_{m3}}{g_{m4}} \quad (3.24)$$

The small-signal equivalent model of the proposed class-AB FVF cell-I for the calculation of the open-loop resistance at node 'Z' (R_{olz}) is shown in Figure 3.7. By applying KCL at node 'Z', we get

$$i_z + g_{m1} v_{g1} - v_z (g_{m1} + g_{mb1}) - \frac{v_z}{1/g_{m2} + r_{o5}} - \frac{v_z}{r_{o3}} = 0 \quad (3.25)$$

By applying KCL at node 'W', the gate voltage of transistor M_1 (v_{g1}) is given as

$$v_{g1} = \frac{r_{o5} v_z}{1/g_{m2} + r_{o5}} \quad (3.26)$$

Using equations (3.25) and (3.26), the R_{olz} can be written as

$$R_{olz} = \frac{1}{g_{mb1}} \quad (3.27)$$

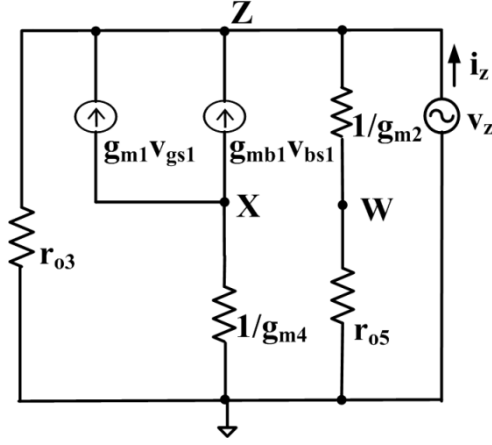


Figure 3.7 Small-signal equivalent model of the proposed class-AB FVF cell-I for the calculation of the open-loop resistance at node ‘Z’

It is observed that there are two poles $w_{px} = \frac{1}{R_{olx}C_x}$ and $w_{pz} = \frac{1}{R_{olz}C_L}$ at node ‘X’ and node ‘Z’, respectively.

Using equation (3.23), the pole at node ‘X’ (w_{px}) can be written as

$$w_{px} = \frac{g_{m4}}{C_X} \quad (3.28)$$

Using equation (3.27), the pole at node ‘Z’ (w_{pz}) can be written as

$$w_{pz} = \frac{g_{mb1}}{C_L} \quad (3.29)$$

For the capacitive loads $C_L < 30\text{pF}$, the dominant pole exists at node ‘X’ and non-dominant pole exists at node ‘Z’. The open-loop voltage gain and dominant pole given in equations (3.24) and (3.28), respectively define the gain-bandwidth product (GBW) of the proposed class-AB FVF cell-I as

$$GBW = \frac{g_{m3}}{C_X} \quad (3.30)$$

To ensure stability, the condition usually used to confirm 45° phase margin is $w_{pz} \geq GBW$ [46].

Using equations (3.29) and (3.30), the stability condition ($w_{pz} \geq GBW$) in this case results in

$$C_L \leq \frac{g_{mb1}}{g_{m3}} C_X \quad (3.31)$$

The condition given in equation (3.31) can be easily maintained by a compensation capacitor C_C at node ‘X’. For large capacitive loads $C_L \geq 30\text{ pF}$, the dominant pole exists at node ‘Z’ and the non-dominant pole exists at node ‘X’. The GBW using equations (3.24) and (3.29) is given as

$$GBW = \frac{g_{m3}g_{mb1}}{g_{m4}C_L} \quad (3.32)$$

Using equations (3.28) and (3.32), the stability condition $w_{px} \geq \text{GBW}$ results in

$$C_L \geq \frac{g_{m3}g_{mb1}}{(g_{m4})^2} C_X \quad (3.33)$$

From equation (3.33), it is evident that the compensation capacitor is not required in this case.

3.3.2 Analysis of proposed class-AB FVF cell-II

This section presents large-signal analysis, small-signal analysis and stability analysis of the proposed class-AB FVF cell-II.

3.3.2.1 Large-signal analysis

For large-signal analysis, it is assumed that the proposed class-AB FVF cell-II is operating under equilibrium conditions. When the input voltage is less than the threshold voltage ($V_{in} < V_{thM2}$), transistor M_2 is off and it results in zero output voltage. With the increase in input voltage, transistor M_1 operates in the saturation region and output voltage follows the input voltage linearly with the level shift of gate-to-source voltage of transistor M_2 . The drain-to-source voltage conditions of transistors $M_{1,2,4,5}$ to operate in the saturation region are given as

$$V_{DS1,2,4,5} \geq V_{DSsat1,2,4,5} = V_{GS1,2,4,5} - V_{th1,2,4,5} \quad (3.34)$$

Using saturation condition given in equation (3.34) for transistor M_2 , the upper limit of output voltage (V_o) is given as

$$V_o \leq V_X - V_{DSsat2} \quad (3.35)$$

Using saturation condition given in equation (3.34) for the transistors $M_{1,5}$, the lower limit of the V_o is given as

$$V_o \geq V_{DSsat1,5} + V_Y - V_{GS1,5} \quad (3.36)$$

From equations (3.35) and (3.36), the output voltage swing (V_{osw}) of the proposed class-AB FVF cell-II can be expressed as

$$V_{osw} = V_{GS4} + V_{GS1,5} - V_{DSsat1,5} - V_{DSsat2} \quad (3.37)$$

where $V_{GSM4} = V_X - V_Y$.

Using saturation condition given in equation (3.34) for transistor M_2 , the upper limit of input voltage (V_{in}) is given as

$$V_{in} \leq V_{GS4} + V_{GS1,5} + V_{th2} \quad (3.38)$$

Assuming transistors $M_{1,5}$ are operating in the saturation regions ($V_{DS1,5} = V_{DSsat1,5}$) and the transistor M_2 is in ON condition, the lower limit of the V_{in} can be written as

$$V_{in} \geq V_{th2} + V_{DSsat1,5} \quad (3.39)$$

Using equations (3.38) and (3.39), the input voltage swing (V_{isw}) of the proposed class-AB FVF cell-II is given as

$$V_{isw} = V_{GS4} + V_{GS1,5} - V_{DSsat1,5} \quad (3.40)$$

The supply voltage (V_{DD}) requirement of the proposed class-AB FVF cell-II (when the path through the output branch is considered) can be written as

$$V_{DD} = V_{SDsat3} + V_{DSsat1,5} + V_{DSsat2} \quad (3.41)$$

The V_{DD} requirement of the proposed class-AB FVF cell-II (when the path through transistor M_4 is considered) can be expressed as

$$V_{DD} = V_{SDsat3} + V_{GS4} + V_{GS1,5} \quad (3.42)$$

From equations (3.41) and (3.42), it can be concluded that the minimum supply voltage (V_{DDmin}) requirement of the proposed class-AB FVF cell-II can be expressed by equation (3.42).

3.3.2.2 Small-signal analysis

This section discusses the analyses of output resistance and transfer function of the proposed class-AB FVF cell-II using small-signal equivalent models.

3.3.2.2.1 Output resistance

The small-signal equivalent model of the proposed class-AB FVF cell-II shown in Figure 3.8 is used to calculate the output resistance. In the figure, the input terminal (G_2) is connected to the ground and the output terminal is connected to the voltage source v_o which gives the output current i_o .

Applying KCL at nodes 'Z', 'Y' and 'X', we get

$$g_{m2}(-v_o) - g_{mb2}v_o + \frac{v_{g4}-v_o}{r_{o2}} = (g_{m1} + g_{m5})v_{g1} + \frac{v_o}{r_{o1}} + \frac{v_o}{r_{o5}} - i_o \quad (3.43)$$

$$g_{m4}v_{gs4} - g_{mb4}v_{s4} = \frac{v_{g1}}{r_{o4}} + v_{g1}g_{m6} \quad (3.44)$$

$$g_{m2}(-v_o) - g_{mb2}v_o + \frac{v_{g4}-v_o}{r_{o2}} = -g_{mb3}v_{g4} - \frac{v_{g4}}{r_{o3}} \quad (3.45)$$

where $g_{m1,2,4,5,6}$ are the transconductances of transistors $M_{1,2,4,5,6}$, $g_{mb2,4}$ are the transconductances of transistors $M_{2,4}$ due to the body effect and $r_{o1,2,3,4,5}$ are the output resistances of transistors $M_{1,2,3,4,5}$.

Using equation (3.44), the value of the gate voltage of transistor M_1 (v_{g1}) is given in equation (3.46).

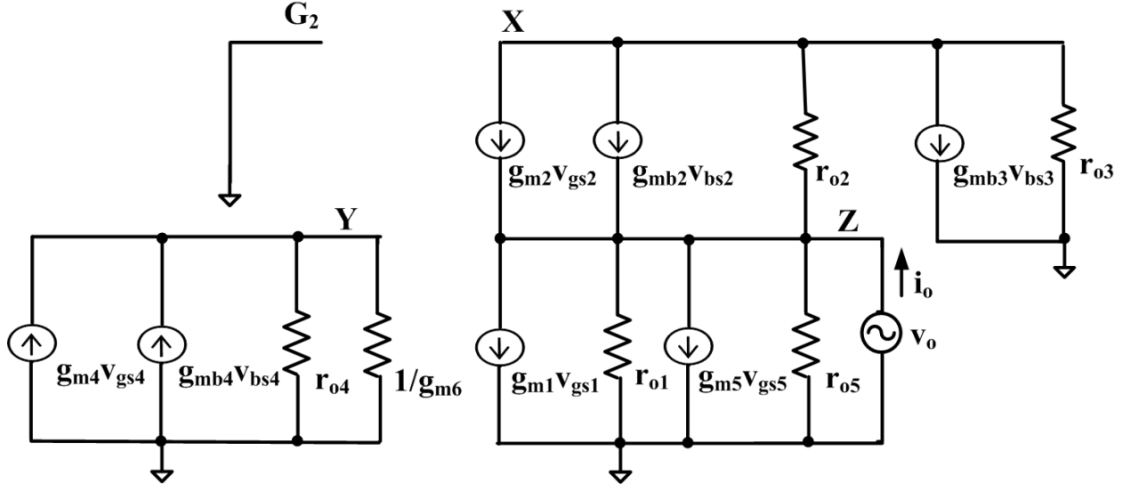


Figure 3.8 Small-signal equivalent model of the proposed class-AB FVF cell-II to calculate the output resistance

$$v_{g1} = \frac{v_{g4} (g_{m4}) (r_{o4} || 1/g_{m6})}{1 + (g_{m4} + g_{mb4}) (r_{o4} || 1/g_{m6})} \quad (3.46)$$

In equation (3.46), the value of $g_{mb4} \ll g_{m4}$, so g_{mb4} can be neglected with respect to g_{m4} and also the value of $r_{o4} \ll 1/g_{m6}$, so only r_{o4} will be effective. Using these approximations, equation (3.46) reduces to

$$v_{g1} = \frac{g_{m4} r_{o4} v_{g4}}{1 + g_{m4} r_{o4}} \quad (3.47)$$

Using approximation $g_m r_o \gg 1$ in equation (3.45), the value of gate voltage of transistor M_4 (v_{g4}) is obtained as

$$v_{g4} = \frac{v_o (g_{m2} + g_{mb2})}{g_{mb3}} \quad (3.48)$$

Substituting the values of v_{g1} and v_{g4} from equations (3.47) and (3.48) in equation (3.43), the output resistance (R_{out}) of the proposed class-AB FVF cell-II is given as

$$R_{out} = \frac{g_{mb3}}{(g_{m2} + g_{mb2})(g_{mb3} + g_{m1} + g_{m5})} \quad (3.49)$$

3.3.2.2.2 Transfer function

The high-frequency small-signal equivalent model of the proposed class-AB FVF cell-II shown in Figure 3.9 is used to calculate the transfer function. In Figure 3.9, the capacitances C_X , C_Y and C_L are included at nodes 'X', 'Y' and 'Z', respectively for the high-frequency analysis. Applying KCL at nodes 'Z', 'Y' and 'X', the relations obtained are given in equations (3.50), (3.51) and (3.52).

$$g_{m2} (v_{in}(s) - v_o(s)) - g_{mb2} v_o(s) + \frac{v_{g4}(s) - v_o(s)}{r_{o2}} = (g_{m1} + g_{m5})v_{g1}(s) + \frac{v_o(s)}{r_{o1}} + \quad (3.50)$$

$$\frac{v_o(s)}{r_{o5}} + sC_L v_o(s)$$

$$g_{m4} v_{gs4}(s) - g_{mb4} v_{s4}(s) - v_{g1}(r_{o4} || 1/g_{m6}) - sC_Y v_{g1}(s) = 0 \quad (3.51)$$

$$g_{m2} (v_{in}(s) - v_o(s)) - g_{mb2} v_o(s) + \frac{v_{g4}(s) - v_o(s)}{r_{o2}} + \left(sC_X + g_{mb3} + \frac{1}{r_{o3}} \right) v_{g4}(s) = 0 \quad (3.52)$$

Since, $g_{mb4} \ll g_{m4}$ and $r_{o4} \ll 1/g_{m6}$ are assumed in equation (3.51), the value of gate voltage of transistor M₁ ($v_{g1}(s)$) is obtained as

$$v_{g1}(s) = \frac{v_{g4}(s)(g_{m4})}{(g_{m4} + sC_Y)} \quad (3.53)$$

Now, using the approximation $g_m r_o \gg 1$ in equation (3.52), the value of gate voltage of transistor M₄ ($v_{g4}(s)$) is given as

$$v_{g4}(s) = \frac{v_o(s) (g_{m2} + g_{mb2}) - v_{in}(s) g_{m2}}{g_{mb3} + sC_X} \quad (3.54)$$

Substituting the values of $v_{g1}(s)$ and $v_{g4}(s)$ from equations (3.53) and (3.54) in equation (3.50), the transfer function ($A_v(s)$) is expressed in equation (3.55).

$$A_v(s) = \frac{v_o(s)}{v_{in}(s)} \quad (3.55)$$

$$= \frac{C_X C_Y g_{m2} s^2 + g_{m2} (C_X g_{m4} + C_Y g_{mb3}) s + g_{m2} g_{m4} (g_{mb3} + g_{m1} + g_{m5})}{C_X C_Y C_L s^3 + \left(\frac{C_X C_L g_{m4}}{g_{m2} C_X C_Y +} \right) s^2 + \left(\frac{C_L g_{mb3} g_{m4}}{C_X g_{m2} g_{m4} + C_Y g_{m2} g_{mb3}} \right) s^1 + g_{m2} g_{m4} \left(\frac{g_{mb3} + g_{m1} + g_{m5}}{g_{m5}} \right)}$$

where $g'_{m2} = g_{m2} + g_{mb2}$.

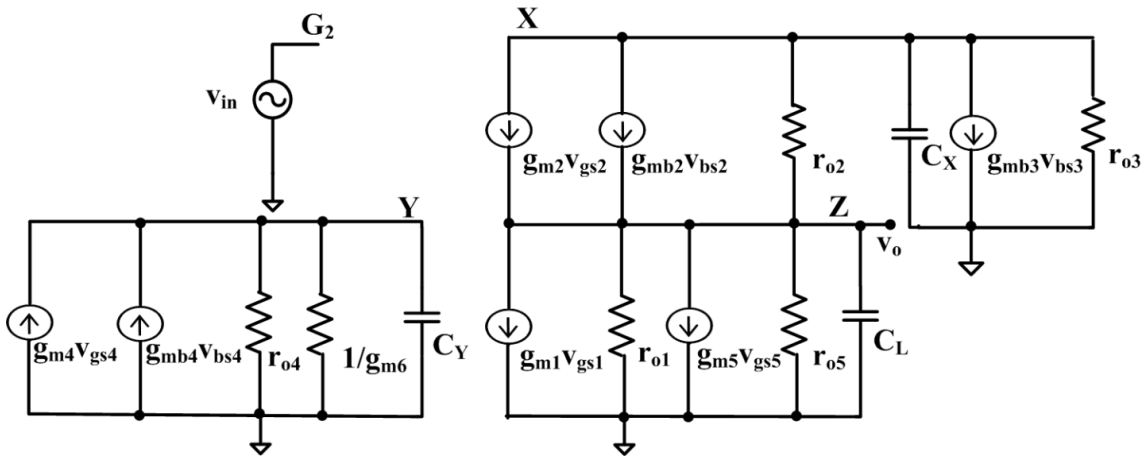


Figure 3.9 High-frequency small-signal equivalent model of the proposed class-AB FVF cell-II to calculate the transfer function

Substituting $s=0$ in equation (3.55), the DC gain (A_V) of the proposed class-AB FVF cell-II is obtained as

$$A_V = \frac{g_{m2}}{g_{m2} + g_{mb2}} \quad (3.56)$$

3.3.2.3 Stability analysis

To analyze the stability of the proposed class-AB FVF cell-II, the feedback path formed by transistor M_4 between gate of transistor $M_{1,5}$ and drain of transistor M_2 is opened. The input voltage source v_y is applied at the gate of transistor $M_{1,5}$ and output is obtained from the drain of the transistor M_2 . The small-signal equivalent model shown in Figure 3.10 is used to calculate the open-loop voltage gain.

Applying KCL at node 'Z' and assuming $g_m r_o \gg 1$, we get

$$\frac{v_z}{v_y} = -\frac{(g_{m1} + g_{m5})}{g_{m2} + g_{mb2}} \quad (3.57)$$

Applying KCL at node 'X' and assuming $g_m r_o \gg 1$, we get

$$\frac{v_z}{v_x} = \frac{g_{mb3}}{g_{m2} + g_{mb2}} \quad (3.58)$$

Using equations (3.57) and (3.58), the open-loop voltage gain (A_{ol}) of the proposed class-AB FVF cell-II is given as

$$|A_{ol}| = \left| \frac{v_x}{v_y} \right| = \frac{g_{m1} + g_{m5}}{g_{mb3}} \quad (3.59)$$

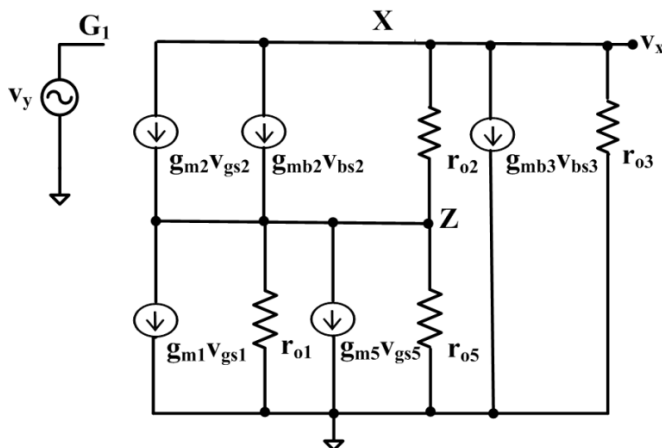


Figure 3.10 Small-signal equivalent model of the proposed class-AB FVF cell-II to calculate the open-loop voltage gain

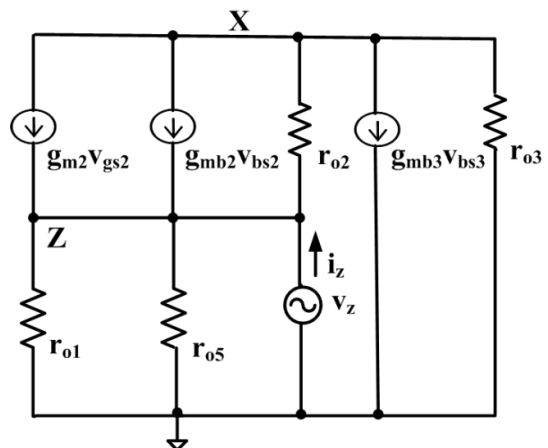


Figure 3.11 Small-signal equivalent model of the proposed class-AB FVF cell-II to calculate the open-loop resistance at node 'Z'

The open-loop resistance at node 'X' (R_{olx}) can be written as

$$R_{olx} = 1/g_{mb3} || g_{m2}r_{o2}(r_{o1}||r_{o5}) \cong 1/g_{mb3}; \text{ since } 1/g_{mb3} \ll g_{m2}r_{o2}(r_{o1}||r_{o5}) \quad (3.60)$$

The open-loop resistance at node 'Z' is calculated using the small-signal equivalent model shown in Figure 3.11. Applying KCL at node 'X' we get

$$v_z \left(g_{m2} + g_{mb2} + \frac{1}{r_{o2}} \right) = v_x \left(\frac{1}{r_{o2}} + \frac{1}{r_{o3}} + g_{mb3} \right) \quad (3.61)$$

By applying KCL at node 'Z', we get

$$i_z = v_z \left(g_{m2} + g_{mb2} + \frac{1}{r_{o1}} + \frac{1}{r_{o2}} + \frac{1}{r_{o5}} \right) - \frac{v_x}{r_{o2}} \quad (3.62)$$

Using equations (3.61) and (3.62), the open-loop resistance at node 'Z' (R_{olz}) is given as

$$R_{olz} = \frac{1}{g_{m2} + g_{mb2}} \quad (3.63)$$

In equation (3.63), it is assumed that $g_m r_o \gg 1$, $\frac{1}{r_{o2}} + \frac{1}{r_{o3}} \gg g_{mb3}$ and $r_{o2} \gg r_{o3}$.

Now, the two poles w_{px} and w_{pz} at nodes 'X' and 'Z' are given in equations (3.64) and (3.65), respectively.

$$w_{px} = \frac{1}{R_{olx}C_x} \quad (3.64)$$

$$w_{pz} = \frac{1}{R_{olz}C_L} \quad (3.65)$$

For the capacitive loads $C_L < 30$ pF, the pole at node 'X' is dominant and the pole at node 'Z' is non-dominant. Using equations (3.59), (3.60) and (3.64), the gain-bandwidth product (GBW) is calculated as

$$GBW = \frac{g_{m1} + g_{m5}}{C_x} \quad (3.66)$$

To ensure the stability of the proposed class-AB FVF cell-II, the condition $w_{pz} \geq GBW$ is expressed in equation (3.67) by using equations (3.63), (3.65) and (3.66).

$$C_L \leq \frac{(g_{m2} + g_{mb2})}{g_{m1} + g_{m5}} C_x \quad (3.67)$$

The condition given in equation (3.67) can be easily maintained by using a compensation capacitor C_c at node 'X'.

For the large capacitive loads $C_L \geq 30$ pF, the dominant pole exists at node 'Z' and non-dominant pole exists at node 'X'. Using equations (3.59), (3.63) and (3.65), the GBW is given as

$$GBW = \frac{(g_{m1} + g_{m5})(g_{m2} + g_{mb2})}{g_{mb3}C_L} \quad (3.68)$$

Using equations (3.59), (3.63) and (3.67), the stability condition $w_{px} \geq \text{GBW}$ results in

$$C_L \geq \frac{(g_{m1} + g_{m5})(g_{m2} + g_{mb2})}{(g_{mb3})^2} C_X \quad (3.69)$$

From equation (3.69), it is evident that the compensation capacitor is not required in this case.

3.3.3 Analysis of proposed class-AB FVF cell-III

The large-signal analysis, small-signal analysis and stability analysis of the proposed class-AB FVF cell-III are discussed in this section.

3.3.3.1 Large-signal analysis

Under equilibrium conditions, the transistors of the proposed class-AB FVF cell-III are operating in the saturation region. Using the condition of saturation region operation for the transistors $M_{1,2,3}$, we get

$$V_{DS1,2} \geq V_{DSsat1,2} = V_{GS1,2} - V_{th1,2} \quad (3.70)$$

$$V_{SD3} \geq V_{SDsat3} = V_{SG3} - V_{th3}$$

Using the condition given in equation (3.70) for transistor M_1 , the upper limit of the output voltage (V_o) is given as

$$V_o \leq V_X - V_{DSsat1} \quad (3.71)$$

Similarly, using the condition given in equation (3.70) for transistor M_2 , the lower limit of the V_o is given by

$$V_o \geq V_{DSsat2} = V_{GS2} - V_{th2} \quad (3.72)$$

From equation (3.70), the voltage V_{SDsat3} can be written as

$$V_{SDsat3} = V_{SD3} = V_{DD} - V_X \quad (3.73)$$

Using equations (3.71), (3.72) and (3.73), the output voltage swing (V_{osw}) can be expressed as

$$V_{osw} = V_{DD} - V_{SDsat3} - V_{DSsat2} - V_{DSsat1} \quad (3.74)$$

The lower limit of the input voltage (V_{in}) is calculated by assuming $V_{DS2} = V_{DSsat2}$ and using ON condition of transistor M_1 as

$$V_{in} \geq V_{th1} + V_{DSsat2} \quad (3.75)$$

Using the condition given in equation (3.70) for transistor M_1 and equation (3.73), the maximum value of the V_{in} can be defined as

$$V_{in} \leq V_{DD} - V_{SDsat3} + V_{th1} \quad (3.76)$$

Using equations (3.75) and (3.76), the V_{in} is bounded as

$$V_{th1} + V_{DSsat2} \leq V_{in} \leq V_{DD} - V_{SDsat3} + V_{th1} \quad (3.77)$$

From equation (3.77), the input voltage swing (V_{isw}) is calculated as

$$V_{isw} = V_{DD} - V_{SDsat3} - V_{DSsat2} \quad (3.78)$$

The supply voltage (V_{DD}) requirement of the proposed class-AB FVF cell-III (when the path through the output branch is considered) is $3V_{DSsat}$. But, to obtain the desired output voltage swing the minimum supply voltage (V_{DDmin}) requirement is calculated using equation (3.74) and it is expressed as

$$V_{DDmin} = V_{osw} + V_{SDsat3} + V_{DSsat2} + V_{DSsat1} \quad (3.79)$$

3.3.3.2 Small-signal analysis

The analyses of output resistance and transfer function of the proposed class-AB FVF cell-III using small-signal equivalent models are explained in this section.

3.3.3.2.1 Output resistance

The high-frequency small-signal equivalent model shown in Figure 3.12 is considered for the calculation of output impedance of the proposed class-AB FVF cell-III. The high-frequency small-signal equivalent model has been used to include the effect of negative feedback as the capacitor C_{bat} acts as a short circuit for the frequencies higher than the cut-off frequency f_o ($1/2\pi R_{large}C_{bat}$). In the model, C_{gs1} is the gate-to-source capacitance of transistor M_1 , C_X is the capacitance at node 'X'. and C_L is the load capacitance connected between output and ground. It is assumed that a non-ideal input voltage source of 0 V with an internal source resistance of R_s and a voltage source of $v_o(s)$ which supplies current $i_o(s)$ are connected at the input and output terminals, respectively. In the model, body effects of input transistor M_1 and bulk-driven transistor M_3 are considered using transconductances due to body effect, i.e., g_{mb1} and g_{mb3} , respectively. The transconductance and output resistance of the transistor M_i are represented by g_{mi} and r_{oi} , respectively, where i varies from 1 to 3. Applying KCL at nodes 'Z', 'X' and 'G₁', the relations are obtained as

$$(sC_{gs1} + g_{m1})v_{g1}(s) + i_o(s) = g_{m2}v_X(s) + (g_{m1} + g_{mb1} + sC_{gs1})v_o(s) \quad (3.80)$$

$$g_{m1}v_{g1}(s) + (g_{mb3} + sC_X)v_X(s) = (g_{m1} + g_{mb1})v_o(s) \quad (3.81)$$

$$v_{g1}(s) = \frac{(sC_{gs1}R_s)}{(1 + sC_{gs1}R_s)}v_o(s) \quad (3.82)$$

To obtain equations (3.80), (3.81) and (3.82), it is assumed that $g_{mi}r_{oi} \gg 1$.

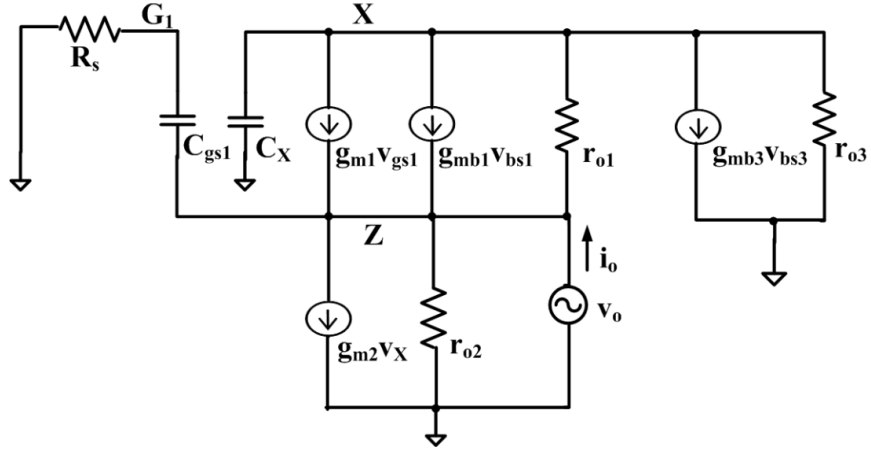


Figure 3.12 Small-signal equivalent model of the proposed class-AB FVF cell-III to calculate the output impedance

Substituting the value of $v_{g1}(s)$ from equation (3.82) in equation (3.80), equation (3.80) is modified as

$$v_X(s) = \frac{(g_{m1} + g_{mb1} + sC_{gs1}R_s g_{mb1})}{(1 + sC_{gs1}R_s)(g_{mb3} + sC_X)} v_o(s) \quad (3.83)$$

Substituting the values of $v_{g1}(s)$ and $v_X(s)$ from equations (3.82) and (3.83), respectively in equation (3.80), the output impedance ($Z_{out}(s)$) is given in equation (3.84).

$$Z_{out}(s) = \frac{C_{gs1}C_X R_s s^2 + (C_{gs1}R_s g_{mb3} + C_X)s + g_{mb3}}{(C_{gs1}C_X + C_{gs1}C_X R_s C_{gs1}g_{mb1})s^2 + (g_{m2}g_{mb1}C_{gs1}R_s + g_{m1}g_{mb3}C_{gs1}R_s + g_{m1}C_X + g_{mb1}C_X + g_{mb3}C_{gs1})s + (g_{m1} + g_{mb1})(g_{m2} + g_{mb3})} \quad (3.84)$$

The expression of output resistance (R_{out}) is given in equation (3.85) if the input voltage is considered as an ideal source and capacitances (C_{gs1} and C_X) are neglected for low frequencies.

$$R_{out} = \frac{g_{mb3}}{(g_{m1} + g_{mb1})(g_{m2} + g_{mb3})} \quad (3.85)$$

3.3.3.2.2 Transfer function

Figure 3.13 depicts the high-frequency small-signal equivalent model of the proposed class-AB FVF cell-III which is used to compute the transfer function.

Assuming $g_{mi}r_{oi} \gg 1$ and applying KCL at nodes 'Z' and 'X', we get

$$g_{m1} v_{in}(s) - g_{m2} v_X(s) = (g_{m1} + g_{mb1} + sC_L) v_o(s) \quad (3.86)$$

$$g_{m1} v_{in}(s) + (g_{mb3} + sC_X) v_X(s) = (g_{m1} + g_{mb1}) v_o(s) \quad (3.87)$$

Substituting the value of $v_X(s)$ from equation (3.87) in equation (3.86), the expression for transfer function ($A_v(s)$) of the proposed class-AB FVF cell-III is obtained as

$$A_v(s) = \frac{v_o(s)}{v_{in}(s)} = \frac{\left(1 + \frac{sC_X g_{m1}}{a}\right) \frac{a}{C_X C_L}}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (3.88)$$

where

$$a = g_{m1}g_{mb3} + g_{m1}g_{m2}; \quad 2\xi\omega_n = \frac{g_{mb3}}{C_X} + \frac{(g_{m1}+g_{mb1})}{C_L}; \quad \text{and } \omega_n^2 = \frac{g_{mb3}(g_{m1}+g_{mb1})+g_{m2}(g_{m1}+g_{mb1})}{C_X C_L}.$$

From equation (3.88), it is observed that the DC gain (A_v) of the proposed class-AB FVF cell-III is $A_v = g_{m1}/(g_{m1} + g_{mb1})$ (for $s = 0$).

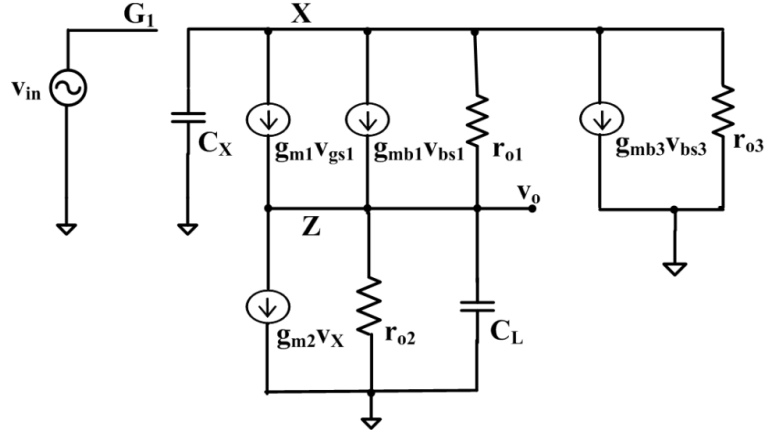


Figure 3.13 High-frequency small-signal equivalent model of the proposed class-AB FVF cell-III to calculate the transfer function

3.3.3.3 Stability analysis

The stability of the proposed class-AB FVF cell-III has been analyzed by opening the feedback path formed by capacitor C_{bat} between the drain of transistor M_1 and the gate of transistor M_2 . The input voltage source v_y is applied at the gate of transistor M_2 and output is obtained from the drain of transistor M_1 (node 'Z'). The small-signal equivalent model shown in Figure 3.14 is used to calculate the open-loop voltage gain. Applying KCL at node 'Z' and assuming $g_m r_o \gg 1$, we get

$$\frac{v_z}{v_y} = -\frac{g_{m2}}{g_{m1} + g_{mb1}} \quad (3.89)$$

Applying KCL at node 'X' and assuming $g_m r_o \gg 1$, the ratio $\frac{v_x}{v_z}$ can be written as

$$\frac{v_x}{v_z} = \frac{g_{m1} + g_{mb1}}{g_{mb3}} \quad (3.90)$$

Using equations (3.89) and (3.90), the open-loop voltage gain (A_{ol}) of the proposed class-AB FVF cell-III is given as

$$|A_{ol}| = \left| \frac{v_x}{v_y} \right| = \frac{g_{m2}}{g_{mb3}} \quad (3.91)$$

The open-loop resistance at node 'X' (R_{olx}) can be expressed as

$$R_{olx} = 1/g_{mb3} \parallel g_{m1}r_{o1}r_{o2} \cong 1/g_{mb3}; \text{ since } 1/g_{mb3} \ll g_{m1}r_{o1}r_{o2} \quad (3.92)$$

The open-loop resistance at node 'Z' is calculated using the small-signal equivalent model shown in Figure 3.15. Applying KCL at node 'X' and assuming $g_m r_o \gg 1$, we get

$$v_z(g_{m1} + g_{mb1}) = v_x \left(\frac{1}{r_{o1}} + \frac{1}{r_{o3}} + g_{mb3} \right) \quad (3.93)$$

Applying KCL at node 'Z' and assuming $g_m r_o \gg 1$, we get

$$i_z = v_z(g_{m1} + g_{mb1}) - \frac{v_x}{r_{o1}} \quad (3.94)$$

Using equations (3.93) and (3.94), the open-loop resistance at node 'Z' (R_{olz}) is given as

$$R_{olz} = \frac{1}{g_{m1} + g_{mb1}} \quad (3.95)$$

Equation (3.95) has been obtained by assuming $\frac{1}{r_{o1}} + \frac{1}{r_{o3}} \gg g_{mb3}$ and $r_{o1} \gg r_{o3}$.

It is observed that there are two poles w_{px} and w_{pz} at node 'X' and node 'Z', respectively which are expressed in equations (3.96) and (3.97).

$$w_{px} = \frac{1}{R_{olx}C_x} \quad (3.96)$$

$$w_{pz} = \frac{1}{R_{olz}C_L} \quad (3.97)$$

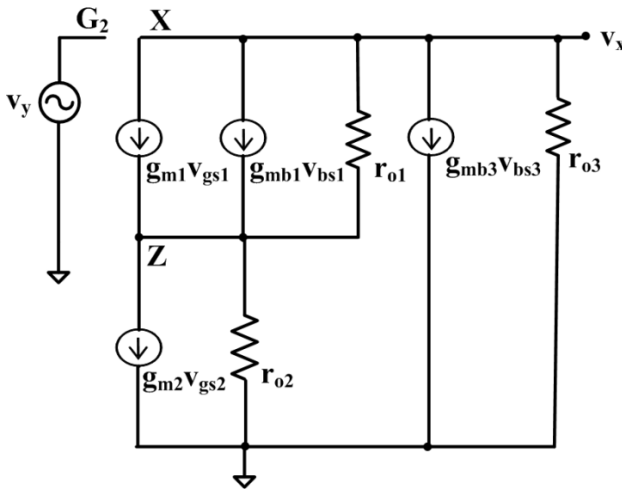


Figure 3.14 Small-signal equivalent model of the proposed class-AB FVF cell-III to calculate the open-loop voltage gain

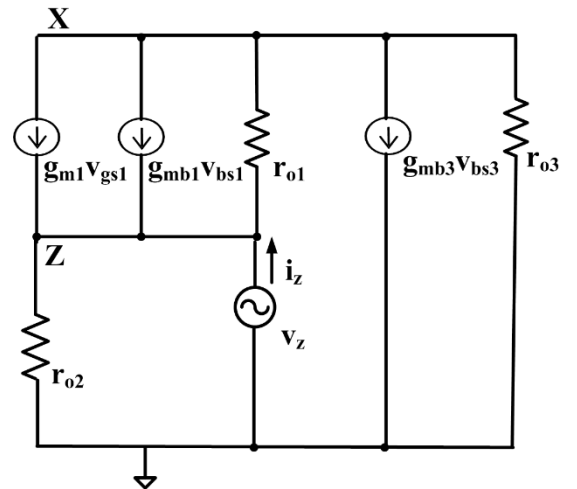


Figure 3.15 Small-signal equivalent model of the proposed class-AB FVF cell-III to calculate the open-loop resistance at node 'Z'

For the capacitive loads $C_L < 30$ pF, the pole at node 'X' is dominant and the pole at node 'Z' is non-dominant. Using equations (3.91), (3.92) and (3.96), the gain-bandwidth product (GBW) is given as

$$GBW = \frac{g_{m2}}{C_x} \quad (3.98)$$

To ensure the stability of the proposed class-AB FVF cell-III, the condition $w_{pz} \geq GBW$ results in equation (3.99) by using equations (3.95), (3.97) and (3.98).

$$C_L \leq \frac{(g_{m1} + g_{mb1})}{g_{m2}} C_x \quad (3.99)$$

The condition given in equation (3.99) can be easily maintained by using a compensation capacitor C_C at node 'X'. For large capacitive loads $C_L \geq 30$ pF, the dominant pole exists at node 'Z' and the non-dominant pole exists at node 'X'. The GBW is given in equation (3.100) by using equations (3.91), (3.95) and (3.97).

$$GBW = \frac{g_{m2}(g_{m1} + g_{mb1})}{g_{mb3}C_L} \quad (3.100)$$

Using equations (3.92), (3.96) and (3.100), the stability condition $w_{px} \geq GBW$ results in equation (3.101) as

$$C_L \geq \frac{g_{m2}(g_{m1} + g_{mb1})}{(g_{mb3})^2} C_x \quad (3.101)$$

From equation (3.101), it is evident that the compensation capacitor is not required in this case.

3.3.4 Analysis of proposed class-AB FVF cell-IV

This section addresses large-signal analysis, small-signal analysis and stability analysis of the proposed class-AB FVF cell-IV.

3.3.4.1 Large-signal analysis

For the analysis of input and output voltage swings of the proposed class-AB FVF cell-IV, all the transistors are assumed under quiescent conditions and operating in the saturation region. Using the saturation condition for the transistors M_1 and M_2 , the maximum and minimum values of output voltage (V_o) are given in equations (3.102) and (3.103), respectively.

$$V_o \leq V_{G4} - V_b - V_{DSsat1} \quad (3.102)$$

$$V_o \geq V_{G2} - V_{th2} \quad (3.103)$$

Using equations (3.102) and (3.103), the V_o is bounded as

$$V_{G2} - V_{th2} \leq V_o \leq V_{G4} - V_b - V_{DSsat1} \quad (3.104)$$

From equation (3.104), the maximum output voltage swing (V_{osw}) is obtained as

$$V_{osw} = V_{GS4} + V_{th2} - V_b - V_{DSsat1} \quad (3.105)$$

Using the saturation condition for the transistor M_1 , the maximum value of input voltage (V_{in}) is defined as

$$V_{in} \leq V_{D1} + V_{GS1} - V_{DSsat1} \quad (3.106)$$

The drain voltage (V_{D1}) of transistor M_1 can be written as

$$V_{D1} = V_{GS4} + V_{GS2} - V_b \quad (3.107)$$

Substituting the value of V_{D1} from equation (3.107) in equation (3.106), the maximum value of V_{in} is given as

$$V_{in} \leq V_{GS4} + V_{GS2} - V_b + V_{GS1} - V_{DSsat1} \quad (3.108)$$

The minimum value of V_{in} can be calculated by assuming the ON condition for the transistor M_1 as

$$V_{in} \geq V_{th1} + V_{DSsat2} \quad (3.109)$$

Using equations (3.108) and (3.109), the V_{in} is bounded as

$$V_{th1} + V_{DSsat2} \leq V_{in} \leq V_{GS4} + V_{GS2} - V_b + V_{GS1} - V_{DSsat1} \quad (3.110)$$

From equation (3.110), the maximum input voltage swing (V_{isw}) is calculated as

$$V_{isw} = V_{GS4} + V_{th2} - V_b \quad (3.111)$$

The supply voltage (V_{DD}) requirement of the proposed class-AB FVF cell-IV (when the path through the output branch is considered) is given as

$$V_{DD} = V_{SDsat3} + V_b + V_{DSsat1} + V_{DSsat2} \quad (3.112)$$

The V_{DD} requirement of the proposed class-AB FVF cell-IV can also be expressed in equation (3.113) for the path through folding transistor M_5 .

$$V_{DD} = V_{SG5} - V_b + V_{GS4} + V_{GS2} \quad (3.113)$$

From equations (3.112) and (3.113), it is clear that the minimum power supply voltage (V_{DDmin}) requirement of the proposed class-AB FVF cell-IV can be expressed by equation (3.113).

3.3.4.2 Small-signal analysis

In this section, output resistance and voltage gain analyses of the proposed class-AB FVF cell-IV are presented using small-signal equivalent models.

3.3.4.2.1 Output resistance

To calculate the output resistance, a small-signal equivalent model of the proposed class-AB FVF cell-IV is shown in Figure 3.16. For the computation of the output resistance, the input

terminal (G_1) is connected to the ground potential and a voltage source v_o is connected at the output terminal which supplies a current i_o .

Applying KCL at node 'W', the relation is obtained as

$$v_o \left(g_{m1} + g_{mb1} + \frac{1}{r_{o1}} \right) = v_{g5} \left(\frac{1}{r_{o1}} + \frac{1}{R_b + r_{o3}} \right) \quad (3.114)$$

Assuming $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}$, $R_b \ll r_{o3}$ and $g_m r_o \gg 1$, equation (3.114) is simplified as

$$v_{g5} = (g_{m1} + g_{mb1}) \frac{r_{o1}}{2} v_o \quad (3.115)$$

Applying KCL at node 'Y', we get

$$v_{g2} = \frac{g_{m4} v_{g4}}{g_{m4} + g_{mb4} + (r_{o4} \parallel 1/g_{m6})^{-1}} \quad (3.116)$$

Assuming $g_m r_o \gg 1$ in equation (3.116), the gate voltage at transistor M_2 (v_{g2}) is given as

$$v_{g2} = \frac{g_{m4} v_{g4}}{g_{m4} + g_{mb4} + g_{m6}} \quad (3.117)$$

The gate voltage of transistor M_4 (v_{g4}) can be written as

$$v_{g4} = \frac{r_{o3} v_{g5}}{r_{o3} + R_b} \quad (3.118)$$

Substituting the value of v_{g4} from equation (3.118) in equation (3.117), voltage v_{g2} is given as

$$v_{g2} = \frac{g_{m4} r_{o3} v_{g5}}{(g_{m4} + g_{mb4} + g_{m6})(r_{o3} + R_b)} \quad (3.119)$$

Applying KCL at node 'Z' and assuming $g_m r_o \gg 1$, we get

$$i_o - v_o(g_{m1} + g_{mb1}) = g_{m5} v_{g5} + g_{m2} v_{g2} \quad (3.120)$$

Using equations (3.115), (3.119) and (3.120), the expression for output resistance (R_{out}) is given in equation (3.121) by assuming that $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}$ and $g_{m4} \approx g_{m4} + g_{mb4}$.

$$R_{out} = \frac{2(g_{m4} + g_{m6})}{(g_{m1} + g_{mb1})(g_{m2} g_{m4} r_{o1} + g_{m5} (g_{m4} + g_{m6}) r_{o1} + 2(g_{m4} + g_{m6}))} \quad (3.121)$$

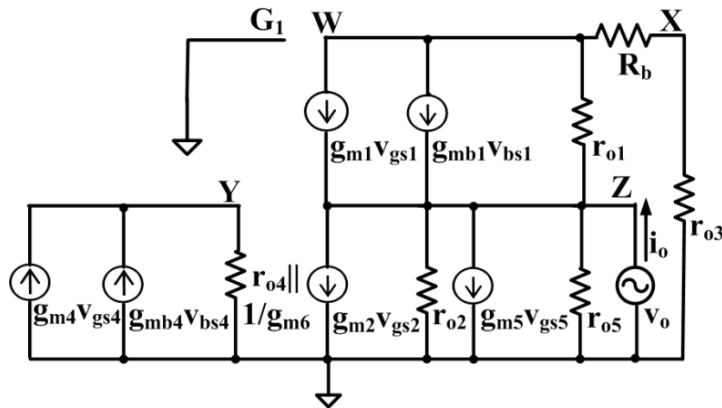


Figure 3.16 Small-signal equivalent model of the proposed class-AB FVF cell-IV to calculate the output resistance

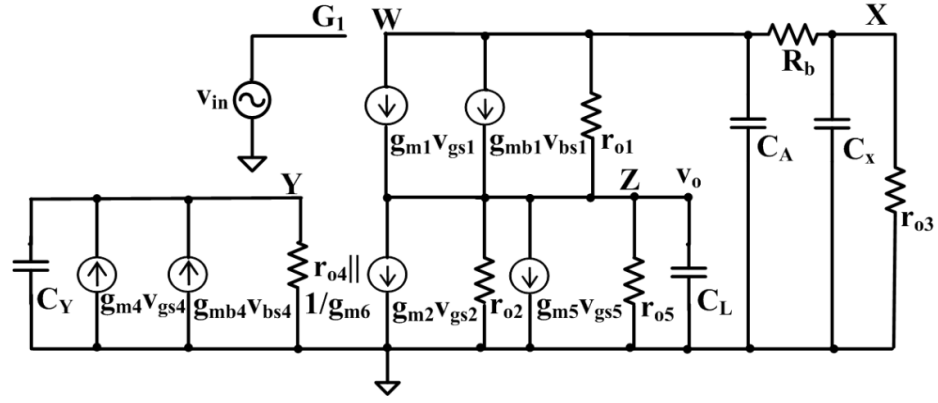


Figure 3.17 High-frequency small-signal equivalent model of the proposed class-AB FVF cell-IV to calculate the transfer function

3.3.4.2.2 Transfer function

The high-frequency small-signal equivalent model of the proposed class-AB FVF cell-IV shown in Figure 3.17 is used to calculate the transfer function. Applying KCL at node ‘Z’ and assuming $g_m r_o \gg 1$, we get

$$g_{m1}v_{in}(s) - (g_{m1} + g_{mb1} + sC_L)v_o(s) = g_{m5}v_{g5}(s) + g_{m2}v_{g2}(s) \quad (3.122)$$

Applying KCL at node ‘W’, we get

$$v_{g5}(s) = \frac{[(g_{m1} + g_{mb1})r_{o1}v_o(s) - g_{m1}r_{o1}v_{in}(s)](1 + sC_XR_b)}{sC_Xr_{o1} + 2 + sC_Ar_{o1}(1 + sC_XR_b)} \quad (3.123)$$

In equation (3.123), it is assumed that $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}$, $R_b \ll r_{o3}$ and $g_m r_o \gg 1$.

On applying KCL at node ‘Y’ and assuming $g_m r_o \gg 1$, the gate voltage ($v_{g2}(s)$) of transistor M_2 is given in equation (3.124).

$$v_{g2}(s) = \frac{g_{m4}v_{g4}(s)}{g_{m4} + g_{mb4} + g_{m6} + sC_Y} \quad (3.124)$$

Applying KCL at node ‘X’, the gate voltage ($v_{g4}(s)$) of transistor M_4 is given as

$$v_{g4}(s) = \frac{v_{g5}(s)}{1 + sC_XR_b} \quad (3.125)$$

Substituting the value of $v_{g4}(s)$ from equation (3.125) in equation (3.124), the voltage $v_{g2}(s)$ is given as

$$v_{g2}(s) = \frac{g_{m4}v_{g5}(s)}{(g_{m4} + g_{mb4} + g_{m6} + sC_Y)(1 + sC_XR_b)} \quad (3.126)$$

Using equations (3.122), (3.123) and (3.126), the expression of the transfer function ($A_v(s)$) is given in equation (3.127).

$$A_V(s) = \frac{v_o(s)}{v_{in}(s)} = \quad (3.127)$$

$$\frac{\left[C_X C_A C_Y R_b s^3 + \left(\frac{C_X C_A g_{m4a} R_b + C_A C_Y + C_X C_Y g_{m5} R_b}{C_A g_{m4a} + C_Y g_{m5}} \right) s^2 + \left(\frac{C_X g_{m4a} + C_X g_{m5} g_{m4a} R_b}{C_A g_{m4a} + C_Y g_{m5}} \right) s^1 + (g_{m4a} g_{m5} + g_{m2} g_{m4}) \right] g_{m1} r_{o1}}{C_X C_A C_Y C_L r_{o1} R_b s^4 + \left[\frac{C_L C_Y r_{o1} (C_X + C_A) + C_A C_X R_b r_{o1} (C_Y g'_{m1} + C_L g_{m4a})}{C_X R_b g'_{m1} r_{o1} (C_A g_{m4a} + C_Y g_{m5}) + C_A C_Y g'_{m1} r_{o1}} \right] s^3 + \left[\frac{C_L g_{m4a} r_{o1} (C_X + C_A) + 2 C_L C_Y + g_{m4a} g'_{m1} r_{o1} (C_X + C_A) + 2 C_L g_{m4a} + g_{m5} g'_{m1} r_{o1} (C_Y + C_X g_{m4a} R_b)}{g_{m4a} g'_{m1} r_{o1} (C_X + C_A) + 2 C_L g_{m4a} + g_{m5} g'_{m1} r_{o1} (C_Y + C_X g_{m4a} R_b)} \right] s^2 + g'_{m1} r_{o1} (g_{m4a} g_{m5} + g_{m2} g_{m4})} s^2 +$$

where $g'_{m1} = g_{m1} + g_{mb1}$ and $g_{m4a} = g_{m4} + g_{m6}$.

Substituting $s = 0$ in equation (3.127), the DC gain (A_V) of the proposed class-AB FVF cell-IV is obtained as

$$A_V = \frac{g_{m1}}{g_{m1} + g_{mb1}} \quad (3.128)$$

3.3.4.3 Stability analysis

For the analysis, the feedback paths are opened by breaking the connections of gate terminals of transistors M_2 and M_5 . To calculate the open-loop voltage gain of the proposed class-AB FVF cell-IV, a small-signal equivalent model is shown in Figure 3.18. The test voltage source (v_t) is applied at gate terminals of transistors $M_{2,5}$ and output voltage (v_r) is drawn from the drain terminal of transistor M_3 . Applying KCL at nodes ‘W’ and ‘Z’ (assuming $g_m r_o \gg 1$), the relations are obtained as

$$v_{d1} = \frac{(g_{m1} + g_{mb1})r_{o1}R_b v_z + r_{o1}v_r}{r_{o1} + R_b} \quad (3.129)$$

$$\frac{v_{d1}}{r_{01}} = (g_{m2} + g_{m5})v_t + v_z(g_{m1} + g_{mb1}) \quad (3.130)$$

where v_z is the voltage at node ‘Z’.

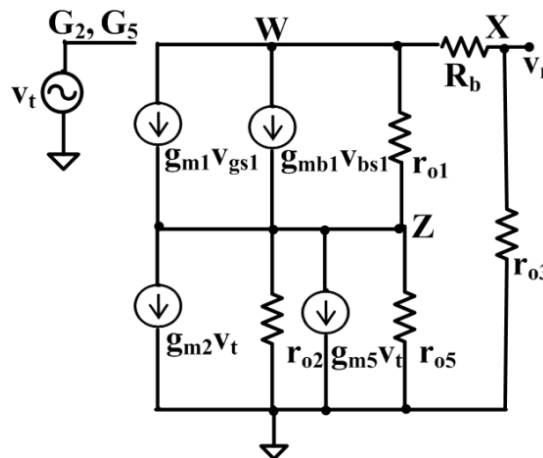


Figure 3.18 Small-signal equivalent model of the proposed class-AB FVF cell-IV to calculate the open-loop voltage gain

Substituting the value of v_z from equation (3.130) in equation (3.129), equation (3.130) is modified as

$$\frac{v_{d1}}{r_{o1}} = (g_{m2} + g_{m5})v_t + \frac{v_{d1}(r_{o1} + R_b) - r_{o1}v_r}{r_{o1}R_b} \quad (3.131)$$

The drain voltage of transistor M_1 (v_{d1}) can be written as

$$v_{d1} = \frac{(r_{o3} + R_b)v_r}{r_{o3}} \quad (3.132)$$

Substituting the value of v_{d1} from equation (3.132) in equation (3.131), the open-loop voltage gain (A_{ol}) is expressed as

$$|A_{ol}| = \left| \frac{v_r}{v_t} \right| = (g_{m2} + g_{m5})r_{o3} \quad (3.133)$$

The small-signal equivalent model shown in Figure 3.19 is used to calculate the open-loop resistance at node 'X' where voltage source v_x connected at node 'X' supplies a current i_x . Using KVL, the voltage v_x can be written as

$$v_x = (i_x - i_{x1})r_{o3} \quad \text{where } i_{x1} = \frac{v_x}{R_{x1}} \quad (3.134)$$

The resistance R_{x1} corresponds to the cascoding structure which is greater than the resistance R_b . So, the resistance R_{x1} can be written as

$$R_{x1} = (g_{m1} + g_{mb1})r_{o1}(r_{o2} || r_{o5}) \quad (3.135)$$

Using equations (3.134) and (3.135), the open-loop resistance at node 'X' (R_{olx}) is given as

$$R_{olx} = \frac{v_x}{i_x} = r_{o3} || ((g_{m1} + g_{mb1})r_{o1}(r_{o2} || r_{o5})) \cong r_{o3}; \quad (3.136)$$

since $r_{o3} \ll (g_{m1} + g_{mb1})r_{o1}(r_{o2} || r_{o5})$.

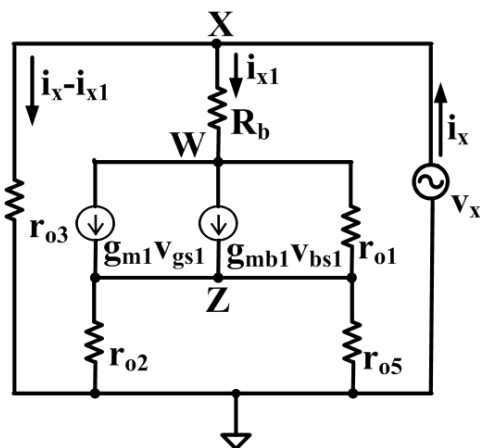


Figure 3.19 Small-signal equivalent model of the proposed class-AB FVF cell-IV to calculate the open-loop resistance at node 'X'

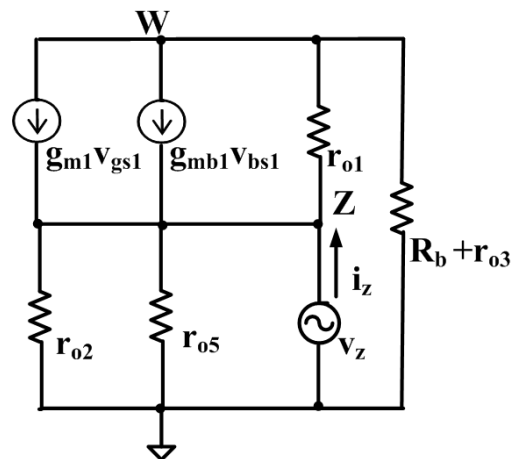


Figure 3.20 Small-signal equivalent model of the proposed class-AB FVF cell-IV to calculate the open-loop resistance at node 'Z'

Using equation (3.136), the pole at node 'X' (w_{px}) is given as

$$w_{px} = \frac{1}{R_{olx}C_x} = \frac{1}{r_{o3}C_x} \quad (3.137)$$

where C_x is the equivalent parasitic capacitance at node 'X'.

To calculate the open-loop resistance at node 'Z', a small-signal equivalent model shown in Figure 3.20 has been used where voltage source v_z connected at node 'Z' supplies a current i_z .

Applying KCL at nodes 'W' and 'Z' (assuming $g_m r_o \gg 1$), we get

$$v_{d1} = \frac{(g_{m1} + g_{mb1})r_{o1}(R_b + r_{o3})v_z}{R_b + r_{o3} + r_{o1}} \quad (3.138)$$

$$i_z + \frac{v_{d1}}{r_{o1}} = v_z(g_{m1} + g_{mb1}) \quad (3.139)$$

Using equations (3.138) and (3.139), the open-loop resistance at node 'Z' (R_{olz}), is given as

$$R_{olz} = \frac{2}{(g_{m1} + g_{mb1})} \quad (3.140)$$

In equation (3.140), it is assumed that $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}, r_{o3}$.

Using equation (3.140), the pole at node 'Z' (w_{pz}) is given as

$$w_{pz} = \frac{1}{R_{olz}C_L} = \frac{g_{m1} + g_{mb1}}{2C_L} \quad (3.141)$$

where C_L is the load capacitance.

For the capacitive loads $C_L < 30\text{pF}$, the dominant pole exists at node 'X' and non-dominant pole exists at node 'Z'. The open-loop gain and dominant pole given in equations (3.133) and (3.137), respectively define the gain-bandwidth product (GBW) of the proposed class-AB FVF cell-IV as

$$\text{GBW} = A_{ol}w_{px} = \frac{g_{m5} + g_{m2}}{C_x} \quad (3.142)$$

To maintain the stability condition, the non-dominant pole must follow the relationship $w_{pz} \geq \text{GBW}$ given in equation (3.143) which is obtained using equations (3.141) and (3.142).

$$C_x \geq \frac{2(g_{m5} + g_{m2})}{(g_{m1} + g_{mb1})} C_L \quad (3.143)$$

The stability condition given in equation (3.143) can be easily maintained by adding a compensation capacitor C_c at node 'X' for capacitive loads $C_L < 30\text{pF}$.

Now, for the large capacitive loads $C_L \geq 30\text{pF}$, the dominant pole exists at node 'Z' and non-dominant pole exists at node 'X'. Using open-loop gain and dominant pole given in equations (3.133) and (3.141), respectively the GBW can be written as

$$\text{GBW} = A_{ol}w_{pz} = \frac{(g_{m1} + g_{mb1})(g_{m5} + g_{m2})r_{o3}}{2C_L} \quad (3.144)$$

In this case, the stability condition $w_{px} \geq \text{GBW}$ results in equation (3.145) which is obtained using equations (3.137) and (3.144).

$$C_L \geq \frac{(g_{m1} + g_{mb1})(g_{m5} + g_{m2})r_{o3}^2 C_x}{2} \quad (3.145)$$

From equation (3.145), it is evident that the compensation capacitor is not required for the capacitive loads $C_L \geq 30\text{pF}$.

3.4 Simulation results of proposed FVF cells

This section presents the post-layout simulation results of the proposed FVF cells. The proposed FVF cells are designed using BSIM3V3 180 nm CMOS technology and simulated using spectre in the Cadence Virtuoso Analog Design Environment. The physical layouts of the proposed FVF cells are designed using Cadence Virtuoso Layout XL editor in 180 nm CMOS technology. To fairly compare the proposed FVF cells, three figures of merit (FOMs) have been used [52]. The FOM_1 is defined as $\text{FOM}_1 = \min(I_o^{\text{Max}+}, I_o^{\text{Max}-})/I_{Q\text{total}}$, where $I_o^{\text{Max}+}$ is the maximum output sourcing current, $I_o^{\text{Max}-}$ is the maximum output sinking current and $I_{Q\text{total}}$ is the total quiescent current. FOM_1 is a unitless quantity. The FOM_2 is defined as $\text{FOM}_2 = (\text{BW} * C_L)/P^Q$, where BW is the bandwidth, C_L is the load capacitance and P^Q is the quiescent power. The FOM_2 has units of $(\text{MHz} * \text{pF})/\mu\text{W}$. The FOM_1 decides the speed limitation for large signals and FOM_2 restricts the speed of small signals. Therefore, FOM_3 corresponds to the geometric mean of FOM_1 and FOM_2 , i.e. $\text{FOM}_3 = \sqrt{\text{FOM}_1 \text{FOM}_2}$, where the units of FOM_3 are $[(\text{MHz} * \text{pF})/\mu\text{W}]^{1/2}$. The higher values of FOM_1 , FOM_2 and FOM_3 confirm the better performance of the circuit.

3.4.1 Simulation results of proposed class-AB FVF cell-I

The proposed class-AB FVF cell-I is biased with current (I_b) of 8 μA . The supply voltage (V_{DD}) calculated using equation (3.9) is obtained as 1.16 V and it is selected as 1.2 V. The performance of the proposed class-AB FVF cell-I has been observed using load capacitances (C_L) of 1 pF and 50 pF. The aspect ratios (W/L) of transistors used to design the proposed class-AB FVF cell-I are listed in Table 3.1.

The physical layout of the proposed class-AB FVF cell-I shown in Figure 3.21 occupies an area of 25.44 $\mu\text{m} \times 28.90 \mu\text{m}$. The current source I_b has been implemented using NMOS transistor M_9 in the layout.

Table 3.1 Aspect ratios of transistors used to design the proposed class-AB FVF cell-I

Transistor	W/L($\mu\text{m}/\mu\text{m}$)
M ₁	50/0.72
M ₂	50/0.72
M ₃	47/0.36
M ₄	6.84/0.54
M ₅	3.42/0.54
M ₆	8/0.54
M ₇	10/0.54
M ₈	10/0.54
M ₉	3/0.54

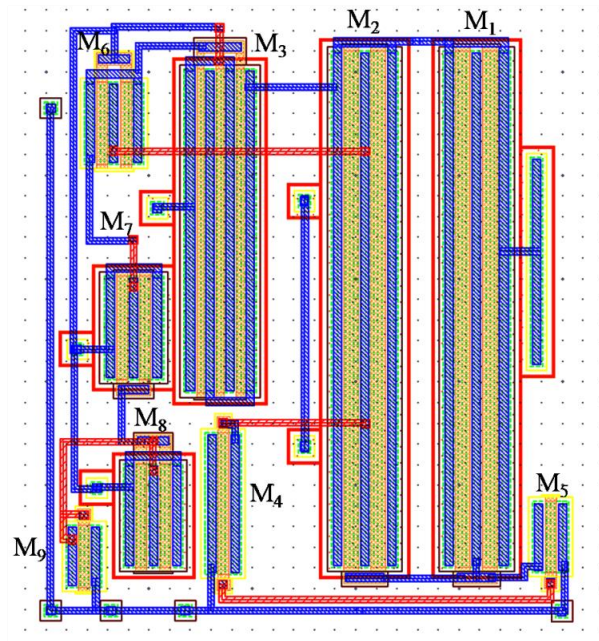


Figure 3.21 Physical layout of the proposed class-AB FVF cell-I

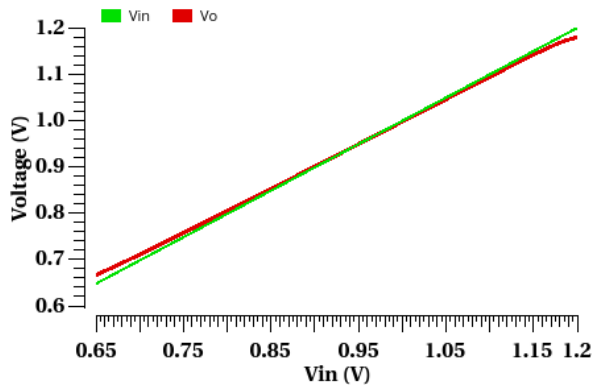


Figure 3.22 Transfer characteristics of the proposed class-AB FVF cell-I

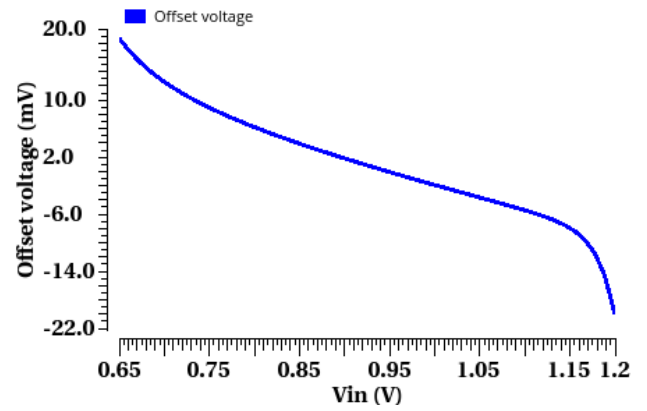


Figure 3.23 Offset voltage of the proposed class-AB FVF cell-I

The transfer characteristics of the proposed class-AB FVF cell-I are shown in Figure 3.22. The plot shows the variations of output voltage when the input voltage is varied in the range of 0.65 V to 1.2 V. From the plots, the output and input voltage swings are observed as 0.511 V and 0.55 V, respectively. Using equations (3.5) and (3.6), both the output and input voltage swings are calculated as 0.51 V and it is clear that both the theoretical and simulated values are approximately matched. The plot of the offset voltage between the output voltage and the input voltage when the input voltage is varied from 0.65 V to 1.2 V is shown in Figure 3.23. From the plot, it is observed that the offset voltage of the proposed class-AB FVF cell-I is 19.6 mV.

The frequency response of the proposed class-AB FVF cell-I is shown in Figure 3.24. From the figure, the gain is obtained as 0.96 while bandwidths are obtained as 52.24 MHz and 3.12 MHz for the load capacitances of 1 pF and 50 pF, respectively. The closed-loop voltage gain at low frequency is also calculated using equation (3.21) as unity and it is clear that both the theoretical and simulated values are approximately matched.

The output resistance versus frequency plot of the proposed class-AB FVF cell-I is shown in Figure 3.25. From the figure, it can be seen that the output resistance is 231 Ω for the frequency range of 0 to 1 MHz. Using equation (3.16), the output resistance is calculated as 235 Ω and it is clear that both the theoretical and simulated values are approximately matched.

The transient analysis for a square input voltage of amplitude 0.65 V to 1.2 V at a frequency of 1 MHz is shown in Figure 3.26. The symmetrical slew rates (SR+/SR-) are observed as 53.84 V/ μ s/ 76.8 V/ μ s and 3.34 V/ μ s/ 7.73 V/ μ s for the load capacitances of 1 pF and 50 pF, respectively.

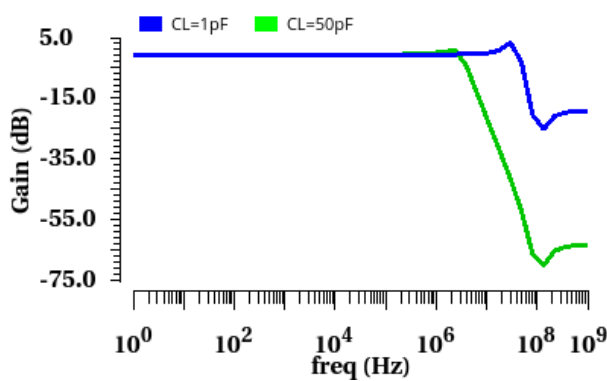


Figure 3.24 Frequency response of the proposed class-AB FVF cell-I

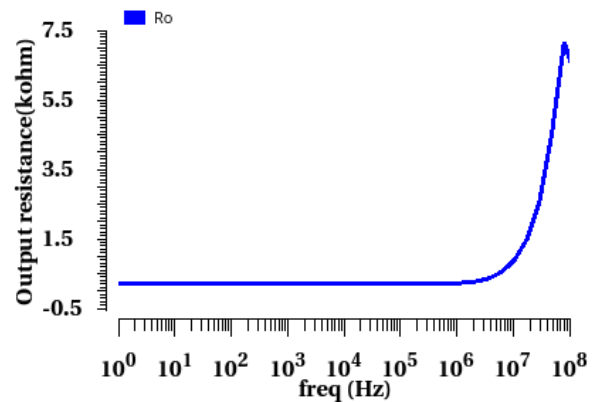


Figure 3.25 Output resistance of the proposed class-AB FVF cell-I

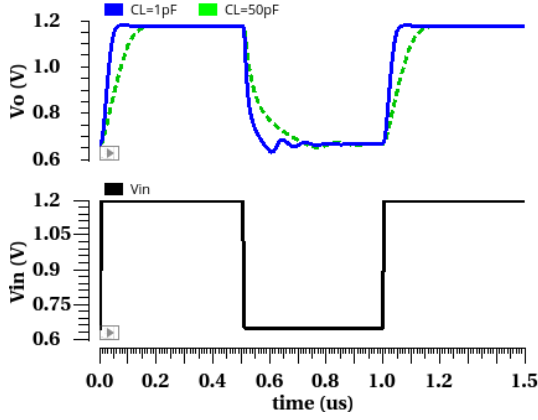


Figure 3.26 Transient response of the proposed class-AB FVF cell-I for a square input pulse

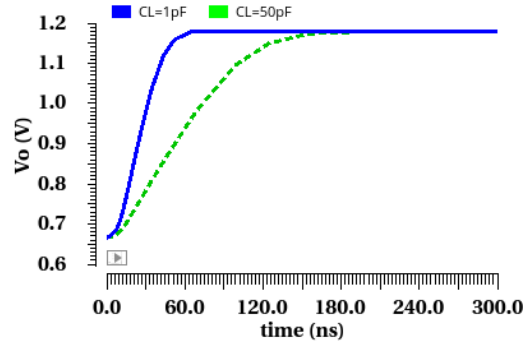


Figure 3.27 Output response of the proposed class-AB FVF cell-I at the rising edge

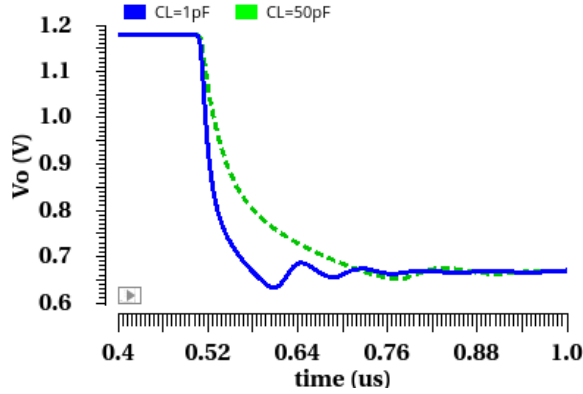


Figure 3.28 Output response of the proposed class-AB FVF cell-I at the falling edge

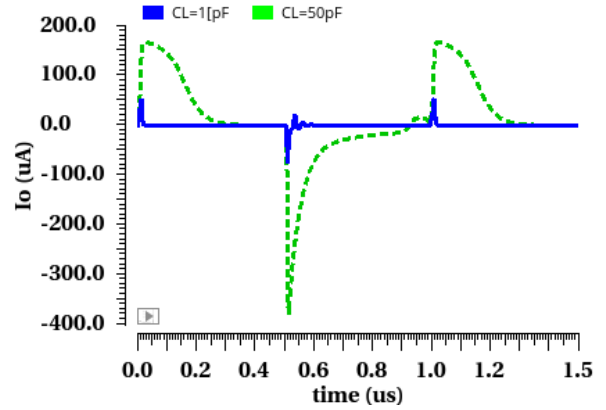


Figure 3.29 Current sourcing and sinking capabilities of the proposed class-AB FVF cell-I

The output responses at the rising edge and falling edge of input voltage are shown in Figures 3.27 and 3.28, respectively. From Figure 3.27, the settling times (2% of the final values) at rising edges are obtained as 66 ns and 150 ns for the load capacitances of 1 pF and 50 pF, respectively. From Figure 3.28, the settling times (2% of the final values) at falling edges are obtained as 145 ns and 250 ns for the load capacitances of 1 pF and 50 pF, respectively.

The current sourcing and sinking capabilities of the proposed class-AB FVF cell-I are shown in Figure 3.29. The current sourcing/sinking capability are obtained as $6.73 I_b / 9.6 I_b$ and $20.89 I_b / 47.43 I_b$ for the load capacitances of 1 pF and 50 pF, respectively. The transient response of proposed class-AB FVF cell-I for a triangular pulse varying from 0.65 V to 1.2 V is shown in Figure 3.30. From the plot, it is observed that the input and output voltage swings are 0.55 V and 0.51 V, respectively.

The input noise spectral density (INSD) of the proposed class-AB FVF cell-I is shown in Figure 3.31. From the figure, it is observed that the INSD is 5.75 nV/sqrt(Hz) at frequency of 100 kHz for the load capacitances of 1 pF and 50 pF.

The total harmonic distortion (THD) versus frequency plot of the proposed class-AB FVF cell-I is shown in Figure 3.32. For THD calculations, a sinusoidal signal of 200 mV peak-to-peak amplitude is applied at the input terminal. The plot shows the variation in THD when the frequency of the input signal is varied from 1 kHz to 1 MHz for the worst-case load capacitance of 50 pF. It is observed that the THD is less than 1% for the frequency range of 1 kHz to 1 MHz. Figure 3.33 shows the variation in THD versus different amplitudes of input signal for a sinusoidal input voltage with offset voltage 0.9 V and 100 kHz frequency for the worst-case load capacitance of 50 pF. From the plot, THD is observed as less than 1 %.

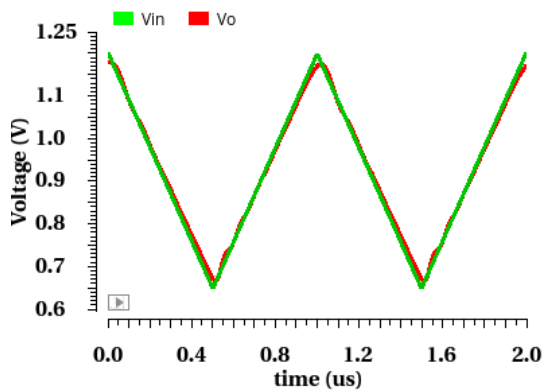


Figure 3.30 Transient response of proposed class-AB FVF cell-I for a triangular input pulse

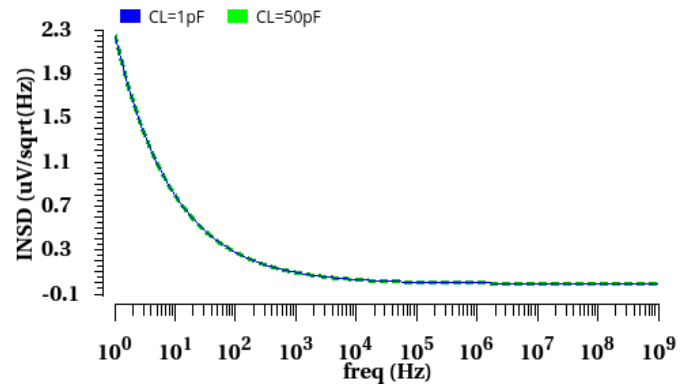


Figure 3.31 Input noise spectral density of the proposed class-AB FVF cell-I

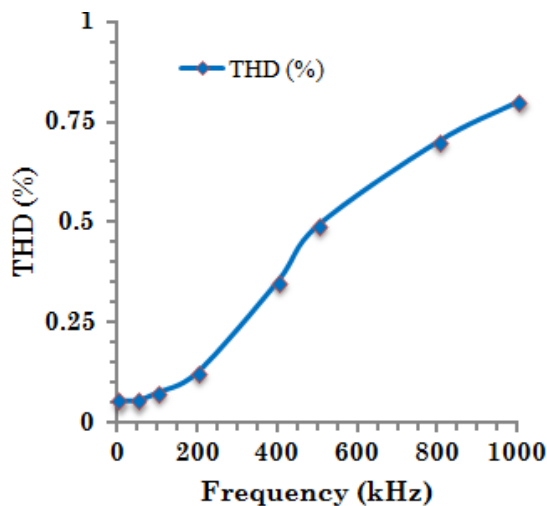


Figure 3.32 THD (%) versus frequency plot of the proposed class-AB FVF cell-I

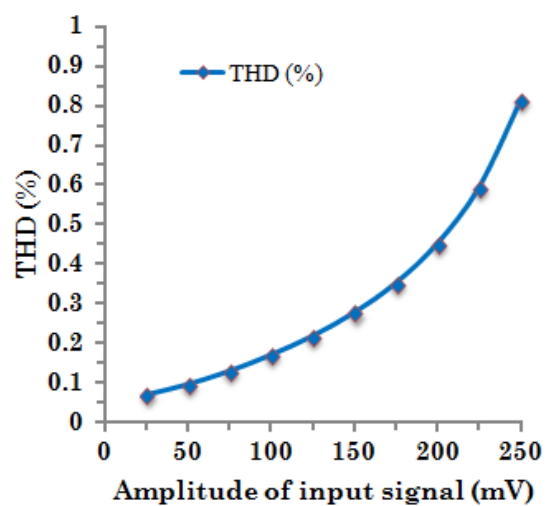


Figure 3.33 THD (%) versus amplitude plot of the proposed class-AB FVF cell-I

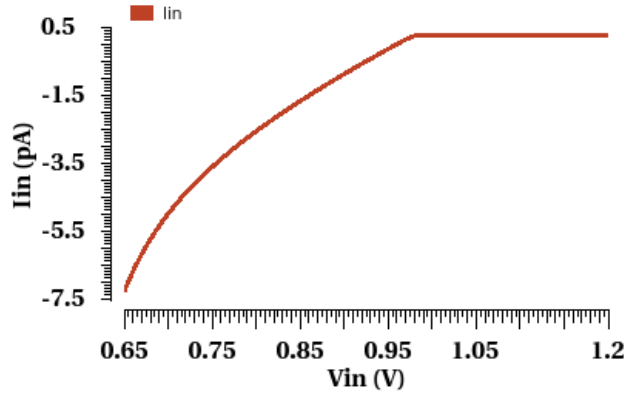


Figure 3.34 Input current plot of the proposed class-AB FVF cell-I

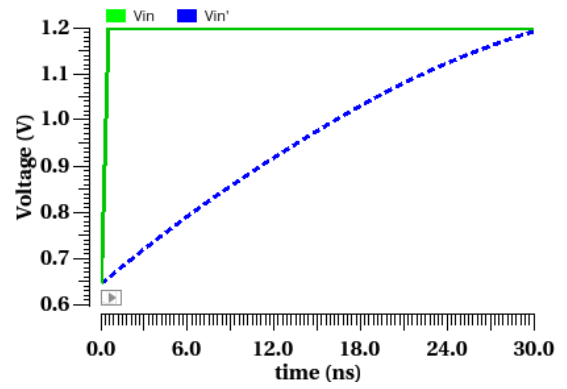


Figure 3.35 Rise time plot of voltage (V'_{in}) at node under the test

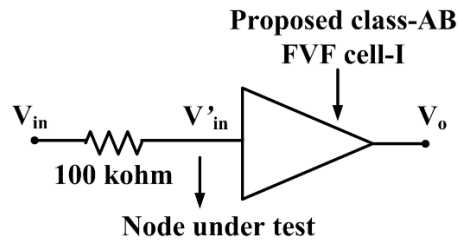


Figure 3.36 Simulation set up to calculate input capacitance of the proposed class-AB FVF cell-I

Since the bulk terminal is used to feed the input voltage, large input current and large input capacitance are not expected to avoid the bulk terminal being forward biased. Figure 3.34 shows the plot of input current for the input voltage varying from 0.65 V to 1.2 V. From the plot, it is observed that input current varies from -7.2 pA to 254 fA, which cannot forward bias the bulk terminal. The plot of the rise time of voltage (V'_{in}) at node under test is shown in Figure 3.35 when V_{in} is varied from 0.65 V to 1.2 V at 1 MHz. To calculate the input capacitance, the setup shown in Figure 3.36 is considered. It is observed that the time constant ($T=RC$) for V'_{in} is 30 ns. So, the input capacitance of the proposed class-AB FVF cell-I is calculated as 300 fF.

The proposed class-AB FVF cell-I has been compared with the FVF cells available in the literature in Table 3.2. The proposed class-AB FVF cell-I offers a voltage gain of 0.96 i.e. approximately equal to one. The proposed class-AB FVF cell-I also shows a symmetrical slew rate. The various structures are compared on the basis of FOMs, which show that the proposed class-AB FVF cell-I offers higher FOM₁ as compared to the reported structures [32-33, 44, 50]. However, the FOM₂ of the proposed class-AB FVF cell-I is higher than the FVF cells [32, 35, 44, 50] but lower than [33]. The FOM₂ is based on the bandwidth, power and load capacitance.

The bandwidth of the proposed class-AB FVF cell-I is limited as the input voltage is given at the bulk terminal. But, the geometric mean of FOM_1 and FOM_2 i.e. FOM_3 of the proposed class-AB FVF cell-I is higher than the reported FVF cells.

Table 3.2 Comparison of the proposed class-AB FVF cell-I with FVF cells available in the literature

References→ Parameters↓	[32]	[33]	[35]	[44]	[50]	Proposed cell-I
Supply voltage (V)	2.7	1.2	1.8	± 1.5	1.5	1.2
Technology (nm)	ALD1106	350	350	500	500	180
Bias current (I_b) (μA)	55	2.5	8	30	50	8
Power (μW)	148.5	3	14.4	225	120	19.2
Input Swing (V)	----	1	----	----	0.7	0.55
Output Swing (V)	----	1 (Offset:10mV)	----	----	0.6	0.511 (Offset:19.6mV)
Gain	----	----	----	----	0.76	0.96
Bandwidth (MHz) @ C_L	2 @280pF	2.8 @10 pF	6 @10pF	6.2 @100pF	15.4 @50pF	52.24@1pF 3.12 @50 pF
R_{out} (Ω)	----	----	----	----	----	231
SR+ (V/ μs) @ C_L	3.75 @280pF	1.9 @10 pF	9.3 @10pF	3.5 @100pF	3.34 @50pF	53.84@1pF 3.34@50pF
SR- (V/ μs) @ C_L	1.82 @280pF	----	13.7 @10pF	4.3 @100pF	4 @50pF	76.8@1pF 7.73@50pF
Sourcing current @ C_L	16.72 I_b @280pF	7.6 I_b @10 pF	11.62 I_b @10pF	26 I_b @100pF	3.34 I_b @50pF	6.73 I_b @1pF 20.89 I_b @50pF
Sinking current @ C_L	9.81 I_b @280pF	----	17.12 I_b @10pF	24 I_b @100pF	4 I_b @50pF	9.6 I_b @1pF 47.43 I_b @50pF
Area (μm^2)	----	----	----	5400	----	735.216
FOM_1	9.81 @280Pf	7.6 @10 pF	11.625 @10 pF	9.6 @100pF	2.08 @50pF	3.40@1pF 10.44@50pF
FOM_2 (MHz*pF)/ μW	3.77 @280pF	9.33 @10 pF	4.166 @10 pF	2.75 @100pF	6.41 @50pF	2.72@1pF 6.51@50pF
FOM_3	6.08 @280pF	8.42 @10 pF	6.95 @10 pF	5.13 @100pF	3.65 @50pF	3.04@1pF 10.20@50pF

*Experimental results

3.4.2 Simulation results of proposed class-AB FVF cell-II

The biasing currents I_b and I_{bias} are selected as 65 μA and 40 μA , respectively for the proper operation of the proposed class-AB FVF cell-II. Using equation (3.42), the supply voltage (V_{DD})

is obtained as 1.148 V and therefore, a supply voltage of 1.2 V is chosen for the proposed class-AB FVF cell-II. The performance of the proposed class-AB FVF cell-II has been observed using load capacitances (C_L) of 1 pF and 50 pF. The aspect ratios (W/L) of transistors used to design the proposed class-AB FVF cell-II are listed in Table 3.3.

Table 3.3 Aspect ratios of transistors used to design the proposed class-AB FVF cell-II

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M_1	14.94/0.36
M_2	34.92/0.72
M_3, M'_3	10.98/0.18
M_4	18/0.54
M_5	14.94/0.36
M_6	9.9/0.54
M_7	4.5/0.18

The physical layout of the proposed class-AB FVF cell-II is shown in Figure 3.37. The layout occupies an area of $23.375 \mu\text{m} \times 16.105 \mu\text{m}$. The current sources I_{bias} and I_b have been implemented using NMOS transistors M_6 and M_7 in the layout.

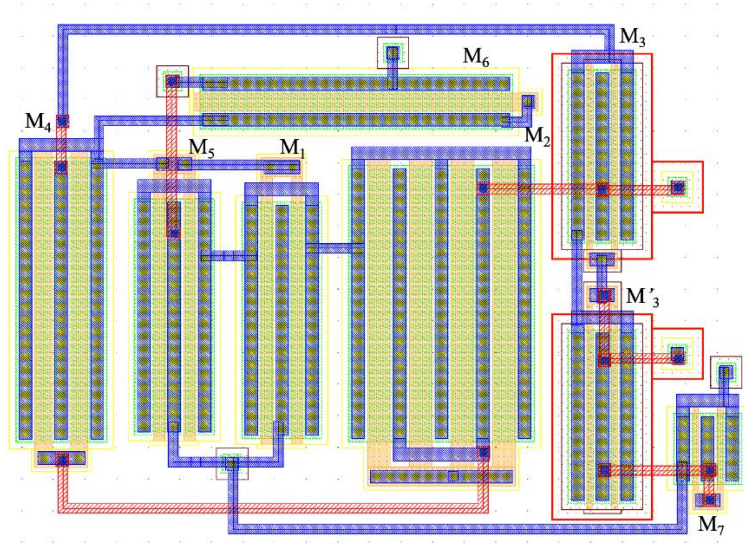


Figure 3.37 Physical layout of the proposed class-AB FVF cell-II

The transfer characteristics of the proposed class-AB FVF cell-II for input voltage varying from 0 to 1.2 V are shown in Figure 3.38. From the input and output voltage plots, it is observed that the output voltage follows the input voltage varying in the range of 0.6 V to 1.2 V which gives output voltage and input voltage swings as 0.475 and 0.6 V, respectively. Using equations (3.37) and (3.40), the output and input voltage swings are also calculated as 0.53 V and 0.65 V, respectively. It is clear that both the theoretical and simulated values are approximately matched.

Figure 3.39 shows the frequency response of the proposed class-AB FVF cell-II. From the frequency response, the voltage gain is obtained as 0.8 while bandwidths are obtained as 695.83 MHz and 15.37 MHz for the load capacitances of 1 pF and 50 pF, respectively. The voltage gain calculated using equation (3.56) is obtained as 0.805 and it is clear that both the theoretical and simulated values are approximately matched. The phase responses for the load capacitances of 1 pF and 50 pF are shown in Figure 3.40 and it is evident that the proposed class-AB FVF cell-II is stable.

The output resistance versus frequency plot of the proposed class-AB FVF cell-II is shown in Figure 3.41. The figure shows that the output resistance of the proposed class-AB FVF cell-II is 100.5Ω for the frequency range of 1 to 100 MHz. The output resistance is also calculated using equation (3.49) as 102Ω and it is clear that both the theoretical and simulated values are approximately matched.

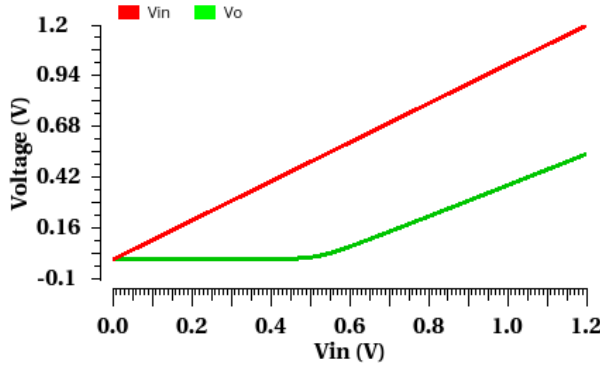


Figure 3.38 Transfer characteristics of the proposed class-AB FVF cell-II

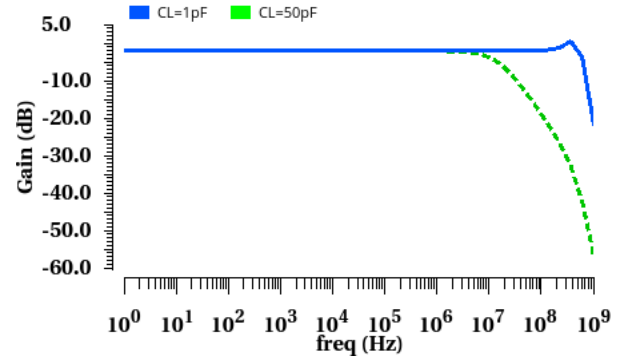


Figure 3.39 Frequency response of the proposed class-AB FVF cell-II

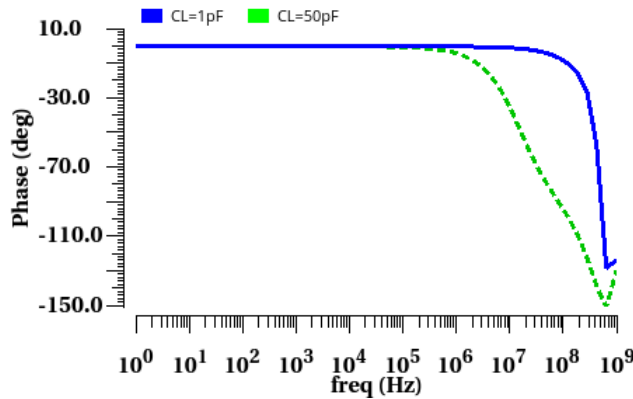


Figure 3.40 Phase response of the proposed class-AB FVF cell-II

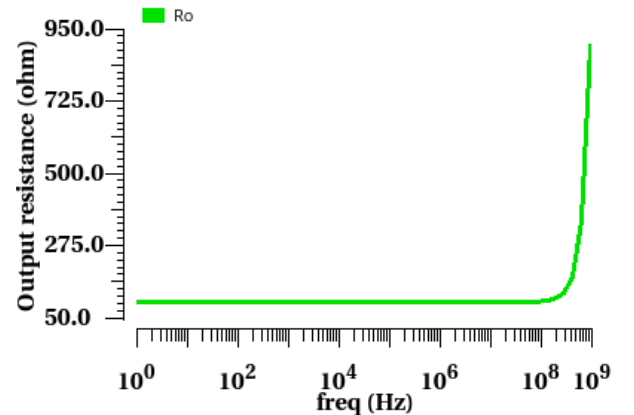


Figure 3.41 Output resistance of the proposed class-AB FVF cell-II

To perform the transient analysis, a square pulse of amplitude 0.6 V to 1.2 V at a frequency of 1 MHz is applied at the input. The transient responses obtained for the load capacitances of 1 pF and 50 pF are shown in Figure 3.42. The plots show that the output voltage follows the input voltage and the symmetrical slew rates (SR^+/SR^-) are calculated as 100.75 V/ μ s/ 76.7 V/ μ s and 32.44 V/ μ s/ 18.39 V/ μ s for the load capacitances of 1 pF and 50 pF, respectively.

The output responses of the proposed class-AB FVF cell-II for the load capacitances of 1 pF and 50 pF at rising and falling edges of the input signal are shown in Figures 3.43 and 3.44, respectively. From Figure 3.43, the settling times (2% of the final values) at rising edges are obtained as 4.71 ns and 31.3 ns for the load capacitances of 1 pF and 50 pF, respectively. From Figure 3.44, the settling times (2% of the final values) at falling edges are obtained as 3.1 ns and 21.7 ns for the load capacitances of 1 pF and 50 pF, respectively.

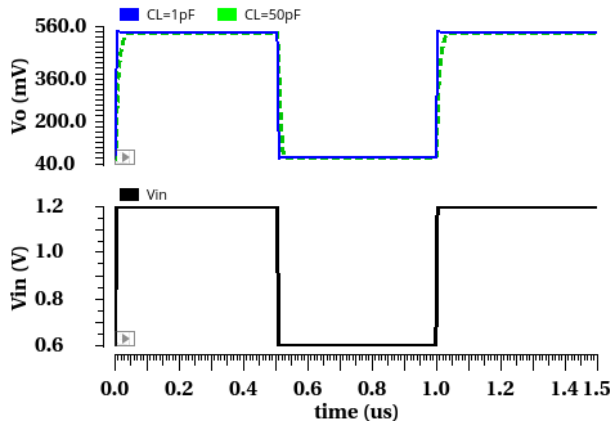


Figure 3.42 Transient response of the proposed class-AB FVF cell-II for a square input pulse

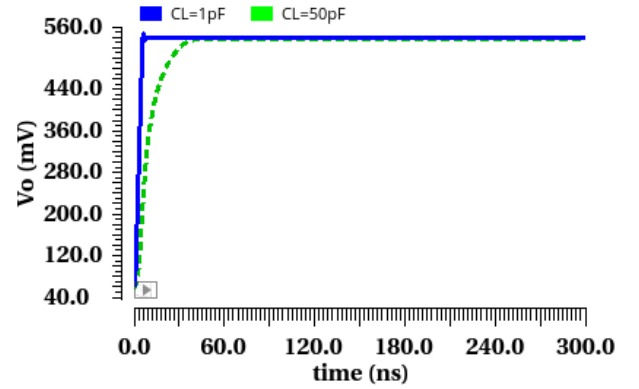


Figure 3.43 Output response of the proposed class-AB FVF cell-II at the rising edge

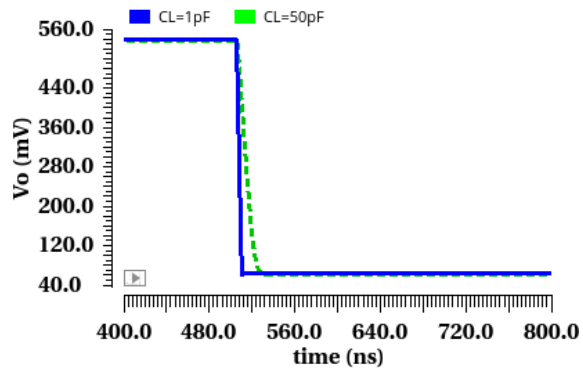


Figure 3.44 Output response of the proposed class-AB FVF cell-II at the falling edge

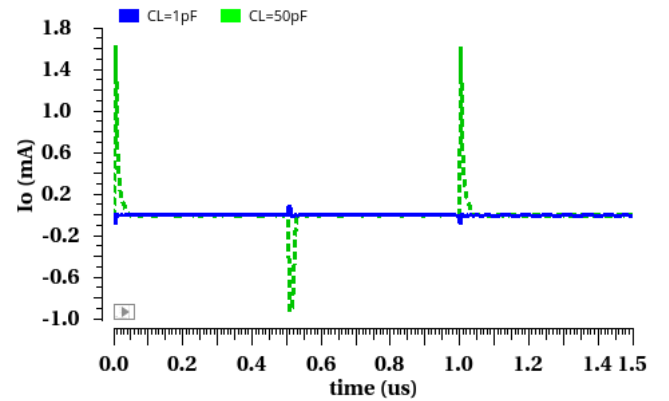


Figure 3.45 Current sourcing and sinking capabilities of the proposed class-AB FVF cell-II

The current sourcing and sinking capabilities of the proposed class-AB FVF cell-II at rising and falling edges of the input signal are shown in Figure 3.45. It is observed that the current sourcing and sinking capabilities are $1.55 I_b$ and $1.18 I_b$, respectively for the load capacitance of 1 pF. For the load capacitance of 50 pF, the current sourcing and sinking capabilities are obtained as $24.96 I_b$ and $14.15 I_b$, respectively.

The transient response of the proposed class-AB FVF cell-II for a triangular pulse varying from 0.6 V to 1.2 V is shown in Figure 3.46. From the plot, the input and output voltage swings are observed as 0.6 V and 0.475 V, respectively.

The input noise spectral density (INSD) of the proposed class-AB FVF cell-II is shown in Figure 3.47. From the figure, it is observed that the INSD of class-AB FVF cell-II remains constant as $2.084 \text{ nV}/\sqrt{\text{Hz}}$ for the load capacitances of 1 pF and 50 pF. It can be concluded that the proposed class-AB FVF cell-II is less sensitive to the noise.

The total harmonic distortion (THD) plot of the proposed class-AB FVF cell-II is shown in Figure 3.48. A sinusoidal signal of 200 mV peak-to-peak amplitude is applied at the input terminal to calculate the THD. The plot shows the variation in THD when the frequency of the input signal is varied from 50 kHz to 10 MHz for the worst-case load capacitance of 50 pF. It is observed that the THD is less than 1% for the frequency range of 50 kHz to 10 MHz. The plot of THD versus input amplitude varying from 20 mV to 200 mV at input frequency of 1 MHz for the worst-case load capacitance of 50 pF is shown in Figure 3.49. The plot shows that the THD remains less than 0.7 % for the input amplitude varying from 20 mV to 200 mV.

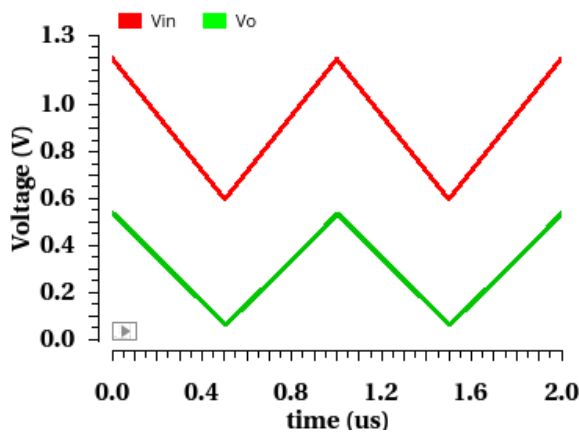


Figure 3.46 Transient response of the proposed class-AB FVF cell-II for a triangular input pulse

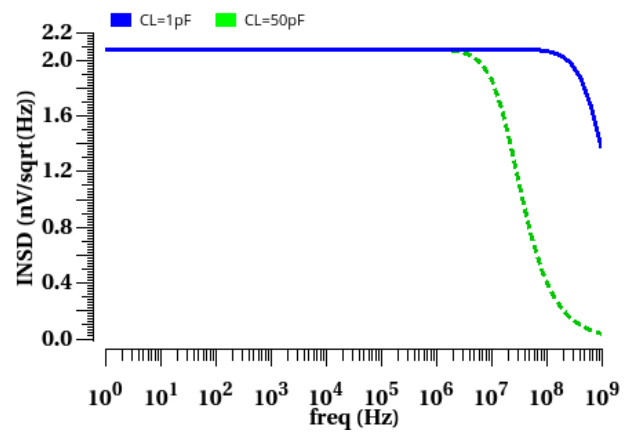


Figure 3.47 Input noise spectral density of the proposed class-AB FVF cell-II

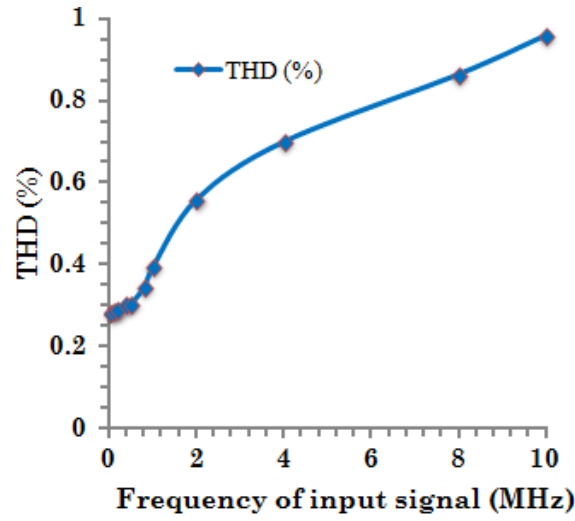


Figure 3.48 THD (%) versus frequency plot of the proposed class-AB FVF cell-II

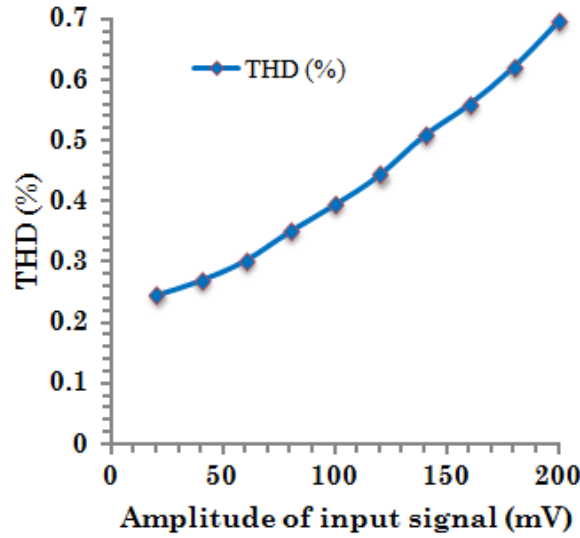


Figure 3.49 THD (%) versus amplitude plot of the proposed class-AB FVF cell-II

The proposed class-AB FVF cell-II has been compared with FVF cells available in the literature in Table 3.4. In the proposed class-AB FVF cell-II input voltage is given at the gate terminal so it overcomes the bandwidth limitation of the proposed class-AB FVF cell-I. The proposed class-AB FVF cell-II offers wide bandwidth. It also shows improved current driving capability and thus high symmetrical slew rate due to the use of bulk-driven technique and sinking transistor. Further, for fairly comparing the FVF cells, the FOMs have been used. The proposed class-AB FVF cell offers higher FOM_1 than the reported FVF cells [32-33, 35, 44, 50] and higher FOM_2 than the suggested FVF cells [32-33, 35, 43-44, 46, 50]. But the overall FOM_3 of the proposed class-AB FVF cell-II is higher than the FVF cells reported in [32-33, 35, 43-44, 50].

Table 3.4 Comparison of the proposed class-AB FVF cell-II with FVF cells available in the literature

References→ Parameters↓	[32]*	[33]	[35]	[43]	[44]	[46]*	[50]	Proposed cell-II
Supply voltage (V)	2.7	1.2	1.8	±1.65	±1.5	1.2	1.5	1.2
Technology (nm)	ALD 1106	350	350	500	500	350	500	180
Bias current (I_b) (μ A)	55	2.5	8	10	30	40	50	65
Power (μ W)	148.5	3	14.4	99	225	30	120	78
Input Swing (V)	----	1	----	----	----	0.534	0.7	0.6
Output Swing (V)	----	1	----	----	----	0.353	0.6	0.475
Gain	----	----	----	----	----	0.78	0.76	0.80
Bandwidth (MHz) @ C_L	2 @280pF	2.8 @10 pF	6 @10pF	13.1 @30pF	6.2 @100pF	200 @1pF	15.4 @50pF	695.83 @1 pF 15.37 @50pF
R_{out} (Ω)	----	----	---	----	---	220	----	100.5
SR+ (V/ μ s) @ C_L	3.75 @280pF	1.9 @10 pF	9.3 @10pF	25 @30pF	3.5 @100pF	29 @15pF	3.34 @50pF	100.75 @1 pF 32.44 @50 pF
SR- (V/ μ s) @ C_L	1.82 @280pF	----	13.7 @10pF	----	4.3 @100pF	27 @15pF	4 @50pF	76.7 @1 pF 18.39 @50 pF
Sourcing current @ C_L	16.72 I_b @280pF	7.6 I_b @10 pF	11.62 I_b @10pF	80 I_b @30pF	26 I_b @100pF	11 I_b @15pF	3.34 I_b @50pF	1.55 I_b @1pF 24.96 I_b @50pF
Sinking current @ C_L	9.81 I_b @280pF	----	17.12 I_b (@10pF)	----	24 I_b @100pF	10.4 I_b @15pF	4 I_b @50pF	1.18 I_b @1pF 14.15 I_b @50pF
INSD (nV/ $\sqrt{Hz}$)	----	880 @1kHz	----	40 @50kHz	----	----	8.6 @1Hz	2.08 @1MHz
Area (μ m ²)	----	----	----	11000	5400	----	----	376.45
FOM ₁	9.81 @280pF	7.6 @10 pF	11.625 @10 pF	26.66 @30pF	9.6 @100pF	16.64 @15pF	2.08 @50pF	1.18 @1pF 14.15 @50pF
FOM ₂ (MHz* μ pF)/ μ W	3.77 @280pF	9.33 @10 pF	4.166 @10 pF	3.96 @30pF	2.75 @100pF	6.66 @1 pF	6.41 @50pF	8.92 @1 pF 9.85 @50 pF
FOM ₃	6.08 @280pF	8.42 @10 pF	6.95 @10 pF	10.27 @30pF	5.13 @100pF	----	3.65 @50pF	3.24 @1 pF 11.80 @50pF

*Experimental results

3.4.3 Simulation results of proposed class-AB FVF cell-III

The proposed class-AB FVF cell-III is biased using current I_{bias} of 50 μ A with C_{bat} = 500 fF and its performance is measured under different load capacitances (C_L) of 1 pF and 50 pF for better comparison with reported FVF cells in the literature. The R_{large} resistance implemented using transistor M_4 is selected as 17 Gohm. The simulations have been performed by considering ideal

($R_s=0$) and non-ideal ($R_s \neq 0$) input voltage sources. The different values of internal resistance (R_s) of the voltage source are chosen as 10 k Ω , 30 k Ω , 50 k Ω , 70 k Ω and 100 k Ω . To obtain the output voltage swing of 0.55 V, the supply voltage is calculated using equation (3.79) as 1.15 V. Hence, the value of supply voltage (V_{DD}) has been selected as 1.2 V for the proper operation of the proposed class-AB FVF cell. The aspect ratios (W/L) of all the transistors used to design the proposed class-AB FVF cell-III are listed in Table 3.5.

Figure 3.50 shows the physical layout of the proposed class-AB FVF cell-III occupying an area of 53.69 $\mu\text{m} \times 25.425 \mu\text{m}$. The current sources I_b and I_{bias} have been implemented using NMOS transistors M_8 and M_9 in the layout.

Figure 3.51 shows the transfer characteristics of the proposed class-AB FVF cell-III. From the plot, the output voltage swing and input voltage swing are observed as 0.545 V and 0.7 V, respectively. Using equations (3.74) and (3.78), the output and input voltage swings are also calculated as 0.60 V and 0.75 V, respectively. It is clear that both the theoretical and simulated values are approximately matched.

Table 3.5 Aspect ratios of transistors used to design the proposed class-AB FVF cell-III

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M_1	26.1/0.36
M_2	28.08/0.36
M_3	10.08/0.18
M'_3	10.08/0.18
M_4	3.96/0.18
M_5	28.08/0.36
M_6	31.88/0.18
M_7	31.88/0.18
M_8	3.06/0.18
M_9	3.06/0.18

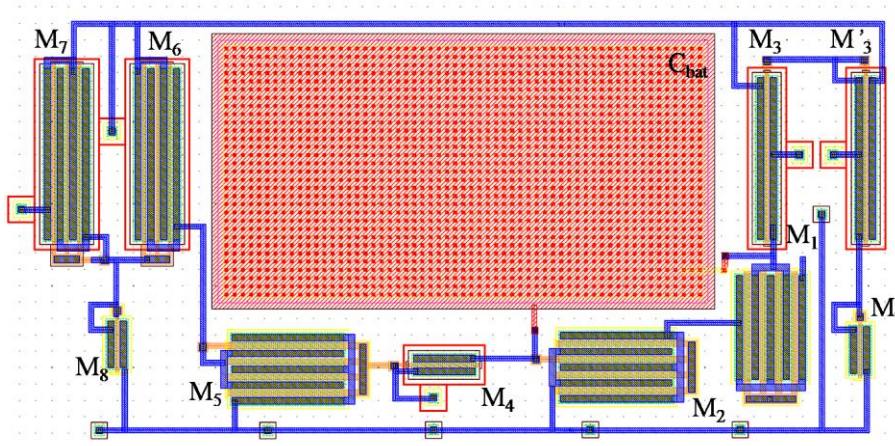


Figure 3.50 Physical layout of the proposed class-AB FVF cell-III

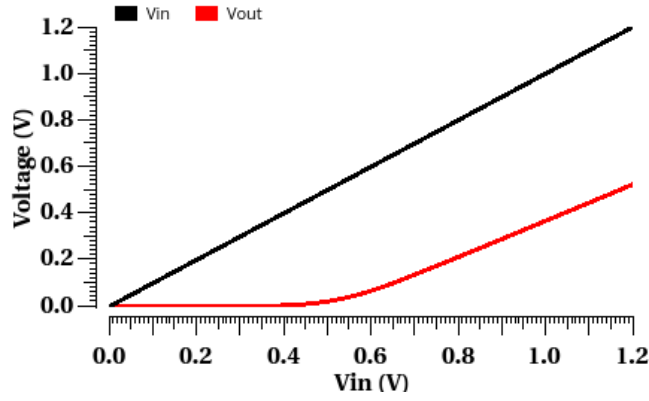


Figure 3.51 Transfer characteristics of the proposed class-AB FVF cell-III

The frequency responses of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF are shown in Figures 3.52 (a) and (b), respectively. The ideal ($R_s=0$) and non-ideal ($R_s \neq 0$) voltage sources of 100 mV at 1MHz are applied at the input terminal to obtain frequency responses. From the figures, the bandwidths are observed as 717.3 MHz and 16.21 MHz for the load capacitances of 1 pF and 50 pF, respectively. The voltage gain is obtained as 0.78. The voltage gain is also calculated using equation (3.88) as 0.79 and it is clear that both the theoretical and simulated values are approximately matched. It is observed that due to the body effect, the gain of the proposed class-AB FVF cell-III is obtained as less than one. But, a PMOS version of the proposed class-AB FVF cell-III can provide gain approximately equal to one because in the PMOS version body effect can be avoided.

Figures 3.53 (a) and (b) show the phase responses of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF, respectively. From the figures, it is evident that the proposed class-AB FVF cell-III is stable for the load capacitances of 1 pF and 50 pF while ideal ($R_s=0$) and non-ideal ($R_s \neq 0$) both input voltage sources are considered.

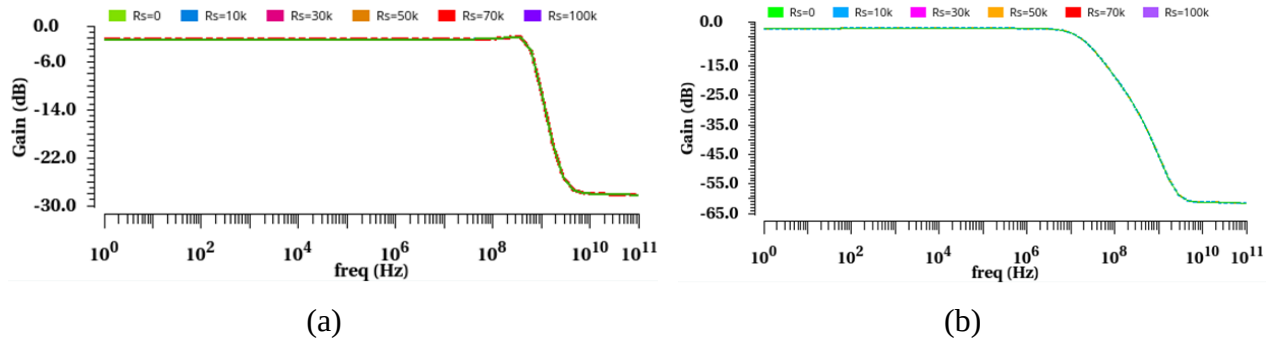


Figure 3.52 Frequency responses of the proposed class-AB FVF cell-III for different values of internal resistances when load capacitance is (a) 1 pF (b) 50 pF

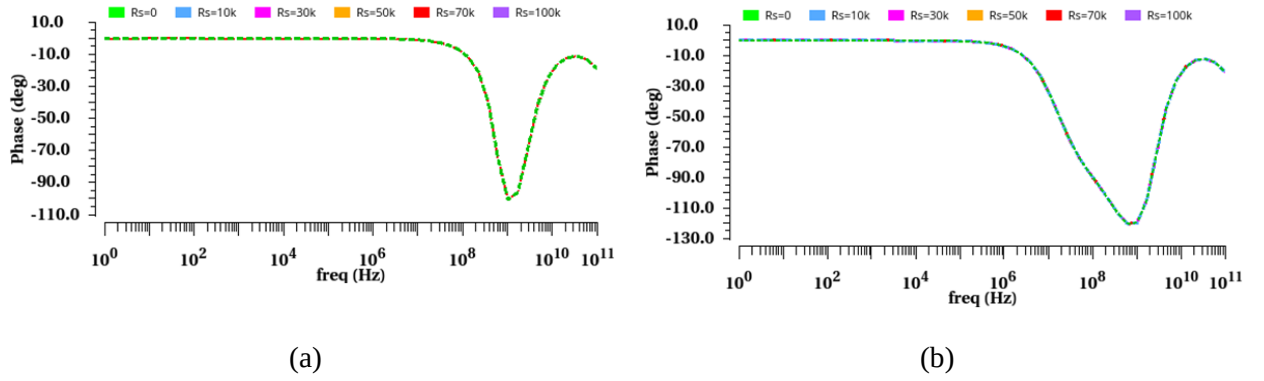


Figure 3.53 Phase responses of the proposed class-AB FVF cell-III for different values of internal resistances when load capacitance is (a) 1 pF (b) 50 pF

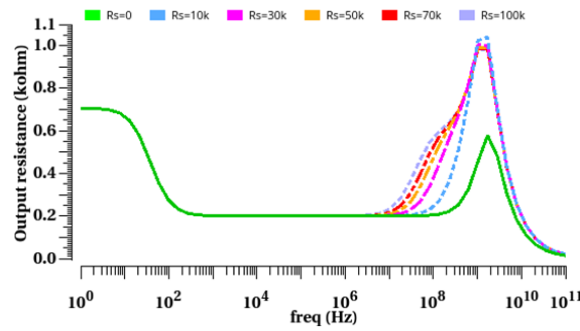


Figure 3.54 Output resistance of the proposed class-AB FVF cell-III

The output resistance versus frequency plots of the proposed class-AB FVF cell-III for ideal ($R_s=0$) and non-ideal ($R_s \neq 0$) input voltage sources are shown in Figure 3.54. The output resistance remains constant as 203Ω for the frequency range of 1 kHz to 40 MHz when $R_s=10 \text{ k}\Omega$, 1 kHz to 11 MHz when $R_s=30 \text{ k}\Omega$, 1 kHz to 9 MHz when $R_s=50 \text{ k}\Omega$, 1 kHz to 7 MHz when $R_s=70 \text{ k}\Omega$ and 1 kHz to 5 MHz when $R_s=100 \text{ k}\Omega$. From the figure, it can also be seen that the proposed class-AB FVF cell-III gives the output resistance of 203Ω in the frequency range of 1 kHz to 180 MHz for $R_s=0 \Omega$. Using equation (3.85), the output resistance is calculated as 205Ω and it is clear that both the theoretical and simulated values are approximately matched.

Figures 3.55 (a) and (b) show the transient responses of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF, respectively. The ideal ($R_s=0$) and non-ideal ($R_s \neq 0$) input voltage sources are considered when a square input pulse of 500 mV peak-to-peak amplitude with a frequency of 1 MHz is applied. From the figures, the symmetrical slew rates (SR^+/SR^-) are calculated as $78.76 \text{ V}/\mu\text{s}/105.2 \text{ V}/\mu\text{s}$ and $33.18 \text{ V}/\mu\text{s}/35.3 \text{ V}/\mu\text{s}$ for the load capacitances of 1 pF and 50 pF, respectively.

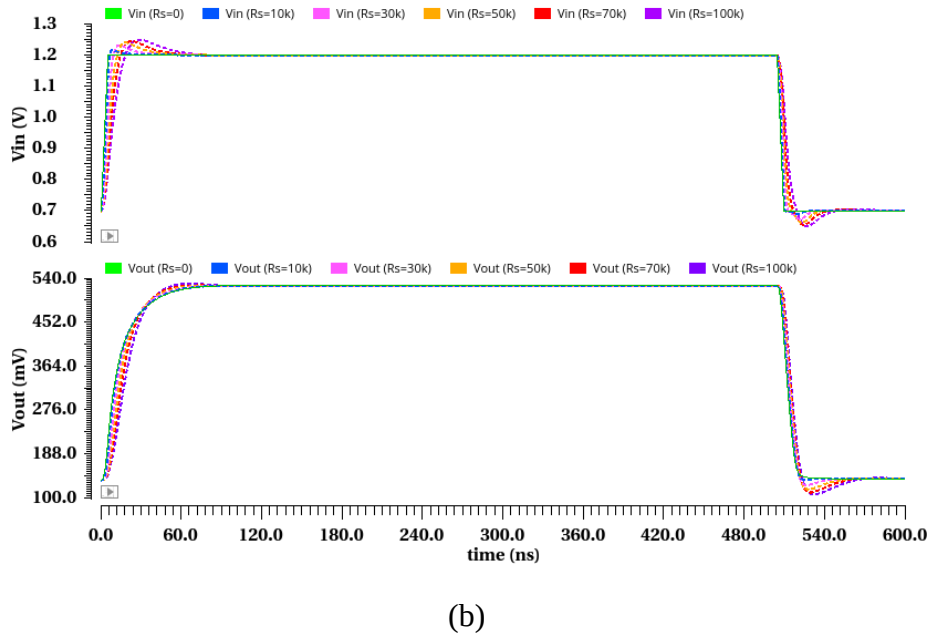
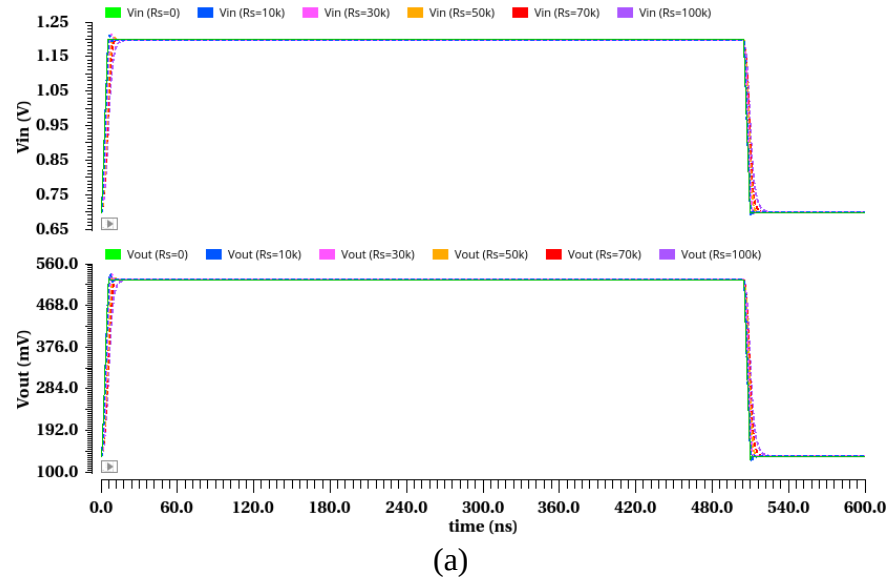


Figure 3.55 Transient responses of the proposed class-AB FVF cell-III for different values of internal resistances when load capacitance is (a) 1 pF (b) 50 pF

The output responses of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF when an input square pulse of 500 mV peak-to-peak amplitude at a frequency of 1 MHz is applied are shown in Figures 3.56 (a) and (b). From Figure 3.56 (a), the settling times (2% of their final values) at rising edges are obtained as 5.37 ns and 55.73 ns for the load capacitances of 1 pF and 50 pF, respectively. From Figure 3.56 (b), the settling times (2% of their final values) at falling edges are obtained as 6.09 ns and 21.38 ns for the load capacitances of 1 pF and 50 pF, respectively.

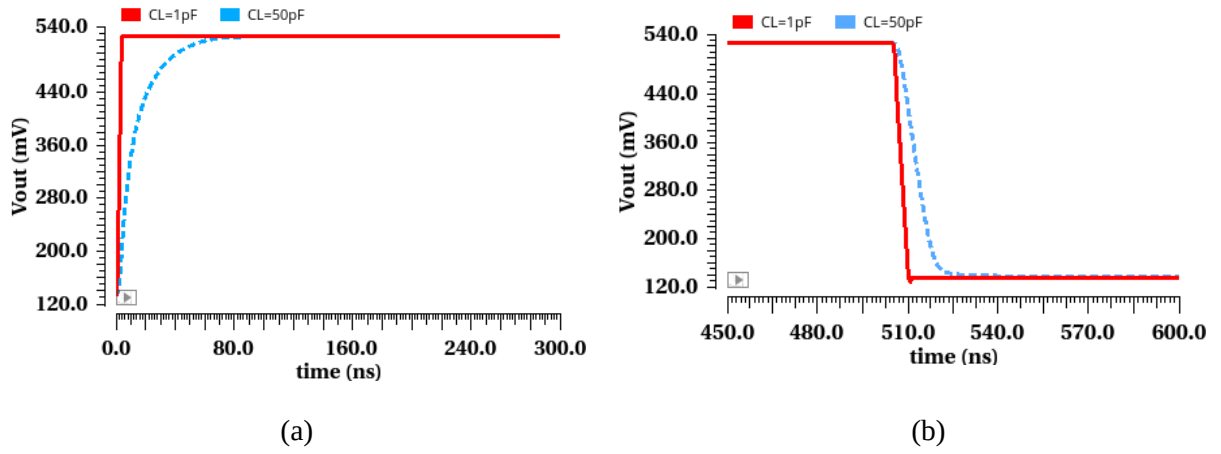


Figure 3.56 Output responses of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF (a) at the rising edge (b) at the falling edge

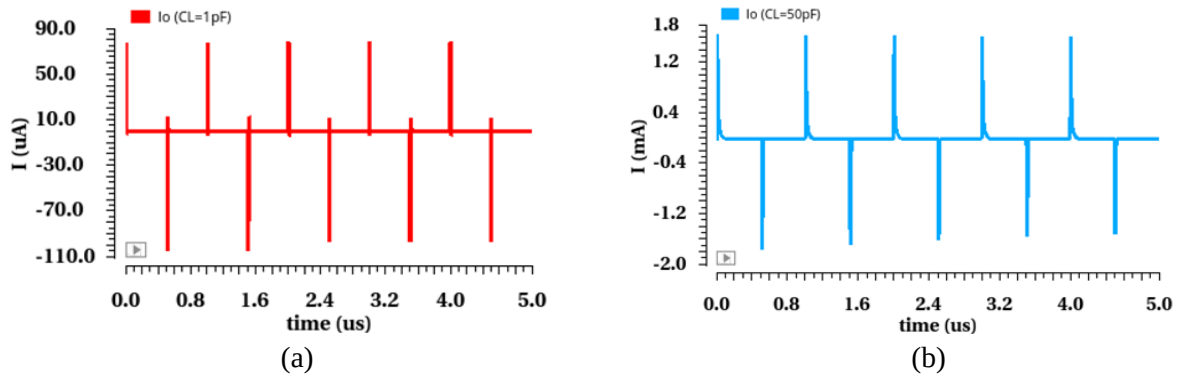


Figure 3.57 Current sourcing and sinking capabilities of the proposed class-AB FVF cell-III for the load capacitance of (a) 1 pF (b) 50 pF

Figures 3.57 (a) and (b) show the output current sourcing and sinking capabilities of the proposed class-AB FVF cell-III for the load capacitances of 1 pF and 50 pF, respectively. The current sourcing capabilities on rising edges of the input signal are observed as $1.57 I_b$ and $33.18 I_b$ for 1 pF and 50 pF, respectively. The current sinking capabilities on falling edges of the input signal are observed as $2.1 I_b$ and $35.3 I_b$ for 1 pF and 50 pF, respectively.

The transient response of the proposed class-AB FVF cell-III for a triangular input pulse of amplitude that varies from 500 mV to 1.2 V with a frequency of 1 MHz is shown in Figure 3.58. From the figure, it is observed that the output voltage swing is 545 mV for the input voltage swing of 700 mV.

The input noise spectral density (INSD) of the proposed class-AB FVF cell-III is shown in Figure 3.59. From the figure, it is evident that the INSD of class-AB FVF cell-III remains constant as $4.83 \text{ nV}/\sqrt{\text{Hz}}$ for the load capacitances of 1 pF and 50 pF. Therefore, it can be concluded that the proposed class-AB FVF cell-III is less sensitive to noise.

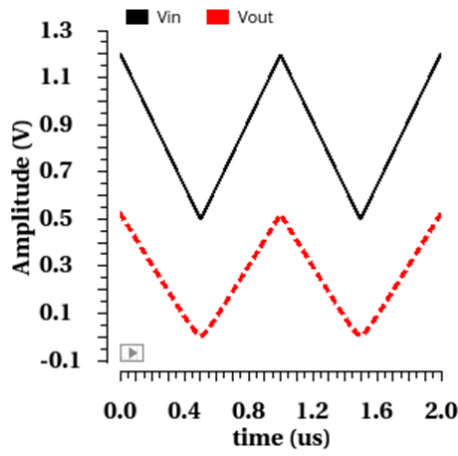


Figure 3.58 Transient response of the proposed class-AB FVF cell-III for a triangular input pulse

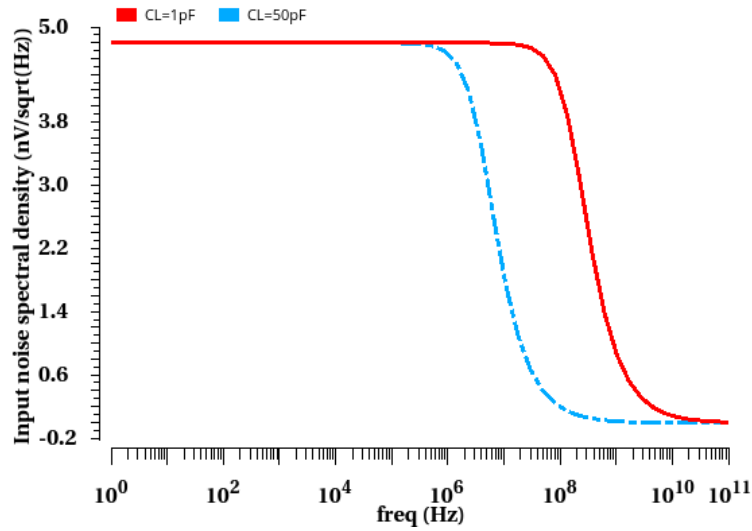


Figure 3.59 Input noise spectral density of the proposed class-AB FVF cell-III

A sinusoidal wave of 200 mV peak-to-peak amplitude with a frequency of 1 MHz is applied at the input terminal to estimate the total harmonic distortion (THD) of the proposed class-AB FVF cell-III. The THD is calculated for various frequencies of the input signal such as 1 MHz, 2 MHz, 4 MHz, 8 MHz, 10 MHz, 20 MHz, 40 MHz, 50 MHz, 80 MHz and 100 MHz. The load capacitance has been chosen as 1 pF for all the THD calculations. The THD (%) plot is shown in Figure 3.60 for the frequency range of 1 MHz to 100 MHz. From the figure, it is clear that the THD is less than 2% for the frequency range of 1 MHz to 100 MHz. The THD (%) versus amplitude of input signal plot for the load capacitance of 1 pF is shown in Figure 3.61. It is observed that THD for the various amplitudes of the input signal is less than 2%.

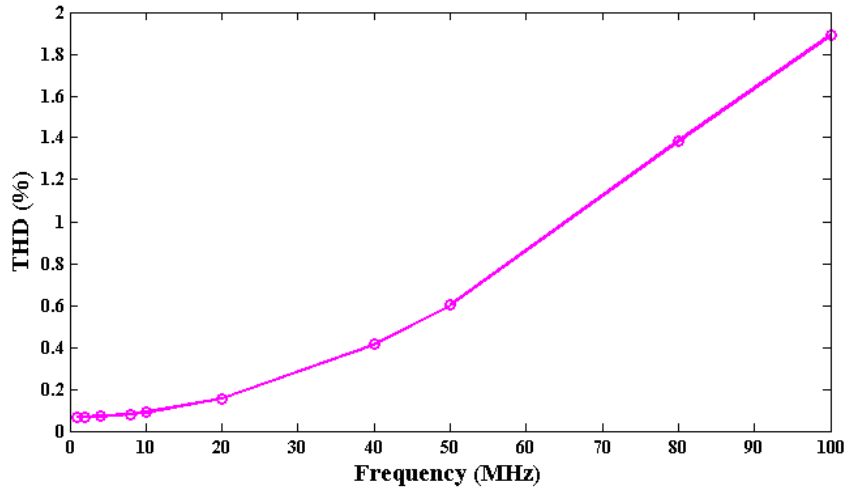


Figure 3.60 THD (%) versus frequency plot of the proposed class-AB FVF cell-III

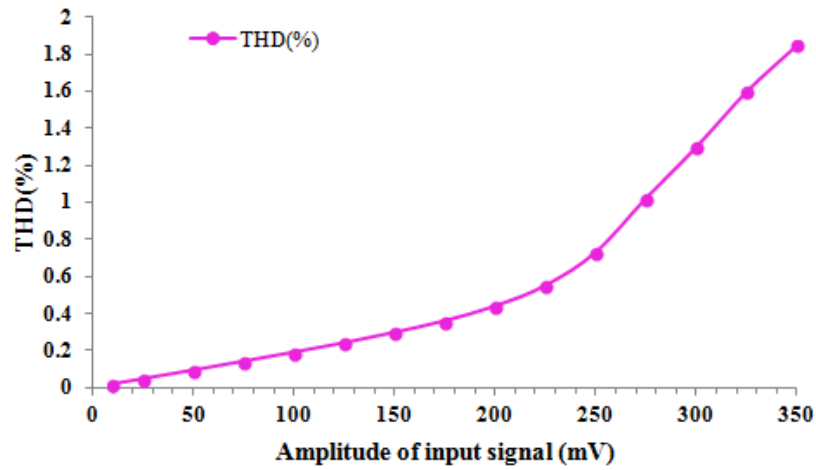


Figure 3.61 THD (%) versus amplitude plot of the proposed class-AB FVF cell-III

The various performance parameters of the proposed class-AB FVF cell-III are compared with the FVF cells available in literature as shown in Table 3.6. It is observed from the comparison that the proposed class-AB FVF cell-III offers high symmetrical slew rates (SR^+ and SR^-), high current sourcing capability and high current sinking capability. The proposed class-AB FVF cell-III has a comparable range of other parameters such as input/output voltage swing, output resistance, gain and bandwidth.

On the basis of three FOMs, it can be concluded that the proposed class-AB FVF cell-III has higher FOM_1 than the reported FVF cells [31–33, 35, 43–44, 46–47, 50–52] and higher FOM_2 than the existing FVF cells [31–33, 35, 43–44, 46, 50, 52] whereas higher FOM_3 than the reported FVF cells [31–33, 35, 43–44, 47, 50–52].

Table 3.6 Comparison of the proposed class-AB FVF cell-III with FVF cells available in the literature

References→ Parameters ↓	[31]	[32]*	[33]	[35]	[39]	[43]*	[44]	[46]*	[47]	[50]	[51]	[52]*	Proposed cell-III
Supply voltage (V)	±1.5	2.7	1.2	1.8	1.2	±1.65	±1.5	1.2	0.9	1.5	1.2	±0.9	1.2
Technology node (nm)	500	ALD 1106	350	350	65	500	500	350	500	500	180	180	180
Bias current (I_{bias}) (μA)	30	55	2.5	8	9.8	10	30	40	16	50	65	30	50
Power (μW)	198	148.5	3	14.4	11	99	225	30	36	120	35	229	60
Input swing (V)	--	----	1	--	----	----	---	0.534	--	----	0.6	---	0.70
Output swing (V)	---	----	1	--	----	----	---	0.353	--	0.6	0.44	---	0.545
Gain	--	----	----	--	0.95**	----	--	0.78	0.96**	0.767	0.8	---	0.78
Bandwidth (MHz)	70 @10pF	2 @280pF	2.8 @10pF	6 @10pF	200 @ 1pF	13.1 @30pF	6.2 @100pF	200 @1pF	76 @10pF	15.4 @50pF	513.02 @1pF 45 @15pF	32 @50pF	717.3 @1pF 16.21 @50pF
R_{out} (Ω)	40	----	----	---	760	----	---	220	210	----	106.78	50	203
SR+ (V/ μs)	85 @10pF	3.75 @280pF	1.9 @10pF	9.3 @10pF	----	25 @30pF	3.5 @100pF	29 @15pF	10.3 @10pF	3.34 @50pF	31.28 @15pF	25.6 @50pF	78.76 @1pF 33.18 @50pF
SR- (V/ μs)	52.5 @10pF	1.82 @280pF	----	13.7 @10pF	----	----	4.3 @100pF	27 @15pF	10.3 @10pF	4 @50pF	27.7 @15pF	20.1 @50pF	105.2 @1pF 35.3 @50pF
Sourcing capability	28.33 I_b @10pF	16.7 I_b @280pF	7.6 I_b @10pF	11.62 I_b @10pF	----	80 I_b @30pF	26 I_b @100pF	11 I_b @15pF	34.3 I_b @10pF	3.34 I_b @50pF	19.77 I_b @15pF	43.3 I_b @50pF	1.57 I_b @1pF 33.18 I_b @50pF
Sinking capability	17.5 I_b @10pF	9.8 I_b @280pF	----	17.12 I_b (@10pF)	----	----	24 I_b @100pF	10.4 I_b @15pF	19 I_b @10pF	4 I_b @50pF	1.88 I_b @15pF	33.6 I_b @50pF	2.1 I_b @1pF 35.3 I_b @50pF
INSD (nV/ $\sqrt{Hz}$)	----	----	880 @1kHz	----	----	40 @50kHz	----	----	----	8.6	----	----	4.83 @1MHz
Area (μm^2)	----	----	----	----	----	11000	5400	----	----	----	342	13524	1365
FOM ₁	7.5 @10pF	9.81 @280pF	7.6 @10pF	11.625 @10pF	----	26.66 @30pF	9.6 @100pF	16.64 @15pF	7.6 @10pF	2.08 @50pF	4.19 @15pF	8 @50pF	1.57 @1pF 33.18 @50pF
FOM ₂ ((MHz*pF)/ μW)	3.53 @10pF	3.77 @280pF	9.33 @10pF	4.166 @10pF	18.18 @ 1pF	3.96 @30pF	2.75 @100pF	6.66 @1pF	21.11 @10pF	6.41 @50pF	19.28 @15pF	7 @50pF	11.95 @1pF 13.50 @50pF
FOM ₃	5.14 @10pF	6.08 @280pF	8.42 @10pF	6.95 @10pF	----	10.28 @30pF	5.13 @100pF	----	12.66 @10pF	3.65 @50pF	8.9 @15pF	7.5 @50pF	4.33 @1pF 21.16 @50pF

*Experimental results

**When body effect is not considered

3.4.4 Simulation results of proposed class-AB FVF cell-IV

The proposed class-AB FVF cell-IV is biased with current (I_b) of 60 μA and the value of current I_{b1s} is chosen as 24 μA . The resistance R_b is chosen as 5 $\text{k}\Omega$. Using equation (3.113), the supply voltage (V_{DD}) requirement of the proposed class-AB FVF cell-IV is calculated as 1.49 V and hence, the supply voltage is chosen as 1.5 V. Its performance is measured under different load capacitances (C_L) of 1 pF and 50 pF. Table 3.7 shows the aspect ratios of transistors used to design the proposed class-AB FVF cell-IV.

In the physical layout of the proposed class-AB FVF cell-IV shown in Figure 3.62, the resistor R_b has been implemented using a poly resistor [117]. The current sources I_{b1s} and I_b has been implemented using transistors M_6 and M_7 , respectively in the layout. The layout consisting of transistors M_{1-7} and resistor R_b occupies an area of $17.70 \mu\text{m} \times 26.03 \mu\text{m}$.

Table 3.7 Aspect ratios of transistors used to design the proposed class-AB FVF cell-IV

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M_1	12/0.36
M_2	30/0.54
M_3	15/0.36
M_4	20/0.54
M_5	20/0.36
M_6	4/0.36
M_7	4.32/0.18

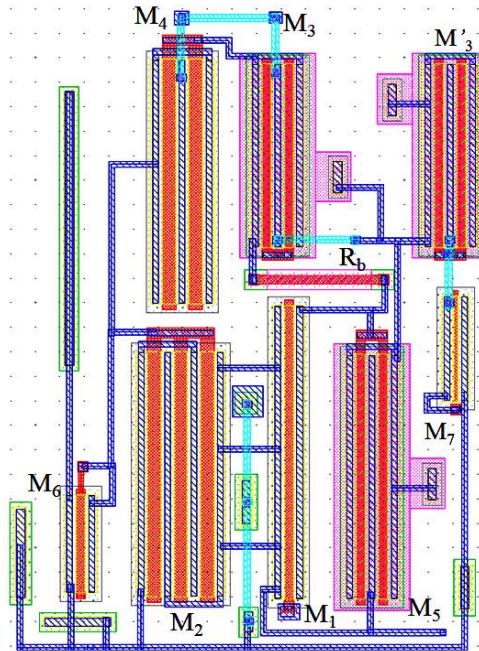


Figure 3.62 Physical layout of the proposed class-AB FVF cell-IV

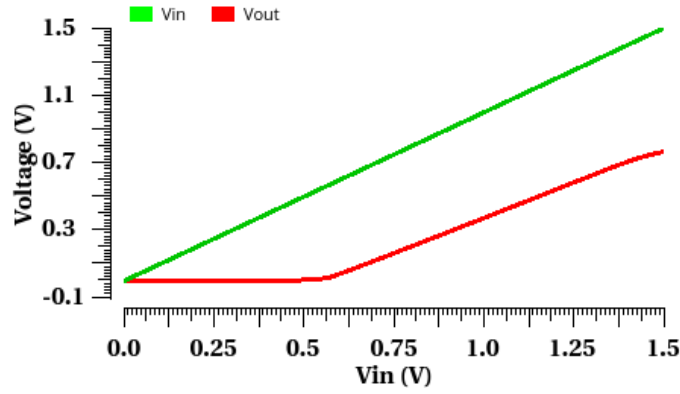


Figure 3.63 Transfer characteristics of the proposed class-AB FVF cell-IV

The transfer characteristics of the proposed class-AB FVF cell-IV for input voltage varying from 0 to 1.5 V are shown in Figure 3.63. The output voltage follows the input voltage in the range of 0.65 V to 1.45 V which gives output and input voltage swings of 0.67 V and 0.80 V, respectively. The output and input voltage swings are also calculated using equations (3.105) and (3.111) as 0.67 V and 0.79 V, respectively and it is clear that both the theoretical and simulated values are approximately matched.

The frequency responses of the proposed class-AB FVF cell-IV for the load capacitances of 1 pF and 50 pF are shown in Figure 3.64. From the figure, it can be seen that the bandwidth decreases with the increase in the value of load capacitance and the bandwidths are obtained as 815 MHz and 54 MHz for the load capacitances of 1 pF and 50 pF, respectively. The closed-loop voltage gain of the proposed class-AB FVF cell-IV is obtained as 0.84. The closed-loop voltage gain is also calculated using equation (3.128) as 0.835 and it is clear that both the theoretical and simulated values are approximately matched. The gain is obtained as less than unity because the body effect has been considered.

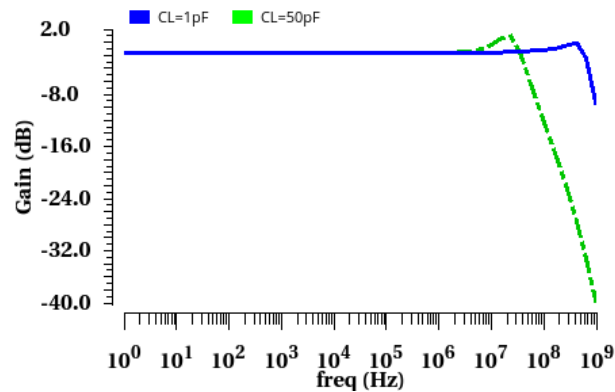


Figure 3.64 Frequency response of the proposed class-AB FVF cell-IV

The phase responses of the proposed class-AB FVF cell-IV for the load capacitances of 1 pF and 50 pF are shown in Figure 3.65. From the figure, it can be seen that the proposed class-AB FVF cell-IV is stable for different load capacitances.

The output resistance versus frequency plot of the proposed class-AB FVF cell-IV is shown in Figure 3.66. The figure shows that the output resistance of the proposed class-AB FVF cell-IV is 10 Ω for the frequency range of 1 to 10 MHz. The output resistance is also calculated using equation (3.121) as 11 Ω and it is clear that both the theoretical and simulated values are approximately matched.

For transient analysis, the input square pulse of magnitude 0.65 V to 1.45 V at a frequency of 1 MHz is applied. The output transient response of the proposed class-AB FVF cell-IV for the load capacitances of 1 pF and 50 pF are shown in Figure 3.67.

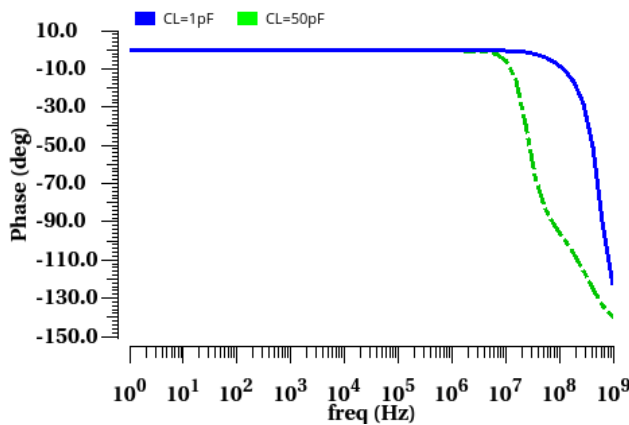


Figure 3.65 Phase response of the proposed class-AB FVF cell-IV

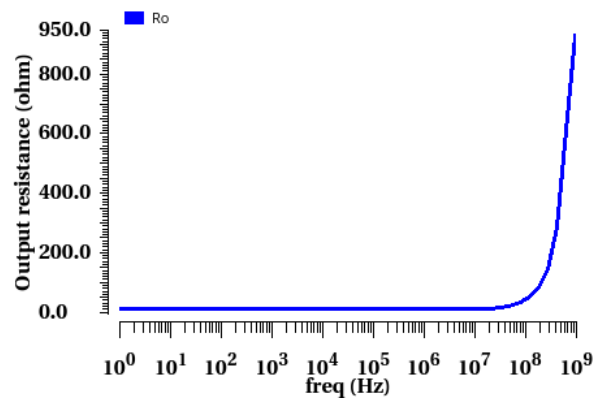


Figure 3.66 Output resistance of the proposed class-AB FVF cell-IV

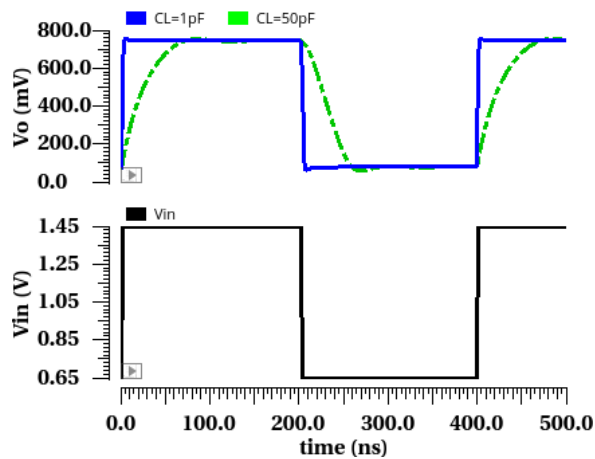


Figure 3.67 Transient response of the proposed class-AB FVF cell-IV for a square input pulse

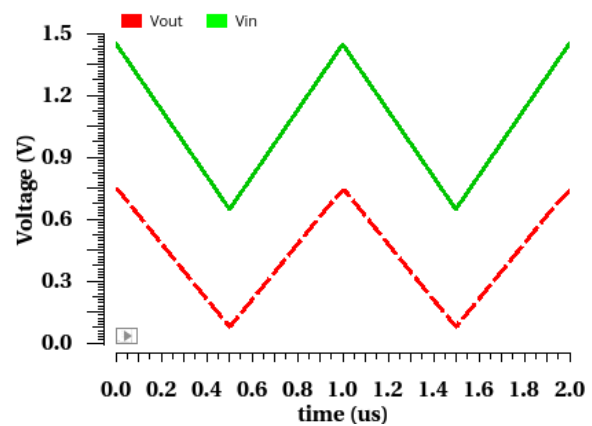


Figure 3.68 Transient response of the proposed class-AB FVF cell-IV for a triangular input pulse

The values of slew rate (SR^+/SR^-) are obtained as 289.8 V/ μ s/ 201 V/ μ s and 22.42 V/ μ s/ 21.90 V/ μ s for the load capacitances of 1 pF and 50 pF, respectively. The proposed class-AB FVF cell-IV shows symmetrical slew rate for different load capacitances. Figure 3.68 shows the transient response of the proposed class-AB FVF cell-IV for a triangular input pulse of amplitude that varies from 650 mV to 1.45 V with frequency of 1 MHz for the worst-case load capacitance of 50 pF. The figure shows that the output voltage follows the triangular input voltage pulse. The input and output voltage swings are obtained as 0.80 V and 0.67 V, respectively.

The output responses of the proposed class-AB FVF cell-IV for the load capacitances of 1 pF and 50 pF at rising and falling edges of the input signal are shown in Figures 3.69 and 3.70, respectively. From Figure 3.69, the settling times (2% of the final values) at rising edges are obtained as 3.03 ns and 71.75 ns for the load capacitances of 1 pF and 50 pF, respectively. From Figure 3.70, the settling times (2% of the final values) at falling edges are obtained as 5.6 ns and 76.4 ns for the load capacitances of 1 pF and 50 pF, respectively.

The current sourcing and sinking capabilities for the load capacitances of 1 pF and 50 pF are shown in Figure 3.71. The current sourcing/sinking capability are obtained as $4.83 I_b / 3.35 I_b$ and $18.69 I_b / 18.25 I_b$ for the load capacitances of 1 pF and 50 pF, respectively.

The input noise spectral density (INSD) of the proposed class-AB FVF cell-IV is shown in Figure 3.72. From the figure, it is observed that the proposed class-AB FVF cell-IV is less sensitive to the noise as the INSD is 10.87 nV/sqrt(Hz), in the flat portion of the curve for the different load capacitances.

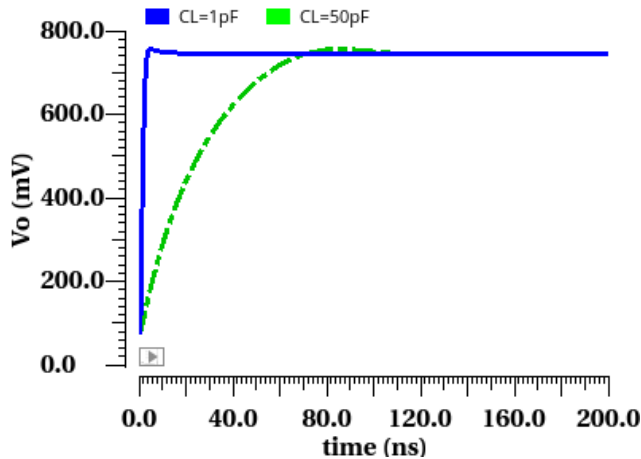


Figure 3.69 Output response of the proposed class-AB FVF cell-IV at the rising edge

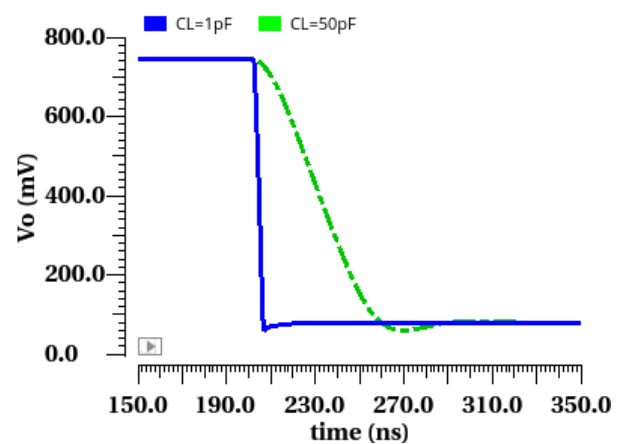


Figure 3.70 Output response of the proposed class-AB FVF cell-IV at the falling edge

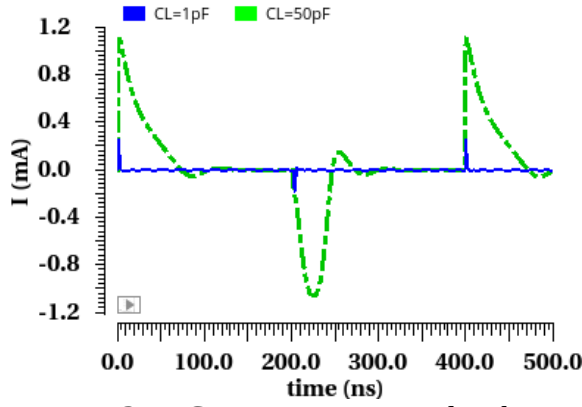


Figure 3.71 Current sourcing and sinking capabilities of the proposed class-AB FVF cell-IV

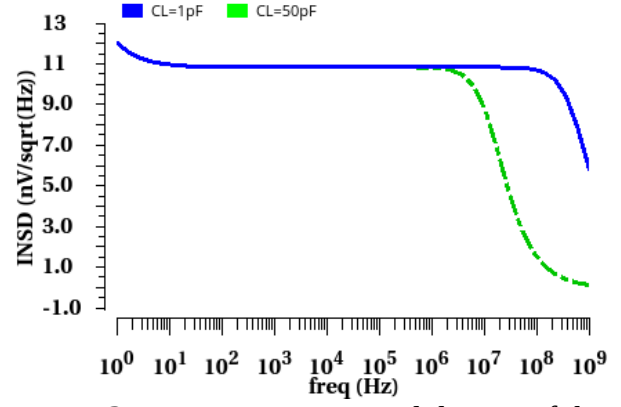


Figure 3.72 Input noise spectral density of the proposed class-AB FVF cell-IV

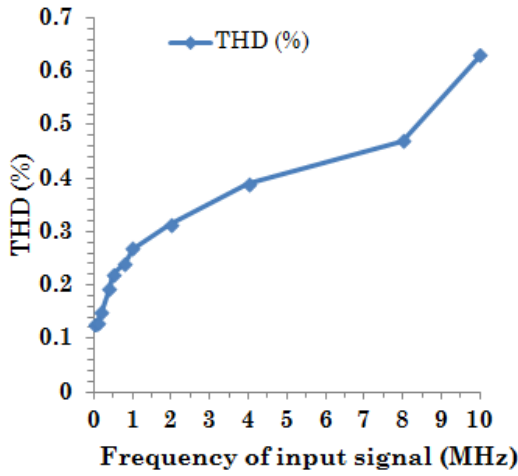


Figure 3.73 THD (%) versus frequency plot of the proposed class-AB FVF cell-IV

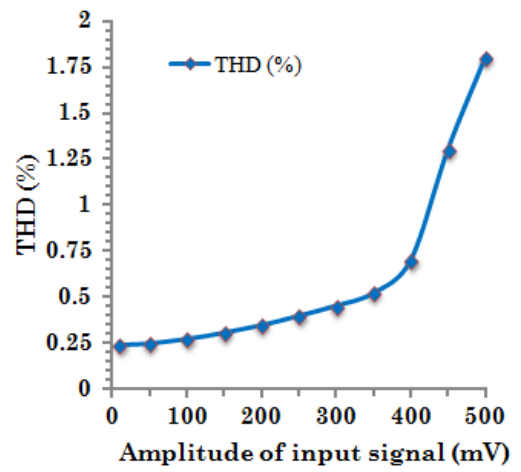


Figure 3.74 THD (%) versus amplitude plot of the proposed class-AB FVF cell-IV

The total harmonic distortion (THD) plot of the proposed class-AB FVF cell-IV is shown in Figure 3.73. For THD calculations, a sinusoidal signal of 200 mV peak-to-peak amplitude is applied at the input terminal. The plot shows the variation in THD when the frequency of the input signal is varied from 50 kHz to 10 MHz for the worst-case load capacitance of 50 pF. It is observed that the THD is less than 1% for the frequency range of 50 kHz to 10 MHz. The plot of THD versus input amplitude varying from 10 mV to 500 mV at a single input frequency of 1 MHz for the worst-case load capacitance of 50 pF is shown in Figure 3.74. The plot shows that the THD remains less than 2 % for the input amplitude varying from 10 mV to 500 mV.

The performance parameters of the proposed class-AB FVF cell-IV and reported FVF cells are listed in Table 3.8. From the table, it is evident that the proposed class-AB FVF cell-IV offers higher FOM_1 than the reported FVF cells [31–33, 35, 44, 46–47, 50–52] and higher FOM_2 than the reported FVF cells [31–33, 35, 39, 43–44, 46–47, 50–52]. The geometric mean of FOM_1 and FOM_2 has also been calculated for global figure of merit (FOM_3) and it is observed that the

proposed class-AB FVF cell-IV has $FOM_3=23.4$, which is higher than the reported FVF cells. Also, the proposed class-AB FVF cell-IV has a wider input/output swing, higher gain and lower output resistance than the reported FVF cells.

Table 3.8 Comparison of the proposed class-AB FVF cell-IV with FVF cells available in the literature

References→ Parameters ↓	[31]	[32]*	[33]	[35]	[39]	[43]*	[44]	[46]*	[47]	[50]	[51]	[52]*	Proposed cell-IV
Supply voltage (V)	±1.5	2.7	1.2	1.8	1.2	±1.65	±1.5	1.2	0.9	1.5	1.2	±0.9	1.5
Technology node (nm)	500	ALD 1106	350	350	65	500	500	350	500	500	180	180	180
Bias current (I_b) (μA)	30	55	2.5	8	9.8	10	30	40	16	50	65	30	60
Power (μW)	198	148.5	3	14.4	11	99	225	30	36	120	35	229	90
Input swing (V)	--	----	1	--	----	----	---	0.534	--	----	0.6	---	0.80
Output swing (V)	---	----	1	--	----	----	---	0.353	--	0.6	0.44	---	0.67
Gain	--	----	----	--	0.95**	----	--	0.78	0.96**	0.767	0.8	---	0.84, 0.99**
Bandwidth (MHz)	70 @10pF	2 @280pF	2.8 @10pF	6 @10pF	200 @1pF	13.1 @30pF	6.2 @100pF	200 @1pF	76 @10pF	15.4 @50pF	513.02 @1pF 45 @50pF @15pF	32 @50pF	815 @1pF 54 @50pF
R_{out} (Ω)	40	----	----	---	760	----	---	220	210	----	106.78	50	10
SR+ (V/ μs)	85 @10pF	3.75 @280pF	1.9 @10pF	9.3 @10pF	----	25 @30pF	3.5 @100pF	29 @15pF	10.3 @10pF	3.34 @50pF	31.28 @15pF	25.6 @50pF	289.9 @1pF 22.42 @50pF
SR- (V/ μs)	52.5 @10pF	1.82 @280pF	----	13.7 @10pF	----	----	4.3 @100pF	27 @15pF	10.3 @10pF	4 @50pF	27.7 @15pF	20.1 @50pF	201 @1pF 21.9 @50pF
Sourcing capability	28.33 I_b @10pF	16.7 I_b @280pF	7.6 I_b @10pF	11.62 I_b @10pF	----	80 I_b @30pF	26 I_b @100pF	11 I_b @15pF	34.3 I_b @10pF	3.34 I_b @50pF	19.77 I_b @15pF	43.3 I_b @50pF	4.83 I_b @1pF 18.69 I_b @50pF
Sinking capability	17.5 I_b @10pF	9.8 I_b @280pF	----	17.12 I_b @10pF	----	----	24 I_b @100pF	10.4 I_b @15pF	19 I_b @10pF	4 I_b @50pF	1.88 I_b @15pF	33.6 I_b @50pF	3.35 I_b @1pF 18.25 I_b @50pF
INSD (nV/ $\sqrt{Hz}$)	----	----	880 @1kHz	----	----	40 @50kHz	----	----	----	8.6	----	----	10.87 @100Hz
Area (μm^2)	----	----	----	----	----	11000	5400	----	----	----	342	13524	460.73
FOM_1	7.5 @10pF	9.81 @280pF	7.6 @10pF	11.625 @10pF	----	26.66 @30pF	9.6 @100pF	16.64 @15pF	7.6 @10pF	2.08 @50pF	4.19 @15pF	8 @50pF	3.5 @1pF 18.25 @50pF
FOM_2 ((MHz* μF) / μW)	3.53 @10pF	3.77 @280pF	9.33 @10pF	4.166 @10pF	18.18 @1pF	3.96 @30pF	2.75 @100pF	6.66 @1pF	21.11 @10pF	6.41 @50pF	19.28 @15pF	7 @50pF	9.05 @1pF 30 @50pF
FOM_3	5.14 @10pF	6.08 @280pF	8.42 @10pF	6.95 @10pF	----	10.28 @30pF	5.13 @100pF	----	12.66 @10pF	3.65 @50pF	8.9 @15pF	7.5 @50pF	5.62 @1pF 23.40 @50pF

*Experimental results **When body effect is not considered

3.5 Conclusion

In this chapter, four different class-AB FVF cells have been proposed namely class-AB FVF cell-I, class-AB FVF cell-II, class-AB FVF cell-III and class-AB FVF cell-IV. The large-signal and small-signal analyses of the proposed class-AB FVF cells have been performed. All the proposed class-AB FVF cells offer various improved electrical features, so these can be widely used as the basic building blocks in the designing of analog and mixed-signal circuits. The physical layouts and post-layout simulation results of the proposed class-AB FVF cells are presented to demonstrate their performance. The proposed class-AB FVF cells have also been compared with existing FVF cells available in the literature. The performance of the proposed class-AB FVF cells can be concluded as

- The proposed class-AB FVF cell-I offers good current sourcing and sinking capability. Also, due to the use of a replica biased scheme at the input transistor, the output voltage follows the input voltage with very little offset voltage and the gain is approximately unity. But, the proposed class-AB FVF cell-I shows limited bandwidth as the input voltage is applied at the bulk terminal.
- To overcome the drawback of limited bandwidth, the proposed class-AB FVF cell-II uses a gate-driven input transistor and offers improved bandwidth. Also, the level shifter introduced in the proposed class-AB FVF cell-II increases the input and output voltage swing. The proposed class-AB FVF cell-II also offers good current sourcing and sinking capabilities at the capacitive load due to the use of a bulk-driven transistor and a sinking transistor in the cell. But, the current sinking capability of the proposed class-AB FVF cell-II has been increased at the expense of an extra sinking transistor.
- The requirement of an extra transistor can be eliminated by introducing the quasi-floating gate technique at the sinking transistor and therefore, both of the techniques (the quasi-floating gate technique and the bulk-driven technique) are used in the proposed class-AB FVF cell-III which increase its sourcing and sinking current capabilities as compared to the proposed class-AB FVF cell-II. Also, the proposed class-AB FVF cell-III shows a high symmetric slew rate and an improved bandwidth at the large capacitive loads. However, the output resistance of the proposed class-AB FVF cell-III is not low enough.
- In the proposed class-AB FVF cell-IV, the folding transistor provides an alternate path for the sourcing current, which results in low output resistance while the level shifter increases the

input/output voltage swing. The proposed class-AB FVF cell-IV also offers a high current sourcing/sinking capability and a high symmetric slew rate.

The comparison of all of the proposed class-AB FVF cells has also been done using three figures of merit (FOM_1 and FOM_2 and FOM_3). Based on these three figures of merit, it can be concluded that the proposed class-AB FVF cell-IV has the highest FOM_3 than the other proposed FVF cells.

CHAPTER-4

PROPOSED CURRENT MIRRORS USING CLASS-AB FLIPPED VOLTAGE FOLLOWER CELLS

4.1 Introduction

Nowadays, in the market of portable electronic devices, consumers are interested in devices with good battery life. The life of the battery can be increased if the electronic devices consume less power. The scaling down of CMOS technology has forced the analog circuit designers to operate the circuits at low supply voltage to reduce the power consumption [61]. However, the design of low-voltage and low-power analog circuits is a challenging task as the performance of analog circuits in terms of voltage swing, bandwidth and delay degrade with the scaling of the supply voltage. The various low-voltage/low-power (LV/LP) transistor implementation techniques have been used to operate the analog circuits at low voltage such as bulk-driven MOSFETs, level shifter technique, sub-threshold MOSFETs, self-cascode MOSFETs and floating-gate MOSFETs (FGMOS). Although these techniques work efficiently to reduce the supply voltage but offer certain limitations such as bulk-driven technique is process dependent, level shifter technique increases the silicon area, sub-threshold MOSFETs degrade the linearity and frequency response, self-cascode MOSFETs require multiple threshold technology and charge gets trapped during fabrication of floating-gate which leads to DC offsets in FGMOS. Flipped voltage follower (FVF) cell is another LV/LP technique that has been efficiently used in the design of various low-voltage and low-power analog and mixed-signal circuits. FVF cell is also considered as a current sensing cell due to its low output resistance. The performance of analog building blocks can be enhanced by using FVF cells. The various current-mode analog building blocks have emerged with the progress in the current-mode analog signal processing in the last few decades [118]. The current mirror is one of the important building blocks amongst the various current-mode analog building blocks which is used for active load, current biasing, level shifting, etc. [119–121]. It is also used to realize various active blocks such as operational amplifiers, analog filters, operational transconductance amplifiers, data converters, current conveyors, low-dropout regulators, etc. [122–127].

The conventional current mirror is formed by a transistors pair where the gates of both the transistors are connected and one of them is diode-connected. But, the conventional current mirror suffers from low output to input resistance ratio. The current mirror topologies with high output resistance have been reported to overcome this drawback [128]. However, this has been

achieved at the expense of an increase in the supply voltage. These current mirrors cannot meet today's industry trends due to the high accuracy and low power supply voltage requirement. To meet today's industry demands various current mirror structures using different techniques have been reported in the literature [66, 72, 129–137]. M. Madhushankara *et al.* [129] and A. Mishra *et al.* [130] reported the Wilson current mirror and double cascode current mirror, respectively using the floating gate technique. The floating-gate technique lowers the requirement of supply voltage and hence reduces the power dissipation but it results in DC offsets. The bulk-driven self-biased cascode mirror (BDSBCM) has been reported by B. Aggarwal *et al.* [131] and the improved version of BDSBCM using a quasi-floating gate technique has been presented by N. Raj *et al.* [132]. However, both the mirrors [131-132] suffer from the limitations of high input resistance and low output resistance. N. Raj *et al.* [133] overcome the limitation of the current mirror reported [132] by using a regulated cascode structure at the output of the mirror and offers high output resistance while consuming large power. The simple and cascode current mirrors using the bulk-driven technique have been presented by K. Sooksood *et al.* [134] but the simple current mirror shows a large error in copying the current. The current mirror with enhanced bandwidth has been presented by M. Tikyani *et al.* but it shows a limited current mirroring range [135]. The resistor based current mirror reported by L. Safari *et al.* [136] shows large input resistance. M. P. Garde *et al.* [137] reported current mirror based on floating-gate and quasi-floating gate techniques to achieve wide swing. Due to the low output resistance and low voltage operation of FVF cell, it has also been extensively used in the designing of the current mirrors [66], [72]. The FVF based current mirror [66] uses the dynamic threshold MOS (DTMOS) technique to operate under low voltage but the DTMOS technique requires triple-well technology. The current mirror based on folded FVF cell [72] shows less current transfer accuracy and poor current mirroring range because the FVF cell shows class-A behaviour.

Therefore, this chapter presents four different current mirrors namely proposed current mirror-I, proposed current mirror-II, proposed current mirror-III and proposed current mirror-IV as applications of proposed class-AB FVF cells discussed in section 3.2 of chapter 3 to validate their performance. These proposed current mirrors offer different improved electrical features such as input resistance, output resistance, current mirroring range, error, minimum input voltage and minimum output voltage.

This chapter is organized as follows. Section 4.2 proposes four different current mirrors and the small-signal analyses of proposed current mirrors are discussed in section 4.3. Section 4.4

addresses the simulation results of the proposed current mirrors. The chapter is concluded in section 4.5.

4.2 Proposed current mirrors

In this section, four current mirrors that are designed using proposed class-AB FVF cells (discussed in chapter 3) have been presented to demonstrate their effectiveness. Since class-AB FVF cells have low output resistances, these are used at the input stage of proposed current mirrors.

4.2.1 Proposed current mirror-I

The proposed current mirror-I uses a class-AB FVF cell-I (Figure 3.1) consisting of transistors M_1 to M_8 at the input stage as shown in Figure 4.1. The class-AB FVF cell-I in Figure 4.1 provides a low resistance node (source of transistor M_1) due to the negative feedback formed by transistor M_3 . The transistors M_2 and M_5 are used to generate the bias voltage V_r which is required at the gate terminals of M_1 and M_{10} for proper biasing. The input current is injected at the source terminal of the transistor M_1 which acts as a current sensing node. The current through transistor M_1 is kept constant by the transistor M_4 . The input current variations are absorbed by the transistor M_3 by changing its gate-to-source voltage (V_{GS3}). The variations in voltage V_{GS3} are reflected to the transistor M_9 . The current $2I_b + I_{in}$ flowing through transistor M_3 is mirrored to transistor M_9 where both the transistors M_3 and M_9 have the same aspect ratios and gate-to-source voltages.

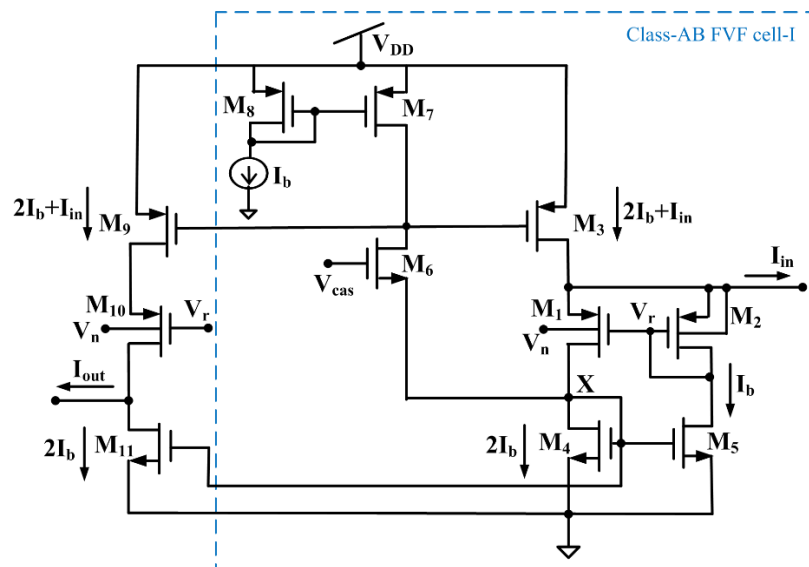


Figure 4.1 Proposed current mirror-I

To mirror the current accurately, transistor M_{10} is connected in cascode with transistor M_9 with its gate terminal tied to the gate terminal of transistor M_1 . This forces the drain-to-source voltages of transistors M_3 and M_9 forming a primary current mirror pair to be equal. Since the output resistance of FVF cell-I is not low enough, the input resistance of the proposed current mirror-I is high as the current flowing through the input node modifies its voltage.

4.2.2 Proposed current mirror-II

The proposed current mirror-II shown in Figure 4.2 overcomes the limitation of the input resistance of current mirror-I by using a class-AB FVF cell-II (Figure 3.2) consisting of transistors M_1 - M_5 at the input stage. The proposed current mirror-II achieves low input resistance because the FVF cell-II offers lower output resistance than FVF cell-I. Also, instead of using simple cascode transistors, the regulated cascode structure [58] consisting of transistors M_8 , M_9 and current source I_b is applied at the output stage to increase the output resistance of the proposed current mirror-II. As the output resistance of class-AB FVF cell-II is low, the drain of transistors $M_{1a,1b}$ acts as the input node for current injection (I_{in}) in the proposed current mirror-II. The transistors M_3 and M_7 with their bulk terminals connected to the drain end act as adaptable current sources (I_b). The bias voltage (V_b) applied at the gate terminals of transistors M_3 and M_7 is generated by a diode-connected transistor M'_3 (replica of transistor M_3). The bulk terminal of the transistor M'_3 is connected to its drain terminal and a sinking current source I_b is connected at the drain terminal.

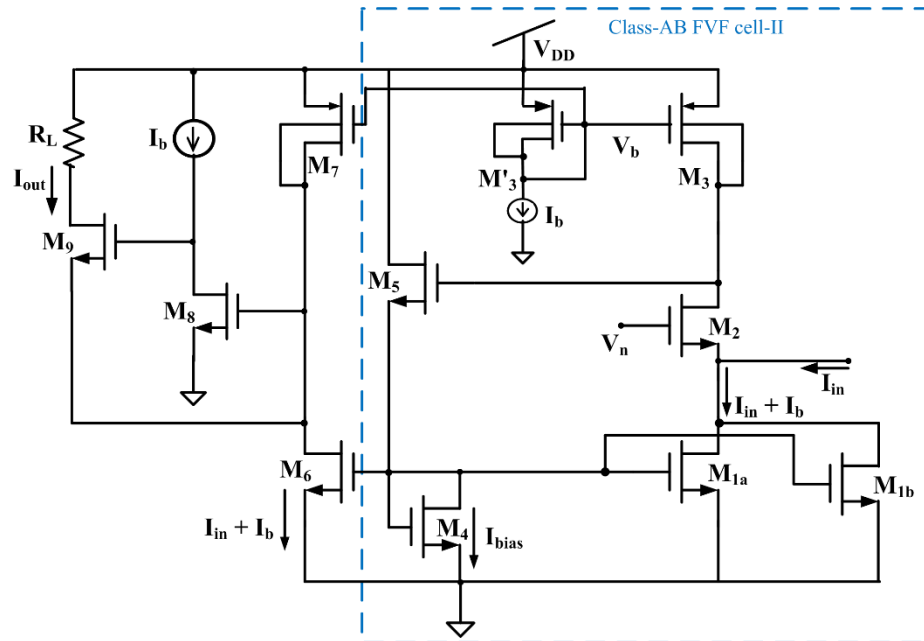


Figure 4.2 Proposed current mirror-II

The low input resistance at the drain of the transistor M_1 (parallel combination of transistors M_{1a} and M_{1b}) allows the sourcing of large input current variations and flow of current $I_{in}+I_b$. The transistor M_6 copies the current of transistor M_1 as the aspect ratios and gate-to-source voltages of transistors M_1 and M_6 are equal. The current range of the proposed current mirror-II is extended to a certain extent by using the transistor M_5 . The current source (I_{bias}) used to bias transistor M_5 is implemented using transistor M_4 . As the current I_b is flowing through transistor M_7 , the output current becomes equal to the input current. The regulated cascode structure consisting of inverting amplifier (transistor M_8 and current source I_b) maintains the drain voltage of transistor M_6 constant. The regulated cascode output boosts the output resistance of the proposed current mirror-II by the gain of the inverting amplifier. Since the current driving capability of FVF cell-II used at the input stage of the proposed current mirror-II is limited, it limits the current mirroring range of the proposed current mirror-II.

4.2.3 Proposed current mirror-III

Figure 4.3 shows the proposed current mirror-III designed by using a class-AB FVF cell-III (Figure 3.3) at the input stage. The FVF cell-III offers high current driving capability which improves the current mirroring range of the proposed current mirror-III. The super cascode structure is used to boost the gain of the output stage and output resistance of the current mirror. The bulk-driven transistors M_3 and M_9 set the bias current (I_{bias}) in the input branch and output branch, respectively. The fixed DC voltage V_{bias} applied at the gate terminals of transistors M_3 and M_9 is generated by a diode-connected transistor M'_3 (replica of transistor M_3). The bulk terminal of the transistor M'_3 is connected to its drain terminal and a sinking current source I_{bias} is connected at the drain terminal. The proposed current mirror-III offers low input resistance at node 'D₂' due to the use of the FVF cell-III. The input current (I_{in}) is injected at the current sensing node 'D₂' and transistor M_2 allows the flow of current $I_{in}+I_{bias}$. The transistor M_8 mirrors the same current because the aspect ratios and gate-to-source voltages of transistors M_2 and M_8 are kept equal. To accurately mirror the current, the transistor M_{1a} with its gate tied with the gate of transistor M_1 is connected at the drain of transistor M_8 which forces the drain-to-source voltages of transistors M_2 and M_8 forming a primary current mirror pair to be equal. Due to the high current driving capability of the FVF cell-III, the transistor M_2 can sink a large input current which increases the current mirroring range of the proposed current mirror-III. The bulk-driven transistor M_9 acts as the replica of transistor M_3 to generate bias current I_{bias} and get the output current (I_{out}) equal to the input current (I_{in}).

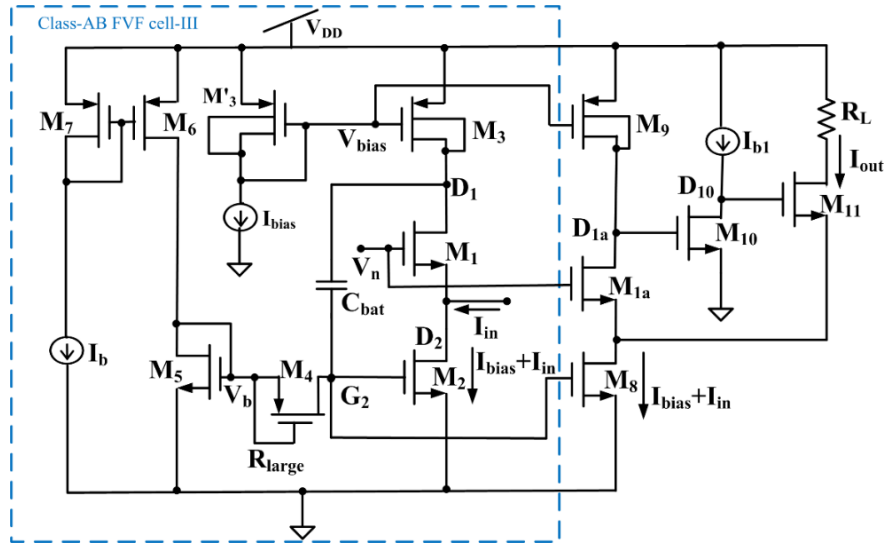


Figure 4.3 Proposed current mirror-III

To enhance the output resistance, output cascode transistor M_{11} is driven by the drain of transistor M_{1a} . As the polarity at the drain of transistor M_{1a} is reversed, transistor M_{10} and current source I_{b1} are used as an inverting stage between the drain of transistor M_{1a} and the gate of transistor M_{11} . The inverting stage drives transistor M_{11} and provides additional gain boosting. The output current I_{out} is delivered to the transistor M_{11} through the load resistance R_L . The three transistors (M_{1a} , M_{10} , M_{11}) and two biasing currents (I_{bias} , I_{b1}) are used to form the super cascode structure [58] which enhances the output resistance of the proposed current mirror-III. In the super cascode structure, there will be no current through transistor M_{11} when $I_{in}=0$. Therefore, super cascode structure employed at the output of the proposed current mirror-III enhances the output resistance at the expense of a decrease in DC accuracy. However, without a super cascode structure, there is no such problem when $I_{in}=0$. Also, the proposed current mirror-III shows high input resistance as compared to the proposed current mirror-II because the class-AB FVF cell-III used at the input stage of the proposed current mirror-III shows high output resistance as compared to class-AB FVF cell-II used at the input of proposed current mirror-II.

4.2.4 Proposed current mirror-IV

The proposed current mirror-IV shown in Figure 4.4 overcomes the limitation of the input resistance of the proposed current mirror-III because it uses a class-AB FVF cell-IV (Figure 3.4) having low output resistance at the input stage. The transistors M_{1-6} and resistor R_b constitute class-AB FVF cell-IV at the input stage of the proposed current mirror-IV. The bias current (I_b) flowing through transistors M_3 and M_{11} at the input and output stage, respectively is generated by

the DC bias voltage (V_{bias}) applied at their gate terminals. This bias voltage is generated by using a replica transistor M'_3 with sinking current source I_b connected at its drain terminal. The shunt feedback provided by transistors M_2 and M_5 reduces the resistance at the drain of transistor M_2 (node ' D_2 '). So, the input current injected at the drain of transistor M_2 does not modify the voltage at node ' D_2 '. The node ' D_2 ' sources large input current variations in transistor M_2 . These current variations are converted to voltage variations at the gate of transistor M_2 (node ' D_6 ') by class-AB FVF cell-IV. The voltage at node ' D_6 ' copies the current flowing through transistor M_2 i.e. $I_{in}+I_b+I_5$ in transistor M_{13} . The drain-to-source voltages of transistors M_2 and M_{13} are maintained equal to accurately mirror the current by connecting transistor M_{12} at the drain of transistor M_{13} . The gate terminal of transistor M_{12} is connected with the gate terminal of transistor M_1 . To get the output current equal to the input current, currents I_5 and I_b need to be subtracted from the current flowing through transistor M_{13} . The current I_b is generated through transistor M_{11} connected at the drain of transistor M_{12} . The transistor M_7 connected at the drain of transistor M_5 allows the flow of current $I_5/2$, which is copied to transistor M_8 as the aspect ratios and gate-to-source voltages of transistors M_7 and M_8 are equal. The same current $I_5/2$ is flowing through transistor M_9 connected at the drain terminal of transistor M_8 . As the aspect ratio of transistor M_{10} is doubled as that of transistor M_9 and their gate-to-source voltages are also equal, the current I_5 is flowing through transistor M_{10} . The transistors M_{10} and M_{11} provide currents I_5 and I_b , respectively, therefore, the output current (I_{out}) becomes equal to the input current (I_{in}).

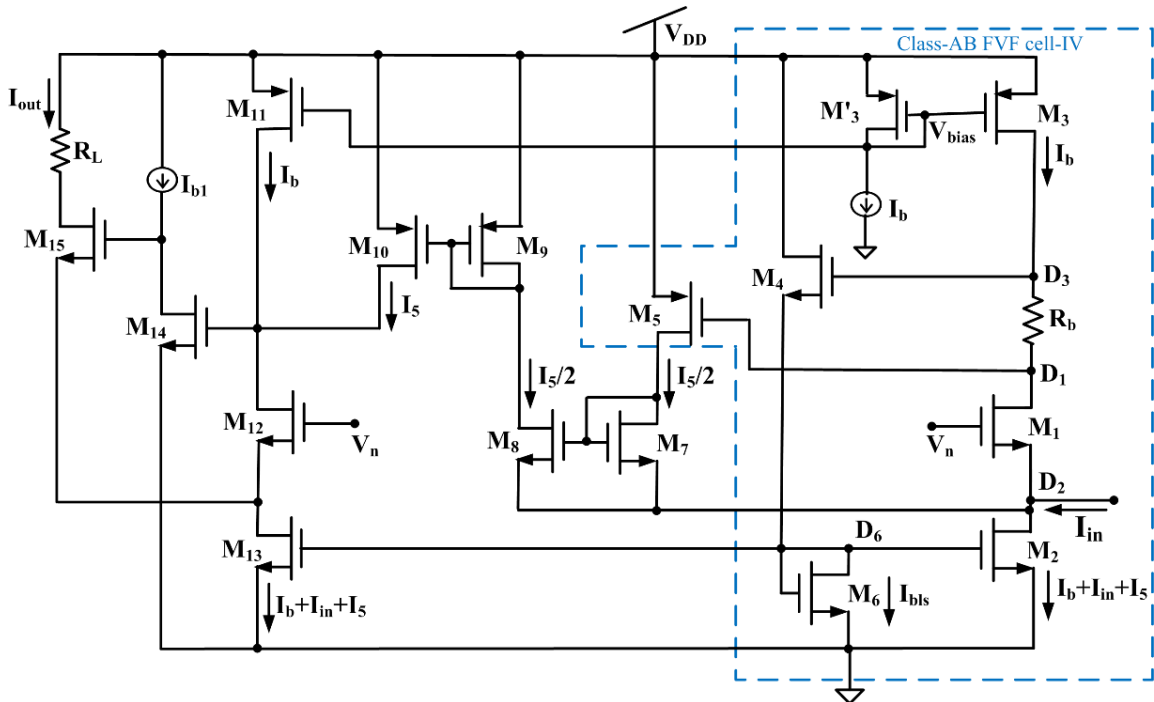


Figure 4.4 Proposed current mirror-IV

The super cascode structure consisting of transistors (M_{12} , M_{14} and M_{15}) and bias currents (I_b and I_{b1}) are connected at the output of the proposed current mirror-IV to enhance the output resistance. The output transistor M_{15} is driven through the drain of transistor M_{12} by using an inverting stage consisting of transistor M_{14} and bias current I_{b1} . The inverting stage provides additional gain which increases the output resistance of the proposed current mirror-IV. The resistor connected at the drain of transistor M_{15} delivers the output current equal to the input current. The proposed current mirror-IV suffers from the same limitation as to the proposed current mirror-III because there will be no current through transistor M_{15} when $I_{in}=0$ in the super cascode structure. Therefore, super cascode structure enhances the output resistance at the expense of a decrease in DC accuracy but there is no such problem in the proposed current mirror-IV when $I_{in}=0$ without a super cascode structure.

4.3 Analysis of proposed current mirrors

This section presents the analysis of all of the proposed current mirrors discussed in section 4.2.

4.3.1 Analysis of proposed current mirror-I

In this section, small-signal analysis and stability analysis of the proposed current mirror-I are presented.

4.3.1.1 Small-signal analysis of proposed current mirror-I

This section discusses the analyses of input resistance, output resistance, transfer function and bandwidth of the proposed current mirror-I using small-signal equivalent models.

4.3.1.1.1 Input resistance

The small-signal equivalent model of the proposed current mirror-I shown in Figure 4.5 is used to calculate the input resistance. In the model, the transconductance of transistor M_i is represented by g_{mi} , the transconductance of transistor M_i due to body effect is represented by g_{mbi} and the output resistance of transistor M_i is represented by r_{oi} , where i varies from 1 to 7. Applying KCL at node 'D₆', we get

$$v_{d6} = (g_{m6} + g_{mb6})r_{o6}v_{d1} \quad (4.1)$$

In equation (4.1), it is assumed that $r_{o7} \gg r_{o6}$ and $g_m r_o \gg 1$.

Applying KCL at node 'G₁' and assuming $g_m r_o \gg 1$, we get equation (4.2).

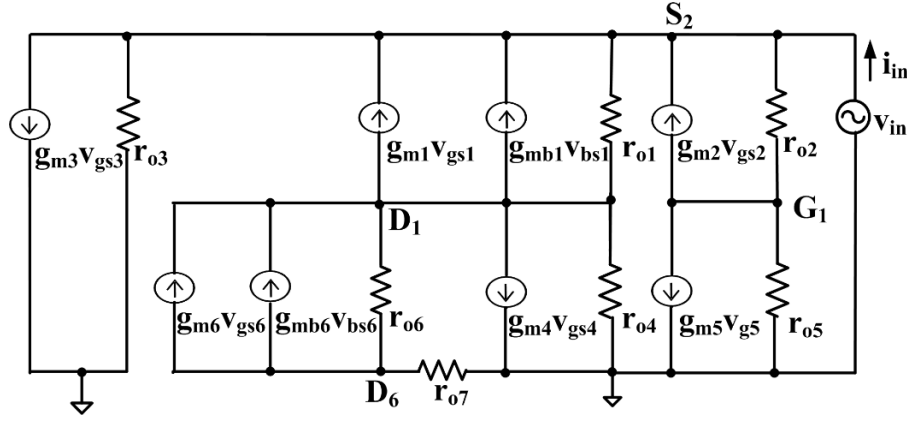


Figure 4.5 Small-signal equivalent model of the proposed current mirror-I to calculate the input resistance

$$v_{g1} = v_o - \frac{g_{m5}}{g_{m2}} v_{d1} \quad (4.2)$$

Applying KCL at node 'D₁', we get equation (4.3).

$$(g_{m1} + g_{mb1})v_{in} = g_{m1}v_{g1} + (g_{m4} + g_{m6} + g_{mb6})v_{d1} - \frac{v_{d6}}{r_{o6}} \quad (4.3)$$

Substituting the values of v_{d6} and v_{g1} from equations (4.1) and (4.2), respectively in equation (4.3), the value of v_{d1} can be written as

$$v_{d1} = \frac{g_{mb1}}{g_{m4}} v_{in} \quad (4.4)$$

In equation (4.4), it is assumed that $g_{m4}g_{m2} \gg g_{m1}g_{m5}$.

Applying KCL at node 'S₂', we get

$$i_{in} = (v_{in} - v_{g1})(g_{m1} + g_{m2}) + g_{mb1}v_{in} + g_{m3}v_{d6} - \frac{v_{d1}}{r_{o1}} \quad (4.5)$$

Using equations (4.1), (4.2), (4.4) and (4.5), the expression of input resistance (R_{in}) of the proposed current mirror-I is given as

$$R_{in} = \frac{g_{m2}g_{m4}}{g_{mb1}g_{m2}g_{m4} + g_{mb1}g_{m5}(g_{m1} + g_{m2}) + g_{mb1}g_{m2}g_{m3}(g_{m6} + g_{mb6})r_{o6}} \quad (4.6)$$

In equation (4.6), it is assumed that $g_m r_o \gg 1$.

4.3.1.1.2 Output resistance

The output resistance of the proposed current mirror-I is calculated using the small-signal equivalent model shown in Figure 4.6. In the model, g_{m10} and g_{mb10} represent the transconductance of transistor M₁₀ and transconductance of transistor M₁₀ due to body effect,

respectively. The output resistances of transistors M_9 and M_{10} are represented by r_{o9} and r_{o10} , respectively.

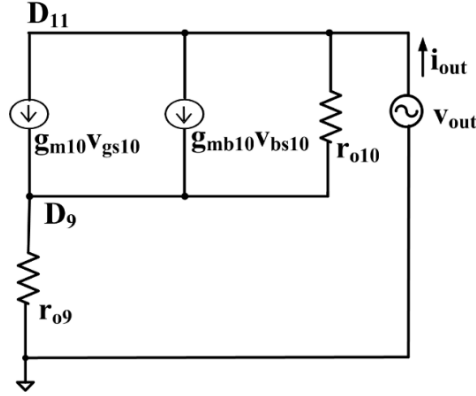


Figure 4.6 Small-signal equivalent model of the proposed current mirror-I to calculate the output resistance

By applying KCL at node ‘D₉’, we get

$$\frac{V_{d9}}{r_{o9}} = \frac{V_{out} - V_{d9}}{r_{o10}} - (g_{m10} + g_{mb10})V_{d9} \quad (4.7)$$

The drain voltage at node ‘D₉’ (V_{d9}) can be written as

$$V_{d9} = i_{out} r_{o9} \quad (4.8)$$

Using equations (4.7) and (4.8), the output resistance (R_{out}) of the proposed current mirror-I is expressed as

$$R_{out} = (g_{m10} + g_{mb10})r_{o9}r_{o10} + r_{o9} + r_{o10} \cong (g_{m10} + g_{mb10})r_{o9}r_{o10} \quad (4.9)$$

4.3.1.1.3 Transfer function and bandwidth

To calculate the transfer function and bandwidth of the proposed current mirror-I, a high-frequency small-signal equivalent model is shown in Figure 4.7. The transistors M_2 and M_5 which generate bias gate voltage V_r are not considered in the model. The various parasitic capacitances at the node ‘D₁’ are represented by capacitance $C_A (=C_{gs4} + C_{gs6} + C_{bs6} + C_{gs11})$. The capacitance $C_B (=C_{gs3} + C_{gs9})$ represents the parasitic capacitance at node ‘D₆’, capacitance $C_C (=C_{gs1} + C_{bs1})$ represents the capacitance at node ‘S₂’ and capacitance $C_D (=C_{gs10} + C_{bs10})$ denotes the parasitic capacitance at node ‘D₉’. Applying KCL at nodes ‘D₁’, ‘S₂’ and ‘D₆’, we get

$$(g_{m1} + g_{mb1})v_{s2}(s) = (g_{m4} + g_{m6} + g_{mb6} + sC_A)v_{d1}(s) \quad (4.10)$$

$$i_{in}(s) = -(g_{m1} + g_{mb1} + sC_C)v_{s2}(s) - g_{m3}v_{d6}(s) \quad (4.11)$$

$$v_{d6}(s) \left(sC_B + \frac{1}{r_{o7}} \right) = (g_{m6} + g_{mb6})v_{d1}(s) \quad (4.12)$$

Substituting the value of $v_{d1}(s)$ from equation (4.12) in equation (4.10), we get

$$v_{s2}(s) = \frac{(g_{m4} + g_{m6} + g_{mb6} + sC_A) \left(sC_B + \frac{1}{r_{o7}} \right)}{(g_{m1} + g_{mb1})(g_{m6} + g_{mb6})} v_{d6}(s) \quad (4.13)$$

Using equations (4.11) and (4.13), the input current ($i_{in}(s)$) is expressed as

$$-i_{in}(s) = \frac{(g'_{m1} + sC_C)(g_{m4} + g'_{m6} + sC_A) \left(sC_B + \frac{1}{r_{o7}} \right) v_{d6}(s) + g'_{m1}g_{m3}g'_{m6}v_{d6}(s)}{g'_{m1}g'_{m6}} \quad (4.14)$$

where $g'_{m1} = g_{m1} + g_{mb1}$ and $g'_{m6} = g_{m6} + g_{mb6}$.

At the output side, by applying KCL at nodes 'D₁₁' and 'D₉', we get

$$i_{out}(s) = -g_{m11}v_{d1}(s) + (g_{m10} + g_{mb10})v_{d9}(s) \quad (4.15)$$

$$v_{d9}(s) = -\frac{g_{m9}}{(g_{m10} + g_{mb10} + sC_D)} v_{d6}(s) \quad (4.16)$$

Using equations (4.12), (4.15) and (4.16), the output current ($i_{out}(s)$) is expressed as

$$-i_{out}(s) = \frac{g_{m11} \left(sC_B + \frac{1}{r_{o7}} \right) (g'_{m10} + sC_D) v_{d6}(s) + g'_{m6}g_{m9}g'_{m10}v_{d6}(s)}{g'_{m6}(g'_{m10} + sC_D)} \quad (4.17)$$

where $g'_{m10} = g_{m10} + g_{mb10}$.

Using equations (4.14) and (4.17), the transfer function ($A_i(s)$) is given as

$$A_i(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{g'_{m1}g_{m11} \left(sC_B + \frac{1}{r_{o7}} \right) (g'_{m10} + sC_D) + g'_{m1}g'_{m6}g_{m9}g'_{m10}}{((g'_{m1} + sC_C)(g'_{m10} + sC_D)(g_{m4} + g'_{m6} + sC_A) \left(sC_B + \frac{1}{r_{o7}} \right) + g'_{m1}g_{m3}g'_{m6}(g'_{m10} + sC_D))} \quad (4.18)$$

Assuming $g_{m3} = g_{m9}$, $g_{m4} = g_{m11}$, $\frac{1}{r_{o7}} \gg g_{m3,9}$ and $g_{m4} \gg g'_{m6}$, the $A_i(s)$ is given in equation (4.19).

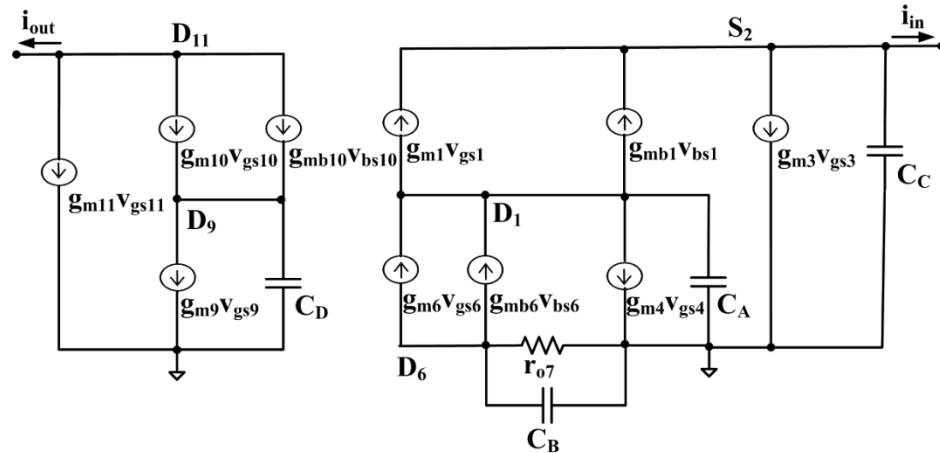


Figure 4.7 High-frequency small-signal equivalent model of the proposed current mirror-I to calculate the transfer function

$$A_i(s) = \frac{g'_{m1}g_{m11}}{(g'_{m1} + sC_C)(g_{m11} + sC_A)} \quad (4.19)$$

From equation (4.19), the poles of the proposed current mirror-I are given as

$$\omega_{p1} = -g'_{m1}/C_C \text{ and } \omega_{p2} = -g_{m11}/C_A \quad (4.20)$$

where $\omega_{p1,2}$ denote the location of poles.

To determine the bandwidth [138], the $A_i(s)$ with one zero and three poles can be written as

$$A_i(s) = \frac{(1 + s/\omega_{z1})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \quad (4.21)$$

Substituting $s=j\omega$ (where ω is the operating frequency), equation (4.21) is modified as

$$A_i(j\omega) = \frac{(1 + j\omega/\omega_{z1})}{(1 + j\omega/\omega_{p1})(1 + j\omega/\omega_{p2})(1 + j\omega/\omega_{p3})} \quad (4.22)$$

By taking the squared magnitude of equation (4.22), we get

$$|A_i(j\omega)|^2 = \frac{(1 + \omega^2/\omega_{z1}^2)}{(1 + \omega^2/\omega_{p1}^2)(1 + \omega^2/\omega_{p2}^2)(1 + \omega^2/\omega_{p3}^2)} \quad (4.23)$$

According to the definition of 3-dB bandwidth ($\omega = \omega_o$), $|A_i(j\omega)|^2 = \frac{1}{2}$ and therefore, equation (4.23) can be expressed as

$$\frac{1}{2} = \frac{(1 + \omega_o^2/\omega_{z1}^2)}{1 + \omega_o^2(1/\omega_{p1}^2 + 1/\omega_{p2}^2 + 1/\omega_{p3}^2) + \omega_o^4(1/\omega_{p1}^2\omega_{p2}^2 + 1/\omega_{p2}^2\omega_{p3}^2 + 1/\omega_{p3}^2\omega_{p1}^2) + \omega_o^6(1/\omega_{p1}^2\omega_{p2}^2\omega_{p3}^2)} \quad (4.24)$$

As ω_o is usually smaller than the frequencies of all poles and zeros, the terms containing ω_o^4 and ω_o^6 can be neglected and hence equation (4.24) reduces to

$$1 + \omega_o^2(1/\omega_{p1}^2 + 1/\omega_{p2}^2 + 1/\omega_{p3}^2) = 2(1 + \omega_o^2/\omega_{z1}^2) \quad (4.25)$$

From equation (4.25), the ω_o is obtained as

$$\omega_o = 1/\sqrt{\left(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2} + \frac{1}{\omega_{p3}^2}\right) - \left(\frac{2}{\omega_{z1}^2}\right)} \quad (4.26)$$

The ω_o for any number of poles and zeros in a transfer function can be generalized by the relation as

$$\omega_o = 1/\sqrt{\left(\frac{1}{\omega_{p1}^2} + \frac{1}{\omega_{p2}^2} \dots\right) - \left(\frac{2}{\omega_{z1}^2} + \frac{2}{\omega_{z2}^2} \dots\right)} \quad (4.27)$$

Thus, substituting pole values from equation (4.20) in equation (4.27), the ω_o of the proposed current mirror is given in equation (4.28).

$$\omega_o \approx \frac{1}{\sqrt{\frac{1}{(g'_{m1}/C_C)^2} + \frac{1}{(g_{m11}/C_A)^2}}} = \frac{g'_{m1}g_{m11}}{\sqrt{C_C^2 g_{m11}^2 + C_A^2 g'^2_{m1}}} \quad (4.28)$$

4.3.1.2 Stability analysis

The stability of the proposed current mirror-I is evaluated using open-loop gain analysis. There is an independent loop present at the input stage of the proposed current mirror-I. The open-loop analysis at the input stage i.e. class-AB FVF cell-I has already been performed in section 3.3.1.3 of chapter 3 which shows that the class-AB FVF cell-I is stable.

4.3.2 Analysis of proposed current mirror-II

In this section, small-signal analysis and stability analysis of the proposed current mirror-II are presented.

4.3.2.1 Small-signal analysis of proposed current mirror-II

The analyses of input resistance, output resistance, transfer function and bandwidth of the proposed current mirror-II using small-signal equivalent models have been addressed in this section.

4.3.2.1.1 Input resistance

The input resistance of the proposed current mirror-II is calculated by using the small-signal equivalent model shown in Figure 4.8. In the model, g_{m1} states for $g_{m1a} + g_{m1b}$, r_{o1} states for $r_{o1a} || r_{o1b}$. The symbols $g_{m1a,1b,2,5}$ denote the transconductances of transistor $M_{1a,1b,2,5}$, $g_{mb2,3,5}$ represent the transconductances of transistors $M_{2,3,5}$ due to body effect and $r_{o1a,1b,2,5}$ are the output resistances of transistors $M_{1a,1b,2,5}$. By applying KCL at node 'D_{1a}', the relation is obtained as

$$g_{m2}(-v_{in}) - g_{mb2}v_{in} + \frac{v_{g5} - v_{in}}{r_{o2}} = g_{m1}v_{g1a} + \frac{v_{in}}{r_{o1}} - i_{in} \quad (4.29)$$

The value of v_{g1a} of transistor M_{1a} can be written as

$$v_{g1a} = \frac{(g_{m5}v_{g5} - g_{mb5}v_{s5})(r_{o5} || 1/g_{m4})}{1 + g_{m5}(r_{o5} || 1/g_{m4})} \quad (4.30)$$

In equations (4.29) and (4.30), $v_{g1a,5}$ are the gate voltages of transistors $M_{1a,5}$. In equation (4.30), the value of $g_{mb5} \ll g_{m5}$, so $g_{mb5}v_{s5}$ is negligible as compared to $g_{m5}v_{g5}$ and also the value of $r_{o5} \ll 1/g_{m4}$, so $1/g_{m4}$ is eliminated.

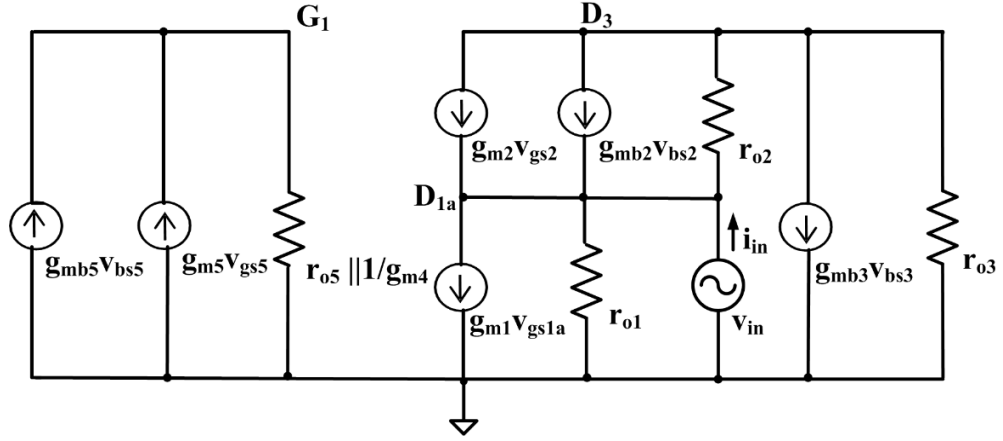


Figure 4.8 Small-signal equivalent model of the proposed current mirror-II to calculate the input resistance

Using the above approximations, equation (4.30) reduces to equation (4.31).

$$v_{g1a} = \frac{g_{m5}r_{o5}V_{g5}}{1 + g_{m5}r_{o5}} \quad (4.31)$$

Substituting the value of v_{g1a} from equation (4.31) in equation (4.29), we get

$$g_{m2}(-v_{in}) - g_{mb2}v_{in} + \frac{V_{g5} - v_{in}}{r_{o2}} = \frac{g_{m1}g_{m5}r_{o5}V_{g5}}{1 + g_{m5}r_{o5}} + \frac{v_{in}}{r_{o1}} - i_{in} \quad (4.32)$$

Using approximation $g_m r_o \gg 1$, equation (4.32) can be written as

$$v_{in}(g_{m2} + g_{mb2}) = i_{in} - v_{g5}g_{m1} \quad (4.33)$$

Applying KCL at node 'D3', we get

$$g_{m2}(-v_{in}) - g_{mb2}v_{in} + \frac{V_{g5} - v_{in}}{r_{o2}} = -g_{mb3}V_{g5} - \frac{V_{g5}}{r_{o3}} \quad (4.34)$$

Assuming $g_m r_o \gg 1$, equation (4.34) reduces to

$$v_{g5} = \frac{v_{in}(g_{m2} + g_{mb2})}{g_{mb3}} \quad (4.35)$$

Substituting v_{g5} from equation (4.35) in equation (4.33), the input resistance (R_{in}) is obtained as

$$R_{in} = \frac{g_{mb3}}{(g_{m2} + g_{mb2})(g_{m1} + g_{mb3})} \quad (4.36)$$

4.3.2.1.2 Output resistance

To calculate the output resistance of the proposed current mirror-II, the small-signal equivalent model shown in Figure 4.9 is used. Applying KCL at node 'D9', we get

$$i_{out} = g_{m9}(v_{g9} - v_{d6}) - g_{mb9}v_{d6} + \frac{v_{out} - v_{d6}}{r_{o9}} \quad (4.37)$$

The values of v_{d6} and v_{g9} are given in equation (4.38).

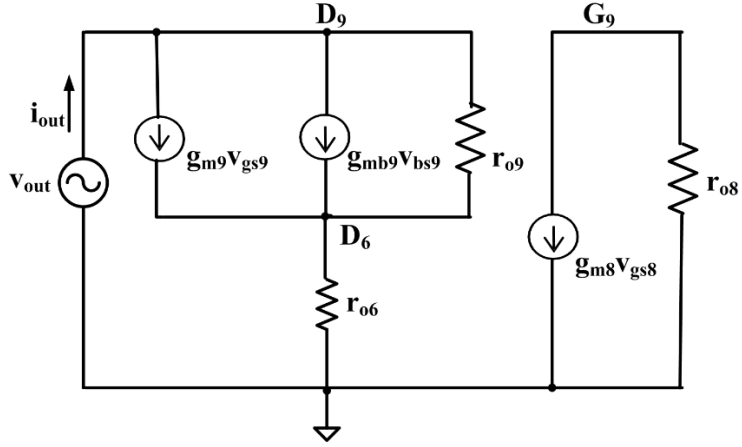


Figure 4.9 Small-signal equivalent model of the proposed current mirror-II to calculate the output resistance

$$v_{d6} = i_{out} r_{o6} \text{ and } v_{g9} = -g_{m8} v_{d6} r_{o8} \quad (4.38)$$

In equations (4.37) and (4.38), v_{d6} is the drain voltage of transistor M_6 , v_{g9} is the gate voltage of transistor M_9 , $g_{m8,9}$ are the transconductances of transistors $M_{8,9}$, g_{mb9} represents the transconductance of transistor M_9 due to body effect and $r_{o6,8,9}$ are the output resistances of transistors $M_{6,8,9}$. The value of $g_{mb9} \ll 1$, so $g_{mb9} v_{d6}$ can be neglected. Now, by substituting the values of v_{d6} and v_{g9} from equation (4.38) in equation (4.37), we get

$$i_{out} + i_{out} r_{o6} \left(g_{m8} g_{m9} r_{o8} + g_{m9} + \frac{1}{r_{o9}} \right) = \frac{v_{out}}{r_{o9}} \quad (4.39)$$

Using equation (4.39), the output resistance (R_{out}) can be written as

$$R_{out} = r_{o6} + r_{o9} + r_{o6} r_{o9} g_{m9} + r_{o6} r_{o8} r_{o9} g_{m8} g_{m9} \quad (4.40)$$

4.3.2.1.3 Transfer function and bandwidth

The high-frequency small-signal equivalent model of the proposed current mirror-II to calculate the transfer function and bandwidth is shown in Figure 4.10. In the figure, the current source I_{bias} implemented using transistor M_4 is replaced by resistance R_b and the current source implemented using transistor M_7 is opened circuit. By applying KCL at nodes ' D_{1a} ', ' D_3 ' and ' S_5 ', we get

$$i_{in}(s) = g_{m1} v_{s5}(s) + v_{s2}(s) (sC_{gs2} + sC_{bs2} + g_{m2} + g_{mb2}) \quad (4.41)$$

$$v_{d3}(s) (sC_{gs5} + sC_{bs3} + g_{mb3}) = (g_{m2} + g_{mb2}) v_{s2}(s) + sC_{gs5} v_{s5}(s) \quad (4.42)$$

$$v_{d3}(s) (sC_{gs5} + g_{m5}) = v_{s5}(s) (sC_{gs1} + sC_{gs5} + sC_{bs5} + sC_{gs6} + g_{m5} + g_{mb5} + \frac{1}{R_b}) \quad (4.43)$$

where C_{gs1} states for $C_{gs1a} + C_{gs1b}$, $C_{gs1a,1b,2,5,6}$ represent gate-to-source capacitances of transistors $M_{1a,1b,2,5,6}$, $C_{bs2,3,5}$ represent body-to-source capacitances of transistors $M_{2,3,5}$, $v_{s2,5}(s)$

are the source voltages of transistors $M_{2,5}$ and $v_{d3}(s)$ is the drain voltage of transistor M_3 . As $g_{m2,5} \gg g_{mb2,5}$ and $C_{gs2,5} \gg C_{bs2,5}$, body effects of transistors M_2 and M_5 can be neglected. The output current ($i_{out}(s)$) at node 'D₆' can be written as

$$i_{out}(s) = g_{m6} v_{s5}(s) \quad (4.44)$$

where g_{m6} is the transconductance of transistors M_6 .

Assuming transistors M_1 (parallel combination of transistors M_{1a} and M_{1b}) and M_6 are perfectly matched i.e. $C_{gs1} = C_{gs6}$, $g_{m1} = g_{m6}$. Substituting the value of $v_{d3}(s)$ from equation (4.43) in equation (4.42), equation (4.42) is modified as

$$v_{s5}(s) \left(2s^2 C_{gs1} C_{gs5} + 2s^2 C_{gs1} C_{bs3} + s^2 C_{bs3} C_{gs5} + 2s C_{gs1} g_{mb3} + s C_{gs5} g_{mb3} + s C_{bs3} g_{m5} + \frac{s C_{gs5}}{R_b} + \frac{s C_{bs3}}{R_b} + \frac{g_{mb3}}{R_b} + g_{m5} g_{mb3} \right) = v_{s2}(s) (s C_{gs5} g_{m2} + g_{m2} g_{m5}) \quad (4.45)$$

Now, by substituting the value of v_{s2} from equation (4.45) in equation (4.41), equation (4.41) can be written as

$$\begin{aligned} i_{in}(s) [g_{m2} (s C_{gs5} + g_{m5}) R_b] &= v_{s5}(s) [s^3 (2 C_{gs1} C_{gs2} C_{gs5} R_b + 2 C_{gs1} C_{gs2} C_{bs3} R_b + C_{gs2} C_{bs3} C_{gs5} R_b) \\ &+ s^2 (2 C_{gs1} C_{gs2} g_{mb3} R_b + 2 C_{gs1} C_{gs5} g_{m2} R_b + 2 C_{gs1} C_{bs3} g_{m2} R_b \\ &+ C_{gs2} C_{gs5} g_{mb3} R_b + C_{gs2} C_{bs3} g_{m5} R_b \\ &+ C_{gs5} C_{bs3} g_{m2} R_b + C_{gs2} C_{gs5} + C_{gs2} C_{bs3}) \\ &+ s^1 (2 C_{gs1} g_{m2} g_{mb3} R_b + C_{gs2} g_{mb3} g_{m5} R_b + C_{gs5} g_{m2} g_{mb3} R_b \\ &+ C_{bs3} g_{m2} g_{m5} R_b + C_{gs5} g_{m1} g_{m2} R_b + C_{gs2} g_{mb3} + C_{gs5} g_{m2} + C_{bs3} g_{m2}) \\ &+ s^0 (g_{m2} g_{mb3} g_{m5} R_b + g_{m1} g_{m2} g_{m5} R_b + g_{m2} g_{mb3})] \end{aligned} \quad (4.46)$$

Using equations (4.44) and (4.46), the transfer function ($A_i(s)$) of the proposed current mirror-II is given in equation (4.47).

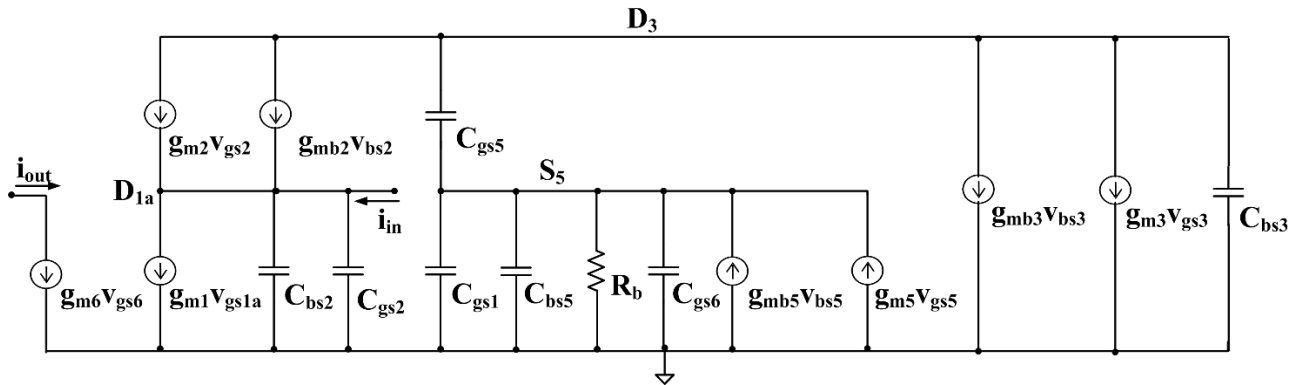


Figure 4.10 High-frequency small-signal equivalent model of the proposed current mirror-II to calculate the transfer function

$$A_i(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{g_m^2(sC_{gs} + g_m)R_b}{s^3(2C_{gs}^3R_b + 3C_{gs}^2C_{bs}R_b) + s^2(3C_{gs}^2g_{mb}R_b + 2C_{gs}^2g_mR_b + 4C_{gs}C_{bs}g_mR_b + C_{gs}C_{bs} + C_{gs}^2) + s^1(4C_{gs}g_mg_{mb}R_b + g_m^2C_{bs}R_b + g_m^2C_{gs}R_b + g_mC_{gs} + g_mC_{bs}) + s^0(g_m^2g_{mb}R_b + g_m^3R_b)} \quad (4.47)$$

In equation (4.47), it is assumed that $C_{gs1} = C_{gs2} = C_{gs3} = C_{gs5} = C_{gs}$, $g_{m1} = g_{m2} = g_{m3} = g_{m5} = g_m$ and $g_mR_b \gg 1$.

From equation (4.47), it is clear that the proposed current mirror-II has one zero and three poles, which are given as

$$\begin{aligned} \omega_{z1} &= -g_m/C_{gs}, \quad \omega_{p1} = -g_m/C_{gs}, \\ \omega_{p2,3} &= -\frac{3C_{gs}g_{mb} + C_{bs}g_m}{4C_{gs}^2 + 6C_{gs}C_{bs}} \left(1 \pm i \sqrt{\frac{4(2C_{gs}^2 + 3C_{gs}C_{bs})(g_mg_{mb} + g_m^2)}{(3C_{gs}g_{mb} + C_{bs}g_m)^2} - 1} \right) \\ \text{or } |\omega_{z1}| &= g_m/C_{gs}, \quad |\omega_{p1}| = g_m/C_{gs}, \quad |\omega_{p2,3}| = \sqrt{\frac{g_m(g_m + g_{mb})}{C_{gs}(2C_{gs} + 3C_{bs})}} \approx g_m/\sqrt{2}C_{gs} \end{aligned} \quad (4.48)$$

where ω_{z1} denotes the location of zero while ω_{p1} , ω_{p2} and ω_{p3} denote the locations of poles. Thus, substituting values of poles and zero from equation (4.48) in equation (4.27), the bandwidth (ω_o) of proposed current mirror-II is given as

$$\omega_o \approx \frac{1}{\sqrt{\frac{1}{\left(\frac{g_m}{C_{gs}}\right)^2} + \frac{2}{\left(\frac{g_m}{\sqrt{2}C_{gs}}\right)^2} - \frac{2}{\left(\frac{g_m}{C_{gs}}\right)^2}}} \approx \frac{g_m}{\sqrt{3}C_{gs}} \quad (4.49)$$

4.3.2.2 Stability analysis

The stability of the proposed current mirror-II is evaluated using open-loop gain analysis. There are two independent loops present at the input and output stages of the proposed current mirror-II. The open-loop analysis at the input stage i.e. class-AB FVF cell-II has already been performed in section 3.3.2.3 of chapter 3 which shows that the class-AB FVF cell-II is stable. The open-loop analysis of the regulated cascode structure at the output stage shows two poles at the drain of the transistor ('D₆') and the drain of the transistor ('D₈'). The pole at node 'D₆' is a non-dominant pole which is given by $w_{p6} = \frac{1}{R_6C_6}$, where R_6 is the equivalent resistance and C_6 is the equivalent capacitance at node 'D₆'. The pole at node 'D₈' is the dominant pole which is given by $w_{p8} = \frac{1}{R_8C_8}$, where R_8 is the equivalent resistance and C_8 is the equivalent capacitance at node 'D₈'. The open-loop gain (A_{ol}) at the output stage is $A_{ol} = -g_{m8}R_8$. The gain-bandwidth product (GBW) at the output stage is expressed as $GBW = A_{ol}w_{p8} = \frac{g_{m8}}{C_8}$. To maintain the

stability condition, the relationship $w_{p6} \geq 2\text{GBW}$ must be satisfied, which is maintained in the proposed current mirror-II.

4.3.3 Analysis of proposed current mirror-III

This section presents the small-signal analysis and stability analysis of the proposed current mirror-III.

4.3.3.1 Small-signal analysis of proposed current mirror-III

This section discusses the analyses of input resistance, output resistance, transfer function and bandwidth of the proposed current mirror-III using small-signal equivalent models.

4.3.3.1.1 Input resistance

To calculate the input resistance of proposed current mirror-III, the small-signal equivalent model is shown in Figure 4.11 in which an input voltage v_{in} that supplies a current i_{in} is applied at the node 'D₂'. In the model, g_{mbi} is the transconductance of transistor M_i due to the body effect, g_{mi} is the transconductance of transistor M_i and r_{oi} is the output resistance of transistors M_i , where i varies from 1 to 3.

Applying KCL at nodes 'D₁' and 'D₂', we get

$$\frac{v_{d1} - v_{in}}{r_{o1}} - (g_{m1} + g_{mb1})v_{in} = -g_{mb3}v_{d1} - \frac{v_{d1}}{r_{o3}} \quad (4.50)$$

$$i_{in} - (g_{m1} + g_{mb1})v_{in} + \frac{v_{d1} - v_{in}}{r_{o1}} = g_{m2}v_{d1} + \frac{v_{in}}{r_{o2}} \quad (4.51)$$

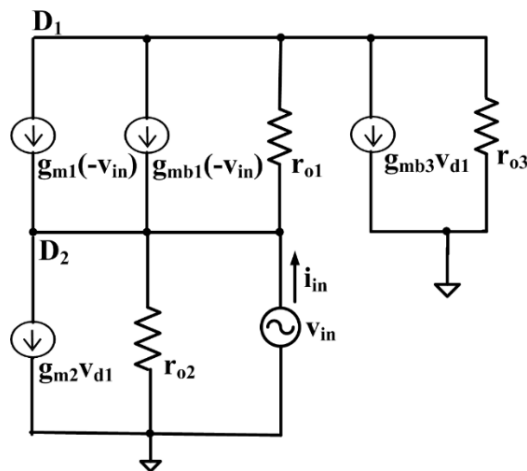


Figure 4.11 Small-signal equivalent model of the proposed current mirror-III to calculate the input resistance

Using equation (4.50) and assuming $g_m r_o \gg 1$, the voltage v_{d1} is given as

$$v_{d1} = \frac{(g_{m1} + g_{mb1})}{g_{mb3}} v_{in} \quad (4.52)$$

Substituting v_{d1} from equation (4.52) in equation (4.51) and assuming $g_m r_o \gg 1$, the input resistance (R_{in}) of the proposed current mirror-III is expressed as

$$R_{in} = \frac{g_{mb3}}{(g_{m1} + g_{mb1})(g_{m2} + g_{mb3})} \quad (4.53)$$

4.3.3.1.2 Output resistance

The small-signal equivalent model of the super cascode output stage of the proposed current mirror-III shown in Figure 4.12 is used to calculate the output resistance where output voltage v_{out} that supplies a current i_{out} is applied at node 'D₁₁'. In the model, $g_{m1a,10,11}$ represent the transconductances of transistors $M_{1a,10,11}$, $g_{mb1a,11}$ represent the transconductances of transistors $M_{1a,11}$ due to body effect and $r_{o1a,8,10,11}$ represent the output resistances of transistors $M_{1a,8,10,11}$.

The voltage at node 'D₁₀' can be written as

$$v_{d10} = -g_{m10} r_{o10} v_{d1a} \quad (4.54)$$

Applying KCL at nodes 'D₁₁' and 'D_{1a}', we get

$$i_{out} = g_{m11}(v_{d10} - v_{d8}) - g_{mb11}v_{d8} + \frac{v_{out} - v_{d8}}{r_{o11}} \quad (4.55)$$

$$g_{m1a}v_{d8} + g_{mb1a}v_{d8} = \frac{v_{d1a} - v_{d8}}{r_{o1a}} \quad (4.56)$$

The voltage at node 'D₈' can be written as

$$v_{d8} = i_{out} r_{o8} \quad (4.57)$$

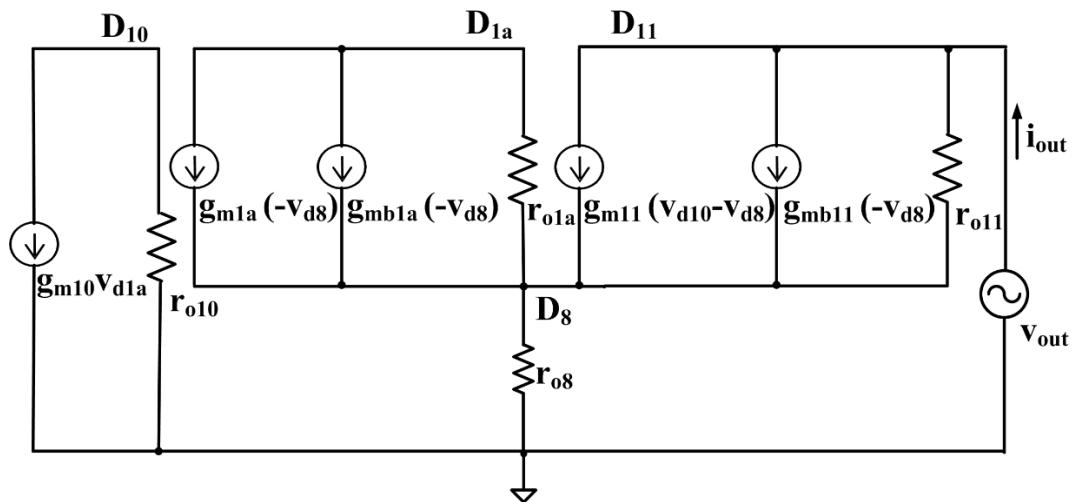


Figure 4.12 Small-signal equivalent model of the proposed current mirror-III to calculate the output resistance

Using equations (4.56) and (4.57), the voltage at node 'D_{1a}' can be written as

$$v_{d1a} = ((g_{m1a} + g_{mb1a})r_{o1a} + 1)r_{o8}i_{out} \quad (4.58)$$

Using equations (4.54), (4.55), (4.57) and (4.58), the output resistance (R_{out}) of the proposed current mirror-III is expressed as

$$\begin{aligned} R_{out} &= r_{o8} + r_{o11} + (g_{m11} + g_{mb11})r_{o8}r_{o11} + g_{m10}g_{m11}r_{o8}r_{o10}r_{o11} \\ &\quad + g_{m10}g_{m11}(g_{m1a} + g_{mb1a})r_{o1a}r_{o8}r_{o10}r_{o11} \\ &\cong g_{m10}g_{m11}(g_{m1a} + g_{mb1a})r_{o1a}r_{o8}r_{o10}r_{o11} \end{aligned} \quad (4.59)$$

4.3.3.1.3 Transfer function and bandwidth

The high-frequency small-signal equivalent model shown in Figure 4.13 is used to calculate the transfer function and bandwidth of the proposed current mirror-III. The current source implemented by transistor M₉ is open-circuited in the model. In the model, C_{gs2} & C_{gs8} are the parasitic capacitances at node 'G₂', C_{gs1} & C_{bs1} are the parasitic capacitances at node 'D₂', C_{gs1a} & C_{bs1a} are the parasitic capacitances at node 'D₈', and C_{bs3} is the parasitic capacitance at node 'D₁'.

Applying KCL at nodes 'D₁', 'D₂' and 'G₂', we obtain

$$v_{d2}(s)(g_{m1} + g_{mb1}) = v_{d1}(s)(sC_{eqv} + sC_{bs3} + g_{mb3})v_{in}(s) \quad (4.60)$$

$$i_{in}(s) = v_{d2}(s)(g_{m1} + g_{mb1}) + g_{m2}v_{g2}(s) + v_{d2}(s)(sC_{gs1} + sC_{bs1}) \quad (4.61)$$

$$v_{g2}(s) = v_{d1}(s)\alpha \quad (4.62)$$

where $C_{eqv} = \frac{2(C_{gs8} + C_{gs2})C_{bat}}{C_{bat} + C_{gs8} + C_{gs2}}$ and $\alpha = \frac{C_{bat}}{C_{bat} + C_{gs8} + C_{gs2}}$.

In equations (4.60), (4.61) and (4.62), it is assumed that $g_m r_o \gg 1$.

Using equations (4.60), (4.61) and (4.62), we get

$$i_{in}(s) = \frac{\left(s^2 C_{gs1} C_Y + s(g_{m1} C_Y + C_{gs1} g_{mb3}) + \right) v_{g2}(s)}{g_{m1} g_{m2} \alpha + g_{m1} g_{mb3}} \quad (4.63)$$

where $C_Y = C_{eqv} + C_{bs3}$.

In equation (4.63), it is assumed that $g_{m1} \gg g_{mb1}$ and $C_{gs1} \gg C_{bs1}$.

Applying KCL at nodes 'D_{1a}' and 'D₈', we get

$$i_{out}(s) = -v_{d8}(s)(g_{m1a} + g_{mb1a}) \quad (4.64)$$

$$v_{d8}(s)(g_{m1a} + g_{mb1a}) + g_{m8}v_{g2}(s) + v_{d8}(s)(sC_{gs1a} + sC_{bs1a}) = 0 \quad (4.65)$$

In equations (4.64) and (4.65), it is assumed that $g_m r_o \gg 1$.

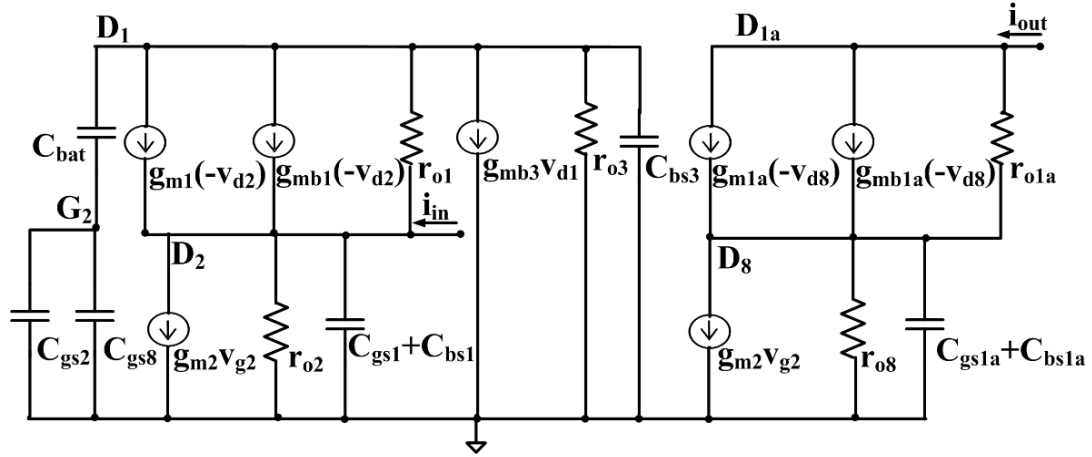


Figure 4.13 High-frequency small-signal equivalent model of the proposed current mirror-III to calculate the transfer function

Using equations (4.64) and (4.65), we get

$$i_{out}(s) = \frac{g_{m1a}g_{m8}V_{g2}(s)}{(g_{m1a} + sC_{gs1a})} \quad (4.66)$$

In equation (4.66), it is assumed that $g_{m1a} \gg g_{mmb1a}$ and $C_{gs1a} \gg C_{bs1a}$.

Using equations (4.63) and (4.66), the transfer function of the proposed current mirror-III can be written as

$$A_i(s) = \frac{i_{out}(s)}{i_{in}(s)} = \frac{g_{m1}g_{m1a}g_{m8}\alpha}{(g_{m1a} + sC_{gs1a})(s^2C_{gs1}C_Y + s(g_{m1}C_Y + C_{gs1}g_{mb3}) + g_{m1}g_{m2}\alpha)} \quad (4.67)$$

In equation (4.67), it is assumed that $g_{m2}\alpha \gg g_{mb3}$ and it shows that the proposed current mirror-III has three poles given as

$$w_{p1} = -\frac{g_{m1a}}{C_{gs1a}} \quad (4.68)$$

$$w_{p2,3} = -\frac{g_{m1}C_Y + C_{gs1}g_{mb3}}{2C_{gs1}C_Y} \left(1 \pm i \sqrt{\frac{4C_{gs1}C_Yg_{m1}g_{m2}\alpha}{(g_{m1}C_Y + C_{gs1}g_{mb3})^2 - 1}} \right)$$

If $g_{m1}C_Y \gg C_{gs1}g_{mb3}$, then the location of poles ($w_{p1,2,3}$) can be written as

$$|w_{p1}| = \frac{g_{m1a}}{C_{gs1a}}, |w_{p2,3}| = \sqrt{\frac{g_{m1}g_{m2}\alpha}{C_{gs1}C_Y}} \quad (4.69)$$

Substituting the values of w_{p1} , w_{p2} and w_{p3} from equation (4.69) in equation (4.27), the bandwidth (w_o) is given as

$$w_o = \frac{1}{\sqrt{\left(\frac{C_{gs1a}}{g_{m1a}}\right)^2 + \frac{2C_{gs1}C_Y}{g_{m1}g_{m2}\alpha}}} \quad (4.70)$$

4.3.3.2 Stability analysis

The stability of the proposed current mirror-III is evaluated using open-loop gain analysis. There are two independent loops present at the input and output stages of the proposed current mirror-III. The open-loop analysis at the input stage i.e. class-AB FVF cell-III is done in section 3.3.3.3 of chapter 3 which shows that the class-AB FVF cell-III is stable. The open-loop analysis of the super cascode structure at the output stage is done by using the method suggested in [58]. The open-loop analysis of the output stage shows three poles at nodes 'D_{1a}', 'D₈', and 'D₁₀'. The pole at node 'D₈' is a non-dominant pole which is given by $w_{p8} = \frac{g_{m1a} + g_{m11}}{C_8}$, where C_8 is the equivalent capacitance at node 'D₈'. Since the resistances at the nodes 'D_{1a}' and 'D₁₀' are large valued, the dominant poles exist at both the nodes and these are given as $w_{p1a} = \frac{1}{R_{1a}C_{1a}}$ and $w_{p10} = \frac{1}{R_{10}C_{10}}$. The open-loop gain at the output stage is $A_{ol} = -g_{m1a}r_{o1a}g_{m10}r_{o10}$.

But to maintain stability with such high loop gain, there must be one dominant pole and two non-dominant poles. To make the pole at node 'D_{1a}' as dominant, there are three different techniques suggested by A. Torralba *et al.* [58] as

- The first is to maintain the equivalent resistance at node 'D_{1a}' (R_{1a}) greater than the equivalent resistance at node 'D₁₀' (R_{10}), so that pole at node 'D_{1a}' becomes dominant.
- The second is to use a miller compensating capacitor between nodes 'D_{1a}' and 'D₁₀'.
- The third is to use both the first and second techniques together.

In the proposed current mirror-III, the first technique has been used to convert two dominant poles into one dominant pole and one non-dominant pole by properly selecting transistor sizes and bias currents. By choosing the non-minimum channel length of transistors M_{1a} & M_9 , and the value of bias current I_{bias} relatively lower than the I_{b1} , the equivalent resistance at node 'D_{1a}' becomes high. Also, by keeping the minimum channel length of transistors M_{10} & M_{12} (used to implement current source I_{b1}) and selecting the value of I_{b1} relatively high, the equivalent resistance at node 'D₁₀' becomes low. Hence, the equivalent resistance at node 'D_{1a}' (R_{1a}) becomes greater than the equivalent resistance at node 'D₁₀' (R_{10}). Finally, the proposed current mirror-III has one dominant pole and two non-dominant poles. So, in this way, the stability of the output stage has been maintained.

4.3.4 Analysis of proposed current mirror-IV

This section presents the small-signal analysis and stability analysis of the proposed current mirror-IV.

4.3.4.1 Small-signal analysis of proposed current mirror-IV

The analyses of input resistance, output resistance, transfer function and bandwidth of the proposed current mirror-IV using small-signal equivalent models are explained in this section.

4.3.4.1.1 Input resistance

The small-signal equivalent model of the proposed current mirror-IV to calculate the input resistance is shown in Figure 4.14. In the model, g_{mi} is the transconductance of transistor M_i where $i=1,2,4,5,6,7$, g_{mbi} is the transconductance of transistor M_i due to the body effect where $i=1,4$ and r_{oi} is the output resistance of transistors M_i where $i=1,2,3,4,5$.

By applying KCL at node 'D₁', we get

$$v_{in} \left(g_{m1} + g_{mb1} + \frac{1}{r_{o1}} \right) = v_{g5} \left(\frac{1}{r_{o1}} + \frac{1}{R_b + r_{o3}} \right) \quad (4.71)$$

Assuming $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}$, $R_b \ll r_{o3}$ and $g_m r_o \gg 1$, equation (4.71) is simplified as

$$v_{g5} = (g_{m1} + g_{mb1}) \frac{r_{o1}}{2} v_{in} \quad (4.72)$$

Applying KCL at node 'D₆', we get

$$v_{g2} = \frac{g_{m4} v_{g4}}{g_{m4} + g_{mb4} + (r_{o4} || 1/g_{m6})^{-1}} \quad (4.73)$$

Assuming $g_m r_o \gg 1$ in equation (4.73), the gate voltage at transistor M_2 (v_{g2}) is given as

$$v_{g2} = \frac{g_{m4} v_{g4}}{g_{m4} + g_{mb4} + g_{m6}} \quad (4.74)$$

The gate voltage at transistor M_4 (v_{g4}) can be written as

$$v_{g4} = \frac{r_{o3} v_{g5}}{r_{o3} + R_b} \quad (4.75)$$

Substituting the value of v_{g4} from equation (4.75) in equation (4.74), voltage v_{g2} is given as

$$v_{g2} = \frac{g_{m4} r_{o3} v_{g5}}{(g_{m4} + g_{mb4} + g_{m6})(r_{o3} + R_b)} \quad (4.76)$$

Applying KCL at node 'D₇' and assuming $g_m r_o \gg 1$, v_{g7} can be written as

$$v_{g7} = \frac{v_{in} g_{m7} - v_{g5} g_{m5}}{g_{m7}} \quad (4.77)$$

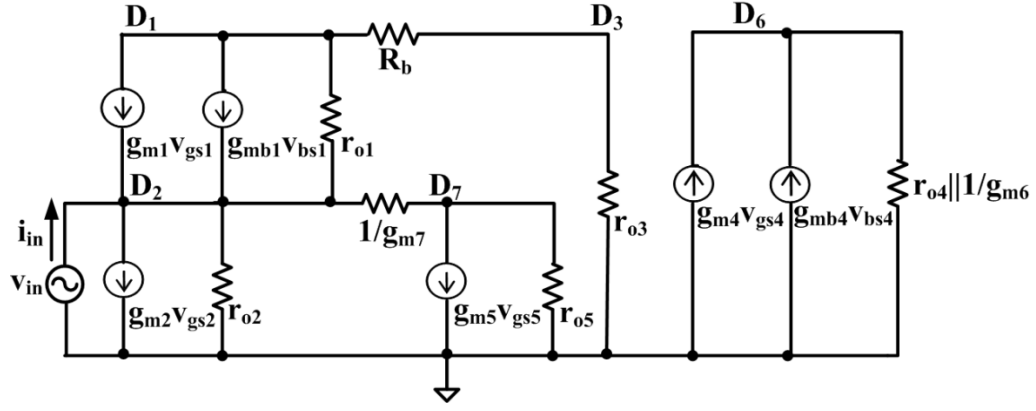


Figure 4.14 Small-signal equivalent model of the proposed current mirror-IV to calculate the input resistance

Applying KCL at node 'D₂' and assuming $g_m r_o \gg 1$, we get

$$i_{in} + g_{m7}v_{g7} = v_{in}(g_{m1} + g_{mb1} + g_{m7}) + g_{m2}v_{g2} \quad (4.78)$$

Using equations (4.72), (4.76), (4.77) and (4.78), the expression for input resistance (R_{in}) is given as

$$R_{in} = \frac{2(g_{m4} + g_{m6})}{(g_{m1} + g_{mb1})(g_{m2}g_{m4}r_{o1} + g_{m5}(g_{m4} + g_{m6})r_{o1} + 2(g_{m4} + g_{m6}))} \quad (4.79)$$

In equation (4.79), it is assumed that $r_{o1} \cong r_{o3}$, $R_b \ll r_{o1}$ and $g_{m4} \cong g_{m4} + g_{mb4}$.

4.3.4.1.2 Output resistance

The small-signal equivalent model of the proposed current mirror-IV to calculate the output resistance is shown in Figure 4.15. The output voltage v_{out} supplying a current i_{out} is applied at node 'D₁₅'. In the model, $g_{m12,14,15}$ represent the transconductances of transistors $M_{12,14,15}$, $g_{mb12,15}$ represent the transconductances of transistors $M_{12,15}$ due to body effect and $r_{o12,13,14,15}$ are the output resistances of transistors $M_{12,13,14,15}$.

The voltages at nodes 'D₁₃' and 'D₁₄' can be written as

$$v_{d13} = i_{out}r_{o13} \quad (4.80)$$

$$v_{d14} = -g_{m14}r_{o14}v_{d12} \quad (4.81)$$

Applying KCL at nodes 'D₁₂', we get

$$\frac{v_{d12}}{r_{o12}} = \left(g_{m12} + g_{mb12} + \frac{1}{r_{o12}} \right) v_{d13} \quad (4.82)$$

Applying KCL at node 'D₁₅', we get

$$i_{out} = g_{m15}(v_{d14} - v_{d13}) - g_{mb15}v_{d13} + \frac{v_{out} - v_{d13}}{r_{o15}} \quad (4.83)$$

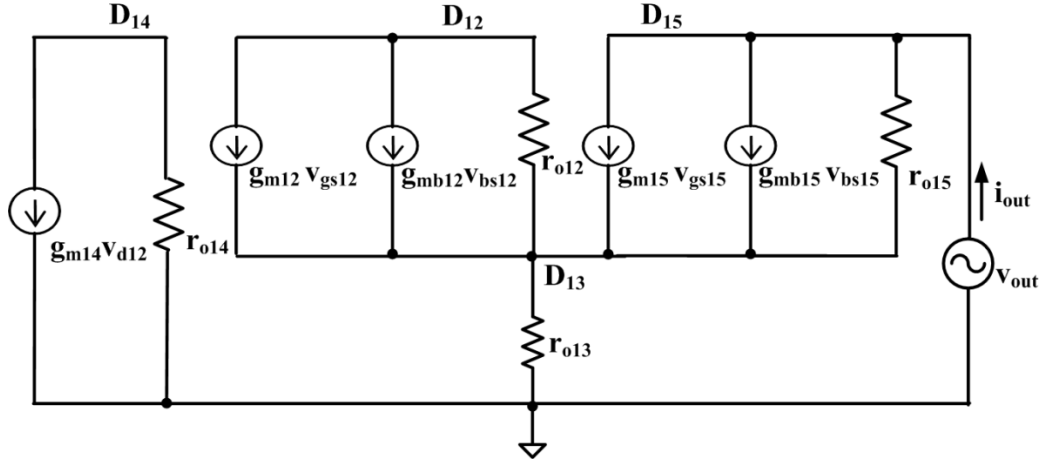


Figure 4.15 Small-signal equivalent model of the proposed current mirror-IV to calculate the output resistance

Using equations (4.80), (4.81), (4.82) and (4.83), the output resistance (R_{out}) of the proposed current mirror-IV is expressed as

$$R_{out} = r_{o13} + r_{o15} + r_{o13}r_{o15}(g_{m15} + g_{mb15}) + r_{o13}r_{o14}r_{o15}g_{m14}g_{m15} + r_{o12}r_{o13}r_{o14}r_{o15}g_{m14}g_{m15}(g_{m12} + g_{mb12}) \quad (4.84)$$

4.3.4.1.3 Transfer function and bandwidth

The high-frequency small-signal equivalent model of the proposed current mirror-IV used to calculate the transfer function and bandwidth is shown in Figure 4.16. The current source implemented by transistor M_{11} is open-circuited in the model. In the model, $C_{gs4,5,12}$ represent gate-to-source capacitances of transistors $M_{4,5,12}$, C_{bs12} represent body-to-source capacitance of transistors M_{12} , C_A consists of parasitic capacitances between nodes 'D₂' and 'D₇', C_B consists of parasitic capacitances at node 'D₈', C_Y consists of parasitic capacitances at node 'D₆' and C_Z consists of parasitic capacitances at node 'D₂'. It is assumed that $g_m r_o \gg 1$, $r_{o1} \approx r_{o3}$, $R_b \ll r_{o1}$ and $R_b \ll r_{o3}$. At the input stage, by applying KCL at nodes 'D₁', 'D₃' and 'D₆', we get

$$(g_{m1} + g_{mb1})v_{d2}(s) = \left(\frac{1}{R_b} + sC_{gs5}\right)v_{d1}(s) - \frac{v_{d3}(s)}{R_b} \quad (4.85)$$

$$\left(\frac{1}{R_b} + sC_{gs4}\right)v_{d3}(s) = sC_{gs4}v_{d6}(s) + \frac{v_{d1}(s)}{R_b} \quad (4.86)$$

$$v_{d3}(s) = \frac{(g_{m4} + g_{m6} + sC_D)}{g_{m4} + sC_{gs4}}v_{d6}(s) \quad (4.87)$$

where $C_D = C_Y + C_{gs4}$ and $C_Y = C_{gs2} + C_{gs6} + C_{gs13} + C_{bs4}$.

Using equations (4.86) and (4.87), the voltage $v_{d1}(s)$ is given in equation (4.88).

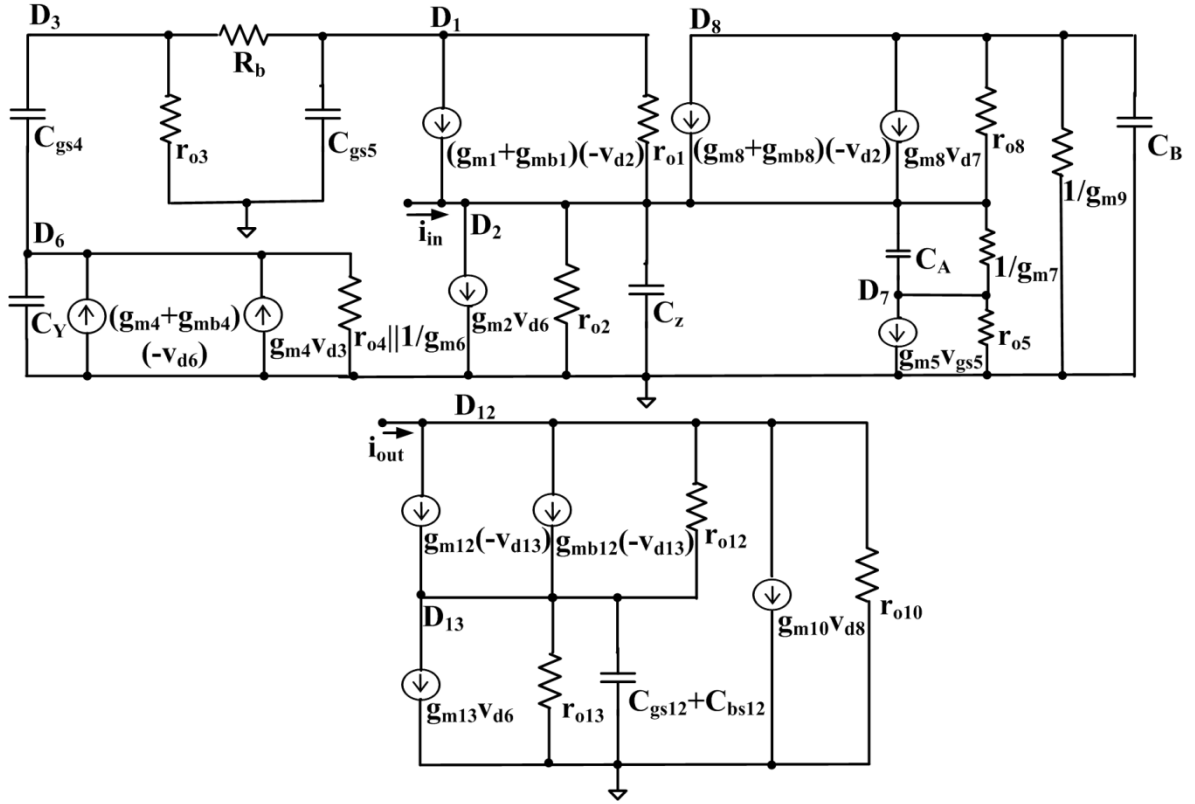


Figure 4.16 High-frequency small-signal equivalent model of the proposed current mirror-IV to calculate the transfer function

$$v_{d1}(s) = \frac{sC_{gs4}(g_{m6} + sC_Y)R_b + g_{m4} + g_{m6} + sC_D}{g_{m4} + sC_{gs4}} v_{d6}(s) \quad (4.88)$$

Using equations (4.85), (4.87) and (4.88), the voltage $v_{d2}(s)$ can be written as

$$v_{d2}(s) = \frac{sC_{gs4}(g_{m6} + sC_Y)R_b + sC_{gs5}R_b(sC_{gs4}(g_{m6} + sC_Y)R_b + g_{m4} + g_{m6} + sC_D)v_{d6}(s)}{g_{m4} + sC_{gs4}} \quad (4.89)$$

Applying KCL at nodes 'D7', 'D8' and 'D2', we get

$$(g_{m7} + sC_A)v_{d2}(s) = g_{m5}v_{d1}(s) + (g_{m7} + sC_A)v_{d7}(s) \quad (4.90)$$

$$(g_{m8} + g_{mb8})v_{d2}(s) = (g_{m9} + sC_B)v_{d8}(s) + g_{m8}v_{d7}(s) \quad (4.91)$$

$$i_{in}(s) - (g_{m1} + g_{mb1} + g_{m8} + g_{mb8} + g_{m7} + sC_Z + sC_A)v_{d2}(s) + (g_{m7} + g_{m8} + sC_A)v_{d7}(s) = g_{m2}v_{d6}(s) \quad (4.92)$$

where $C_A = C_{gs7} + C_{gs8}$, $C_B = C_{gs9} + C_{gs10}$ and $C_Z = C_{gs1} + C_{bs1} + C_{bs7} + C_{bs8}$.

Assuming $g_{m7} = g_{m8}$, $g_{m1} \gg g_{mb1}$ and $g_{m8} \gg g_{mb8}$, equation (4.92) is modified as

$$i_{in}(s) = g_{m2}v_{d6}(s) + (g_{m1} + 2g_{m7} + sC_Z + sC_A)v_{d2}(s) - (2g_{m7} + sC_A)v_{d7}(s) \quad (4.93)$$

Using equations (4.88), (4.89), (4.90) and (4.93) the input current ($i_{in}(s)$) can be written as

$$i_{in}(s) = \frac{\left(g_{m2}(g_{m4} + sC_{gs4})(g_{m7} + sC_A) + g_{m5}sC_{gs4}R_b(2g_{m7} + sC_A)(g_{m6} + sC_Y) + \right) v_{d6}(s)}{g_{m5}(2g_{m7} + sC_A)(g_{m4} + g_{m6} + sC_D)} \quad (4.94)$$

$$= \frac{(g_{m4} + sC_{gs4})(g_{m7} + sC_A)}{(g_{m4} + sC_{gs4})(g_{m7} + sC_A)}$$

In equation (4.94), it is assumed that $C_A \gg C_Z$ and $2g_{m7} \gg g_{m1}$.

At the output stage, applying KCL at nodes 'D₁₂' and 'D₁₃' we get

$$i_{in}(s) = -g_{m12}v_{d13}(s) + g_{m10}v_{d8}(s) \quad (4.95)$$

$$v_{d13}(s) = -\frac{g_{m13}v_{d6}(s)}{(g_{m12} + sC_{gs12})} \quad (4.96)$$

Using equations (4.90) and (4.91), we get

$$v_{d8}(s) = \frac{g_{m5}g_{m8}v_{d1}(s)}{(g_{m7} + sC_A)(g_{m9} + sC_B)} \quad (4.97)$$

Using equations (4.88), (4.95), (4.96) and (4.97), the output current ($i_{out}(s)$) can be written as

$$i_{out}(s) = \frac{\left(g_{m12}g_{m13}(g_{m4} + sC_{gs4})(g_{m7} + sC_A)(g_{m9} + sC_B) + g_{m5}g_{m8}g_{m10} \right) v_{d6}(s)}{(g_{m12} + sC_{gs12})(sC_{gs4}(g_{m6} + sC_Y)R_b + g_{m4} + g_{m6} + sC_D)} \quad (4.98)$$

$$= \frac{(g_{m4} + sC_{gs4})(g_{m7} + sC_A)(g_{m9} + sC_B)(g_{m12} + sC_{gs12})}{(g_{m4} + sC_{gs4})(g_{m7} + sC_A)(g_{m9} + sC_B)(g_{m12} + sC_{gs12})}$$

Using equations (4.94) and (4.98), the transfer function ($A_i(s)$) is given as

$$A_i(s) = \frac{i_{out}(s)}{i_{in}(s)} \quad (4.99)$$

$$= \frac{g_{m4}g_{m12}g_{m13}(g_{m7} + sC_A)(g_{m9} + sC_B)(1 + sC_{gs4}R_b) + g_{m8}g_{m10}g_{m13}}{(g_{m12} + sC_{gs12})(g_{m6} + sC_Y)(1 + sC_{gs4}R_b)}$$

$$= \frac{g_{m4}g_{m12}g_{m13}(g_{m7} + sC_A)(g_{m9} + sC_B)(1 + sC_{gs4}R_b) + g_{m8}g_{m10}g_{m13}}{g_{m2}(2g_{m7} + sC_A)(g_{m6} + sC_Y)(1 + sC_{gs4}R_b)(g_{m9} + sC_B)(g_{m12} + sC_{gs12})}$$

To obtain equation (4.99), it is assumed that $g_{m2} = g_{m5} = g_{m13}$, $g_{m6} \gg g_{m4}$, $g_{m4} = 1/R_b$ and $C_Y \gg C_{gs4}$. Now, assuming $g_{m7} = g_{m8} = g_{m12}$, $g_{m10} \gg g_{m4}$, $g_{m6} \gg g_{m9}$, $C_A = C_{gs12}$ and $C_Y \gg C_B$, the $A_i(s)$ is modified as

$$A_i(s) = \frac{g_{m8}g_{m10}g_{m13}(g_{m7} + sC_A)}{g_{m2}(2g_{m7} + sC_A)(g_{m9} + sC_B)(g_{m12} + sC_{gs12})} \quad (4.100)$$

Equation (4.100) shows that the proposed current mirror-IV has one zero and three poles which are given as

$$w_{z1} = -\frac{g_{m7}}{C_A}, w_{p1} = -\frac{2g_{m7}}{C_A}, w_{p2} = -\frac{g_{m9}}{C_B} \text{ and } w_{p3} = -\frac{g_{m12}}{C_{gs12}} \quad (4.101)$$

The location of zero (w_{z1}) and poles ($w_{p1,2,3}$) can be expressed as

$$|w_{z1}| = \frac{g_{m7}}{C_A}, |w_{p1}| = \frac{2g_{m7}}{C_A}, |w_{p2}| = \frac{g_{m9}}{C_B} \text{ and } |w_{p3}| = \frac{g_{m12}}{C_{gs12}} \quad (4.102)$$

Substituting the values of w_{z1} , w_{p1} , w_{p2} and w_{p3} from equation (4.102) in equation (4.27), the bandwidth (w_o) is given as

$$w_o = \frac{1}{\sqrt{\left(\frac{C_B}{g_{m9}}\right)^2 + \left(\frac{C_{gs12}}{g_{m12}}\right)^2 - \frac{7}{4}\left(\frac{C_A}{g_{m7}}\right)^2}} \quad (4.103)$$

By assuming $g_{m7} = g_{m12}$, $g_{m9} = 2g_{m12}$, $C_A = C_{gs12}$ and $C_B = 2C_{gs12}$ in equation (4.103), the w_o is given as

$$w_o = \frac{2g_{m12}}{C_{gs12}} \quad (4.104)$$

4.3.4.2 Stability analysis

The stability of the proposed current mirror-IV is evaluated using the open-loop gain analysis. There are two independent loops present at the input and output stages of the proposed current mirror-IV. The open-loop analysis at the input stage i.e. class-AB FVF cell-IV is done in section 3.3.4.3 of chapter 3 which shows that the class-AB FVF cell-III is stable. The open-loop analysis of the super cascode structure at the output stage shows three poles at nodes 'D₁₂', 'D₁₃', and 'D₁₄'. The pole at node 'D₁₃' is a non-dominant pole which is given by $w_{p13} = \frac{g_{m12} + g_{m15}}{C_{13}}$, where C_{13} is the equivalent capacitance at node 'D₁₃'. But, the poles at both the nodes 'D₁₂' and 'D₁₄' are dominant poles which are given as $w_{p12} = \frac{1}{R_{12}C_{12}}$ and $w_{p14} = \frac{1}{R_{14}C_{14}}$. The open-loop gain (A_{ol}) at the output stage is $A_{ol} = -g_{m12}r_{o12}g_{m14}r_{o14}$. To maintain stability with such high loop gain, there must be one dominant pole and two non-dominant poles. So, the pole at node 'D₁₂' should be maintained as dominant and the pole at node 'D₁₄' should be maintained as non-dominant by properly selecting transistor sizes and bias currents. The channel lengths of transistors M₁₁ & M₁₂ are kept at non-minimum value and the channel lengths of transistors M₁₄ & M₁₆ are kept at minimum value. Also, the bias current I_b is kept lower than the current I_{b1} . Then, the resistance at node 'D₁₂' becomes greater than the resistance at node 'D₁₄'. Further, the compensation capacitor C_p is connected at node 'D₁₂'. So, the resistance and capacitance at node 'D₁₂' become greater than the resistance and capacitance at node 'D₁₄'. In this way, the pole at node 'D₁₂' becomes dominant, the pole at node 'D₁₄' becomes non-dominant and stability of the output stage is maintained.

4.4 Simulation results of proposed current mirrors

The post-layout simulation results of the proposed current mirrors have been presented in this section. The proposed current mirrors are designed using BSIM3V3 180 nm CMOS technology and simulated using spectre in the Cadence Virtuoso Analog Design Environment. The physical layouts of the proposed current mirrors are designed using Cadence Virtuoso Layout XL editor in 180 nm CMOS technology. The two figures of merit FOM₁ [139] and FOM₂ [120] are used to fairly compare the performance of the proposed current mirrors with various structures of the current mirrors available in the literature. These figures of merit are defined as

$$\text{FOM}_1 = \frac{\text{Bandwidth}}{\text{Input resistance} * \text{Error} (\%)} (\text{MHz ohm}^{-1}) \quad (4.105)$$

$$\text{FOM}_2 = \frac{\text{Power} * V'_{\text{in,min}}}{I_{\text{out}} * R_{\text{out}} * \text{Bandwidth} * V_{\text{Compliance}}} (\text{Atto AHZ}^{-1}) \quad (4.106)$$

The first figure of merit (FOM₁) depends upon -3dB bandwidth, input resistance, and error (%) of the current mirror. The higher value of FOM₁ confirms the better performance of the current mirror. From the relation given in equation (4.106), it can be seen that FOM₂ uses total power, minimum input voltage required ($V'_{\text{in,min}}$), output current (I_{out}), output resistance (R_{out}), -3 dB bandwidth, and output voltage compliance ($V_{\text{Compliance}}$) of the circuit. While comparing the various current mirror structures, the minimum input voltage and output voltage compliance ($V'_{\text{in,min}}$ and $V_{\text{Compliance}}$) are calculated with respect to the supply voltage of the circuit to eliminate the role of the power supply as $V'_{\text{in,min}} = V_{\text{in,min}}/V_{\text{DD}}$ and $V_{\text{Compliance}} = (V_{\text{DD}} - V_{\text{out,min}})/V_{\text{DD}}$, where $V_{\text{out,min}}$ is the minimum output voltage. The smaller value of FOM₂ confirms the better performance of the current mirror.

4.4.1 Simulation results of proposed current mirror-I

The proposed current mirror-I is biased with a current (I_b) of 8 μA . The supply voltage (V_{DD}) is chosen as 1.2 V. The values of V_n and R_L used in proposed current mirror-I are 0.8 V and 4 k Ω , respectively. The aspect ratios (W/L) of the transistors used to design the proposed current mirror-I are given in Table 4.1.

Figure 4.17 shows the physical layout of the proposed current mirror-I which occupies an area of 26.605 $\mu\text{m} \times 31.07 \mu\text{m}$ without including bond pads. The current source I_b has been implemented using NMOS transistor M_{12} in the layout.

Table 4.1 Aspect ratios of the transistors used to design the proposed current mirror-I

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M ₁ , M ₂	5/0.54
M ₃ , M ₉	50/0.36
M ₄ , M ₁₁	6.84/0.54
M ₅	3.42/0.54
M ₆	8/0.54
M ₇ , M ₈	10/0.54
M ₁₀	50/0.54
M ₁₂	3/0.54

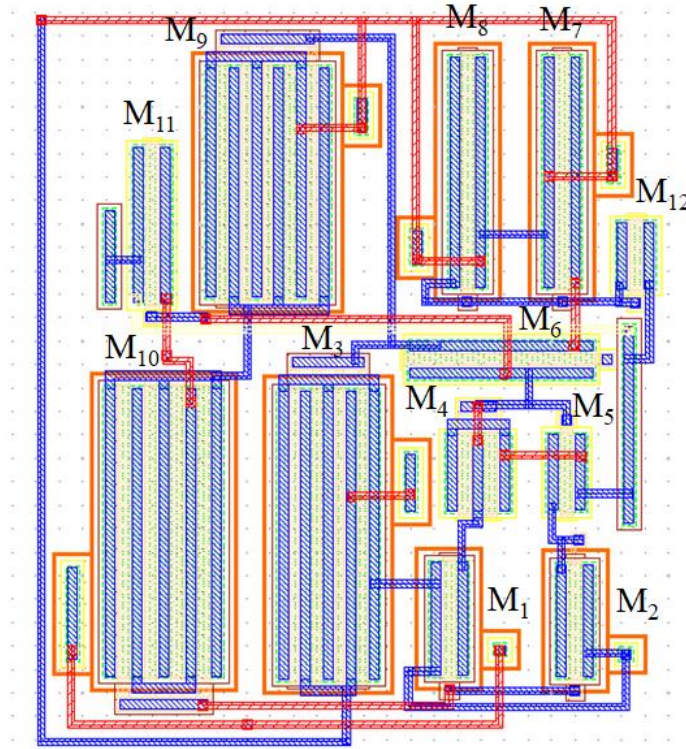


Figure 4.17 Physical layout of the proposed current mirror-I

The variation of the output current versus input current which varies from 0 to 120 μA is shown in Figure 4.18. From the figure, it is observed that the output current follows the input current linearly. Figure 4.19 illustrates the percentage error ($((I_{\text{out}} - I_{\text{in}})/I_{\text{in}}) \times 100$) plot of the proposed current mirror-I and the average error is calculated as 1.46 %.

Figure 4.20 shows the variation of input voltage versus input current of proposed current mirror-I. It is observed that the input voltage changes from 0.817 V to 0.71 V for the input current varying from 0 to 120 μA . The variations of output current versus the output voltage for different values of input current varying from 20 μA to 120 μA with the increment of 20 μA are shown in Figure 4.21. The minimum required output voltage is obtained as 0.10 V.

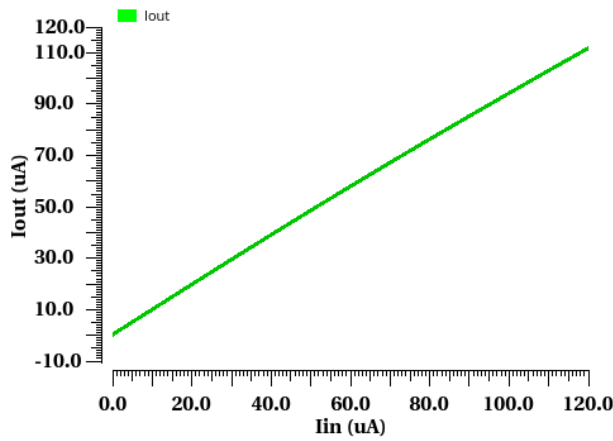


Figure 4.18 DC characteristics of the proposed current mirror-I

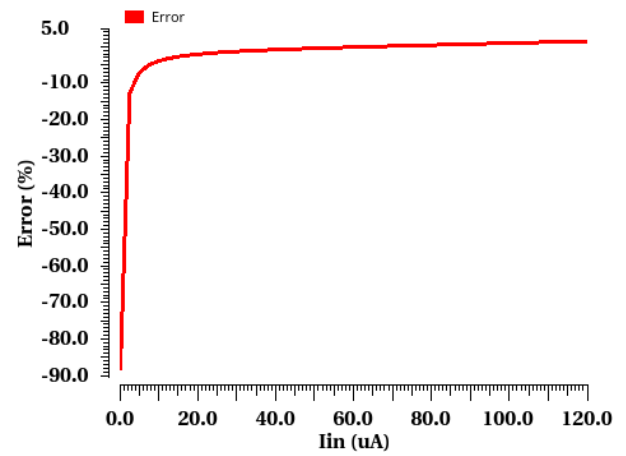


Figure 4.19 Percentage error plot of the proposed current mirror-I

The gain versus frequency plot of the proposed current mirror-I is depicted in Figure 4.22. To obtain the gain versus frequency response, an alternating current source of 1 μA AC magnitude with an offset current of 50 μA (at a frequency of 1 MHz) is applied at the input of the proposed current mirror-I. From the plot, gain and bandwidth are calculated as 0.94 and 134 MHz, respectively. The plots of input resistance versus frequency and output resistance versus frequency of the proposed current mirror-I are shown in Figure 4.23 and Figure 4.24, respectively. The proposed current mirror-I offers low input resistance of 340 Ω when the quiescent input current is 10 μA and high output resistance of 2.6 M Ω .

The transient response of the proposed current mirror-I for a step signal varying from 0 to 120 μA at 1 MHz frequency is shown in Figure 4.25. From the plot, it is observed that the settling time (2 % of the final value) is 20.4 ns at the rising edge of output current.

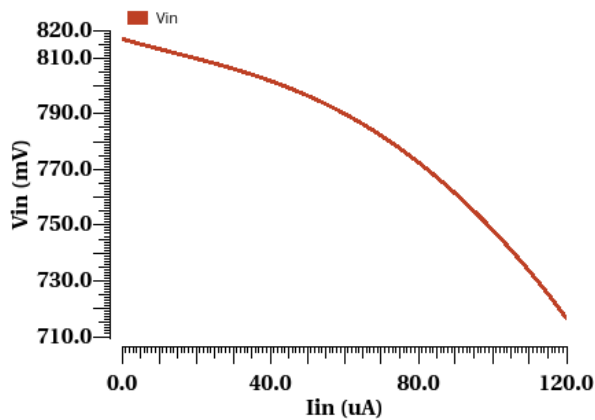


Figure 4.20 Variation of input voltage versus input current of the proposed current mirror-I

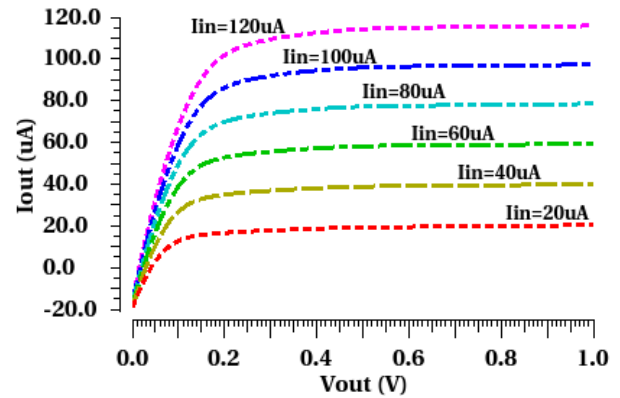


Figure 4.21 Variation of output current versus output voltage of the proposed current mirror-I

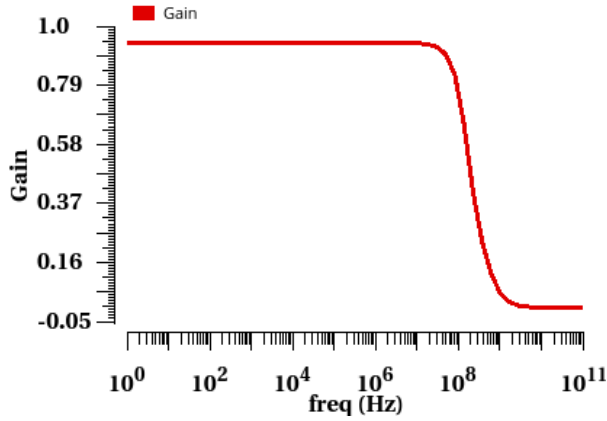


Figure 4.22 Gain versus frequency plot of the proposed current mirror-I

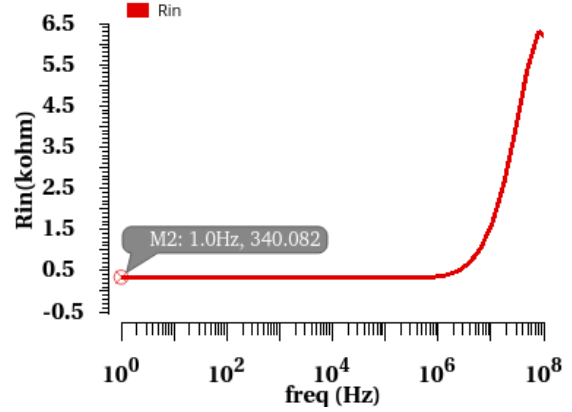


Figure 4.23 Input resistance versus frequency plot of the proposed current mirror-I

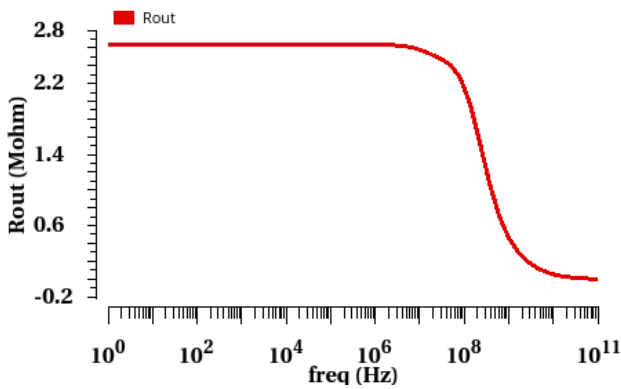


Figure 4.24 Output resistance versus frequency plot of the proposed current mirror-I

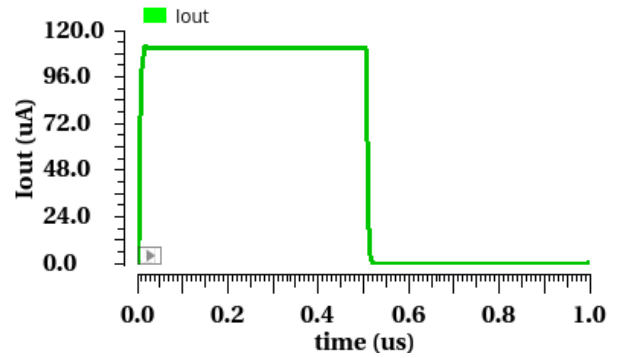


Figure 4.25 Transient response of the proposed current mirror-I

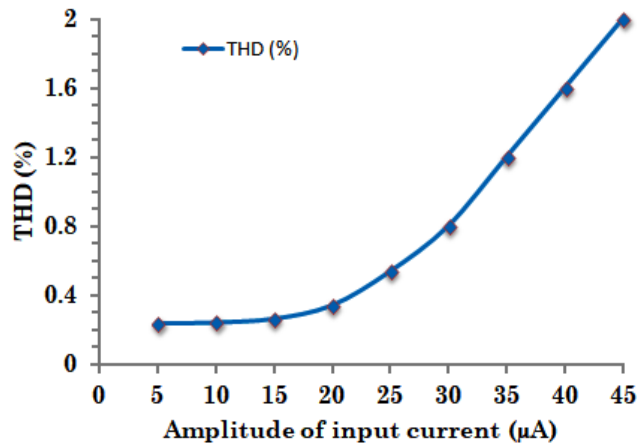


Figure 4.26 THD (%) of the proposed current mirror-I

The plot of total harmonic distortion (THD) versus different amplitudes of the input current is shown in Figure 4.26. A sinusoidal input current with a quiescent current of 50 μA at 1 MHz frequency is applied for the calculation of THD of the proposed current mirror-I. From the plot, the THD is observed as less than 2 % for different amplitudes of the input current.

The proposed current mirror-I has been compared with the existing current mirrors available in the literature in Table 4.2. The two figures of merit (FOM_1) and (FOM_2) are used to compare the performance of the proposed current mirror-I with various existing structures of the current mirrors. From the table, it is observed that the proposed current mirror has high output compliance voltage and consumes less power. Also, the proposed current mirror-I has a larger FOM_1 as compared to the existing current mirror [61]. The parameters required to calculate FOM_2 are not reported in the structures [61, 121, 129, 131, 134] so the FOM_2 of these structures has not been calculated.

Table 4.2 Comparison of the proposed current mirror-I with existing current mirrors available in the literature

References→ Parameters↓	[61]	[121]	[129]	[131]	[134]	Proposed current mirror-I
Supply Voltage (V)	1.5	1.8	1.8	± 0.5	1	1.2
Technology (μm)	0.18	0.18	0.18	0.25	0.18	0.18
Current Range (μA)	-----	-----	0 to 100	0 to 280	0.01 to 100	0 to 120
% Error	1.4	-----	-----	-----	6 to 11	1.46
Minimum Input voltage (V)	-----	-----	-----	0.25	-----	0.71-0.817
Minimum Output voltage (V)	-----	0.135	0.4	----	0.11	0.10
Output voltage compliance(V)	-----	0.925	0.78	-----	0.89	0.92
Input Resistance (Ω)	3 k	-----	-----	2.7 k	-----	340
Output Resistance (Ω)	-----	1 M	-----	578 k	1.8 M	2.6 M
Bandwidth (MHz)	212	-----	-----	132	-----	134
Power (μW)	218	-----	413	----	-----	81.39
FOM_1 (MHz ohm^{-1})	0.050	-----	-----	-----	-----	0.27
FOM_2 (Atto AHZ^{-1})	-----	-----	-----	-----	-----	1240

4.4.2 Simulation results of proposed current mirror-II

The biasing currents (I_b and I_{bias}) are selected as 15 μA and the supply voltage (V_{DD}) is chosen as 1.2 V for the proper operation of the proposed current mirror-II. The values of V_n and R_L used in proposed current mirror-II are 1 V and 5 $k\Omega$, respectively. The aspect ratios (W/L) of the transistors used to design the proposed current mirror-II are given in Table 4.3.

The physical layout of the proposed current mirror-II is shown in Figure 4.27. The layout of the proposed current mirror-II occupies a silicon die area of 34.77 $\mu m \times 32 \mu m$ without including bond pads. The sourcing current source I_b at the output stage and sinking current source I_b at the input stage have been implemented using PMOS transistors M_{10} and NMOS transistor M_{11} , respectively in the layout.

Table 4.3 Aspect ratios of the transistors used to design the proposed current mirror-II

Transistor	W/L ($\mu m/\mu m$)
M_{1a}, M_{1b}	25/1.08
M_2	15.69/1.08
M_3, M_3', M_7	32.97/1.44
M_4, M_{11}	3.06/0.36
M_5	24.12/1.26
M_6	50/1.08
M_8	12.54/0.54
M_9	5.89/1.08
M_{10}	4.12/0.18

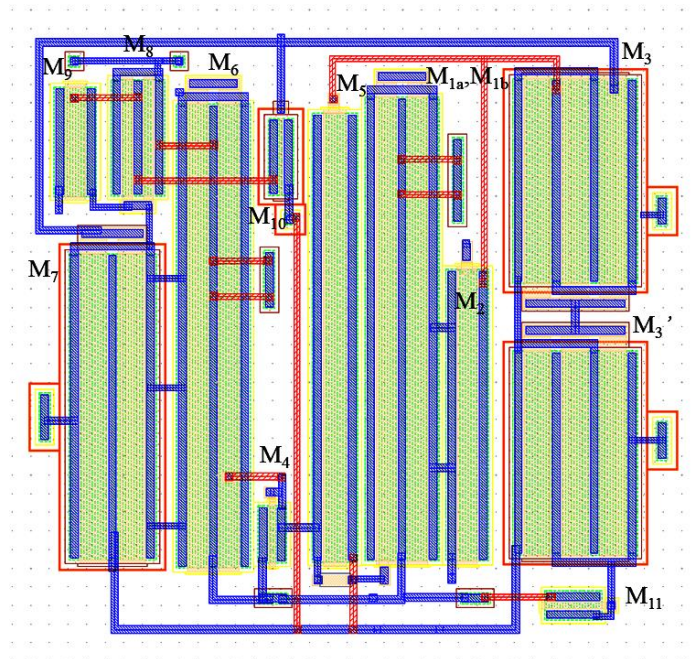


Figure 4.27 Physical layout of the proposed current mirror-II

The DC characteristics of the proposed current mirror-II is shown in Figure 4.28 where the input current varies from 0 to 200 μA . From the plot, it is clear that the output current is mirroring the input current for the range of 0 to 200 μA .

The plot of variation in relative current tracking error for different values of the input current is shown in Figure 4.29. The relative percentage current tracking error of the proposed current mirror-II is obtained as 1.2 %.

The input voltage variation of proposed current mirror-II for the input current which varies from 0 to 200 μA is given in Figure 4.30. It is observed that the proposed current mirror-II requires the input voltage in the range of 0.356 to 0.40 V.

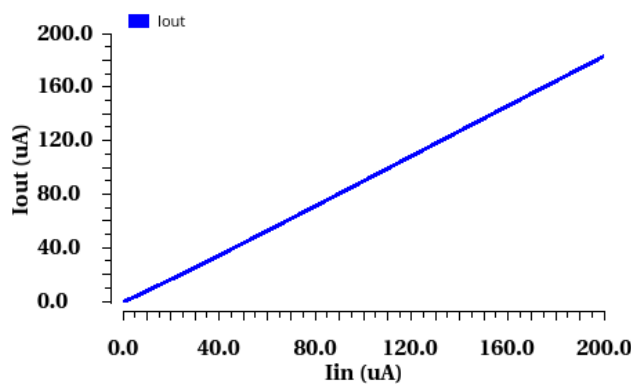


Figure 4.28 DC characteristics of the proposed current mirror-II

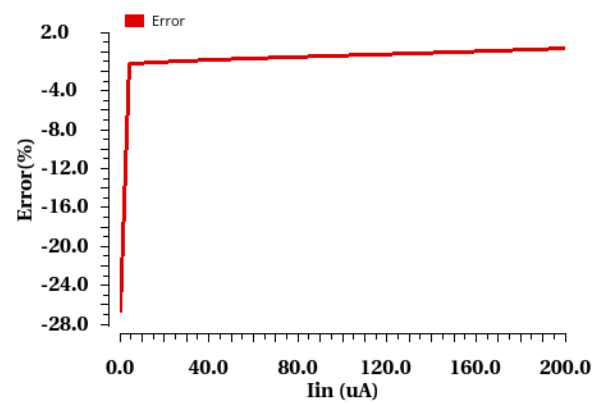


Figure 4.29 Percentage error plot of the proposed current mirror-II

The variations of output current versus the output voltage for different values of input current varying from 50 μA to 200 μA with the increment of 50 μA are shown in Figure 4.31. The minimum required output voltage is obtained as 0.40 V.

The frequency response of the proposed current mirror-II shown in Figure 4.32 is obtained by applying an alternating current source of 1 μA AC magnitude with an offset current of 50 μA (at a frequency of 1 MHz) at the input. The proposed current mirror-II shows the gain and bandwidth of 0.96 and 143.846 MHz, respectively. The plot of input resistance versus frequency of the proposed current mirror-II when quiescent input current is 100 μA is shown in Figure 4.33. From the plot, the input resistance is obtained as 132 Ω . The output resistance is observed using a regulated cascode structure and it is obtained as 13 M Ω as shown in Figure 4.34.

Figure 4.35 shows the transient response of the proposed current mirror-II when a square input pulse of 0 to 200 μA at 1 MHz is applied. It is observed that the output current mirrors the input current. The settling time (2 % of the final value) is obtained as 17.02 ns at the rising edge of output current.

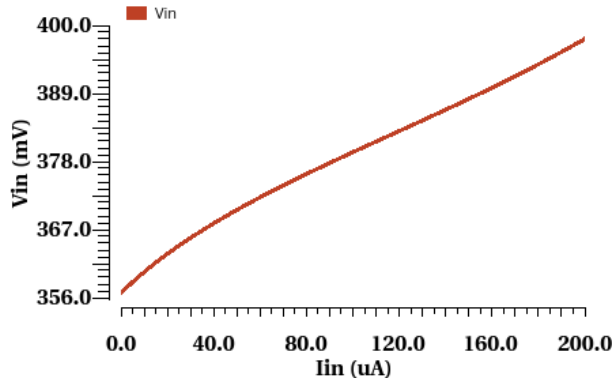


Figure 4.30 Variation of input voltage versus input current of the proposed current mirror-II

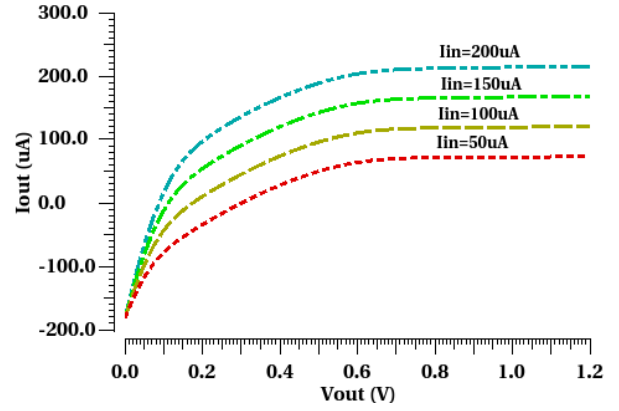


Figure 4.31 Variation of output current versus output voltage of the proposed current mirror-II

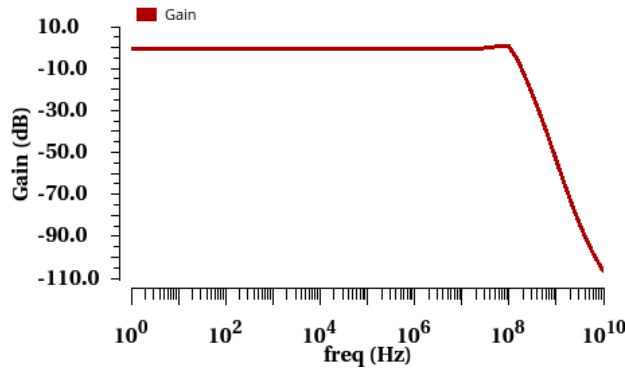


Figure 4.32 Gain versus frequency plot of the proposed current mirror-II

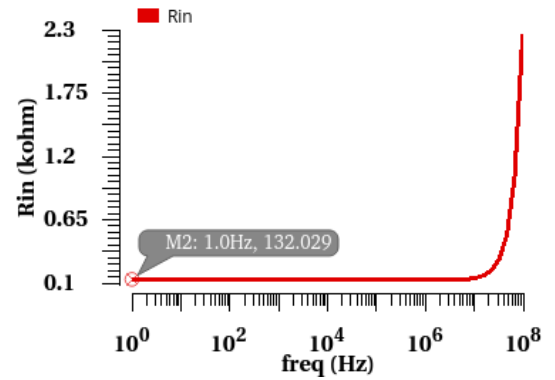


Figure 4.33 Input resistance versus frequency plot of the proposed current mirror-II

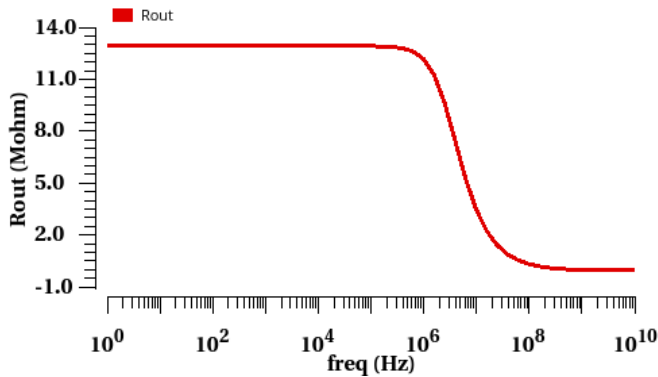


Figure 4.34 Output resistance versus frequency plot of the proposed current mirror-II

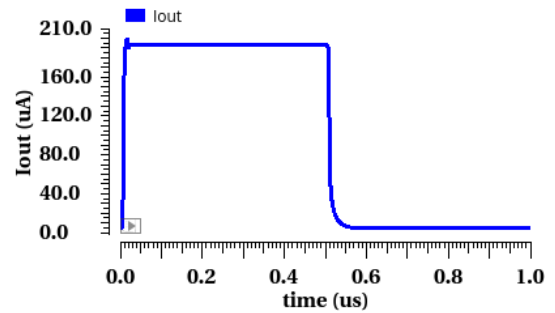


Figure 4.35 Transient response of the proposed current mirror-II

The plot of total harmonic distortion (THD) versus different amplitudes of the input current is shown in Figure 4.36. A sinusoidal input current with a quiescent current of 100 μA at 1 MHz frequency is applied in the proposed current mirror-II for the calculation of THD. From the plot, the THD is observed as less than 1.8 % for the different amplitudes of input current.

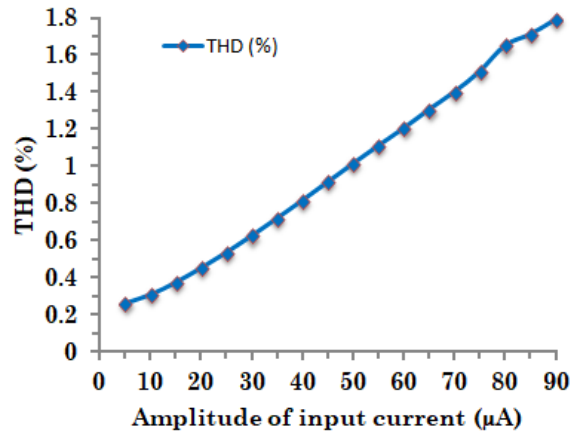


Figure 4.36 THD (%) of the proposed current mirror-II

Table 4.4 Comparison of the proposed current mirror-II with existing current mirrors available in the literature

References→ Parameters↓	[61]	[66]	[121]	[129]	[131]	[134]	[135]	[136]	Proposed current mirror-II
Supply Voltage (V)	1.5	1.2	1.8	1.8	± 0.5	1	1.3	0.9	1.2
Technology (μm)	0.18	0.25	0.18	0.18	0.25	0.18	0.18	0.18	0.18
Current Range (μA)	-----	-----	-----	-----	0 to 280	0.01 to 100	0 to 100	----	0 to 200
% Error	1.4	-----	-----	-----	-----	6 to 11	-----	0.6	1.2
Minimum Input voltage (V)	-----	-----	-----	-----	0.25	-----	-----	0.04	0.35
Minimum Output voltage (V)	-----	-----	0.135	0.4	-----	0.11	-----	0.1	0.40
Output compliance voltage (V)	-----	-----	0.925	0.78	-----	0.89	-----	0.88	0.67
Input Resistance (Ω)	3 k	-----	-----	-----	2.7 k	-----	-----	496	132
Output Resistance (Ω)	-----	-----	1 M	-----	578 k	1.8 M	-----	1 M	13 M
Bandwidth (MHz)	212	168.4	-----	-----	132	-----	162	181	143
Power (μW)	218	102.17	-----	413	-----	-----	-----	154	104
FOM ₁ (MHz ohm ⁻¹)	0.050	-----	-----	-----	-----	-----	-----	0.61	0.902
FOM ₂ (Atto AHZ ⁻¹)	-----	-----	-----	-----	-----	-----	-----	-----	146.122

Table 4.4 compares the performance parameters of the proposed current mirror-II with existing current mirrors available in the literature [61, 66, 121, 129, 131, 134–136]. From the table, it can be seen that the proposed current mirror-II has lower input resistance, higher output resistance and lower power dissipation than the existing structures of current mirrors. Hence, the proposed current mirror-II offers a large value of FOM_1 as compared to [61, 136]. The FOM_2 is based on total power, minimum input voltage required, output current, output resistance, -3 dB bandwidth, and output voltage compliance of the circuit. Some of the parameters required to calculate FOM_2 of the current mirrors reported in the literature have not been mentioned. So, only FOM_2 of the proposed current mirror-II has been calculated.

4.4.3 Simulation results of proposed current mirror-III

The proposed current mirror-III is biased using the currents I_{bias} , I_b and I_{b1} of 20 μA , 20 μA and 100 μA , respectively with $C_{bat} = 500fF$. The supply voltage (V_{DD}) of the proposed current mirror-III is selected as 1.2 V. The values of V_n and R_L used in proposed current mirror-III are 1.2 V and 1.5 $k\Omega$, respectively. The aspect ratios (W/L) of the transistors used to design the proposed current mirror-III are tabulated in Table 4.5.

Table 4.5 Aspect ratios of the transistors used to design the proposed current mirror-III

Transistor	W/L ($\mu m/\mu m$)
M_1, M_{1a}	40.32/1
M_2, M_5, M_8	25.16/1
M_3, M_3', M_9	30.06/0.5
M_4	3.96/0.18
M_6, M_7	6.48/0.18
M_{10}	40.32/0.18
M_{11}	12.56/1
M_{12}	15.06/0.18
M_{13}, M_{14}	1.6/0.18

The physical layout of the proposed current mirror-III is shown in Figure 4.37. In the layout, current sources I_{b1} , I_b and I_{bias} are implemented using MOS transistors M_{12} , M_{13} and M_{14} , respectively. The layout occupies an area of $54.79 \mu m \times 38.04 \mu m$ without including bond pads. The variation of output current for the input current ranging from 0 to 300 μA is shown in Figure 4.38 and it is observed that the output current mirrors the input current. The plot of the current

copying error $(I_{out} - I_{in}/I_{in})$ in percentage versus input current is shown in Figure 4.39. The average value of error is observed as 0.522 %.

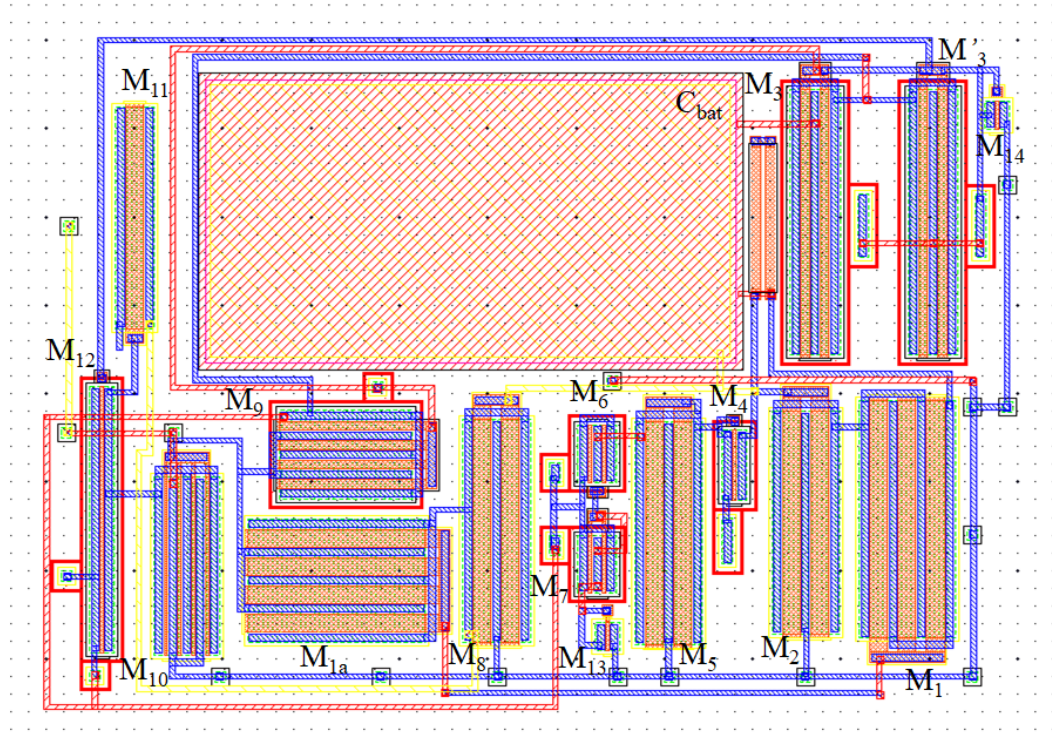


Figure 4.37 Physical layout of the proposed current mirror-III

The variation of input voltage versus input current which varies from 0 to 300 μA is shown in Figure 4.40. From the figure, it is observed that the minimum required input voltage is 0.347 V. Figure 4.41 shows the variation of output current versus the output voltage for various values of input current i.e. 50 μA , 100 μA , 150 μA , 200 μA , 250 μA and 300 μA . The minimum required value of output voltage is obtained as 0.20 V.

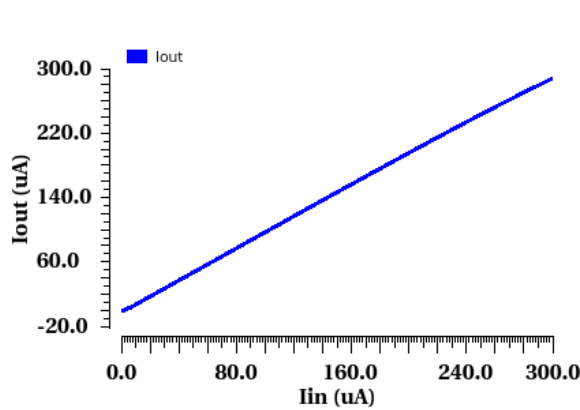


Figure 4.38 DC characteristics of the proposed current mirror-III

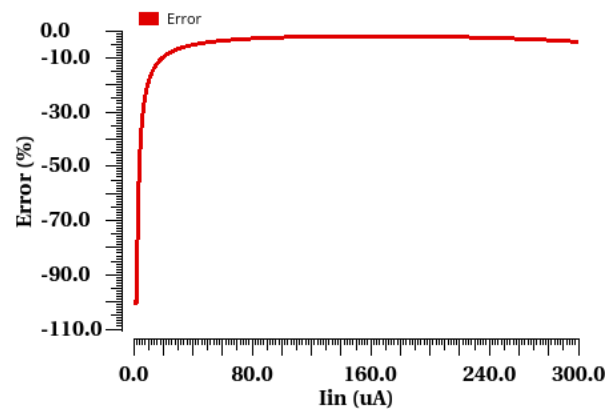


Figure 4.39 Percentage error plot of the proposed current mirror-III

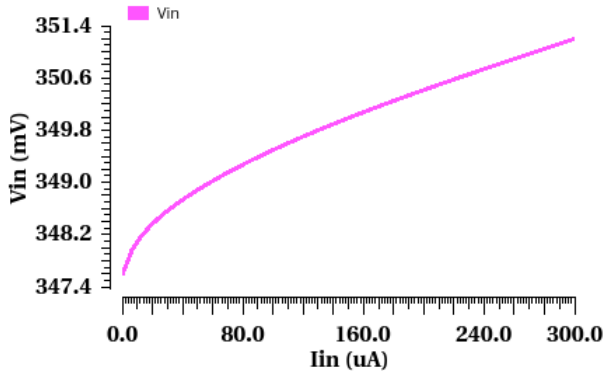


Figure 4.40 Variation of input voltage versus input current of the proposed current mirror-III

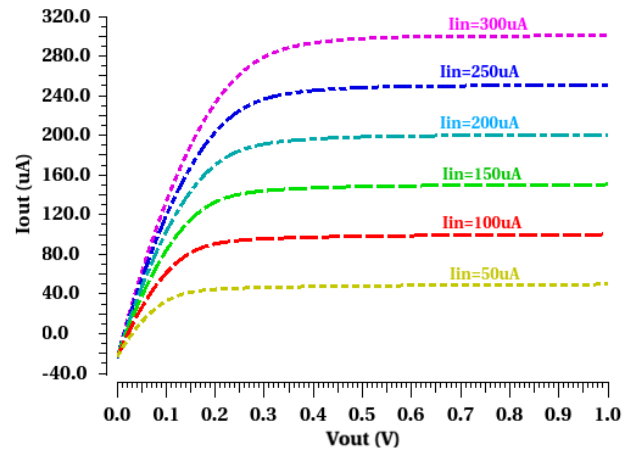


Figure 4.41 Variation of output current versus output voltage of the proposed current mirror-III

The frequency response of the proposed current mirror-III illustrated in Figure 4.42 is obtained by applying an alternating current source of $1 \mu\text{A}$ AC magnitude with an offset current of $50 \mu\text{A}$ (at a frequency of 1 MHz) at the input. The proposed current mirror-III shows the gain and bandwidth of 0.994 and 319.8 MHz , respectively.

The plots of input resistance versus frequency when the input current is $50 \mu\text{A}$ and output resistance versus frequency are shown in Figures 4.43 and 4.44, respectively. The plots show that the proposed current mirror-III offers input resistance of 161Ω and output resistance of 19.83 MHz .

The step response of the proposed current mirror-III for the square input current which varies from 0 to $300 \mu\text{A}$ at 1 MHz is shown in Figure 4.45. From the plot, the settling time is obtained as 40 ns at the rising edge of output current.

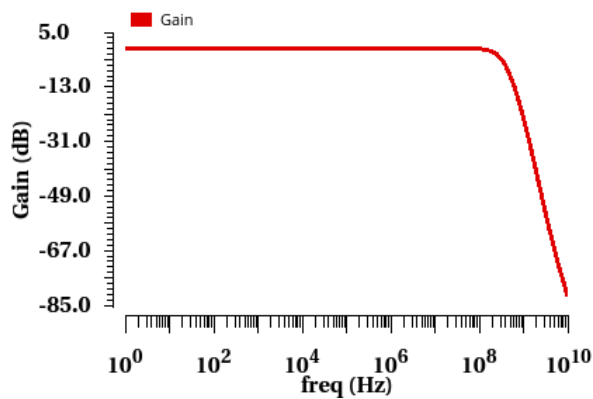


Figure 4.42 Gain versus frequency plot of the proposed current mirror-III

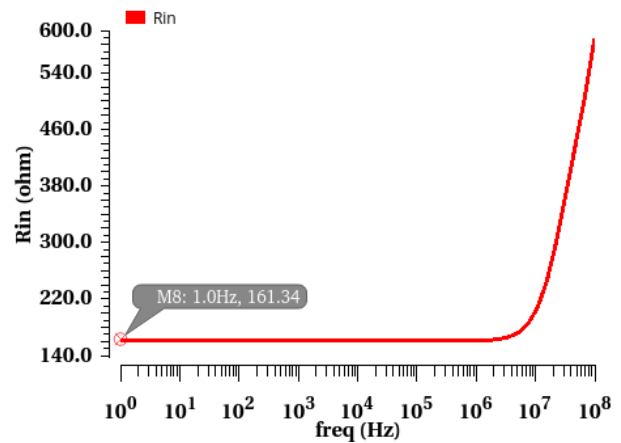


Figure 4.43 Input resistance versus frequency plot of the proposed current mirror-III

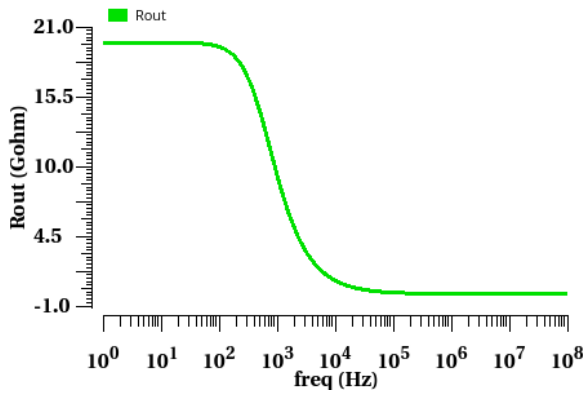


Figure 4.44 Output resistance versus frequency plot of the proposed current mirror-III

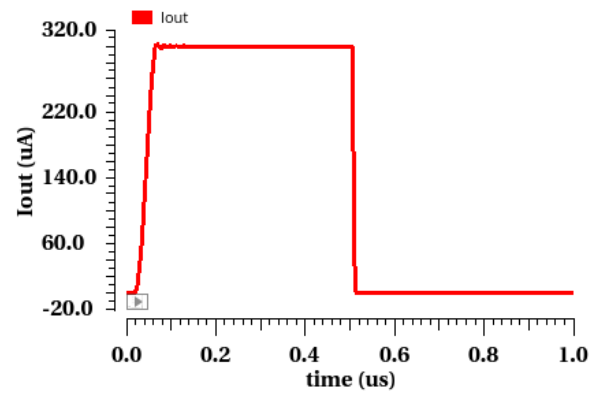


Figure 4.45 Transient response of the proposed current mirror-III

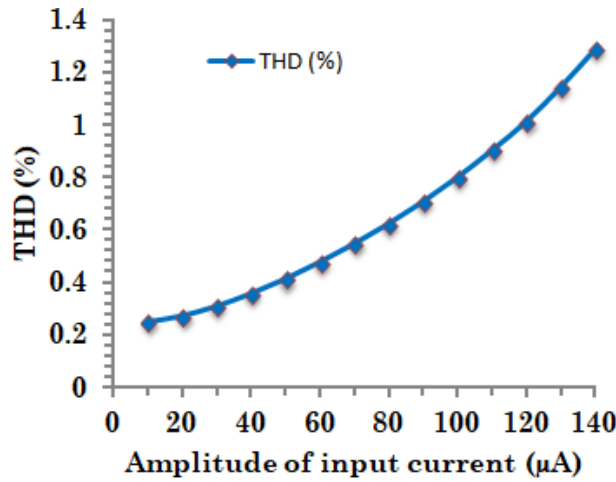


Figure 4.46 THD (%) of the proposed current mirror-III

The total harmonic distortion (THD) plot of the proposed current mirror-III for the different amplitudes of the input current is shown in Figure 4.46. For the calculation of THD (%), the input current is given at 1 MHz frequency and the quiescent current is kept at 150 μA . The plot shows that the THD for different amplitudes of input current remains less than 1.4 %.

The different performance parameters of the proposed current mirror-III and existing current mirrors reported in the literature [61, 66, 121, 129–136] have been listed in Table 4.6. From the table, it is observed that the proposed current mirror-III shows the highest FOM_1 and lowest FOM_2 . Also, the proposed current mirror-III offers high output resistance, wide bandwidth, low input resistance, and less current copying error. However, the proposed current mirror-III shows improved performance at the expense of an increase in the area since there are some tradeoffs between different circuit parameters in analog electronics.

Table 4.6 Comparison of the proposed current mirror-III with existing current mirrors available in the literature

References→ Parameters↓	[61]	[66]	[121]	[129]	[130]	[131]	[132]	[133]	[134]	[135]	[136]	Proposed current mirror -III
Supply Voltage (V)	1.5	1.2	1.8	1.8	±0.4	±0.5	±0.3	±0.2	1	1.3	0.9	1.2
Technology (μm)	0.18	0.25	0.18	0.18	0.18	0.25	0.18	0.18	0.18	0.18	0.18	0.18
Current Range (μA)	-----	-----	-----	0 to 100	-----	0 to 280	0 to 200	0 to 250	0.01 to 100	0 to 100	0 to 100	0 to 300
% Error	1.4	-----	-----	-----	-----	-----	-----	-----	6 to 11	-----	0.6	0.52
Minimum Input voltage (V)	-----	-----	-----	-----	-----	0.25	-----	-----	-----	-----	0.04	0.34
Minimum Output voltage (V)	-----	-----	0.135	0.4	0.3	-----	0.10	-----	0.11	-----	0.1	0.20
Output voltage Compliance (V)	-----	-----	0.925	0.78	0.625	-----	0.83	-----	0.89	-----	0.89	0.83
Input Resistance(Ω)	3 k	-----	-----	-----	-----	2.7 k	306	240	-----	-----	496	161.34
Output Resistance (Ω)	-----	-----	1 M	-----	3.33 M	578 k	165 k	19.5 G	1.8 M	-----	1M	19.83 G
Bandwidth (MHz)	212	168.4	-----	-----	-----	132	180	285	-----	162	181	319.8
Power Dissipation (μW)	218	102.1	-----	413	39.48	-----	-----	349	-----	-----	154	94
FOM ₁ (MHz ohm ⁻¹)	0.050	-----	-----	-----	-----	-----	-----	-----	-----	-----	0.608	3.81
FOM ₂ (Atto Ahz ⁻¹)	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	420	0.0242

4.4.4 Simulation results of proposed current mirror-IV

The proposed current mirror-IV is biased using currents I_{b1s} , I_b and I_{b1} of 20 μA, 20 μA and 100 μA, respectively. The supply voltage (V_{DD}) of the proposed current mirror-IV is selected as 1.5 V. The resistance R_b is chosen as 5 kΩ. The values of V_n and R_L are 1 V and 1 kΩ, respectively. The aspect ratios (W/L) of the transistors used to design the proposed current mirror-IV are listed in Table 4.7.

The physical layout of the proposed current mirror-IV is shown in Figure 4.47. The current sources I_{b1} and I_b are implemented using MOS transistors M_{16} and M_{17} , respectively. The layout occupies an area of 26.12 μm × 49.77 μm without including bond pads.

The DC characteristics of the proposed current mirror-IV is shown in Figure 4.48. From the figure, it is observed that the output current mirrors the input current for the range of 0 to 500

μA . The plot of error (%) between output current and input current during mirroring is shown in Figure 4.49. The average value of error (%) is calculated as 0.82 %.

Table 4.7 Aspect ratios of the transistors used to design the proposed current mirror-IV

Transistor	W/L ($\mu\text{m}/\mu\text{m}$)
M_1, M_7, M_8, M_{12}	12/0.72
M_2, M_5, M_{13}	30/0.54
M_3, M_3', M_{11}	20/0.72
M_4	8/0.36
M_6	15/0.36
M_9	18/0.54
M_{10}	36/0.54
M_{14}	20.32/0.18
M_{15}	10/1
M_{16}	30/0.36
M_{17}	4/0.36

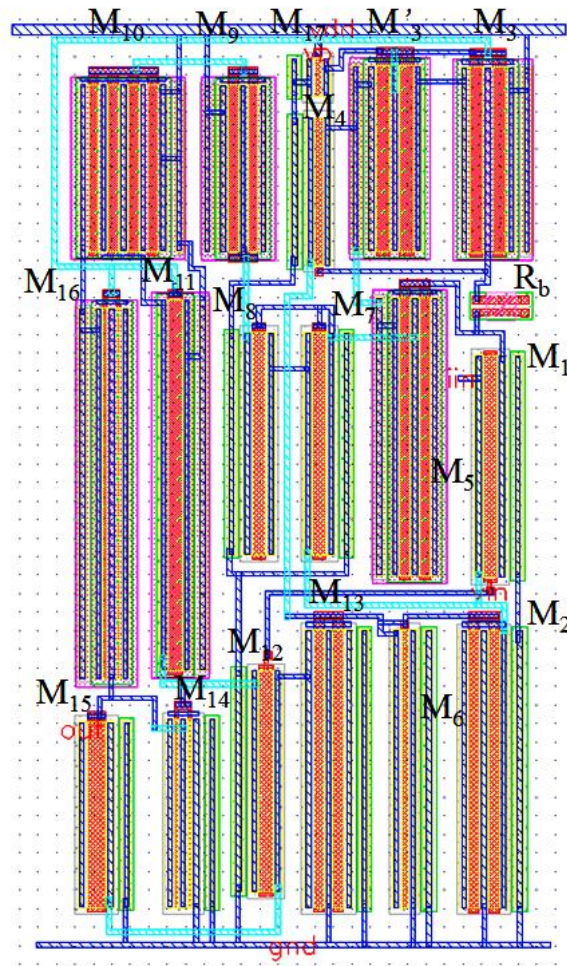


Figure 4.47 Physical layout of the proposed current mirror-IV

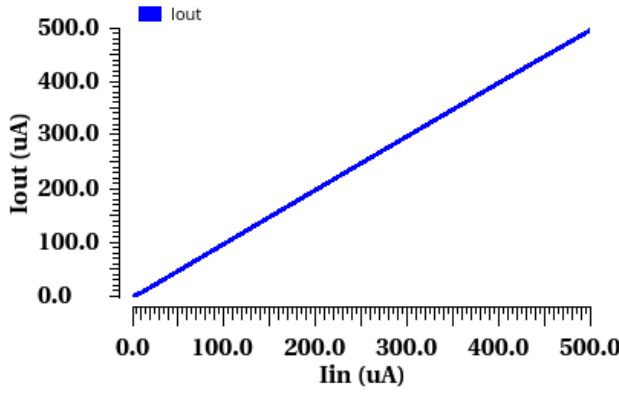


Figure 4.48 DC characteristics of the proposed current mirror-IV

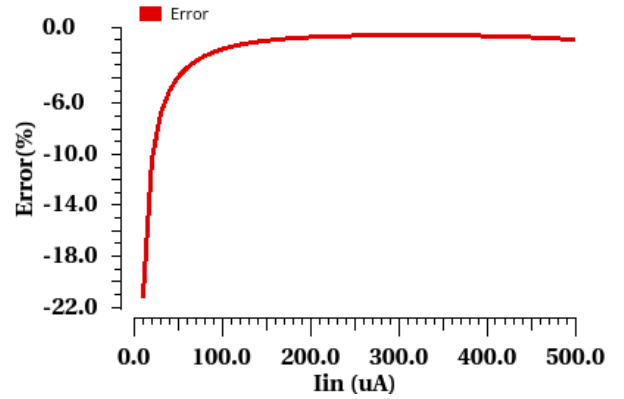


Figure 4.49 Percentage error plot of the proposed current mirror-IV

The variation of input voltage for the input current which varies from 0 to 500 μA is shown in Figure 4.50. From the figure, it is observed that the minimum required input voltage is 0.38 V. The variations of output current versus the output voltage for various values of input current i.e. 100 μA , 200 μA , 300 μA , 400 μA , and 500 μA are shown in Figure 4.51. The minimum required value of output voltage is obtained as 0.32 V.

The gain versus frequency plot of the proposed current mirror-IV shown in Figure 4.52 is obtained by applying an alternating current source of 1 μA AC magnitude with an offset current of 50 μA (at a frequency of 1 MHz) at the input. From the plot, it is observed that the gain and bandwidth of the proposed current mirror-IV are 0.998 and 208 MHz, respectively.

The plot of input resistance versus frequency when the input current is 50 μA is shown in Figure 4.53. The proposed current mirror-IV offers low input resistance of 24.15 Ω . The plot of output resistance versus frequency of proposed current mirror-IV is shown in Figure 4.54 which shows that the output resistance is 28.39 G Ω .

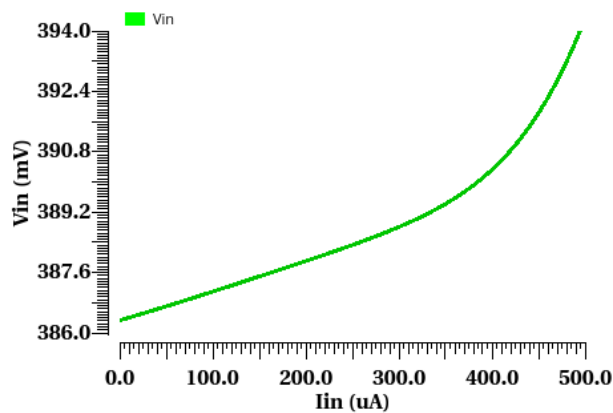


Figure 4.50 Variation of input voltage versus input current of the proposed current mirror-IV

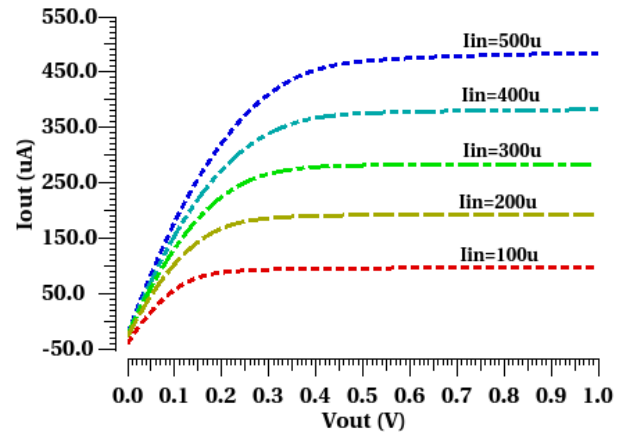


Figure 4.51 Variation of output current versus output voltage of the proposed current mirror-IV

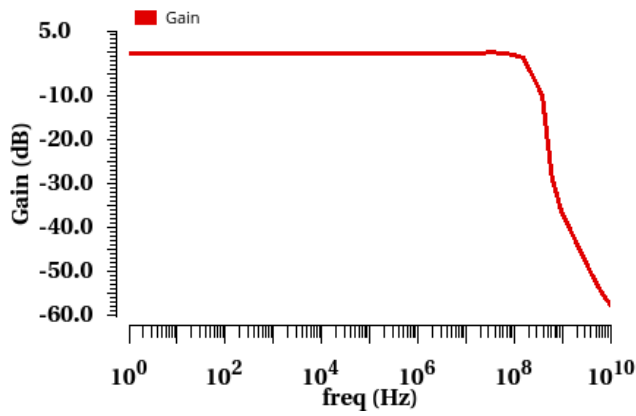


Figure 4.52 Gain versus frequency plot of the proposed current mirror-IV

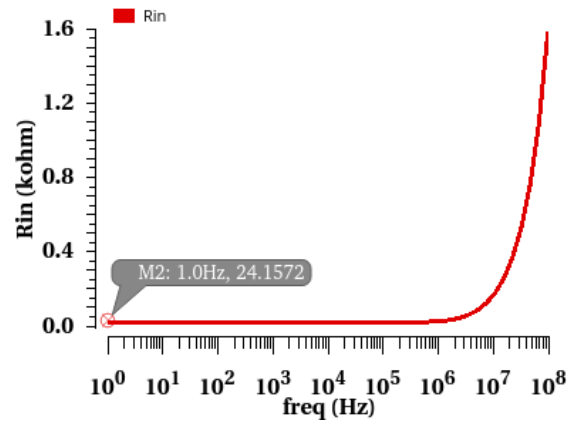


Figure 4.53 Input resistance versus frequency plot of the proposed current mirror-IV

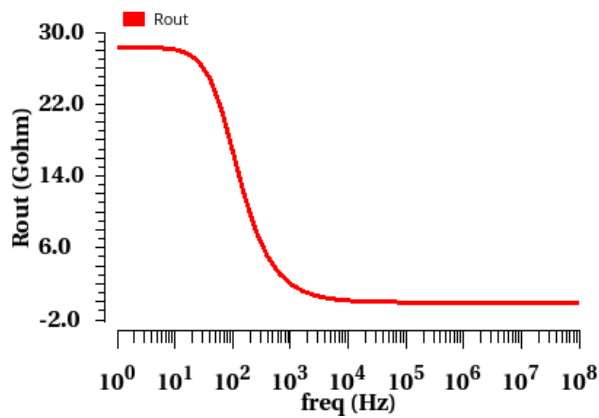


Figure 4.54 Output resistance versus frequency plot of the proposed current mirror-IV

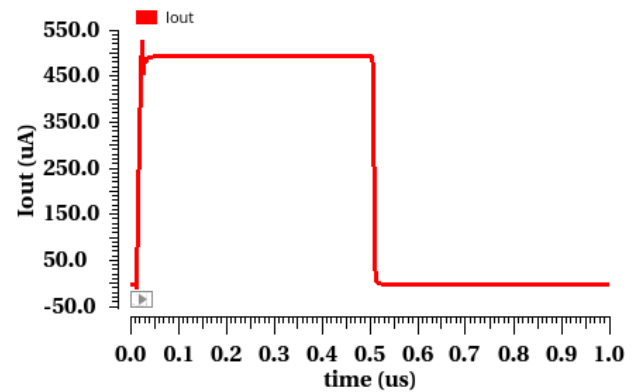


Figure 4.55 Transient response of the proposed current mirror-IV

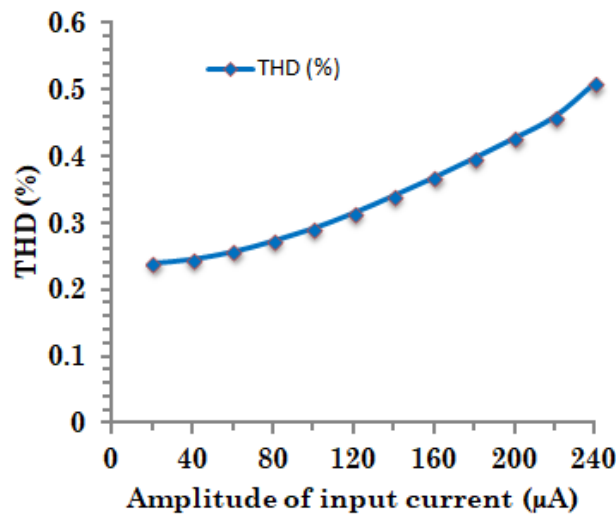


Figure 4.56 THD (%) of the proposed current mirror-IV

The transient response of proposed current mirror-IV when input current pulse of 0 to 500 μA at 1 MHz is applied is shown in Figure 4.55. From the figure, settling time (2% of the final value) is obtained as 32.10 ns at the rising edge of output current.

The plot of total harmonic distortion (THD) of the proposed current mirror-IV for the different amplitudes of the input current is shown in Figure 4.56. The different amplitudes of input current are given at a frequency of 1 MHz and the quiescent current is kept at 250 μA for the calculation of THD (%). The plot shows that the THD remains less than 0.6 % for different amplitudes of input current.

The proposed current mirror-IV has been compared with various existing current mirrors reported in the literature [61, 66, 72, 121, 129–137] in Table 4.8. From the table, it is observed that the proposed current mirror-IV offers a large current range, low input resistance and high output resistance. Also, the table shows that the proposed current mirror-IV offers the highest FOM_1 and lowest FOM_2 which confirm its better performance.

Table 4.8 Comparison of the proposed current mirror-IV with existing current mirrors available in the literature

References→ Parameters↓	[61]	[66]	[72]	[121]	[129]	[130]	[131]	[132]	[133]	[134]	[135]	[136]	[137]*	Proposed current mirror-IV
Supply Voltage (V)	1.5	1.2	0.9	1.8	1.8	± 0.4	± 0.5	± 0.3	± 0.2	1	1.3	0.9	± 0.75	1.5
Technology (μm)	0.18	0.25	0.18	0.18	0.18	0.18	0.25	0.18	0.18	0.18	0.18	0.18	0.5	0.18
Current Range (μA)	-----	-----	0 to 100	-----	0 to 100	-----	0 to 280	0 to 200	0 to 250	0.01 to 100	0 to 100	0 to 100	-----	0 to 500
% Error	1.4	-----	<3	-----	-----	-----	-----	-----	-----	6 to 11	-----	0.6	-----	0.82
Minimum Input voltage (V)	-----	-----	0.8	-----	-----	-----	0.25	-----	-----	-----	-----	0.04	-----	0.38
Minimum Output voltage (V)	-----	-----	0.38	0.135	0.4	0.3	-----	0.10	-----	0.11	-----	0.1	-----	0.32
Output voltage Compliance (V)	-----	-----	0.577	0.925	0.78	0.625	-----	0.83	-----	0.89	-----	0.89	-----	0.786
Input Resistance(Ω)	3 k	-----	43.5	-----	-----	-----	2.7 k	306	240	-----	-----	496	21	24.15
Output Resistance (Ω)	-----	-----	6.93 M	1 M	-----	3.33 M	578 k	165 k	19.5 G	1.8 M	-----	1 M	177 M	28.3 G
Bandwidth (MHz)	212	168.4	1730	-----	-----	-----	132	180	285	-----	162	181	66	280
Power Dissipation (μW)	218	102.1	-----	-----	413	39.48	-----	-----	349	-----	-----	154	120	143.85
FOM_1 (MHz ohm^{-1})	0.050	-----	13.25	-----	-----	-----	-----	-----	-----	-----	-----	0.608	-----	14.12
FOM_2 (Atto AHz^{-1})	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	420	-----	0.0116

*Experimental

4.5 Conclusion

This chapter has proposed four different current mirror structures based on class-AB FVF cells namely current mirror-I, current mirror-II, current mirror-III and current mirror-IV. The small-signal analyses of the proposed current mirrors have been performed to compute input resistance, output resistance, transfer function and bandwidth. The physical layouts and post-layout simulation results of the proposed current mirrors are presented to demonstrate their performance. The features of the proposed current mirrors can be summarized as

- The proposed current mirror-I requires minimum output voltage and offers the highest output compliance voltage while consuming less power. But, the proposed current mirror-I has high input resistance and low output resistance.
- The proposed current mirror-II offers improved input resistance, output resistance, current mirroring range and error as compared to the proposed current mirror-I. But it shows comparable bandwidth and power consumption as that of the proposed current mirror-I.
- The proposed current mirror-III further improves the current mirroring range with less error. It offers higher output resistance and bandwidth than the proposed current mirror-II. However, the input resistance of the proposed current mirror-III is high.
- The proposed current mirror-IV offers low input resistance and high output resistance. It also shows a large current mirroring range while the other performance parameters such as error and bandwidth are limited as compared to the proposed current mirror-III.

Therefore, it is concluded that the proposed current mirror-III and current mirror-IV are the optimal current mirrors based on current mirroring range, error, input resistance, output resistance and bandwidth. Further, the proposed current mirrors have been compared with the existing current mirrors available in the literature using two figures of merit (FOM_1 and FOM_2) and it is observed that the proposed current mirror-IV has the highest FOM_1 and lowest FOM_2 .

CHAPTER 5

CONCLUSION AND FUTURE SCOPE

5.1 Conclusion

The increasing prominence of miniaturized circuits and portable systems has led to the development of low-voltage/low-power (LV/LP) analog circuits. But, it is a very challenging task for analog circuit designers to operate the analog circuits at low supply voltage without degrading their performance. To achieve low voltage operation of the analog circuits, the various LV/LP transistor implementation techniques such as bulk-driven MOSFETs, level shifter, sub-threshold MOSFETs, self-cascode MOSFETs, floating-gate MOSFETs, flipped voltage follower (FVF) cell, etc. are widely used. Out of these LV/LP transistor implementation techniques, FVF cell offers advantages of low supply voltage requirement, low power dissipation, and hence it increases device portability. But, the conventional FVF cell shows class-A behaviour since the bias current limits the maximum current at the output. So, the FVF cell needs to be modified to achieve class-AB behaviour which enables driving of large capacitive loads without an increase in bias current. In the thesis, four class-AB FVF cells namely class-AB FVF cell-I, class-AB FVF cell-II, class-AB FVF cell-III, and class-AB FVF cell-IV have been proposed which offer several improved electrical features such as current sourcing/sinking capability, output resistance, slew rate, and input/output voltage swing.

In a conventional FVF cell, the output voltage follows the input voltage with the DC level shift of gate-to-source voltage. The proposed class-AB FVF cell-I reduces the level shift between input and output voltages and shows approximately unity voltage gain. But, the proposed class-AB FVF cell-I shows limited bandwidth as the input voltage is applied at the bulk terminal. So, the gate-driven input transistors are employed in the other three suggested FVF cells. The class-AB FVF cells (II and III) show symmetrical slew rates but the output resistances of these class-AB FVF cells are not low enough. To reduce the output resistance, a folding transistor has been used in class-AB FVF cell-IV. Due to the various advantages offered by the proposed class-AB FVF cells, these can be widely used in the designing of various analog and mixed-signal circuits. The different structures of the current mirror namely current mirror-I, current mirror-II, current mirror-III, and current mirror-IV are also presented as applications of the proposed class-AB FVF cells in the work. The proposed class-AB FVF cells are used at the input stages of the current mirrors to achieve low input resistance. The proposed current mirror-III and current

mirror-IV are the optimal current mirrors among four proposed current mirrors in terms of current mirroring range, error, input resistance, output resistance, and bandwidth. Further, the proposed current mirrors have been compared with the existing current mirrors available in the literature using two figures of merit and it is observed that the proposed current mirror-IV has the highest first figure of merit and lowest second figure of merit which confirm its better performance.

5.2 Future Scope

The class-AB FVF cells offering enhanced slew rate without increase in bias current have been proposed in this work, but still, there is some scope that can be carried forward in the future. The proposed FVF cells designed using NMOS transistors suffer from the body effect which results in less than unity voltage gain. So, to achieve approximately unity voltage gain, the input NMOS transistors of the proposed FVF cells can be designed without body effect using twin well technology. The proposed FVF cells have been employed at the input stage to design low input resistance current mirrors. The work can also be extended to design other basic analog circuits such as operational transconductance amplifiers, low drop-out regulators, current conveyors, etc.

List of Publications

SCI Journal Papers

Published

1. Caffey Jindal, Rishikesh Pandey, “High Performance CMOS Current Mirror Using Class-AB Level Shifted Bulk Driven Flipped Voltage Follower Cell,” *Journal of Circuits, Systems, and Computers*, vol. 28, no. 8, pp. 1950140-1-21, 2019. doi: 10.1142/S0218126619501408 (SCI Journal, **Impact Factor: 1.278, Publisher: World Scientific**)
2. Caffey Jindal, Rishikesh Pandey, “High slew rate and low output resistance class-AB flipped voltage follower cell with increased current driving capability”, *Sādhana*, vol. 45, no. 108, pp. 1-5, 2020. doi: 10.1007/s12046-020-01350-0 (SCI Journal, **Impact Factor: 1.214, Publisher: Springer**)
3. Caffey Jindal, Rishikesh Pandey, “A class-AB flipped voltage follower cell with high symmetrical slew rate and high current sourcing/sinking capability”, *International Journal of Circuit Theory and Applications*, vol. 48, no. 7, pp. 1108-1123, 2020. doi: 10.1002/cta.2782 (SCI Journal, **Impact Factor: 2.378, Publisher: Wiley**)
4. Caffey Jindal, Rishikesh Pandey, “Class-AB Flipped Voltage Follower Cell with High Current Driving Capability and Low Output Resistance for High Frequency Applications”, *Wireless Personal Communications*, vol. 118, pp. 773-787, 2021. doi: 10.1007/s11277-020-08043-1 (SCI Journal, **Impact Factor: 2.017, Publisher: Springer**)
5. Caffey Jindal, Rishikesh Pandey, “A very low output resistance and wide-swing class-AB level-shifted folded flipped voltage follower cell”, *Integration*, vol. 81, pp. 84-98, 2021. doi:10.1016/j.vlsi.2021.05.001 (SCI Journal, **Impact Factor: 1.345, Publisher: Elsevier**)
6. Caffey Jindal, Rishikesh Pandey, “A high output resistance, wide bandwidth, and low input resistance current mirror using flipped voltage follower cell”, *International Journal of Circuit Theory and Applications*, vol. 49, no. 10, pp. 3286-3301, 2021. doi: 10.1002/cta.3085 (SCI Journal, **Impact Factor: 2.378, Publisher: Wiley**)

Communicated

1. Caffey Jindal, Rishikesh Pandey, “A low-power bulk-driven flipped voltage follower based current mirror”, *Wireless Personal Communications*. (Communicated)
2. Caffey Jindal, Rishikesh Pandey, “High-performance flipped voltage follower based low input resistance current mirror with wide current mirroring range and high output resistance”, *Integration*. (Communicated)

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