Numerical Investigation of Thermal Management and Structural Integrity of MCM-BGA array using Porous MCHS

A thesis submitted in partial fulfillment of the requirements
for the award of the degree of

Master of Engineering

in

Thermal Engineering

by

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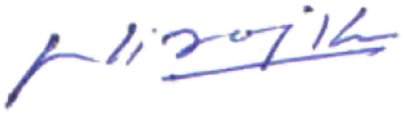
August, 2024

Certificate

This is to certify that the dissertation entitled **"Numerical Investigation of Thermal Management and Structural Integrity of MCM-BGA array using Porous MCHS"**, submitted by **Harpreet Singh** to the Thapar Institute of Engineering & Technology, for the award of the degree of ME Thermal Engineering, represents original and bonafide research work carried out by him under our mentorship. The dissertation meets the standards and fulfills the requirements as stipulated by the regulations governing the award of the degree.

To the best of our knowledge, the research findings presented in this dissertation have not been previously submitted, either in whole or in part, to any other university or institute for the award of any degree or diploma.



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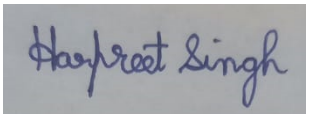
Declaration

I hereby declare that this dissertation is a product of my own work and reflects my original ideas. Where I have incorporated the ideas and words of others, I have duly cited and referenced the original sources. I affirm that I have adhered to the principles of academic honesty and integrity, and have not misrepresented, fabricated, or falsified any ideas, data, facts, or sources in this submission. I understand that any breach of the above may result in disciplinary action by the Institute and could also lead to legal consequences if proper citation or permission has not been obtained where required.



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Abstract

Effective thermal management of packaging technology is a critical factor for the reliable functioning of electronic equipment. This study explores and compares the thermal management of MCM-BGA array using cooling methods, including heat spreader coupled with different microchannel heat sinks (MCHS) configurations. Numerical analysis has been conducted to evaluate various setups' thermal and structural performance using COMSOL Multiphysics software. The study evaluates temperature profiles and thermal stress distributions to determine the efficacy of the proposed cooling solutions. The CHT analysis of the designed MCM-BGA package equipped with all-sided porous MCHS reduces 58 degrees from the hotspots compared to the baseline configuration comprising only a heat spreader. Similarly, the thermo-structural analysis revealed that a package encompassing all-sided porous MCHS reduces significant 125 MPa maximal thermal stress, representing 51.7% improvement compared to the baseline setup. The resultant optimized configuration of all-sided porous MCHS obtained using the Nelder Mead optimization algorithm improves the Figure of Merit (FOM) and heat transfer coefficient by 10.7% and 23.8%, respectively, at a Reynolds number of 700. Additionally, fatigue analysis indicates the all-sided optimized porous package configuration is best for maintaining the structural integrity and reliability of the solders, demonstrating the highest cycles to failure for the critical solders.

Acknowledgement

I sincerely express my profound gratitude to my supervisor, Dr. Neeraj Kumar, for his unwavering support, encouragement, and guidance throughout this project. I would also like to express my deep appreciation to Dr. Sandeep Nain for his valuable input over the past few months, which enabled me to complete this research on time. My heartfelt thanks go to Professor Dr. J.S. Saini for his continuous support and guidance during my master's studies.

Lastly, I am immensely grateful to my parents for their unwavering support and motivation, which played a crucial role in driving me to excel throughout this project and my academic journey.

Publications

1. Singh, H., Whan, A.S., Kumar, N., "Investigation of Micro Channel Heat Sink and Graphene-Based Heat Spreader for Thermal Management of 3D TSV Chip". 4th Biennial International Conference on Future Learning Aspects of Mechanical Engineering (FLAME 2024), 31 July to 02 August 2024, Noida, India

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Abbreviations

MCM-BGA Array	Multi-Chip Module Ball Grid Array
IC	Integrated circuit
I/O	Input/Output
MCP	Multi-chip packaging
SIP	System-in-package
CTE	Coefficient of thermal expansion
MCHS	Micro-channel heat sink
FEM	Finite element method
MEMS	Micro-electro-mechanical systems
ASIC	Application-specific integrated circuit
IGBT	Insulated-gate bipolar transistor
MPF	Micro pin fin
VLSI	Very large-scale integrated
MCM	Multi chip module

Symbols

ϵ	Porosity of the porous domain
$\vec{V}$	Velocity vector of fluid
Pi	Pressure
V_{th}	Threshold voltage
I_{DS}	Drain-source current
K_p	Permeability
C	Forchheimer's constante
μ_f	Fluid viscosity
T	Temperature
k_e	Effective thermal conductivity
$(\rho c)_e$	Effective volumetric heat capacity
ν	Poisson's ratio
E	Young's modulus
σ	Thermal stress
ε	Thermal strain
α	Linear expansion coefficient
D_h	Hydraulic diameter of the channel
T_{max}	Maximum temperature of the heat sink
A_w	Area of the heated wall
$T_{(w,m)}$	Average wall temperature
$T_{(f,m)}$	Volume average temperature of the fluid
$\dot{\varepsilon}$	Plastic strain rate
ξ	Multiplier of stress

m	Strain rate sensitivity
Q	Activation energy
R	Universal gas constant
h_0	Hardening constant
a	Strain rate sensitivity of hardening
$\hat{s}$	Coefficient
n	Strain rate sensitivity for the saturation
N_f	Cycles to failure
N_0	Cycles to crack initiation
ΔW	Average viscoplastic energy density dissipated/cycle
a	Final crack size
da/dN	Crack growth rate
$K1, K2, K3, K4$	Material constants
N_f	Cycles to failure
$\Delta\varepsilon_p$	Plastic strain amplitude
ε_p	Effective plastic strain
c	Fatigue ductility exponent
ε'_f	Fatigue ductility coefficient

Chapter 1

Introduction

1.1 Background

Electronic devices have become an integral part of our daily lives, playing a pivotal role in various aspects of modern living, such as healthcare, transportation, telecommunication, computing, etc. As electronic devices continue to grow in complexity to meet increasing performance demands, ensuring their reliability becomes increasingly critical. This has prompted the researchers to explore alternatives to the traditional electronics packaging technology currently practiced in the industry [1].

The electronic package serves as a link connecting integrated circuits, multiple electronic components, and sub-units into a single unit, ensuring that the unit and environment do not interfere with each other [2]. Electronic packaging is characterized by three key parameters that highly influence the effectiveness of packaging at the system level:

- the Input/Output count and the wiring requirements of the Integrated Circuit (IC) package
- the size of the ICs and other functional components

- the power allowance between ICs and passive devices.

The function of electronics packaging involves providing a path to allow signal and power distribution to and from the chip and passive devices while maintaining an efficient heat removal rate and structural integrity, as illustrated in Figure 1.1.

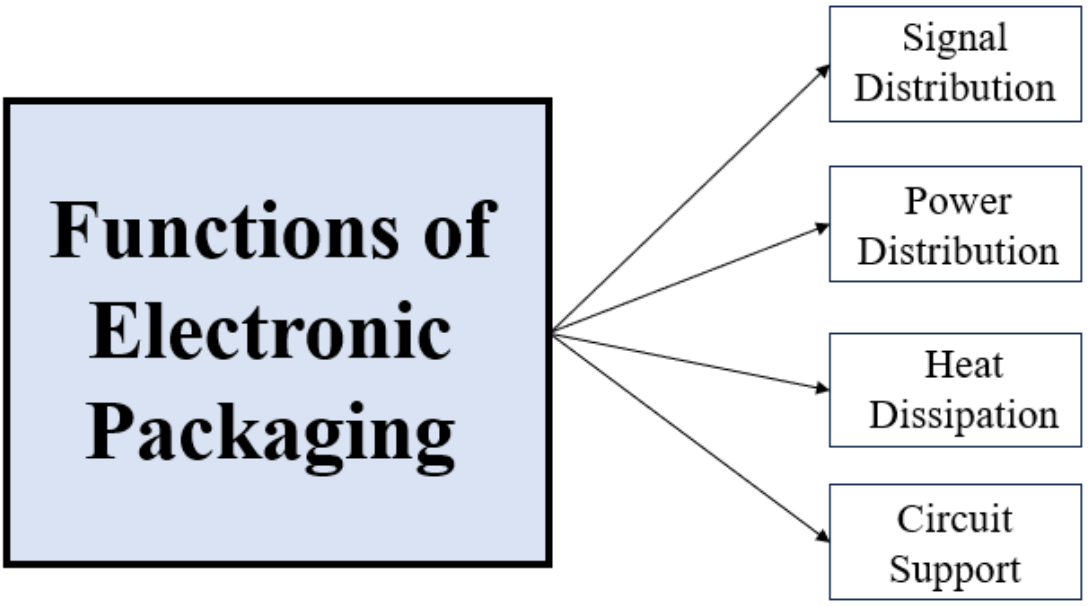


FIGURE 1.1: Various functions of electronics packaging.

The interconnections between various components of an integrated package can significantly influence the performance of the integrated chip. Therefore, these interconnections must exhibit low reflection and low insertion losses [3]. Various types of interconnections have been developed over the years; the common ones that exist are, namely, wire bonding and flip chip bonding. Wire bonding, as shown in Figure 1.2(a), is still one of the most prevalent techniques for creating interconnects in power-electronic devices operating at lower frequencies. The connection between the semiconductor die, and the substrate is created utilizing metallic wires. Despite its extensive usage, it has certain limitations:

- Increase in electrical resistance and thermal impedance due to connection among no. of I/O leads and dies.
- Parasitic inductance dominates at elevated frequencies, leading to signal losses.
- Poor thermo-mechanical reliability.

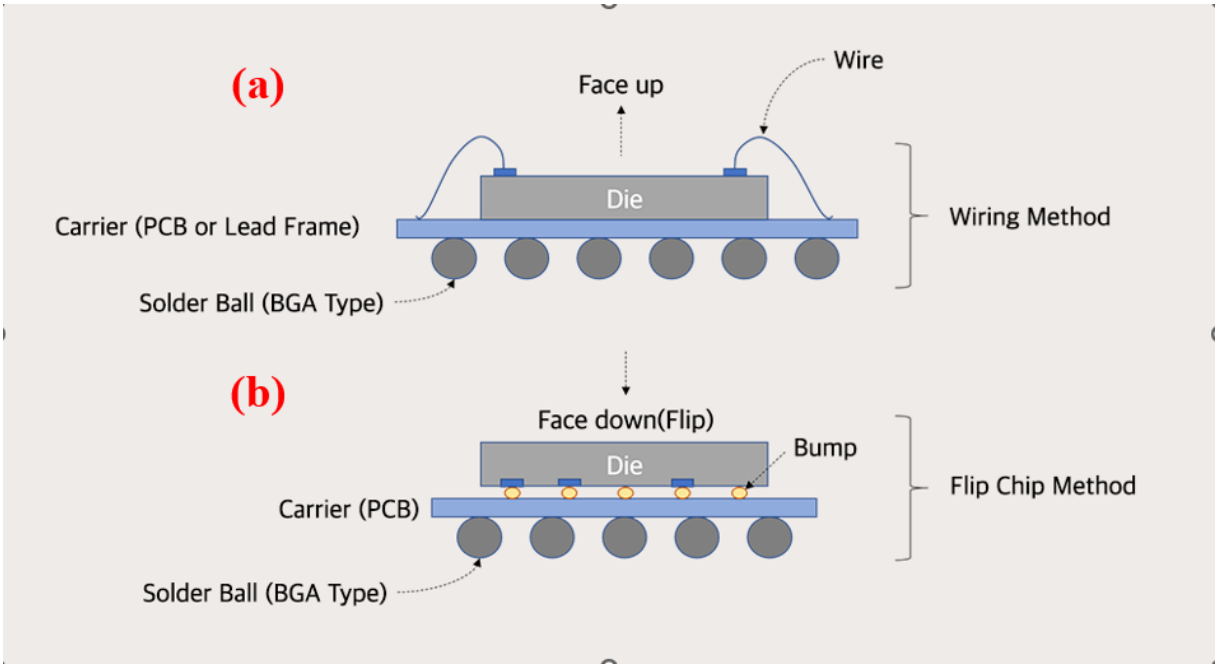


FIGURE 1.2: Comparison of Packaging configurations (a)Wired BGA, (b)Flip-chip BGA [4].

Flip chip bonding has been developed to address the issues associated with wire bonding, whereby the chip is positioned face-down on the substrate, as shown in the Figure 1.2(b). The superiority of flip-chip technology over the wire bonds lies in the reduction in package height as it does not acquire extra space for wire bonds, leading to closer and localized arrangements of functional blocks within their structure. Moreover, they do not suffer from parasitic inductance, which is quite significant in wire bonding technology at a high-frequency range.

Nowadays, engineers and researchers are bringing down the circuits beyond the limits of the physical dimensions. Recent advancements in electronic packaging technology, known as multi-chip packaging (MCP), integrate electronic systems by interconnecting

multiple integrated circuits (ICs) within a single packaging structure. MCP technology can be implemented either through multi-chip modules (MCMs) or through system-in-package (SiP). Chip stacking can be achieved by stacking single-chip packages, by stacking multiple chips within a single package, or by a combination of these approaches. In the MCM packaging technology, multiple electronic chips are stacked and connected using wire bonds or via flip chip onto a single substrate in a planar fashion, allowing the entire system to function as a unified device. This configuration results in more accessible neighbors and increased bandwidth, enhancing performance. Added advantage includes improved thermal capability since it can be used in conjunction with heat spreaders and heat sinks to increase heat dissipation from the chips.

1.2 Motivation

Power electronics systems consistently demand enhanced functionality within a reduced packaging volume while meeting the reliability requirements. These systems are characterized by elevated volumetric and gravimetric power density requirements, which, in turn, necessitates thermal management solutions to prevent critical junction temperature within circuits. Integrating multiple modules within a single package further makes heat dissipation more challenging owing to increased power requirements and the formation of hot spots due to heat entrapment, thereby making heat dissipation more challenging.

Mechanical failure poses a significant challenge to interconnection materials in electronic packages. Thermal or residual stresses that are induced within a package at elevated temperatures can lead to various types of failures in electronic devices, such as package cracks, die cracks, wire breakage, and delamination. The primary cause is the mismatch among the thermal properties of different components present in the package. The mismatch in the coefficient of thermal expansion (CTE) of the substrate and other

components causes distortion in the flip-chip assembly, inducing stresses at the corner edges of the solder joint. The local thermal expansion mismatch results in stress concentration at the corners of the solder bump. When such a distorted structure is subjected to fatigue or thermal cycling loads, it goes through differential expansion and contraction, leading to the failure of the interconnect, as shown in Figure 1.3.

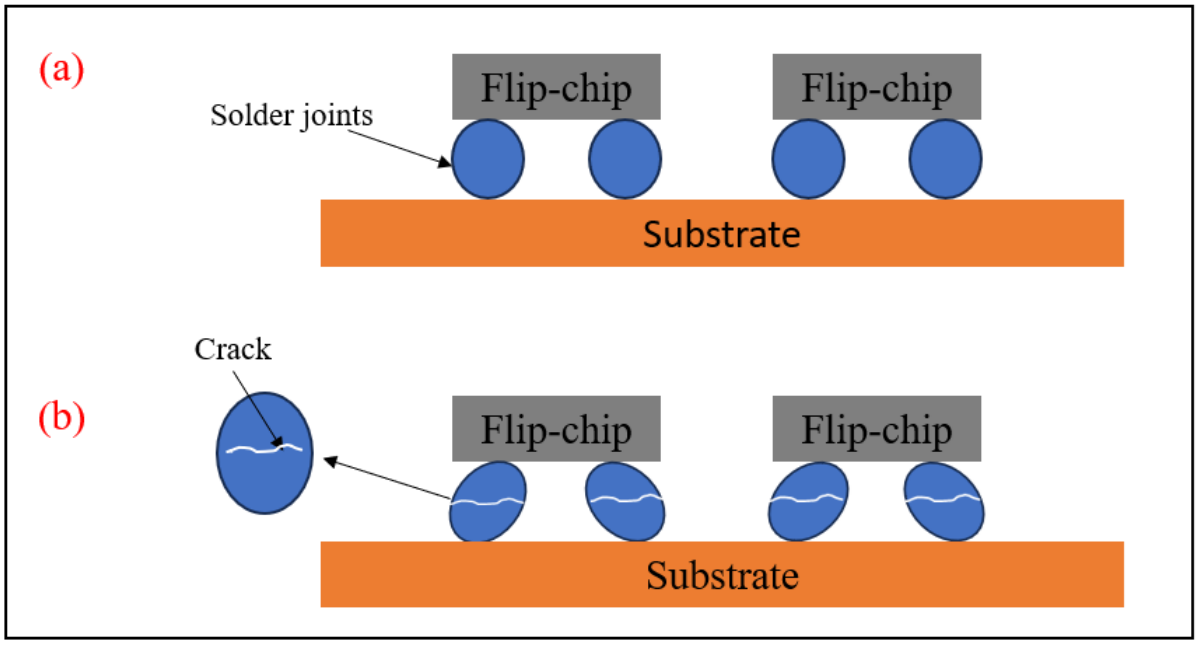


FIGURE 1.3: Effect of substrate-chip CTE mismatch on the failure of solders (a) at Room temperature, (b) at elevated temperature.

1.3 Aims and Objectives

The primary motivation for this study was to explore different configurations of conventional and Porous MCHS and understand their impact on the thermo-structural performance of an MCM-BGA Array model. The project aims to develop a novel configuration featuring maximizing heat transfer with low pumping power requirements. In this regard, the Nelder-Mead multi-objective optimization algorithm is utilized to optimize the geometrical parameters, which results in maximizing the heat transfer

coefficient (h_{mchs}). The aims of the project will be achieved by fulfilling the following objectives:

- Conducting a detailed literature survey to understand different cooling solutions employed for thermal management of electronics packaging using heat spreaders and heat sinks and identify the potential gaps in the research.
- Performing 3D numerical analysis using COMSOL Multiphysics to validate and assess the impact of fluid flow on the thermo-structural performance of the base model.
- Conducting a detailed examination of the various functional parameters of conventional and porous MCHS.
- Conducting a Nelder Mead optimization of porous MCHS to find the best set of the combination of geometric parameters to design a configuration with an optimal pumping power and heat transfer coefficient.
- Extending and applying the same physics to perform a thermo-structural analysis of the standard and optimized model to evaluate the thermal stresses and determine the fatigue life cycle of solders when chips are loaded periodically.

1.4 Thesis Organization

The thesis is overall divided into 5 chapters, including the present Chapter 1 of introduction to the research topic. This chapter describes the background, motivation, aims, objectives of the study and a brief thesis outline.

Following this introduction, Chapter 2 provides a detailed literature review that focuses on previous research work on thermal management of Electronics packaging, with a particular emphasis on conventional and porous MCHS.

Chapter 3 presents the governing differential equations that capture the fluid flow through a porous media and Anand's viscoplastic model to determine the fatigue life of the solders. For methodology, the chapter also provides an overview of the construction of CAD designs, meshing to setting boundary constraints to perform simulations utilizing commercial FEM software COMSOL Multiphysics.

Chapter 4 presents and discusses the results of conjugate heat transfer coupled with structural analysis. This chapter also includes a parametric analysis and optimization of the porous MCHS that will be incorporated into the standard model to enhance the fatigue life of the solders.

Chapter 5 summarizes the key findings and contributions to the field and provides recommendations for future work based on the study's results.

Chapter 2

Literature Review

2.1 Introduction

Micro-electro-mechanical systems (MEMS) have gathered considerable attention in scientific research and electronic applications in recent years as they serve as sensing layers in various domains of UAV, the Internet of Things, telecommunications, smartphones, vehicles, and medical equipment. The relentless miniaturization of the MEMS has led to the rapid development of the semiconductor industry and higher integration in packaging technology [5]. As outlined in the International Technology Roadmap for Semiconductors, the three-dimensional integration of MEMS and ASIC components has led to a shift from the traditional Moore's Law scaling due to a reduction in the size of transistors and chips [6]. The exponential growth in computing power nearly every 1.5-3 years has led to increasing the heat flux value from 100 W/cm^2 in traditional ICs to $10^3 - 10^4$ and beyond in VLSI devices [7–9]. This continuous growth in computing power and in the number of electronic components on semiconductor packages results in a significant enhancement in their overall performance. However, this enhancement also poses a substantial challenge to thermal management, which is crucial

for their proper functioning. Previous studies have shown that a 10 K rise in temperature can reduce the reliability of electronic devices up to 50% [10].

The microprocessors in modern-day high-powered devices, IGBTs, and laser diode arrays generally generate heat fluxes exceeding the value of $10^3 W/cm^2$.These abnormal heat fluxes, in turn, lead to excessive local temperatures at various critical positions in the IC package, such as wire bonds, die-substrate connections, bond pads, and vias [11]. Failure in timely heat dissipation from these local zones develops thermal stresses, leading to warpage and deformation among various package components, risking their life and reliability. Consequently, the thermal management of heat surges in microelectronics applications has become a critical aspect of 2.5-3D IC packaging.

Various cooling techniques have evolved over these years to enhance the heat transport rate associated with high-powered electronic devices; out of them most widely practiced are as follows:

- air cooling [12, 13]
- fluorochemical liquids-forced convection [14]
- fluorochemical liquid-boiling heat transfer [14]
- water-forced convection [15]
- water boiling cooling [16]
- jet impingement [17–20]
- microchannel cooling [21–24]
- spray cooling [25, 26]

The maximum heat flux dissipated by air-cooling and heat pipes is $100 W/cm^2$ and $200 W/cm^2$ approximately, indicating that these methods are insufficient for meeting

current and future needs in electronic packaging [27]. Jet impingement and spray cooling seem promising solutions for thermal management, as depicted in Figure 2.1 [28]. However, they require significant space and high pumping power to accelerate droplets, adding weight and complexity to already densely packaged designs and affecting the miniaturization of electronic devices.

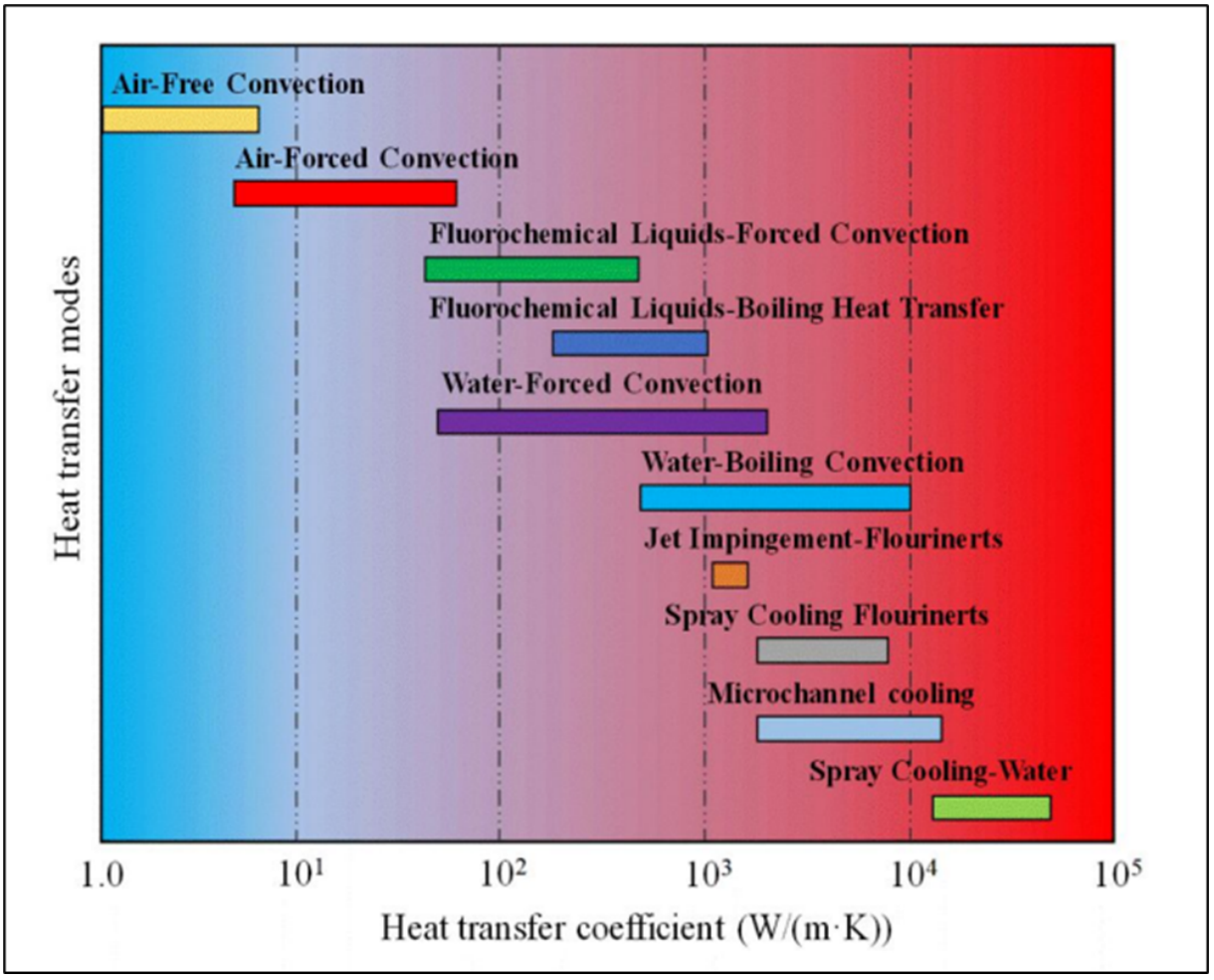


FIGURE 2.1: Comparison of cooling capacity of different cooling methods [28].

With rapidly developing micromachining technology, microchannel heat sinks (MCHS) have emerged as an effective solution for electronic heat dissipation, offering a multitude of advantages such as a large specific surface area, compact size, and coolant saving.

2.2 Background

Microchannel heat sinks have been extensively used for thermally managing microelectronics applications ever since they were first discovered by Tuckerman and Pease in 1981 [29], owing to their high convective heat transport coefficient and compact size. Since then, many researchers have been researching the utilization of microchannel structures in electronic packaging. Missaggia et al. pioneered the use of MCHS to enhance heat transfer on a 2D high powered density diode[30, 31]. Changing the coolant liquid and modifying the structure of the channel are effective ways to enhance the thermal performance of the MCHS [32–35]. Hassan et al. explored the effect of microfluidics cooling on the 3D stacked memory systems, and the chip's cooling was significantly improved as compared to conventional methods [36]. Brunschwiler et al. added the microchannel structure on the dual side of the chip and found that interlayer cooling is the effective way to deal with the number of chips in the stack to achieve compact 3D integration as the cooling performance improved by 2 folds [37, 38]. Bayraka et al.examined different geometric configurations for the microchannel and assessed their respective thermal-hydraulic performance [39]. Naphon et al. did experimental work investigating nanofluids directed on a microchannel heat sink using jet impingement, whereby they found that nanofluids with a 0.015 % concentration suspended in de-ionized water resulted in an 18.56 % increase in convective heat transfer [40]. Vajdiet al. examined the MCHS made out of a ZrB2 ceramic [41]. Lee et al.investigated cylindrical channels with variable pin pitch and conducted a topology optimization [42]. Xiao et al. used inclined parallelepiped ribs in the channels to alter the flow pattern and optimize thermal performance [43]. Awais and Man-Hoe Kim optimized the header geometry using nanofluids, resulting in a 17% rise in the overall heat transfer coefficient and a decrease of 43% in the pressure drop [44]. Wan et al. investigated the Nu number of different MPF shapes and found that the squared MPF geometry offers a higher Nu number than the circular shape [45]. The squared MPF

structures are widely used to counter the heat management issues encountered in compact-size applications [46, 47].

The cooling performance in power-electronic devices, can further be enhanced by incorporating metal foams in conventional MCHS. Chein et al. analyzed the water-cooled copper foam heat sink, plate-fin, and pin-fin heat sinks and concluded that copper foam heat sink offered superior thermal performance [48].In another work, Bayomy et al. investigated an aluminum foam heat sink with water as the coolant to cool the Intel core i7 processor [49]. Rachedi and Chikh investigated the effects of the Reynolds number, Darcy number, thermal conductivity and properties such as porosity and permeability for the foam materials. They found that the foam insertion reduces the temperature by 50 % compared to the fluid condition [50]. Fu et al.conducted an experimental study using the channel of aluminum metal foam. The local surface temperature was found to be a function of the dimensionless axial flow direction distance until it reached a near-constant value when the flow became fully developed thermally. [51]. De-ionized water is widely used as a coolant for conventional and porous MCHS as compared to dielectric fluids such as FC-72, HFE7000, and HFE7100, as its thermal conductivity is higher by ten times [52–55]. Various researchers conducted experimental studies using water-cooled sintered porous heat sinks for electronics cooling and observed a substantial rise in heat transfer, with a significant increase in pressure losses [56–58]. Leong et al. developed a heat sink with graphite foam and baffles, reducing the pressure drop while maintaining a good heat transfer capability [59]. Yang et al. demonstrated that a heat sink with the elliptic porous pin fin configuration enhances heat transfer and reduces pressure drop simultaneously [60]. Numerous researchers have investigated the combination of MCHS with straight and wavy porous fins with baffles of high thermal conductivity [61–67]. Hung et al. numerically studied different porous configurations and demonstrated that the sandwich configuration is the more effective design in terms of hydraulic and thermal performances [68]. The heat loading density in the above applications has been assumed to be uniform. For most

2.5D - 3D compact-sized ICs, heat fluxes are generally concentrated within confined hot spots, which often don't bear a constant value; transient studies are required to determine the unsteady cooling behavior [69, 70]. The use of MCHS and, in particular, Porous MCHS to reduce thermal stresses and increase the life cycle of solders in Microelectronic packaging has not been reported until now.

2.3 Research Gaps

The literature review reveals that conventional cooling methods involving natural and forced convection using air and water are inadequate in meeting the heat dissipation requirements of high-heat flux ICs. Currently, most of the research work embodying MCHS assumes heat loading to be a constant. On the contrary, this heat flux in the actual IC package is non-uniform due to the presence of regularly or unevenly distributed localized hotspots. This localised flux being excessively high poses a significant challenge to performance of the package.

Hence it is necessary to consider non-uniform loading density in order to mitigate the hotspots and address the reliability and life of the whole package. The active cooling methods, such as spray cooling and jet impingement, although extensively used in cooling devices, have a limited scope in the thermal management of microelectronic packaging owing to space constraints and complex arrangements. The passive cooling method integrating microchannel heat sinks with porous metal foam can be widely used in very large-scale integrated (VLSI) devices due to higher cooling capability and compact size.

Although the porous MCHS being superior to conventional MCHS in terms of heat transfer performance requires a high pumping power. In an ideal case, the porous MCHS should have higher heat transport at the lower pumping power. The optimization of geometric parameters to enhance the thermo-fluid performance of

MCHS, particularly in the thermal management of MCM-BGA array, has not been explored fully. Most of the current research work incorporating conventional and porous heat sinks solely investigates the thermal and hydraulic performance of MCHS without discussing structural integrity in detail

In addition, most of the current research efforts are invested in developing effective thermal management solutions for electronic devices operating under steady-state operations. However, real-life practical electronic applications, such as microcontrollers, IGBTs, and other high-powered electronic devices, hardly operate under steady-state conditions. The time-variant loading induces residual stresses and develops fatigue to the various parts inside the package, causing ultimate failure before expected. From the literature review, it has been found that the existing solutions for the thermal management of electronic devices are prominently designed for steady-state loading and are insufficient for the devices operating under transient loading. The present study explores the effect of heat spreaders and conventional and porous MCHS in increasing the fatigue life cycle of the MCM BGA array operating under transient loading.

Chapter 3

Design Methodology

3.1 Introduction

This chapter discusses in detail the underlying physics governing the heat and fluid transport, structural mechanics, and the methodology to develop the novel cooling solution by carrying out heat transfer and structural examination of the MCM-BGA array attached to the heat spreader and add-on conventional and porous MCHS. An engineering tool is designed to develop a 3D model and investigate the thermal and structural behavior of various package configurations with add-on devices such as heat spreaders, conventional MCHS, and porous MCHS.

The Engineering Tool consisted of three main stages:

1. Construction of the body to be tested
    - COMSOL Multiphysics modeling environment was used to develop a three-dimensional body from a given geometry to be tested.
2. Generation of a mesh around the domain

- A physics-defined/user-defined mesh is generated on the body's surface for analysis.
- The mesh is essential since the analysis is calculated on each mesh and integrated over the entire body.

3. Analyse the performance of the system

- Then the solver (Conjugate Heat transfer/ Solid Mechanics) is built on the nodes of the mesh to carry out calculations regarding the thermal performance and the other behavioral characteristics of the model

3.2 Design Principle

The CAD geometry inspired by the flip chip ball grid array contains symmetrically distributed nine chips attached to the substrate, with each chip joined by a 4x4 array of 5Sn- 95Pb solder balls; the bottom of the substrate layer is connected to the PCB in an array of 16x16 60Sn- 40Pb solders. Thermal interface material is applied between nine chips and the copper heat spreader, and MCHS has been placed on the heat spreader. Initially, a baseline microelectronic package comprising a PCB, solders, substrate, IC chips, TIM, and heat spreader was designed to conduct thermo-structural analysis utilizing the individual components. Subsequently, to develop a novel configuration that demonstrates optimal performance, an additional conventional and porous MCHS with varying porous arrangements were employed to design a total of four distinct assemblies.

Figures 3.1 and 3.2 present the schematics of all individual components and various porous configurations of the MCHS unit. Figure 3.3 represents the assembled configurations designated as follows: Baseline MCM-BGA package, MCM-BGA package with an add-on MCHS, MCM-BGA package with a horizontally placed porous MCHS, MCM-BGA package with a vertically placed porous MCHS, and MCM-BGA package with a MCHS

featuring all sides porous layout. The dimensions and materials used for each part of the MCM-BGA model are listed in Tables 3.1 and 3.2 [71]. Additionally, Table 3.3 contains the properties of materials for all components [71].

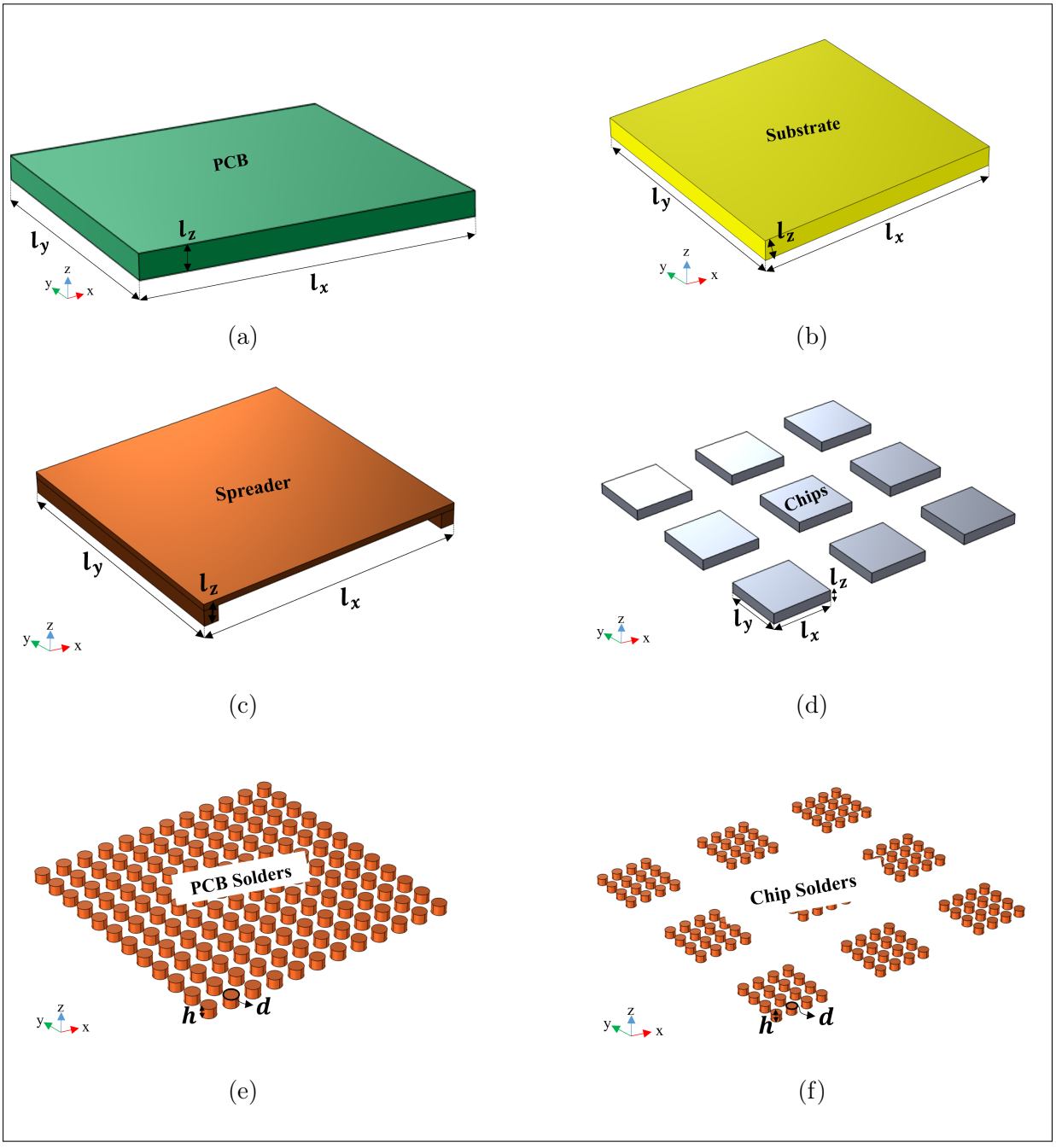


FIGURE 3.1: Schematic diagram of individual components (a) PCB, (b) substrate, (c) heat Spreader, (d) chips, (e) PCB solders and (f) chip solders.

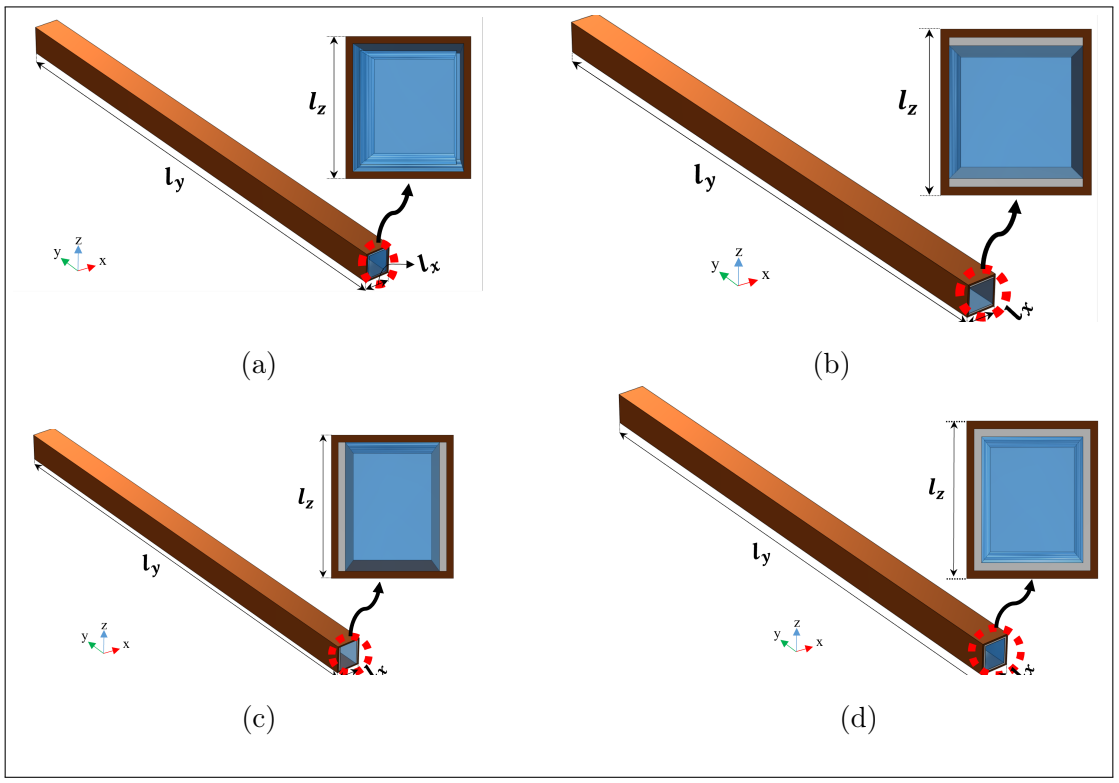


FIGURE 3.2: Schematic of different units of MCHS (a) conventional MCHS, (b) horizontally placed porous MCHS, (c) vertically placed porous MCHS, and (d) all-sided porous MCHS.

Components	**Length (mm)**	**Width (mm)**	**Height (mm)**	**Material**
PCB	20	20	1.2	FR4
Substrate	12.3	12.3	1	Polyimide
Heat spreader	12.3	12.3	1	Copper
Chips	2	2	0.35	Silicon
Thermal grease	2	2	0.15	Grease
MCHS	12.3	12.3	0.7	Copper
Components	**Diameter (mm)**	**Pitch (mm)**	**Height (mm)**	**Material**
Chip solders	0.3	0.5	0.2	5Sn/95Pb
PCB solders	0.6	1.5	0.4	60Sn/40Pb

TABLE 3.1: Dimensions and respective materials for components of MCM-BGA Array [71].

Porous Configurations	**Solid thickness (mm)**	**Porous thickness (mm)**	**Material**
All sided	0.035	0.035	Copper
Vertically placed	0.035	0.035	Copper
Horizontally placed	0.035	0.035	Copper

TABLE 3.2: Dimensions and material for different configurations of porous MCHS [71].

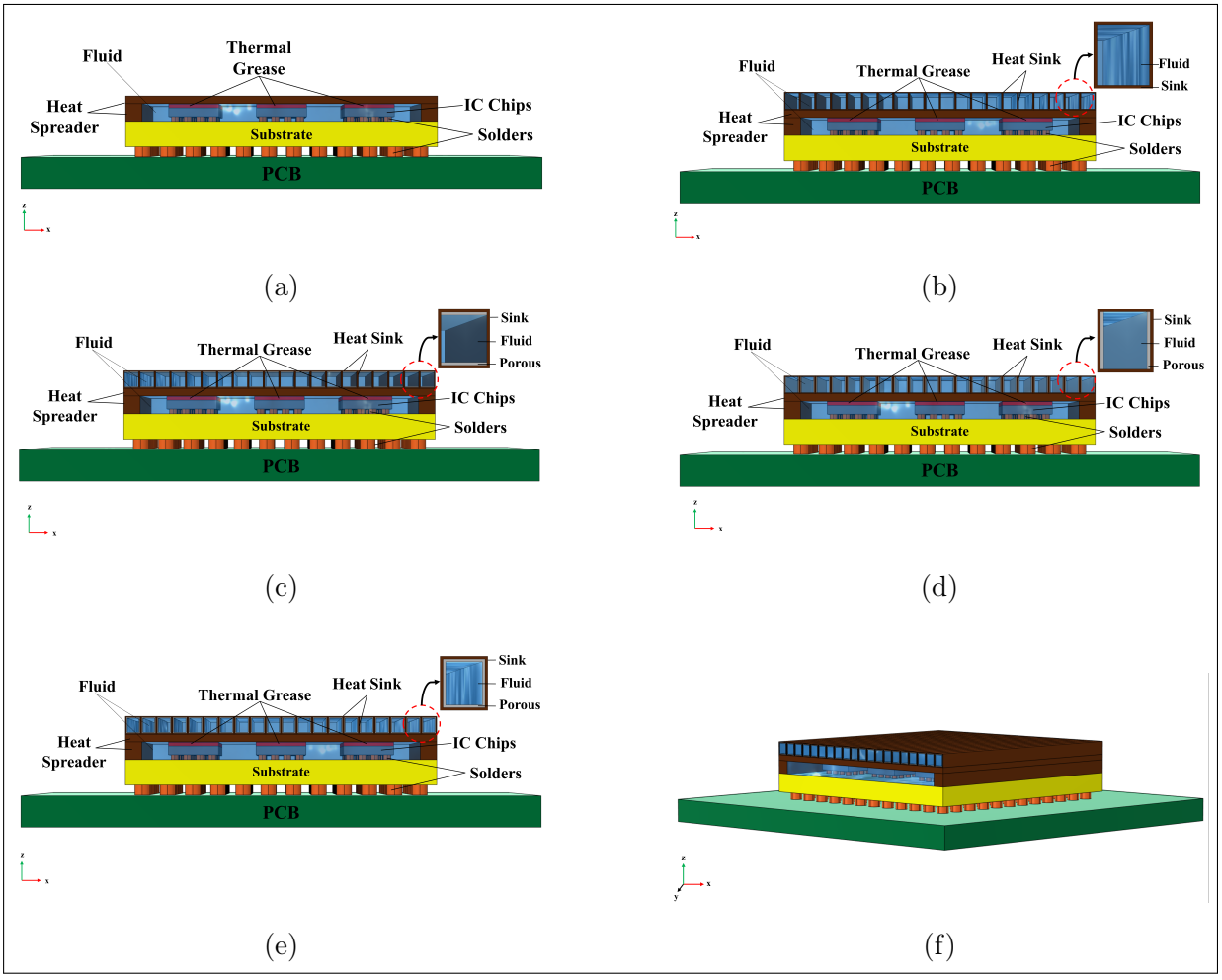


FIGURE 3.3: Schematic of complete MCM BGA package with an add-on (a) only heat spreader, (b) conventional MCHS, (c) horizontally placed porous MCHS, (d) vertically placed porous MCHS, (e) all-sided porous MCHS and (f) 3D isometric view.

Materials	**Thermal conductivity (W/mK)**	**Poisson's ratio**	**Young's Modulus (Pa)**	**Coefficient of thermal expansion (K^{-1})**
FR4	0.3	0.15	$2.2 * 10^10$	$1.8E-05$
60Sn/40Pb	50	0.4	1E 10	$2.1E-05$
Polyimide	0.2	0.35	$3.2E09$	$7E-05$
5Sn/95Pb	36	0.4	$2.6E10$	$1.9E-05$
Silicon	150	0.28	$1.7E11$	$2.6E-06$
Grease	10	0.4	$3.1E09$	$6.5E-06$
Copper	390	0.35	$1.1E11$	$1.7E-05$

TABLE 3.3: Material properties of the MCM BGA Array [71].

3.3 Mathematical Model for stationary loading

A three-dimensional fluid-solid conjugate model coupled with a Solid mechanics module is employed to analyze the velocity, temperature, and thermal stress profiles of an MCM module equipped with both conventional and porous MCHS, respectively.

The following assumptions are incorporated into the numerical model:

- The flow is single-phase, steady, incompressible, and laminar.
- Properties of the coolant and ribs are considered constant.
- Gravity effects and thermal contact resistance between the bottom wall and electronic equipment are neglected.
- Porosity in porous ribs is assumed to be homogeneous and isotropic.
- Local thermal equilibrium is presumed to be achieved between the solid and liquid phases inside the porous ribs.

3.3.1 Flow and heat transfer governing equations

The governing equations applicable for the conventional MCHS and the channels of porous MCHS are as follows:

$$\nabla.\left(\rho_f \vec{V}\right) = 0 \tag{3.1}$$

$$\left(\rho_f \vec{V}.\nabla\right)\vec{V} = -\nabla P + \mu_f \nabla^2 \vec{V} \tag{3.2}$$

$$\rho_f c_f \left(\vec{V}.\nabla T\right) = k_f \nabla^2 T \tag{3.3}$$

Brinkman-Forchheimer's formulation is used to model the fluid flow through porous domains of porous MCHS. The following equations are used to model the physics through porous domains:

$$\nabla . \left(\varepsilon \rho_f \vec{V} \right) = 0 \tag{3.4}$$

$$\frac{\rho_f}{\varepsilon^2} \left(\vec{V} . \nabla \right) \vec{V} = -\nabla P - \left(\frac{\mu_f}{K_p} + \frac{\rho_f C}{\sqrt{K_p}} \left| \vec{V} \right| \right) \vec{V} + \frac{\mu_f}{\varepsilon} \nabla^2 \vec{V} \tag{3.5}$$

$$(\rho c)_e \left(\vec{V} . \nabla T \right) = k_e \nabla^2 T \tag{3.6}$$

Where ϵ is the porosity of the porous domain, ρ_f is the density of fluid, $\vec{V}$is the velocity vector of fluid, P is the pressure, K_p is permeability, C is the Forchheimer's constant, μ_f is the fluid viscosity, and T is the temperature.

$$k_e = \varepsilon \; k_f + (1 - \varepsilon) \, k_s \tag{3.7}$$

$$(\rho c)_e = \varepsilon \rho_f c_f + (1 - \varepsilon) \, \rho_s c_s \tag{3.8}$$

k_e and $(\rho c)_e$ are the effective thermal conductivity and effective volumetric heat capacity, respectively, where f and s indicate fluid and solid.

3.3.2 Thermal stress equations

The equations of thermal stresses and thermal strains due to temperature differences between various functional components of the model are as follows:

$$\varepsilon_x - \varepsilon_0 = \frac{\sigma_x}{E} - \frac{\nu}{E}(\sigma_y + \sigma_z) \tag{3.9}$$

$$\varepsilon_y - \varepsilon_0 = \frac{\sigma_y}{E} - \frac{\nu}{E}(\sigma_z + \sigma_x) \tag{3.10}$$

$$\varepsilon_z - \varepsilon_0 = \frac{\sigma_z}{E} - \frac{\nu}{E}(\sigma_x + \sigma_y) \tag{3.11}$$

where ν is Poisson's ratio, E is Young's modulus, σ, and ε are the thermal stress and thermal strain, respectively. The influence of material expansion on the thermal strains is expressed as:

$$\varepsilon_0 = \alpha \Delta T \tag{3.12}$$

where α is the linear expansion coefficient.

3.3.3 Boundary conditions

The boundary conditions of the entire BGA package are depicted in the Figure and are listed as follows:

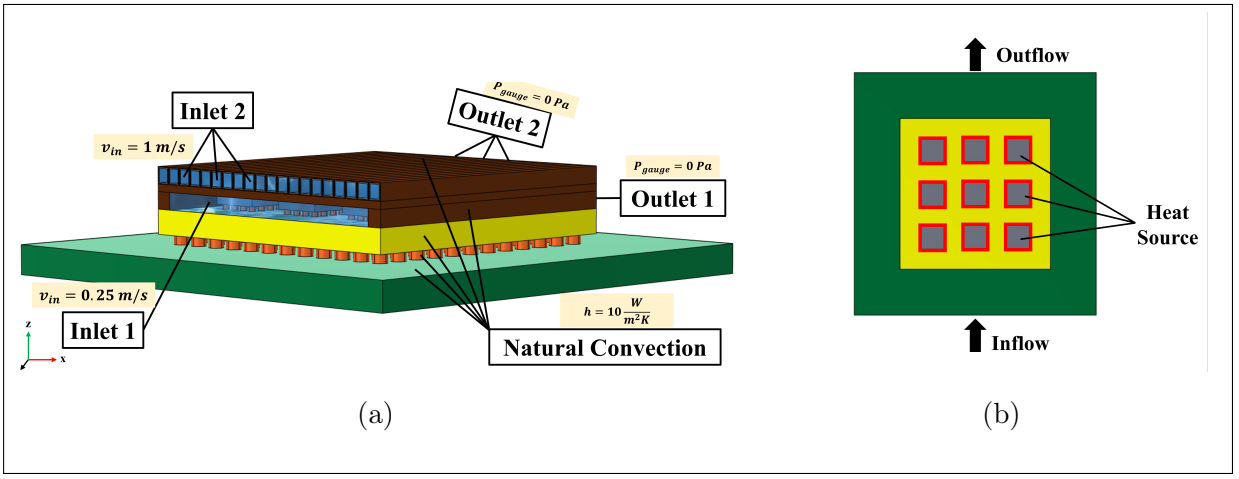


FIGURE 3.4: Boundary conditions for Conjugate heat transfer analysis of the BGA package: (a) 3D isometric view showing thermal and fluid boundaries, (b) Top view indicating inlet, outlet, and heat source boundary conditions.

For the analysis of the model with add-on conventional and porous MCHS, Conjugate Heat Transfer is used where the chips are emanating heat at 120W, with water flowing through the mid-channel and MCHS with an inlet velocity equal to 1m/s and T = 300K. The outlet of both MCHS and mid-channel is assigned 0 pressure. The bottom of the chips and the top of the substrate are fixed, and the bottom surface of the PCB is fully constrained for thermo-mechanical modelling.

The detailed boundary conditions for the modeling of porous MCHS are as follows:

1. At inlet of MCHS (y=0):

$$v = v_{\text{in}}, \quad T = T_{\text{in}}, \quad u = w = 0$$

2. At base of MCHS (z=0):

$$q = q_w$$

3. At outlet of MCHS (y=L):

$$\frac{\partial T_f}{\partial y} = 0, \frac{\partial u}{\partial x} = \frac{\partial v}{\partial y} = \frac{\partial w}{\partial z} = 0$$

4. At left and right wall of MCHS (x=0, x=width):

$$\frac{\partial T_s}{\partial x} = 0$$

5. At interface of porous and solid fins

$$-k_{\text{eff}} \frac{\partial T_p}{\partial n} = -k_s \frac{\partial T_s}{\partial n}, \quad T_s = T_p, \quad u = v = w = 0$$

6. At interface of fluid and porous

$$q|_f = q|_p, \quad u|_f = u|_p, \quad \mu_f \frac{\partial v}{\partial n}|_f = \frac{\mu_f}{\varepsilon} \frac{\partial v}{\partial n}|_p$$

7. At other outside walls

$$-k_s \frac{\partial T_s}{\partial n} = h\Delta T$$

3.3.4 Performance parameters

The thermal and hydraulic performance of the conventional and porous microchannel heat sinks are evaluated by examining various parameters as follows:

- Friction factor

$$f = \frac{1}{2}\frac{D_h}{L_y}\frac{\Delta p}{\rho_f v_{in}^2} \tag{3.13}$$

- Reynolds no.

$$Re = \frac{\rho_f v_{in} D_h}{\mu_f} \tag{3.14}$$

- Average heat transfer coefficient

$$h_m = \frac{q_w}{(T_{w,m} - T_{f,m})} \tag{3.15}$$

- Nusselt no.

$$Nu_m = \frac{h_m D_h}{k_f} \tag{3.16}$$

- Thermal resistance

$$R_T = \frac{T_{\max} - T_{\text{in}}}{q_w A_w} \tag{3.17}$$

- Pumping power

$$\Omega = v_{in} l_f w_f \Delta p \tag{3.18}$$

- Figure of merit

$$FM = \frac{\left(\frac{h_{\text{m,new}}}{h_{\text{m,base}}}\right)}{\left(\frac{\Omega_{\text{m,new}}}{\Omega_{\text{m,base}}}\right)^{(1/3)}} \tag{3.19}$$

where D_h is the hydraulic diameter of the channel, $D_h = 4l_f * w_f/2(l_f + w_f)$, T_{max} is the maximum temperature of the heat sink, A_w is the area of the heated wall, $T_{(w,m)}$ and

$T_{(f,m)}$ are the average wall temperature and the volume average temperature of the fluid, respectively.

3.4 Mathematical Model for transient loading

3.4.1 Flow and heat transfer governing equations

The assumptions incorporated into the model would be the same, except that the heat transfer and flow phenomena would become transient. The governing equations applicable for the conventional MCHS and the channels of porous MCHS are as follows:

$$\frac{\partial \rho_f}{\partial t} + \nabla . \left(\rho_f \vec{V} \right) = 0 \tag{3.20}$$

$$\frac{\partial \rho_f \vec{V}}{\partial t} + \left(\rho_f \vec{V} . \nabla \right) \vec{V} = -\nabla P + \mu_f \nabla^2 \vec{V} \tag{3.21}$$

$$\rho_f c_f \frac{\partial T}{\partial t} + \rho_f c_f \left(\vec{V} . \nabla T \right) = \ k_f \nabla^2 T \tag{3.22}$$

The following equations are applicable through porous domains:

$$\nabla . \left(\varepsilon \rho_f \vec{V} \right) = 0 \tag{3.23}$$

$$\frac{\rho_f}{\varepsilon^2} \left(\vec{V} . \nabla \right) \vec{V} = -\nabla P - \left(\frac{\mu_f}{K_p} + \frac{\rho_f C}{\sqrt{K_p}} \left| \vec{V} \right| \right) \vec{V} + \frac{\mu_f}{\varepsilon} \nabla^2 \vec{V} \tag{3.24}$$

$$(\rho c)_e \frac{\partial T}{\partial t} + (\rho c)_e \left(\vec{V} . \nabla T \right) = \ k_e \nabla^2 T \tag{3.25}$$

3.4.2 Thermal stress equations

All of the package components except chip solders are assumed to be linear elastic material and have the same governing equations as mentioned in the stationary loading case. For modeling the viscoplastic chip-solders Anand Viscoplasticity model has been incorporated [72].

The constitutive model is based on a scalar internal variable 's' that represents the resistance of material to plastic deformation. The Anand model collectively describes both the rate-independent plastic behavior and the creep behavior of the material through the three fundamental equations:

1. Stress equation

$$\sigma = \frac{s}{\xi} \sinh^{-1}\left(\frac{\dot{\varepsilon_p}}{A} \exp\left(\frac{Q}{RT}\right)\right)^m \tag{3.26}$$

2. Flow equation

$$\dot{\varepsilon_p} = A \exp\left(-\frac{Q}{RT}\right) \sinh\left(\frac{\xi\sigma}{s}\right)^{1/m} \tag{3.27}$$

3. Evolution equation.

$$\begin{aligned} s =& \hat{s}\left(\frac{\dot{\varepsilon_p}}{A} \exp\left(\frac{Q}{RT}\right)\right)^n \\ &- \left(\left(\hat{s}\left(\frac{\dot{\varepsilon_p}}{A} \exp\left(\frac{Q}{RT}\right)\right)^n - s_0\right)^{(1-a)}\right. \\ &\left. + (a-1)\left(\left((h_0)\left(\frac{\dot{\varepsilon_p}}{A} \exp\left(\frac{Q}{RT}\right)\right)^n\right)^{-a}\right)\varepsilon_p\right)^{\frac{1}{(1-a)}} \end{aligned} \tag{3.28}$$

where $\dot{\varepsilon}$ is the plastic strain rate, A is the pre-exponential factor, ξ is the multiplier of stress, m is the strain rate sensitivity, Q is the activation energy, R is the universal gas constant, T is the absolute temperature, h_0 is the hardening constant; a is the strain

rate sensitivity of hardening, $\hat{s}$ is the coefficient, and n is strain rate sensitivity for the saturation value of deformation resistance.

The value of all the nine parameters (A, ξ, Q/R, m, h_0, a, s_0, $\hat{s}$ *and* n) for the chip solders for implementing Anand's viscoplasticity model has been taken from [73].

3.4.3 Fatigue Life cycle analysis

There are numerous models used to predict the fatigue failure. In the present study, the Darveaux model and Coffin-Manson model have been used to evaluate the solder fatigue life of the BGA package equipped with conventional and porous MCHS. The mathematical expressions for the energy-based Darveaux model are as follows:

- Thermal cycle to crack initiation:

$$N_0 = K_1 \left(\Delta W_{ave}\right)^{K_2} \tag{3.29}$$

- Rate of crack propagation per thermal cycle

$$\frac{da}{dN} = K_3 \left(\Delta W_{ave}\right)^{K_4} \tag{3.30}$$

- Fatigue life

$$N_f = N_0 + \frac{a}{da/dN} \tag{3.31}$$

where N_f is cycles to failure, N_0 is cycles to crack initiation, ΔW average viscoplastic energy density dissipated/cycle, a is the final crack size, da/dN is the crack growth rate, and $K1, K2, K3, K4$ are material constants.

The expression for the strain life-based Coffin-Manson model is as follows:

$$N_f = \frac{1}{2}\left|\frac{\Delta\varepsilon_p}{2\varepsilon'_f}\right|^{\frac{1}{c}} \tag{3.32}$$

where N_f is cycles to failure, $\Delta\varepsilon_p$ is the plastic strain amplitude, ε_p is the effective plastic strain (obtained from FEA results), c is fatigue ductility exponent, and ε'_f is fatigue ductility coefficient.

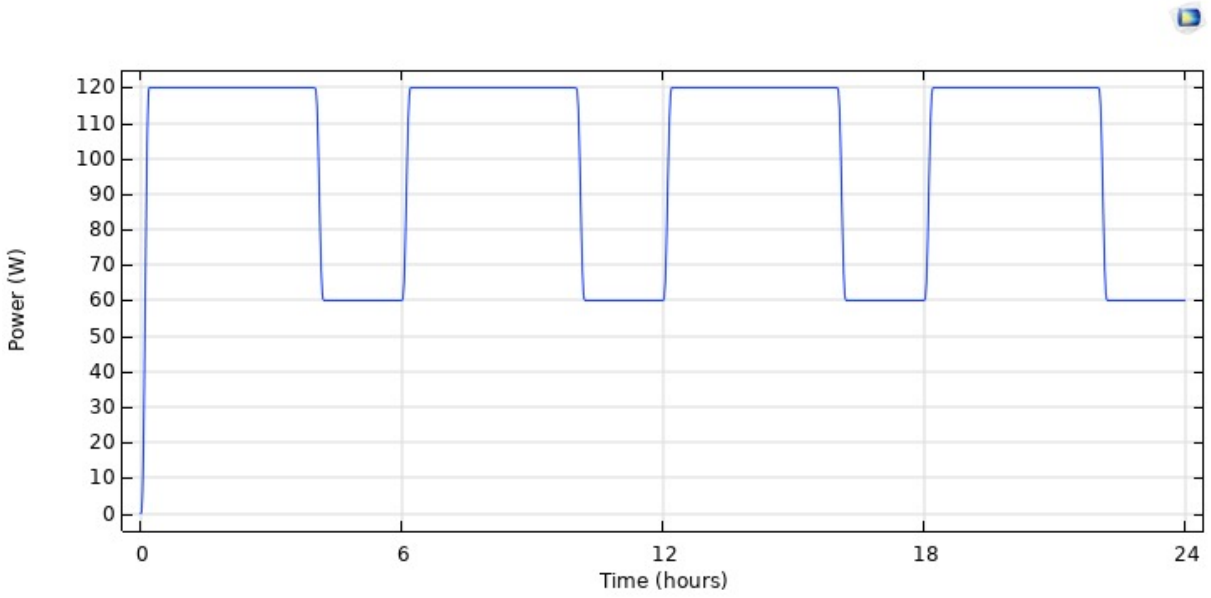


FIGURE 3.5: Power loading curve.

3.4.4 Boundary conditions

The similar boundary constraints applied for stationary loading are utilized for the transient case, with a notable difference in transient load density, modeled as the thermal power cycle shown in Figure 3.5. It is visible that a single cycle includes the following phases: the power ramps up from 0 to 120W upon activation, maintains a high power level of 120W for 4 hours in high-power mode, then drops from 120W to 60W, and finally, operates at a reduced power of 60W for 2 hours. This sequence is then repeated for four cycles.

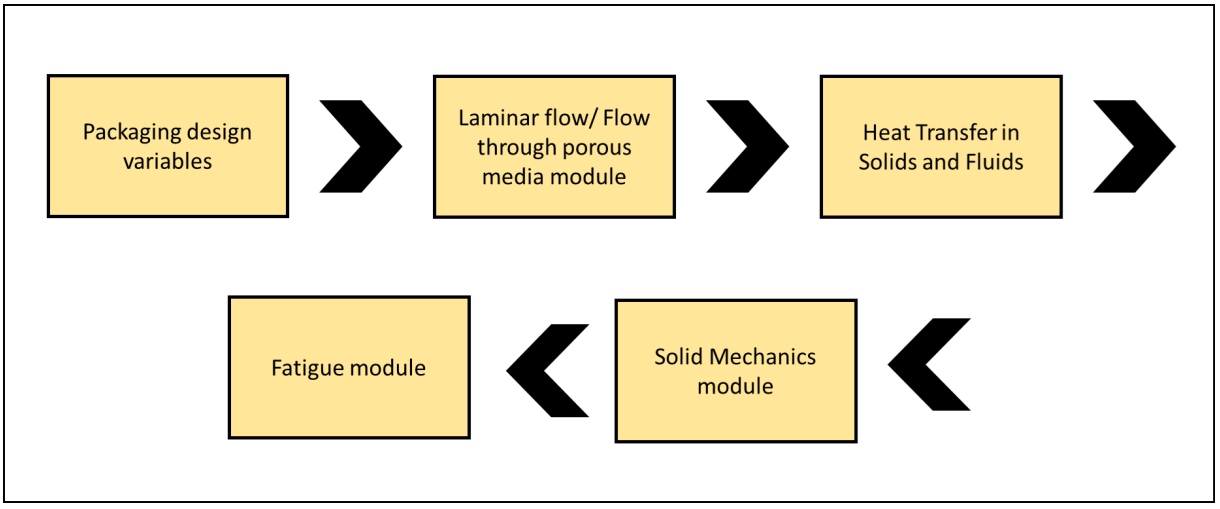


FIGURE 3.6: Workflow of the conducted study.

The workflow to carry out transient FEA analysis to study flow behavior and thermo-structural integrity is depicted in the Figure 3.6

Chapter 4

Results and Analysis

4.1 Introduction

This chapter discusses the outcomes of various simulations for different MCM-BGA array setups. To ensure the accuracy and reliability of the simulations, an initial study of grid independence was conducted on the MCM-BGA package featuring a conventional MCHS.

Prior to initiating simulations on our developed MCM-BGA package models, we opted to validate our formulated algorithm for conjugate heat transfer phenomena using a comparable MCHS study by Gong et al. [71]. This was done by applying the same coolant flow and boundary conditions. The temperature distribution across the mid-channel on the bottom surface of the chips, as observed along the centerline, is depicted in Figure 4.1. The outcomes of our simulations, generated through the algorithm, demonstrated a close match with the computational findings, showcasing a maximum deviation of 3.57%.

Five meshes with total elements between 759160 and 35994876 were simulated to check the numerical grid dependency test results. The relative error between the finest grid's

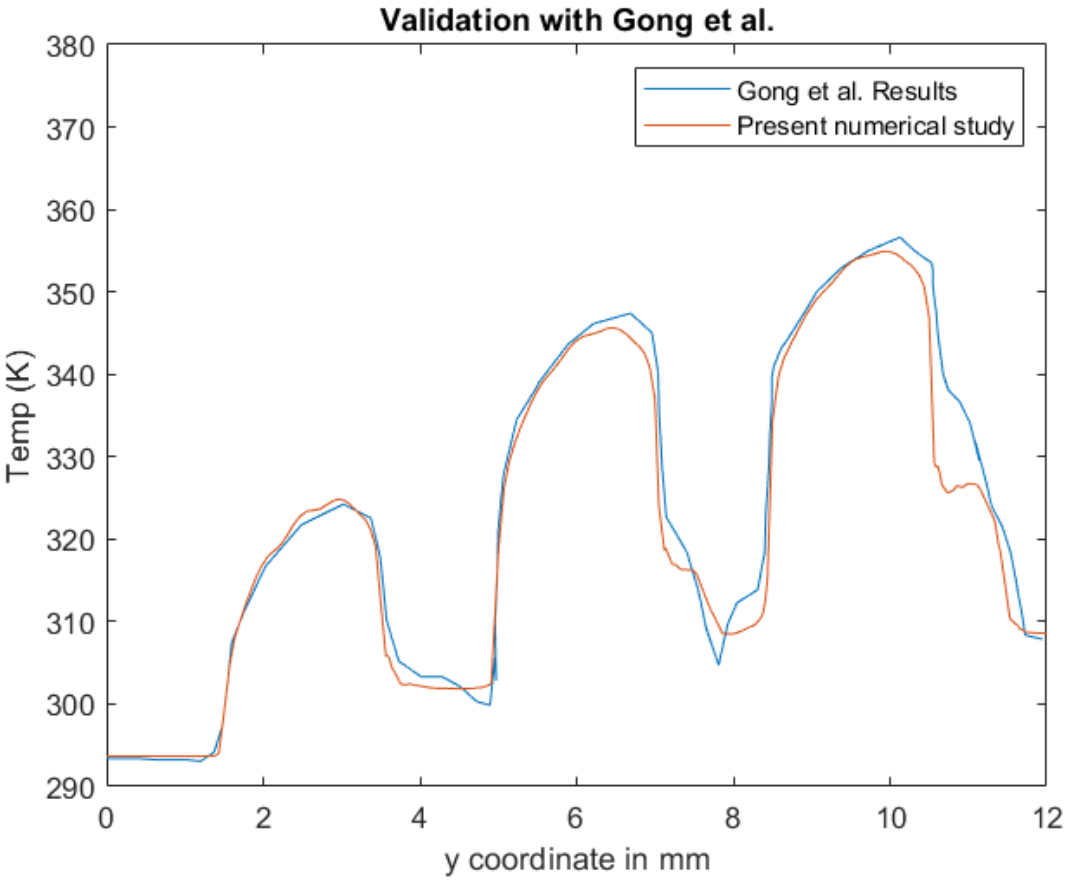


FIGURE 4.1: Validation of Simulation Results with Gong et al.

maximum temperature (T) and other grids (Ti) can be written as:

$$e\% = \left| \frac{T_i - T}{T} \right| * 100 \tag{4.1}$$

Total Mesh Elements	**Maximum Temperature (K)**	**% error**
759160	351.67	3.83
2779979	357.80	2.12
9704321	360.31	1.46
34495629	364.38	0.35
35994876	365.67	-

TABLE 4.1: Grid independence study.

Table 4.1 shows that the maximum temperature value after the grid with 34495629 elements is almost the same, with an absolute error not exceeding 0.35%. However, the grid with 759160 elements was adopted in this study to reduce computational time.

Following that, the remaining scenarios were analyzed using the standard mesh settings to effectively balance computational time with accuracy and efficiency. The findings are presented in the following manner: the initial evaluation compares the thermal and structural attributes of the Baseline MCM-BGA package to those with an added MCHS, setting a foundation for additional scrutiny. The next phase of the study delves into a thermo-structural examination of the MCM-BGA array employing traditional MCHS and various porous MCHS designs, aiming to assess their effects on heat dissipation and fluid flow. A particular focus is given to the fifth scenario, which was subjected to multi-objective optimization to both improve the heat transfer coefficient and reduce the required pumping power, yielding an ideally configured design. Lastly, a fatigue analysis was conducted on all the designed models to evaluate the system's long-term durability under the effects of transient thermal stresses.

4.2 Comparative Analysis of Baseline MCM-BGA Package and MCM-BGA with Conventional MCHS

The section provides a detailed comparison of the standard MCM-BGA package, which includes only a heat spreader, against the MCM-BGA package augmented with a conventional MCHS. The primary objective of this comparison is to assess the differences in temperature distribution and thermal stresses experienced by the MCM-BGA package when subjected to steady-state loading density conditions.

Considering the fluid flow through the mid-channel between the heat spreader and the substrate is confined, and there are no geometry and flow conditions changes, the velocity profile is consistent throughout. Figure 4.2 shows the velocity flow pattern along the middle channel of the package.

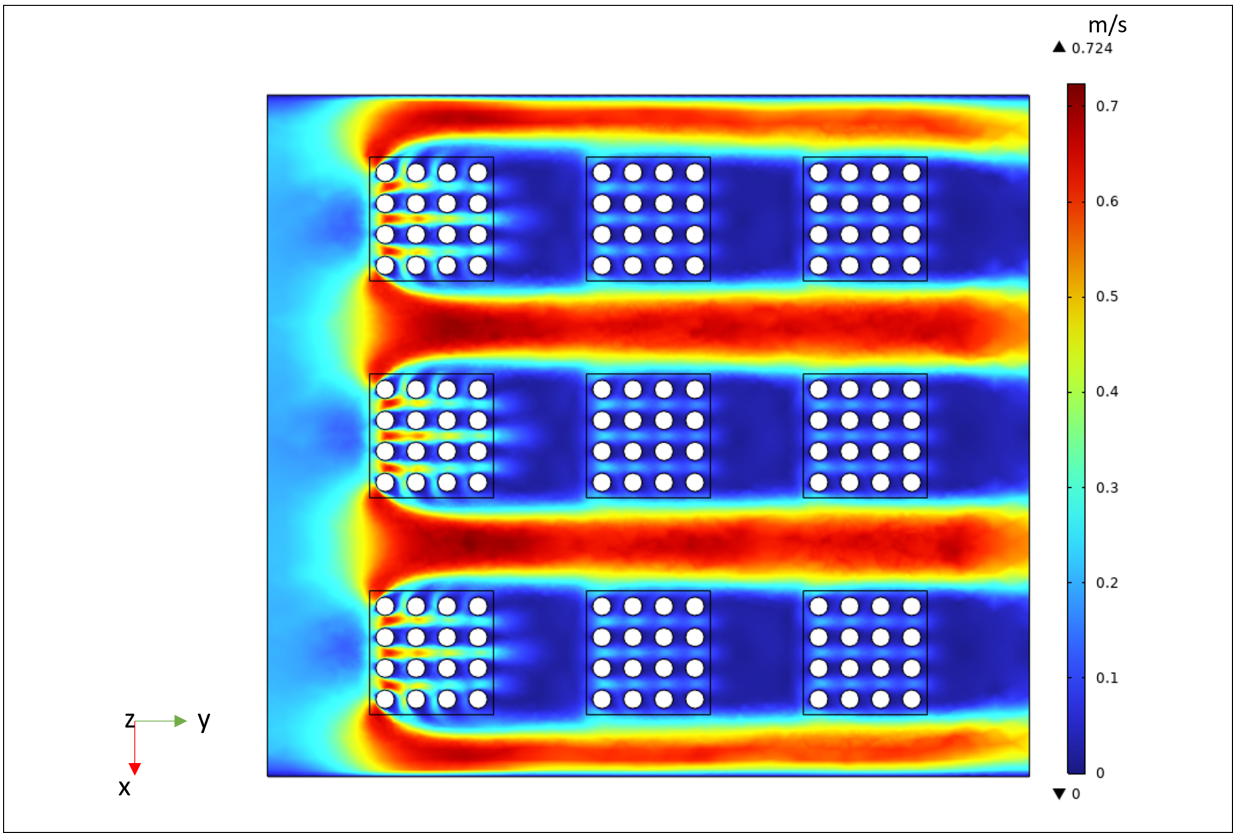


FIGURE 4.2: Velocity contour along the mid-channel between the substrate and the heat spreader.

The velocity stays high between chips along the flow direction. The velocity of fluid remains high over a clear passage between chips along the flow direction; however, it reduces significantly between the solder balls, resulting in a non-uniform flow pattern. The flow velocity between the chip solders is remarkably reduced between the last two rows of chips, which affects the heat transport rate along the flow direction. Near the inlet, the solder balls experience greater speeds owing to the influence of the in-flowing fluid. The velocity significantly reduces amongst the solder balls located in the final two rows of chips. The velocity nearly reaches zero in regions perpendicular to the direction of flow.

Three sections were taken to visualize heat dissipation from the IC chips along the flow direction. These sectional areas are outlined by cross-sections taken at $y = -2.75$ mm, $y = 0.75$ mm, and $y = 4.25$ mm, intersecting the final row of chip solders, see Figure 4.3.

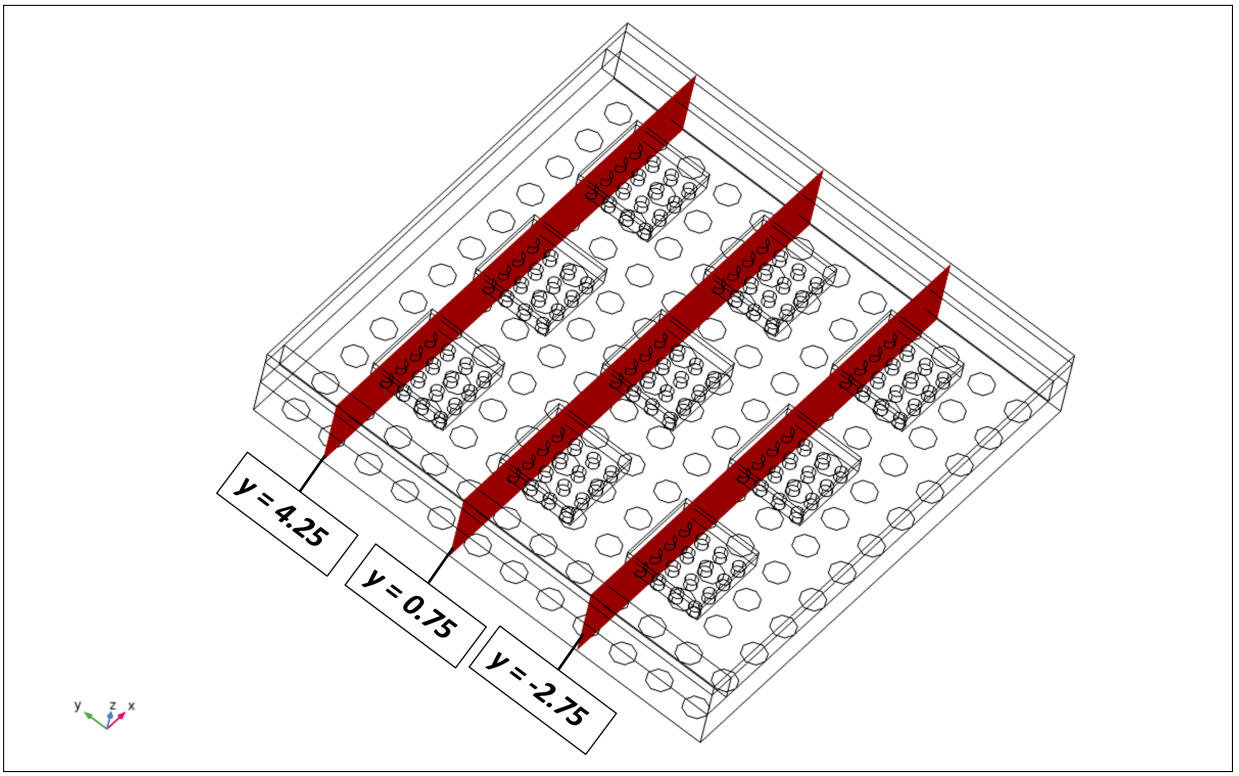


FIGURE 4.3: Velocity contour along the mid-channel between the substrate and the heat spreader.

Figures 4.4(a) and 4.4(b) exhibit the temperature profiles within these planes for both baseline and conventional MCHS-equipped MCM BGA packages. Across most areas, temperatures remain low and evenly spread, with notable increases around the chips and their immediate vicinity. The temperature variation across the chip rows is pronounced along the flow direction, attributed to the velocity distribution in the center. Chip temperatures stay uniformly low near the inlet. However, the highest temperature is observed near the outlet plane, where temperature gradients are approximately $1.2242E + 06$ K/m for the standard package and $6.8582E + 05$ K/m for the MCHS-enhanced package. Figure 4.8 presents this temperature variation plotted along a centerline passing along the flow direction at the bottom surface of the IC chips. It is visible from the graph that the temperature gradually increases along the flow direction, with peaks observed indicating the hotspot's position and dips indicating empty areas between chips filled with coolant. A constant pattern of a sharp temperature rise

followed by a gradual decline from the inlet to the outlet increases the coolant's overall temperature, thereby reducing heat transfer efficiency.

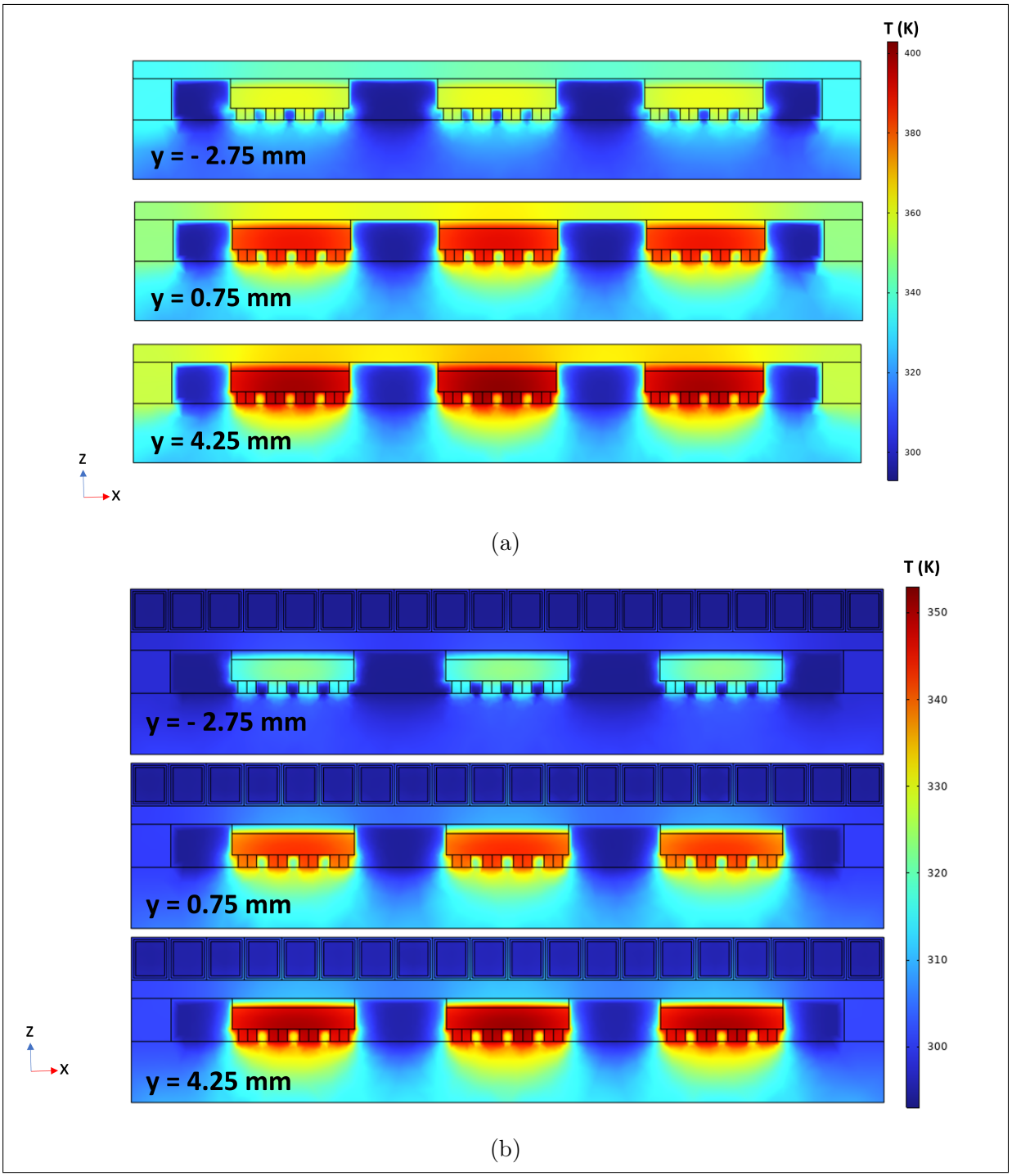


FIGURE 4.4: Temperature variations across different cross-sectional planes of the IC chips for (a) the Baseline MCM-BGA package and (b) the conventional MCHS equipped MCM-BGA package.

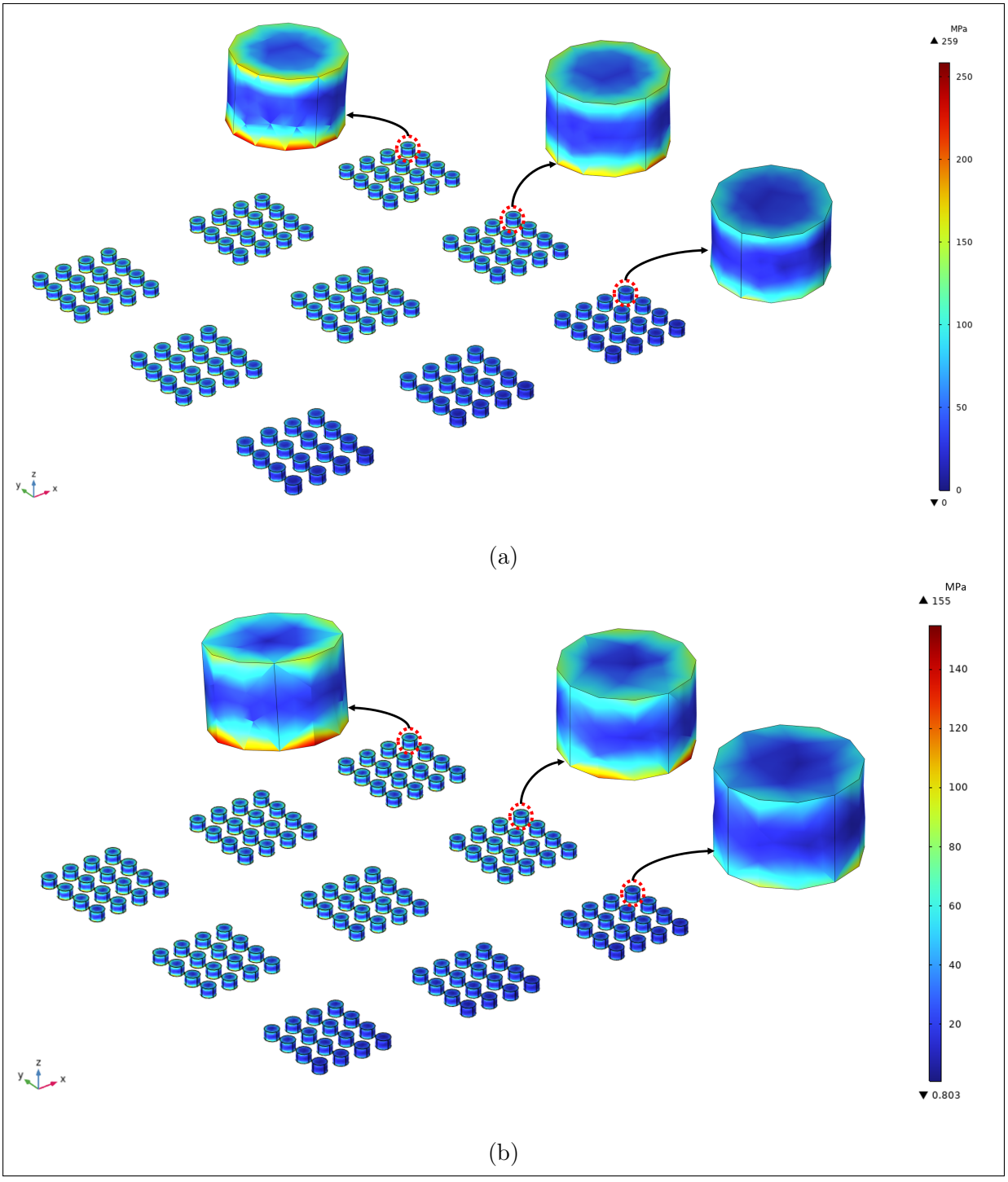


FIGURE 4.5: Thermal stress contours of chip solders for (a) the Baseline MCM-BGA package and (b) the conventional MCHS equipped MCM-BGA package.

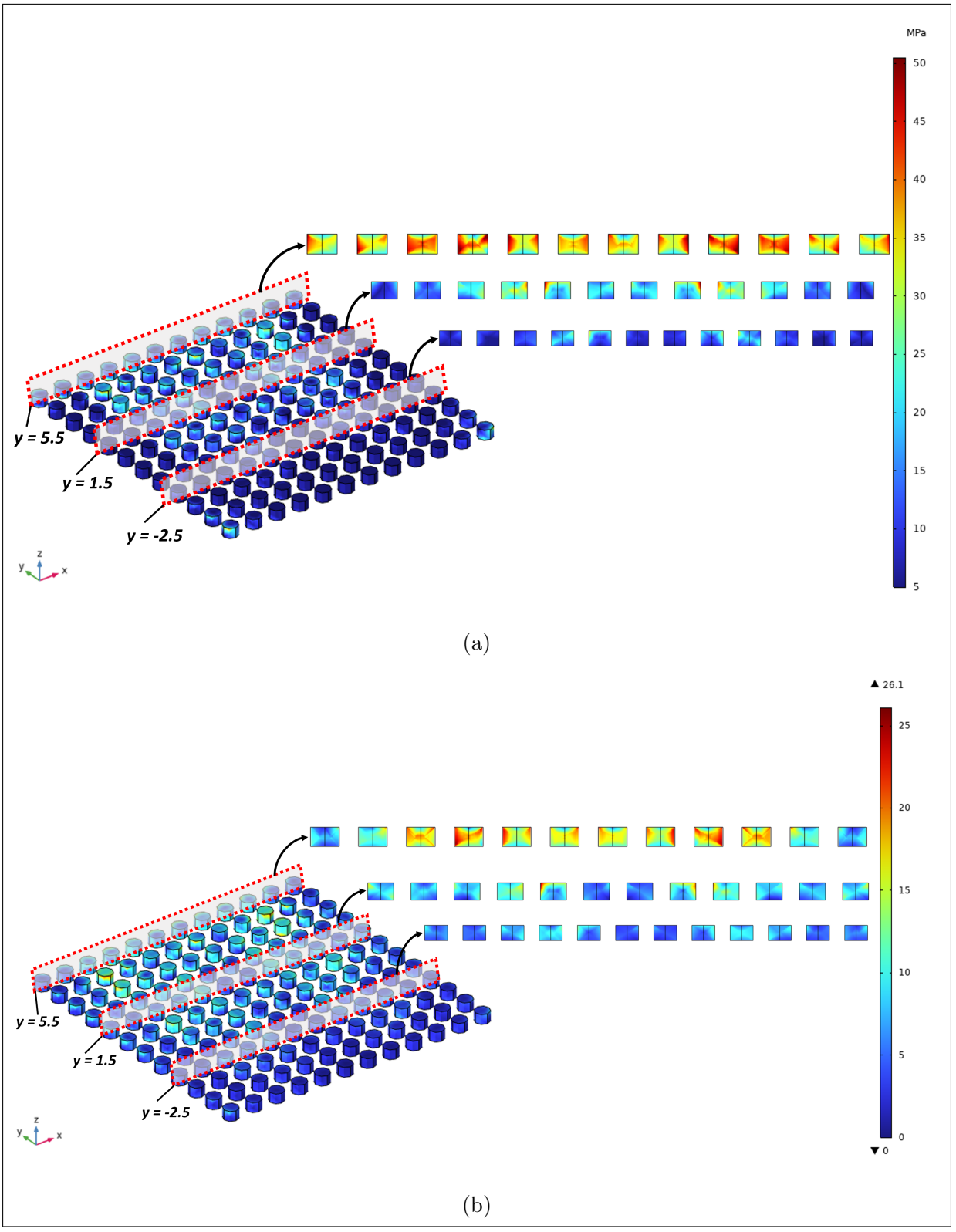


FIGURE 4.6: Thermal stress contours of PCB solders across different cross-sectional planes for (a) the Baseline MCM-BGA package and (b) the conventional MCHS equipped MCM-BGA package.

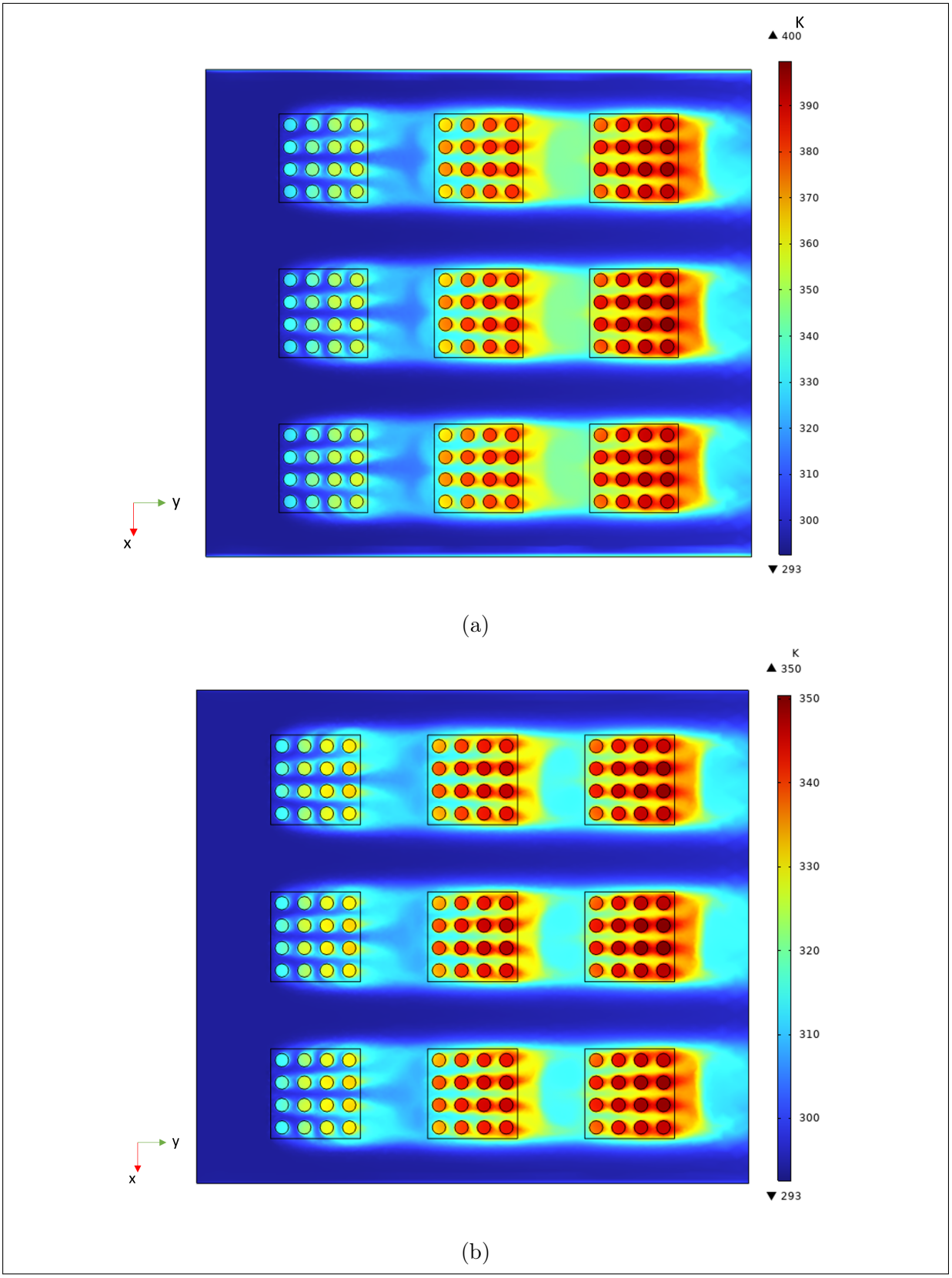


FIGURE 4.7: Temperature variations across an interface between substrate and chip solders for (a) the Baseline MCM-BGA package and (b) the conventional MCHS quipped MCM-BGA package.

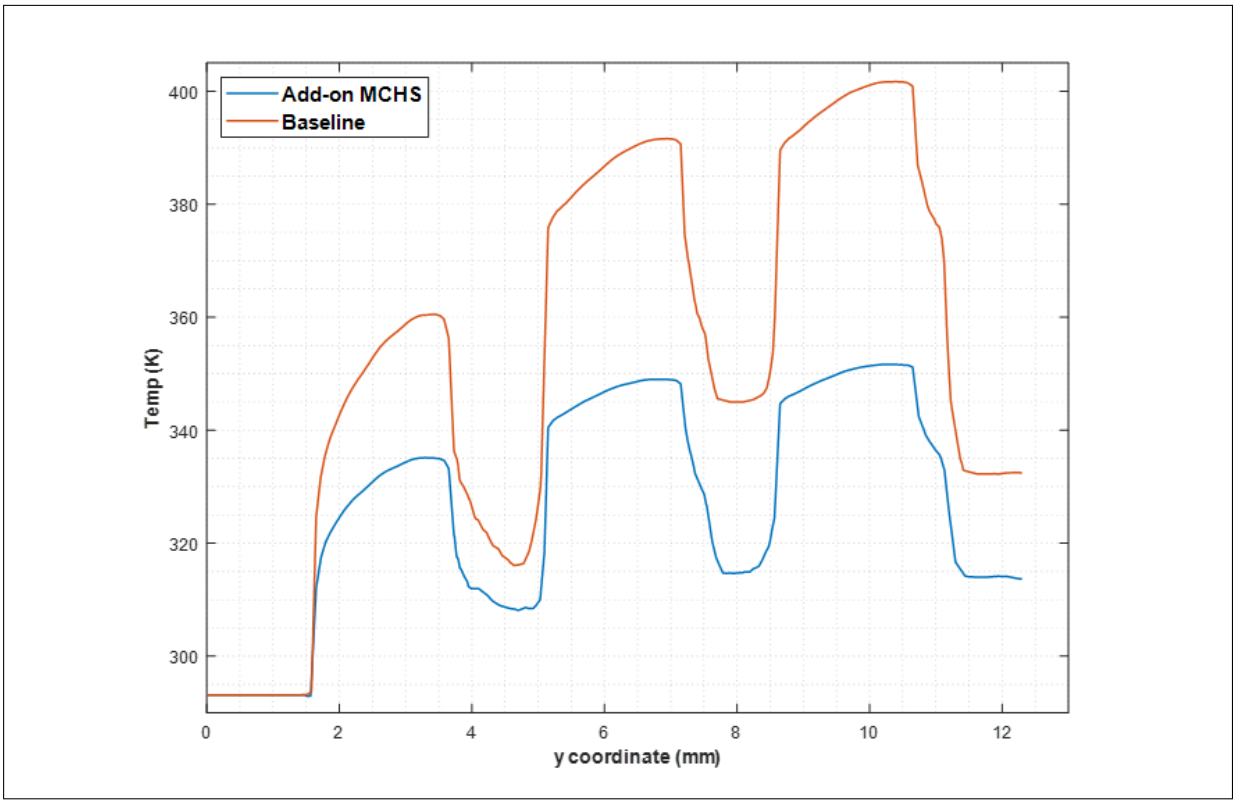


FIGURE 4.8: Comparison of temperature variation along the flow direction at the bottom surface of the chip for(a) the Baseline MCM-BGA package and (b) conventional MCHS equipped MCM-BGA package.

Figure 4.5 compares and presents the thermal stress distribution of chip solders for baseline and MCHS-equipped microelectronic packages. It also presents the zoomed-in view of the critical regions of soldiers exhibiting high-stress values. In general, the stress distribution intensifies in the flow direction, exhibiting minimal stress values at the solder near the inlet and increased stress values towards the outlet. This is primarily due to more heat accumulation towards the outlet, especially in the solders in the middle area. The stress distribution across the PCB solders is observed at three different planes located at $y = -2.5$ mm, $y = 1.5$ mm, and $y = 5.5$ mm, passing through PCB solder balls. Figures 4.6(a) and 4.6(b) exhibit the overall stress and plane stress profiles for both baseline and conventional MCHS equipped MCM BGA packages. Across most regions, stress levels remain low and display a symmetrical pattern, with higher stresses at the top surfaces and lower stresses at the bottom surfaces attached to the PCB. This is due to the higher

temperature zone at the substrate and PCB solder interface and the lower temperature zone at the top of the PCB.

Figures 4.7 and 4.8 provide a comparison of the temperature distribution across the chip solders, using a surface contour plot and a line plot, respectively. The temperature distribution of the chip solders is closely similar to that of the chips, with significantly higher temperatures observed near the outlet compared to the inlet. The overall distribution is non-uniform, with a high-temperature gradient near the outlet, reaching $4.676E + 06$ K/m and $1.7477E + 06$ K/m for baseline and MCHS equipped packages, respectively. The temperature of microelectronic package comprising add-on MCHS exhibits a more uniform distribution. The highest temperature in both the models appears on solders at the middle chip next to the outlet of the mid-channel. Figure 4.8 clearly displays that incorporating a conventional MCHS in conjunction with an MCM-BGA array significantly enhances cooling efficiency, lowering temperatures at hotspots and chip solders by 50 degrees more than the basic package comprising only an MCM-BGA array with a heat spreader. Moreover, the peak stress experienced by the solder connections on the chip has been significantly reduced by 104 MPa when employing a micro-channel heat sink (MCHS) as opposed to the standard setup.

4.3 Comparative Study of MCM-BGA Packages with Conventional and Porous MCHS

The section provides a detailed comparison between the thermal and structural performance of MCM-BGA packages equipped with conventional MCHS and that of the MCM-BGA package incorporating different configurations of porous MCHS. Three configurations of porous MCHS, including a vertically placed porous substrate, a horizontally placed porous substrate, and an all-sided porous substrate, have been

considered for the study. The objective is to assess the effectiveness of porous microchannels in enhancing heat dissipation and reducing thermal stresses within the package, compared to the traditional MCHS when subjected to steady-state loading density conditions. By evaluating key parameters such as temperature distribution, heat transfer coefficient, and induced thermal stresses, this study aims to highlight the advantages and potential drawbacks of incorporating porous structures into MCHS designs. The findings from this analysis will provide valuable insights into the performance trade-offs and the overall feasibility of using porous microchannels for advanced thermal management in high-density loading electronic packages.

The velocity contours at inlet and outlet cross-sections are plotted to determine velocity distributions across horizontal porous, vertical porous, all-sided porous, and standard MCHS setups. Figure 4.9 shows that the flow distribution and velocity magnitudes at the entry and exit points differ considerably. The variations can be attributed to the distinct structural configurations and the pressure losses.

In a conventional MCHS case without porous material, the velocity contour in Figure 4.9(a) demonstrates an even distribution. The flow encounters minimal resistance, allowing it to maintain a relatively consistent velocity pattern from the inlet to the outlet. However, the maximum velocity values occur at the center of the inlet and outlet sections, reaching values of 2.1 m/s and 1.28 m/s, respectively. Additionally, due to the no-slip boundary condition, the resultant velocity at the channel walls is roughly zero.

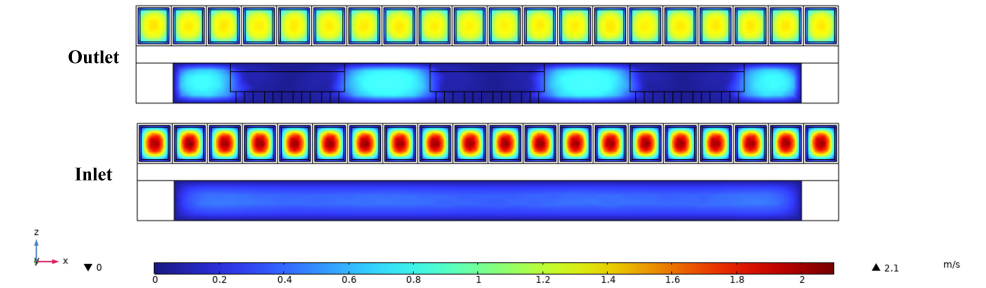
In the case of horizontally placed porous along the top and bottom faces of the Microchannel Heat Sink (MCHS), the velocity magnitude in Figure 4.9(b) at central areas reaches values of 2.45m/s and 1.83m/s at inlet and outlet cross-sections, respectively. Also, vertically placed porous material in Figure 4.9(c) along the left and right faces of the Microchannel Heat Sink (MCHS) shows similar magnitudes of velocities in the inlet and outlet sections. The main difference evident in both cases from the contour plots is that while employing the porous horizontally, the spread of

velocities increases along the width direction, and when porous is used vertically, the spread of velocities increases along the height of the channels. The primary reason behind the rise in the velocity spread is the restriction brought up by integrating the porous material in the channels. Moreover, the velocity magnitudes at channel walls and outlet sections show an identical pattern to conventional MCHS.

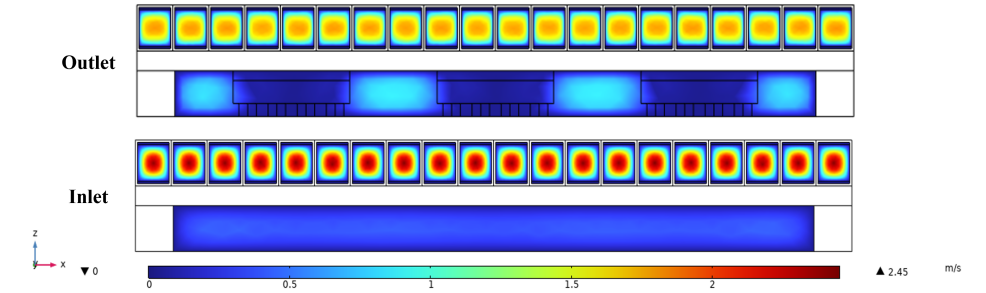
In the case of the MCHS case, with porous material placed on all faces, the flow encounters maximal resistance (refer Figure 4.9(d)), allowing the maximum velocity magnitudes at the center of the inlet and outlet sections with the values of 2.82 m/s and 2.52 m/s, respectively. Additionally, due to the no-slip boundary condition, the resultant velocity at the channel walls is roughly zero. The maximum velocity across the mid-channel for all the cases at the inlet and outlet remains 0.428 m/s and 0.821 m/s, respectively.

Even though there is a reduction in the velocity at the outlet of all-sided porous, the velocity is still higher even than velocities at the inlet of all other configurations. This is likely due to more concentration towards the channel's center due to higher pumping losses in porous regions. The added resistance (by porous material) reduces the velocity near the walls, causing the fluid to be redirected towards the center of the channel, where there is less resistance. As a result, the fluid in the center moves faster to compensate for the slower flow near the walls, leading to an overall increase in velocity at the channel's center.

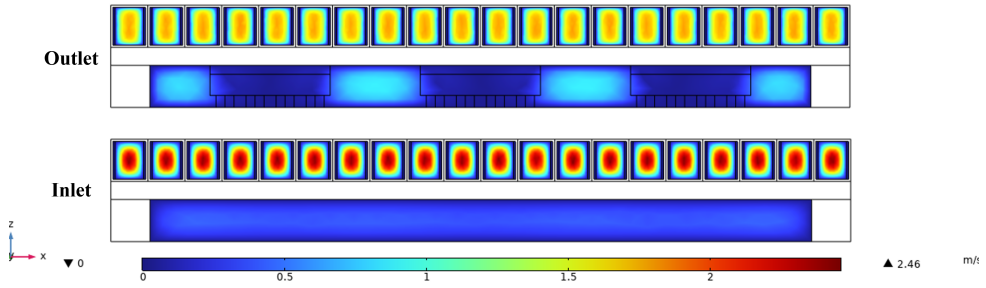
Figure 4.10 compares and presents the temperature contours at the region of maximum heat accumulation near the outlet (y = 4.25 mm) for the standard MCHS and various porous MCHS configurations of microelectronic packages. The subfigures generally indicate a symmetric temperature distribution across all configurations, with different maximum temperature magnitudes. The highest temperatures are found at the hotspots on the IC chips, followed by the thermal grease, chip solders, substrate, and then the PCB, with the coolest temperatures detected in the MCHS channels.



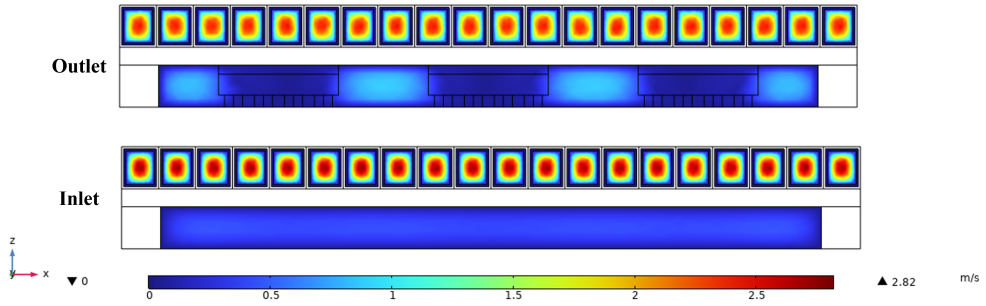
(a)



(b)



(c)



(d)

FIGURE 4.9: Velocity contours at inlet and outlet cross-sections for MCM-BGA package equipped with (a) the conventional MCHS, (b) the horizontally placed porous MCHS, (c) the vertically placed porous MCHS, and (d) the all-sided porous MCHS.

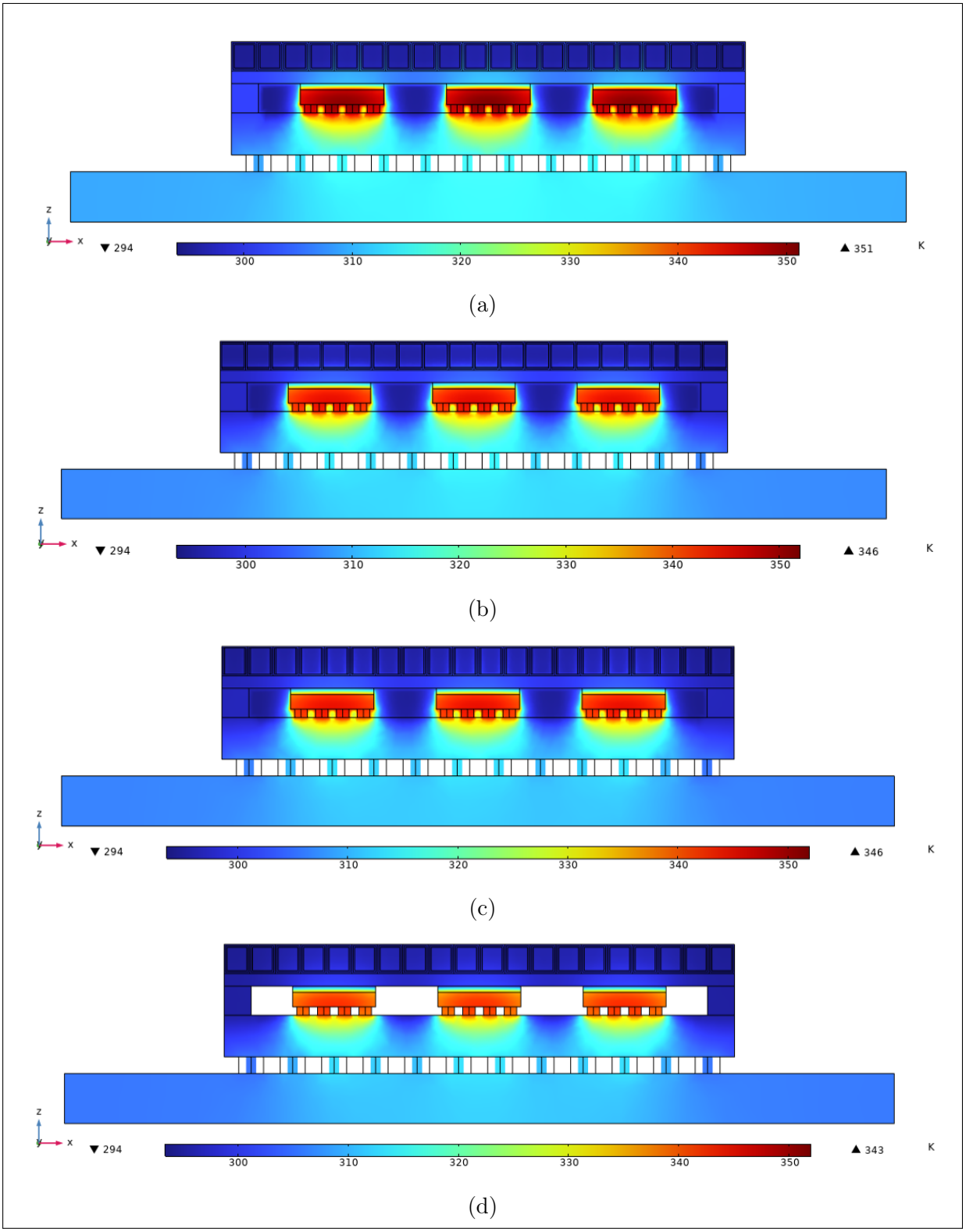
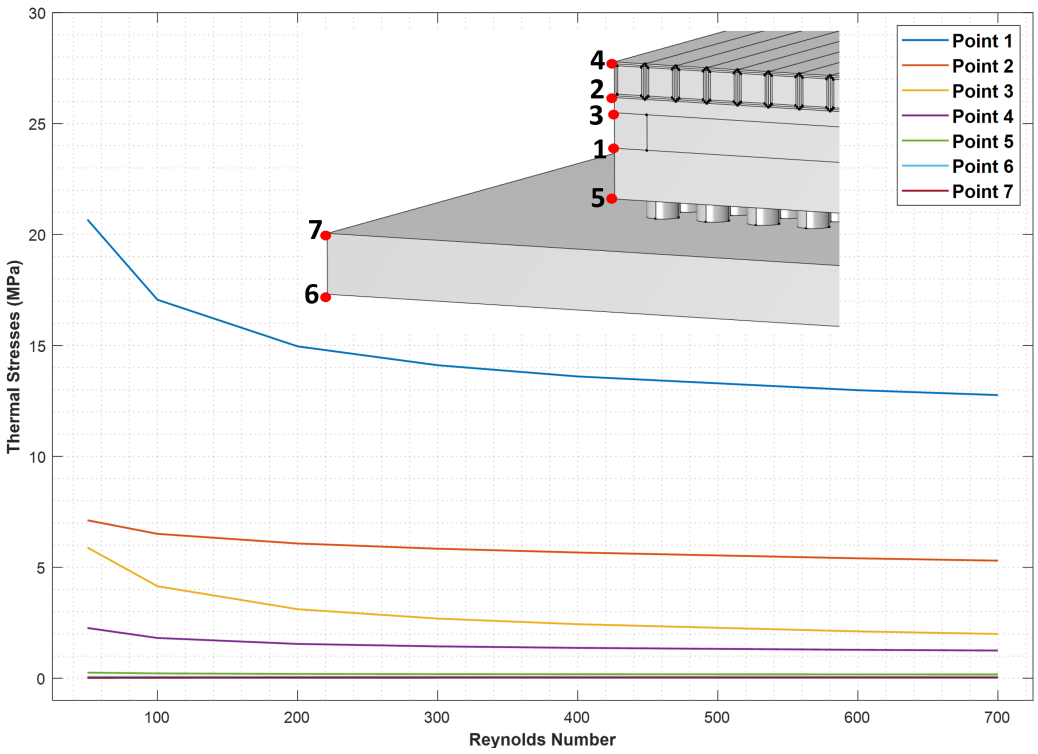
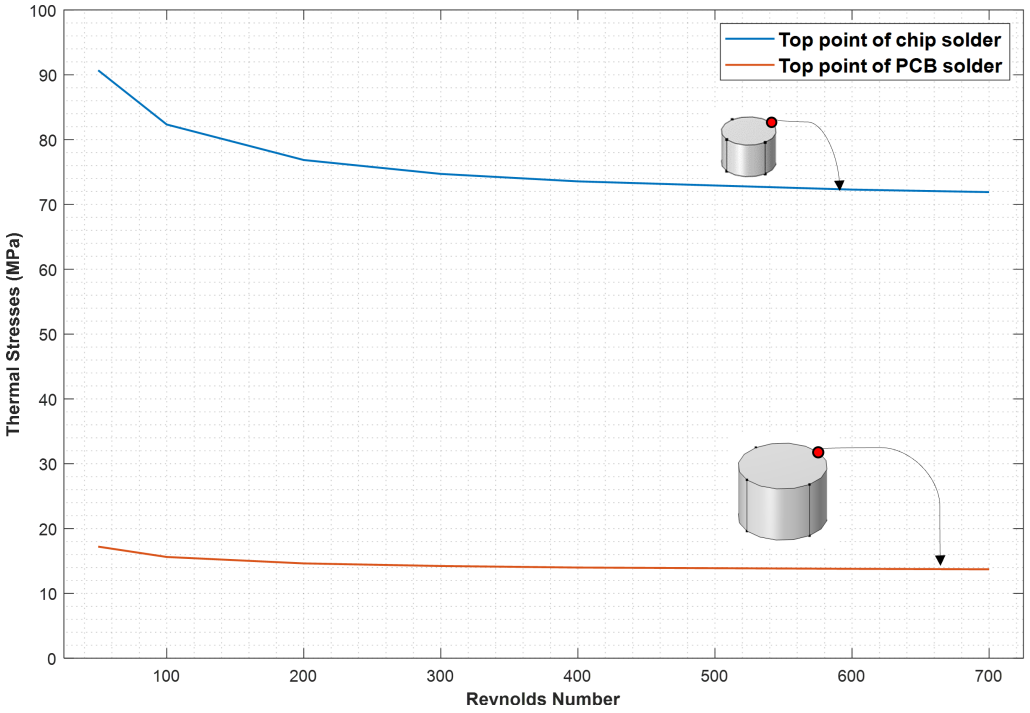


FIGURE 4.10: Temperature distribution at a cross-sectional plane (at y = 4.25mm) for the MCM-BGA package equipped with (a) the conventional MCHS, (b) the horizontally placed porous MCHS, (c) the vertically placed porous MCHS, and (d) the all-sided porous MCHS.



(a)



(b)

FIGURE 4.11: Impact of Reynolds Number on Thermal Stress at (a) Various Target Points within the MCM-BGA Package Structure and (b) Top Points of Chip and PCB Solder Joints.

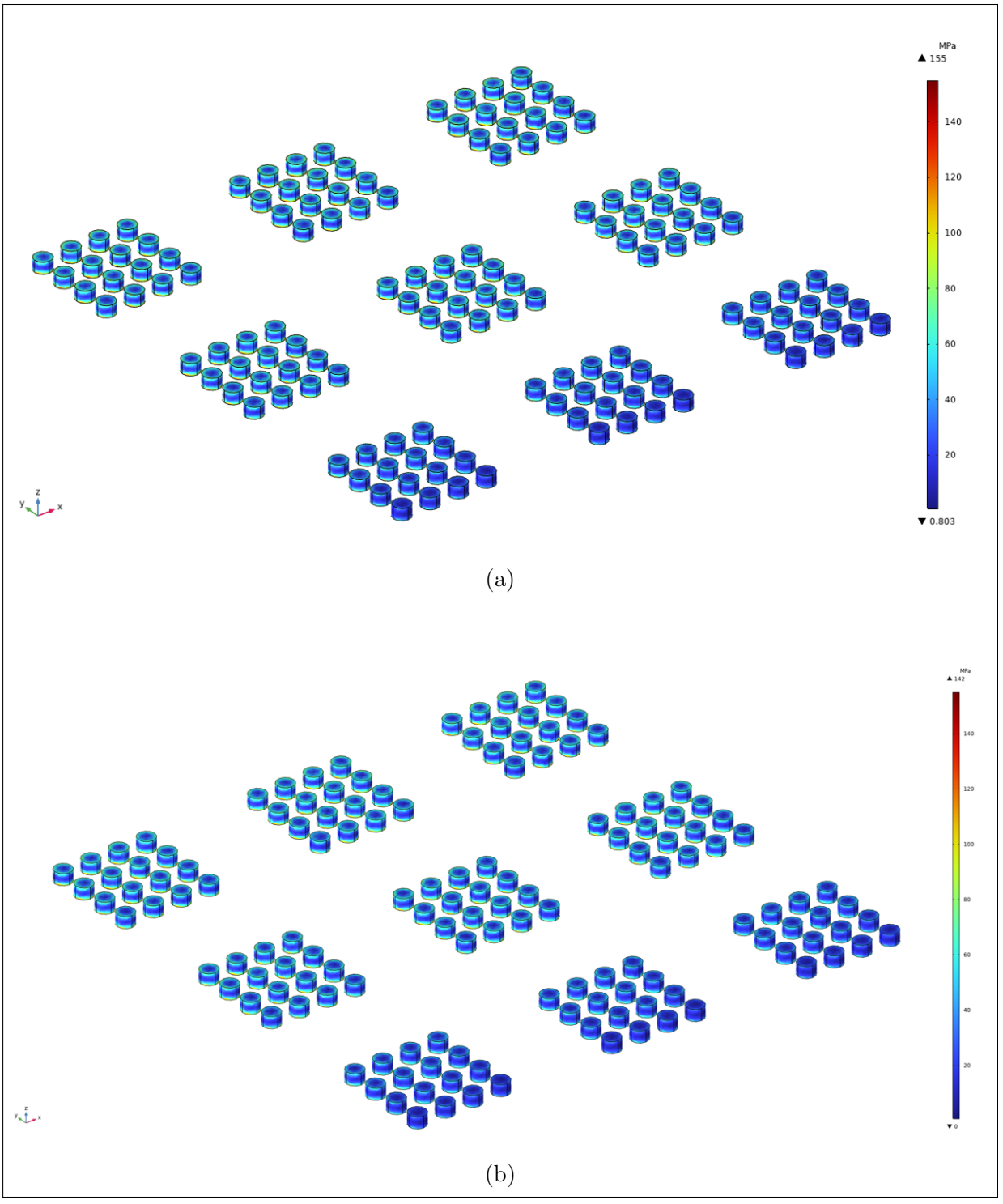


FIGURE 4.12: Thermal stress contours of chip solders for MCM-BGA package equipped with (a) the conventional MCHS and (b) the horizontally placed porous MCHS.

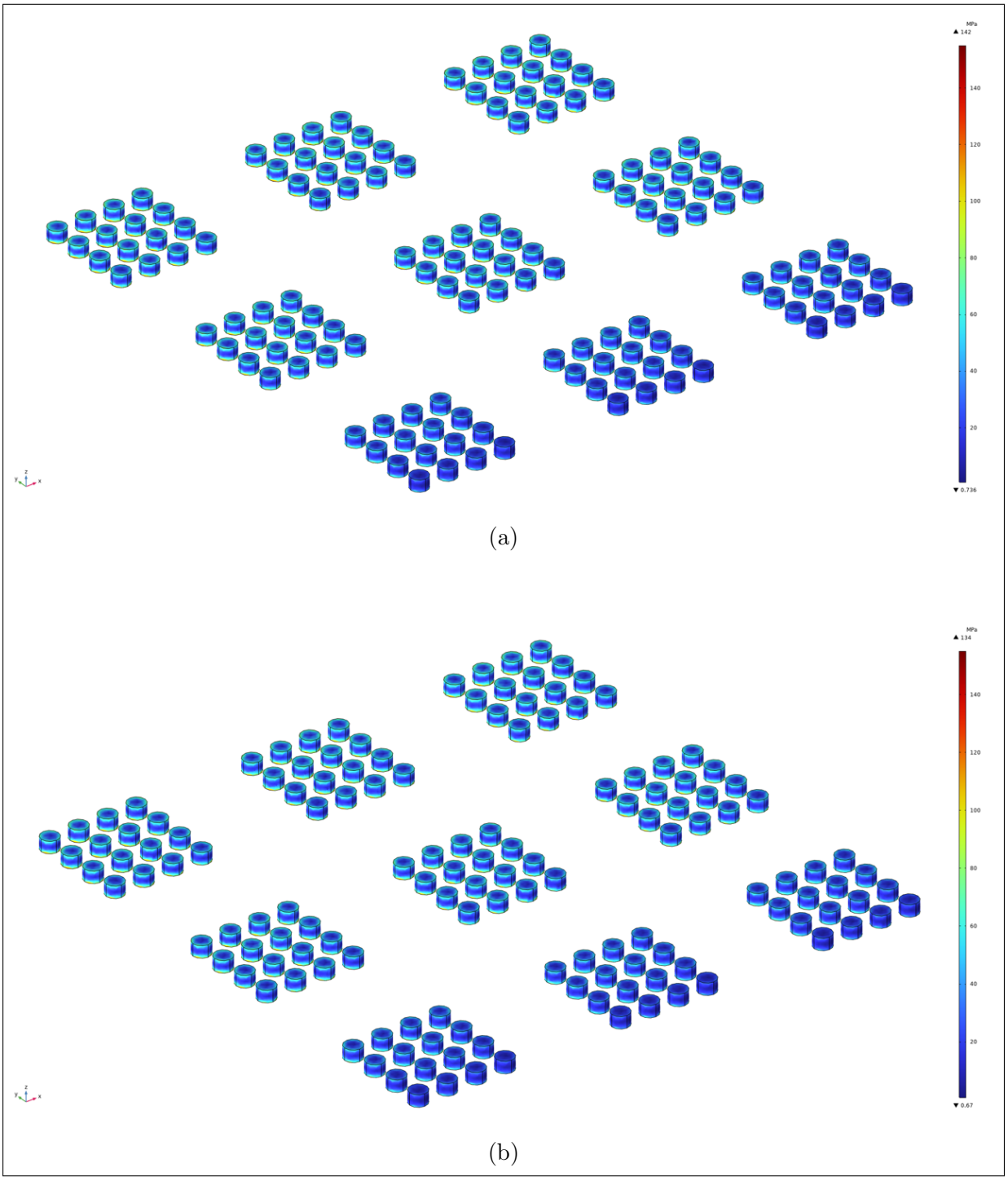


FIGURE 4.13: Thermal stress contours of chip solders for MCM-BGA package equipped with (a) the vertically placed porous MCHS, and (b) the all-sided porous MCHS.

Figure 4.10(a) displays the temperature distribution for the conventional MCHS setup. The maximum temperature is observed on the chip and chip solder, reaching approximately 352K. This is followed by the substrate at 350K, the thermal grease at 348K, and the PCB and PCB solder at about 316K. The heat spreader and MCHS exhibit the lowest temperature at 310K and MCHS at 309K.

For the MCM-BGA array with a horizontal porous MCHS setup (refer 4.10(b)), the temperature of the chip and chip solders decreased to 346K, while the substrate temperature reduced to 345K, and the thermal grease to 343K. The PCB and PCB solder temperatures dropped to 314K, with the heat spreader and MCHS temperatures further declining to 305K and 303K, respectively.

For the MCM-BGA array with a vertical porous MCHS setup (refer 4.10(c)), the temperature of the chip and chip solders decreased to 345K, while the substrate temperature reduced to 344K, and the thermal grease to 342K. The PCB and PCB solder temperatures dropped to 312K, with the heat spreader and MCHS temperatures further declining to 304K and 303K, respectively.

For the MCM-BGA array with all sides porous MCHS layout (refer 4.10(d)), the temperature of the chip and chip solders decreased to 343K, while the substrate temperature reduced to 341K, and the thermal grease to 340K. The PCB and PCB solder temperatures dropped to 312K, with the heat spreader and MCHS temperatures further declining to 300K and 299K, respectively. Therefore, it becomes clear that the MCM-BGA Array with all sides porous MCHS setup is the most effecting configuration, showing the best temperature reduction over the hotspots by 9 degrees compared to conventional MCHS setup without porous.

To identify the regions bearing the maximum value of thermal stresses, seven different target points at the outlet cross-section of the electronic package and two points on chip solders and PCB solders were considered for the evaluation. Figure 4.11 depicts the

locations of seven selected target points and their corresponding thermal stress distributions across varying Reynolds numbers. The thermal stresses at these points demonstrate a consistent declining trend as the Reynolds number increases. At the Reynolds number of 700, the maximum thermal stress of 13 MPa is observed at Point 1, located at the bottom of the heat spreader, followed by approximately 5 MPa at Point 2, situated at the bottom of the MCHS. The other identified points show very low stress levels, all under 5 MPa, implying a minor effect on deformation, thus maintaining the structural integrity of the overall package.

Figure 4.11(b) depicts the thermal stress at the top points of the chip and PCB solder. The stress values at the top point of the chip solder are notably high, ranging from 91 to 72 MPa, as the Reynolds number varies from 50 to 700. The stresses on the PCB solder joints are significantly lower, ranging from 17 to 14 MPa across the same range of Reynolds numbers. However, it was also observed that at lower Reynolds numbers, the thermal stresses at the chip solder joints exceeded the critical value of 160 MPa in certain regions (as discussed in the next chapter).

Figures 4.12 and 4.13 present the thermal stress distribution of the chip solders of microelectronic packages equipped with various configurations of MCHS. The analysis reveals that the stress pattern within solders is non-uniform, with the stress values significantly higher at interfaces (welded regions) than in other areas. The stress levels increase rapidly along the flow direction, bearing maximum stresses at solders near the outlet. The thermal stresses at the welding spots in the package equipped with conventional MCHS come out to be 155 MPa, followed by 142 MPa for both horizontally and vertically placed porous MCHS configurations. The lowest value of maximum thermal stress, 134 MPa, was observed in the case of an all-sided porous arrangement due to the lower temperature gradient near the outlet.

4.4 Parametric Study and Optimisation Results

The section presents a comprehensive parametric analysis undertaken to assess the thermo-structural and hydraulic performances of MCM-BGA packages equipped with different configurations of MCHS. This examination focuses on key parameters, such as the maximum temperature, maximum thermal stresses, Heat transfer coefficients, Nusselt number, pressure loss, and pumping power, as the function of the Reynolds number. The analysis aims to identify the optimal MCHS configuration out of the various MCHS configurations based on the aforementioned performance parameters. The section further details designing a novel porous MCHS setup for the MCM-BGA package. This novel configuration aims to achieve a higher heat transfer coefficient and figure of merit (FOM) using the e Nelder-Mead Optimization algorithm implemented in COMSOL.

4.4.1 Parametric Study Results

The section presents the results of the thermo-structural and hydraulic parameters plotted against varying Reynolds numbers for an MCM-BGA package integrated without porous, horizontally placed porous, vertically placed porous, and all-sided porous MCHS.

Figures 4.23(a) and 4.23b show the impact of increasing the Reynolds number on the Maximum temperature and maximum stresses within the package for different MCHS configurations. A general declining trend of the stress and temperature values is visible from the plots with increasing Reynolds numbers. The reduction in stress and temperature is more pronounced at higher Reynolds, particularly for all cases. At lower Reynolds numbers between 50-100, the temperature and stress remain more or less the same for designs integrating conventional MCHS, horizontally and vertically placed porous MCHS. However, an all-sided porous configuration shows a significant difference in stress and temperature values, even at low Reynolds numbers. At a higher Reynolds number of 700,

the all-sided porous MCHS configuration demonstrates the most significant reduction in both maximum temperature and thermal stress. Specifically, the maximum temperature is reduced by 3°C and 8°C, and the thermal stress decreases by 8 MPa and 21 MPa compared to vertical/horizontal porous and conventional MCHS configurations.

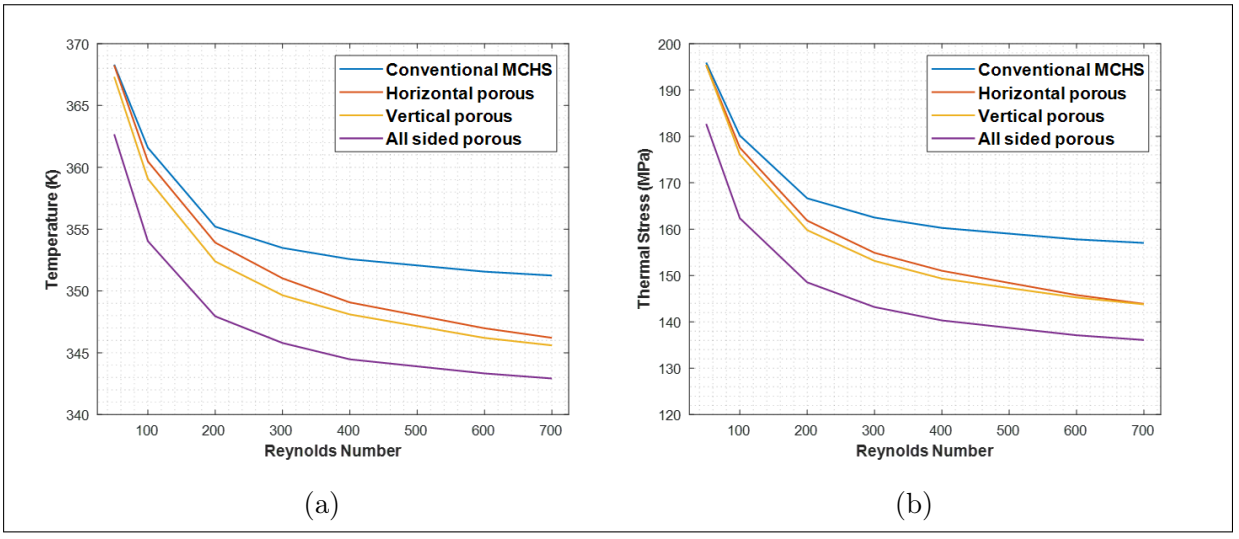


FIGURE 4.14: Variation of maximum temperature and thermal stress with Reynolds number for different packages.

Figures 4.15(a) and 4.15(b) show the impact of increasing the Reynolds number on the pressure drop and pumping power for different MCHS configurations. A general increasing trend of the pressure drop and pumping power values is visible from the plots with increasing Reynolds numbers. The increase in pressure losses and pumping power is more pronounced at higher Reynolds, particularly for all cases. At Reynolds numbers between 50-200, the pressure drop and pumping power required remain more or less the same for designs integrating conventional MCHS, horizontally and vertically placed porous MCHS. However, an all-sided porous configuration shows a rapid increase in the values, with a gradual increment in Reynolds numbers. At a higher Reynolds number of 700, the all-sided porous MCHS configuration demonstrates the most significant increase in both parameters. Specifically, the pressure drop is increased by roughly 153 KPa and 170 KPa, and the pumping power increases by 0.10 W and 0.12 W compared to vertical/horizontal porous and conventional MCHS configurations.

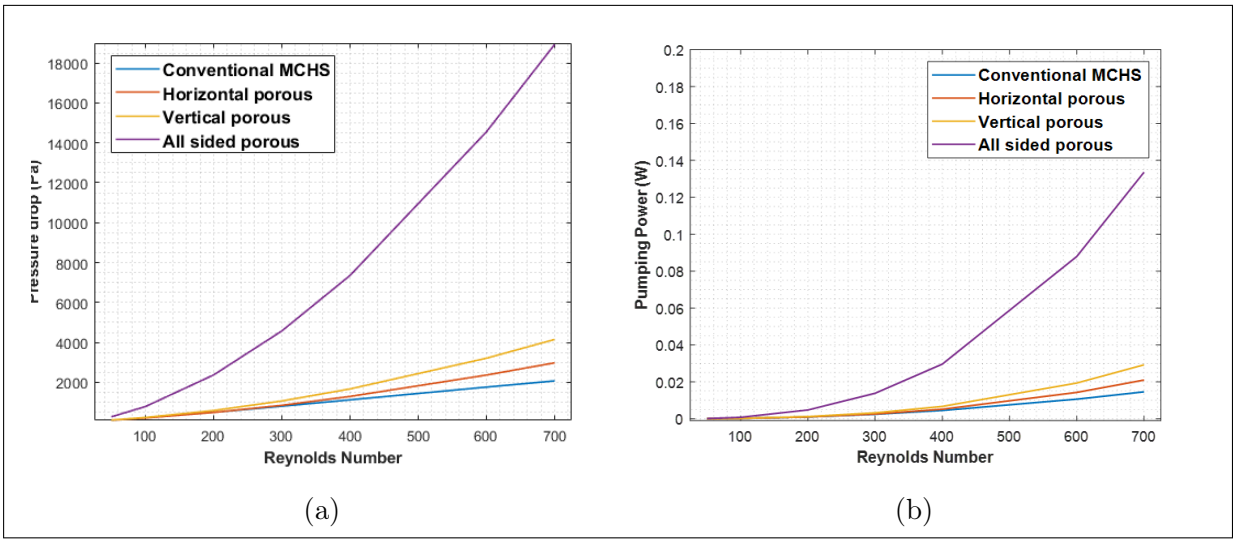


FIGURE 4.15: Variation of pressure drop and pumping power with Reynolds number for different packages.

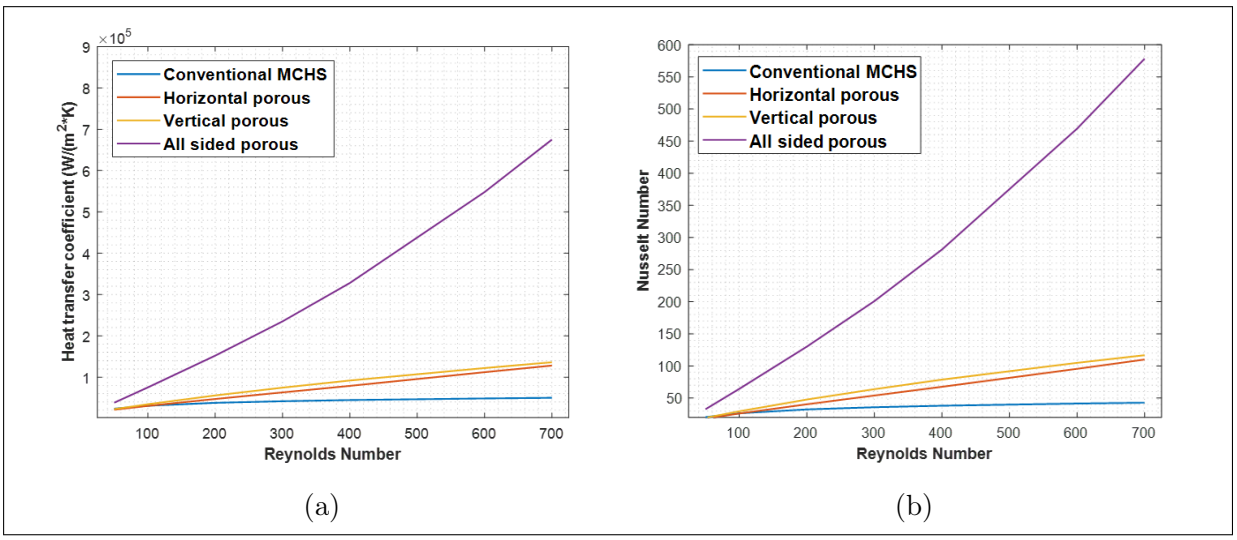


FIGURE 4.16: Variation of heat transfer coefficient and Nusselt number with Reynolds number for different packages.

Figures 4.16(a) and 4.16(b) show the impact of increasing the Reynolds number on the heat transfer coefficient and Nusselt number for different MCHS configurations. A general increasing trend of the heat transport coefficient and Nusselt number values is visible from the plots with increasing Reynolds numbers. Both thermal performance parameters increase is more pronounced at higher Reynolds, particularly for all-sided porous MCHS. There is a minimal rise in both values for conventional MCHS, which remains almost stagnant with the increasing Reynolds number. At Reynolds numbers

between 50-200, the Nusselt number and heat transport coefficient remain more or less the same for horizontally and vertically placed porous MCHS. However, an all-sided porous configuration shows a rapid increase in the values, with a gradual increment in Reynolds numbers. At a higher Reynolds number of 700, the all-sided porous MCHS configuration demonstrates the most significant increase in both parameters. Specifically, the heat transfer coefficient is increased by roughly 539 $KW/(m^2.K)$ and 625 $KW/(m^2.K)$, and the Nusselt number increases by 468 and 536 compared to vertical/horizontal porous and conventional MCHS configurations.

4.4.2 Optimisation Results

Among all four MCHS configurations, the all-sided porous MCHS was found to be the most effective in reducing thermal stresses and temperatures in the BGA package. Before proceeding with optimization, parametric studies were done on a single unit of all-sided porous MCHS to understand the impact of increasing porous thickness on the heat transfer coefficient, pumping power, and Figure of Merit.

For the parametric study for a single unit of the all-sided porous configuration, the solid thickness was kept constant while the porous thickness was varied from 0.05 mm to 0.245 mm. The resulting heat transfer coefficients corresponding to the varying porous thicknesses are plotted and shown in Figure 4.17. It is evident from the figure that the heat transfer coefficient increases with the porous thickness up to 0.211 mm, after which it begins to decrease. The initial jump in the heat transport coefficient is because the increased porous area facilitates better heat exchange between the fluid and the microchannel walls. After reaching the critical limit of the porous thickness, the clear passage within the channel narrows significantly, restricting the flow of the fluid. This restriction leads to a higher flow resistance and reduced fluid velocity through the channel. The reduced velocity, in turn, diminishes the convective heat transfer rate, resulting in a slight drop in the heat transfer coefficient.

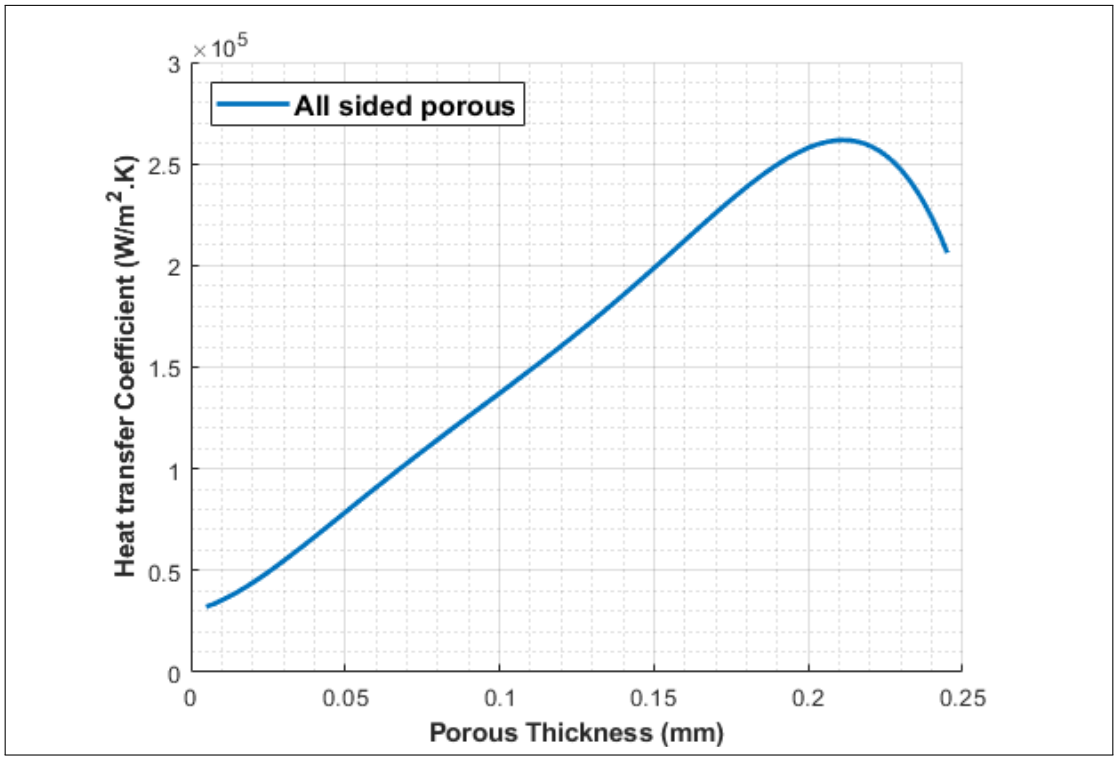


FIGURE 4.17: Variation of heat transfer coefficient with varying porous thickness for a single MCHS unit.

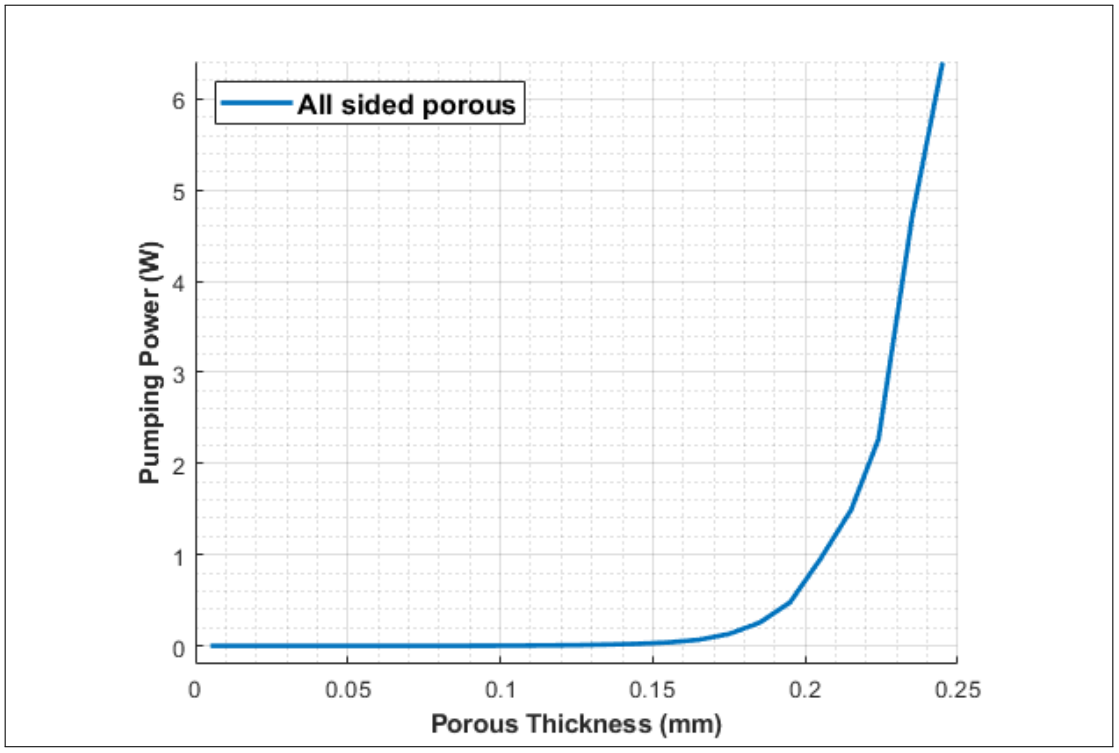


FIGURE 4.18: Variation of pumping power with varying porous thickness for a single MCHS unit.

Figure 4.18 displays the pumping power as a function of varying porous thickness. The curve indicates a very gradual increase in pumping power up to a porous thickness of 0.15 mm, after which the increase becomes much steeper. This behavior can be attributed to the increasing flow resistance as the porous thickness expands. Initially, the flow remains relatively less obstructed, resulting in a slight increase in pumping power. However, as the porous layer becomes thicker, it significantly constricts the flow passage, leading to a rapid increase in resistance and, consequently, a sharp rise in the pumping power is required to maintain the same flow rate.

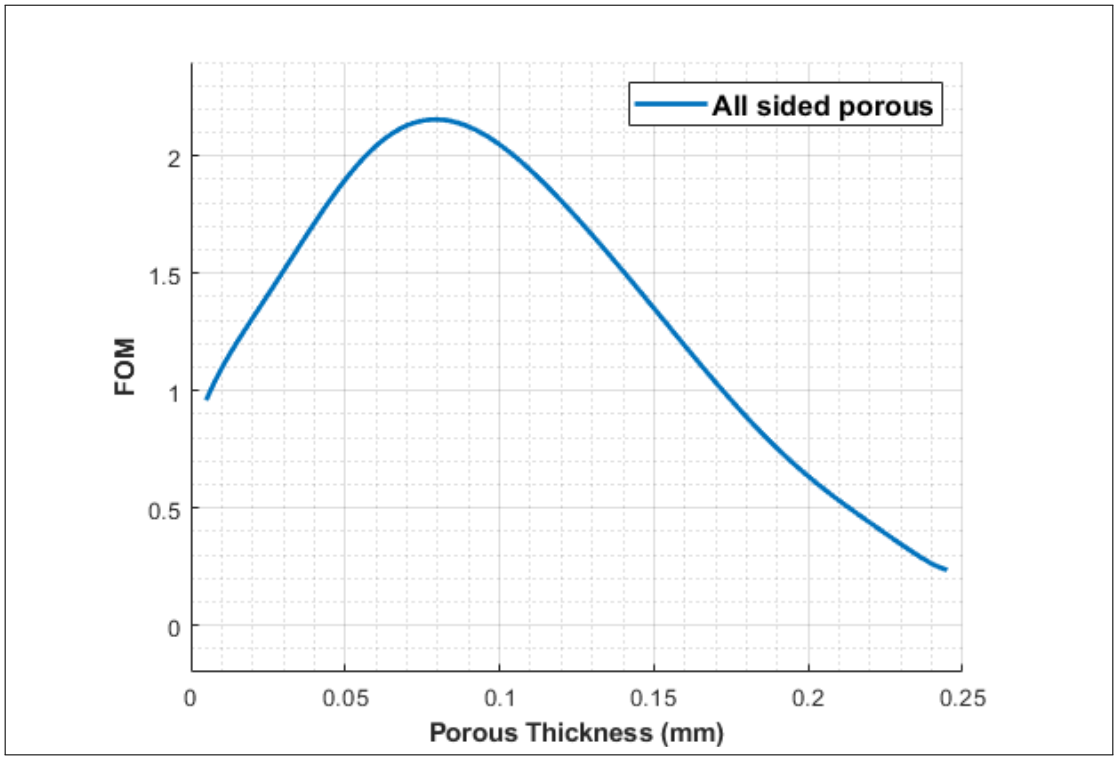


FIGURE 4.19: Variation of figure of merit with varying porous thickness for a single MCHS unit.

The Figure of Merit (FOM), as defined in the Mathematical modeling subsection, compares all-sided porous MCHS design with varying porous thickness to conventional MCHS, allowing for the evaluation of improvements in one design relative to another by considering both heat transfer performance and pumping power. Figure 4.19 represents the trend of FOM with increasing porous thickness, with maximum FOM occurring at 0.07 mm porous thickness. Initially, as the porous thickness increases, there is an

apparent rise in the FOM due to an enhancement in the heat transport coefficient. A moderate increase in pumping power accompanies this increase in the heat transport coefficient. However, beyond a porous thickness of 0.07 mm, the improvement in the heat transport coefficient becomes minimal, while the increase in pumping power becomes more pronounced. This results in a decrease in the FOM, as described by Equation 3.19.

To determine the optimal porous thickness based on the parametric results obtained for varying porous thicknesses, a multi-objective optimization was performed to maximize the Figure of Merit (FOM) for a single MCHS unit. The primary objective selected for optimization is to maximize FOM for a unit showcasing optimal heat transfer coefficient and a mild increase in the pumping power. The optimization targets finding the optimal solid and porous thicknesses for the porous MCHS unit that achieved the highest FOM.

To reduce computational time, the optimization was conducted on a single unit of the all-sided porous MCHS. The average heat flux, computed at the base of the all-sided porous MCHS MCM-BGA model, was utilized to optimize a single unit of all-sided porous MCHS. This approach ensured an accurate and efficient optimization of the overall thermo-structural performance without much compromise in pumping power. The constrained optimization process utilized the Nelder-Mead algorithm, built within COMSOL, to optimize a single unit. For defining constraints, both solid and porous thicknesses were set to lower and upper bounds of 0.05 mm and 0.25 mm, respectively. For the simulation setup, the heat flux value of 1.259 E +06 $W/(m^2.K)$ is assigned at the base of the MHS, assuming all the outside walls are insulated. The optimization resulted in a total of 32 different possible solutions with improved FOMs. Out of all the possible solutions, the solution that yields the highest heat transfer coefficient (1.66E +05 $W/(m^2.K)$) and FOM (2.8688) with minimal increment in pumping power (0.0018519 W) has been considered to be the optimal solution. The corresponding optimal porous and solid thicknesses were found to be 0.0849 mm and 0.429 mm,

respectively. The resulting Pareto fronts with the optimal highlighted objectives are presented in Figures 4.20 (a) and (b).

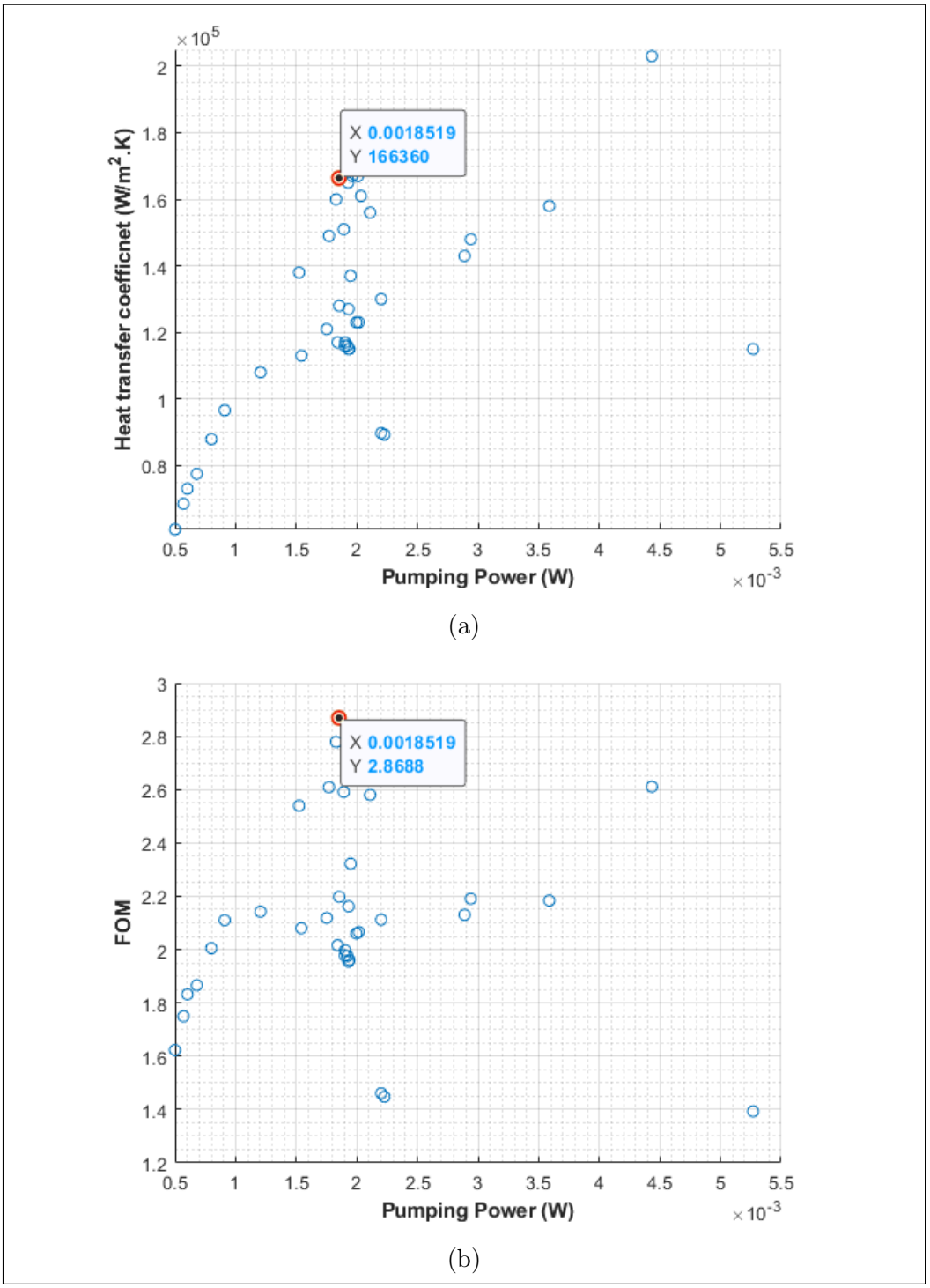


FIGURE 4.20: Figures representing (a) optimal heat transfer coefficient w.r.t pumping power and (b) figure of merit w.r.t pumping power.

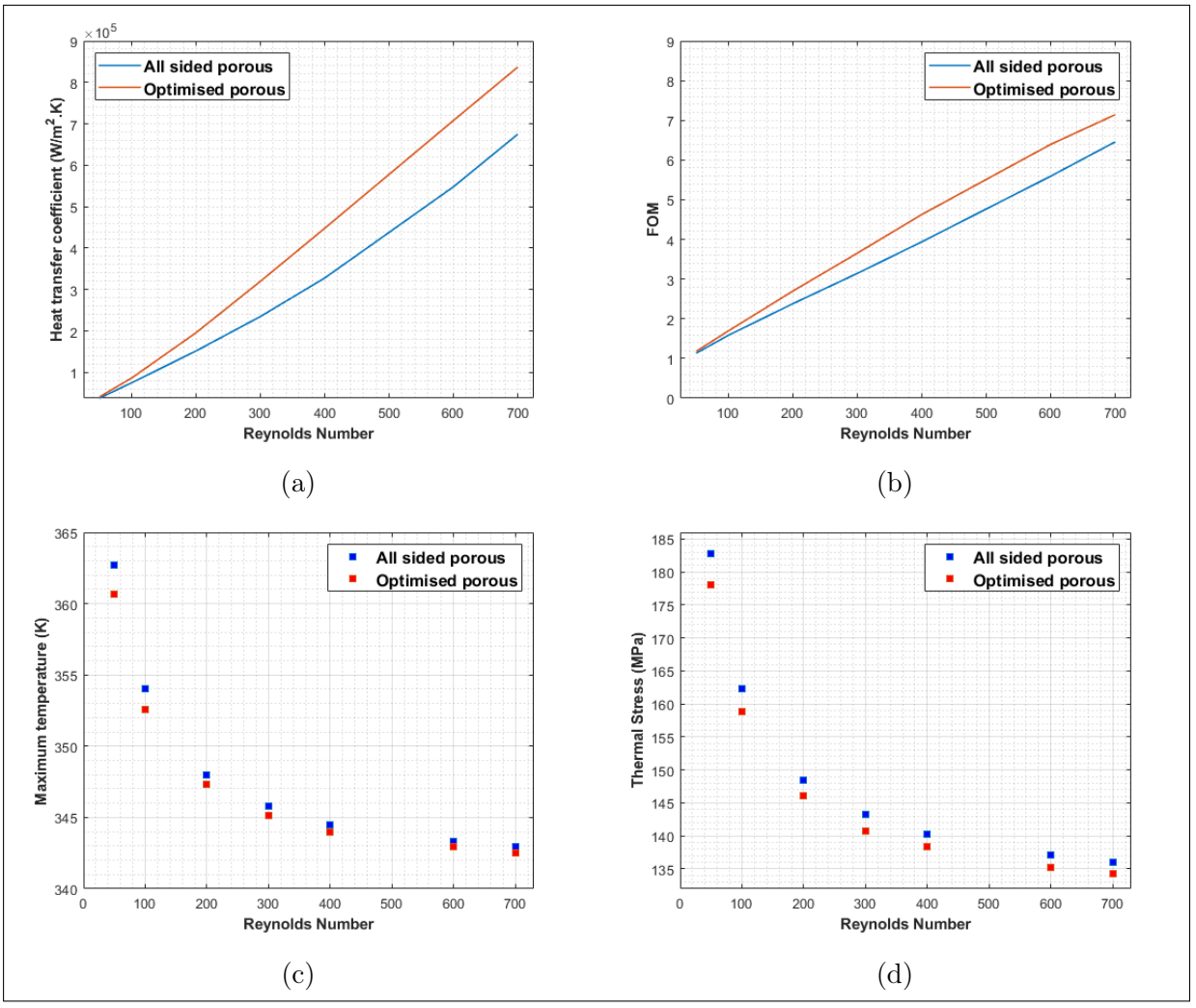


FIGURE 4.21: Impact of Reynolds number variations on an MCM-BGA array with all-sided and optimized porous MCHS setups, showing (a) heat transfer coefficient, (b) Figure of Merit (FOM), (c) maximum temperature, and (d) thermal stress.

The obtained array of the single optimized units through optimization of all-sided porous configuration is then integrated with the MCM-BGA array. Figures 4.21(a) and 4.21(b) indicate the improvement in heat transfer coefficients and FOM with varying Reynolds numbers. A general increasing trend of heat transfer coefficient and FOM for both the all-sided porous and optimized porous MCHS has been observed with increasing Reynolds number. At a lower Reynolds number of 50, the values of both parameters are almost identical. However, with an increase in Reynolds number, the difference becomes more pronounced for both configurations. At Reynolds no. of 700, the optimized porous configuration shows an increase in the heat transfer coefficient by

162 $KW/((m^2.K)$ and an improvement in FOM from 6.45 to 7.142 compared to the all-sided porous configuration. Figures 4.21(c) and 4.21(d) indicate the pattern of maximum temperature and thermal stresses with varying Reynolds numbers. Both the maximum temperature and maximum stress values exhibit a similar declining trend for the BGA packages integrated with all-sided porous and optimized porous MCHS with increasing Reynolds number.

4.5 Fatigue Life Cycle Analysis Results

The section discusses the fatigue life cycle analysis of the baseline MCM-BGA and MCM-BGA packages equipped with various microchannel heat sink (MCHS) configurations. This analysis aims to analyze how the different designs affect the reliability of packages when IC chips are subjected to periodic loading density. The stress and temperature contours obtained from simulations at various time steps were assessed to determine the structural integrity of each setup. The fatigue life cycle is evaluated through the application of the Coffin-Manson and Darveaux methods to predict the lifespan of the chip solders.

To understand the impact of periodic loading density on various geometrical setups, the temperature and stress distribution contours from the simulated results are plotted at the different time steps. The temperature contours for the package integrating optimized MCHS were plotted by taking a plane at y=4.25mm, the region with a maximum temperature gradient for different time steps, and are represented in Figure 7. Since maximum stress is generated in the solders placed between substrate and chips, the plotted stress contours at the same time as the steps above are shown in Figures 9 and 10. Figure 4 represents the temperature distribution at four different time steps during the first load cycle, where time steps correspond to the activation phase, peak loading, idle or standby stage, and the dwell period before the onset of the next load cycle.

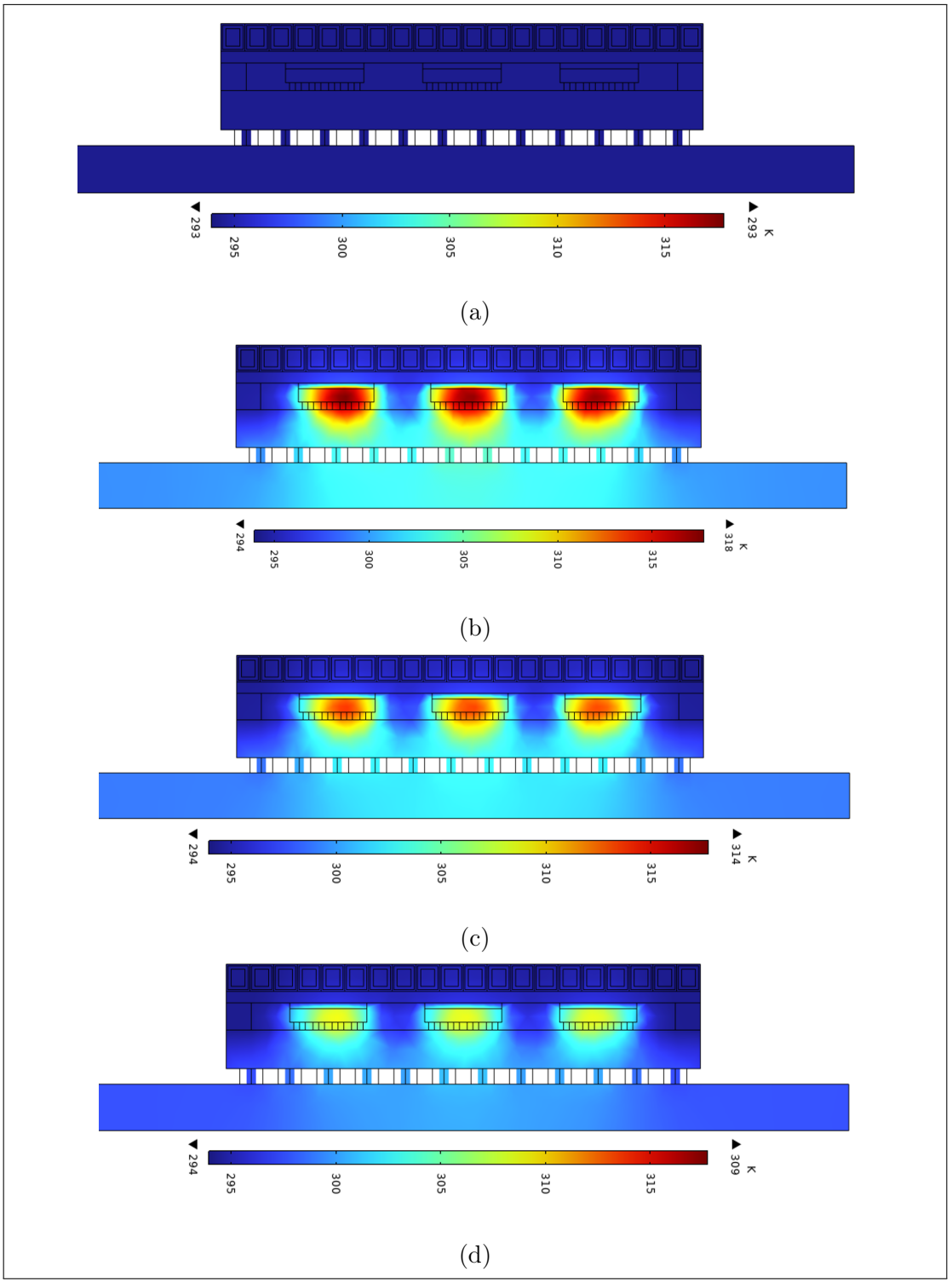


FIGURE 4.22: Transient temperature distribution at a cross-sectional plane (at y = 4.25mm) for the optimized MCM- MCM-BGA package at (a) 18 sec, (b) 1440 sec, (c) 14580 sec, and (d) 18000 sec.

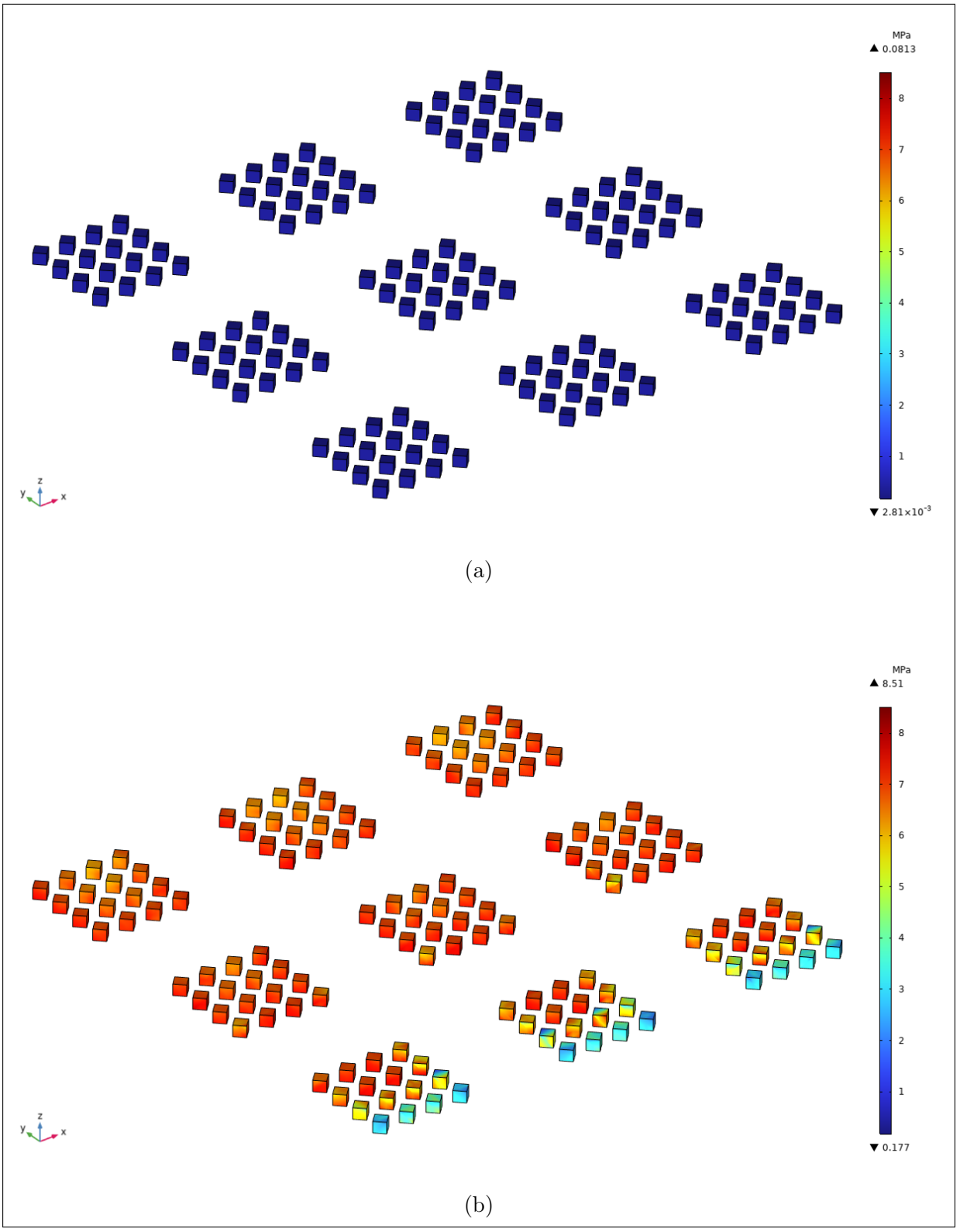


FIGURE 4.23: Transient stress contours of the chip solders for the optimized MCM-BGA package at (a) 18 sec, (b) 1440 sec.

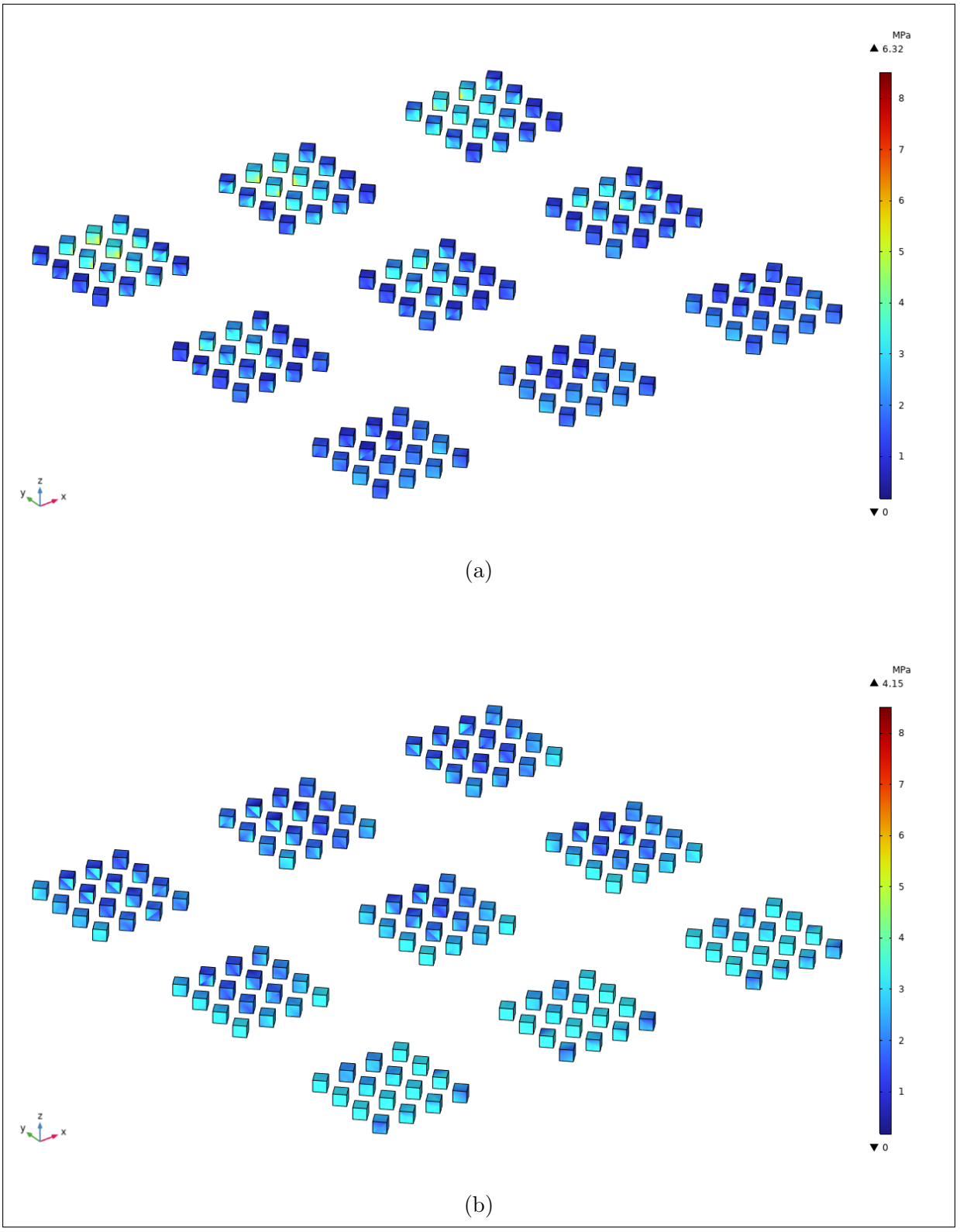


FIGURE 4.24: Transient stress contours of the chip solders for the optimized MCM-BGA package at (a) 14580 sec and (b) 18000 sec.

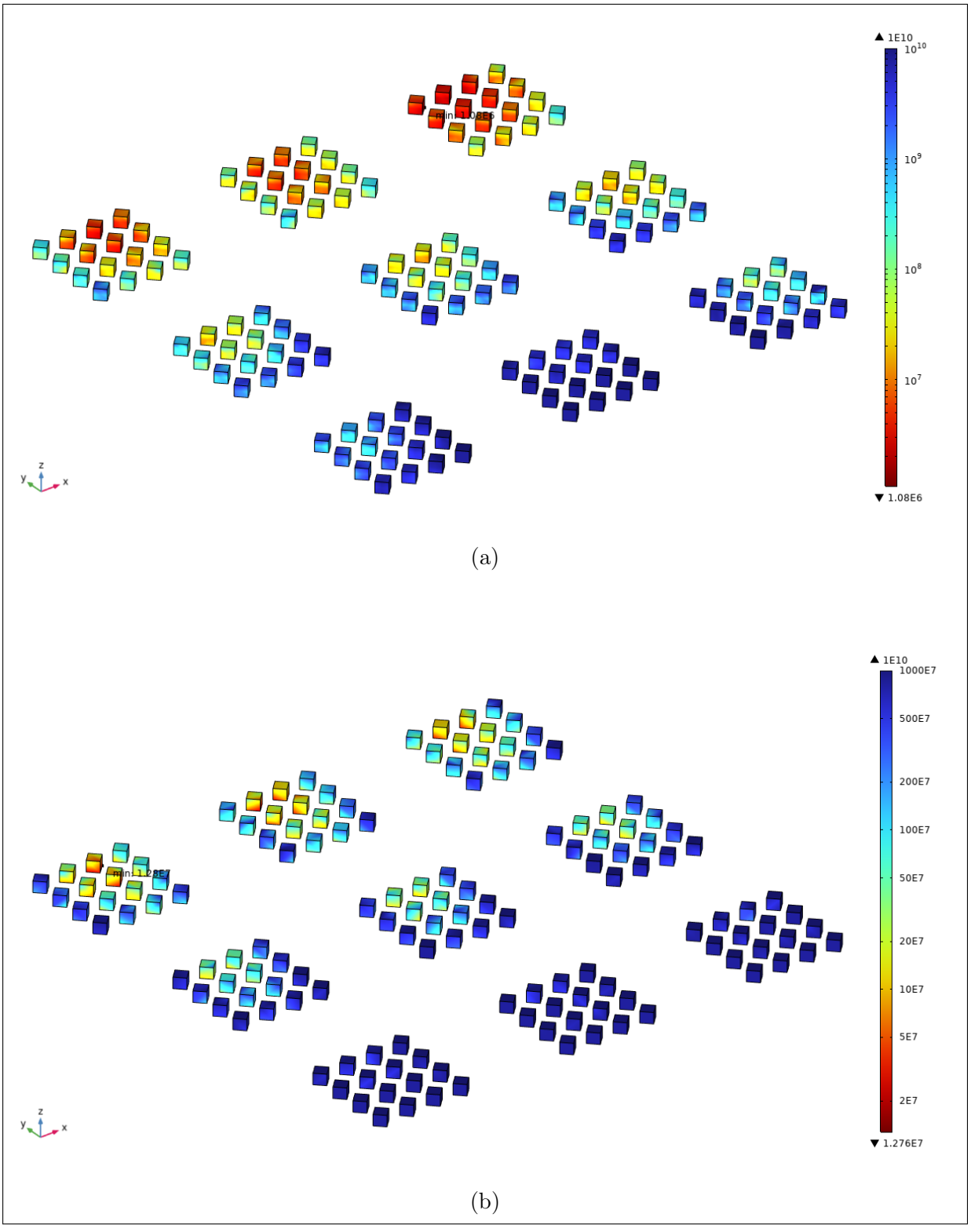


FIGURE 4.25: Coffin-Manson life cycle results for chip solders of (a) Baseline MCM-BGA package and (b) MCM-BGA package equipped with a conventional MCHS.

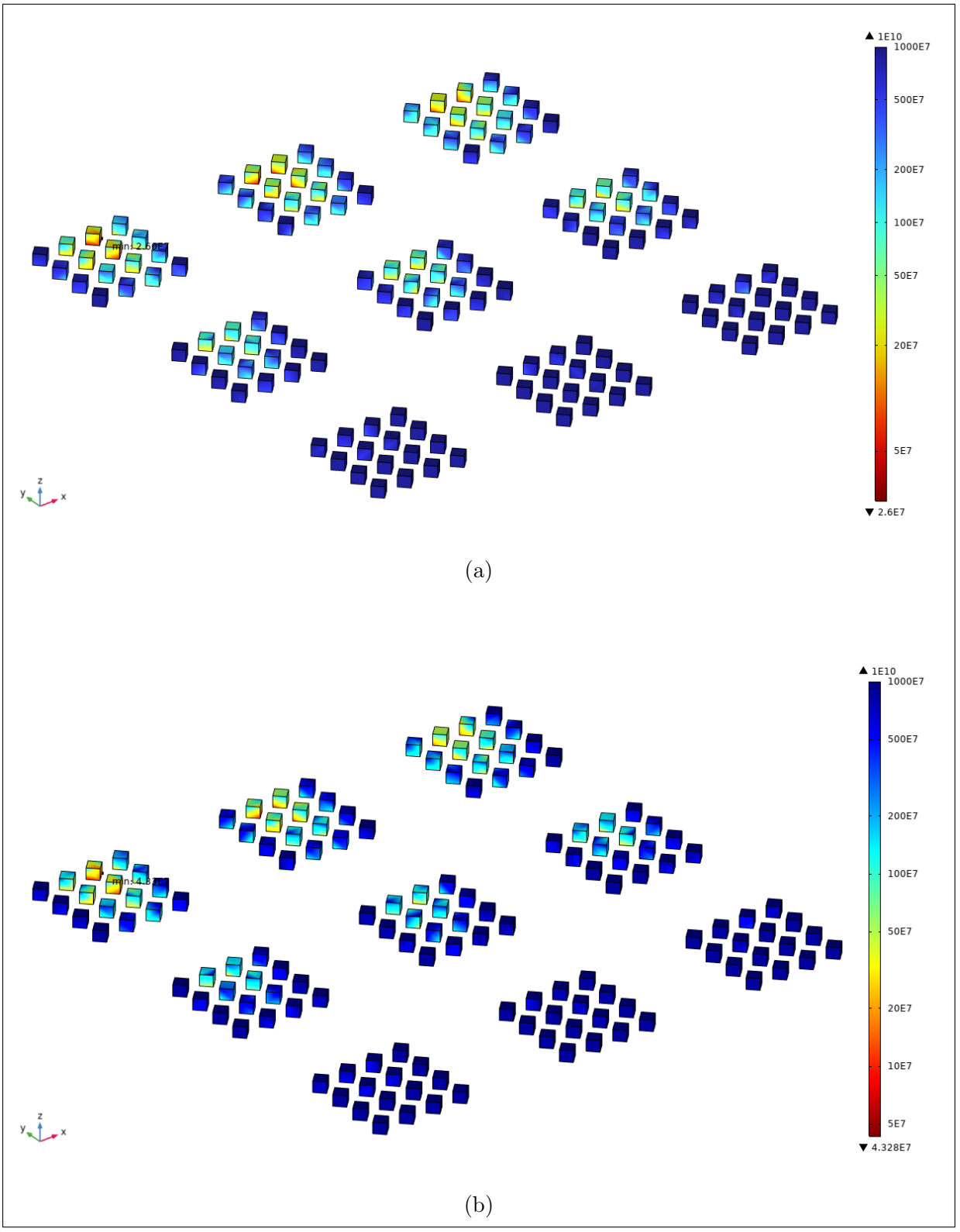


FIGURE 4.26: Coffin-Manson life cycle results for chip solders of MCM-BGA package equipped with (a) all-sided porous MCHS and (b) all-sided optimized porous MCHS.

Figure 4.22(a) displays the temperature distribution of the initial heating phase at t=18 seconds. It is evident from the contour that the temperature throughout the body remains constant, reflecting the ambient temperature conditions at 293 K. A similar pattern is observed for the stress distribution for the initial heating phase, as shown in Figure 4.23(a).

Figure 4.22(b) shows the temperature distribution during the high heating phase at t = 1440 seconds. The contour indicates a more pronounced temperature gradient in regions surrounding IC chips and chip solders, with the maximum temperature increasing to 318 K. The stress contours shown in Figure 4.23(b) exhibit a similar behavior where maximum stress at the solders near the outlet increases from 0.081 MPa to 8.51 MPa at peak loading.

Figure 4.22(b) demonstrates the temperature distribution during the startup of the ramp-down period at t = 14580 seconds. The maximum temperature within the load cycle slightly reduces from 318 K to 314 K. Moreover, the stress contours shown in Figure 4.24(a) at this time show the reduction in the solders' maximum stress from 8.51 MPa to 6.32 MPa.

Figure 4.22(d) represents temperature distribution towards the dwell period at the end of the first load cycle at t=18000 seconds, with the maximum temperature reducing to 309K before the onset of the next load cycle. The corresponding stress contours in Figure 4.24(b) at this time step show the solders' maximum stress reduction to 4.15 MPa.

Cycles to failure value is the critical parameter for evaluating the reliability of any electronics package. After studying the stress distribution, it was found that it was found that stresses within the package were mainly concentrated over the chip solders. The Coffin-Mansion Manson and Darveaux methods were used to investigate the fatigue life of the chip solders, considering them as viscoplastic.

Figures 4.25 and Figure 4.26 represent the cycles to failure computed from the Coffin-Manson method for the chip solders for the configurations of baseline MCM-BGA package, MCM-BGA package integrated with conventional MCHS, and MCM-BGA

package integrated with all-sided porous MCHS and MCM-BGA package integrated with optimized porous MCHS respectively. The figures reveal that the lowest life cycle mainly exists for chip solders near the outlet of the mid-channel, whereas the soldiers near the inlet have a larger life span. Therefore, the minimum cycles to failure for the chip solders at the outlet, which experiences a large temperature gradient, evaluated by the Coffin-Manson and Darveaux method, as shown in the Figure. The bar graphs in Figures 4.27(a) and (b) indicate that the package integrated with optimized porous MCHS shows a lower tendency to reach failure when compared to other configurations.

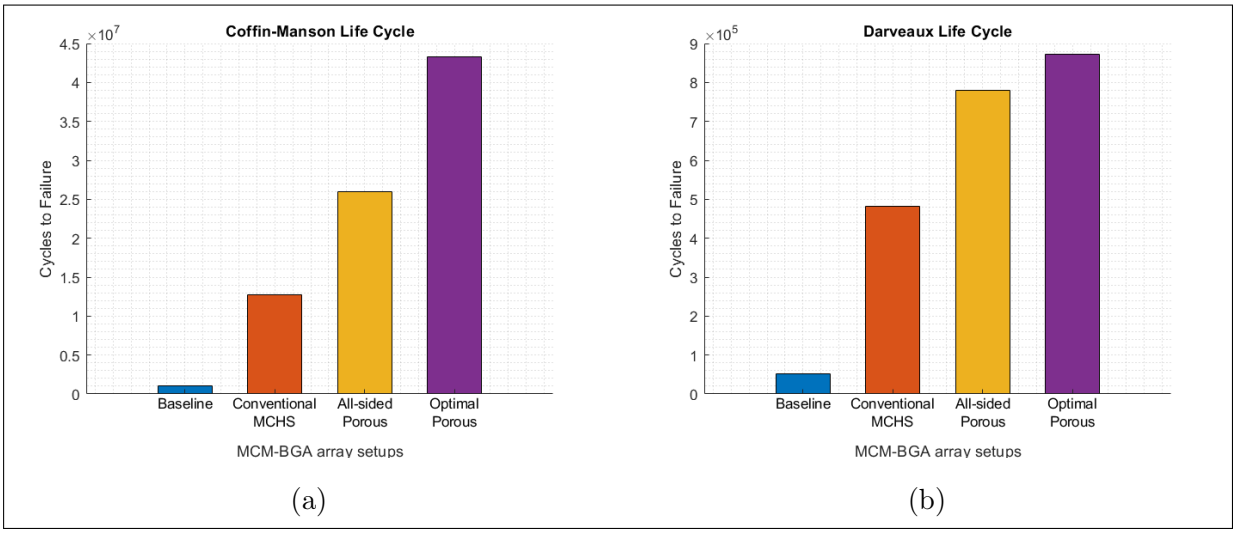


FIGURE 4.27: Predicted cycles to failure for various configurations using (a) the Coffin-Manson model and (b) the Darveaux model.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

The goal of the thesis is to develop a novel cooling solution for the thermal management of the MCM-BGA package. In this regard, different configurations of the MCM-BGA package, integrating only heat spreader, add-on conventional MCHS, and add-on porous MCHS with different porous layouts, were designed and investigated using COMSOL Multiphysics. The BGA package configuration with an all-sided porous MCHS, which demonstrated superior thermal and structural performance, was further optimized using the Nelder-Mead optimization algorithm. To determine the reliability performance of the package under transient loading density, Coffin Manson and Darveaux methods were employed to predict the life cycles to failure of chip solders as they exhibited a maximum stress value in the whole package. The main findings of the research work are detailed as follows:

- The conjugate heat transfer (CHT) computational analysis performed for different setups revealed that the BGA package equipped with conventional MCHS significantly reduces 50 degrees from the hotspots compared to the baseline

configuration comprising only the heat spreader. The utilization of both vertically and horizontally porous MCHS led to a reduction of 55 degrees in temperature. In contrast, the utilization of all-sided porous MCHS led to a total reduction of 58 degrees compared to the baseline configuration, representing a 14.25% improvement in temperature reduction from hotspots.

- The thermo-structural computational analysis revealed that maximum stresses are generated in the chip solders located near the outlet, while stresses developed in other components are relatively insignificant. Moreover, the study showed that the BGA package equipped with conventional MCHS significantly reduces maximum thermal stress by 104 MPa from the chip solders compared to the baseline package. The utilization of both vertically and horizontally porous MCHS led to a reduction of 117 MPa in thermal stress values. In contrast, the utilization of all-sided porous MCHS led to a total reduction of 125 MPa compared to the baseline configuration, representing a 51.7% improvement in maximal stress reduction from chip solders.

- The optimization to improve FOM using the Nelder Mead optimization algorithm yielded solid thickness and porous thickness values of 0.429 mm and 0.0849 mm, respectively. The optimized configuration of MCHS, when integrated with the package, improved FOM and heat transfer coefficient by 10.7% and 23.8%, respectively, at a Reynolds number of 700.

- To determine the structural integrity of the critical solders, Fatigue life cycle analysis was conducted using Coffin-Manson and Darveaux models for packages equipped with baseline, conventional MCHS, all-sided porous, and optimized porous MCHS. The analysis revealed the optimal porous setup outperforms and exhibits a maximum increase in the value of cycles to failure.

5.2 Future Works

In the near future, the present research work can be expanded to develop new novel thermal management solutions for electronic packaging by integrating one or more of the techniques mentioned below:

- Utilizing the nano-fluid, liquid metals, and phase-changing materials as a coolant within MCHS.

- Using a graphene-based heat spreader or vapor chamber heat spreader in place of a copper heat spreader.

- Conducting thermal cycling tests where the MCM-BGA package is exposed to rapid temperature changes to simulate environmental stress conditions.

- Performing vibration and shock testing to determine how the MCM-BGA array withstands mechanical stresses induced by random vibrations or shock impacts.

- Performing microstructural characterization of solder materials and intermetallic compounds to understand failure mechanisms better and optimize material choices.

- Conducting multi-objective optimization of the entire package to improve thermo-hydraulic performance and reliability, considering variable fin designs and hybrid porous structures within MCHS.

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