“CALIBRATED HIGH PERFORMANCE PROGRAMMABLE LOW DROP OUT VOLTAGE REGULATOR FOR PHY DRIVERS”

A Thesis Submitted in Partial Fulfillment of the Requirement for the Award of the Degree of

Master of Technology

In VLSI DESIGN

Submitted By

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JUNE, 2018

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Date: June 08, 2018

CERTIFICATE

This is to certify that Harpreet Singh, Registration No. 601662008, a student of M.Tech (VLSI Design), Thapar Institute of Engineering and Technology, Patiala has successfully completed one year (August 2017 – June 2018) internship programme in INTEL TECHNOLOGY INDIA PVT. LTD. His title of dissertation is **"CALIBRATED HIGH PERFORMANCE PROGRAMMABLE LOW DROP-OUT VOLTAGE REGULATOR FOR PHY DRIVERS"**

During the period of his internship programme, he was punctual and hardworking.

I wish him every success in life.

Sunil Kumar C R
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DECLARATION

I, **Harpreet Singh,** hereby declare that the thesis entitled **"CALIBRATED HIGH PERFORMANCE PROGRAMMABLE LOW DROP OUT VOLTAGE REGULATOR FOR PHY DRIVERS"** in fulfillment of the requirement for the award of degree of Master of Technology in VLSI DESIGN submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Alpana Agarwal,** HECED, from June 2016 to June 2018. The matter presented in this thesis has not been submitted either in part or full to any other university or institute for the award of any other degree.

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Date: 13-06-2018

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It is certified that the above statement made by the student is correct to the best of my knowledge and belief.

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ACKNOWLEDGEMENT

It is my proud privilege to acknowledge and extend my gratitude to several persons who helped me directly or indirectly in completion of this report. I express my heart full indebtedness and owe a deep sense of gratitude to my guide **Dr. Alpana Agarwal, HECED Thapar Institute Of Engineering & Technology**, for her sincere guidance and support with encouragement to go ahead. I would like to thank my manager, **Er. Sunil Kumar, Circuit Design Manager, Intel Technology India Pvt. Ltd, Bangalore**, for his valuable suggestions, feedback and persuasion to do something new and challenging and to give freedom to work in my way.

I would like to thank my mentor **Er. Ragvendera Kulkarni, Analog Design Engineer, Intel Technology India Pvt. Ltd, Bangalore and all team members** for great support to learn basics and give me a proper guidance and extended support in my difficult time.

I am also thankful to my hiring manager **Mr. Giridhar Bajpe, Sr. Manager DCG India Planning & Operations, Intel, Bangalore** for his regular motivation and inspiration and that triggered me for the work. I would like to thanks my sister **Amandeep Kaur, Research Scholar, IIT Delhi** for acting like my tutor and clearing my doubts.

I would also like to thank to **Dr. R.S. Kaler (Deputy director, Thapar University, Patiala), Dr. S.S. Bhatia (DOAA, Thapar University, Patiala)** for allowing me to do an internship and carrying out my thesis work at **Intel Technology India Pvt. Ltd. Bangalore.**

Last but not the least, I would like to thank my parents for their years of unyielding love and encourage. They have always wanted the best for me and I admire their determination and sacrifice.

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ABSTRACT

A calibrated high performance programmable low drop out (LDO) regulator for PHY drivers, is presented in the thesis. The designed LDO is capable of generating five different regulated voltage levels, starting from 400mV to 600mV, with a level increment of 50mV and has the capability to drive up to 40mA current. These voltages are generated corresponding to five different reference voltages applied at the input of error amplifier. For generating reference voltages, resistive ladder is employed. The normal resistive ladder tapping points give voltages which show variations of about $\pm 20\%$ with respect to original value. Calibration of LDO helps in reducing this variations to as low as $\pm 5\%$.

The proposed LDO has been designed and simulated on 10nm CMOS technology process. Compensation technique employed for stability helps in settling the response within 23ns. Compensation technique employed for leaker current makes our LDO to work under two different ranges i.e. from no-load to 2.5mA and from 2.5mA-40mA. Usage of this compensation technique helps in reducing the leaker current up to 1.5 times. During driving PHY drivers with voltage power supply of 0.4V, provided by our LDO, common mode noise of less than 12mV is noted. The working input frequency of driver is 4.5 GHZ. The differential voltage levels varies from -205.6 mV to 206 mV and alternating current in range 1.991 to 2.19 mA flows through the output resistance of driver.

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CHAPTER 1

INTRODUCTION

Low drop-out regulator (LDO) is a kind of linear voltage regulator which controls the voltage and current using transistor as variable impedance elements. It is commonly used in portable equipment due to low noise and fast transient response. Due to its usage in portable devices, the operating voltage of LDO also needs to be low and thus resulting in low quiescent current and low leaker current requirement. In this chapter, voltage regulator and its types are studied. The basic introductory part of LDO and various mathematical equations involved with it are also discussed. The different components of LDO are also explained. The block diagram level working of LDO is also studied in this chapter. After discussing about various pros and cons of LDO, some of important parameters of LDO and their dependence upon different elements of LDO are introduced. In last section the literature review that we have done regarding LDO is mentioned.

1.1 VOLTAGE REGULATORS

Whenever, there is requirement to produce a constant and regulated voltage, under those conditions a special circuit known as voltage regulator is opted for. In order to achieve the regulation process, voltage regulator may use an open loop configuration or it may use a closed loop configuration. If the configuration employed is a closed loop, then it must be a negative feedback mechanism. Regulators can be used for regulating electrical signal or it may be used to regulate electronic signals. Depending upon the requirement, it can be used to regulate multiple AC or DC voltages. Basically, voltage regulator is of two types:-

1. Linear Voltage Regulator
2. Switching Voltage Regulator

1.1.1 Linear Voltage Regulator

Under this type of voltage regulator, there is a presence of pass element, whose conductance varies in order to achieve the regulated output voltage. Low drop out voltage regulator is an example of Linear Voltage regulator. It is further of two types:-

1. Series Voltage Linear Voltage Regulator
2. Shunt Voltage Linear Voltage Regulator

1.1.1.1 Series Voltage Linear Voltage Regulator

In case of Series Voltage Linear regulators, the pass element, which is acting as a variable element is presented in series with the load. In order to achieve a proper regulation, the conductance of series element varies with respect to variations in the output voltage and thus overcome the variations and we get a regulated voltage at the output node. It is shown in Figure 1.1.

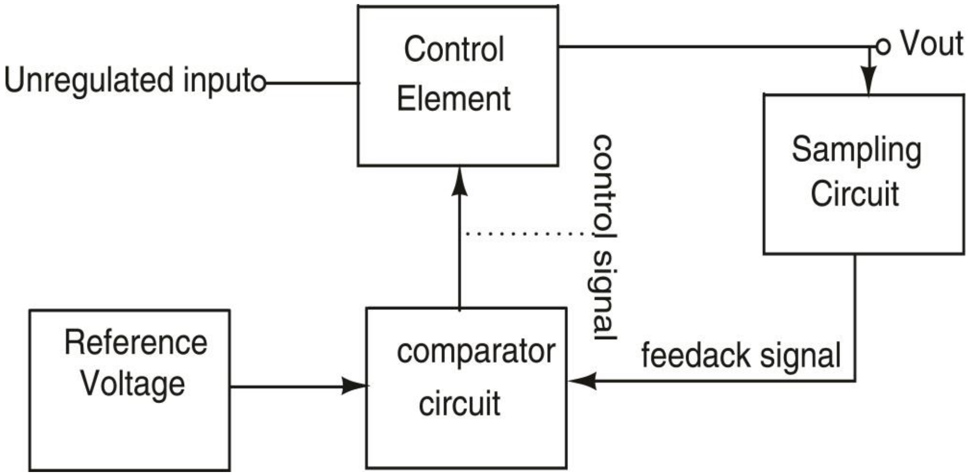

Figure 1.1 Block description of series voltage linear regulator

1.1.1.2 Shunt Voltage Linear Voltage Regulator

Under this type of Linear Voltage Regulator, the pass element, which is acting as a variable element is presented in shunt with the load. In order to produce regulated voltage at the output, the conductance of shunt path varies with respect to variations in the output and thus allowing extra current to pass through it. Whenever load current at the output increases, the shunt path allows the extra current to pass through it to ground and it blocks the current, whenever the load current decreases. It is shown in Figure 1.2.

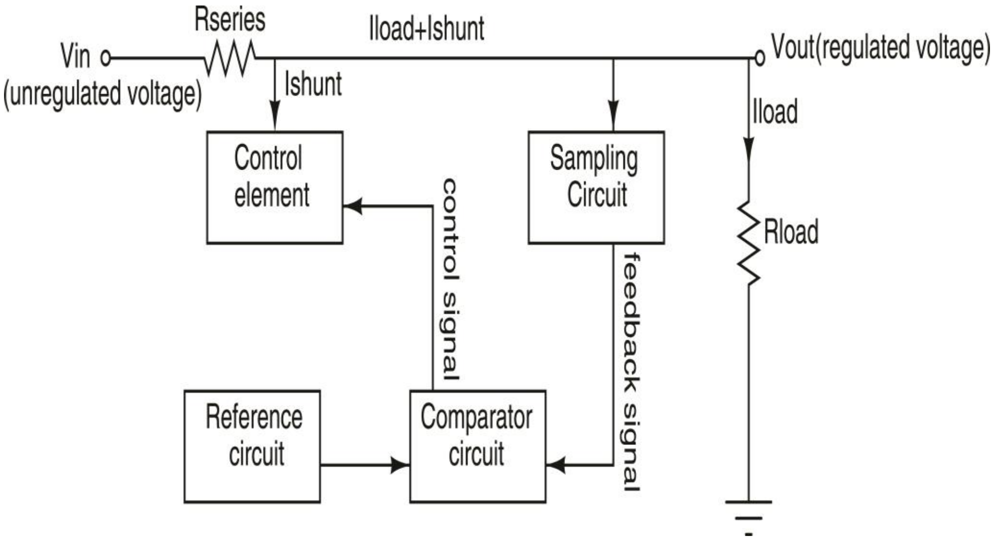

Figure 1.2 Block description of shunt voltage linear regulator

1.1.2 Switching Voltage Regulator

It is a type of voltage regulator, in which a series element is presented, which act as a variable element. The instances of series elements are rapidly made to be switched on or off, in order to produce regulated voltage. Switching power dissipation takes place in such type of regulation process. It is also of two types:-

1. Step-up Voltage Regulator
2. Step-down Voltage Regulator

1.1.2.1 Step-up Voltage Regulator

Whenever, there is a requirement of higher output voltage, provided the circuit is fed with lower voltages, then under those condition, Step-up Voltage regulator is opted for. It is also known as boost up circuit. It is shown in Figure 1.3.

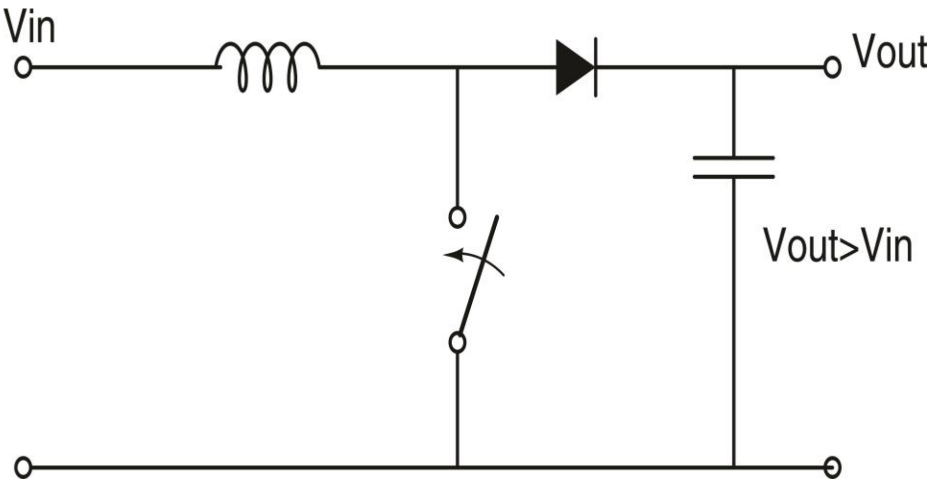

Figure 1.3 Step-up voltage regulator circuit

1.1.2.2 Step-down Voltage Regulator

Whenever, there is a requirement of lower output voltage, provided the circuit is fed with higher voltages, then under those condition Step-down Voltage Regulator is opted for. It is shown in Figure 1.4.

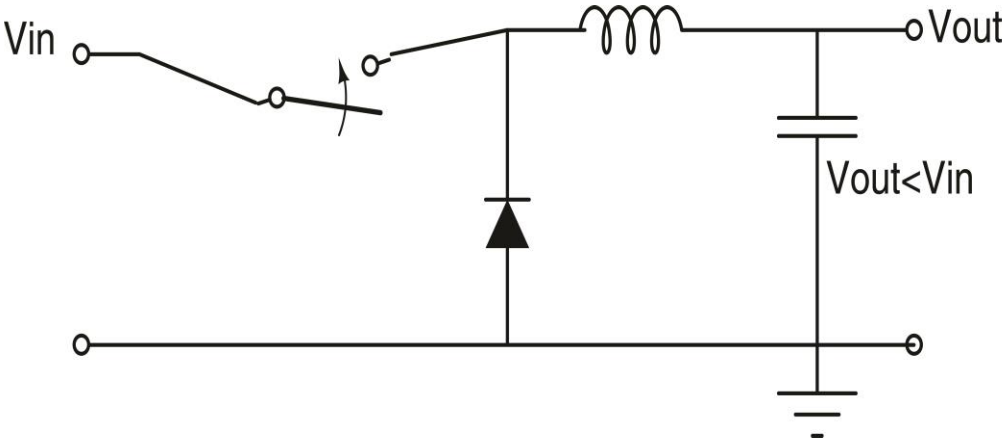

Figure 1.4 Step-down voltage regulator circuit

1.1.3 LDO

LDO is an abbreviation for Low Drop out Voltage regulator. If the output voltage which is needed to be regulated is very close to the input supply voltage, then under those conditions LDO is used. Low Drop out Voltage regulator is very easy to design consists of few components and is very economical. LDO which is generating a DC supply for system on chip requires a wide range of current, so during designing of LDO, these specifications are taken into consideration. The basic structure of LDO is shown in Figure 1.5.

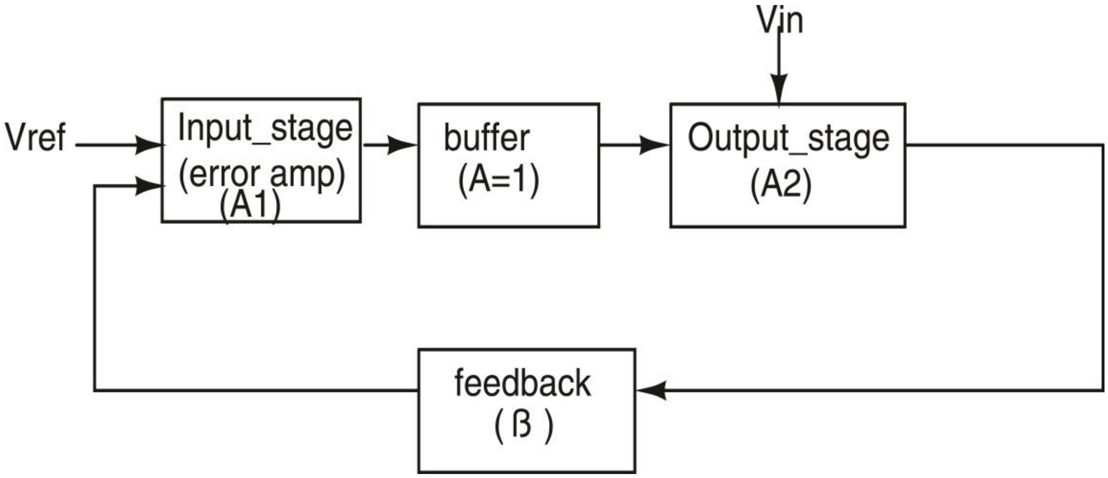

Figure 1.5 Basic LDO circuit

In order to fulfill high range of current, the size of pass element transistor needed to be very large which means area requirement is also more. This means there is a tradeoff between area and the current needed to drive the output load. Various compensation techniques are needed for stability and calibration techniques are needed for generating reference voltages. Overall power dissipation in LDO is very high, so there is a need of introducing some new circuit to our LDO for reducing power dissipation. In order to reject the ripples, coming from power supply, power supply rejection ratio and line regulation parameters are needed to be improved. Load regulation should be least, so that with variations in load, the output voltage remains fixed and regulated. Low drop out voltage regulators are used widely in mobile systems and transmitters.

Based on the Figure 1.5, the output voltage derived is given by:-

$$\mathrm{V_{out}} = \frac{\mathrm{V_{ref}A_1A_2}}{1+\mathrm{A_1A_2}\beta} + \frac{\mathrm{V_{in}}}{1+\mathrm{A_1A_2}\beta} \approx \frac{\mathrm{V_{ref}}}{\beta} + \frac{\mathrm{V_{in}}}{\mathrm{A_1A_2}\beta} \tag{1.1}$$

The output voltage depends upon the open loop gain. So, our output to remain constant, even with the change in load, then open loop gain of our error amplifier should be made as large as possible. For calculating transfer function of LDO its signal flow graph is needed. Signal flow diagram of LDO is shown in Figure 1.6.

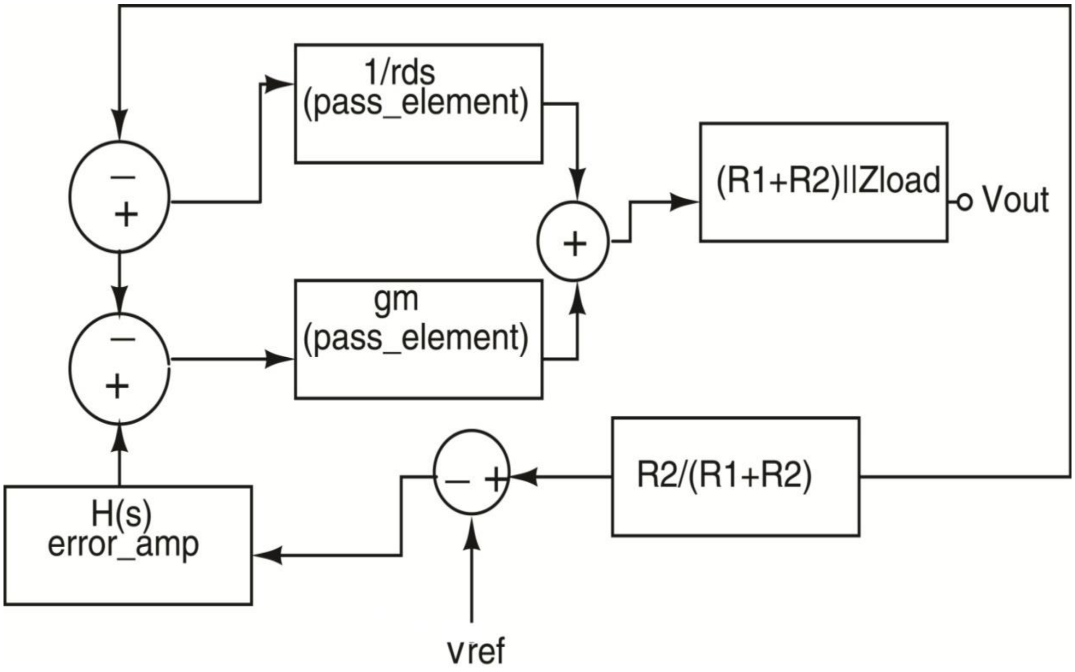

Figure 1.6 Signal flow diagram of LDO

The feedback topology employed by LDO is Series Shunt. This means that output impedance of our LDO should be as low as possible and the input impedance of our LDO should be as high as possible. Load regulation will improve with the decrement in output impedance. By changing feedback resistor values, output can be changed. Further we generally fix one of the feedback resistors and vary other resistor. Using KCL/KVL we can calculate transfer function and hence output voltage can be represented as:-

$$\mathrm{V_{out} = H_1V_{in} + H_2V_{ref}} \tag{1.2}$$

$$\mathrm{where\ H_1 = \frac{V_{out}}{V_{in}}\ and\ H_2 = \frac{V_{out}}{V_{ref}}}$$

$$\mathrm{\frac{V_{out}}{V_{ref}} = \frac{A_{ea}gm_{pass}r_{fl}}{1 + A_{ea0}gm_{pass}r_{fl}\beta + \frac{r_{fl}}{rds_{pass}}}} \tag{1.3}$$

$$\Rightarrow \mathrm{\frac{V_{out}}{V_{ref}} \approx \frac{1}{\beta}\ if\ A_{ea0}gm_{p}r_{fl}\beta \gg 1} \tag{1.4}$$

$$\mathrm{Now\ r_{fl} = (r_1 + r_2)||r_l}$$

$$\mathrm{and\ Z_l = r_l\ for\ DC}$$

$$\Rightarrow \mathrm{\frac{V_{out}}{V_{in}} = \frac{1 + gm_{pass}rds_{pass}}{1 + (A_{ea0}gm_{pass}rds_{pass}\beta + \frac{rds_p}{r_l})}} \tag{1.5}$$

$$\therefore \mathrm{\frac{V_{out}}{V_{in}} \approx \frac{1}{A_{ea0}\beta}\ if\ gm_{pass}rds_{pass} \gg 1} \tag{1.6}$$

1.1.4 Roles of LDO

Basically there are three roles that LDO should fulfill, in order to do regulation process efficiently:-

1. Ripple suppression
2. Isolation
3. Low Noise.

Before discussing these roles, let's discuss how power management system looks like. The basic power management system is as shown in Figure 1.7.

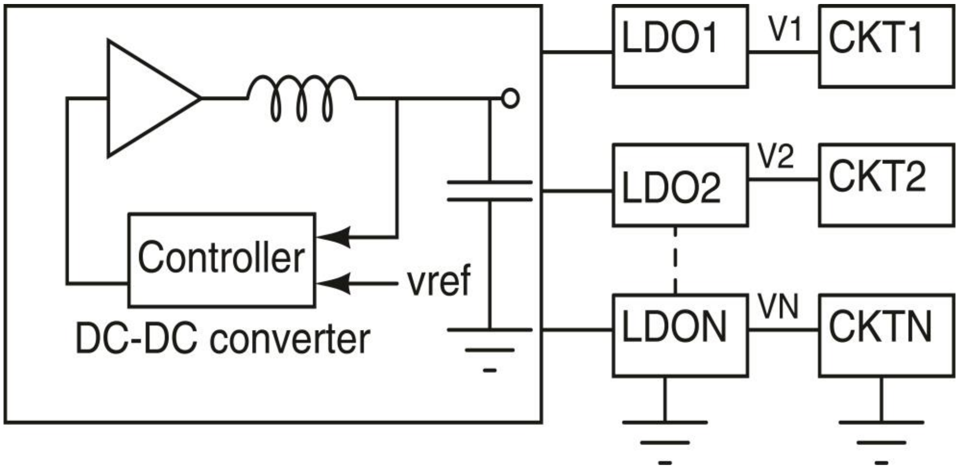

Figure 1.7 Basic power management systems

1.1.4.1 *Ripple Suppression*

Power supply to LDO is provided mainly by DC-DC converters. Power supply provided by the converter, has ripples. LDO should be designed in such a way that the effects of ripples remain negligible at the output. In case of analog, mixed or RF signal, power supply rejection is very important parameter to be analyzed.

1.1.4.2 *Isolation*

Sometimes, situation arises, in which large switching activity takes place at the circuit level. Such a huge switching activity, may affect the performance of DC-DC converter. LDO should act as an isolator between these two stages i.e. between circuit, which is being derived by the LDO itself and the DC-DC converter and avoid coupling of noise between these two stages.

1.1.4.3 Low noise

LDO should provide a noise free output, even though input has a lot of noise in it.

Now talking about, main difference between LDO and non LDO regulators, then non-LDO regulators use emitter/source follower topology, whereas LDO uses open collector or open drain topology. In the open collector topology, transistor may be easily driven into saturation region with the available voltages to the regulator. Due to this advantage, voltage drop from the power supply gets reduced to as low as the voltage require to place the device in saturation that is voltage drop will remain equal to overdrive voltage. When we talk about pass element, then if the difference between input and output voltages is less, we go for either PMOS or NMOS device. On the other hand, if the difference between input voltage and the output voltage required is more, then under those conditions, we select PNP or NPN transistors as a pass element. Voltage drop across BJT's transistors is more as compare to MOSFET transistors.

1.1.5 Advantages and Disadvantages of LDO

There are number of advantages as well as disadvantages of LDO. These are discussed in this section.

1.1.5.1 Advantages

- Switching noise is absent in LDO, as no switching action takes place during its operation.
- Very simple design.
- No need of transformers and inductors.
- Design is very economical.
- Consists of few components.
- Produce regulated output, even when the difference between input and output is very less.

1.1.5.2 Disadvantages

- More power dissipation.

- Need separate circuit for stability compensation.
- Calibration is needed for producing reference voltage.
- There is a tradeoff between driving capability of LDO and chip area.

1.1.6 Components of LDO

LDO consists of four main components as shown below:-

1. Error amplifier
2. Reference Voltage source
3. Pass element
4. Feedback network

1.1.6.1 Error Amplifier

It is basically a cascade connection of differential amplifier, with common source amplifier. This error amplifier is used to generate a signal at its output, after comparing its two input signals, the reference voltage source signal and the feedback signal. Depending upon the difference between two signals, the conductance of pass element is going to vary. The second stage in the cascaded connection is of common source amplifier. This amplifier, combine with differential amplifier, provide with good overall gain. For precise LDO operation, basic expectation from two stage cascaded amplifier is good input common mode voltage, PSRR and gain. Looking with respect to common mode input requirement, if common mode input range is a low voltage range, then under those condition, PMOS input pair and NMOS pair as a load for differential amplifier is a good combination, and if the common mode input requirement is a higher voltage range value, then under those condition NMOS input pair and PMOS pairs as a load of differential amplifier combination will be a good option. Looking with respect to power supply rejection ratio, then PMOS input pair differential amplifier provide good PSRR as compare to NMOS input pair, for the same input pair size. PMOS input pair provides more output impedance, as a result of which any change in the supply voltage, doesn’t appear at the output. NMOS input pair provide very low output impedance, which results in the appearance of almost entire ripples across the output. Mathematically it is as shown below:-

$$\frac{V_{out}}{V_{dd}} = -G_M R_{out} \tag{1.7}$$

$$R_{out} = (rds_2||rds_4)$$

$$i_{out} = 2i_x + \frac{V_{dd}}{rds_4}$$

$$i_x = gm_1 rds_1 \frac{1}{gm_2} + rds_2 \approx 2rds_1$$

$$\Longrightarrow i_x = \frac{V_{dd}}{\frac{1}{gm_3} + 2rds_1} \approx \frac{V_{dd}}{2rds_1}$$

As $G_M^{-1} = (rds_1||rds_4)$

and $rds_1 = G_M^{-1}$

$$\therefore \frac{V_{out}}{V_{dd}} \approx 1 \tag{1.8}$$

1.1.6.2 Reference Voltage Source

One of the inputs of error amplifier is connected with the reference voltage source. The signal generated by the reference voltage source is compared with the feedback signal to generate output signal. Resistive ladder or band gap reference (BGR) can be used for reference purposes. Resistive ladder consumes more power, more chip area and difficult to fabricate, whereas BGR on the other hand consumes less power and can be fabricated easily, but it requires a BJT, which is not available in 10nm technology. So in our work, we will design a resistive ladder. The output of LDO depends upon the reference voltage. Mathematically, it is as shown below:-

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right) \tag{1.9}$$

where R_1 and R_2 are the feedback resistors.

1.1.6.3 Pass Element

It is one of the most important components of LDO. Earlier bipolar junction transistors were used as a pass element, but now a day's PMOS or NMOS is being used widely as a pass element. Whenever the difference between input and output voltages is less, we go for either PMOS or NMOS device. On the other hand, if the difference between input voltage and the output voltage required is more, then under those conditions, we select PNP or NPN transistors as a pass element. Bipolar junction transistor consumes lots of power, as large amount of voltage drop occur across it. Chip area, needed for BJT is also more as compare to FET. So for all these reasons, FET's are being preferred than BJT's as a pass element. Again there are number of advantages and disadvantages of using PMOS and NMOS as a pass element. NMOS devices require a positive drive signal with respect to output while PMOS devices required a negative signal with respect to input. Generating a positive drive signal becomes difficult at low input voltages, as a result of which the LDO's which are designed to regulate lower voltages are implemented using PMOS as a pass element. Further LDO's with PMOS as a pass element is free from body effect, this is again a positive point of using PMOS as a pass element.

1.1.7 Working of LDO

The basic working diagram of LDO is shown in Figure 1.8. From the Figure 1.8, it is clear that it consists of error amplifier, pass element, feedback resistors and reference voltage source as its main components. Error amplifier consists of two input signals. One of them is generated by reference voltage source and another one is the feedback signal, which is being fed back to error amplifier by the feedback element. Actually, only a part of output signal is fed back to error amplifier, in our work we are feeding back half of the output signal. So, whenever there occur some variations in the output voltage, same variations will be fed back to error amplifier and will appear across the input of error amplifier. Now based on the two input signals, error amplifier produces a strong or weak signal. Suppose due to some ripples in the input supply, the output voltage is increased. Now the voltage which is being fed back to error amplifier is also increased. When error amplifier compares two input signals, then it will produce more positive or strong signal at its output, which is driving the pass element. Basically, we are using PMOS as a pass element, so with a positive high signal at the output of error amplifier, or at the input of pass element, the driving capability of PMOS pass element will decrease. Due to decrement in the conductance of pass element, the extra voltage, which early being appeared at the output, will be dropped across pass element, making the output voltage to become regulated.

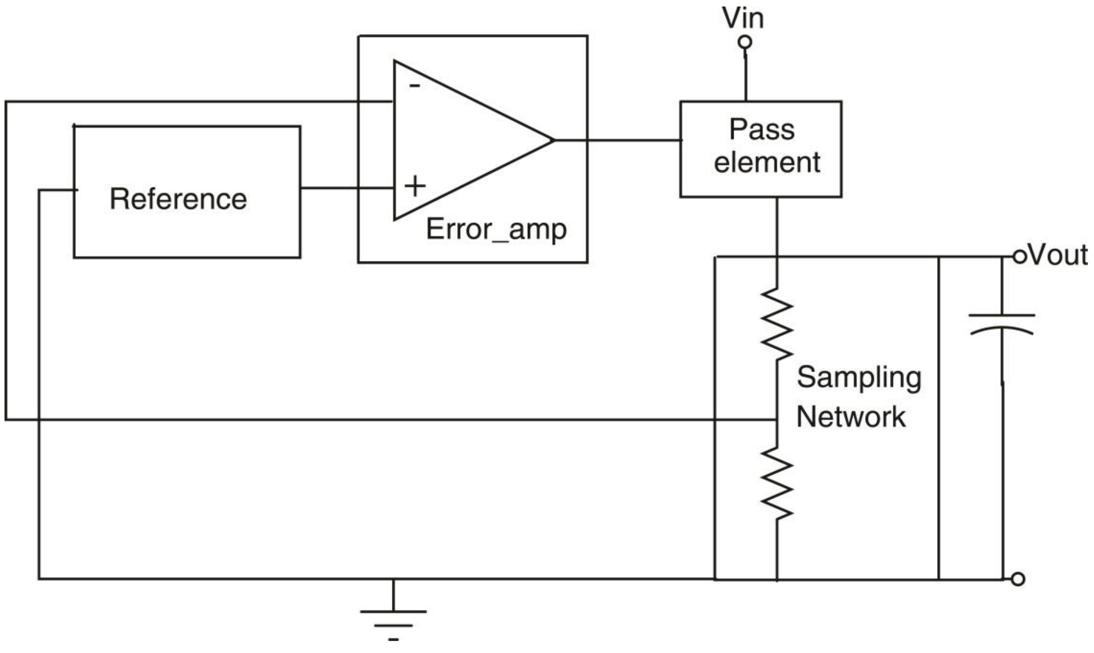

Figure 1.8 Working block level description of LDO

1.1.8 Specifications of LDO

There are number of parameters, which are needed to be specified, for the proper working of LDO. We will discuss them one by one. Metric performance of LDO is shown in Figure 1.9.

1.1.8.1 Line Regulation

It is the LDO's ability to maintain the output voltage regulated, even when there occur some variations in the supply voltage. It is the steady state parameter and hence is measured at zero frequency. By steady state parameter, we mean if the V_{IN} changes the output remains stuck to a fix value. For example, if V_{IN} changes from 1 to 1.2V and at 1.2V, the output is becoming constant, and then we have to do analysis for 1.2V. Mathematically, it is as shown below:-

$$\text{Line regulation} = \frac{\Delta \text{Vout}}{\Delta \text{Vin}} \tag{1.10}$$

It should be as small as possible. Increasing open loop gain improves line regulation. It is specify in mV/V. As already discussed, LDO's transfer function is given by:-

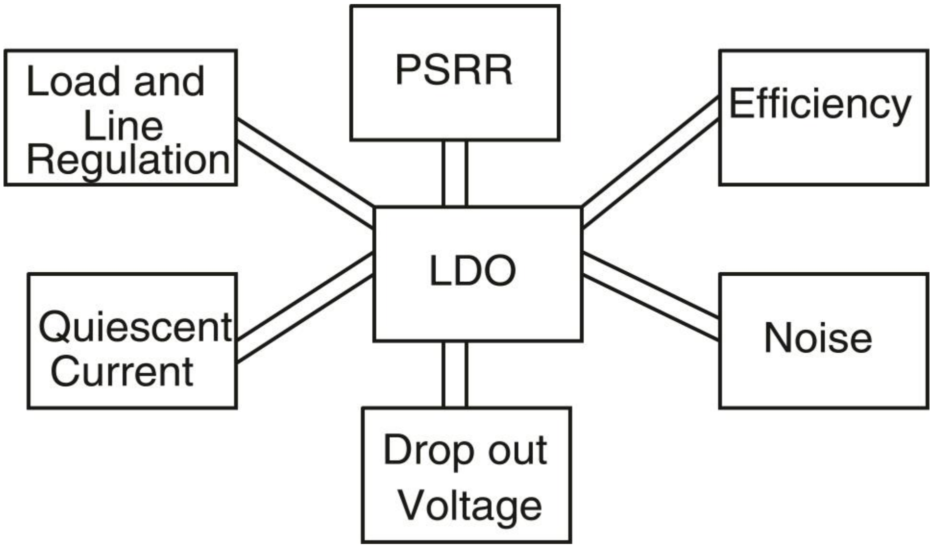

Figure 1.9 Metric performance of LDO

$$\frac{V_{out}}{V_{in}} = \frac{1+gm_{pass}rds_{pass}}{1+(A_{ea0}gm_{pass}rds_{pass}\beta+\frac{rds_p}{r_l})} \tag{1.11}$$

$$\Rightarrow \frac{V_{out}}{V_{in}} \approx \frac{1}{A_{ea0}\beta} \text{ if } gm_{pass}rds_{pass} \gg 1$$

$$\Rightarrow \text{Line regulation} = \frac{\Delta Vout}{\Delta Vin} \approx \frac{1}{A_{ea0}\beta} \quad (1.12)$$

Hence, for improving line regulation, open loop DC gain should be increased i.e. variations in V_{IN} can be suppressed by increasing error amplifier open loop gain. Output voltage variations after considering error amplifier variations along with offset voltage variation and reference voltage variations is given by:-

$$\Delta Vout = \frac{\Delta V_{in}}{A_{ea0}\,\beta} + \frac{\Delta V_{ref} + \Delta V_{os}}{\beta} \quad (1.13)$$

Variations in V_{IN} will be suppressed by error amplifier gain, but variations due to reference voltage and offset voltage drift of error amplifier will be amplified by $1/\beta$ factor. Point to be noted here is that, there is a trade of between error amplifier variation suppression and the variations due to offset voltage and reference voltage.

1.1.8.2 Load Regulation

It is the ability of LDO to maintain output voltage even with the variations in load. Like line regulation, it is also a steady state parameter and hence, measured at zero frequency. By steady state we mean, we are going to calculate this parameter at which the output voltage become constant, irrespective of variations in load current. Worst case occurs when load current varies from no load to maximum rated value. In our case it is in between 0-40mA. Mathematically, it is as shown below:-

$$\text{Load regulation} = \frac{\Delta V_{out}}{\Delta I_{out}} \quad (1.14)$$

In order to find out, load regulation, apply a small current at output and check how much output varies. The circuit diagram for deriving its formula is shown in Figure 1.10.

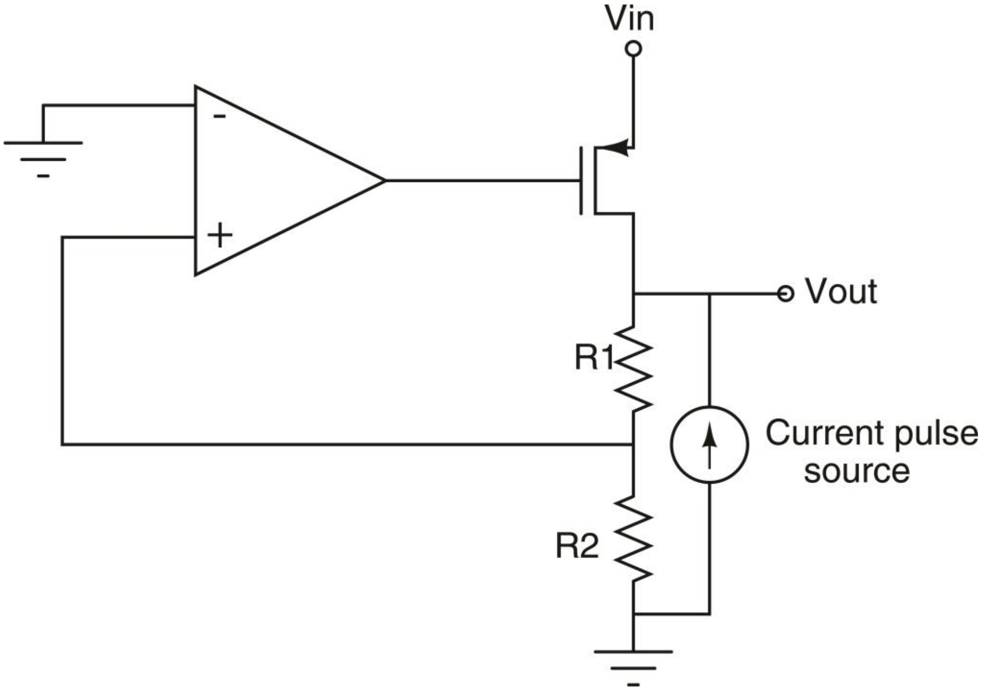

Figure 1.10 Circuit diagram for deriving load regulation

$$\Delta I_{out} = \frac{\Delta V_{out}}{[rds_{pass}||(R_1 + R_2)]} + \Delta V_{out}\beta A_{ea0} gm_{pass}$$

$$\text{Load regulation} = \frac{rds_{pass}||(R_1+R_2)}{1+A_{ea0} gm_{pass}\beta[rds_{pass}||(R_1+R_2)]}$$

$$\Rightarrow \text{Load regulation} \approx \frac{rds_{pass}}{1 + T_0} \qquad (1.15)$$

where T_0 is the open loop transfer function.

From the equation 1.15, it is cleared that, load regulation also depends upon open loop gain. In order to improve load regulation, open loop gain of error amplifier should be increased. Output impedance also gets lowered by loop gain, which is again a bonus for good regulation process, as our LDO demand low output impedance and higher input impedance for proper regulation. Ideally, load regulation should be as low as possible and it is measured in μV/A.

1.1.8.3 Drop-out Voltage

Drop-out voltage is the voltage before which output voltage is no longer remains regulated. Every MOS device needs some voltage to turn on. So the difference between required input voltage to turn on the device and the regulated output voltage is the drop out voltage. Actually, it is the minimum voltage drop that our LDO required before producing a regulated output. Mathematically, it is given as:

$$V_{\mathrm{dropout}} = V_{\mathrm{in}} - V_{\mathrm{out}} \tag{1.16}$$

Every pass element has some on resistance, as shown in Figure 1.11. Due to the presence of on resistance, whenever some current starts to flow through pass device, then some voltage drop takes place across it. This voltage is the drop voltage of LDO. It depends upon the pass device and the load current. It should be as low as possible. Generally, it varies in the range of 0.1-0.5V. Improvement in drop out voltage is in tradeoff with power supply and load transient.

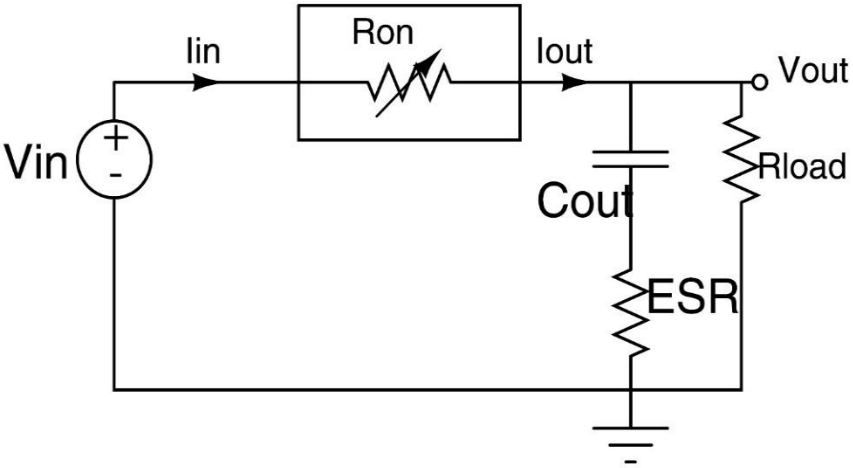

Figure 1.11 Circuit diagram for driving drop out voltage

1.1.8.4 *Load Transient Response*

It is the ability if LDO, to maintain its output voltage even with the variations in the load. It is similar to load regulation, but with a difference that load regulation is measured at the steady state whereas, load transient response is plotted for the entire frequency range. In terms of mathematical terms, it can be represented as:-

$$\text{Load regulation} = \frac{\Delta V_{\text{out}}}{\Delta I_{\text{out}}} \text{ at all frequencies.} \qquad (1.17)$$

It is a dynamic parameter. It depends on output capacitor, parasitic of output capacitor and on the internal compensation being employed for getting good stability performance. As output load current changes, correspondingly output voltage also changes. The variations in the output voltage are feedback to the error amplifier. Error amplifier always takes some time to compensate the output voltage variations. During this response time, spikes are induces at the output of LDO. A typical LDO is presented in Figure 1.12.

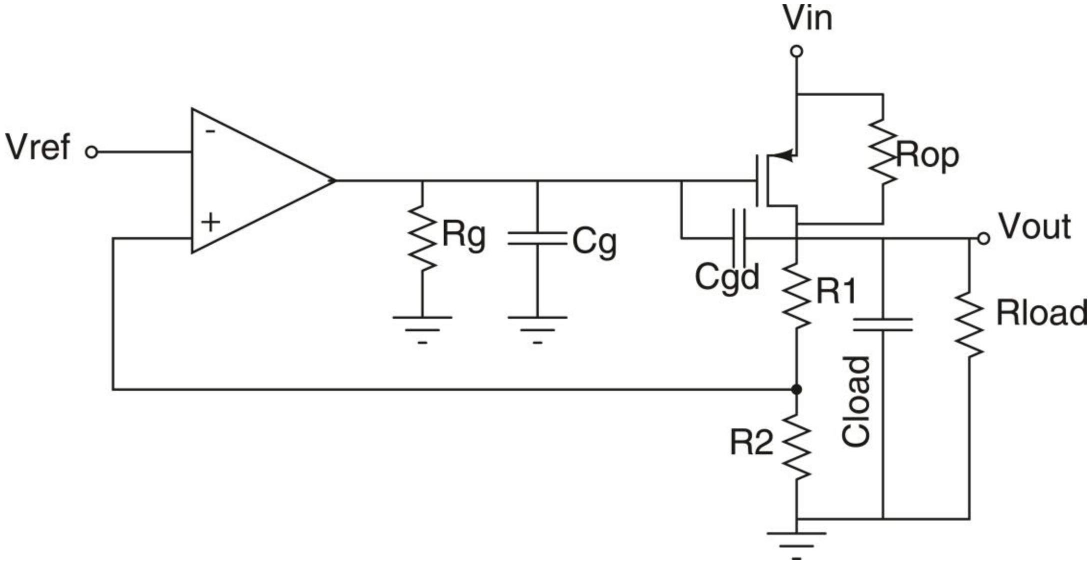

Figure 1.12 Typical LDO circuit with parasitic

The maximum peak value of such a spike is known as droop. Mathematically, it is given by

$$\text{Ripple voltage} = \mathrm{I} * \mathrm{ESR}_{\mathrm{total}} \tag{1.18}$$

The basic reason behind the origination of droop and thus spikes is the parasitic capacitance associated with the pass element. Due to these parasitic capacitors, delay is induced. In order to reduce the output error, delay should be reduced, which further depend upon the reduction of these parasitic

1.1.8.5 Quiescent Current

It is difference between input and the output current. It is mainly due to bias current in reference generator, error amplifier, feedback resistors and other support circuits. Mathematically, it is given by:-

$$\mathrm{I_q} = \mathrm{I_{in}} - \mathrm{I_{out}} \tag{1.19}$$

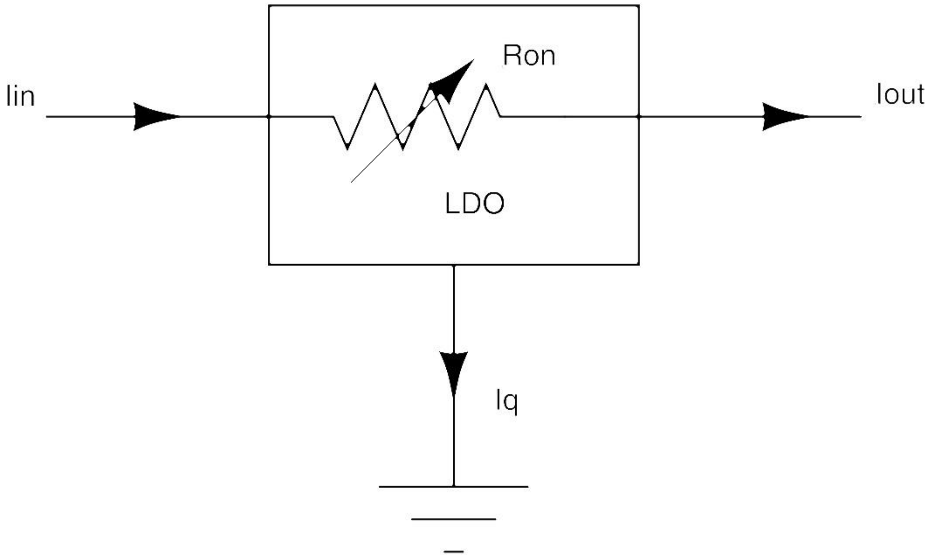

Figure 1.13 Circuit for deriving quiescent current

It is independent of load current, when the pass element being employed is a MOS device. In case of BJT, a quiescent current increase as it is a current driven device. For MOS, it is independent of load current MOS is a voltage driven device. Efficiency is also calculated in terms of quiescent current, as shown below:-

$$\eta = \frac{I_{out}}{I_{in}} * 100 = \frac{I_{out}}{I_{out} + I_q} * 100 \tag{1.20}$$

So, it should be as low as possible, in order to enhance the efficiency. Its value is usually determined by ambient temperature and the pass element.

1.1.8.6 PSRR

Power supply rejection ratio is the ability of regulator to maintain the output voltage to be constant, even with the ripples in the input supply voltage. It is similar to line regulation, but it includes all the frequencies i.e. it is not a steady state parameter and hence is measured with respect to frequency. It is measured for small signal variations. Mathematically, it is as shown below:-

$$\mathrm{PSRR}(f) = \frac{\Delta V_{out}(f)}{\Delta V_{in}(f)} \tag{1.21}$$

One of the major roles of LDO is to suppress the ripples at the output, present in the input supply. Ideally, we need no ripple at the output, so lower PSRR is preferred. Lower the current passing through pass element, lower will be PSRR. During calculation of PSRR, we consider the complete summation of ripples coming at the output via reference circuit, due to ripples in supply voltage coming at the output via pass element and due to ripples coming at the output from power supply via error amplifier. For lower frequencies, PSRR is high. PSRR in terms of gain is given as:-

$$\mathrm{PSRR} = 20 \log_{10} \frac{A_v}{A_{v0}} \tag{1.22}$$

where A_{v0}, is the open loop gain and A_v, is the closed loop gain.

Control loop is the dominant contribution of ripple rejection. Larger output capacitor and with low ESR, improves the PSRR performance. At low frequency, open loop gain is high, thus ripple rejection is very good. Afterwards gain starts to decline and thus our PSRR. PSRR is better for low load than higher load. Low load means, lesser current is driven from LDO. To reduce PSRR, it is necessary to maintain a proper speed response of error amplifier. For maintaining the speed, the bias current of error amplifier, cannot be reduced much. So, high PSRR with lower power is not possible with a standard LDO structure. Ripples come in LDO structure as the power supply is again generated by some other converter circuit. During the passage of voltage from DC to DC converter without ripple is almost an impossible task, so need of good PSRR. There are three regions of PSRR:- PSRR at low frequency, PSRR at medium frequency and PSRR at high frequency. Region first varies up to dominant frequency and open loop gain is high under this region and thus PSRR is good. Region second varies from dominant frequency up to UGB and open loop gain is lesser under this region and thus PSRR is lesser as compare to region first. In the third region, PSRR varies from UGB to higher frequencies and PSRR is lowest. PSRR at low frequency is given by:-

$$\mathrm{PSRR_{DC}} = \frac{1}{\mathrm{A_{ol-dc}}\beta} \tag{1.23}$$

From the above equation it is clear that, increasing open loop gain can improve PSRR at low frequency.

PSRR at mid frequency is given by:-

$$\mathrm{PSRR_{MF}} = \frac{1+\frac{\mathrm{S}}{\mathrm{BW_A}}}{(\mathrm{A_{ol}}\beta)(1+\frac{\mathrm{S}}{\mathrm{UGB}})} \tag{1.24}$$

At mid frequency, PSRR can be improved by high loop gain and by wide bandwidth amplifier. A variation at the output, due to variations or ripples in supply voltage is given by:-

$$\frac{\mathrm{V_{out}}}{\mathrm{V_{DD}}} = \left(\frac{1-\frac{\mathrm{V_{0A}}}{\mathrm{V_{DD}}}}{\mathrm{A_{ea}}\ \beta} + \frac{1}{\mathrm{rds_{pass}A_{ea}}\beta\mathrm{gm_{pass}}}\right) \tag{1.25}$$

where $\mathrm{V_{0A}}$ is the output voltage of error amplifier, $\mathrm{A_{ea}}$ is the gain of error amplifier, $\mathrm{rds_{pass}}$ is the ON resistance of pass element and $\mathrm{gm_{pass}}$ is the conductance of pass element. It is clear that under low frequency ripple rejection is more as gain at low frequency is more. At higher frequency greater than UGB, the internal gain is not able to reject ripple, for ripple rejection at higher frequency external capacitor is needed. Parasitic capacitor of pass element also helps in ripple rejection.

1.1.9 PHY Drivers

Drivers are just like a buffer used to pass the data it received, by enhancing the speed, and reducing the switching power. It does all the process without introducing any change to the original data. The basic flow of signal via driver is represented in figure 1.14

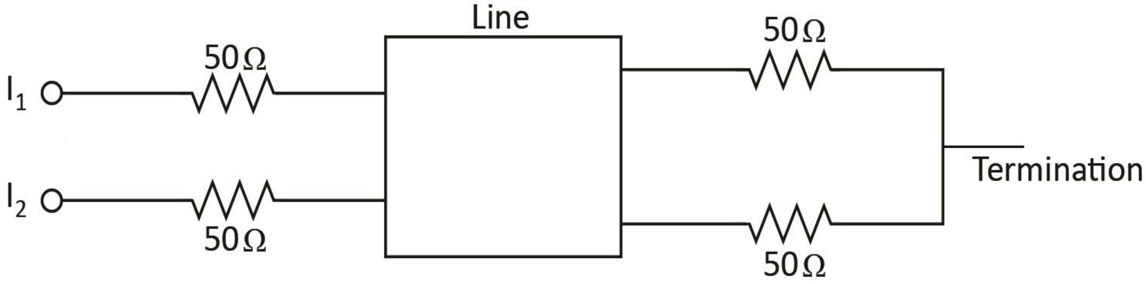

Figure 1.14 Basic signal flows through driver

It only changes the logic level of data input to it and hence saving power and improving speed. The word PHY is added to the drivers because it is connecting the transmitter to the physical world. The driver that we are using is calibrated for 50 ohms. Both the upper arm and the lower arm are made to design with MOS device and resistors. The block description of PHY driver is shown in figure 1.15. MOS devices and resistor values are selected in such a way that they both give a value close to the 50 ohms. 50 ohm resistance is the standard value of resistance which is being used for termination. So, in order to avoid reflection of signal, upper arm as well as lower arm of driver is designed to produce a resistance of 50 ohms.

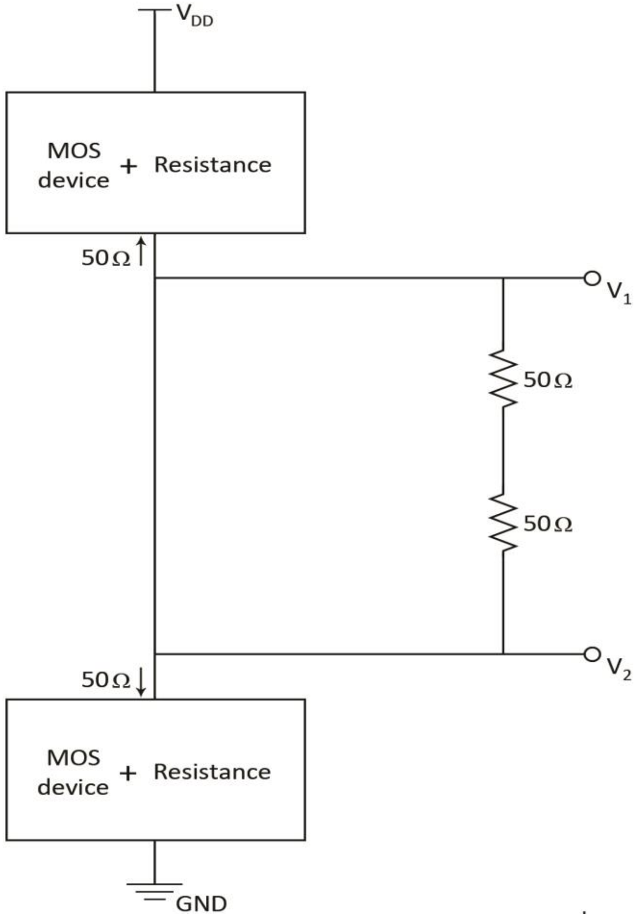

Figure 1.15 Block description of PHY driver

1.2 LITERATURE REVIEW

1. Everett Rogers in 1999 analyzed Low Drop out Voltage Regulator by using PMOS device as a pass element. Stability analysis, open loop response, and pole-zero analysis is presented in the paper. Effect of reference voltage, error amplifier, feedback element, pass element ,ESR, output capacitor, bulk capacitor, error amplifier resistance, pass element capacitance are also analyzed in the paper. Various conditions for selecting pass element for the LDO and the advantages linked with using PMOS as a pass element is presented in the paper.
2. Brian M. King in 2000 presented a paper for understanding the load transient response of low drop out voltage regulator. Various compensation techniques for stability and transient response are defined. Effect of output capacitance, bulk capacitance, and the effect of ESR and series inductance linked with these capacitance, on the stability is explained precisely.

Different poles and zeros location, open loop dc gain associated with the LDO is shown by means of bode plot. All the factors and parameters which affect the stability and settling time are mentioned in the art. In addition to the main feedback loop, some LDOs contain a second feedback loop that allows the LDO to respond faster to large-output transients. This fast-transient loop basically bypasses the error amplifier stage and drives the pass element directly. A symbolic representation of an LDO with this secondary compensation is shown in Figure 1.16. By responding faster than the error amplifier compensation, LDOs that contain this loop are better able to minimize the effects of a load transient.

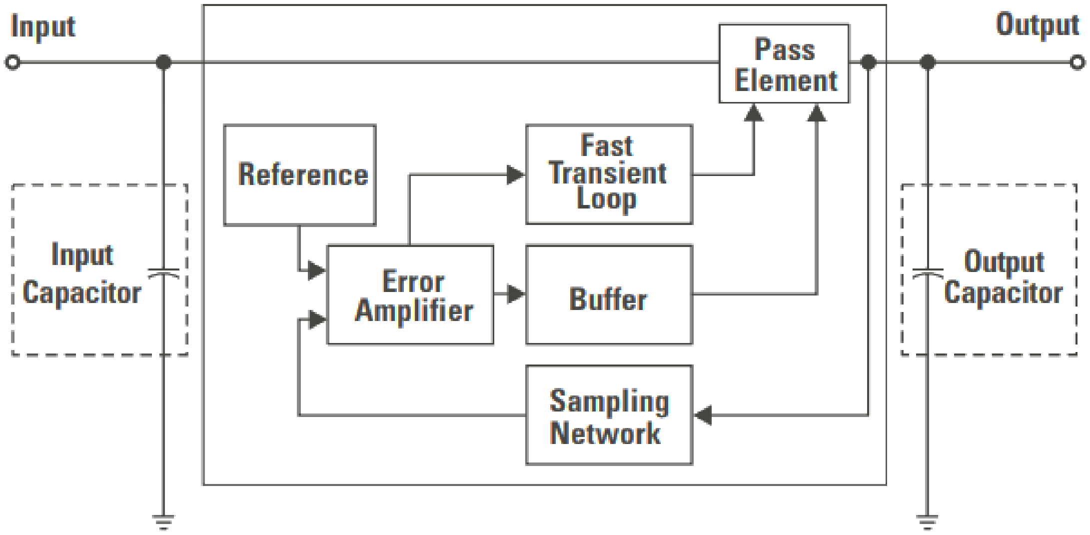

Figure 1.16 Symbolic representation of an LDO with this secondary compensation [2]

3. John C Teel in 2005 presented a paper for understanding power supply rejection in linear regulators. PSRR has been found out at different regions of frequencies i.e. from low to higher value of frequencies. Different circuit elements and parameters on which PSRR depends have been presented in the paper. The writer presented a complete PSRR plot with respect to frequency. It is as shown in Figure 1.17. At low frequency Power supply rejection ratio completely depends upon open loop gain of error amplifier, so by increasing the gain, power supply rejection can be improved.

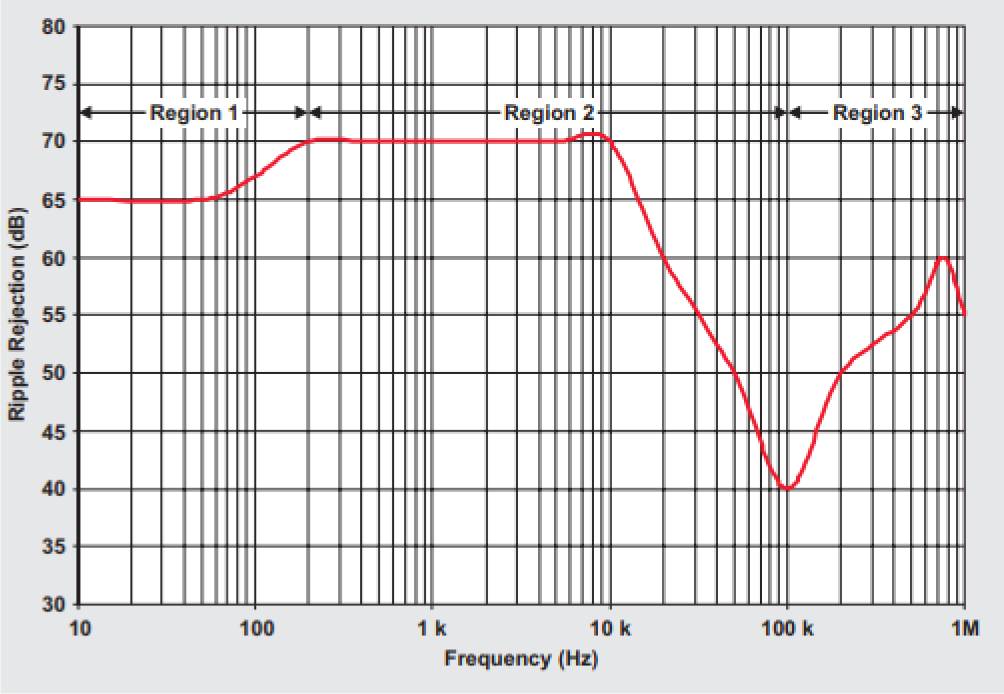

Figure 1.17 PSRR Plots [3]

At mid frequency, PSRR can be improved by high loop gain and by wide bandwidth amplifier. It is clear that under low frequency ripple rejection is more as gain at low frequency is more. At higher frequency greater than UGB, the internal gain is not able to reject ripple, for ripple rejection at higher frequency external capacitor is needed. Parasitic capacitor of pass element also helps in ripple rejection.

4. Michal Day in 2006 explained the requirement of low drop out voltage regulators. The paper provides understanding regarding Low drop out voltage regulators. Various parameters like drop out voltage, PSRR, line regulation, load regulation, quiescent current are explained in the paper along with their dependence elements. Various components and working of Low drop out voltage regulators is also presented in the paper. Brief description of linear and non linear type low drop out voltage regulators are explained and different types of devices which can be used as a pass element is presented in the paper.
5. P.M. Figueiredo in 2006, proposed a technique for eliminating kickback noise in comparator circuits. Three different comparators namely static, dynamic and Class AB comparators are discussed, and various problems linked with each comparator is highlighted. Kickback nose

definition, its origination and technique that can be employed for removing it, is mentioned in the paper. The technique proposed for reducing kickback noise is presented in Figure 1.18.

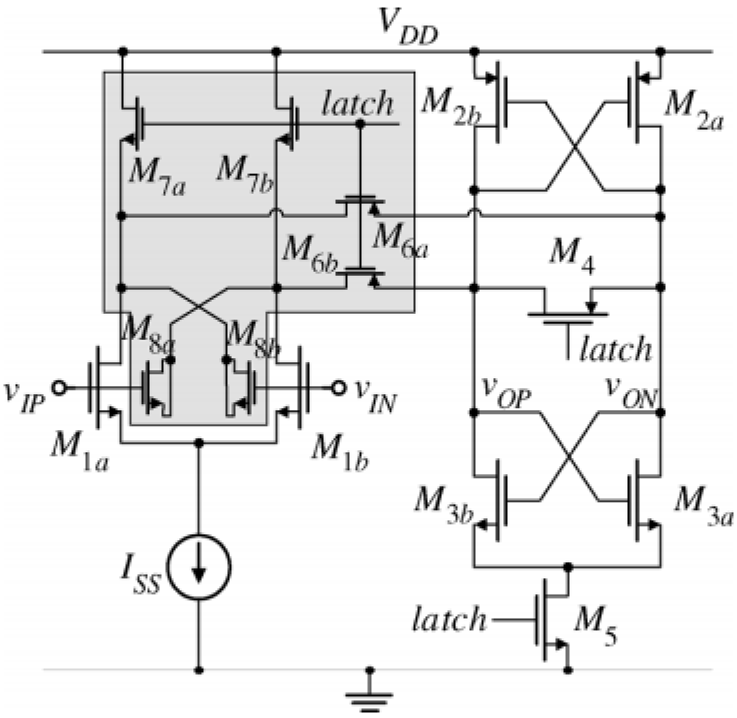

Figure 1.18 Proposed technique for reducing kickback noise [5]

The basic idea behind the proposed technique is that, kick back noise can be reduced by adding a pre-amplifier before the comparator circuit. The proposed technique is for Class-AB type comparator. Basically two steps are employed for reducing the kickback noise, out of which first one is to reduce the voltage variations across the differential nodes followed by neutralization technique.

6. Hu Zhiming in 2010, proposed a Low drop out voltage regulator with advanced capacitive coupling feed forward compensation. LDO is designed on 130nm technology. LDO is designed on 130nm CMOS process. LDO is capable of driving 50mA load. Pseudo-input stage feed forward compensation is proposed. This paper employing the method of capacitive coupling to provide large dynamic current for driving power transistors. Slew rate enhancement technique is also used, resulting in overshoot less than 170mV in 0.1us. The proposed technique is presented in Figure 1.19.

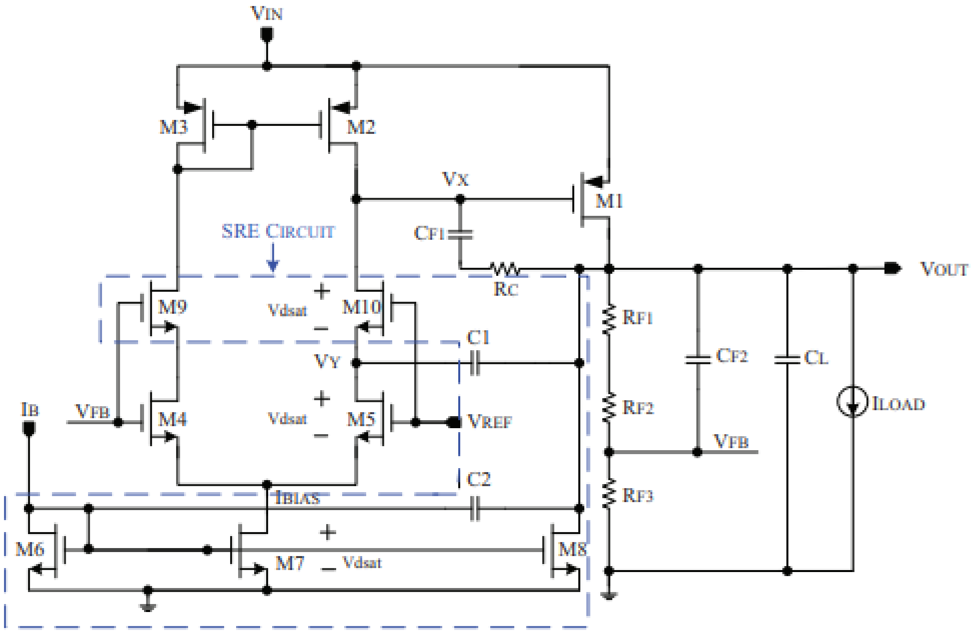

Figure 1.19 Slew rate enhancement technique [6]

LDO is acting as a two stage amplifier with last stage consists of power transistor. M2-M5 are the single stage amplifier, M1 is the power transistor and M6-M8 are the transistors used for biasing purposes.

7. Marco Ho in 2010 presented a Low drop out voltage regulator in 90nm technology. Small gain providing stages are used. By using 1V power supply, LDO is capable of providing an output voltage of 0.9V and maximum output current of 50mA.The quiescent current of LDO is 9.3µA. PSRR, line regulation and load transient responses as well as performances are also improved. No on chip capacitor is needed and hence the chip area of LDO is only 72.5um*37.8um.
8. Zhi-Meng Wu in 2010, proposed a Low drop out voltage regulator for 180nm CMOS technology. The LDO is capable of driving 50mA current at an output voltage of 0.5V, with an input supply voltage of 0.65-1.8V. For the current varying from 5mA-50mA, a settling time of 9.9us can be achieved with a line and load regulation of 0.847%/V and 22.8 p-p mV/mA

respectively. The proposed technique uses a positive feedback to build an error amplifier. Further feedback gain is less than unity to ensure stability.

9. Loai Salem in 2010 introduced a 65nm technology Low drop out voltage regulator. A parallel compensation technique is employed by means of which a zero is introduced at approximately three times of output pole. 0.24 ns response time with 94% current efficiency is recorded. Further LDO uses a supply voltage of 1.2V and produces an output voltage of 1V. 79mV peak to peak droop voltage is recorded.

10. YounghunKo in 2012, proposed Low drop out voltage regulator with fast transient response. LDO is designed for 180nm CMOS process. The proposed technique is by changing the slew current path, the slew rate and unity gain bandwidth can be controlled independently. Drop out voltage recorded is 0.2V and the maximum current that our LDO can drive is 200mA. Quiescent current flowing through the LDO is 7.5µA and unity gain bandwidth obtained is greater than 1 MHZ.

11. Youngil Kim in 2013, proposed a capacitor less Low drop out voltage regulator with fast feedback technique. The proposed LDO contains a low quiescent current Error amplifier. Slew rate enhancement circuit is used to minimize compensation capacitance. LDO is designed by using 110nm technology. Trans conductance amplifier being employed help in getting higher DC gain. Further the settling time is reduced by six times as compare with conventional LDO.

12. Jianping in 2013, proposed a 25mA CMOS Low drop voltage regulator. PSRR of -85dB is recorded at 2.5mA. LDO is designed at 180nm technology providing a maximum load current of 25mA. LDO chip occupies an area of 0.042mm^2. The quiescent current is 15µA. Undershoot and overshoot voltages are less than 40mV, when load changes between 1mA and 2.5mA. The response settles down within 40ns. The proposed technique is shown in Figure 1.20. M1 and M2 are the two transistors used in the same branch and doing the function of feed forward amplifier. M2 is acting as a common gate amplifier. By setting the e ratio of sizes of M2 and M1, the ripple appearing at the input gate of pass element can be controlled.

13. Kamyar Keikhosravy in 2014 presented a 130nm CMOS low-power capacitor less Low drop out voltage regulator. A bulk modulation technique is used, which is enhancing the performance of LDO. When comparing with conventional LDO, higher stability, accuracy and driving capability is obtained. About 75% improvement in stability is noted. The recovery time noted is almost ten times from no load to full load transition. The LDO is providing a regulated voltage of 1V from 1.2V input supply. The proposed technique for achieving good stability and accuracy is shown in

Figure 1.21. The idea behind the proposed technique is that by controlling the bulk of pass element, the output driving current capability of LDO can be enhanced.

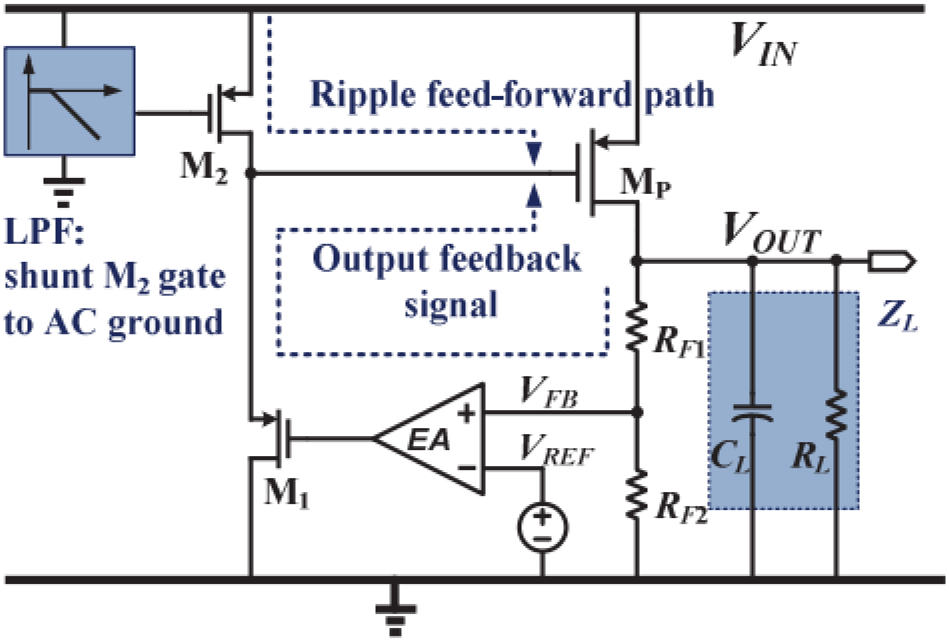

Figure 1.20 Proposed LDO design [12]

In order to improve the output driving capability of LDO, we rely upon the threshold voltage of pass element. The threshold voltage of a MOS device depends upon the bulk voltage. Thus, by controlling the bulk voltage, threshold voltage can be reduced to increase the driving capability of LDO.

14. Ippei Akita in 2013, presented a special Low drop out voltage regulator for OOK transmitter. On chip capacitor is employed for stability purposes and its value is even less than 1pF. Adjustable charge injection technique is used, which guarantees fast load response. The technology employed is 180nm CMOS process. The drop out voltage measured is 100mV peak to peak and consuming a power of 65µA at a power supply of 1.8V.

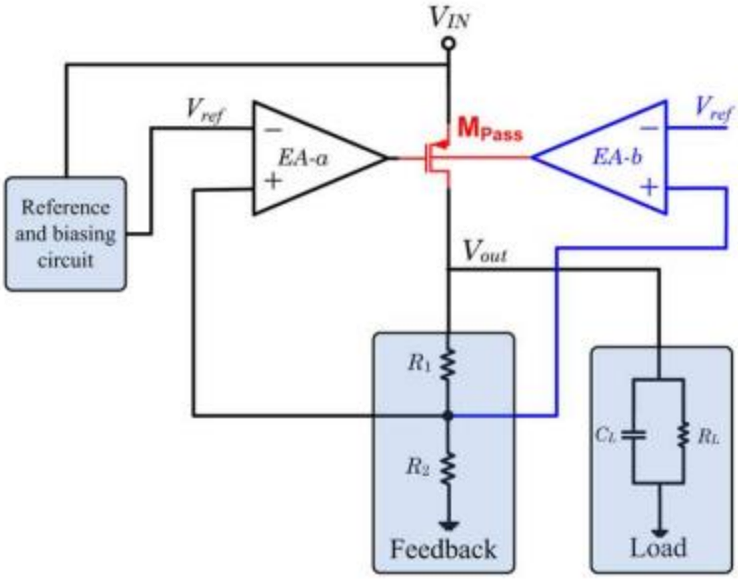

Figure 1.21 Proposed technique for achieving good stability and accuracy [13]

15. Xiao Liang Tan in 2014, proposed a Low drop out voltage regulator with weighted current feedback technique. The concept involved behind the proposed paper is through feedback of a weighted current, the WCF allows accurate management of output impedance and also the management of inter-gain stage. WCF does not allow the right-half plane pole to originate and further it also push the non-dominant pole to the higher frequencies. Maximum current that LDO can drive is 50mA. Settling time is within 400ns and a quiescent current of 15.9µA is following through the LDO. Technology involved is 65nm. Figure of merit recorded is also very good.

16. Meriam Gay Bautista in 2015, proposed high power supply rejection ratio, Low drop out voltage regulator with low power dissipation. The technology involved is 180nm CMOS process. Input supply voltage of 1.8V is used, and by means of LDO we are getting a regulated output voltage of 1.68V. The driving capability of LDO is 50mA. A transient response of 5.5mV overshoot and 3.4mV undershoot is recorded. PSRR of -73dB at a frequency of 16.7 MHZ and a relatively Low power of 90mW is achieved. The proposed technique is presented in Figure 1.22. Reference circuit and error amplifier circuit are specially designed. The pass element is chosen to work under saturation region. A loop gain of greater than 60dB is achieved, and load as well as line regulations are also getting improved using this technique.

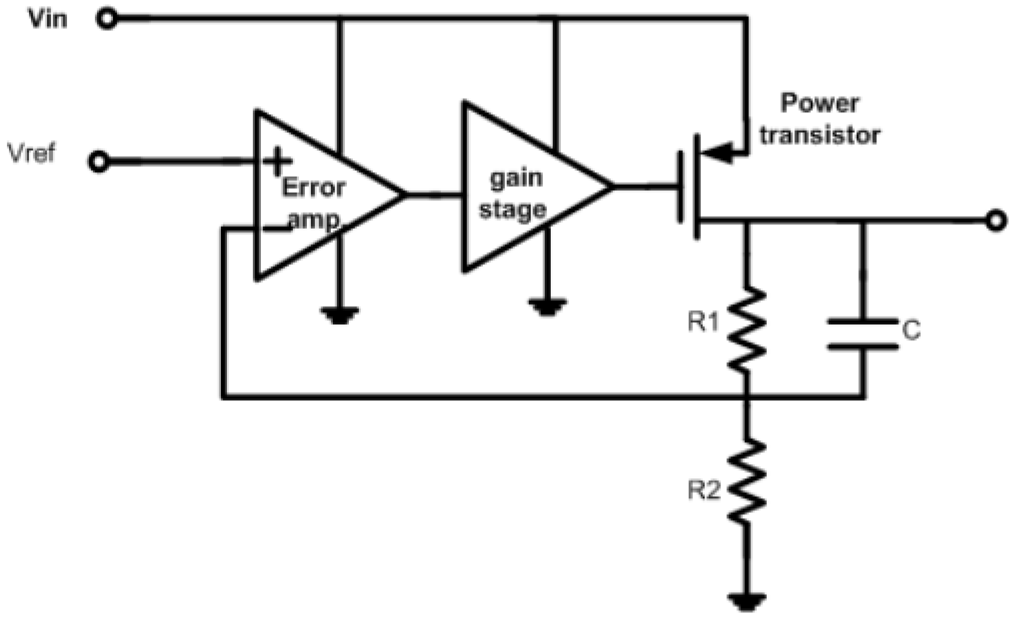

Figure 1.22 Proposed high PSRR LDO design [16]

17. Mehdi Nasrollahpour in 2016, proposed fast transient response Low drop out voltage regulator in 180nm CMOS technology. The idea proposed is to design a replica circuit that injects current into the second stage of amplifier. A PSRR of -40dB and -75dB is achieved at frequency of 24MHZ and 200 kHz respectively. Overshoot and undershoot are less than 4.78mV and 4.2mV with a rise and fall time of 200ns, when the load current is varied from 100mA to 0mA. Line regulation of 3.6mV/V and load regulation of 0.35% per mA is achieved.

18. Amandeep Kaur in 2016, proposed a low power low latency comparator. Comparator is proposed for ramp ADC in CMOS imagers. The technology employed is 180nm. SR latch is proposed to enhance the switching speed of comparator. Circuit consumes a total power of 4.289µW with a clock frequency of 20MHz.

The circuit diagram and the proposed technique is shown in the Figure 1.23.The settling time of the comparator is reduced using adaptive bias technique. The current aiding and starving at the output nodes of the SR latch helps in reduction in the settling time.

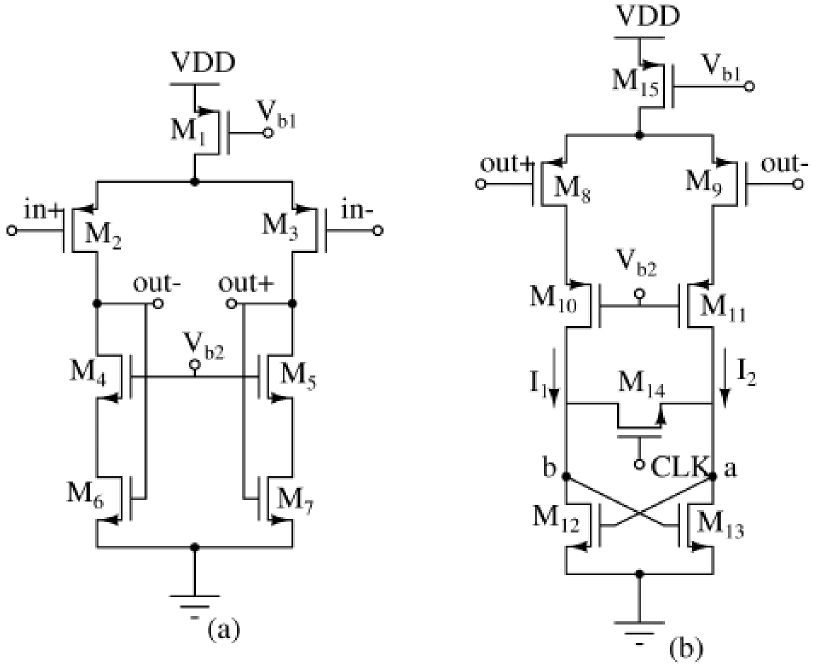

Figure 1.23 Proposed SR latch for static comparator [18]

19. VahidehShirmohammadli in 2017 proposed low power output capacitor less Class-AB CMOS Low drop out voltage regulator. The proposed LDO contains two complementary pass transistor. These transistors are controlled using a level shifter technique. LDO is designed on 180nm CMOS technology. LDO is able to drive 100mA of load current, using a 10pF capacitor. Quiescent current of 3.14µA flows through LDO. Corresponding to supply voltage of 1.2-2.5V, it produces a regulated voltage of 1V with a current efficiency of 99.99%.

20. SeongJin Yun in 2017, proposed a cap less Low drop out voltage regulator. Paper is focusing on the idea that to minimize the power supply noise, higher PSRR is needed. Under this paper, a negative capacitance circuit and a voltage damper is proposed for enhancing power supply rejection ratio and Figure of merit. The on chip capacitor used is around 12.7pF and the achieved PSRR is -76dB at 1 MHZ. Figure of merit recorded is 96.3fs. The technology used for designing LDO is 180nm.

21. Younghgun Lim in 2017, proposed an external capacitor-less Low drop out voltage regulator. Paper focusing on ASRC i.e. adaptive supply-ripple cancellation technique for enhancing the PSRR. LDO is designed for 65nm technology. The LDO is designed to have a dominant pole at the gate of PMOS, so that there remains no need for the output capacitor. If the dominant pole is at the gate of pass element, than the stability can be achieved easily even when the output current varies. LDO is taking an active area of 0.087 mm^2 and the total power consumption is around 360uW. The proposed technique is presented in Figure 1.24.

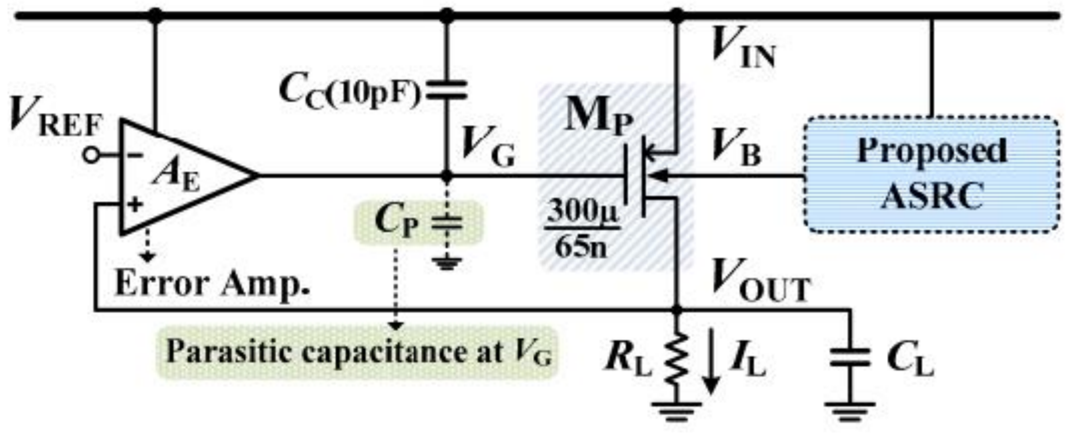

Figure 1.24 Proposed capacitor-less LDO design [21]

22. Po-Yu-Kuo in 2017, proposed an output capacitor less Low drop out voltage regulator. The proposed LDO has a PSRR of -132dB at 1 kHz. It uses a rising Class A voltage buffer, which pushes the parasitic poles at higher frequencies. The technology employed in 180nm CMOS process. 32µA quiescent current flows through the circuit with a settling time of 0.5us. LDO is capable of driving 100mA load current and the drop out voltage is less than 200mV.The proposed technique is presented in Figure 1.25.The proposed LDO has a fully differential input stage, a rising Class-A buffer, PMOS element and feedback resistors. Using voltage buffer, high impedance can be achieved at the output node of error amplifier. Thus, the gate at the power transistor can be decoupled.

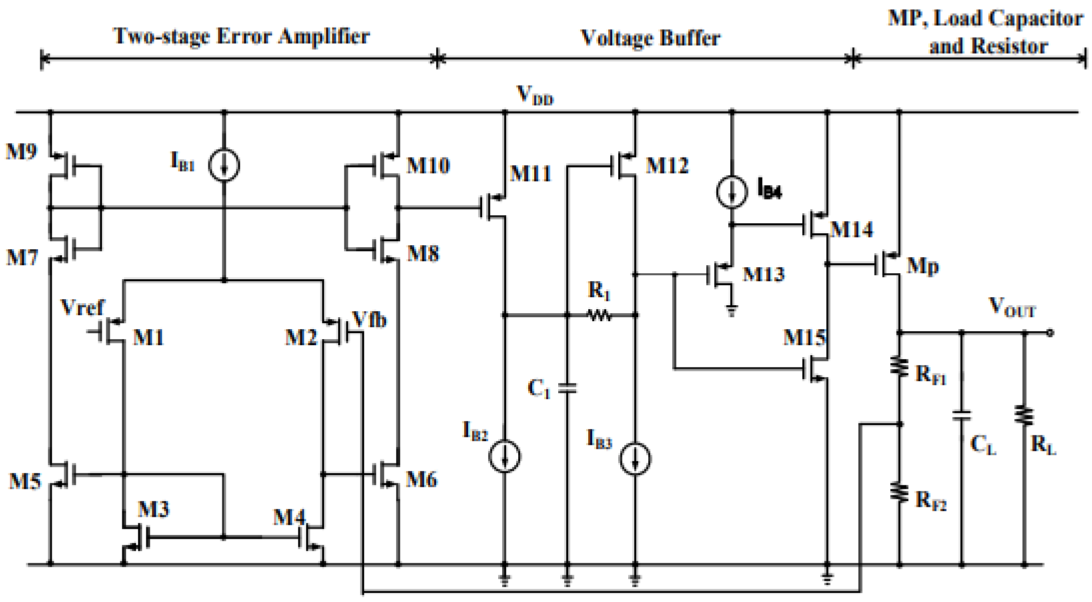

Figure 1.25 Proposed LDO designs [22]

23. Chirag Desai in 2018, proposed an output cap-less Low drop out voltage regulator. 180nm CMOS technology is being used for designing LDO. For an input voltage range of 1.6-1.8V, the LDO is generating a regulated voltage of 1.4-1.6V. 130μA quiescent current is consumed by LDO core and the measured settling time is 20ns. Error amplifier being employed for LDO consists of a differential cross-coupled common gate input stage. By using such an error amplifier around twice conductance and UGB can be achieved as compare to conventional LDO. LDO can drive a current in between 9-40mA in 20ns with a load change in 250ps. The measured undershoot is 158mV.

CHAPTER 2

RESEARCH WORK

2.1 INTRODUCTION

In the conventional LDO’s for solving out stability problem, a larger capacitor is generally employed, which is presented outside the LDO chip. As a result of larger capacitor, dominant pole is generated at the output node. Using this technique for stability has number of problems. One of the major problems originated with the variation of output load. As the output load current varies, the location of dominant pole also varies, as a result of which phase margin of LDO changes and hence stability of LDO system deteriorates. When we are designing an on-chip LDO and on 10nm technology, then chip area is of great concerned. So, the conventional methods used for stability needs to be modified. In section 2.1, we will discuss about stability. Power dissipation due to leaker current also, become a great concern, as the driving capability of LDO increases. When there is need of higher load current driving capability of LDO, size of pass element also increases, which originates the need of leaker, in order to produce a regulated output voltage within given limits. In our work, we come with an idea for tackling out the leaker current. The idea is being discussed in section 2.2. Finally, for generating a reference voltage, we introduce a calibration technique, which is discussed in section 2.3.

2.2 COMPENSATION CIRCUIT FOR STABILITY

In conventional LDO’s the dominant pole is generally presented at the output node, by using a larger off chip capacitor. The presented work is for on-chip LDO and at 10nm technology, so we cannot use a larger capacitor at the output node. There are basically 3 poles, which are originated in LDO without compensation:-

1. Pole in the error amplifier
2. Pole at the output node
3. Pole due to parasitic capacitance at the input of pass element or at the output of second stage of error amplifier.

Pole presented at the output node, varies with load current. All these poles are presented very close to each other for the on-chip LDO. Closely-spaced poles compromise stability. So, we need frequency compensation either by Pole Zero cancellation technique or by Pole splitting technique. If output pole dominated capacitors is there, then Miller compensation is not that much useful. But in our work, dominant pole is not presented at the output node, so we will use Miller compensation. In our work, we are using modified version of Miller compensation. Before discussing its advance version, let's discuss about Miller compensation first. If we are using a compensation capacitor of C_c in two stage error amplifier, then Miller Compensation will creates 2 poles and one zero. One pole will be created at the input side of error amplifier. Another pole will be generated at the output side of amplifier. Input side generated pole is given as:-

$$P_{\mathrm{input}} = (1 + A)C_c \tag{2.1}$$

where A is the open loop gain of error amplifier, C_c is the compensation capacitor.

Error amplifier with compensation capacitor is shown in Figure 2.1.

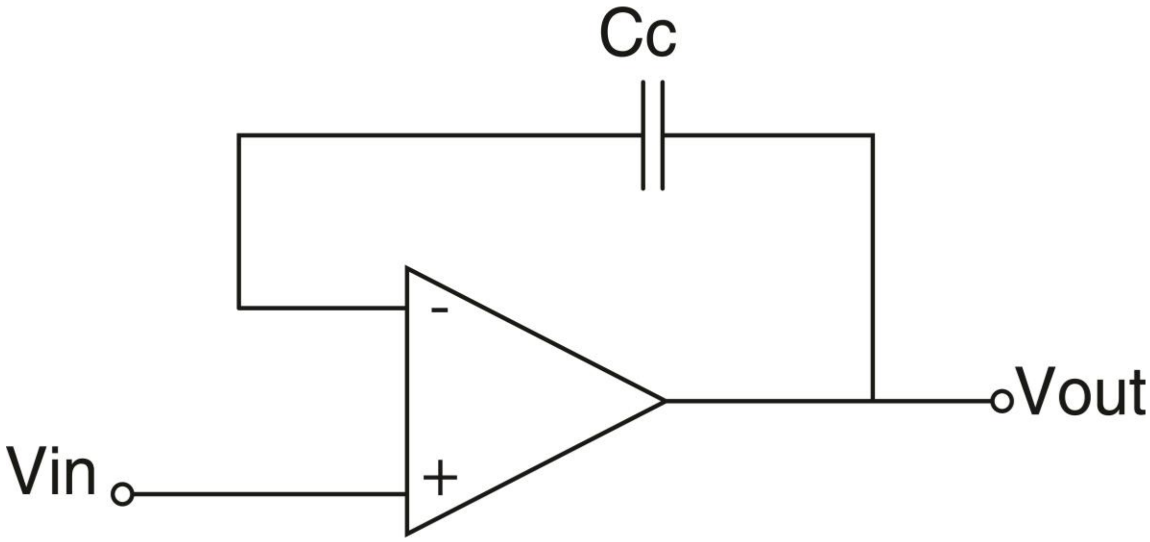

Figure 2.1 Miller compensation

Pole generated at the output of amplifier is given as:-

$$P_{output} = \left(1 + \frac{1}{A}\right) C_c \tag{2.2}$$

Further it also creates a zero at:-

$$Z_o = \frac{gm_2}{C_c} \tag{2.3}$$

where gm_2 is the conductance of input NMOS device of second stage of error amplifier

In order to remove the effect of zero, we can add a compensation resistance R_c, in series with $C_{c,}$ such that

$$R_c = \frac{1}{gm_2} \tag{2.4}$$

By this, Z_0, can be shifted to infinity by obeying the function

$$S_0 = \frac{1}{\left(\frac{1}{gm_2} - R_c\right) C_c} \tag{2.5}$$

So, it is a known fact that at

$$R_c = \frac{1}{gm_2} \text{ zero shift to } \infty \tag{2.6}$$

And for

$$R_c > \frac{1}{gm_2} \text{ zero shifts to the left side plane.}$$

We are using this concept and doing modification in the miller compensation i.e. we are adding a compensation resistance in series with C_c such that$R_c > \frac{1}{gm_2}$. By doing so, we are going to get good phase margin. This compensation is shown in Figure 2.2. So, by using this compensation technique, we can get a good phase margin of 60 degrees to 79 degrees from slow to fast corners. Stability issue can be easily solved out using such type of compensation technique.

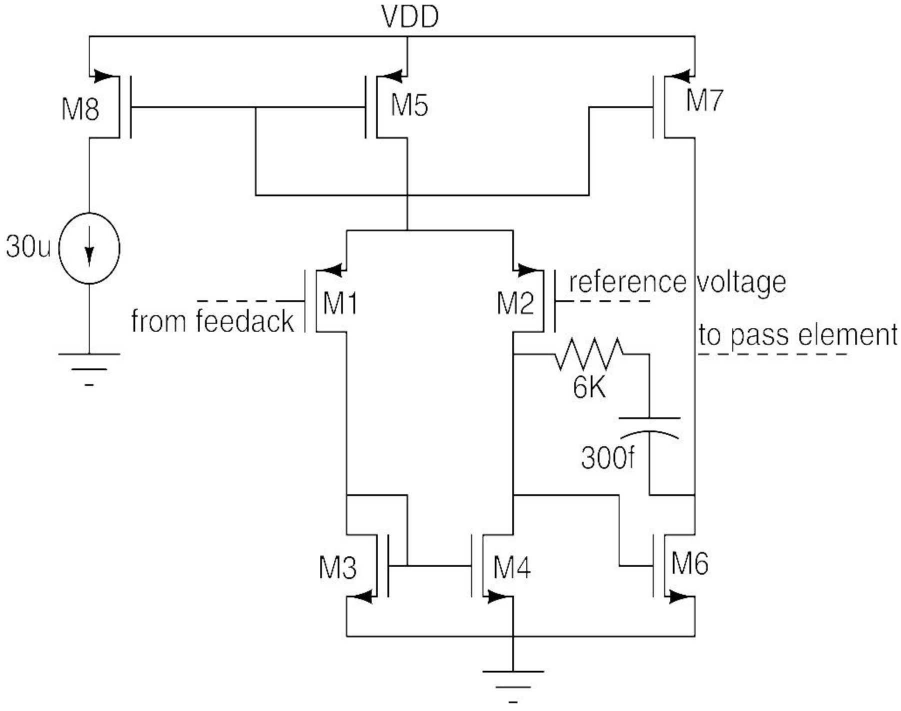

Figure 2.2 Compensation technique for stability

2.3 PASS ELEMENT SLICES SELECTION CIRCUIT FOR REDUCING LEAKER CURRENT

As the driving capability of LDO increases, the size of pass element require to drive the load also increases. With the increment in size of pass element, getting a regulated voltage, without the usage of leaker is quite difficult, especially under no load condition. With the addition of leaker, an extra leaker current also starts to flow, which means that most of power corresponding to leaker will be dissipated every time. In order to avoid the usage of leaker, we need to add some additional circuit to our design, such that output voltage remains regulated, under no load condition. The circuit that we are going to use is a digital 2:1 MUX circuit. We are dividing our circuit to work under two different load conditions, one is in between no load to 2.5 mA and second part is from 2.5 mA to 40 mA. Complete LDO circuit with added 2:1 MUX is shown in Figure 2.3. When the output current is less than equal to 2.5 mA, then under those conditions, we need to use only 90 slices, whereas when the output current required is in between 2.5 mA-40 mA, then under those conditions, we are using 1300 slices of PMOS device. Number of slices being used, depends upon the minimum value of current that can flow through our device, which is 30µA. Now, under no load condition, selecting circuit will select a single bundle of 90 slices, and when the driving current needed is greater than 2.5 mA-40 mA, then under those conditions, selecting network, will select both bundles of 90 and 1200 slices. By the addition of selecting network, we get rid of using leaker. Further, by the addition of digital circuit, we can use higher value of feedback resistances, which again reduces the overall power dissipation. Earlier about 2 times of power dissipation has been saved by the addition of 2:1 MUX. So, in whole, addition of MUX, allows us to use our LDO without leaker, reduces the overall power dissipation and also helps in improving no load regulation. The circuit diagram of 2:1 MUX consists of 2 transmission gates is shown in Figure 2.4.

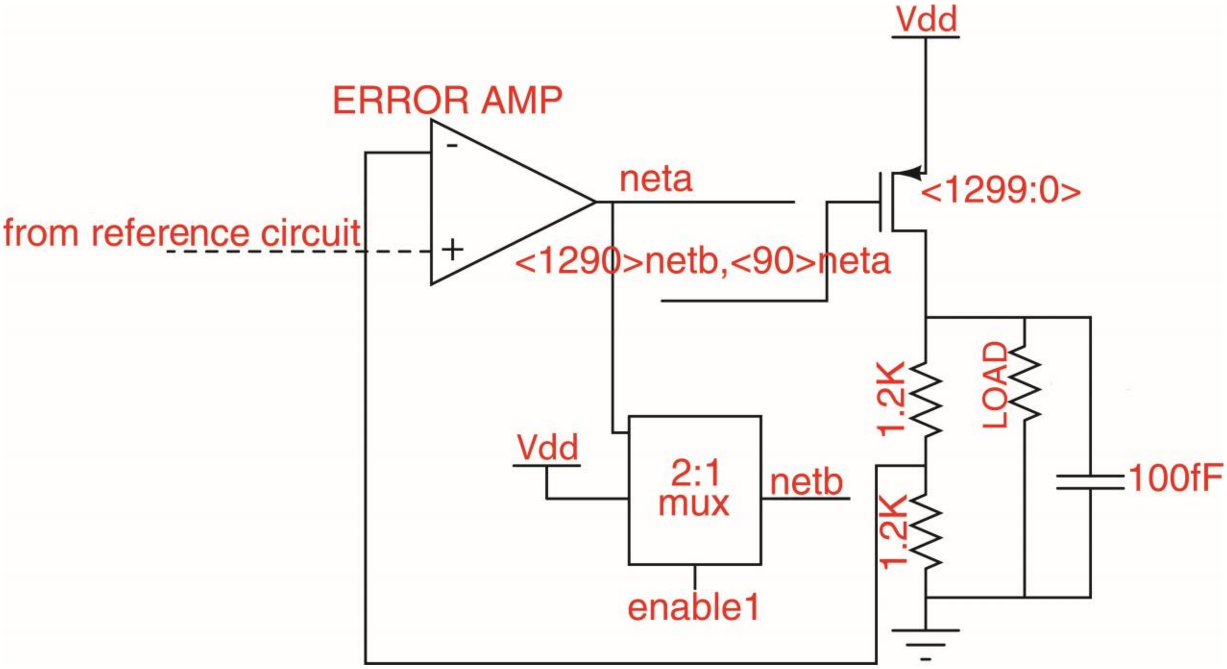

Figure 2.3 Compensation technique for leaker current

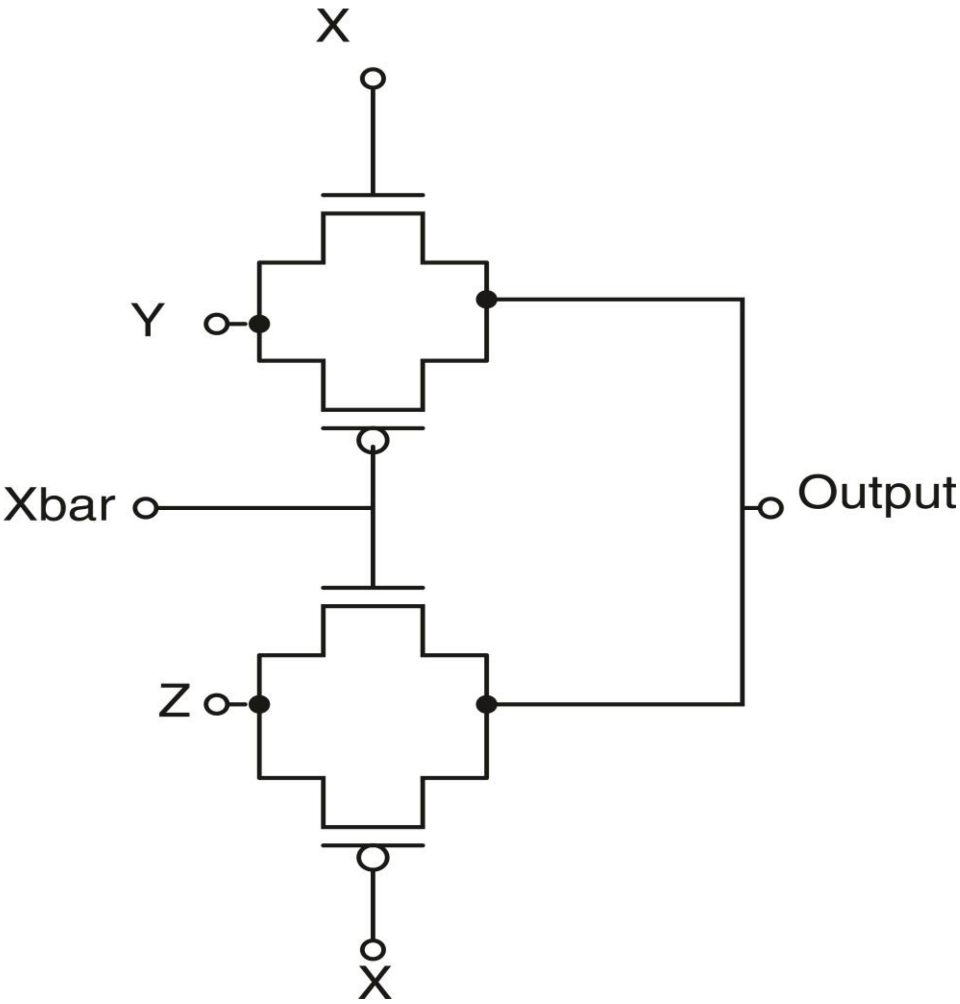

Figure 2.4 MUX circuit using transmission gates

2.4 CALIBRATION TECHNIQUE FOR REFERENCE VOLTAGE

Out of four important components of LDO, reference voltage is one of them. Reference voltage is the voltage from which the feedback element is compared and accordingly, the conductance of pass element is varied. Basically, resistive ladder and the BGR are the two important reference circuits that are generally used. Out of these two circuits, BGR is widely used. But our work is on 10nm and there is no easy access to BJT under normal condition. Further, fabricating resistance under 10nm is very simple as compare to BJT. As variations in the output voltage allowed is±3%, so we need not required very precise reference voltage for error amplifier. Under 10nm technology, resistance is fabricated using polysilicon. As in higher technology, resistance if fabricated using metals, so the net variations in resistance value is very less under 10nm than in higher technology. In the fabrication of BJT, three different layers need to be diffused, for the creation of three different layers i.e. emitter, base and collector. Current gain of BJT depends upon the thickness of these three diffused layers. Variations in the thickness of these layer, results in change of current gain and thus overall working of BJT gets affected. Further it is very difficult to diffuse these layers without any thickness variations, which means getting accurate and precise results from BJT is quite difficult. For all the above mention reasons, we opt resistive ladder instead of BGR. Without calibration, the resistive ladder employed is giving 20mV variations, from slow to nominal corner and from nominal to fast corner. The current which is allowed to flow through our resistive ladder is 50µA. For calibration additional comparator, counter and 32:1 MUX are being used. 32 tap points from resistive ladder are connected to the 32 inputs of 32:1 MUX. These tapping points are at a voltage difference of 5mV. The tapping point above or below these 32 tapping points can have any value of voltage difference. These 32 points varies from 180mV-330mV. Further, the current being fed to the resistive ladder is 50µA. The comparator output is connected to the up/down counter. Whenever the output of comparator comes out to be 1, it starts to do up counting, and when output of comparator, comes out to be 0, counter starts to do down counting. One of the input of comparator, is connected to the reference voltage. This reference voltage will be provided from off chip and will be available for mille of seconds. For example, we want to generate a 0.2V of reference voltage by means of resistive ladder, and then 0.2V will be available from off chip for mille of seconds. Similar concept is valid for 0.225V, 0.25V, 0.275V and 0.3V. The other input of comparator is feedback from the output of 32:1 MUX. Comparator will compare the input signal and based on the two signal difference, it will generate 0 or 1and correspondingly up/down counting of counter takes place. For example, if we want to produce 200mV for our LDO, then corresponding to different condition, two of the tapping point will be very close to reference voltage of comparator. Whenever, counter after counting up or down counting reaches to such a point at which output of comparator starts to toggle then that input number of MUX is stored by RTL logic. In order to remove variation in resistive ladder, calibration technique is used as shown in Figure 2.5.

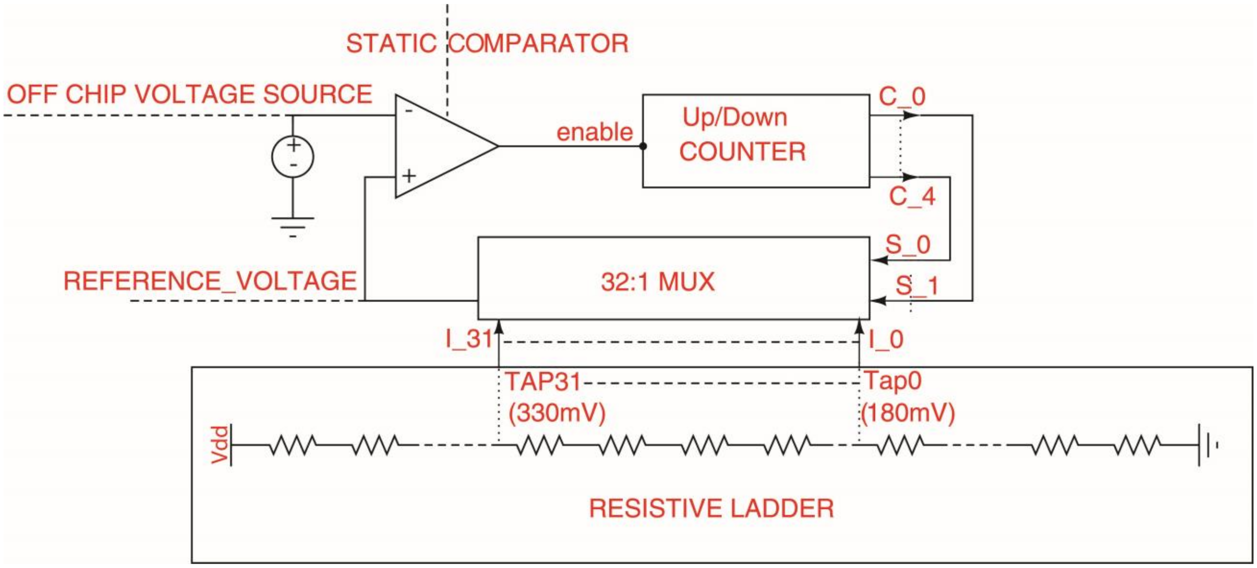

Figure 2.5 Calibration technique for reference voltage

For different external condition, stored number will be different. Afterwards comparator is removed from LDO circuit and the corresponding stored code by RTL is used by LDO to produce the required result at the output. Same procedure is repeated for 0.225V, 0.25V, 0.275V and 0.3V.

CHAPTER 3

Circuit flow diagram and design implementation

3.1 DESIGN FLOW DIAGRAM

The following flow diagram in Figure3.1represents the design flow of LDO, starting from specifications

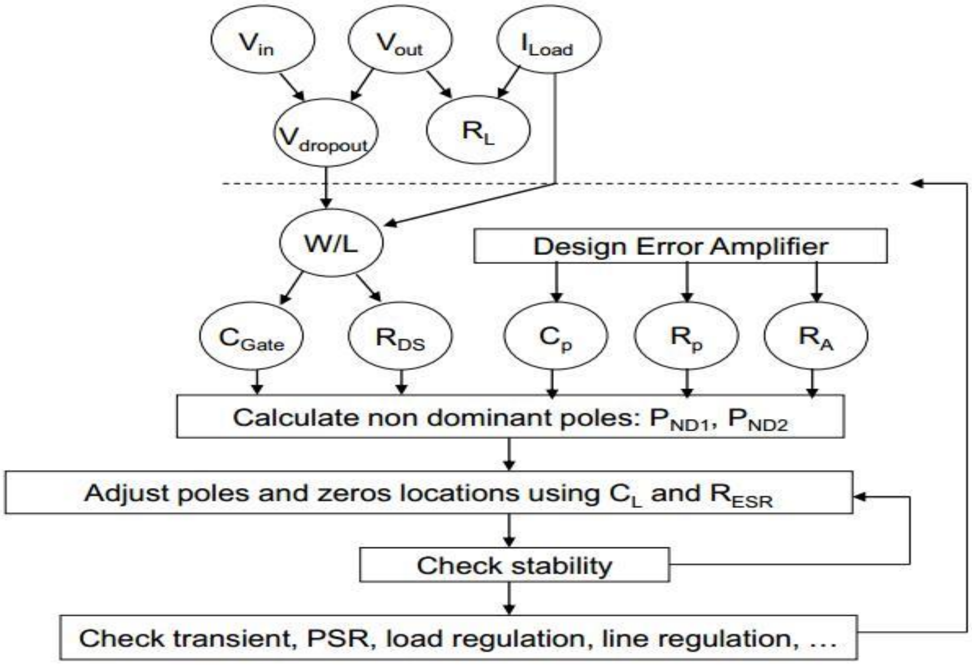

Figure 3.1 Flow diagram of designing LDO

3.2 CIRCUIT DESIGN OF ERROR AMPLIFIER

Looking into LDO’s complete circuit, the specification for error amplifier is decided. There are basic four important parameters, that error amplifier should possess, in order to do comparison for LDO precisely. These four parameters are common mode input voltage, Gain, PSRR and the bias current. LDO being designed is a programmable LDO, which is going to generate five different voltages at the output. These voltages are 0.4V, 0.45V, 0.5V, 0.55V and 0.6V. The feedback factor that we are using is 0.5. This implies that, corresponding to above mention output voltages; feedback voltages are going to be 0.2V, 0.225V, 0.25V, 0.275V and 0.3V respectively. As these voltages are being feedback into input of error amplifier, so based upon these feedback voltages, the common mode Input voltage being decided is in between 150mV-340mV, keeping all the variations across corners into account. Open loop gain of an error amplifier greatly affect, the load regulation, line regulation, stability and overall PSRR of LDO. Higher its value, better these parameters are going to be. Based on the requirement the specification decided for the gain is in between 40dB-65dB from fast to slow corners. In order to fulfill requirement of gain, we are using cascading stage of differential amplifier followed by common source amplifier. Ripples at the output of LDO, comes via error amplifier, pass element and the reference circuit. In order to prevent ripples to reach at the output of LDO via error amplifier, Input pair of first stage of error amplifier, should be properly selected. As discussed, earlier if we use NMOS as an input pairs, then

$$\frac{V_{EA0}}{V_{DD}} \approx 1 \tag{3.1}$$

where V_{EA0} is output of first stage of differential amplifier and V_{DD} is the input power supply.

On the other hand, if PMOS are selected as an input pair, ripples at the input power supply, gets suppressed and doesn't appear at the output of differential amplifier. This is because output impedance of PMOS input pair differential amplifier is very large, which doesn't allows ripples to appear at its output. For this reason, we are using PMOS as an input pairs of differential amplifiers. Specification of Error amplifier is shown in table 3.1

Table 3.1 Specification of error amplifier

Parameter	Value/Device used
1. Bias Current	30µA
2. Gain	40-65dB
3. Input common mode range	150-330mV
4. Output common mode range	180-440mV
5. Supply voltage	1V
6. Device employed for Input pair	PMOS device

Output common mode range of error amplifier is also very important to be considered. The output of error amplifier is going to drive the pass element. For proper LDO's regulation process, the pass element should be remained under saturation region. The complete two stage error amplifier is shown in Figure 3.2

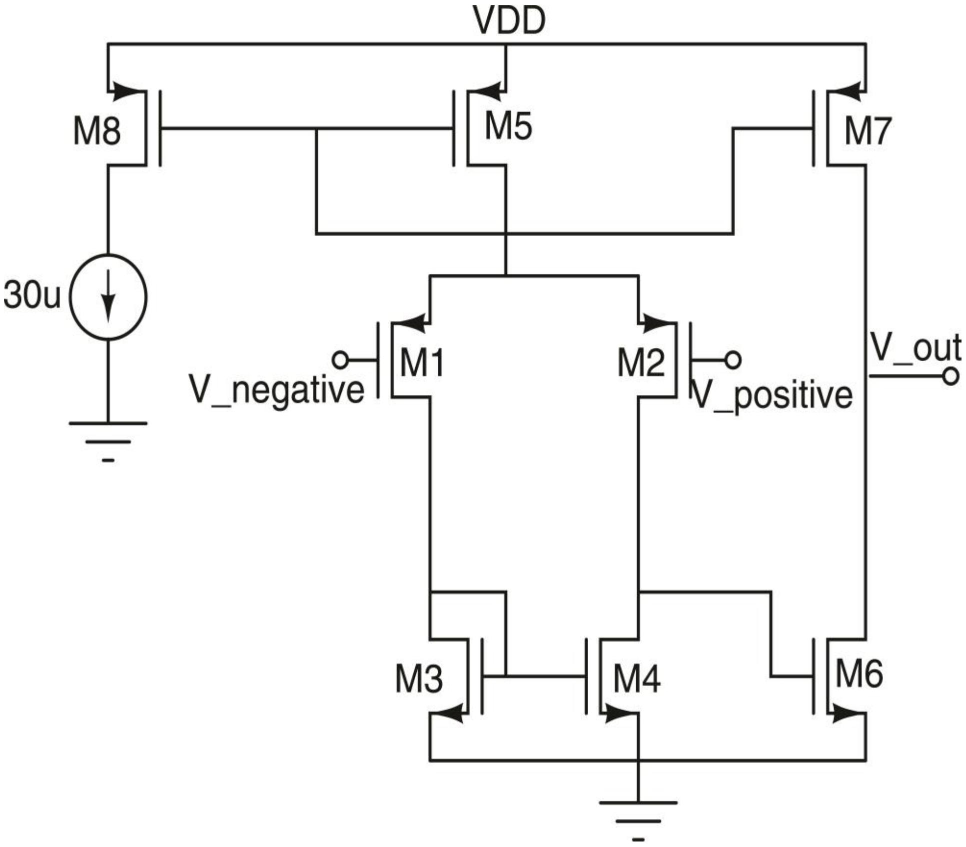

Figure 3.2 Two stage error amplifier

From the Figure, it is cleared that first stage is a PMOS differential amplifier whereas the second stage is a common source amplifier.

3.2.1 Steps for designing Error Amplifier

The aspect ratio of M5, M7, and M8is obtained using power consumption or the slew rate.

- The trans-conductance of M1 and M2 is obtained from unity gain bandwidth and the open loop gain, and are also sized to maintain the ICMR.
- The transistors M3 and M4 are sized to maintain the common mode range of the op-amp. The devices are biased in saturation region.
- Design of M7 from assumption that gm2=10gm1 to convert two pole system to single pole system for the improved stability.

3.2.2 Current mirror design

In our error amplifier design, for mirroring of current, we are using stacked device as shown in Figure 3.3.For understanding the concept of stacked device, consider the circuit 3.4.From the Figure 3.4 it is clear that $V_{SG1} = V_{SG2}$. Now due to variations in drain current, for an instant say it increases. Because of increment in current, voltage drop across resistance increases, as a result of which voltage at node N decreases. So, V_{SG} decreases and hence the variation in current is neutralized and the mirroring of current is maintained. Now in real design, resistance, are replaced by PMOS devices. For proper functioning of current mirror, M3 and M4 are to be placed in linear region and lower two PMOS devices M1 and M2, are to be made to work under saturation region. By following the above configuration, current is copied very precisely as compare to other current mirror configurations.

3.3 DESIGN OF PASS ELEMENT

The five basic possible configurations for the pass element are NPN Darlington, NPN emitter follower, common emitter lateral PNP, NMOS source follower, and common source PMOS transistor. The degree of freedom for the choice of topology is dependent on the process technology and the required specifications of the LDO. Multiple transistor structures are also possible candidates for pass devices. However, the intrinsic performance characteristics of these structures revolve around the transistor that actually delivers the output current. The remaining devices can be grouped into the output stage of the error amplifier, otherwise referred as the buffer stage. Table 6.1 shows a comparison between the different pass elements with respect to their applicable LDO performance parameters. Bipolar devices are capable of delivering the highest output currents for a given supply voltage. The output current capabilities per unit area of MOS transistors exhibit limited performance with high dependencies on aspect ratio and gate drive. However, the voltage driven nature of MOS devices is beneficial in minimizing quiescent current flow. Bipolar transistors are current driven devices with finite forward current gains (â) that can be as low as 20 A/A over process variations. As a result, the error amplifier that drives a bipolar pass element must be able to source or sink relatively high base currents during high load-current conditions. The base current of the NPN transistor, however, flows to the output while that of the PNP counterpart is lost as ground current.

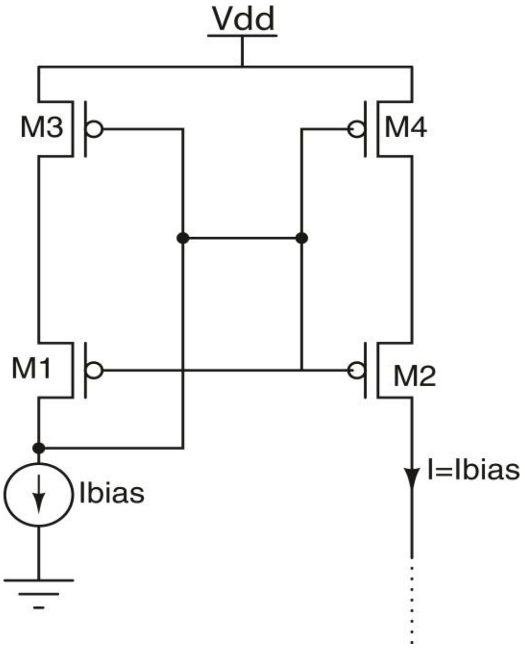

Figure 3.3 Current mirror design using stacked device

Consequently, NPN structures are better suited for low quiescent current designs than PNP realizations. Moreover, the quiescent current flow during drop-out conditions for PNP pass devices can become significantly large. The fastest response, needed for transient load-current steps, is achieved by the NPN structures. PNP transistors, on the other hand, are commonly created as lateral devices and thus exhibit inherently slower response times. Vertical PNP structures yield fast response times but their availability in standard process technologies is limited. MOS transistors are typically slower than vertical bipolar devices but faster than lateral PNP realizations.

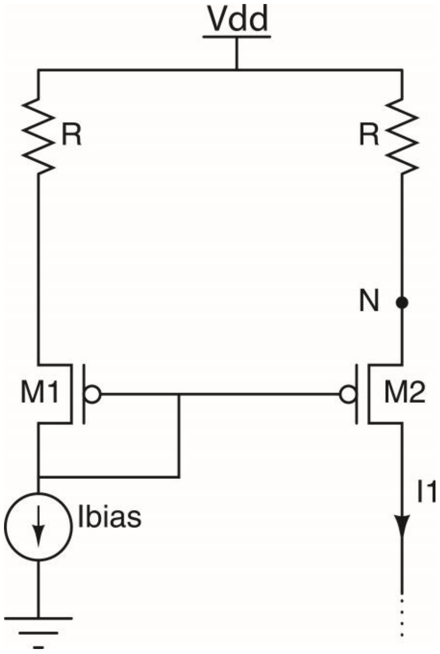

Figure 3.4 Concept of using stacked device

Lowest drop-out voltages are achieved by PMOS (Vsd-sat) and PNP (Vec-sat) transistors, approximately between 0.1 and 0.4 V. The NPN Darlington, NPN and NMOS structures involve at least one Vbe [Vgs] in addition to one Vec-sat [Vsd-sat] with a minimum drop-out voltage of roughly 0.8 to 1.2 V. However, the drop-out voltage of these pass devices can be improved by utilizing a charge pump. The disadvantage of this technique lies in complexity and cost. It requires an oscillator thereby increasing quiescent current overhead, noise injection, and circuit complexity. Excluding the charge pump method, PMOS transistors exhibit the lowest drop-out voltages because of their characteristically variable resistance, Vsd changes with gate drive and aspect ratio. On the other hand, PNP devices have a constant saturation voltage of approximately 200 mV. In conclusion, PMOS devices are typically the best overall choice yielding a good compromise of drop-out voltage, quiescent current flow, output current, and speed. Comparison of different types of pass element that can be used as a pass element is shown in table 3.2.

3.4 DESIGN OF REFERENCE CIRCUIT AND CALIBRATION OF LDO

For reference voltage, resistive ladder or BGR can be used. In our work, we are using resistive ladder for generating reference voltage, which is acting as one of the input of error amplifier. The current which is allowed to flow through the resistive ladder is 50µA. Power supply available is 1V. So, accordingly we are using 20kohm resistance. The resistive ladder is shown in Figure 3.7.

Table 3.2 Comparison of pass element structures.

Parameter	**Darlington**	**NPN**	**PNP**	**NMOS**	**PMOS**
Io-max	High	High	High	Medium	Medium
I quiescent	Medium	Medium	Large	Low	Low
V drop-out	Vsat+2Vbe	Vsat+Vbe	Vec-sat	Vsat-gs	Vsd-sat
Speed	Fast	Fast	Slow	Medium	Medium

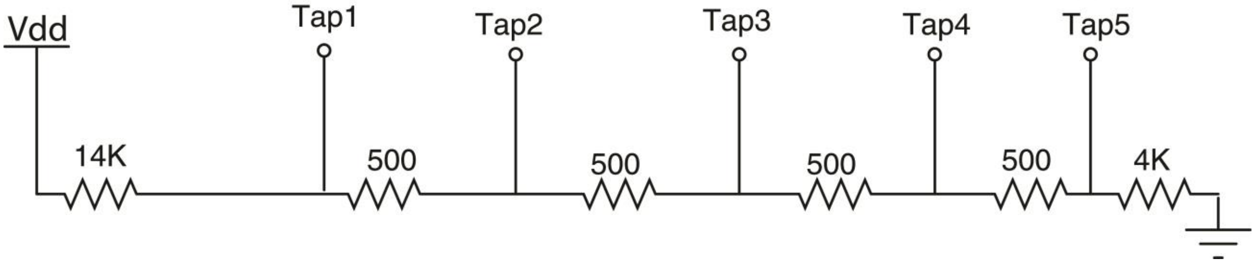

Figure 3.5 Resistive ladder

If we use this resistive ladder without any calibration then various tapping points which are made corresponding to resistive ladder shows a variations of around 20mV. This variation occurs because of PVT variations i.e. process, voltage and temperature variations. In order to make our resistive ladder to be free from these variations or to minimize the PVT variations, we generally go for calibration technique. Basic components that we are using for reference circuit include comparator, up/down counter, RTL logic and 32:1 MUX. Actually, the basic concept behind the calibration technique is that out of N tapping points, which are showing variation, in its value, one of the tap point, surely give us a required voltage. There is a need for proper selection of that tapping point. By means of comparator, counter and MUX, we achieve our requirement. We make some of modification in resistive ladder. Out of 20K ohm total resistance, we are tapping out 32 points, with a voltage difference of 5mV under nominal working condition. These tapping points vary from 330mV to 170 mV. These 32 tapping points are connected to 32 inputs of 32:1 MUX, whose output is connected to the comparator. Comparator produce either 0 or 1, based upon the difference of two input signals given to it. When it gives 0, counter will do up count else do down count. Various specifications decided for calibration is shown in table 3.5. The modified resistive ladder is shown in Figure 3.6. We are employing static comparator instead of dynamic comparator. The offset requirement for dynamic comparator is very high, which is not fulfilling our requirement. Clock is not available so, again we cannot employ dynamic comparator, which synchronize its working with clock.

Table 3.3 Specifications of calibration

Parameter	Value/Function/Type
1. Supply Voltage	1V
2. Current through resistive ladder	50µA
3. Offset for comparator	2mV
4. Bias current for comparator	30µA
5. Total resistance of resistive ladder	20k
6. Counter A) For input=0 B) For input=1	 Up counting Down counting
7. Type of comparator	Static

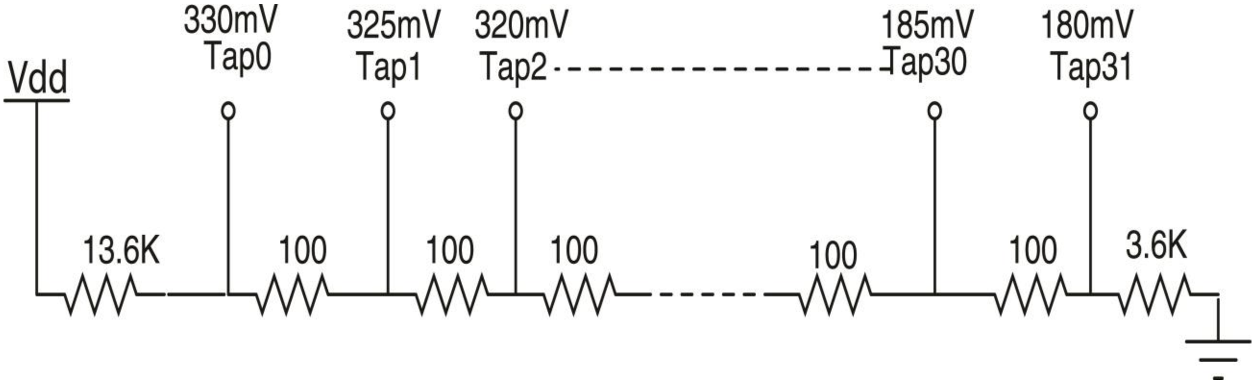

Figure 3.6 Modified resistive ladder

Dynamic comparators also suffer from two different problems:-Charge injection and kick back noise. Kick back noise is the coupling of variations presented at the output or regeneration nodes of comparators with the input node. Generally, parasitic capacitances are presented in the design. By means of parasitic capacitances, the output gets coupled with the input and produce disturbance in the input signal. Further, this type of coupling is possible as input source has non-zero output impedance. On the other hand, if we talk about charge injection, then such type of problem generally arises, wherever we are using a clock. For this reason, charge injection is also known as clock feed through. Wherever switching action is taking place, charge injection occurs. When switch is on, voltage difference between drain and source is zero. During turning off, the charges present in the channel of a device comes out via drain and source junction, and gets linked with other elements of a circuit and generating errors in the result. We know, static comparators are slow as well as consume more power, but on the other hand kickback noise, offset, and charge generation problems are absent in it. The basic comparator that we are employing for our work is shown in Figure 3.6. Actually, we are using op-amp under open loop configuration. Offset requirement for calibration is less than 5mV. By using error amplifier under open loop configuration, we are not able to fulfill offset requirement. Offset achieved varies up to 32mV, which is far away from specifications. The reason behind offset problem is the low sensing of error amplifier. As a result it will take more time to give decision and the decision is not complete 1 or 0. In order to overcome this problem, we are adding an inverter after error amplifier as shown in Figure 3.7.

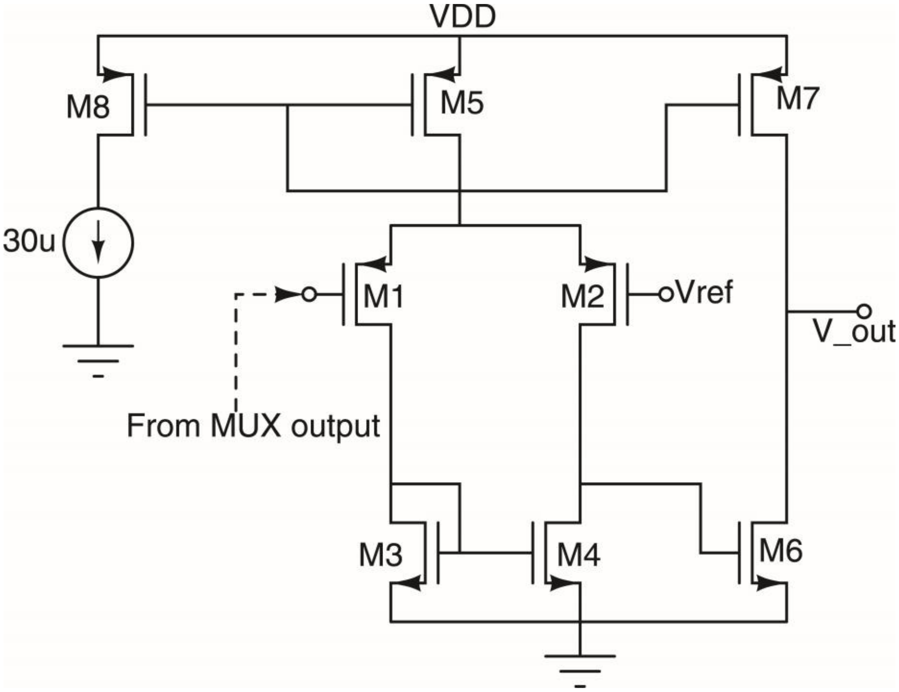

Figure 3.7 Basic comparator circuit

Inverter enhances the sensing capability of error amplifier. The offset achieved using such configuration is less than 2.5mV, which is fulfilling the specification requirement efficiently. While using inverter, extra current of 170µA flow through comparator circuit. So, there is a trade-off between offset value and power dissipation. This extra power is tolerable as only for few mille seconds, comparator is going to operate. Afterwards, comparator is made to disconnect from the LDO circuit, and this extra power dissipation is no longer going to create problems in regulation circuit.

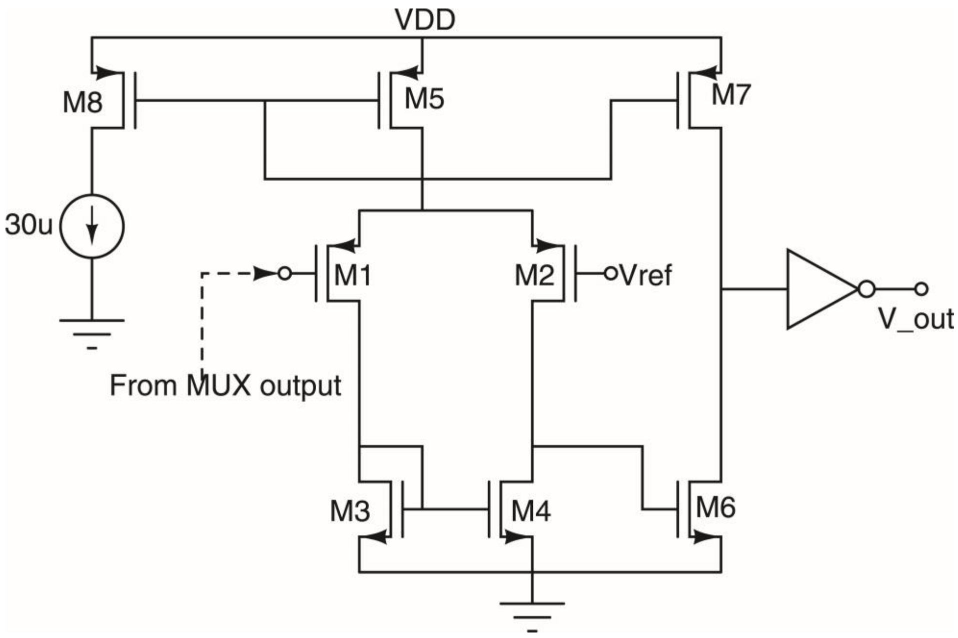

Figure 3.8 Modified comparator circuit

Counter which is being used is just a RTL code. 32:1 MUX is designed by using 17, 2:1 MUX. Each 2:1 MUX is designed by using transmission gates.

CHAPTER 4

SIMULATION RESULTS

In this chapter, simulation results corresponding to different analysis are presented. Different analysis like DC analysis, AC analysis, Tran's analysis, Pole-Zero analysis and stability analysis for LDO circuit is done. Before analyzing different results, it is important to discuss about the simulation environment conditions under which simulations is being done. Different PVT conditions for simulations are:-

1. Process Corners :- Slow ,Fast and Nominal
2. Voltage variations in supply voltage :- 0.9V -1.1V (10% variations)
3. Temperature variations :- -40°C-125°C

4.1 **DC ANALYSIS**

Basically, there are three blocks, on which we do DC analysis separately. Firstly, DC analysis on resistive ladder with or without calibration is done. Then DC analysis, on one of the important block of LDO i.e. error amplifier is initiated. Lastly, DC analysis for the entire LDO is being done, and output voltage across different corners is noted.

4.1.1 DC analysis of reference circuit

Resistive ladder instead of BGR is being used, because there are number of advantages linked with resistive ladder as compare to BGR, less than 10 nm technologies. In this section, we represent DC simulation results, for resistive ladder, with or without calibration.

4.1.1.1 DC simulation results for resistive ladder without calibration

In the specification, 1V power supply and 50µA current is provided. In order to fulfill these conditions, 20K resistance has to be used. Further,5 different voltages as a reference voltage for error amplifier are needed, corresponding to 5 different output voltages. Variations in these reference voltages, corresponding to PVT variations is shown in Table 4.1.

Table 4.1 DC simulation results of resistive ladder without calibration

Parameter	Min value	Max value
1. Reference voltage required in (mV)		
i) 200	180	226.6
ii) 225	202.5	254.6
iii) 250	225	282.5
iv) 275	247.5	310.1
v) 300	270	337.6

4.1.1.2 DC simulation results for resistive ladder with calibration

Reference voltage, generated by resistive ladder without calibration shows, ± 20%variations. According to specifications, only ±5% variations in these reference voltages are allowed. For this reason, we employed calibration technique for resistive ladder. Reference voltages generated after calibration are as shown in Table 4.2.

Table4.2 DC simulation results of resistive ladder with calibration

Parameter	Min value	Max value	Targeted value
1. Reference voltage required in (mV)			
i) 200	198	205.4	195-205
ii) 225	220.5	229.5	220-230
iii) 250	247.5	254.6	245-255
iv) 275	270	279	270-280
v) 300	297	304.6	295-305

4.1.2 DC analysis of error amplifier

Under DC analysis of error amplifier, simulations are being done to find out three parameters:-Input common mode range, quiescent current and the output common mode range of two stage amplifier. Bias current of 30µA is used. In the quiescent current of error amplifier, three components of current will be added. These three current components are:-bias current, current through differential amplifier and the current through second stage of error amplifier. The second important parameter required for error amplifier is input common mode range. It is the input range, in which error amplifier works efficiently. Output common mode range is required to drive the pass element in saturation region. All these parameters are as shown in Table 1.3.

Table 4.3 DC analysis of error amplifier

Parameter	**Min value**	**Max value**
1. Quiescent current(µA)		
A) Bias current	30	30
B) Current through first stage	27	32.2
C) Current through second stage	26.2	34.3
D) Total quiescent current	83.2	96.5
2. Input common mode voltage	150	355
3. Output common mode voltage	175	415

4.1.3 DC analysis of LDO design

Under this section, simulations to find out DC output voltages, corresponding to 5 different output voltage levels, for which we design LDO, is being done. ±3% variations in the output voltage are allowed in specification. For calculating 400mV, reference voltage of 200mV is applied, similarly for 450mV, 500mV, 550mV and 600mV output level, reference voltages of 225mV, 250mV, 275mV and 300mV respectively are used. Since, LDO for two different ranges is being used, out of which first one is from no load to 2.5mA whereas second one is from 2.5mA to 40mA. DC output current is also found under this section. Finally, at the end of this section, DC analysis with or without considering calibration is performed.

Table 4.4 DC analysis of LDO under no load condition using 90 slices

Parameter	Min value	Max value
1.Output voltage in (mV)		
i) Level1 - 400	399.6	411.2
ii) Level2 - 450	449.6	462.1
iii) Level3 - 500	499.5	510.6
iv) Level4 – 550	549.4	559.5
v) Level5 – 600	599.3	608.3
2.DC leaker current (µA)		
i) Level1 - 400	79.31	258.3
ii) Level2 - 450	91	290.3
iii) Level3 - 500	101.4	322.3
iv) Level4 – 550	112.2	354.3
v) Level5 – 600	122.9	386.4

Table 4.5 DC analysis of LDO for 2.5mA load using 90 slices

Parameter	Min value	Max value
1.Output voltage in (mV)		
i) Level1 - 400	399.6	408.6
ii) Level2 - 450	449.3	462
iii) Level3 - 500	499.2	512.3
iv) Level4 - 550	549	552
v) Level5 – 600	599	604
2.DC load current (mA)		
i) Level1 - 400	2.43	2.512
ii) Level2 - 450	2.45	2.514
iii) Level3 - 500	2.47	2.53
iv) Level4 - 550	2.49	2.52
v) Level5 - 600	2.495	2.517

Table 4.6 DC analysis of LDO for 2.5mA load using 1300 slices

Parameter	Min value	Max value
1.Output voltage in (mV)		
i) Level1 - 400	399.7	409
ii) Level2 - 450	449.6	460.1
iii) Level3 - 500	499.5	509.2
iv) Level4 - 550	549.4	558.4
v) Level5 – 600	599.3	608.6
2.DC load current (mA)		
i) Level1 - 400	2.431	2.512
ii) Level2 - 450	2.437	2.523
iii) Level3 - 500	2.452	2.554
iv) Level4 - 550	2.497	2.541
v) Level5 – 600	2.491	2.53

Table 4.7 DC analysis of LDO for full load using 1300 slices

Parameter	Min value	Max value
1.Output voltage in (mV)		
i) Level1 - 400	399	405.7
ii) Level2 - 450	449.3	455.7
iii) Level3 - 500	499	504.6
iv) Level4 -550	549	555.6
v) Level5-600	599	604
2.DC load current (mA)		
i) Level1 - 400	39.9	40.6
ii) Level2 - 450	39.91	40.45
iii) Level3 - 500	39.92	40.37
iv) Level4 - 550	39.93	40.31
v) Level5 – 600	39.95	40.26

Table 4.8 DC analysis of LDO without selection circuit at no load

Parameter	**Min value**	**Max value**
1.Output voltage in (mV)		
i) Level1 - 400	399.8	421.3
ii) Level2 - 450	449.7	465.3
iii) Level3 - 500	499.6	513.8
iv) Level4 -550	549.5	562.5
v) Level5-600	599.4	611.4
2. Leaker current (µA)		
i) Level1 - 400	335.2	1035
ii) Level2 - 450	377	1163
iii) Level3 - 500	418.2	1291
iv) Level4 - 550	460	1419
v) Level5 – 600	501.3	1547
3. Power dissipation(leaker in µW)		
i) Level1 - 400	134	432
ii) Level2 - 450	169.5	541
iii) Level3 - 500	209	663.3
iv) Level4 - 550	252.77	798.2
v) Level5 – 600	300.5	946

Table 4.9 DC analysis of LDO with selection circuit at no load

Parameter	Min value	Max value
1.Output voltage in (mV)		
i) Level1 - 400	399.6	411.2
ii) Level2 - 450	449.6	462.1
iii) Level3 - 500	499.5	510.6
iv) Level4 -550	549.4	559.5
v) Level5-600	599.3	608.3
2.DC load current (mA)		
i) Level1 - 400	79.31	258.3
ii) Level2 - 450	91	290.3
iii) Level3 - 500	101.4	322.3
iv) Level4 - 550	112.2	354.3
v) Level5 – 600	122.9	386.4
3. Power dissipation(leaker in µW)		
i) Level1 - 400	31.7	106.9
ii) Level2 - 450	40.9	134.1
iii) Level3 - 500	50.6	164.6
iv) Level4 - 550	61.6	198.2
v) Level5 – 600	73.6	235

4.2 AC ANALYSIS

Under this section, open loop gain of error amplifier, unity gain bandwidth and PSRR of LDO are calculated. The set up for open loop gain is shown in Figure 4.1.Graphical results of open loop DC gain and unity gain bandwidth for best case and the worst case is shown in Figure 4.2 and Figure 4.3 respectively. The setup for validating the performance of LDO in the presence of small ac signal, applied at the input is as shown in Figure 4.4.PSRR plot for the best case and the worst case is presented in Figure 4.5 and Figure 4.6 respectively.

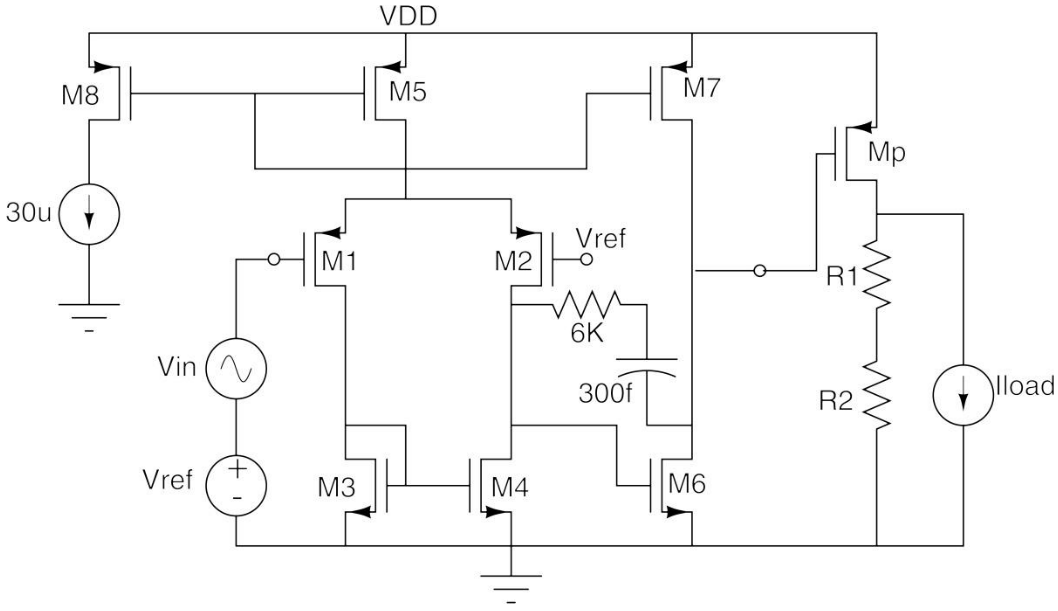

Figure 4.1 Circuit set up for open loop gain analysis

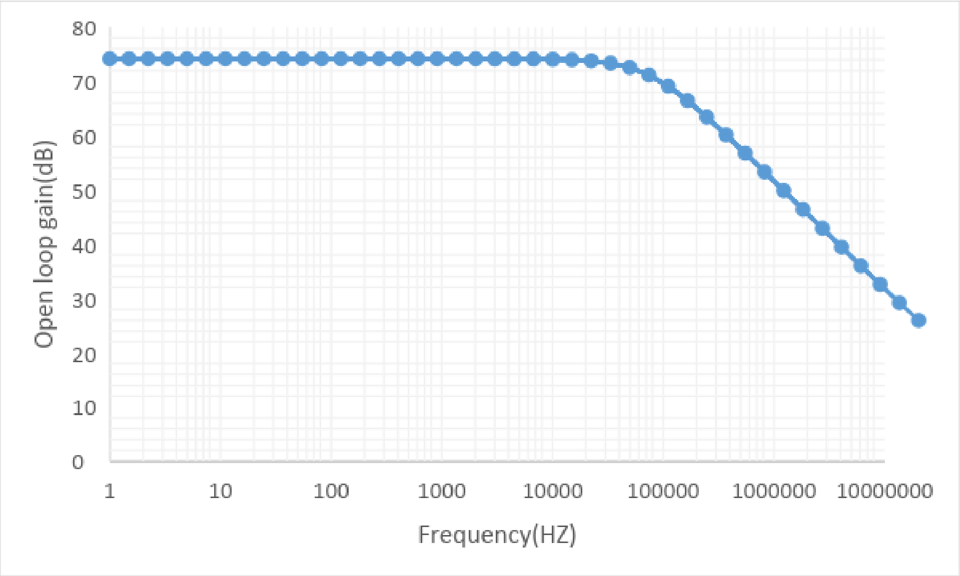

Figure 4.2 Open Loop gain best case

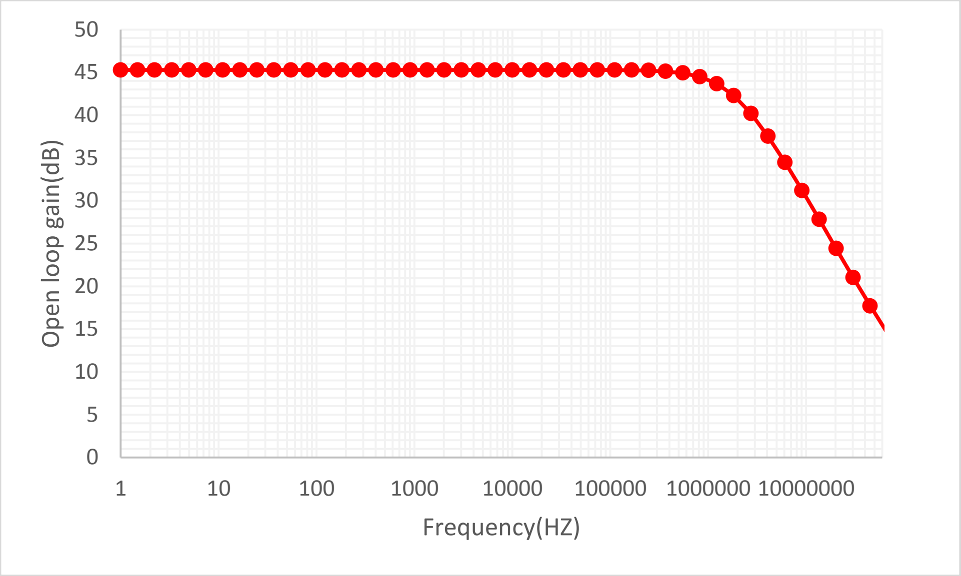

Figure 4.3 Open Loop Gain worst case

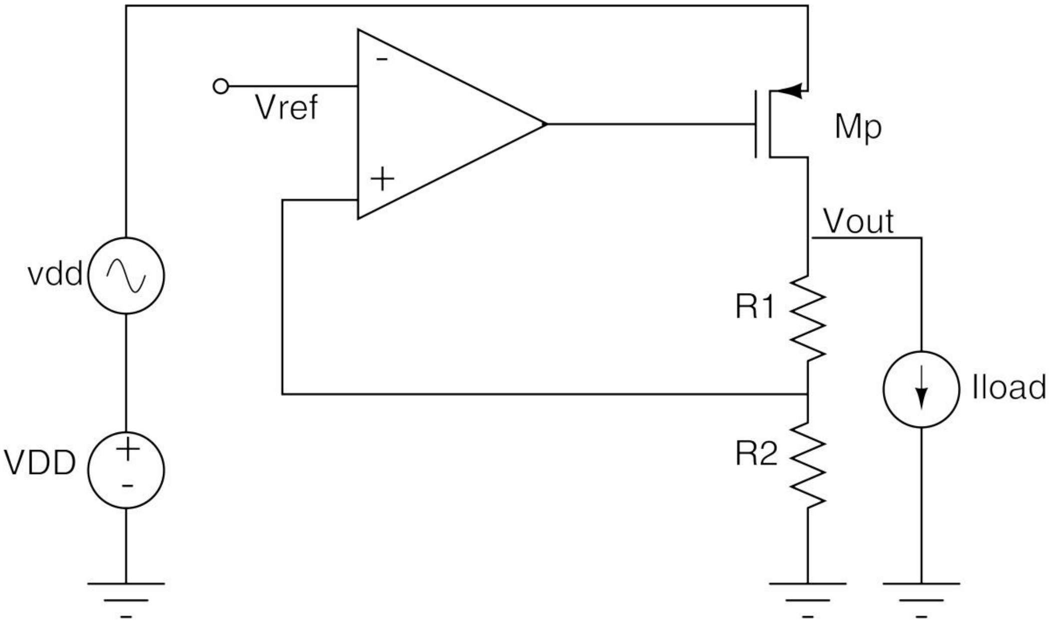

Figure 4.4 Circuit set up for PSRR analysis

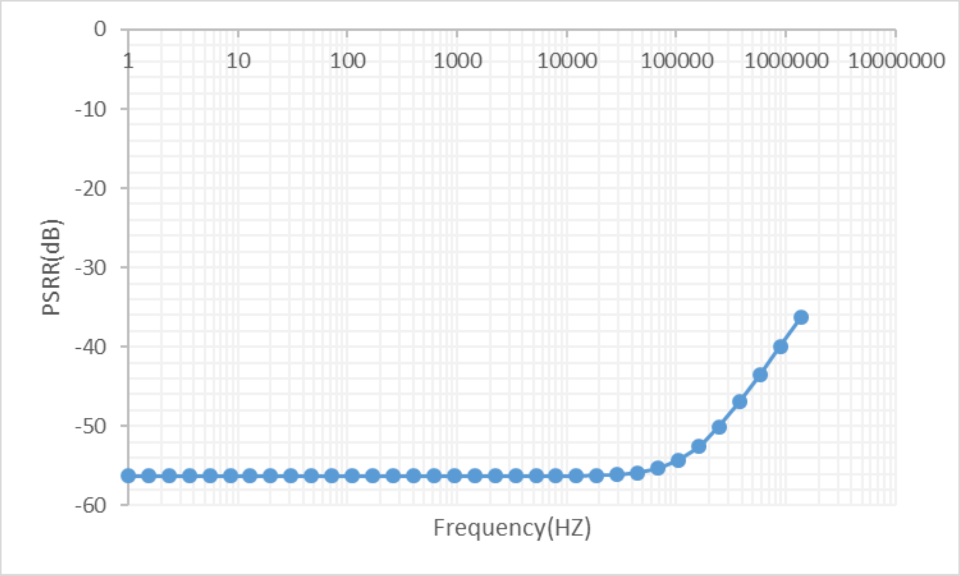

Figure 4.5 Best case PSRR

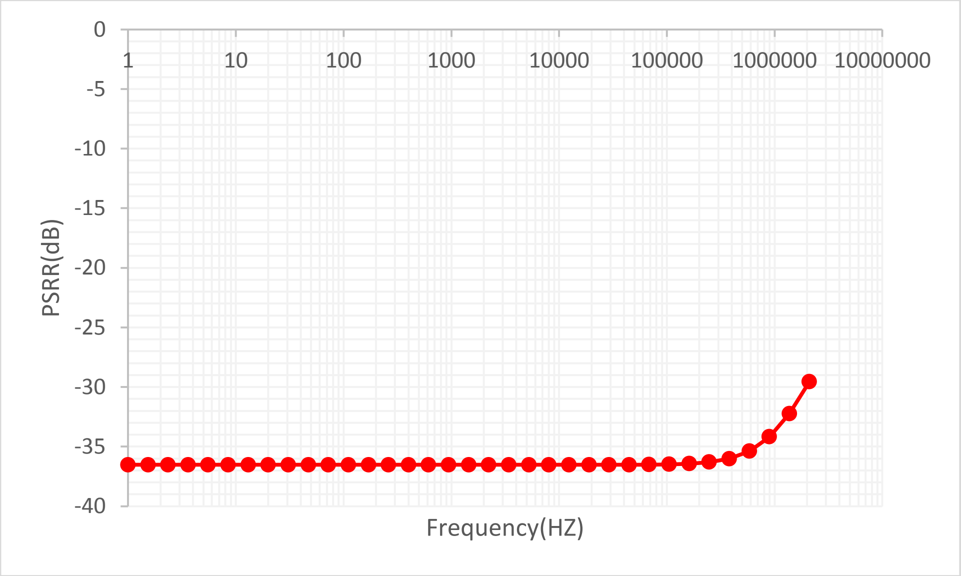

Figure 4.6 Worst case PSRR

Table 4.8 Simulation results of AC analysis

Parameter	**Min**	**Max**
1. Open loop gain (in dB)	45	76
2. Unity gain bandwidth (in MHz)	117	176
3. PSRR (in dB)		
a) DC frequency	43	56
b) 1MHz frequency	39	53

4.3 TRANSIENT ANALYSIS

Under this section, load transient regulation and line transient regulation of LDO parameters are calculated. Comparator transient analysis is also presented. Droop present in response is also presented. Circuit set up for load transient calculation is shown in Figure 4.7. The circuit basically consists of connecting a current pulse at the load end. The rise and fall time for the output pulse is 10ns. The output current pulse varies from 2.5mA-40mA. For getting the load transient response, output node is plotted with respect to time, and its variation is noted as the output current pulse varies.

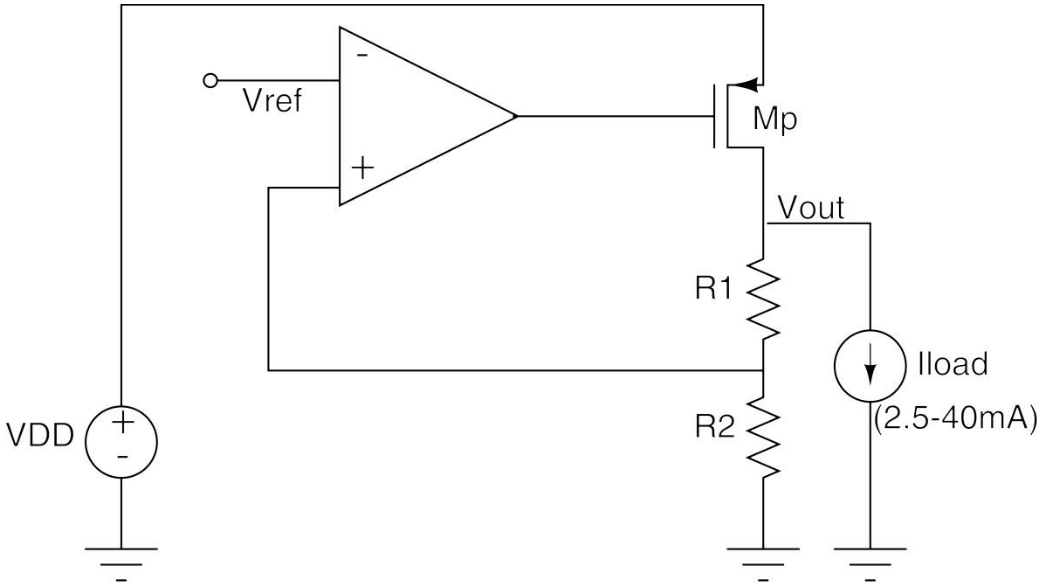

Figure 4.7 Circuit set up for load transient analysis

Undershoot and overshoot voltages corresponding to current pulse, whose rise and fall time is 10ns are coming out to be 18mV and 46 mV respectively. Droop corresponding to response is coming out to be 103mV for the worst case and 24mV for the best case. The response is settling after 24 ns, for the worst case. Load regulation plot with droop is shown in Figure 4.8 and Figure 4.9.

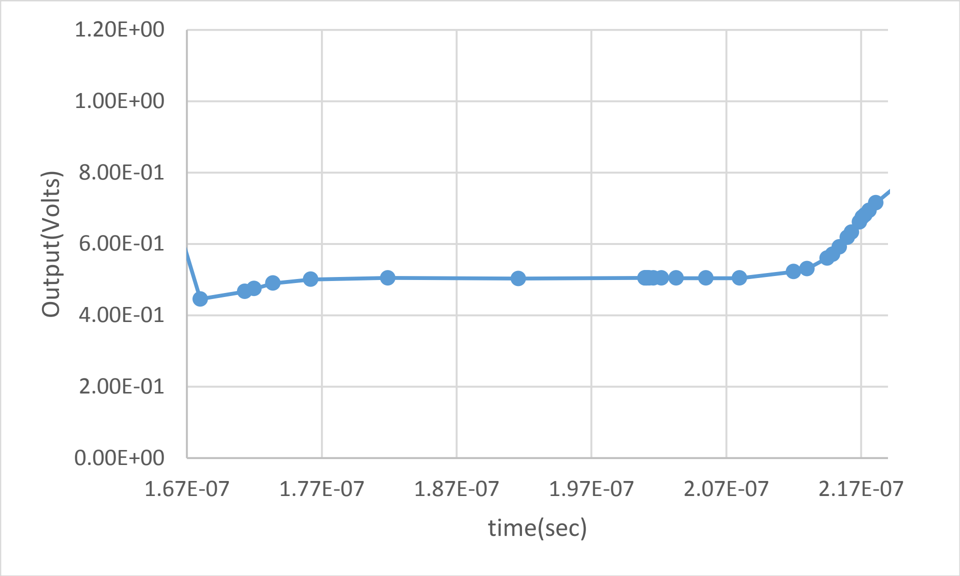

Figure 4.8 Load regulation with droop under best case

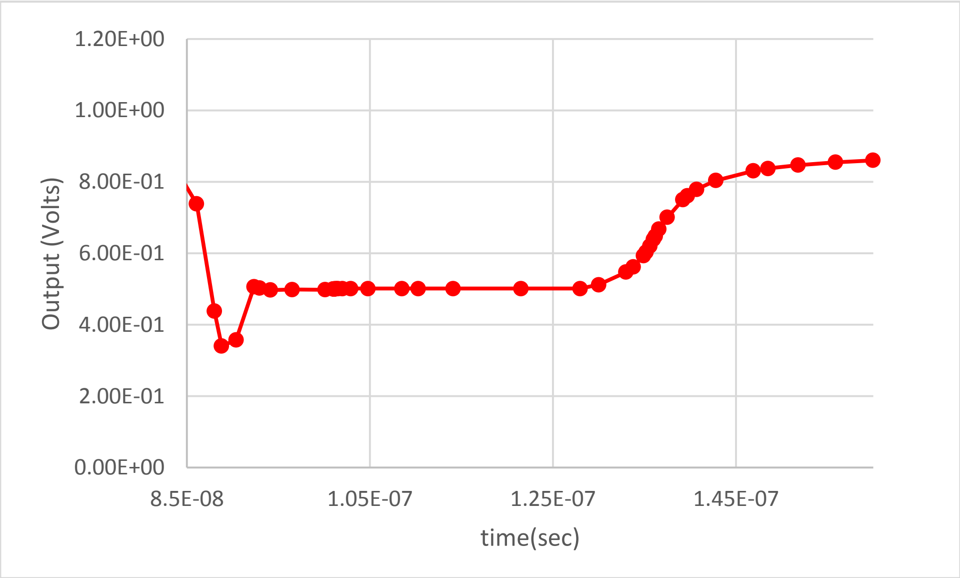

Figure 4.9 Load regulation with droop under worst case

By comparator transient analysis, offset values for the worst and the best case are found. The circuit set up for comparator for calculating offset is shown in Figure 4.10

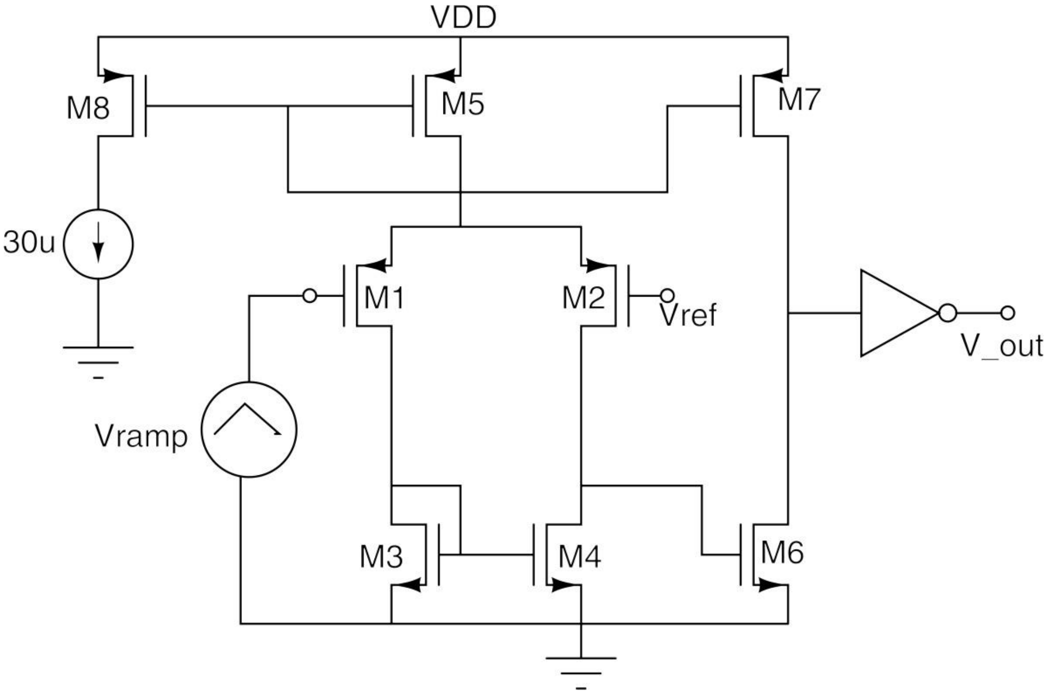

Figure 4.10 Circuit set up for offset calculation

Table 4.9 Simulation results of transient analysis

Parameter	**Min.**	**Max.**
1.Settling time	22.7	32
2.Droop(in mV)	24	103
3.Offset(in mV) a) without inverter b)with inverter	 2 0.129	 27 2.4
4.Peak current through comparator(µA)	41	171

4.4 STABILITY ANALYSIS

Under this section, simulation results corresponding to phase margin, and checking the response of LDO corresponding to the obtained phase margin are recorded. The response is checked at the output of LDO, when an enable signal is provided to the LDO. Basically, a pulse at the place of bias current is provided and the output of LDO is checked. The basic set up for finding such a response is as shown in Figure 4.11.

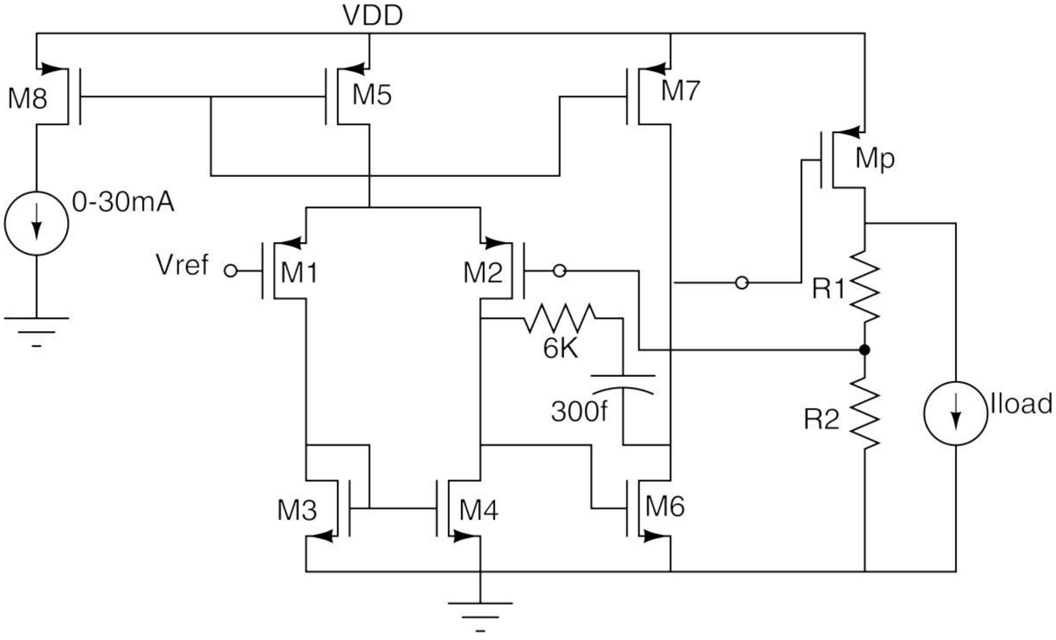

Figure 4.11 Circuit set up for stability analysis

Since, LDO is used under two different levels, values of settling time for both 90 slices and 1300 slices separately is mentioned via Tables 4.10, 4.11, 4.12 and a response corresponding to 1300 slices is plotted only. Phase margin results obtained is in between 61-80. So the response which is obtained is near to sluggish behavior, as shown in Figure 4.12 and Figure 4.13 respectively

Table 4.10 Simulation results of stability analysis for 2.5mA load with 90 slices

Parameter	**Min**	**Max**
Settling time(in ns)	12	19
Phase margin(in degree)	61	85

Table 4.10 Simulation results of stability analysis for 2.5mA load with 1300 slices

Parameter	**Min**	**Max**
Settling time(in ns)	14	27
Phase margin(in degree)	61	85

Table 4.11 Simulation results of stability analysis for full load

Parameter	**Min**	**Max**
Settling time(in ns)	13	25
Phase margin(in degree)	61	85

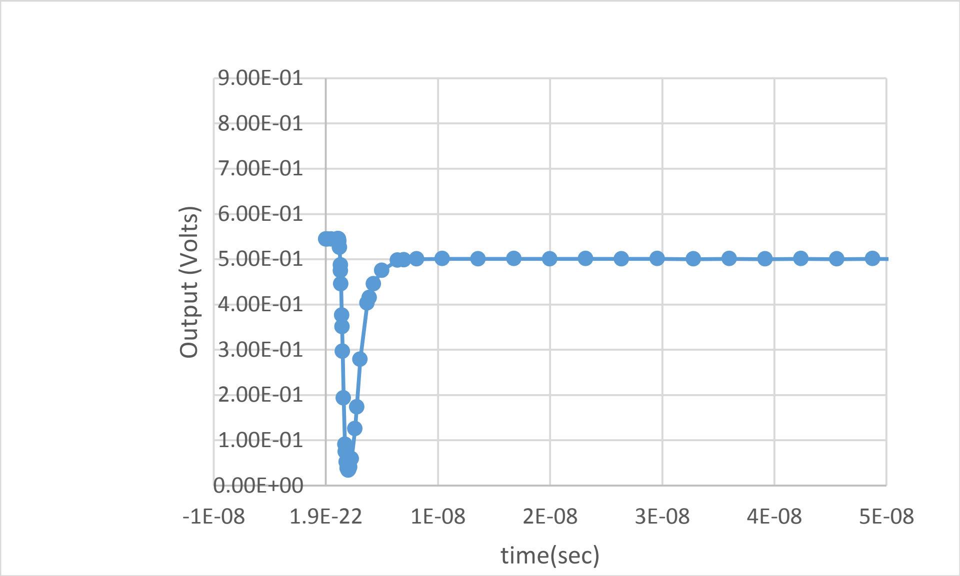

Figure 4.12 settling time with input enable best case

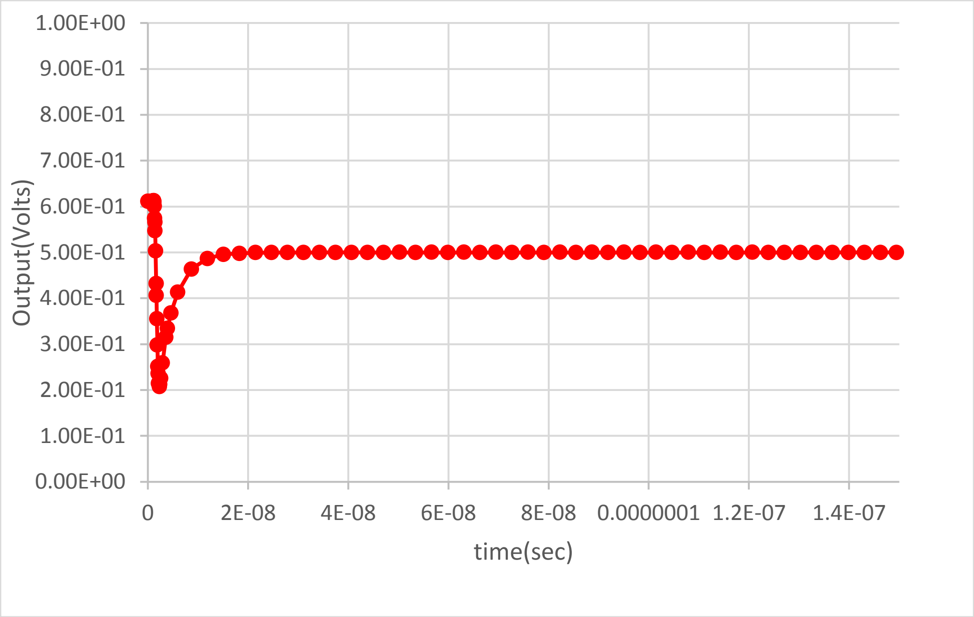

Figure 4.13 settling time with input enable worst case

4.5 **MONTE CARLO SIMULATIONS**

Monte Carlo simulations are performed under this section to check the variations in the offset value. Further variations in the resistive ladder tapping points due to mismatching in the device and different PVT conditions, with or without calibration is also noted under this section.

Table 4.12 Monte-Carlo simulation

Parameter	**Min**	**Max**
1.Offset of comparator(in mV)		
a)with inverter	0.1348	4.896
b)without inverter	2.881	34.81
Parameter	**Mean**	**Std. Dev**
2.Reference voltage(in mV)		
(without calibration)		
i) Level1 - 200	234.8	23.6
ii) Level2 – 225	259.8	26.04
iii) Level3 - 250	284.8	27.94
iv) Level4 - 275	309.8	28.10
v) Level5 – 300	334.8	30.02
2.Reference voltage(in mV)		
(with calibration)		
i) Level1 - 200	201.2	3.4
ii) Level2 - 225	225.6	2.8
iii) Level3 - 250	251.2	2.9
iv) Level4 - 275	275.2	3.1
v) Level5 – 300	300.5	2.6

4.6 PHY DRIVER ANALYSIS

The basic set up used for analyzing performance of LDO with PHY driver is as shown in figure 4.14. The driver upper arm resistance varies from 48.35 to 52.76 ohms whereas the lower arm shows a variation of 47.43-52.68 ohms across different PVT conditions. The common mode noise as well as differential outputs is plotted for the worst case across input frequency given to driver equal to 4.5 GHZ as shown in figure 4.15 and figure 4.16 respectively. The plot of alternating current for the worst conditions is represented in figure 4.17. The peak to peak value requirement for the common mode noise is coming to be 12 mV for the worst case. Differential voltage is varying from -207 mV to 208 mV. Very low variations in the alternating current are noted, and it is from 1.991 mA to 2.18 mA.

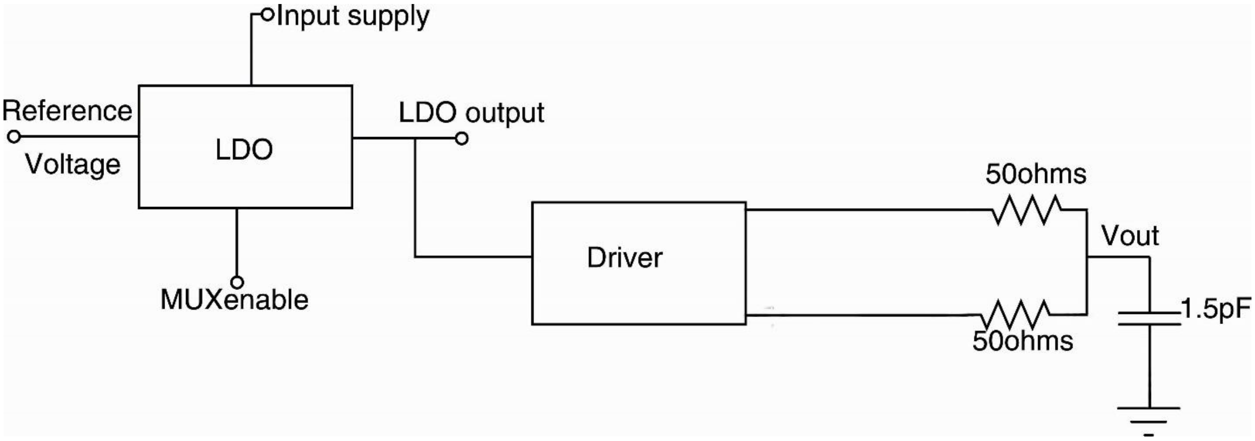

Figure 4.14 Circuit diagram for PHY driver analysis

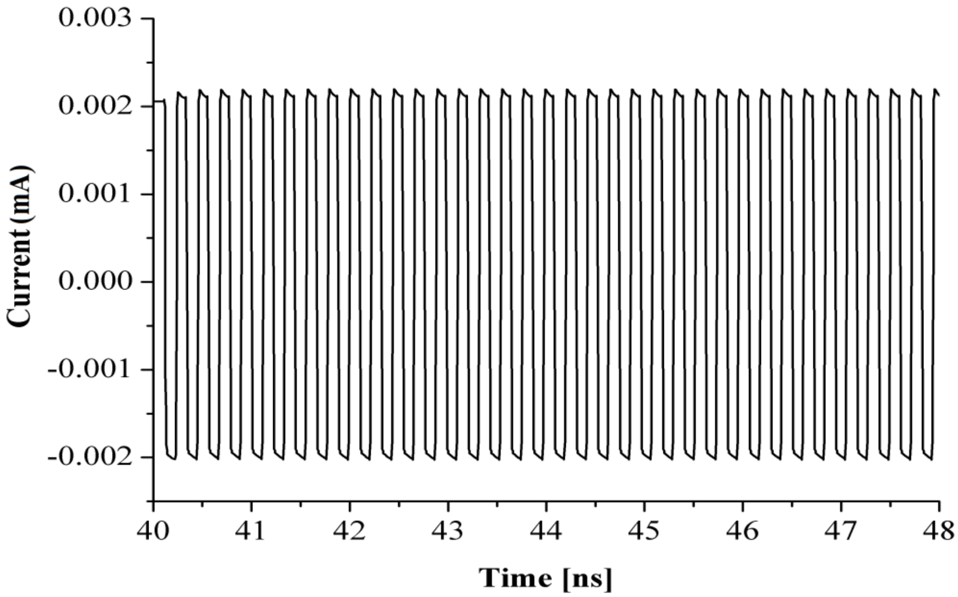

Figure 4.15 Alternating current of PHY driver

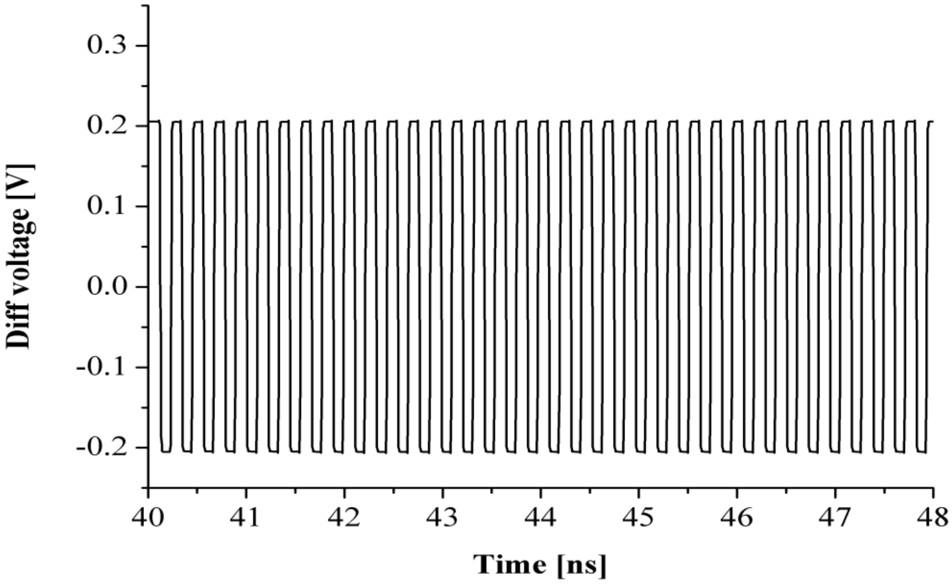

Figure 4.16 Differential voltage of PHY driver

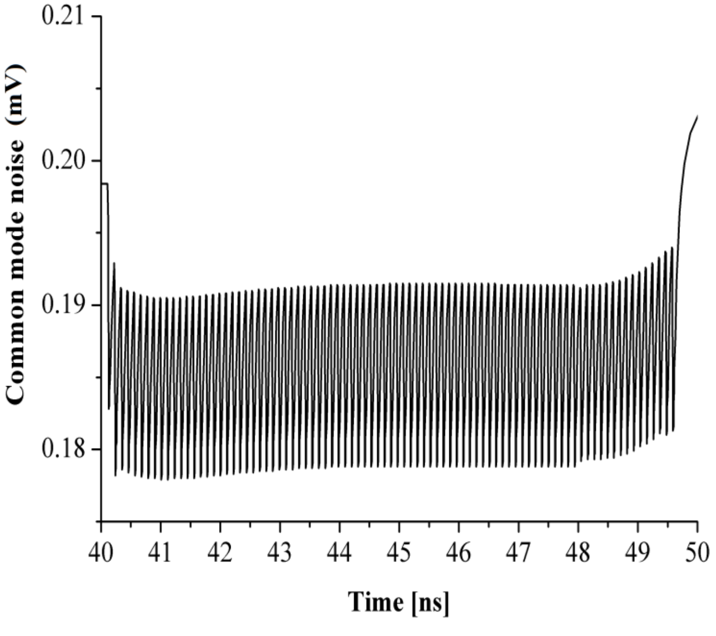

Figure 4.17 Common mode noise of PHY driver

4.7 SUMMARY OF SIMULATION RESULTS

The summary of specs of our work and how it compares with the previous work is shown in Table 4.12.

Table 4.12 Comparison table

Reference	**[12]**	**[16]**	**[22]**	**[23]**	**This work**
Year	**2013**	**2015**	**2017**	**2018**	**2018**
Technology(nm)	180	180	180	180	10
Input Voltage (Volts)	1	1.8	1.8	1.6-1.8	1
Output Voltage(mV)	0.9	1.68	1	1.4-1.6	0.4-0.6
Max. Load current(mA)	25	50	100	50	40
Quiescent current(µA)	9.3	15	32	130	96.5
Loop Bandwidth(MHz)	-	16.7	-	-	117
PSRR(dB)	-85	-73	-132	-	-39
Load cap(pF)	-	-	-	50	4.5
Overshoot(mV)	-	39	55	140	46
Undershoot(mV)	-	32	34	158	18
Settling time(ns)	-	40	-	21	22

From the comparison table, it is clear that LDO presented in thesis is designed for the latest technology of 10nm and is far lowest than other references. The overshoot and undershoot values as well as settling time are far better than other mentioned references. PSRR results of the presented LDO seem to be very less as compare to other references. Actually the reference LDO's, uses a separate compensation technique for PSRR, in order to eliminate ripples even at higher frequency. In the presented work, PSRR compensation technique is not used, as power supply has ripples at lower frequency, which can be easily curable by the value which is achieved.

CHAPTER 5

CONCLUSIONS

In this thesis, A Calibrated high performance programmable LDO, which can drive PHY drivers is designed. Designed LDO is capable of generating five different regulated voltage levels of 0.4V, 0.45V, 0.5V, 0.55V and 0.6V. Driving capability of LDO is 40 mA. For enhancing stability, stability compensation technique is used. By using the proposed compensation, phase margin in between 61-85 degrees is produced. Addition of such compensation allows the response to settle down at 22ns for the worst case, after enable signal of LDO is activated.

A special compensation technique for reducing leaker current is proposed, which results in the reduction of leaker current to around two times of that of conventional LDO. This introduced technique also helps in improving the regulation voltage at the output, especially under no load condition. In this compensation technique, by just paying for a 2:1 MUX area, we are able to save power and enhance our voltage regulation. Power supply rejection ratio of -38 dB has been noted at dc frequency and -32dB at 1MHZ for the worst case. The best value of PSRR is recorded to be -56dB at dc frequency. The regulated output voltage shows less than 3% variations, which is fulfilling our specifications.

A calibration technique is proposed for generating the reference voltage. Corresponding to five different output voltage levels, five different reference voltage levels are needed. By using calibration technique, we are able to generate five different reference voltage levels, with just a variation of less than 5mV, which was noted around 20mV for conventional resistive ladder. Static comparator with sensitivity less than 2.4 mV is also designed for calibration. Monte-Carlo simulation results for static comparator offset shows a variation up to 4.896 mV, which is under the limit of 5mV.Resistive ladder is also

When LDO is made to drive MIPI PHY driver, by using 0.4V level from its output, peak to peak voltage of less than 12mV is noted. The differential voltage is varying in between -207 mV to 208 mV and the variation in alternating current is in between 1.991 - 2.071 mA. All these results are meeting the real time requirement of driver, for connecting the transmitted data to the outer world at low switching noise and higher speed. The driver is also designed and for designing only MOS devices are employed. So, without using resistance, the upper arm of driver resistance is varying from 48.35 to 52.76 ohms and the lower arm resistance varies in between 47.43-52.68 ohms.

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