Power Aware Efficient Approximate Multiplier Design with Automated Power Rollup and Indicator

A Thesis Submitted in Partial Fulfilment of the Requirement for the Award of the Degree of

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in VLSI Design

Submitted By
SHAUVIK PANDA
601662018

Under Supervision of

Dr. ALPANA AGARWAL
Associate Professor
and
BHARATHI V
Principal Engineer
Intel Tech. Pvt. Ltd.

THAPAR INSTITUTE
OF ENGINEERING & TECHNOLOGY
(Deemed to be University)

ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT
THAPAR INSTITUTE OF ENGINEERING & TECHNOLOGY
(A DEEMED TO BE UNIVERSITY), PATIALA, PUNJAB
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CERTIFICATE

This is to certify that **Shauvik Panda (Regn. No. 601662018)**, a student of M.Tech.(VLSI Design), **Thapar Institute of Engineering and Technology, Patiala** has successfully completed one year (August 2017 – June 2018) internship programme in **Intel Technology India Pvt. Ltd, Bangalore**. His title of dissertation is "**Power Aware Efficient Approximate Multiplier Design with Automated Power Rollup and Indicator**".

During the period of his internship programme, he was punctual and hardworking.

I wish him every success in life.

Bharathi V

Bharathi V
Principal Engineer
PDS, LP

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DECLARATION

I, Shauvik Panda hereby declare that the work presented in this thesis entitled **"Power Aware Efficient Approximate Multiplier Design with Automated Power Rollup and Indicator"** in partial fulfillment of the requirement for the award of degree of Master of Technology (VLSI Design) submitted at Electronics and Communication Engineering Department, Thapar Institute of Engineering & Technology (Deemed to be University), Patiala is an authentic record of work carried out under supervision of **Dr. Alpana Agarwal (Associate Professor, ECED)** from June, 2017 to June, 2018. The matter presented in this has not been submitted either in part or full to any other university or institute for the award of any other degree.

Date: 15/6/18 ....

S. Panda
Shauvik Panda
601662018

It is certified that the above statement made by the student is correct to best of my knowledge and belief.

Date: 15/6/18 ....

Alpana
Dr. Alpana Agarwal
Associate Professor
Electronics and Communication Engineering Department
Thapar Institute of Engineering & Technology
(A Deemed To Be University), Patiala, Punjab

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DATE: 15/6/18

S. Panda

PLACE: Patiala

SHAUVIK PANDA
601662018

ABSTRACT

Power is the most valuable design metric in today's world. The reduction of power will provide competitive edge to any product. Multiplier is a versatile component in digital system and is a part of many error tolerant applications. The approximation in multiplier can enable low power by sacrificing the exact output. Performance parameters can be improved by reducing the exactness in the actual output. But this approximation needs a constant monitoring as it can temper the original functionality. Power management is also important as by doing efficient power management in terms of power aware system, a lot of power can be saved. Now, power estimation is also a big challenge to provide insight to the power projection at different stages of the design. This work revolves around the efficient approximate multiplier in terms of power and speed.

Circuit and algorithmic changes in approximate multiplier results into 61.2%, 41.2% and 49.1% power reduction using structures of Ripple Carry Adder (RCA), Carry Select Adder (CSA) and CSA with Binary to Excess 1 Converter (BEC) in comparison to the exact architecture. Speed has been improvised by 10.2%, 33.3% and 34.5%. Multi Vt structure resulted into 29.2%, 19.7% and 22.2% speed improvement for RCA, CSA, and BEC than the standard Vt architecture. Further a Gaussian filter has been implemented using this approximate multiplier. The processed image is having a less than 5% deviation in Peak Signal to Noise Ratio (PSNR) value than the exact multiplier.

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LIST OF ABBREVIATIONS

BEC	:	Binary to Excess 1 Converter
CAD	:	Computer Aided Design
CSA	:	Carry Select Adder
CSV	:	Comma Separated Value
ED	:	Error Distance
EDA	:	Electronic Design Automation
HDL	:	Hardware Description Language
HIP	:	Hard Intellectual Property
HVT	:	High Vt
KPI	:	Key Performance Indices
LSB	:	Least Significant Bit
LVT	:	Low Vt
MED	:	Mean Error Distance
MRED	:	Mean Relative Error Distance
MSB	:	Most Significant Bit
MUX	:	Multiplexer
NED	:	Normalized Error Distance
NMED	:	Normalized Mean Error Distance
PSNR	:	Peak Signal to Noise Ratio
RCA	:	Ripple Carry Adder
RED	:	Relative Error Distance
RTL	:	Register Transfer Logic
SoC	:	System on Chip
SIP	:	Soft Intellectual Property
TCL	:	Tool Command Language
UPF	:	Unified Power Format

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

Multipliers are building blocks of digital based designs. There are many operations including multimedia processing and data mining which are error tolerant up to certain extent, exact multiplications are not required for such cases. Approximation having the same stages of operation like exact but logic complexity is reduced with the inclusion of computational error with certain benefits like power, speed and area improvisation. Now to implementation of this kind of structure in a system and provide real cases of operation requires further modification of the design flow. Also each stages of design contains useful information regarding design improvement and analyzing aspects which are essential from a designer viewpoint. This thesis revolves around efficient approximate multiplier design along with power intent specification to provide system interactive capability with power awareness and automatic rollup and indicator system which will provide better visibility of the power flow. This steps will enable proper power model to provide what-if analysis before silicon is in hand.

1.2 OBJECTIVE

Designing of an efficient approximate multiplier design with the goal of low power and high speed of operation by exploring different existing techniques of architectural and implementation modification. Also proper indication of error metrics will give the quality of the output expected from the design. Then this structure included into a Soft Intellectual Property (SIP) design to get an understanding of System on Chip (SoC) level design issues and improvised in terms of power. Power intent is provided to the design and compatibity of the design is checked at each stages of design flow to design a power aware system. An automation rollup framework is provided to get the power and design information data in a single place to analyze the design after design tool implementation as manual data extraction can be a tedious task. This mechanism will inbuilt to the tool flow but only executed on tool generated reports. An indicator system will provide the performance indices of the design after implementation of each phase. It’s backed by centrally controlled database which has feature of auto updating to provide the user constant monitoring with updated collaterals.

1.3 PROBLEM STATEMENT

Basically problem statement is divided in three parts. First part of the problem has been defined as to design architecturally modified approximate multiplier circuit with the goal of low power and high speed. Secondly to design the proposed architecture based SIP design. This design can incorporated with power intent specifications which is essential for power aware design. Thirdly most of the tools in design flow dump out a series of information which are usually big and not user friendly. Rollup and indicator will sort this information, ease the job of collecting crucial information and present it in efficient manner. Designed approximate multiplier's capability in application like image processing also needs to be tested.

1.4 ORGANIZATION OF DISSERTATION

The whole thesis is divided into six chapters. **Chapter 2** describes the literature survey of existing architecture published till now. **Chapter 3** tells about power intent specifications and its approach. **Chapter 4** deals with the proposed architecture for modified approximate multiplier circuit and power aware multiplier system. Also rollup and indicator system methodologies are discussed. **Chapter 5** describes results of our modification of approximation multiplier circuits, power aware analysis and automation works. **Chapter 6** presents conclusion and future scope of proposed methodologies.

CHAPTER 2

LITERATURE SURVEY

2.1 OVERVIEW

For over a long time the main design parameter of digital design is based on three parameters namely area, power and speed. But over a decade due to development of error tolerant systems in different applications such as multimedia processing, signal processing, image processing etc. accuracy also became an important parameter to play to break the bottleneck of above mentioned three parameters. So in such applications instead of exact multiplier approximate multipliers are introduced. In this chapter the approaches towards this idea has been discussed. Also discussion of the existing low power design approaches and power intent specifications for betterment of design has been included.

Khaing Yin Kyaw *et al.* [1] in their proposed an algorithmic approach of multiplier design where the input to the multiplier is divided in two parts (i) non-multiplication part to give the lower order bits of the final output and (ii) multiplication part to generate the higher order bits of the product. The Least Significant Bit (LSB) related part will only check for 1 in the input pattern after which it will take 1 as output otherwise 0. The whole operation can be implemented with any number of inputs with no hard and fast rule that these parts should be equal. The choice of two parts depends upon the resulted error acceptance threshold values. In their design they conclude that with more no of input bits this approach can give better results. Due to less logic complexity both power and area is reduced.

Parag Kulkarni *et al.* [2] proposes an approach of architecture modification of multiplier block where inaccuracy is introduced only when all the input bits are 1. From the analysis of truth table and simplification they conclude that if the output in the case of all 1's in the input is truncated then the logic implementation of multiplier will be using less numbers of gates for their operation. With this approach for 2x2 multiplier block approximation uses only three output lines instead of four. This will results into forming a multiplication block with no XOR gates. Also the critical path delay in this case will be less by one gate delay compared to conventional structure. The error is present with a magnitude of 2. Larger multipliers are built by using the inaccurate 2x2 block to produce partial products and then adding the shifted partial products. Although error probability is increased with this approach the mean error is more or less almost same with input bit width increase.

Chia-Hao Lin *et al.* [3] purposed an architecture based on approximation of Wallace tree multiplier. For conventional approach of Wallace tree multiplication contains stages depending on the partial products which is reduced in terms of partial product accumulation stage. This stage includes full adder, half adder and compressor structures. In their design at the stage of partial product reduction phase inaccurate 4:2 counter and use a 2:1 Multiplexer (MUX) to replace a XOR gate. The difference between an inaccurate 4:2

counter and an ordinary counter is that an ordinary counter gives the sum 100_2 when all four inputs are 1, but an inaccurate 4:2counter simplifies the architecture by using two bits to present the 3-bit result. With this inaccuracy power and area is reduced where speed is increased.

Vaibhav Gupta *et al.* [4] proposed an inaccurate or rather say approximate adder structure which can be used in many application including multiplication. Their proposed design contains schematic level of changes with main goal of switching power reduction with less number of transistor use. Upon reviewing the full adder output combinations they conclude total four approximate full adder circuit with different error in sum and carry bit. With all these four one approximation with the observation of sum is actually inverted version of carry output in six cases out of eight contains the less amount of error.

Cong Liu *et al.* [5] described a structure combining approximation and error correction. In their approach they preprocessed the input data based on the interchangeability of bits with the same weights in different addends to form propagate and generate signals which fed into parallel adders to reduce the delay. The preprocessed input data processing performs on interchangeability of same weight input bits. Here instead of carry propagated to the higher bit which in turn increased the delay, an error signal is produced in parallel. These error signals are preventing the propagation of carry signal. These error signals are produced at each stages of operation can be added after each stage. This error signals are accumulated after each stage. To reduce the error, this accumulated error vector is added to the adder tree output using a conventional adder to produce final stage output. This configurable error recovery that can produce more accurate results.

Zhixi Yang *et al.* [6] provided architecture of approximate multiplier with main modification of compressor circuit. They improvised the 4:2 compressor circuit by introducing error cases in four cases out of sixteen in case of sum generation and one case in case of carry generation. As the partial product being generated as one is less probable case the above mentioned modification is done on the case of maximum occurrences of ones in input of compressor. Now the total multiplication is divided into three parts where LSB related inputs are truncated, middle part is computed using approximation and Most Significant Bit (MSB) related part is computed with accurate compressors. Use of truncation and approximation is to reduce area and power where accurate computation is to achieve more accuracy.

Amir Momeni *et al.* [7] proposed two designs related to approximate multiplier circuit where both of the design is based on modification of 4:2 compressor circuit. Conventional 4:2 compressor which can be used in a multiplier can have four normal input, one previous stage carry input and it produce one sum and two carry signal using two full adder structure as final result. In modification stages of approximation carry in the second stage made equal to the input carry which in turn produces an error of decimal value of 2 because of binary weight difference. This difference is made back to value 1 with changes in sum and other stage carry network expression. Both of this two output carry having same binary weights can be interchangeable in terms of implementation. The proposed design shows improvement in delay and power due to approximation scheme.

Srinivasan Narayanamoorthy *et al.* [8] proposed an approach of selecting only a part of input operand and multiply only the selected segment instead of input operand. Their approached design select segments from the input operand is greater or equal to the half-length of the inputs. Segment can start only from one of two or three fixed bit positions depending on where the leading one bit is located for a positive number. This approach can provide much higher accuracy than one simply truncating the LSBs, because it can more effectively capture more noteworthy bits. For the final result of this multiplier is the expanded version of the output of segment input multiplier result. For this segmented approach they replaced the leading one detector circuit and shifters with less complex OR gates and MUX structure at the expense of accuracy. As all the auxiliary circuit design is primarily depends on the segment selection, the variability of segment choice gives a very high design flexibility.

David May *et al.* [9] provide a new set of approximation approach based on voltage over scaling. As supply voltage is inversely proportional to the delay of the circuit, this criteria can be explored to achieve the approximation goal. In their approach initially they find out the timing data as well as fan in information each endpoints of design. As the error tolerability is fixed, the inputs of this end points are connected with circuitry of scaled voltage. Scaled voltage naturally reduces the energy consumption of the whole circuit where the timing violation will provide the approximation of results.

Georgios Zervakis *et al.* [10] explored a new space for applying approximation in multiplier circuit. In their approach they applied perforation in the partial product generation stage. The partial product perforation technique omits the generation of some successive partial products starting from a specific position. A perforated partial product is not inserted in the accumulation tree, and hence some full adders can be eliminated. This approach is different with the truncation method where removing circuit elements is done on the accumulation of partial product stage. The proposed technique omits a number of partial products enabling high area and power savings while retaining high accuracy.

Jinghang Liang *et al.* [11] in their work proposed new metrics for evaluating the reliability as well as the power efficiency of approximate and probabilistic adders. In every approximated circuits errors are introduced which is reflected in output. To check this error level they defined basically three error metrics named as error distance, mean relative error and normalized error distance. Error distance (ED) will basically provide the absolute difference between accurate and error value. Then mean error distance (MED) is basically mean of error distances for all possible outcome of each input which is very useful to determine reliability of implemented design. Where normalized error distance (NED) is metric to compare error between two different designs as it depends on operand bits. The MED is, therefore, useful in assessing the effectiveness of an approximate or probabilistic implementation, while the NED is useful in characterizing the reliability of a specific design

Tanay Karnik *et al.* [12] although talks about challenges for Computer Aided Design (CAD) because lowering the process nodes there problem definition and solution measure is worth mentioning. For switching power reduction they talk about dual Vcc structure for a system. In that system approach for latency non-critical block and throughput essential blocks can use low Vcc for reducing power and maintain the timing requirement. For leakage power reduction use of high Vth cell is recommended but at the expense of timing. Combination of low Vth, high Vth and standard Vth cells are used to meet the leakage power reduction and timing demand. Also stacking effect is also explored for the purpose of leakage power reduction.

Kaushik Roy *et al.* [13] provides overview of leakage mechanism and their reduction methods in their paper. As the process nodes are shrinking leakage power becomes a point of concern for overall power scenarios. The leakage currents like gate tunneling current, sub threshold leakage current, reverse bias leakage current, Gate Induced Drain Leakage (GIDL), punch through etc. not only degrades the performance whole design by effects like Vth roll off, Drain Induced Barrier Lowering (DIBL), injection of carriers into oxide etc. but also increase the overall power consumption. To overcome these effects they suggested different approaches at different level of implementation. For channel engineering modification halo doping and retrograde doping could be beneficial. Where in case of circuit level of reduction stacking effect and different multiple Vth based design will be best to implement.

Stefan Hadjis *et al.* [14] in their paper provided a solution to the area reduction method in any design. Only structural changes are not the only solutions for efficient design, algorithmic changes can also do the same. Resource sharing is a key area-reduction approach in high level synthesis in which a single hardware functional unit is used to implement multiple operations in the high level circuit specification. With this approach by using multiplexer architecture certain resources can be shared between different operands. Special care should be taken to identify the shareable and unshareable cases. This optimization technique after synthesis will results into lesser area and lesser power.

UPF stands for Unified Power Format is an IEEE standard [15] used to design power aware design. UPF is designed to reflect the power intent of a design at a relatively high level. In a complex design structure it's very much required to provide low power strategies in a systematic approach. And doing so we have to make sure the design operation is not compromising. Power domain and their supply connections is to provide the different power island architecture which is very efficient in terms of power reduction. Different strategies like level shifting, Isolation and retention provide the justification to the power intent of the design, power states are provided for summarize the power management scenarios. Different boundary conditions can also applied using this format.

Venkatesh Gourisetty *et al.* [16] proposed SYNOPSYS tool flow along with UPF. UPF addresses the need for a common standard to describe low power design intent. It helps improve the way complex integrated circuits can be designed, verified, and implemented. The purpose of the UPF is to provide portability of low power design specifications that can be used with a variety of commercial products throughout an electronic system design. The Register Transfer Logic (RTL) and UPF descriptions are contained in separate files so that they can be maintained and modified separately. To make the design power aware each stage of design flow namely RTL simulation, synthesis, placement and routing should be verified with the UPF. Each tool modifies the UPF according to their implementation which fed to the next stage. The basic intent is never change and after each stage validation of generated UPF with the implemented design is a must case scenario. As the main UPF is defined at higher abstraction level they implemented UPF based design flow up to physical layout point.

CHAPTER 3

POWER INTENT

3.1 OVERVIEW

A power aware system contains the power intent of the design which has to be in some common format. It has been done by specifying UPF. Introduced by ACCELLERA and now being an IEEE standard UPF provide all the strategies for low power intent specified. But to make it work the power management components specified with UPF must be implemented in RTL, inferred exactly in synthesis and placed and routed efficiently. One of the key point to remember is that everything defined in the UPF must also be present in the logical hierarchy. Also UPF never contains information regarding place and route. Syntax of UPF similar to TCL interface which being a common scripting language used in industry standard Electronic Design Automation (EDA) tools makes it easy to write. The simple methodology of UPF flow across common VLSI design flow is shown below in Figure 3.1. where UPF' and UPF'' are tool modified UPF.

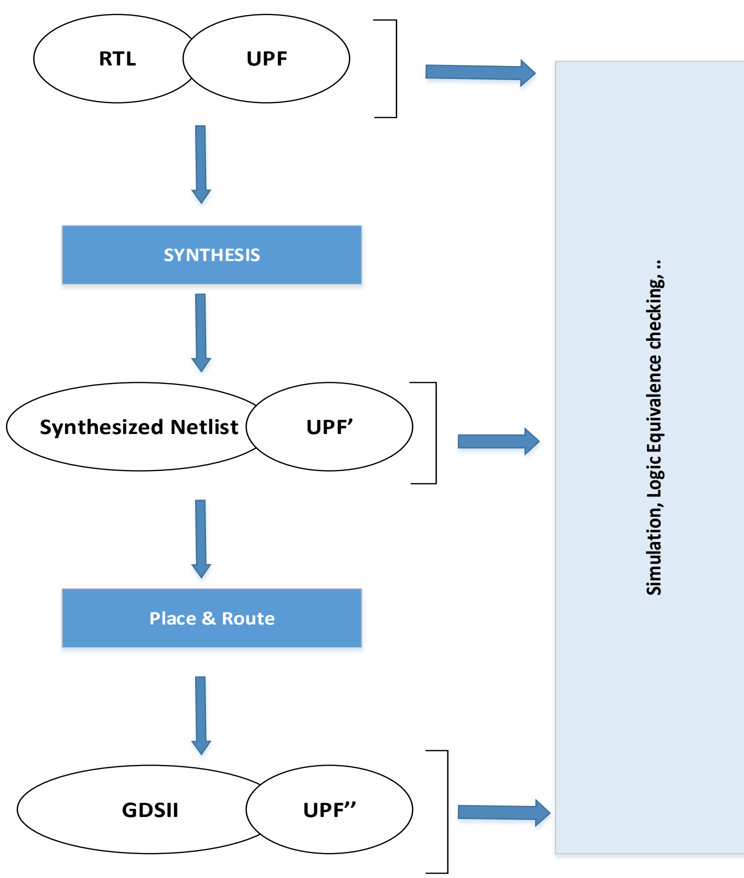


Figure 3.1 UPF Methodology Flow

3.2 UPF ELEMETNS

To specify the power intent of a design UPF requires certain elements. They incorporate with low power strategies specified in power intent. Proper strategies are required for implementing this elements. Below are the description and example of these elements.

3.2.1 Power domains

Power domain is basically creating a boundary, inside which elements are working with a same voltage. Creation of different power domains in a design felicitates the benefits of using power island architecture to improve the performance. Each domain can have many supply nets either gated or ungated. But they have one primary power and ground net. Each cell inside a power domain if not specified will be connected to the primary supply nets. Power domain creates an ease of connection between elements operating under same voltage. A sample of created power domains named as Pd_default, pd1, pd2 in an UPF is shown below in Figure 3.2, where each power domain primary supply is denoted as power and ground. For each domain power supplies are connected through nets and ports. Here three supplies 0f 1.05V, 0.85V, ground are considered as Vcc_1p15, Vcc_0p85 and vss.

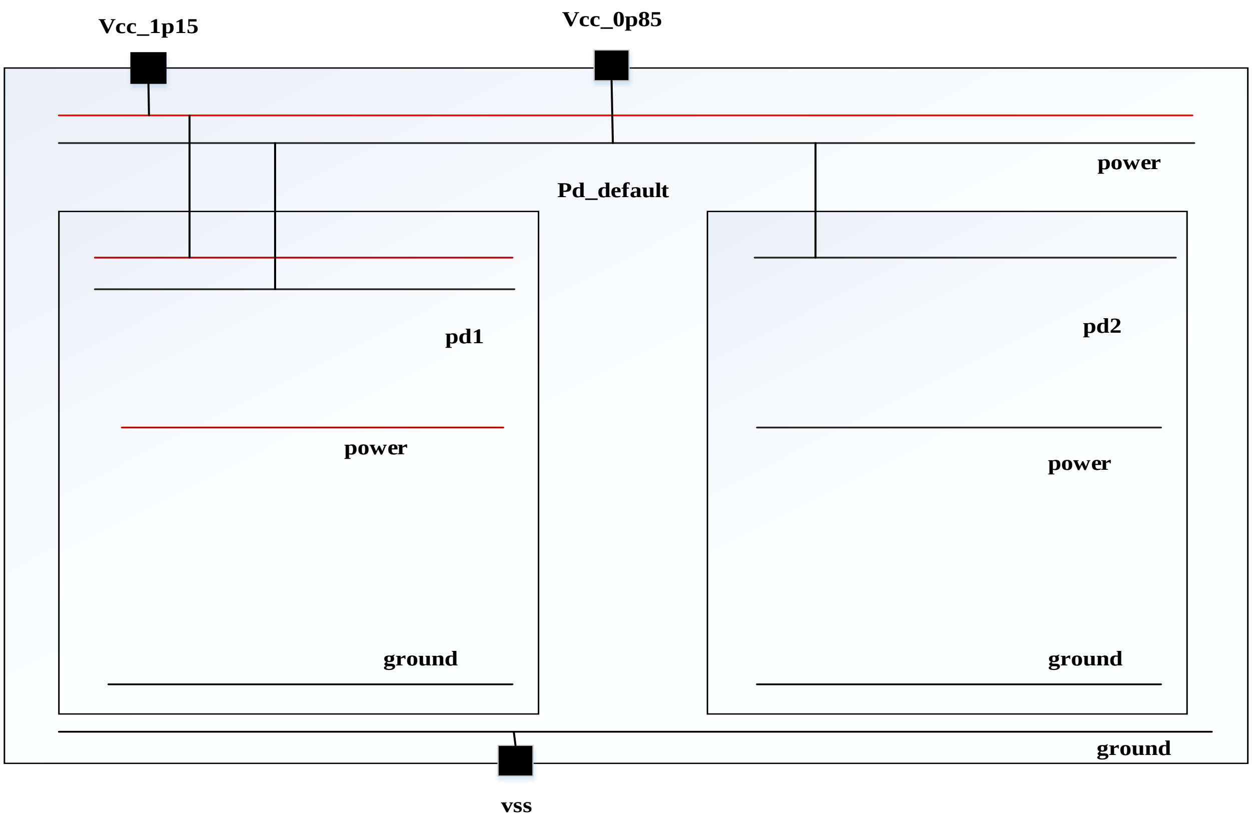


Figure 3.2 Power Domains and Connections

3.2.2 Power switches

To enable the power gating by switching, part of the design is switched off using power switches specified in UPF. Power domain having power switches always use gated supply net as their primary supply. Depending upon the power management module signals turning on and off mechanism of power switches are decided. Power switches has at least one input and output supply port. Upon activation of this switch, output port is shut down which means no power. Power switches are extremely beneficial to turn off redundant design elements in different operations to save power. Insertion of the kind of switch say power switch using PMOS or NMOS depends upon the functionality of power switch. These switches are typically inserted at placement and routing stage. Overview of power switches namely sw1 and sw2 creation in an UPF along with power domains to make switchable domains is shown below in Figure 3.3.

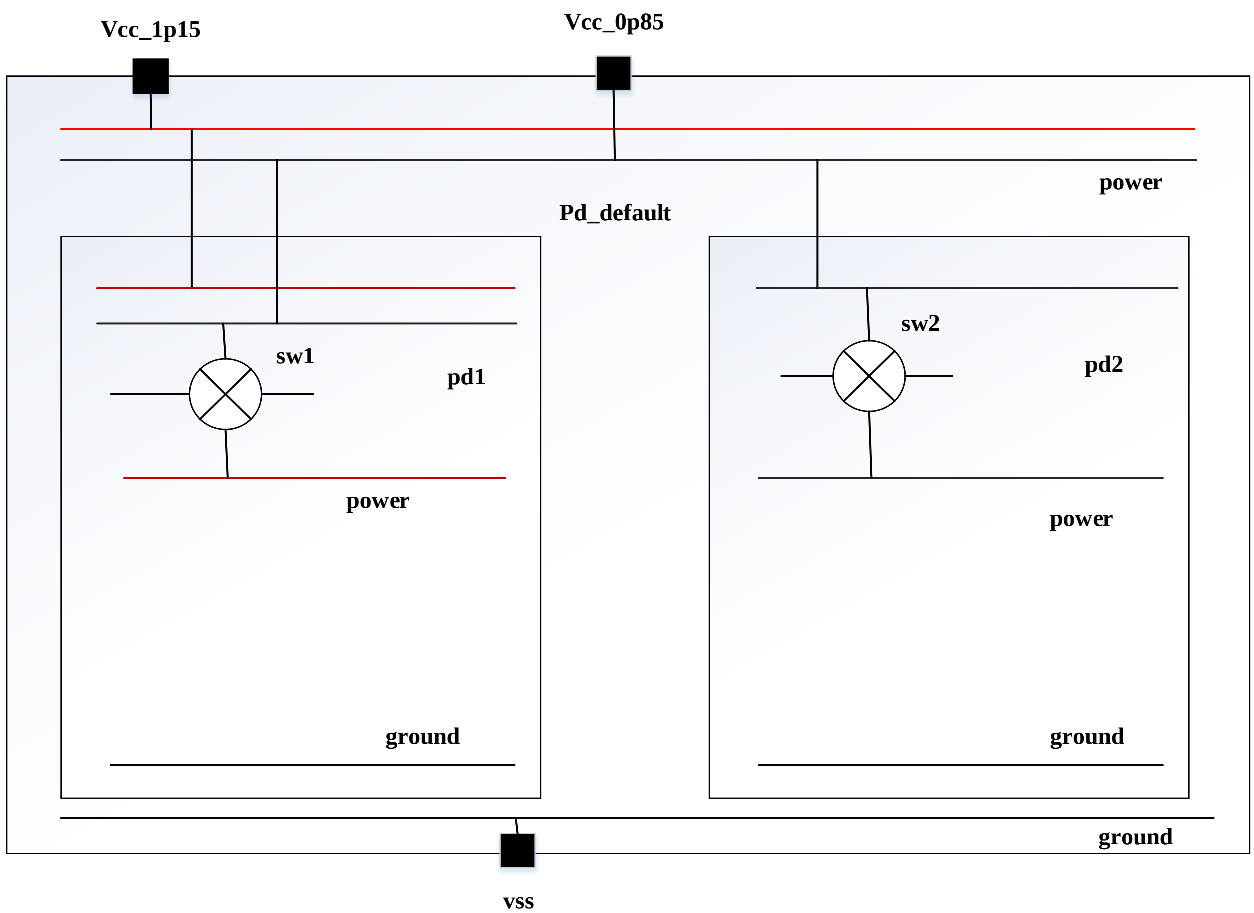


Figure 3.3 UPF Diagram with Power Switch and Power Domain Connection

3.2.3 Isolation cells

For connection between switchable and always on domains in design, isolation is essential. Whenever a switchable domain act as an input to switchable or always on domain there are cases when input to those domains may float to unknown values due to switching operation. This will in turn cause malfunction of the design due to unknown or gibberish data as well as rise in the short circuit current due to floating input. Isolation cell will clamp the output of the outputs of switchable domain in case of switching to a known value to provide proper functionality of the design. Depends upon the clamp value e.g. 0 or 1or known value along with isolation sense value e.g. Low, high different isolation cells are inferred e.g. AND, OR, latch. Clamp value 0 with isolation sense 0 will infer an AND gate whereas clamp value 1 and isolation sense high will infer to an OR gate. It’s worth mentioning that power supply to the isolation cells will be always on supply nets not the gated one. In UPF isolation strategy always accompanies with the isolation control methods. Two isolation cells named as iso1 and iso2 for two different domain and their supply connection is shown below in Figure 3.4.

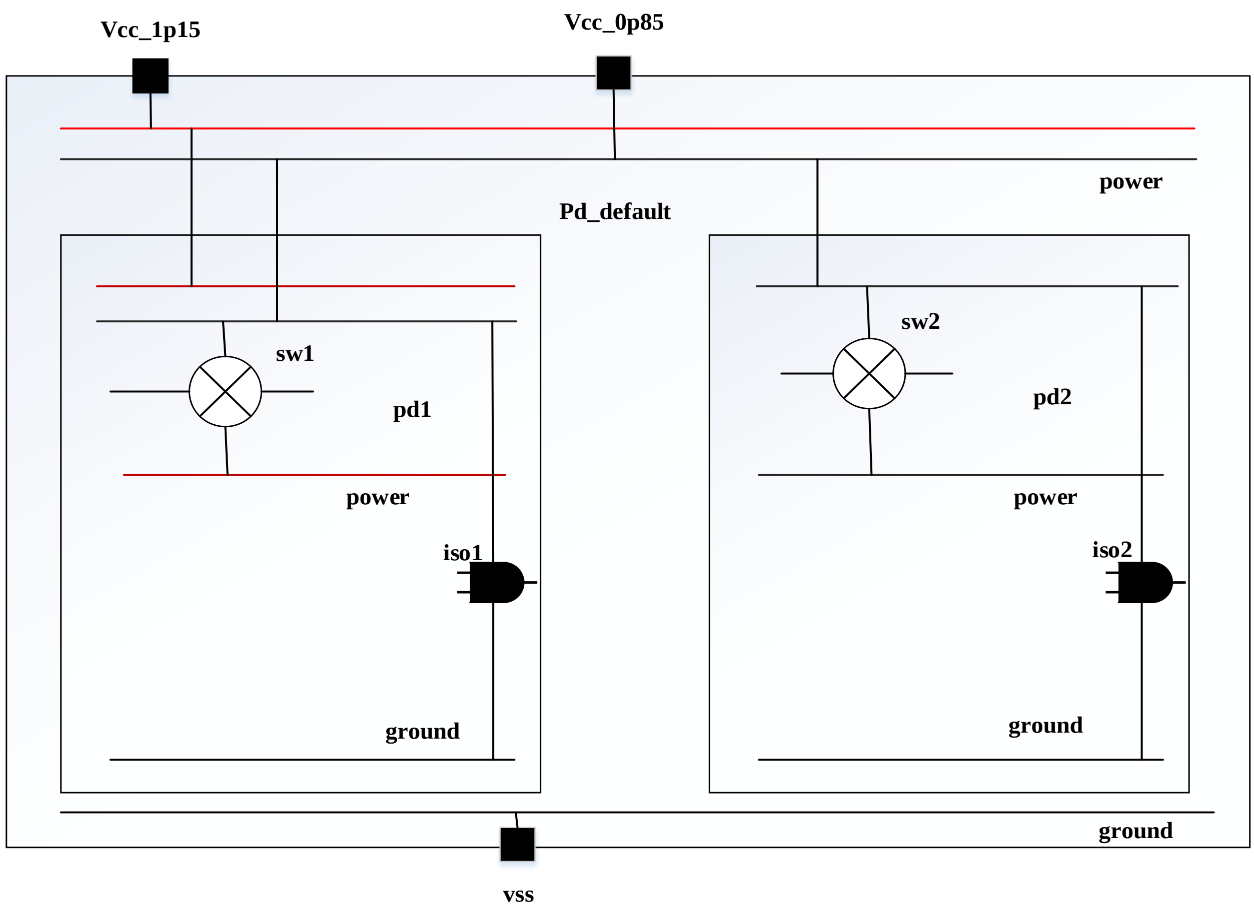


Figure 3.4 UPF Diagram with Isolation cells, Power Domain and Power Switches

3.2.4 Level shifter cells

Interactions of different power domains based on their different operated voltage needs some modification. As different power domain has different voltage levels, signals interacts with these domains or in between needs voltage shifting methodology for proper information interchange and intact credibility of design function. UPF implements this level shifting strategy based on the requirement. Two type of level shifting cells are available High to Low and Low to High. Location of these cells are based upon the design constraints. These level shifters can be applied to outputs as well as inputs of the elements of the power domain. Level shifter cells will provide proper functionality with multi voltage based designs. An implementation of level shifter cells for domain pd1 is shown below in Figure 3.5, where Ls_in and Ls_out will apply for inputs and outputs for the domain elements.

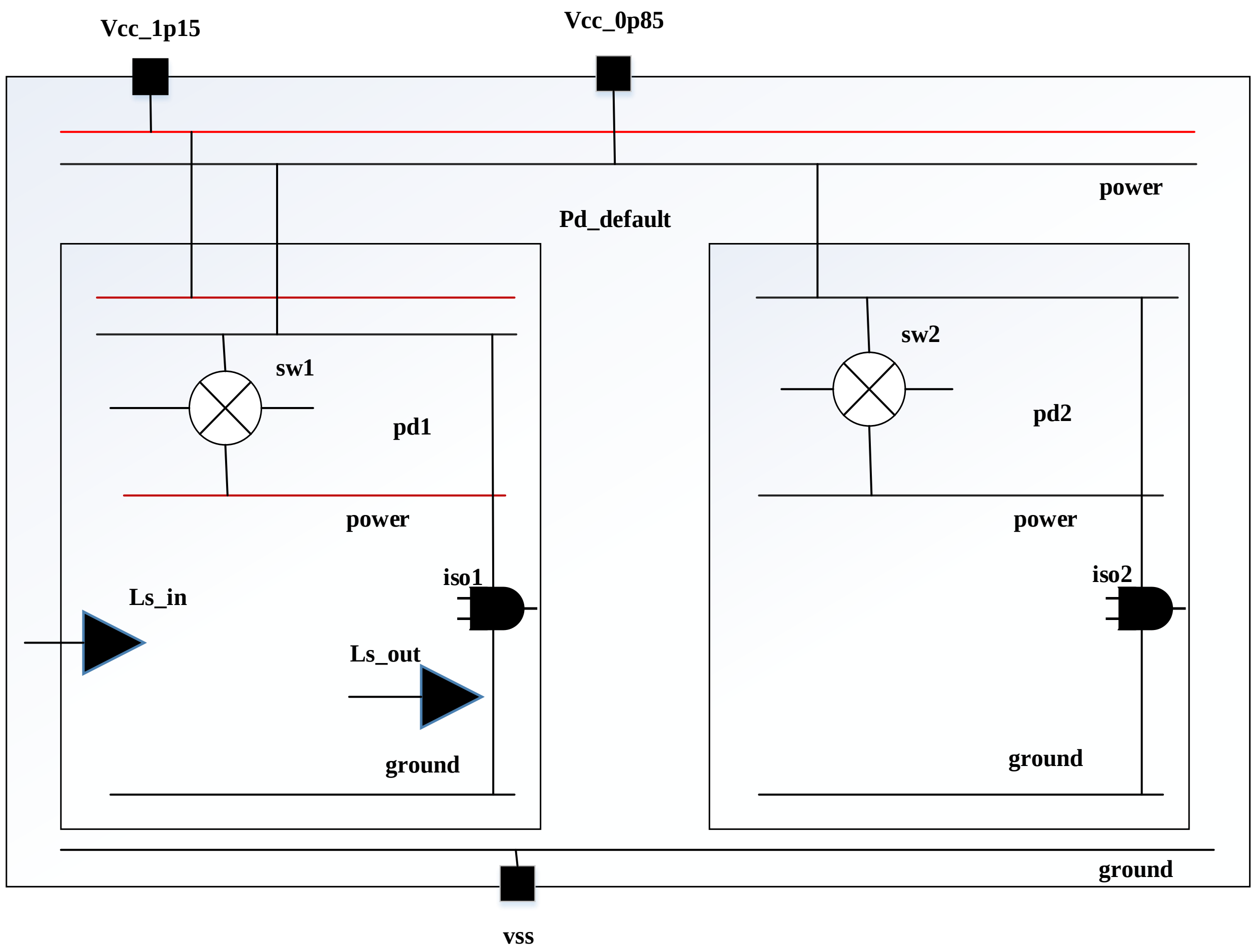


Figure 3.5 UPF Diagram of Implementation of UPF Elements

3.2.5 Retention cells

These cells are basically registers which serves a special purpose. When a power domain is shut off or go into sleep mode, there are some state values that needs to be stored. These values are needed when that domain is active again. Retention cells specified by retention strategy serve this particular purpose. Save and restore signal specified in the retention control strategy will control its operation. An example of retention strategy applied on a D flip-flop is shown below in Figure 3.6.

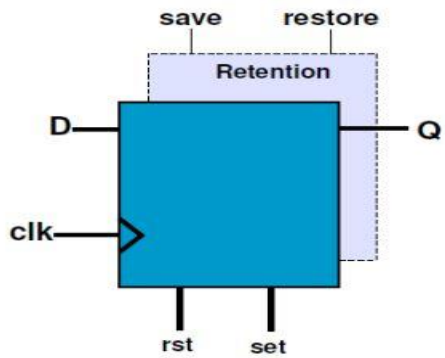


Figure 3.6 Retention Strategy

3.2.6 Power state tables

A power state table defines the legal combination of states that can exist simultaneously during the operation of the design. A power state table is a set of power states of a design in which each power state is represented as an assignment of power states to individual power nets. A power state table of a design captures all the possible operational modes of the design in terms of power supply levels. An example of power state table is given in Table 3.1 to provide an insight of power state situations.

Table 3.1 Power State Table

State_name	**Vcc_0p85**	**Vcc_1p15**	**Vcc_0p85_gated**	**Vcc_1p15_gated**	**Ground**
ALL_ON	ON	ON	ON	ON	ON
PD1_ON	ON	ON	ON	OFF	ON
PD2_ON	ON	ON	OFF	ON	ON
PRE_BOOT	ON	ON	OFF	OFF	ON

CHAPTER 4

PROPOSED METHODOLOGY

4.1 OVERVIEW

This chapter deals with architectural modifications that have been used to improve the performance parameters of an Approximate Multiplier. Along with this the power intent verification methodology is also discussed. Lastly, power rollup and indicator methodology have been discussed for the betterment of design flow output understanding.

4.2 APPROXIMATE MULTIPLIER

Approximation circuits can be applied to any multiplier to improve its power, area and delay at the expense of quality. Here approximation is applied to the DADDA multiplier architecture. The approximate multiplier design approach is mainly divided into three major parts. Firstly, modification of the generated partial products in terms of probability. Secondly, approximation of the partial product accumulation circuitry for the partial product reduction. Last one is the addition of generated sum and carry from partial product reduction tree by vector merging to get the final product.

4.2.1 Partial product alteration [17]

In normal or exact case, partial products are basically produced by AND operation bit by bit between multiplier and multiplicand. Approximation or alteration of these partial products has been set as the first goal to achieve the approximation. In the design, the partial products are being altered with a column of more than three elements to propagate and generate the signals. These signals are basically alteration of partial products by clubbing two partial products of same weight using AND or OR operation. This will not reduce the number of total partial products but this will help in next accumulation stage for applying approximate circuits. Generation of these signals has been given by equations 4.1 to 4.3.

$$a_{m,n} = \alpha_m . \beta_n \tag{4.1}$$

$$p_{m,n} = a_{m,n} + a_{n,m} \tag{4.2}$$

$$g_{m,n} = a_{m,n} . a_{n,m} \tag{4.3}$$

Where α, β are two unsigned 8-bit input operands represented as given in equations 4.4 and 4.5.

$$\alpha = \sum_{m=0}^{7} \alpha_m \, 2^m \tag{4.4}$$

$$\beta = \sum_{n=0}^{7} \beta_n \, 2^n \tag{4.5}$$

Figure 4.1 depicts complete picture of how all the partial products for an 8-bit DADDA multiplier will look after alteration along with binary weights associated with them.

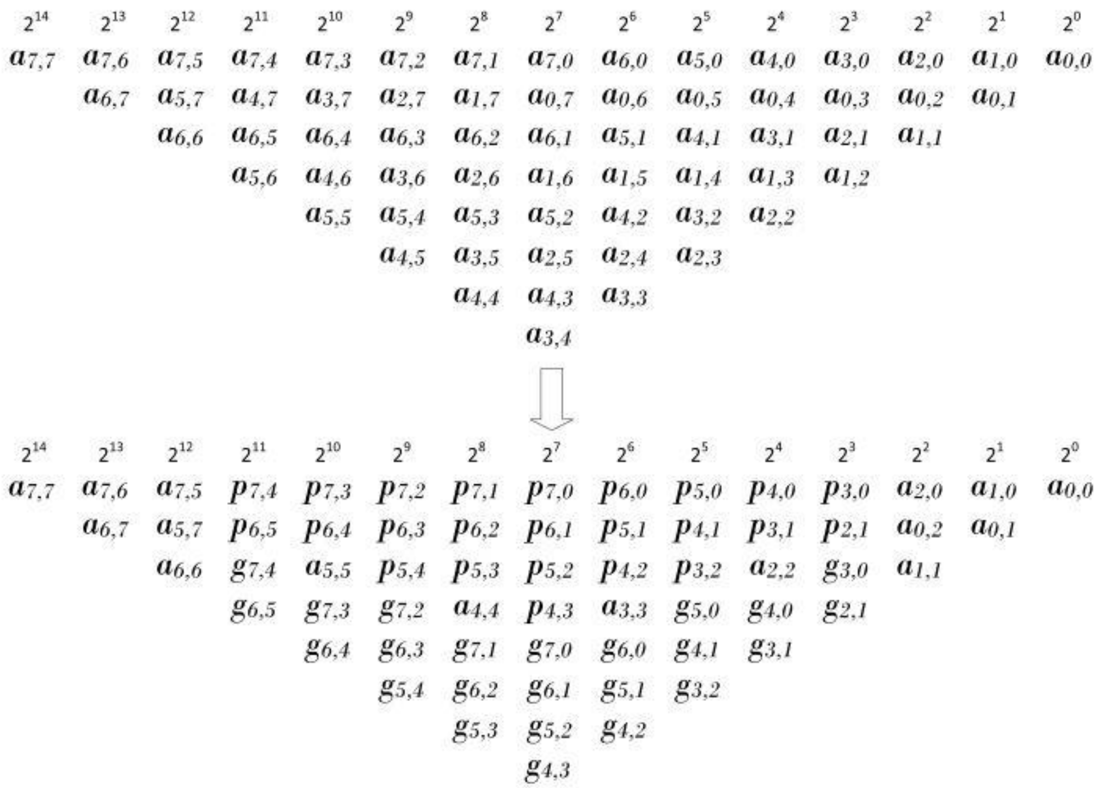


Figure 4.1 Conversion of Conventional Partial Product into Modified Partial Products

Alteration of the partial products has been done based on probability statistics to achieve less possible error. The probability of being 1 for propagated signals is 7/16, generated signals is 1/16 and normal partial product is 1/4. As whenever the output of partial product is 1, it can change the final product. This partial product alteration provides a useful approximation technique in terms of less error. Different approximation circuitry has been applied for their accumulation to reduce the error in final result.

4.2.2 Partial product accumulation [17]

This is the second stage of approximation, where approximate circuits are being used.

Three types of partial products are available after partial product alteration stage on which two types of partial product accumulation has been performed.

Based on the probability statistics, the generated signals are accumulated column wise using only simple OR gates. This is because getting a wrong value in case of generate signal is quite low than the propagate signals. Error is generated for the cases where two or more generate signals are coming as 1. Probability of this conditions is very low. A probability analysis of error generation for columns having generate signals of two, three and four elements have been calculated as 0.00390, 0.0124, and 0.02153, taking the probability of being 1 for generate signal is 1/16. But one thing that has to be kept in mind that the error would increase linearly if the number of generated signals are increased in a column. So the number of OR gates used for accumulation of generate signals is $\lceil m/4 \rceil$, where m is generate signals of a column.

For the accumulation of propagated signals and original partial products, three approximate circuits are used namely approximate half adder, approximate full adder and approximate 4-2 compressor based on accumulation of products having same binary weight. The summarized difference between these approximate circuits with their conventional counterpart is the absolute output difference of 1. To make it happen, the architecture has been modified in such way that the carry is approximated only when sum is also approximated. This is because binary weight of carry is higher and any error in it produces greater error in the output. Also XOR gates is prone to a higher area and delay in case of adder and compressor architecture.

4.2.3 Approximate half adder

Conventional half adder structure is made of one XOR gate to produce sum and one AND gate to produce carry. In case of approximated half adder structure, an OR gate has been used in place of an XOR gate. From the truth table of OR and XOR gate, it has been observed that both produces the same output when either bit is different. So this modification will cost one error in the computation of sum out of possible four cases. Carry generation will remain unchanged. The altered equations of sum and carry are shown below in Equations 4.6 and 4.7. Altercation of circuit results into modified truth table shown below in Table 4.1.

$$Sum = A1 + A2 \tag{4.6}$$

$$Carry = A1.A2 \tag{4.7}$$

Where A1 and A2 are the two inputs of the half adder.

Table 4.1 Truth Table of Approximate Half Adder

Inputs		**Exact Outputs**		**Approximate Outputs**		**Absolute Difference**
A1	**A2**	**Sum**	**Carry**	**Sum**	**Carry**	
0	0	0	0	0	0	0
0	1	1	0	1	0	0
1	0	1	0	1	0	0
1	1	0	1	1	1	1

4.2.4 Approximate full adder

Approximate full adder structure has been realized with one XOR gate along with OR gate for sum generation. By this approximation, we modify the requirement of two XOR gate with one XOR and one OR gate. Carry circuit has also been modified by using only two gates for its generation whereas conventional will take more than that. Although carry modification results in one error but the absolute error difference has been kept as 1. Modified equations of the approximation full adder has been given in Equation 4.8 and 4.9. Table 4.2 gives the modified truth table for this circuit.

$$Sum = (A1 + A2) \oplus A3 \tag{4.8}$$

$$Carry = (A1 + A2).A3 \tag{4.9}$$

Table 4.2 Truth Table of Approximate Full Adder

Inputs			**Exact Outputs**		**Approximate Outputs**		**Absolute Difference**
A1	**A2**	**A3**	**Sum**	**Carry**	**Sum**	**Carry**	
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	1
1	1	1	1	1	0	1	1

This will provide two error cases out of total eight possible cases. Although the actual errors in the approximate circuit have been observed to be equal to three, two in sum generation and one in carry generation.

4.2.5 Approximate 4-2 compressor

Approximate 4-2 compressor uses only 2 output lines instead of three as in the conventional architecture. Three output lines are only required in case of all the inputs as 1 which has very less probability to happen. This will reduce requirement of 4 XOR gates to 2 XOR and 1 OR gate to implement the summation architecture. Also to make the absolute difference as 1, one extra AND operation of all the inputs is required to be included in the sum calculation. Carry circuit has also been modified using only 3 gates, which is very less compared to the conventional one with a goal to make absolute difference as 1.

Truth table and equations of the modified approximate 4-2 compressor is given below,

$$Sum = (A1 \oplus A2) + (A3 \oplus A4) + A1.A2.A3.A4 \quad (4.10)$$

$$Carry = A1.A2 + A3.A4 \quad (4.11)$$

Table 4.3 Truth Table of Approximate 4-2 Compressor

Inputs				**Approximate Outputs**		**Absolute Difference**
A1	**A2**	**A3**	**A4**	**Sum**	**Carry**	
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	1	0	1
0	1	1	0	1	0	1
0	1	1	1	1	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	1
1	0	1	0	1	0	1
1	0	1	1	1	1	0
1	1	0	0	0	1	0
1	1	0	1	1	1	0
1	1	1	0	1	1	0
1	1	1	1	1	1	1

The approximation has resulted into total five error cases out of 16 where both sum and carry have been errored five times.

4.2.6 Summarized architecture

The summarized architecture of 8-bit approximate DADDA multiplier is shown in Figure 4.2. Although it has been seen that three stages are involved but the total multiplication process involves two more steps. First step is to produce propagate (p) and generate (g) partial product in partial product alteration step as previously discussed in 4.2.1 section. Stage 1 as shown in the Figure 4.2 are depicting the use of approximate circuits like approximate full adder, approximate half adder, approximate 4-2 compressor, OR gate usage in order to partial product reduction. Stage 2 in the same Figure deals with the second level partial product reduction using approximation half and full adder to the outputs of stage 1 where G_i denotes the outputs of OR operation and S_i and C_i being output of the approximate circuits corresponds to column i with weight 2^i and i can be any value between 0 to 14.

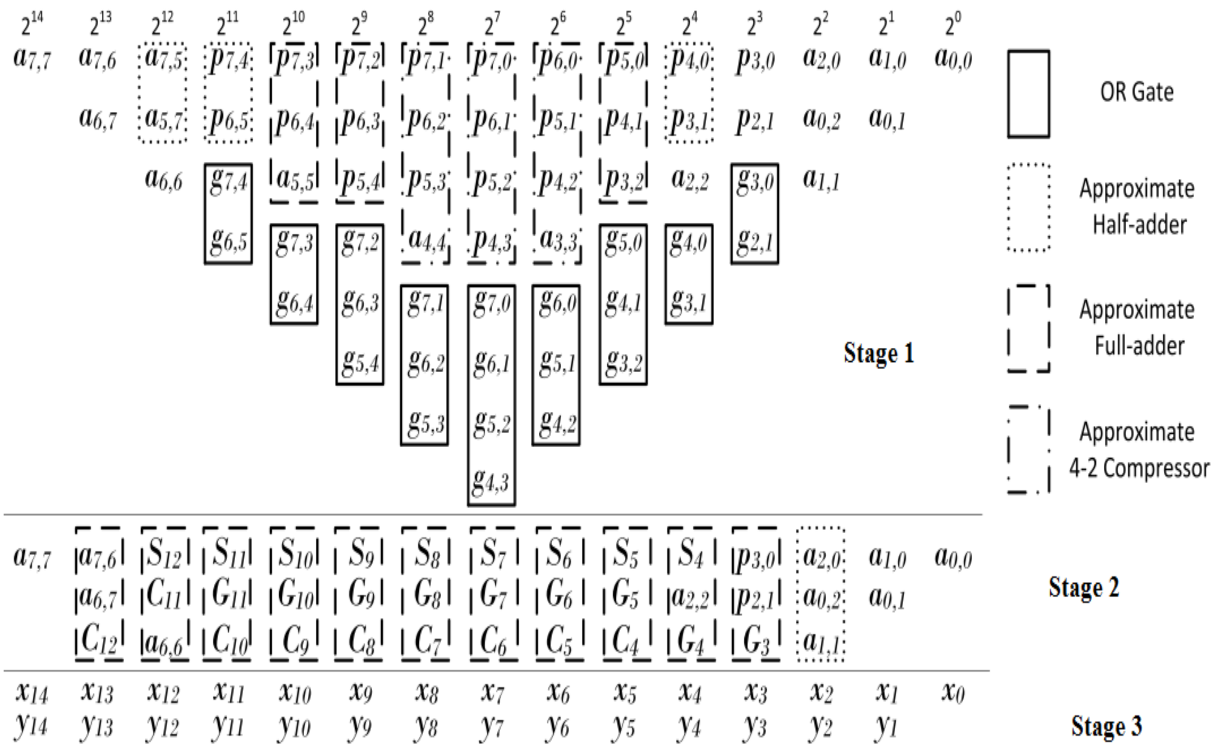


Figure 4.2 Summarized Approximate Multiplier Architecture

Whereas stage 3 shows the inputs to the final stage adder as final operands x_i and y_i. For the final product as result, outputs of stage 3 is fed to multi bit supporting adder which is the final stage not shown in the above Figure. For this addition operation we opted ripple carry adder, carry select adder and one modified version of carry select adder has been considered to achieve the goal of low power, high speed and less area.

The requirements of approximate circuits to implement the approximate multiplier architecture specified in stage 1 to 3 for an 8 bit approximate DADDA multiplier are 9 OR gate, 3 approximate 4-2 compressor, 14 approximate full adder, 4 approximate half adder. By comparing with the conventional DADDA architecture with this approach, it has been observed that it required only 3 stages of partial product reduction and accumulation to get the final product where conventional one required 5 stages of operation.

4.2.7 Last stage multi-bit adder modifications

After stage 3, two rows of data has been available. These data has to be added to get the final sum. For this stage normal adder structure has been used. Full adders can be used to add three one bit binary numbers. Logical circuit using multiple full adders to add N-bit binary numbers has been used to design multi-bit adder. In 8-bit approximate multiplier design 16-bit adder circuit has been used. Three such adders are discussed below

4.2.7.1 Ripple carry adder

Ripple carry adder (RCA) is a simple structure of full adders where carry is rippling from one adder to the next adder. In a ripple carry adder the sum and carry out bits of any full adder stage is not valid until the carry in of that stage occurs.

As the delay of ripple carry adder is increased in a linear fashion as the bit length is increased, this adder results into a higher delay contributing architecture. Architecture used for a 4-bit ripple carry adder in the approximate multiplier shown below in Figure 4.3. 4-bit RCA has been constructed using four full adders where the third input carry is propagated from the previous stage full adder output. To have 16-bit adder structure 16 full adder structures has been needed.

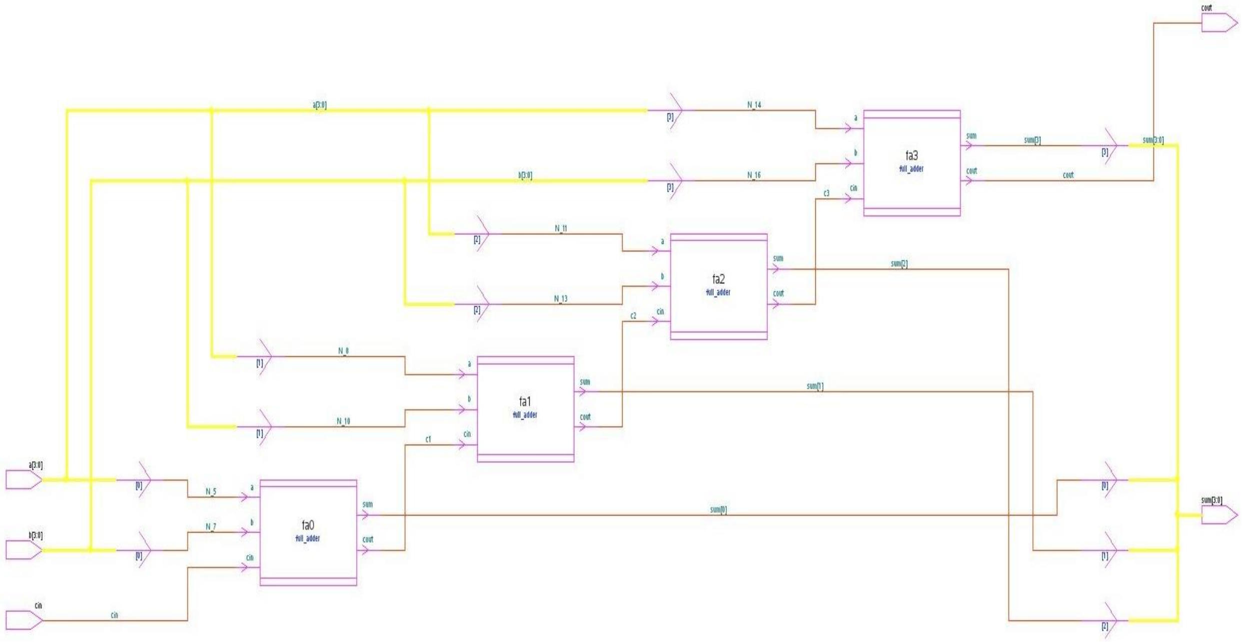


Figure 4.3 4-bit Ripple Carry Adder

4.2.7.2 Carry select adder [18]

Carry select adder (CSA) is next evolution of the ripple carry adder. It alleviates the problem of carry propagation delay by independently generating the multiple carries and then select a carry to generate the sum. This adder operates on a principle that there are only two possibilities, either carry would be 0 or 1.

So, instead of waiting for carry propagation these adder uses parallel structure of two ripple carry adders. Both of these ripple carry adder output is given to a 2:1 mux whose select line is the carry from the previous stage. By this approach, the delay is drastically reduced as each full adder stage does not wait for the previous stage completion. This approach is not an area efficient because it uses multiple pairs of RCA.

The architecture of a 4-bit CSA is given below Figure 4.4. 16-bit CSA adder will be combination of this type of structures. As we can see in the Figure 4.4, 4-bit CSA adder is constructed using two 4-bit RCA adders with two set of multiplexer structures, one for the sum and other one for the carry. Select lines of these multiplexers are carry output of previous stages.

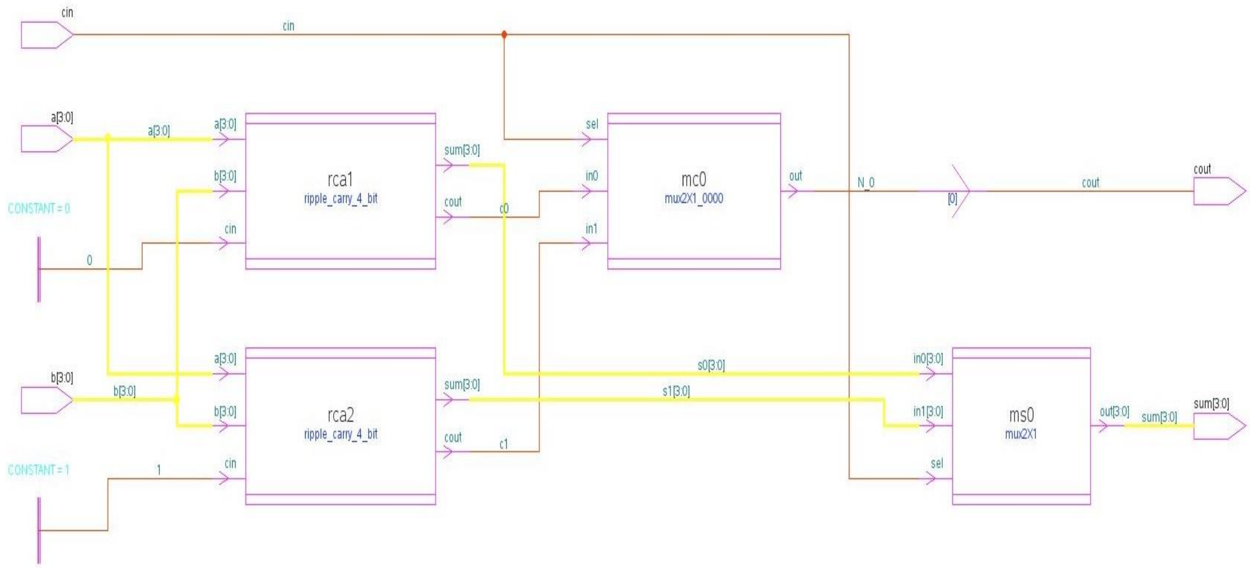


Figure 4.4 4-bit Carry Select Adder Architecture

Also the architecture used in approximate multiplier circuit is square root carry select adder structure which uses variable sized ripple carry blocks. This type of implementation results into less delay due to critical path reduction.

16-bit CSA adder structure used is shown below in Figure 4.5.

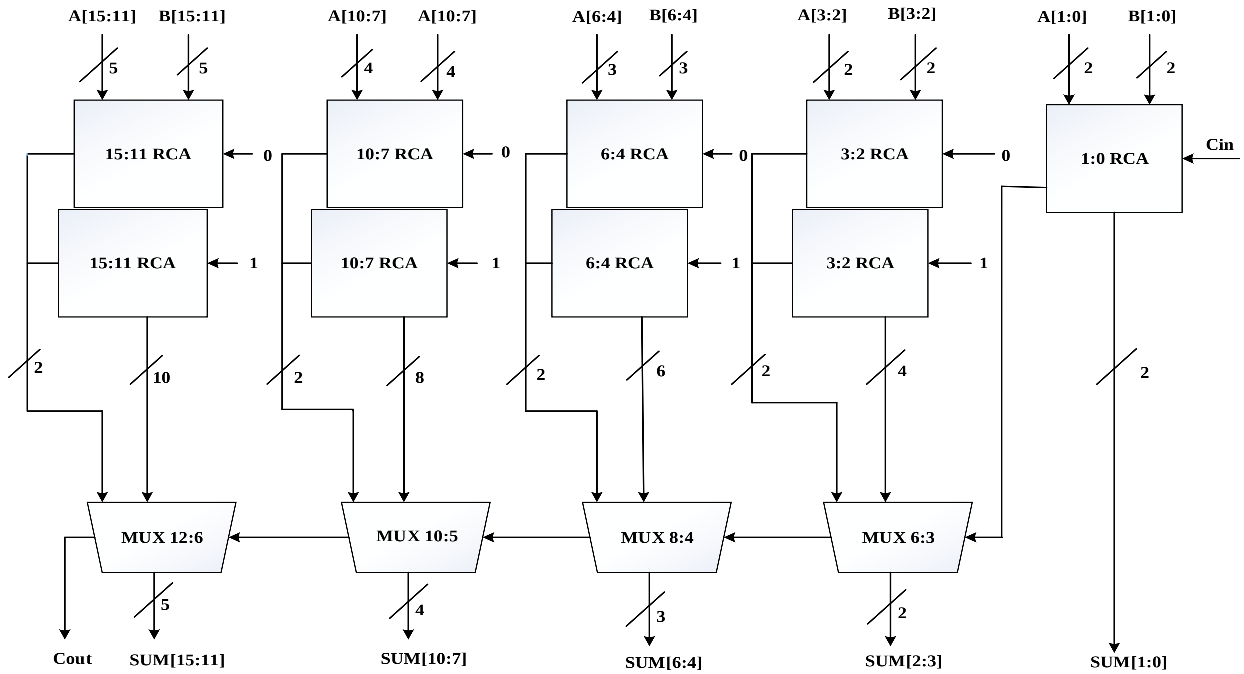


Figure 4.5 16-bit CSA Adder

Each data line bit width is shown in the above Figure 4.5. The incremental or variable size structure is implemented to support less delay structure. Sizes of multiplexer are depends upon the inputs fed to them.

4.2.7.3 Carry select adder using binary to excess 1 converter [18]

Disadvantage of high area and power of carry select adder can be reduced by using binary to excess 1 converter (BEC) architecture. In CSA, both the RCA architecture will do the same operation using different carry values. Binary to excess 1 converter basically converts binary bits by adding 1 to them which is equivalent of RCA using carry signal as 1 in case of CSA. In modified CSA, the ripple carry structure associated with carry value taken as 1 been replaced with binary to excess 1 converter. This architecture requires less number of gates, so it will serve the goal of low power and area reduction. The binary to excess converter should be of 1 bit higher than the ripple carry adder to provide same functionality as conventional CSA. The equations derived for a 4-bit binary to excess 1 converter are shown in equations 4.12 to 4.15, where B0, B1,B2,B3 being binary bits and X0,X1,X2,X3 are converted bits are given below.

$$X0 = \sim B0 \tag{4.12}$$

$$X1 = B0 \oplus B1 \tag{4.13}$$

$$X2 = B2 \oplus (B0.B1) \tag{4.14}$$

$$X3 = B3 \oplus (B0.B1.B2) \tag{4.15}$$

In this equations X0 and B0 denotes least significant bit whereas X3 and B3 denotes most significant bit of a 4-bit number.

It’s pretty evident that number cells required by BEC is very low than an RCA structure of same bit length. Architecture of carry select adder with binary to excess 1 converter for 4-bit operation is shown below in Figure 4.6. For 4-bit adding operation, 4-bit RCA and 5-bit BEC structure has been used. The output has been taken for the multiplexer to which input is output of RCA and BEC structure. The select line in multiplexers has become the carry output of previous stage.

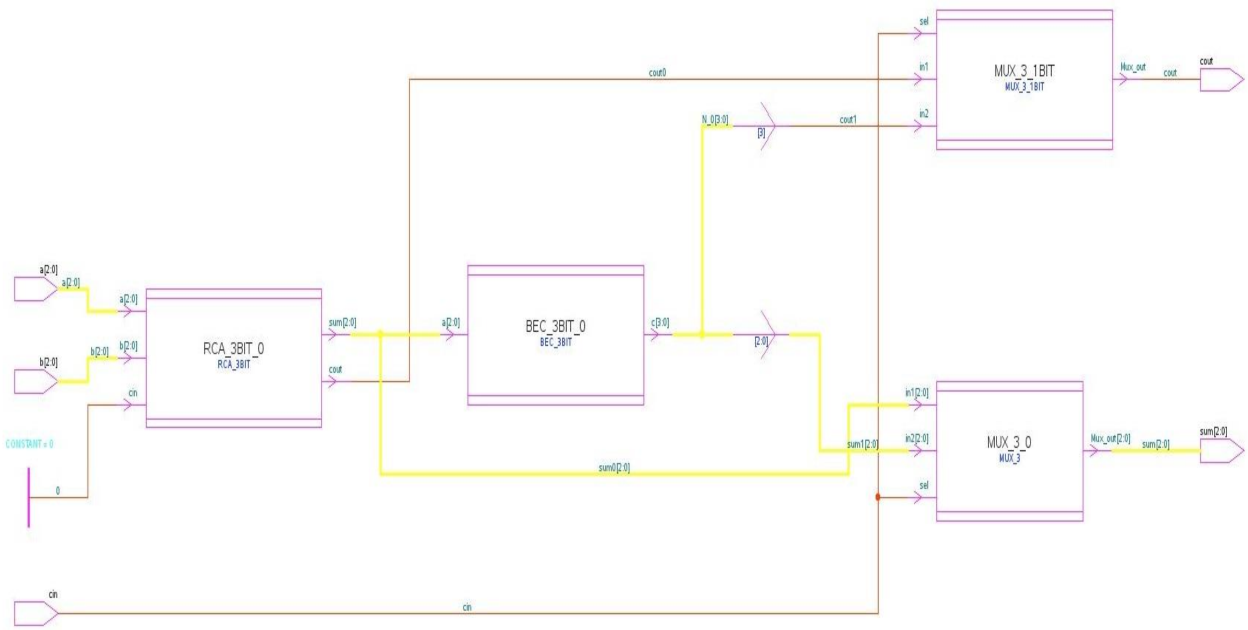


Figure 4.6 4-bit Carry Select Adder with Binary to Excess 1 Converter Architecture

16-bit CSA with BEC architecture is shown in Figure 4.7. Due to variable sized CSA structure, BEC structures are also variable sized. For 16-bit structure maximum of 5-bit RCA and 6-bit BEC structure has been used,

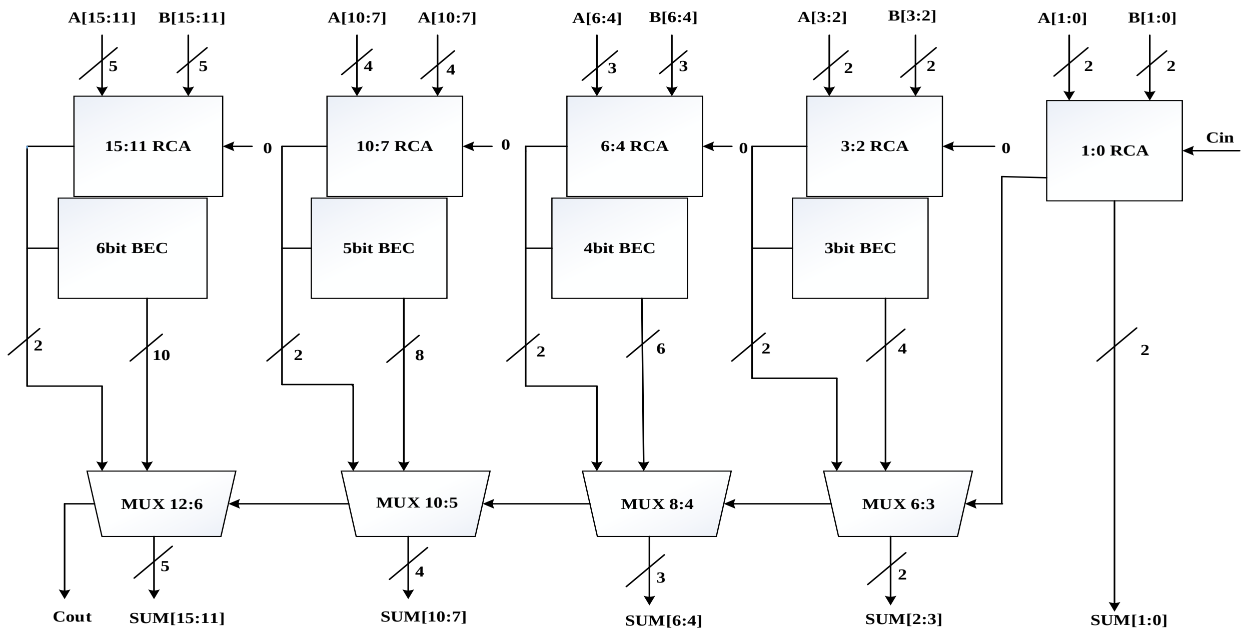


Figure 4.7 16-bit CSA with BEC Architecture

4.3 PERFORMANCE IMPROVEMENT TECHNIQUES

Performance of a design is measured in terms of its power consumption, area required and speed of operation apart from functionality. In most of the cases improvement of any one or two parameter out of these three parameter results of degrading other parameters. Approximate multiplier design primarily concerned with improvement of power and speed of operation. There are many techniques present to achieve these but only a few is implemented in the design to get optimum results.

4.3.1 Algorithmic level change

This type of changes deals with the optimum coding styles. In synthesis, the cells or components generated depends upon the coding style. Power, delay & area are directly related with number of cells that are used in the design. At the algorithmic level, we use resource sharing to minimize the cell requirements to implement same logic.

Also efficient level of coding uses operator reduction to improve the performance parameters.

4.3.2 Multi Vdd design

It's a very efficient technique to reduce power consumption. The main idea is to divide the circuit into different power domains which will operate at different voltages. Voltage selection basically depends on the frequency of operation of that part of the circuit. Higher operating frequency region will need a higher voltage and vice versa. To implement this technique, some extra cells are required which will be provided by the UPF specifications.

A multi Vdd structure must comply with the timing analysis. The delay of a circuit is inversely related to voltage where power is proportionally related to voltage. For efficient design, the elements in the critical path should be operated at higher voltage to have high speed operation by keeping a check on power.

4.3.3 Multi Vt design

In Deep Sub-micron process, power dissipation due to leakage current becomes very much significant in the total power dissipation count. With different types of leakage power optimizing techniques available, multi Vt technique has been used to reduce the leakage power. Also as threshold voltage is also affecting the speed performance of a circuit, it’s possible to optimize a design over speed and leakage power by mapping non-critical paths and critical paths in the design with cells having different threshold voltages quite early in the design flow.

There are three type of Vt cells are present in technology libraries namely standard, low and high Vt. High Vt cells are preferred for low leakage power achievement but have a drawback of high delay. In order to meet the timing constraints and low power, using the combination of low and high Vt cells is recommended. Basically any cells other than critical path will use high Vt cells. These optimization is basically done during the synthesis.

4.3.4 Power gating

Power gating is the circuit design technique that has been most widely used in the industry. Power gating is conceptually very simple: a circuit is cut off from its power supply in sleep mode by means of a current switch to remove completely dynamic and static power during this period. This power gating is again supported by UPF.

It has although two main disadvange. Firstly additional circuits i.e. isolation, power switch, retention cells required to suitably implement power gating architecture. And secondly timing penalty for entering and exiting power gating mode. Also problem of ground bound and rush currents during switching on operation is point of concern.

An overview of power gating implementation is shown below in Figure 4.8.

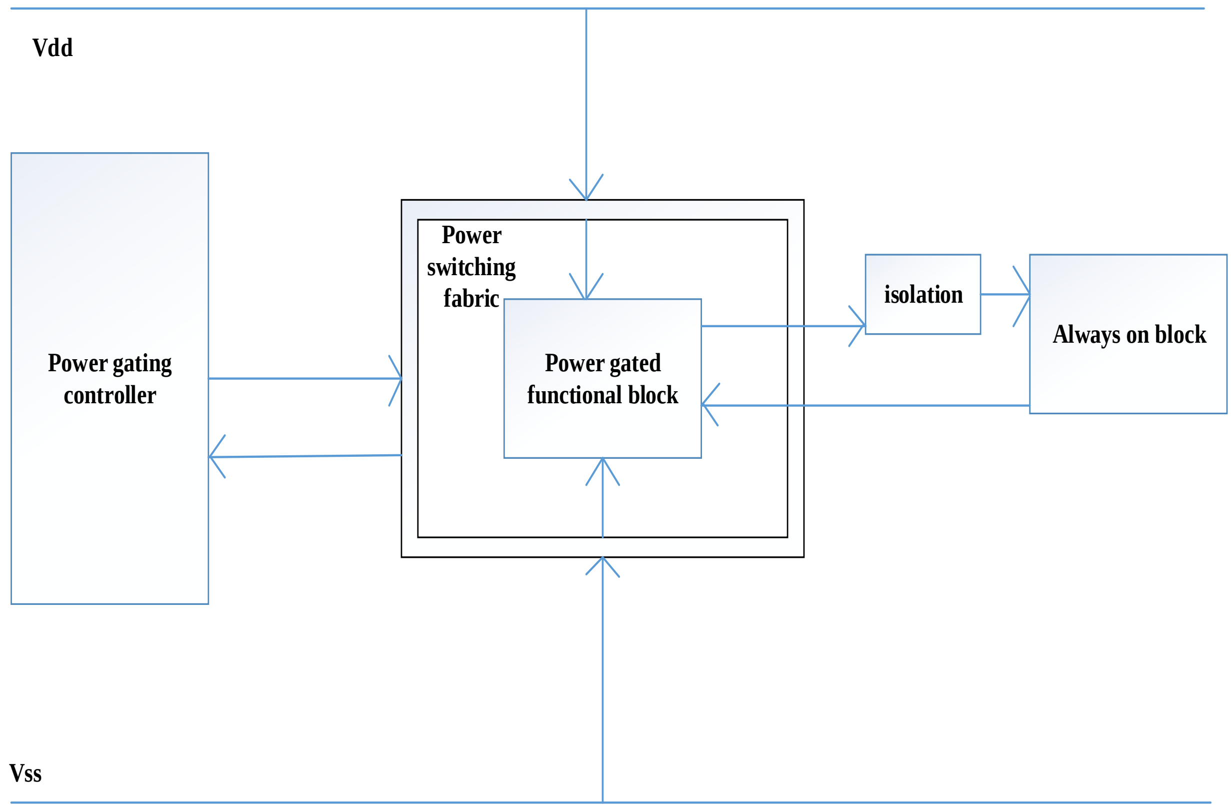


Figure 4.8 Typical Power Gating Strategy

4.4 ERROR METRIC

Introducing approximation in the calculation, main output is erroneous as in many cases the output is differed from the exact cases. In terms of power reduction or efficient operation, we cannot change the functionality of the main design. To check the quality of output and to make sure the functionality of the design is intact, it is essential to define some metrics which will provide insight of deviation in the functionality. In this context it can be said that the error rate is basically probability of having an erroneous output.

To define this metrics the accurate product result as $\boldsymbol{P}$ and approximate product result as $\boldsymbol{P'}$ has been taken.

4.4.1 Error Distance (ED)

Absolute difference between exact and approximate product result for same input.

$$ED = |P - P'| \tag{4.16}$$

This metric will differ as per the inputs are differ in real cases.

4.4.2 Mean Error Distance (MED)

Average value of all ED for all possible cases.

$$MED = \frac{\sum_i ED}{i} \tag{4.17}$$

where i is number of input cases considered.

4.4.3 Normalized Mean Error Distance (NMED)

Normalization of MED with the maximum possible error value possible in the design.

$$NMED = \frac{MED}{P_{MAX}} \tag{4.18}$$

Where $P_{MAX} = (2^N - 1)^2$ for N bit multiplier.

4.4.4 Relative Error Distance (RED)

Checks the relative difference of the error with respect to the accurate result for each input.

$$RED = \frac{ED}{P} \tag{4.20}$$

4.4.5 Mean Relative Error Distance (MRED)

Mean value of RED for all possible cases.

$$MED = \frac{\sum_i RED}{i} \tag{4.21}$$

All these metrics are always input specific. Depending upon the input samples these values are varied. But variation of these metrics are very low in terms of change in input sample space.

4.5 POWER INTENT VERIFICATION

Power intent verification is basically pipe-cleaning the power intent of the design specified in UPF format. Basically multi-voltage, static low power checker is applied to verify the design capable of voltage control methods for power management. Verification at each stage of design flow is essential to proceed the design with a clean UPF.

4.5.1 Features

Features of power intent verification process are basically involves certain checklist that needs to be complete to ensure the proper UPF flow throughout the design to achieve low power goal. These checks are as follows,

- Power intent consistency checks.

Power intent consistency checks deals with syntax and semantics before implementation of UPF is started with design.

- Signal corruption checks.

  Signal corruption checks deals with violation of power architecture at gate level netlist due to wrong implementations.
- Structural checks.

  Structural checks deals with insertion and connection of UPF elements such as isolation cells, retention cells, power switches, level shifters in design flow throughout.
- Power and ground (PG) consistency checks

  PG checks UPF consistency for routed power network in physical netlist.
- Functional checks.

  Functional checks the functionality of power switches and isolation cells.

At each stage of design flow it is essential to check for power intent specifications are carry forwarded or not. Early design cycle checks helps to debug power intent based design issues for efficient and fast way. Each stage of design flow contains more than one checks that needs to be performed for proper validation of UPF with the design.

4.5.2 Collateral

Prerequisite for running this power verification checks are,

- Netlist
- UPF
- Libraries

4.5.3 Methodology

Power intent verification flow at different stages of design is given below Figure 4.9.

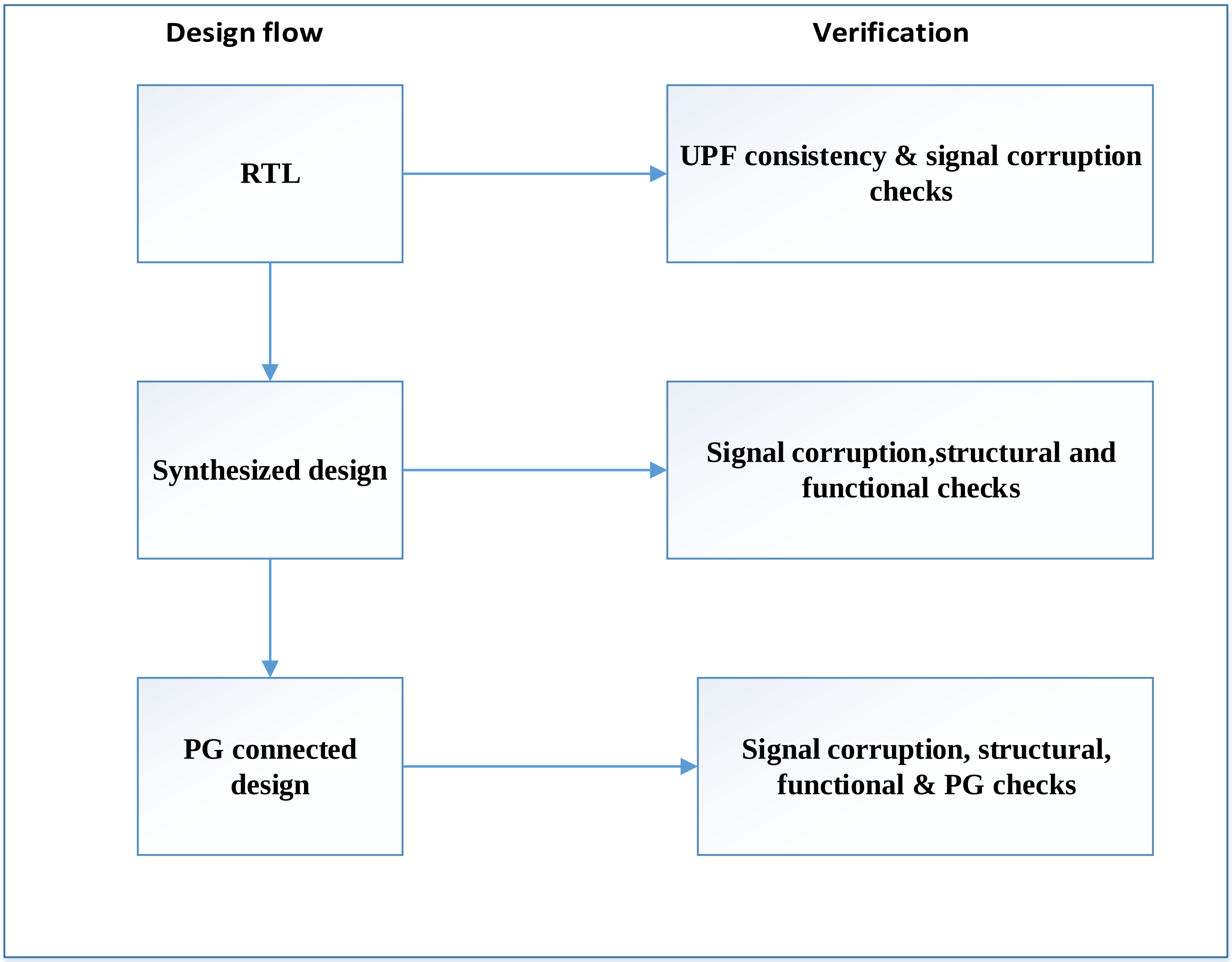


Figure 4.9 Power Intent Verification Flow

At RTL level verification deals the completion of the semantically corrected UPF. Also it will check for design compatibility with isolation and level shifter strategies for all power modes available.

At netlist level verification mainly deals with functionality and structural checks as there are possibility of cases where structurally corrected design is functionally incorrect. Also inserted cells consistency with the UPF and library is also needed.

PG connected design checks are mainly deals with verification of power/ground pin connection in post layout design consistent with UPF.

4.6 SIP DESIGN

To design a power aware system, a SIP structure has been considered.This was needed as approximate multiplier can only support multi Vdd structure. Implementation of multi Vdd requires some extra cells which consumes more power. So variation of power and usefulness of UPF cannot be shown. An overview of the SIP architecture has been shown in Figure 4.10.

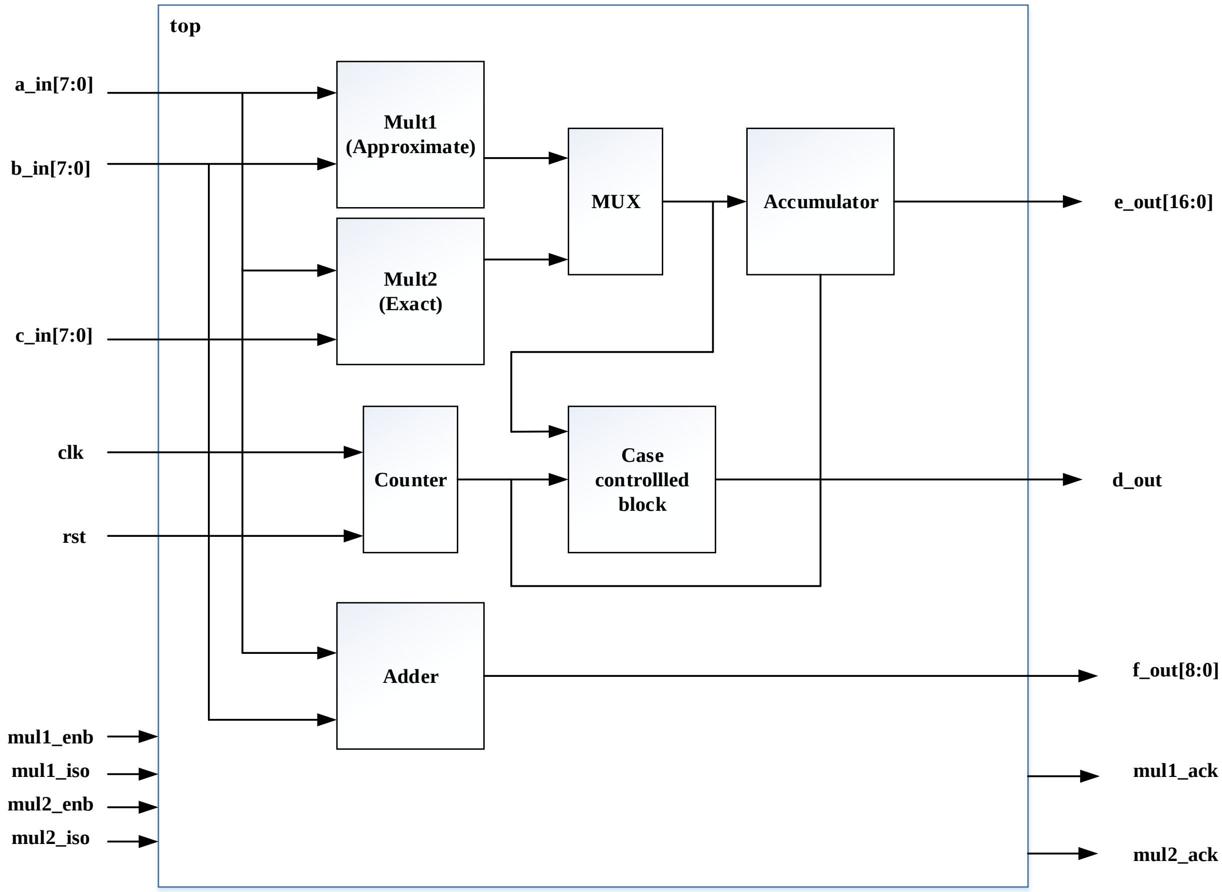


Figure 4.10 Architecture of SIP

The SIP structure contains both approximate structure and exact multiplier structure with 8-bit inputs a_in, b_in and c_in. The outputs of these two multipliers are fed to a multiplexer which is controlled by another input signal as select line. An adder is implemented for the addition of two input data lines. One counter is implemented with clock and reset signal controlling the case statement controlled architecture. This architecture will populate d_out from multiplexer output depending upon counter output. Another output e_out is coming from accumulation of output of selected multiplier and counter output. Two enable and two isolation inputs have been provided. These are signals required by the UPF elements.

Power intent of the SIP are as follows,

- All the design elements excluding Mult1 i.e. approximate multiplier is said to operate at voltage of 0.85V whereas Mult1 operated at 1.05V.
- Both multipliers are switchable.

The functionality or output of this SIP is not required as this design is only used for design implementation and automated framework generation.

4.7 POWER ROLLUP

For any design it contains different elements but primarily SIP and Hard Intellectual Property (HIP), core, graphics etc. HIPs are already characterized for power, SIPs has to go through different design phase to estimate their power contribution. The approximate multiplier we designed is made a part of a SIP and try to modify the existing power rollup approach to ease the design understanding.

After each stage of design or implementation, power estimation is done e.g. RTL power estimation, Gate level power estimation etc. This generated reports are in spreadsheet format along with some tool generated valuable reports.

4.7.1 Methodology

Already in industrial level a lot of work done on the roll up. Designed rollup along with validation check approach has been worked after the tool generate existing flow based power and other reports. This rollup mechanism take all the necessary reports from the report area, extract the needful information and put it in a single compact report format. This report will then goes to the next level of design to provide the summarized version of design.

The flow of power rollup generation is given below Figure 4.11.

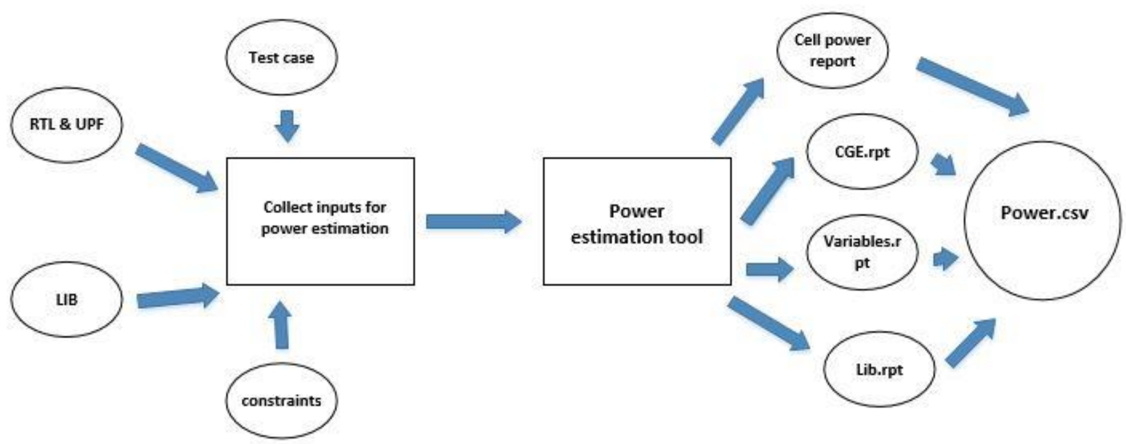


Figure 4.11 Power Rollup Generation Mechanism

The rollup mechanism act as a add on feature to the existing approach which will not hog the design flow from tool standpoint as it will not invoke the tool for its operation.

This rollup approach has been included one extra feature of validation of power numbers. This approach basically deals with certain cells in design where power numbers are not present in the library or specified as zero or NA which results into wrong power estimation. This cells needs to report back to design team to either not used in the design or design with proper power characterization. This validation process flow is mention in the below Figure 4.12.

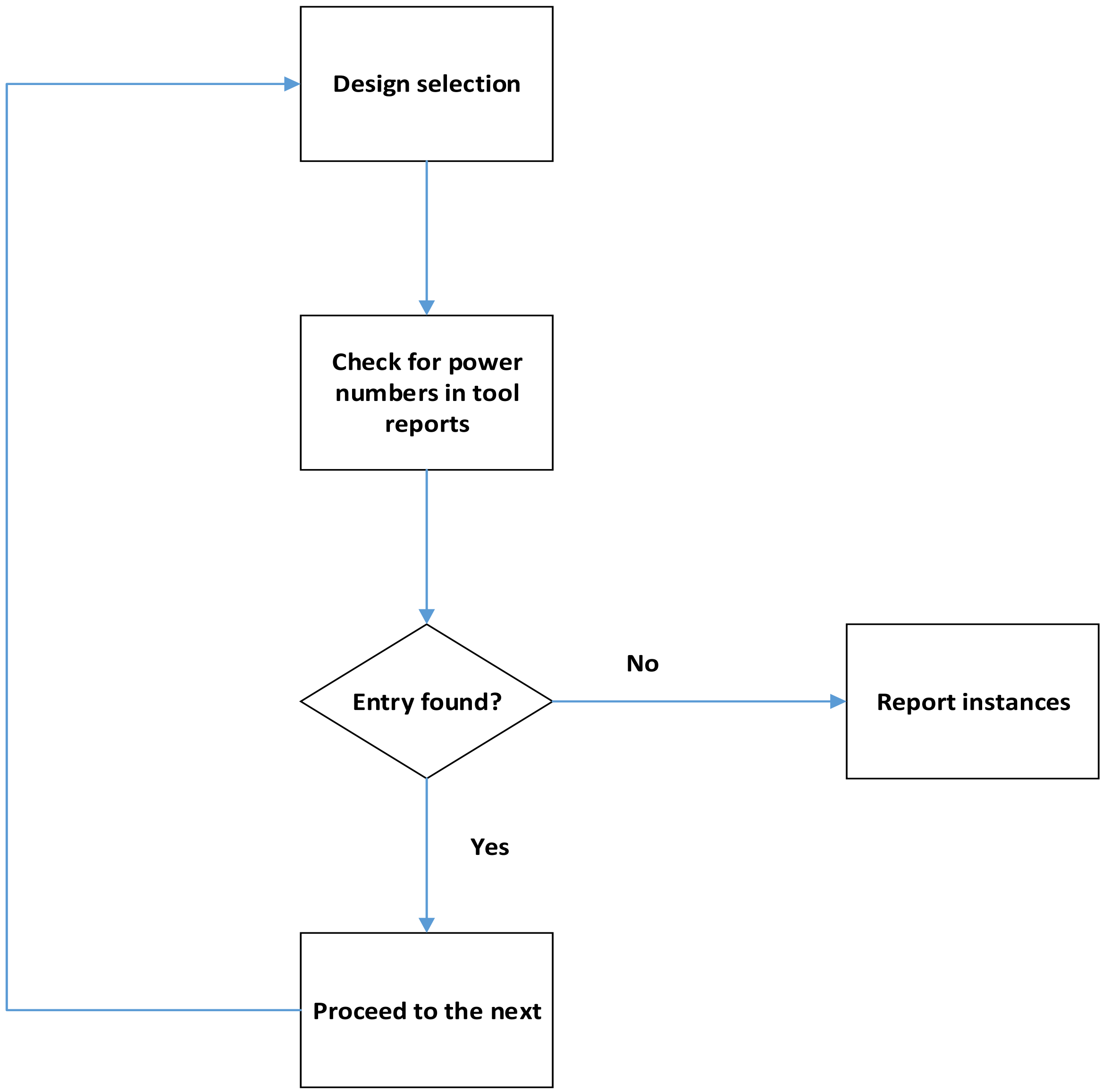


Figure 4.12 Validation Algorithm

4.8 POWER INDICATOR SYSTEM

This indicator system is basically use dashboard publishing platform to publish the evaluated data.

This publishing platform works as a front-end framework which felicitates horizontal capabilities of feasible dashboards with tables, charts, Key Performance Indices (KPI) and many other analysis features. For functionality of publishing platform requirements are following:

- Microsoft Excel.
- SQL database.
- Power Pivot Publisher to publishing platform installation.
- Permissions.

Microsoft's Excel being industry standard tool for data processing, inbuilt feature of this tool known as PowerPivot with the help of data analysis expressions (DAX) can process and filter large data very easily.

4.8.1 Power pivot publisher

PowerPivot Publisher comes with some predefined options as shown in the Figure 4.13. This is the connecting interface to publish data onto dashboard.

Figure 4.13 PowerPivot Publisher

Publish is used to publish or republish data onto dashboard. Dashboard properties are useful to set the alignment of columns in a table. To directly navigate through the indicator dashboard page open in browser is used. Links used to enable the drill down feature. Dashboard properties are also being set from here only. One of the best feature of this publisher is auto data refresh feature. By setting as per our convenient time data are picked from SQL server and auto update in dashboard.

4.8.2 Working features

Each tool after completion of their implementation, optimization and analysis dump reports in comma separated value (CSV) format by use of PERL, TCL and python scripts. This CSV files are easily uploaded to the SQL database using the following command,

mysqlimport --host=<hostname> --user=<username> --password=<password> -ignore-lines=1 --fields-terminated-by=, --verbose --local <database name> <csv file name>

Then this data can be easily imported to excel using PowerPivot and process accordingly.

Basic traits of power indicator system are,

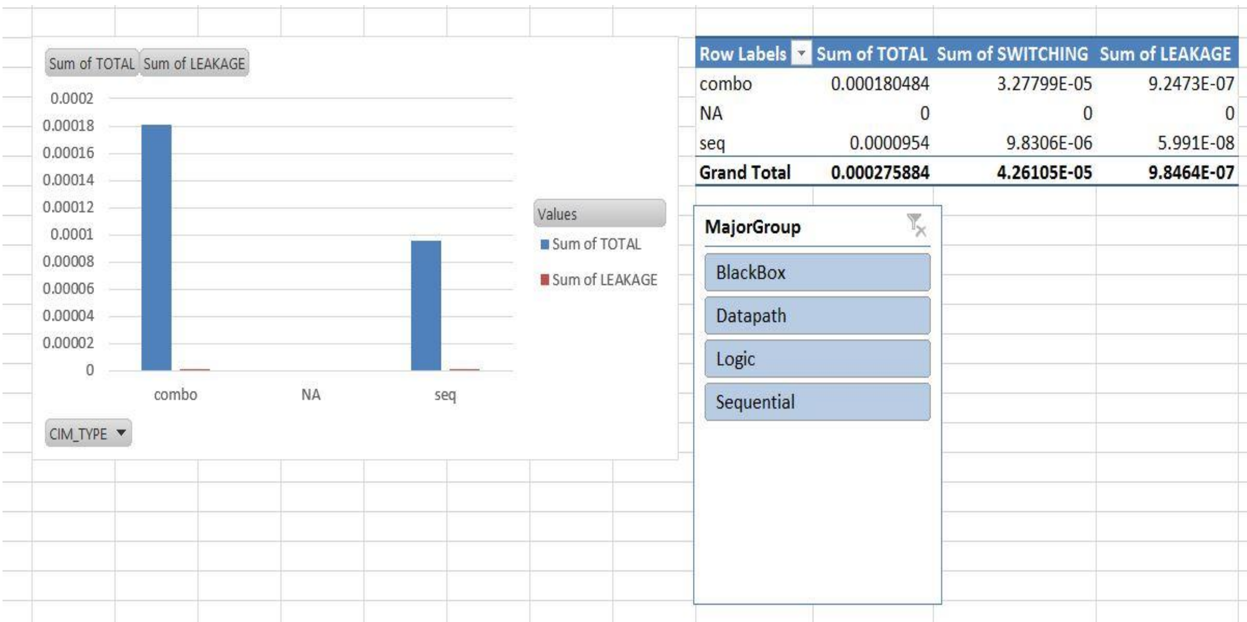
- The worksheets published from PowerPivot to publishing platform are in form of dashboards. This dashboards are republish able and also can be shared by email link.
- Single or multi select slicer and filter availability in dashboard
- Pivot table and chart to depict the trend of process data. Large, flattened tables are supported in dashboard.

Pivot chart and table creation is an excellent feature provide by PowerPivot. It's very easy to process the data seen by charts and tables also understand the power trend. To create a chart and table in PowerPivot menu we have to add pivot chart and table. Then in excel we have to add x and y axis for chart, and for tables we have to add rows and values.

There is also drill down option is available in the PowerPivot is to steer through different target dashboard from a source dashboard. This option is used to connect different indicator dashboard. In power trend analysis the source dashboard act as a top envelope contains the overview level information where target dashboards contains detailed information. It is possible to bind filters in the connecting dashboard as well as to delete a filter in the target dashboard.

4.8.3 Slicer

The unique feature of slicer enables easy understanding in dashboard. Using slicer feature with charts and tables can enable selective values to show. These feature is very useful to analyze and debug the power trend of the design. An implementation of chart, table and slicer feature is shown in Figure 4.14 and 4.15.



Row Labels	Sum of TOTAL	Sum of SWITCHING	Sum of LEAKAGE
combo	0.000180484	3.27799E-05	9.2473E-07
NA	0	0	0
seq	0.0000954	9.8306E-06	5.991E-08
Grand Total	**0.000275884**	**4.26105E-05**	**9.8464E-07**

Figure 4.14 Pivot Chart and Table with All Options in Slicer is Selected

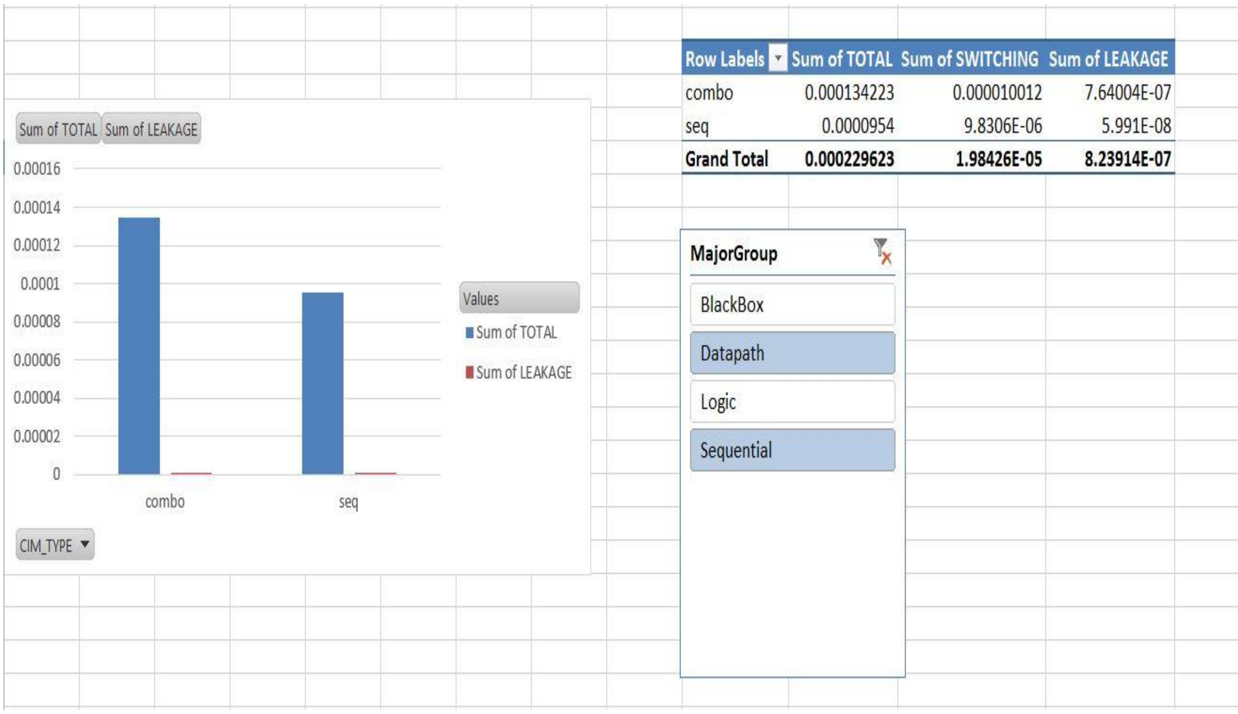


Figure 4.15 Pivot Chart and Table with Only Data Path and Sequential is Selected in Slicer

4.9 IMAGE PROCESSING

Approximate multiplier has been used in the Gaussian filter for image processing. In Gaussian filter filtering is done by convolution of original image with the defined Gaussian mask. The convolution process involves multiplication. For this multiplication process approximate multiplier has been used. The quality of the processed image is evaluated in terms of Peak Signal to Noise Ratio (PSNR) value. Computation of PSNR value is following the below equation,

$$PSNR = 20\log_{10}\frac{R}{MSE} \tag{4.22}$$

$$MSE = \frac{1}{MN}\sum_{i=0}^{M-1}\sum_{j=0}^{N-1}(I_1(i,j) - I_2(i,j))^2 \tag{4.23}$$

Where R is maximum fluctuation possible in input image data.

MSE is mean square error which represents the cumulative squared error in between original (I_1) and filtered image (I_2).

M, N are the number of rows and columns in the images and i, j are the pixels of image.

Operation of Gaussian filter using approximate multiplier for image filtering cum smoothening is shown in Figure 4.16.

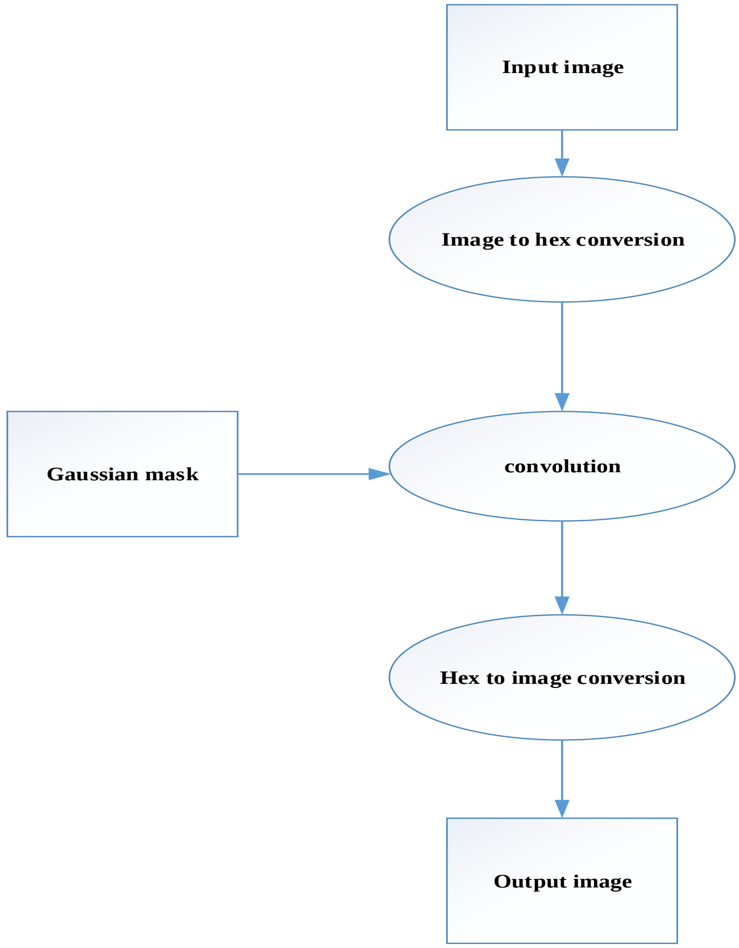


Figure 4.16 Image Processing Flow Using Gaussian Filter

The image to hex and hex to image conversion is MATLAB controlled process to convert image data to hexadecimal values. Also PSNR calculation is inbuilt to this coding. Convolution is a common image processing operation that filters an image by calculating the sum of products between the input image and a smaller image like Gaussian mask. Multiplying the values of input image pixels with the pixels covered by the mask and then summing the results provide the value of the particular pixel in the output image. The multiplication has been done using approximate multipliers. The whole process, apart from image conversion processes has been designed in Verilog Hardware Description Language (HDL).

CHAPTER 5

RESULTS AND DISCUSSION

5.1 OVERVIEW

This chapter deals with all the analysis of an 8-bit approximate DADDA multiplier. The results have been illustrated for all the different architectures that have been adopted to improve performance. The implementation of power aware SIP design using approximate multiplier has been verified and analyzed. Also, automotive power roll up and power indicator system results have been shown.

Synthesized design of partial product generation and accumulation has shown below in Figure 5.1. Only this part of design remain unaltered in approximation design and analysis.

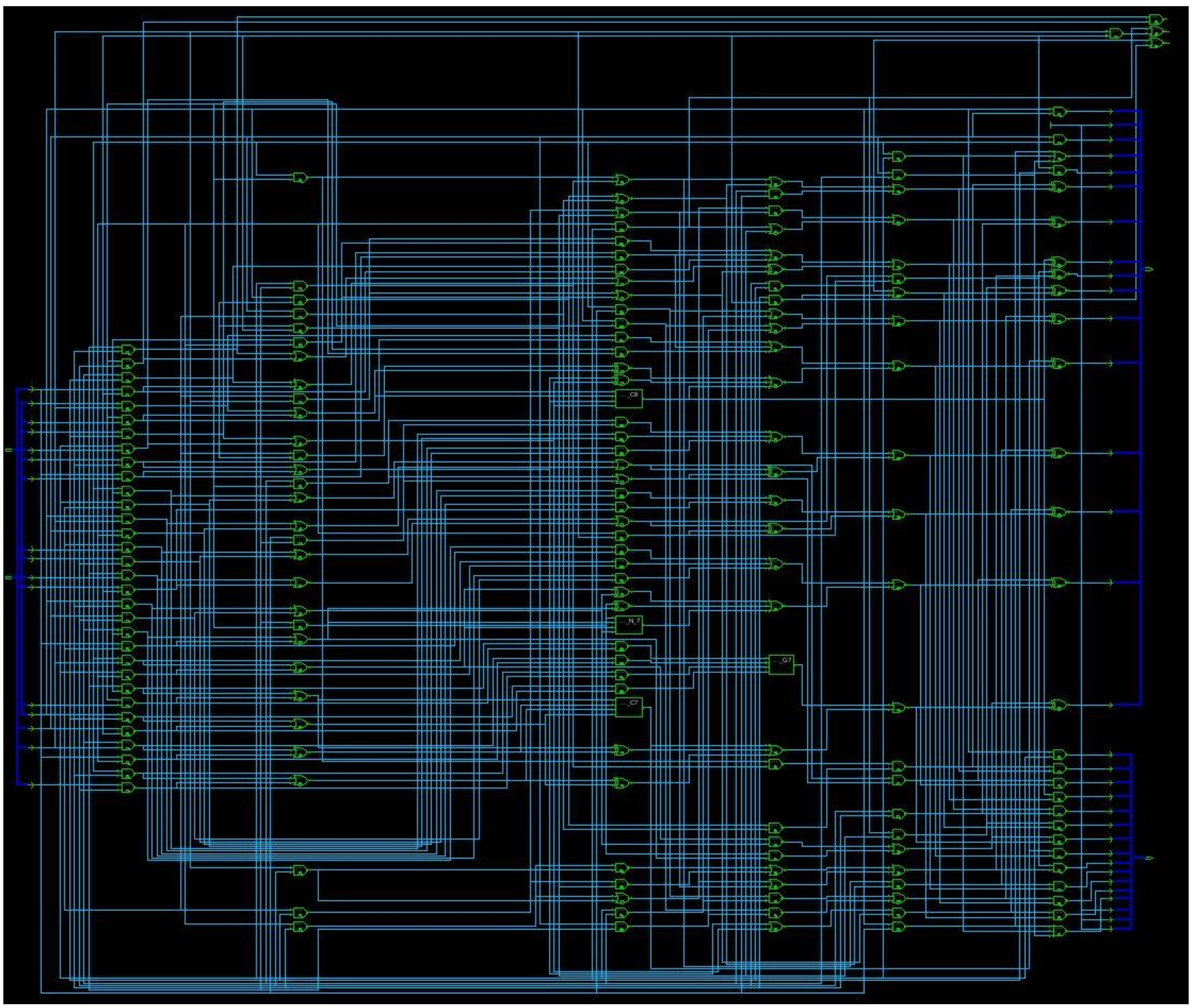


Figure 5.1 Synthesized Partial Product Generation and Accumulation Circuit

5.2 APPROXIMATE MULTIPLIER SIMULATION

After implementing the approximate design as discussed in previous Chapter 4 in Verilog HDL, the simulated result has been shown in Figure 5.2. We can see that in the simulation waveform both exact and approximate results have been shown. We can find that there are some cases where the exact output is different from the approximate output because of approximation applied in the design.

For example, as shown in the Figure 4.2, when both inputs of the multiplier is 63(3f in hexadecimal), 34(22 in hexadecimal), the exact output is 2142(085e in hexadecimal) where approximate output is 2046(07fe in hexadecimal). HDL verification and simulation is very essential to meet the functional requirement.

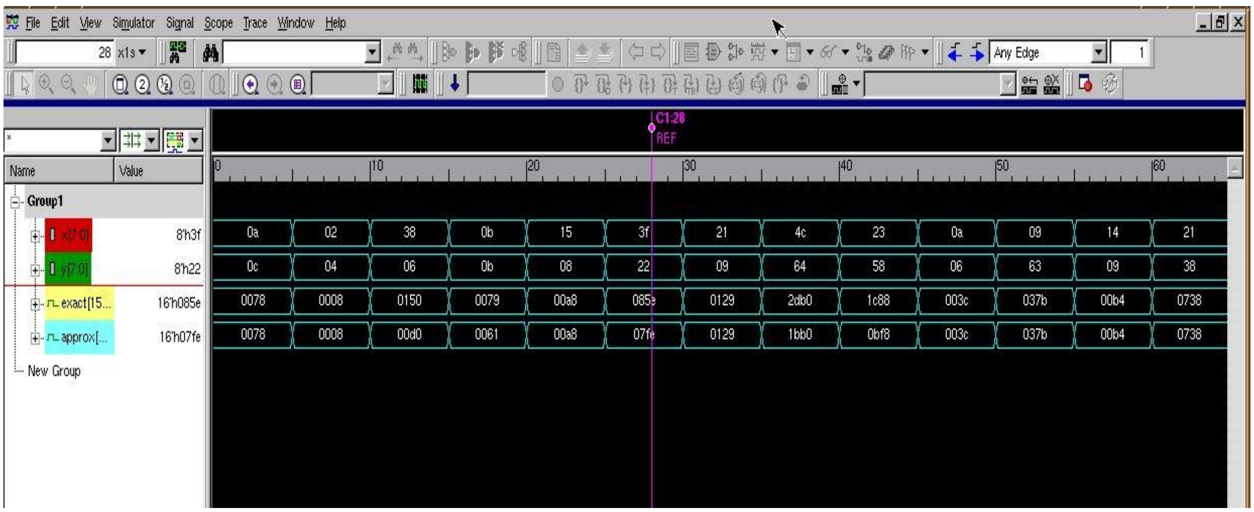


Figure 5.2 Simulated Waveform Contains both Exact and Approximate Outputs

5.3 PERFORMANCE PARAMETER ANALYSIS

As per the improvement techniques discussed in Chapter 3, the architecture has gone through the stage of synthesis to define design performance parameter. The performance parameters of any design are power, area and speed. The summarized performance of these designs are given in Table 5.1 and 5.2. Synthesis is done using standard cell library at typical process corner with supply voltage of 1.05 Volt and with temperature 25ºC.

Table 5.1 Area and Delay Analysis of Exact and Approximate Multipliers

Design	**Area (μm^2)**	**Delay (ps)**
Exact multiplier	98.3718	703.49
APM_RCA	66.2709	631.79
APM_CSA	92.5344	469.2
APM_CSA_BEC	79.1856	461.19

Table 5.2 Power Analysis of Exact and Approximate Multipliers

Design	**Internal power (mW)**	**Leakage power (nW)**	**Switching power (mW)**	**Total power (mW)**
Exact multiplier	0.4689	14.9344	0.3847	0.8536
APM_RCA	0.1685	10.7513	0.1677	0.3362
APM_CSA	0.2646	15.5128	0.2467	0.5113
APM_CSA_BEC	0.2055	11.1857	0.2306	0.4361

As seen from the above analyzed results, approximate circuits with RCA structure have 61.2% lesser power where CSA and modified CSA with BEC have 41.2% and 49.1% lesser power in comparison with exact multiplier structure. Then area reduction of approximate circuits using RCA, CSA and modified CSA and BEC in comparison with exact structure are 32.6%, 5.9% and 19.5%.

The speed reduction of approximate circuits using RCA, CSA and modified CSA and BEC in comparison with exact structure are 10.2%, 33.3% and 34.5%. But between these three approximate circuits CSA and modified CSA with BEC will have less delay in comparison with RCA structure with overhead of area and power. But as we have seen modified CSA with BEC, the area penalty by CSA architecture has been reduced by 14.6%.

Multi Vt technique has resulted into change in leakage power and delay. High Vt (HVT) cells have resulted into low leakage but greater delay. Whereas low Vt (LVT) cells does the opposite. Such multi Vt design results have been summarized in the Table 5.3.

Table 5.3 Power and Speed Analysis of Multi Vt Based Designs

Design	**Leakage Power (µW)**	**Delay (ps)**
APM_RCA	0.6526	453.26
APM_CSA	1.1132	376.8
APM_CSA_BEC	0.6351	358.84

As approximate structure has already reduced the power dissipation, by multi Vt design approach mainly focuses on the delay performance. The approximate multiplier design has been divided into two parts namely partial product and final stage adder. From the timing analysis it has been found that final stage adder stage is the main contributor of delay as well as leakage in the design. So to mitigate the issues of low speed, final stage adder has been designed with LVT cells and rest of the design with HVT cells. However, this has resulted into higher leakage power dissipation which in turn increases total power consumption. With multi Vt structure, the speed of the approximate multiplier circuit based on RCA, CSA and modified CSA with BEC has improved by 29.2%, 19.7% and 22.2% with high leakage power.

5.4 ERROR ANALYSIS

Error analysis of the proposed approximate multiplier has been done in accordance with the evaluation of error metrics. As in the real case scenarios, inputs are random in nature. 10^8 random input combinations have been used as a sample data and error metrics has been evaluated.

Automation is considered as the heart of the industrial process. So, whole of the error metrics calculation has been done based on a Tool Command Language (TCL) script. Output after execution of this script contains the details of error metrics that has been given in Figure 5.3. Also the error metric analysis summary has been given below,

```
        ###############
total 100000000 random inputs are sampled
        ###############

        ###############
Mean Error Distance, MED = 3615.29193812
Normalized Error distance, NED = 0.05559849193571703
Mean Related Error distance, MRED = 0.21367200254565882
        ###############
```

Figure 5.3 Error Analysis Script Output

Table 5.4 Error Metric Analysis

Sl. No	Attribute	Value
1	Inputs	10^8
2	ED	Depends on inputs
3	RED	Depends on inputs
4	MED	3615.292
5	NED	5.56×10^{-2}
6	MRED	2.14×10^{-1}

Depending upon the input data sampled, the values of error metrics may vary. But these variations are small.

In our analysis, the sampled data sets have been collected from the Verilog Compiler and Simulator (VCS) and has been put into Comma Separated Value (CSV) format which act as a backup data set that can be used for any debugging purpose. The database generated by the automated script contains input, output and error information as shown in Figure 5.4.

count	a_in	b_in	exact_data	approx_data	error_distance	relative_ed
2	13	141	1833	1789	44	0.024004364
3	101	18	1818	1754	64	0.03520352
4	1	13	13	13	0	0
5	118	61	7198	4094	3104	0.431230897
6	237	140	33180	30716	2464	0.074261603
7	249	198	49302	32470	16832	0.341406028
8	197	170	33490	28618	4872	0.145476262
9	229	119	27251	16383	10868	0.398811053
10	18	143	2574	2558	16	0.006216006
11	242	206	49852	32764	17088	0.342774613
12	232	197	45704	32712	12992	0.284263959
13	92	189	17388	15868	1520	0.087416609
14	45	101	4545	4093	452	0.099449945
17	170	157	26690	32218	5528	0.207118771
19	13	83	1079	1023	56	0.051899907
20	107	213	22791	15839	6952	0.305032688
21	2	174	348	348	0	0
22	29	207	6003	4095	1908	0.317841079
23	35	10	350	350	0	0
24	202	60	12120	8152	3968	0.327392739
25	242	138	33396	32756	640	0.019163972
26	65	216	14040	14040	0	0
27	120	137	16440	16376	64	0.003892944
28	235	182	42770	32254	10516	0.245873276
29	198	174	34452	28668	5784	0.167885754

Figure 5.4 Error CSV Example

5.5 POWER AWARE ANALYSIS

The approximate multiplier design is a less complex design. So, in order to elaborate each feature of power intent by UPF, a SIP architecture has been taken into consideration. In this architecture, we have used both the approximate and the exact multiplier along with some other functional block. This multiplier based SIP has been analyzed where both the multiplier are switchable blocks with different operating voltage. Synthesized approximate multiplier inside of the SIP along with UPF elements such as isolation and level shifter cells has shown in Figure 5.5.

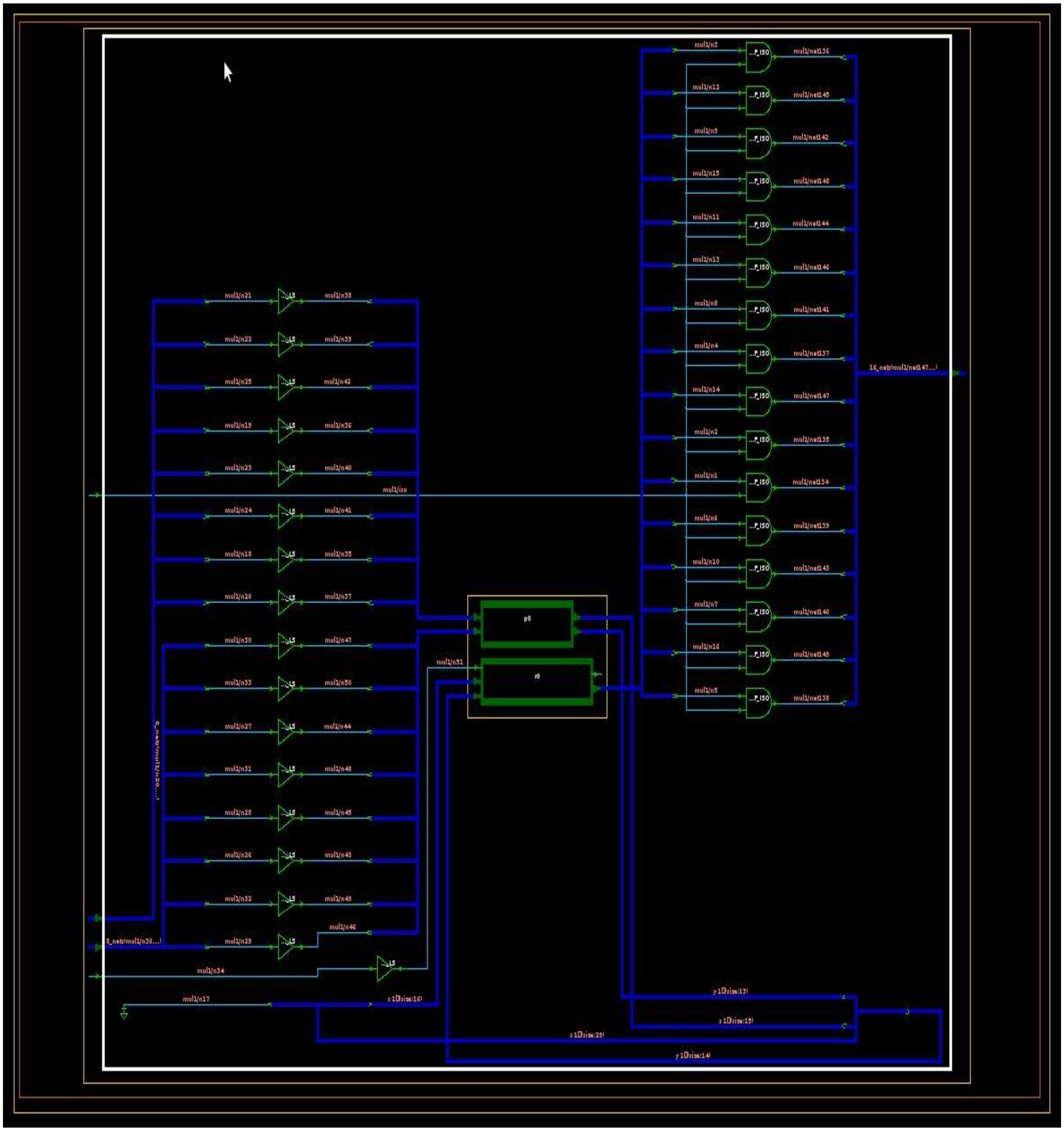


Figure 5.5 Synthesized Approximate Multiplier within SIP with UPF Elements

Power and area have been analyzed and summarized for the SIP in the table 5.5, where results are compiled on Design compiler using standard libraries with temperature of 25ºC at a typical process corner.

Table 5.5 Summarized Analysis Report of SIP

Design Name	Voltage (V)	Area (μm^2)	Internal Power (mW)	Switching Power (mW)	Leakage Power (μW)	Total Dynamic Power (mW)	Total Power (mW)
SIP without UPF	1.05	225.0083	1.3019	0.9011	3.6906	2.2029	2.2066
SIP without UPF	0.85	212.8291	0.6651	0.3678	2.2645	1.0328	1.0351
SIP with UPF	1.05 & 0.85	355.6451	1.0375	0.6292	4.3262	1.6667	1.6711

In the SIP design, two level of analysis have been done. First one without any power intent information and the second one with the power intent specification. It has been noted from the Table 5.5 that reducing voltage will reduce the switching power and also the total power. But a low voltage will result in a higher delay in the circuit. For that reason, multi voltage based designed are the best choice for having the best performance. There is increase in area and leakage power of the design due to the inclusion of the UPF elements for proper functionality of the power aware design. It has been noted that the SIP operated with combination of 1.05 V and 0.85 V can have a power savings of almost 26% with an area overhead of 58% in comparison to the design when operated at 1.05 Volt only.

Synthesized UPF diagram of the design and power state table used in UPF has been given in Figure 5.6.

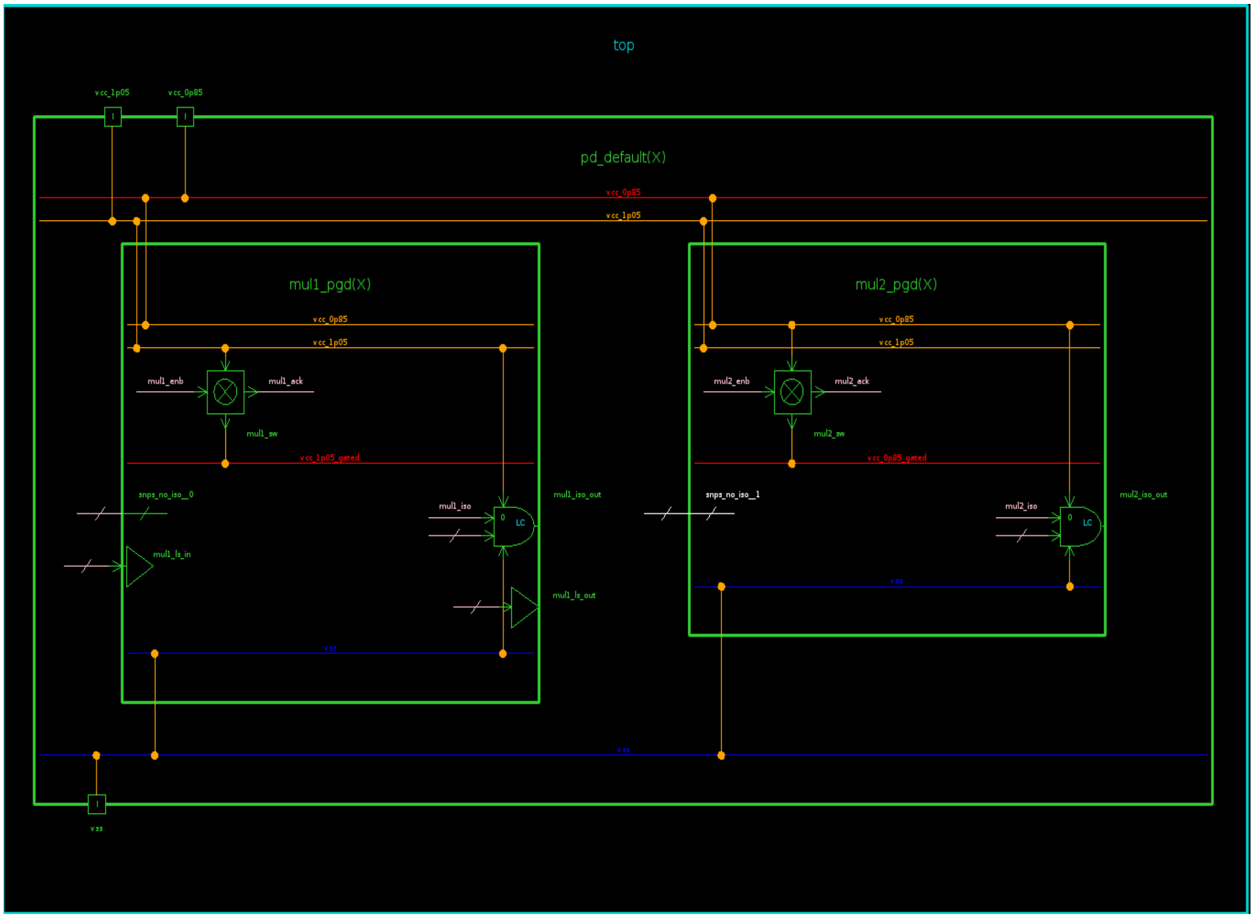
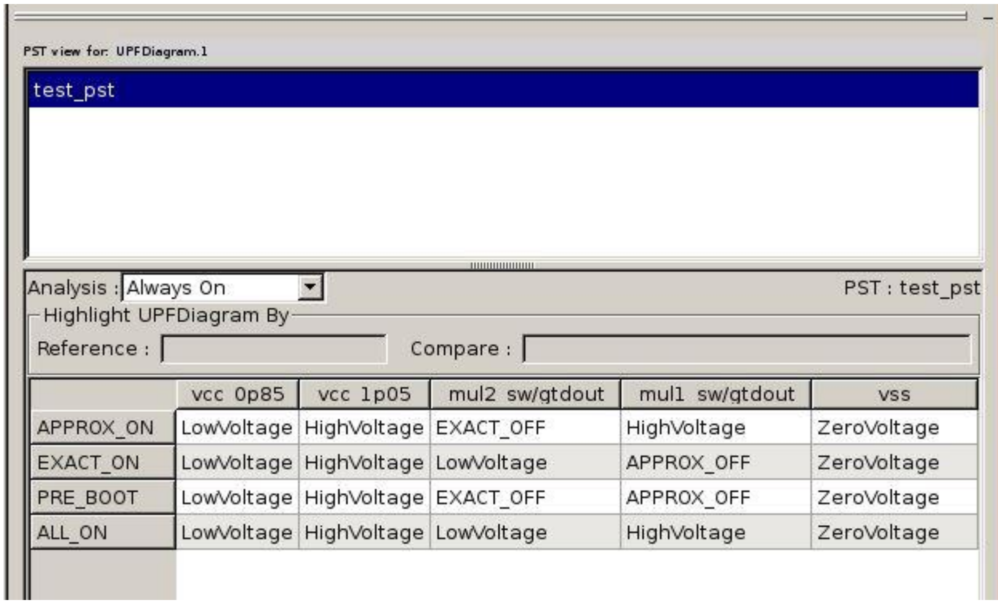


Figure 5.6 Synthesized UPF Diagram

By analyzing the UPF diagram, position of the UPF elements had to be decided in the design. There are three domains that can be seen as pd_default, mul1_pgd and mul2_pgd. Mul1_pgd and mul2_pgd contain only mult1 (approximate multiplier) and mult2 (exact multiplier) as their elements. pd_default is the top level power domain that contains these two domains along with all other elements of the designed SIP. According to the given UPF description, the power switch, level shifter, and isolation strategies have been placed. Their control inputs, outputs and supply connection can also be seen in the synthesized diagram. Power switch is an indication of mul1_pgd and mul2_pgd as switchable domains. Isolation strategies are indication of interaction of switchable domain with always on domain. Level shifter has been provided to interact mul1_pgd elements with other domain elements as they operate at higher voltage than others. The power state table gives an insight of power management scenarios that can be seen in the Figure 5.7.



	vcc 0p85	vcc 1p05	mul2 sw/gtdout	mul1 sw/gtdout	vss
APPROX_ON	LowVoltage	HighVoltage	EXACT_OFF	HighVoltage	ZeroVoltage
EXACT_ON	LowVoltage	HighVoltage	LowVoltage	APPROX_OFF	ZeroVoltage
PRE_BOOT	LowVoltage	HighVoltage	EXACT_OFF	APPROX_OFF	ZeroVoltage
ALL_ON	LowVoltage	HighVoltage	LowVoltage	HighVoltage	ZeroVoltage

Figure 5.7 Power State Table

The projected power numbers in Figure 5.8 to 5.11 are only library predefined power numbers with always on condition. Means this will be the power projection of the design when every power domain is active. But as being a power aware design UPF gives us flexibility to derive power based on the power state table. In a normal real time behavior this states are random in nature but for each state we can define the power by power state table based power analysis. Such analysis result of our system is shown in the below Figures 5.8 to 5.11.

```
================================================================================
Power Report For PST Group test_pst State ALL_ON
================================================================================


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (      %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.449e-04    0.0000    0.0000 2.449e-04 (21.91%)  i
register                6.476e-05 2.048e-05 2.748e-07 8.551e-05 ( 7.65%)
combinational           4.540e-04 3.313e-04 2.043e-06 7.873e-04 (70.44%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 3.518e-04   (31.47%)
  Cell Internal Power  = 7.636e-04   (68.32%)
  Cell Leakage Power   = 2.318e-06   ( 0.21%)
                         ---------
Total Power            = 1.118e-03  (100.00%)
```

Figure 5.8 Power Analysis Report Based on Power State ALL_ON

```
================================================================================
Power Report For PST Group test_pst State EXACT_ON
================================================================================


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.449e-04    0.0000    0.0000 2.449e-04 (25.27%)  i
register                6.476e-05 2.048e-05 2.748e-07 8.551e-05 ( 8.82%)
combinational           3.789e-04 2.584e-04 1.537e-06 6.389e-04 (65.91%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.789e-04   (28.77%)
  Cell Internal Power  = 6.886e-04   (71.04%)
  Cell Leakage Power   = 1.812e-06   ( 0.19%)
                         ---------
Total Power            = 9.693e-04  (100.00%)
```

Figure 5.9 Power Analysis Report Based on Power State EXACT_ON

```
================================================================================
Power Report For PST Group test_pst State APPROX_ON
================================================================================


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.449e-04    0.0000    0.0000 2.449e-04 (29.21%)  i
register                6.476e-05 2.048e-05 2.748e-07 8.551e-05 (10.20%)
combinational           3.090e-04 1.973e-04 1.569e-06 5.079e-04 (60.58%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 2.178e-04   (25.98%)
  Cell Internal Power  = 6.187e-04   (73.80%)
  Cell Leakage Power   = 1.844e-06   ( 0.22%)
                         ---------
Total Power            = 8.383e-04  (100.00%)
```

Figure 5.10 Power Analysis Report Based on Power State APPROX_ON

```
================================================================================
Power Report For PST Group test_pst State PRE_BOOT
================================================================================


  Attributes
  ----------
      i  -  Including register clock pin internal power
      u  -  User defined power group

                        Internal  Switching  Leakage    Total
Power Group             Power     Power      Power      Power   (     %)  Attrs
--------------------------------------------------------------------------------
clock_network           2.449e-04    0.0000    0.0000 2.449e-04 (35.50%)  i
register                6.476e-05 2.048e-05 2.748e-07 8.551e-05 (12.40%)
combinational           2.340e-04 1.244e-04 1.063e-06 3.595e-04 (52.10%)
sequential                 0.0000    0.0000    0.0000    0.0000 ( 0.00%)
memory                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
io_pad                     0.0000    0.0000    0.0000    0.0000 ( 0.00%)
black_box                  0.0000    0.0000    0.0000    0.0000 ( 0.00%)

  Net Switching Power  = 1.449e-04   (21.00%)
  Cell Internal Power  = 5.436e-04   (78.80%)
  Cell Leakage Power   = 1.338e-06   ( 0.19%)
                         ---------
Total Power            = 6.899e-04  (100.00%)
```

Figure 5.11 Power Analysis Report Based on Power State PRE_BOOT

As discussed earlier, these power states have the possible combination of modes of operation of the domains. These power state analysis will reflect power numbers according to the power state table. PrimeTime PX has been used for power state analysis.

Power scenario at each state analysis totally depends on the number of elements active at that time. The different power states corresponds to different elements being active, power state analysis will give the respective power. In ALL_ON every element being on, power is highest. Whereas in APPROX_ON state, exact multiplier block and in EXACT_ON state approximate multiplier block has been switched off. In PRE_BOOT state, both the multiplier blocks are off as shown in Figure 5.7. As different elements have been powered on, the power in EXACT_ON, APPROX_ON and PRE_BOOT state is 13.3%, 25.1% and 39.35% lesser than ALL_ON state. In real case scenarios, depending on the simulation vectors, these states can appear randomly and total power depends on the accumulation of all those states. Power state based analysis gives a complete overview of actual power aware scenarios.

5.6 POWER INTENT VERIFICATION

Power aware verification has been done to check UPF compatibility with the design. Different tools used in VLSI design flow will produce RTL, gate level netlist, physical netlist where UPF has been modified. Power intent verification process has statically check the compatibility of the UPF and the design for each stage. Figure 5.12 have shown the error in the UPF used in SIP due to wrong implementation of supply net, isolation and level shifter. Verification process will produce two part results. First part has shown the overview of the errors, warnings, information generation based on the checks done by verification part. Where as in the second part detailed description of these errors, warnings, information have been elaborated. Figure 5.12 depicts the summarized error during UPF verification.

```
------------------------------------------------------------------------------
Management Summary
------------------------------------------------------------------------------
Stage  Family              Errors   Warnings     Infos
-----  ----------------  ---------  ---------  ---------
UPF    Isolation                16         16          0
UPF    UpfConsistency           68          1          0
-----  ----------------  ---------  ---------  ---------
Total                           84         17          0


------------------------------------------------------------------------------
Tree Summary
------------------------------------------------------------------------------
Severity  Stage  Tag                       Count
--------  -----  -----------------------  -----
error     UPF    ISO_STRATEGY_MISSING        16
error     UPF    UPF_CROSSOVER_NOSTATE       66
error     UPF    UPF_SUPPLY_NOSTATE           2
warning   UPF    ISO_STRATEGY_REDUND         16
warning   UPF    UPF_SUPPLY_NOLOAD            1
--------  -----  -----------------------  -----
Total                                       101
```

Figure 5.12 Summarized Power Verification Report

```
Tag                     : ISO_STRATEGY_MISSING
Description             : Isolation required on crossing from [Source] to [Sink], but strategy missing
Violation               : LP:73
Source
  PinName               : mul2/r0/rca2/fa3/h2/sum
Sink                    : mul2_op[7]
SegmentSourceDomain     : mul2_pgd
SegmentSinkDomain       : pd_default
LogicSource
  PinName               : mul2/r0/rca2/fa3/h2/sum
LogicSink               : mul2_op[7]
DomainSource            : mul2/product[7]
DomainSink              : mul2/product[7]
SourceInfo
  PowerNet
    NetName             : vcc_0p85_gated
    NetType             : UPF
  PowerMethod           : FROM_UPF_POWER_DOMAIN
  GroundNet
    NetName             : vss
    NetType             : UPF
  GroundMethod          : FROM_UPF_POWER_DOMAIN
SinkInfo
  PowerNet
    NetName             : vcc_0p85
    NetType             : UPF
  PowerMethod           : FROM_UPF_POWER_DOMAIN
  GroundNet
    NetName             : vss
    NetType             : UPF
  GroundMethod          : FROM_UPF_POWER_DOMAIN
States
  State                 : test_pst/APPROX_ON
```

Figure 5.13 Detailed report of Isolation Strategy Missing Error

In Figure 5.13 one of the summarized error named as ISO_STRATEGY_MISSING has been elaborated. The error in the UPF described the requirement of isolation because of connection has been made between a gated and always on domain, but isolation is missing in the UPF. For proper implementation of power aware design, power verification report should be error free. Some warnings can be neglected depends upon the warning and its effect to the further stages of the design flow.

5.7 IMAGE PROCESSING RESULT

The application of designed approximate multiplier has been justified by using it in Gaussian filter. Predefined Gaussian mask value has been multiplied with image data for smoothening purpose. Quality of this filtering output has been measured in terms of their PSNR values. Image processing outputs has been shown below in Figure 5.14 to 5.16.

Image1

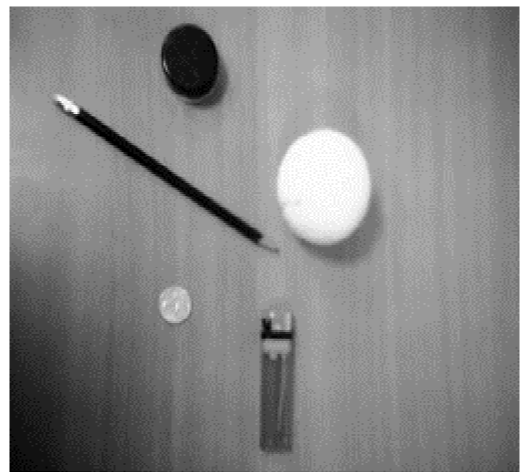


Image2

Figure 5.14Original Images

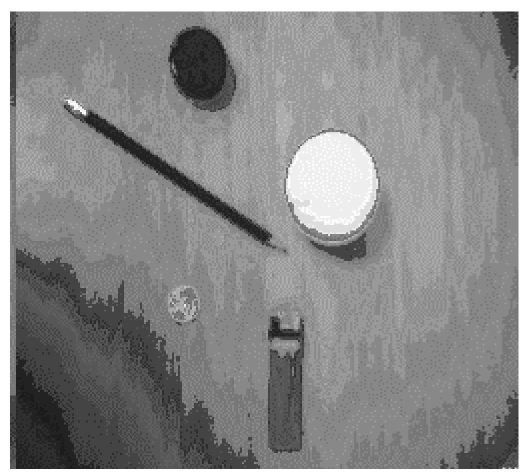


Figure 5.15 Filtered Images Using Exact Multiplier

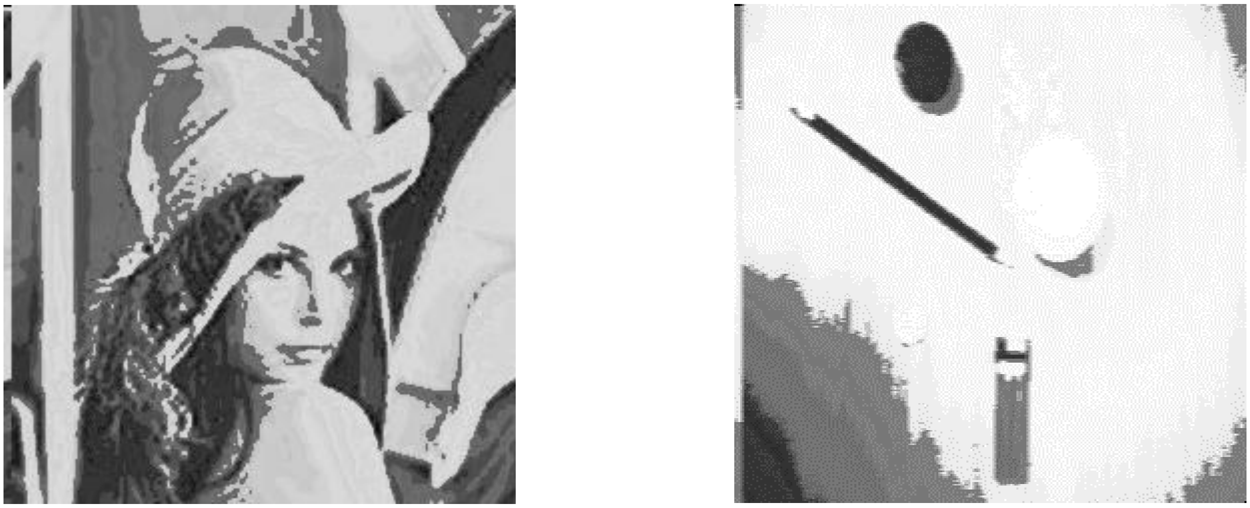


Figure 5.16 Filtered Images Using Approximate Multiplier

For image process using Gaussian filter, only gray scale images has been considered. Merit of the processed images has been given below in Table 5.6 in terms of PSNR values. Higher PSNR value has results into a higher image quality.

Table 5.6 PSNR Values of Original and Processed Images

Image	**PSNR of noisy image (dB)**	**PSNR of filtered image using exact multiplier (dB)**	**PSNR of filtered image using approximate multiplier (dB)**
Image1	31.4426	56.1082	53.9699
Image2	32.5482	56.3420	54.6801

The PSNR values has been improved by the filtering operation as we can see in the table 5.6. As per the the quality analysis for image1 and image2, PSNR values has been deteriorated by only 4% and 3% as compared to the PSNR values obtained using exact multiplier.

5.8 ROLLUP TEMPLATE

Power template has been designed to put analysis results in a specified format after every design step. There have been a lot of design analysis reports which must be sort out in an efficient manner. As discussed in the chapter 4, the proposed template will take reports generated by power estimation tools as collaterals. An overview of generated power template of the SIP design is shown in the Figure 5.17 and 5.18. This power template has shown rail based analysis report using a TCL script to enable automation. Specific fields has been populated with specific data for the designed SIP.

A	B	C	D	E	F	G	H	I	J	K	L	N
IPName	IPMODULE	IPType	ProcessCo	Temperature	TestFrequency(MHz)	VoltageRa	Voltage_v	StaticPower_W	Switchingpower_W	LeakagePower_W	DynamicPower_w	TotalPower_W
top	top	SIP	tttt	25c	11111100	vcc_0p85	0.85	0.000642658	0.000248433	1.69E-06	0.000891092	0.000892793
top	top	SIP	tttt	25c	11111100	vcc_1p05	1.05	0.000133986	0.000111446	2.00E-02	0.000245432	0.000246151

Figure 5.17 Power Rollup Report

O	P	Q	R	S	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF	AG	AH
Opvar1	Opvar1_Val	Opvar2	Opvar2_Val	Opvar3	Opvar3_Val	Opvar4	Opvar4_Va	Opvar5	Opvar5_Val	Opvar6	Opvar6_Val	Opvar7	Opvar7_Value	Opvar8	Opvar8_Val	Opvar9	Opvar9_Val	Opvar10	Opvar10_Val
Cdyn(pf)	111.00119	clk_main	clk	freq_main(Mhz)	11111100	clk_fast	clk	freq_fast(Mhz)	11111100	cell	lvt:hvt	prcnt	15.50:40.17	TYPE	NA:std_cell	LEAKAGE(mW)	0.000:0.002	DYNTOTAL	0.000:0.891
Cdyn(pf)	200.35285	clk_main	clk	freq_main(Mhz)	11111100	clk_fast	clk	freq_fast(Mhz)	11111100	cell	lvt:hvt	prcnt	12.268:30.008	TYPE	NA:std_cell	LEAKAGE(mW)	0.000:0.001	DYNTOTAL	0.000:0.245

Figure 5.18 Continuation of Rollup Report

The opvar field in the template has considered as dynamic field which can be changed as per requirement. Generation of this template has been taken still existing reports so hogging the power estimation tool can never happen. Some of the basic features that have been added as opvar field which worth mentioning shown below,

- Load capacitance (Cdyn).
- Test frequency.
- Cell based power.
- Vt type cell usage.

Upon unavailability of the required reports which have been used as collaterals in rollup process error flags has raised. This will help the designer to debug which report has been missing.

5.8.1 Power checker algorithm

During the power template generation a power checker algorithm has been applied to check the standard cells used in the design should not have null power annotation for leakage and internal power. This Algorithm has only checked for the cells which comes under standard cells category. Output of this algorithm has been applied in power template generation step and produced output for designed SIP in Figure 5.19.

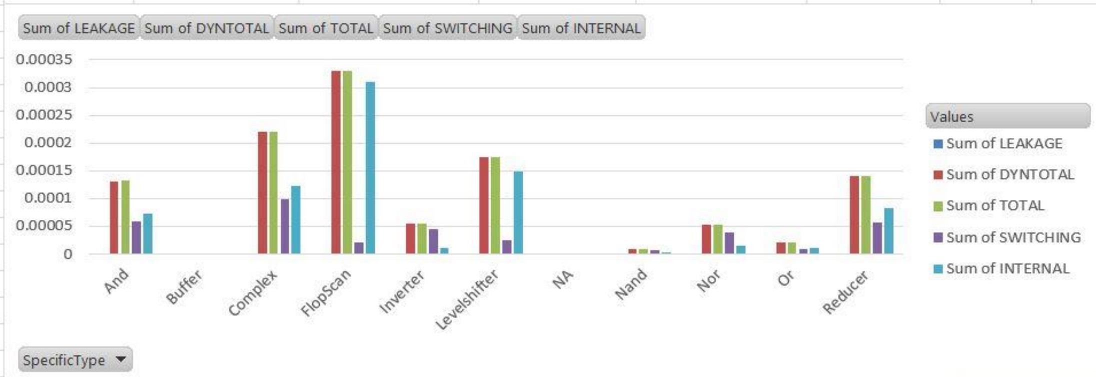
A	B	C	D	E	F	G
CellName	Rule1	Internal_Power_Value	Rule1_Stat	Rule2	Leakage_Power_Value	Rule2_Status
orn002ah1n02x5	Internal_Power_Check	2.682E-07	pass	Leakage_Power_Check	3.045E-09	Pass
orn002ah1n02x6	Internal_Power_Check	1.3184E-06	pass	Leakage_Power_Check	6.685E-09	Pass
orn002ah1n02x7	Internal_Power_Check	5.999E-08	pass	Leakage_Power_Check	3.235E-09	Pass
orn002ah1n02x8	Internal_Power_Check	1.54785E-06	pass	Leakage_Power_Check	4.9451E-09	Pass
orn002ah1n02x9	Internal_Power_Check	0.000021447	pass	Leakage_Power_Check	1.08545E-07	Pass
orn002ah1n02x10	Internal_Power_Check	0.000066552	pass	Leakage_Power_Check	2.9979E-07	Pass
orn002ah1n02x11	Internal_Power_Check	1.6642E-07	pass	Leakage_Power_Check	4.167E-09	Pass
orn002ah1n02x12	Internal_Power_Check	1.8467E-06	pass	Leakage_Power_Check	6.758E-09	Pass
orn002ah1n02x13	Internal_Power_Check	0.000007351	pass	Leakage_Power_Check	1.8275E-08	Pass
orn002ah1n02x14	Internal_Power_Check	8.916E-07	pass	Leakage_Power_Check	2.894E-09	Pass
orn002ah1n02x15	Internal_Power_Check	7.548E-07	pass	Leakage_Power_Check	2.964E-09	Pass
orn002ah1n02x16	Internal_Power_Check	9.985E-07	pass	Leakage_Power_Check	4.7745E-09	Pass
orn002ah1n02x17	Internal_Power_Check	6.278E-07	pass	Leakage_Power_Check	3.039E-09	Pass
orn002ah1n02x18	Internal_Power_Check	2.778E-07	pass	Leakage_Power_Check	3.043E-09	Pass
orn002ah1n02x19	Internal_Power_Check	1.1347E-06	pass	Leakage_Power_Check	6.528E-09	Pass
orn002ah1n02x20	Internal_Power_Check	1.30112E-07	pass	Leakage_Power_Check	2.99E-09	Pass
orn002ah1n02x21	Internal_Power_Check	6.215E-08	pass	Leakage_Power_Check	9.589E-10	Pass
orn002ah1n02x22	Internal_Power_Check	0.000003188	pass	Leakage_Power_Check	6.359E-09	Pass
orn002ah1n02x23	Internal_Power_Check	1.0385E-06	pass	Leakage_Power_Check	2.761E-09	Pass
orn002ah1n02x24	Internal_Power_Check	1.9692E-06	pass	Leakage_Power_Check	6.487E-09	Pass
orn002ah1n02x25	Internal_Power_Check	2.561E-07	pass	Leakage_Power_Check	3.088E-09	Pass
orn002ah1n02x26	Internal_Power_Check	0.000000652	pass	Leakage_Power_Check	4.412E-09	Pass
orn002ah1n02x27	Internal_Power_Check	5.904E-07	pass	Leakage_Power_Check	2.992E-09	Pass
orn002ah1n02x28	Internal_Power_Check	1.1908E-06	pass	Leakage_Power_Check	2.937E-09	Pass
orn002ah1n02x29	Internal_Power_Check	3.469E-07	pass	Leakage_Power_Check	1.577E-09	Pass
orn002ah1n02x30	Internal_Power_Check	0.000001231	pass	Leakage_Power_Check	3.215E-09	Pass
orn002ah1n02x31	Internal_Power_Check	0.000002647	pass	Leakage_Power_Check	6.212E-09	Pass
orn002ah1n02x32	Internal_Power_Check	9.207E-08	pass	Leakage_Power_Check	8.955E-10	Pass
orn002ah1n02x33	Internal_Power_Check	4.225E-07	pass	Leakage_Power_Check	1.862E-09	Pass

Figure 5.19 Power Checker Algorithm Output

Pass condition have been considered those cases where internal and leakage power annotated with some value. Whereas fail conditions has been considered cases where these powers annotate as 0 or NA.

5.9 INDICATOR OUTPUTS

Indicator outputs has been consists of charts and tables which will published as dashboard on publishing platform. These outputs will provide the insights of power obtained at different analysis stage. Below Figure 5.20 depicts published chart and table for different used cell based power analysis of the designed SIP in PowerPivot and publishing platform, where power rail value has been taken as slicer value.



Row Labels	Sum of INTERNAL	Sum of SWITCHING	Sum of LEAKAGE	Sum of DYNTOTAL	Sum of TOTAL
And	0.000072062	5.95182E-05	2.58891E-07	0.000131575	0.000131775
Buffer	0.000000211	0.000000953	3.51E-09	0.00000116	0.00000117
Complex	0.000121962	9.82156E-05	5.5239E-07	0.000220135	0.00022064
FlopScan	0.00030995	0.0000206	2.745E-07	0.000330422	0.00033076
Inverter	0.000011214	0.000044209	1.05662E-07	0.000055443	0.00005558
Levelshifter	0.00014837	0.0000253	7.2538E-07	0.00017362	0.00017445
NA	0	0	0	0	0
Nand	2.3642E-06	6.2021E-06	2.6012E-08	0.00000856	0.000008585
Nor	0.00001576	0.000038039	7.3382E-08	0.000053769	0.00005391
Or	1.15615E-05	1.00436E-05	8.655E-08	0.000021598	0.000021698
Reducer	0.00008337	0.00005677	3.017E-07	0.00014008	0.00014041
Grand Total	**0.000776824**	**0.000359851**	**2.40798E-06**	**0.001136362**	**0.001138978**

PRIM_RAIL

vcc_0p85

vcc_1p05

Figure 5.20 PowerPivot Chart and Table Worksheet of Cell Based Power Report

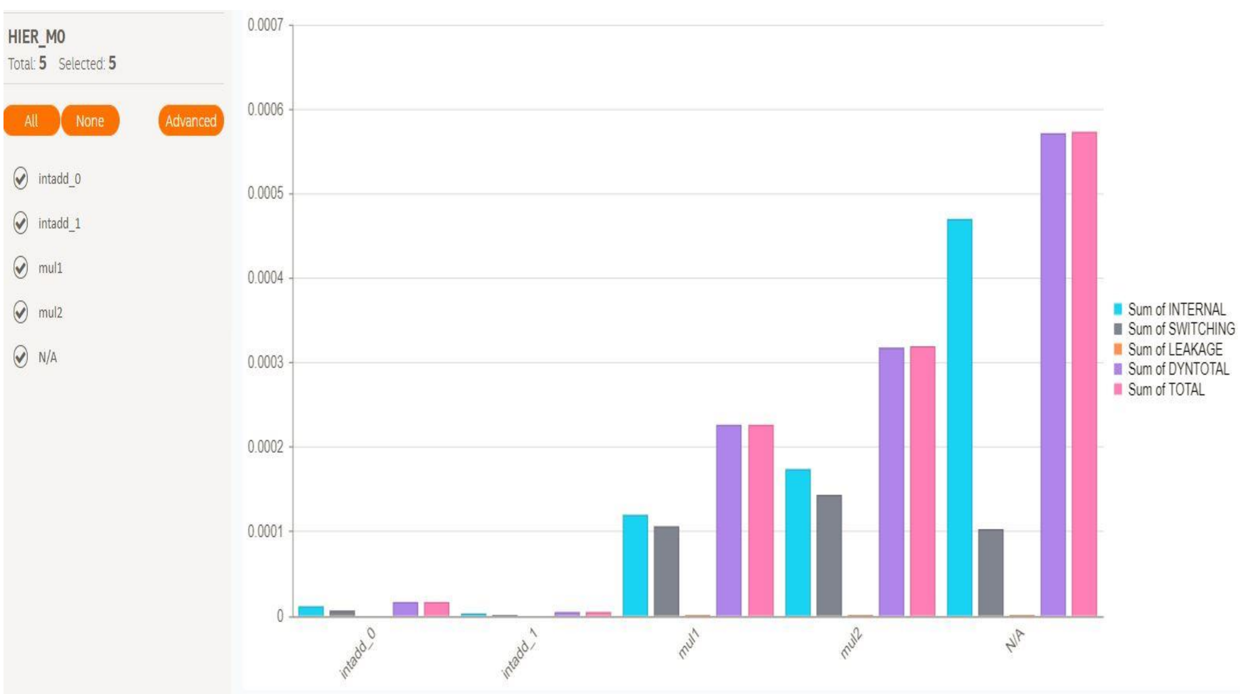
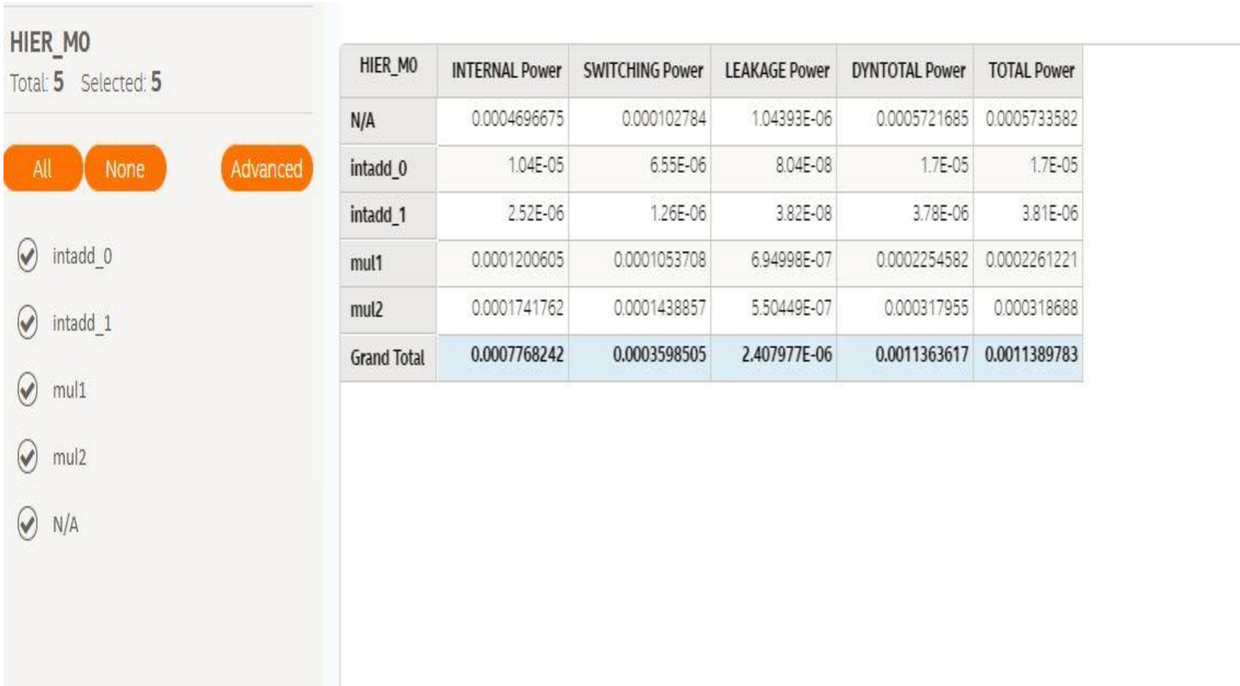


Figure 5.21 Published Power Analysis Chart at Top-most Hierarchy



HIER_M0	INTERNAL Power	SWITCHING Power	LEAKAGE Power	DYNTOTAL Power	TOTAL Power
N/A	0.0004696675	0.000102784	1.04393E-06	0.0005721685	0.0005733582
intadd_0	1.04E-05	6.55E-06	8.04E-08	1.7E-05	1.7E-05
intadd_1	2.52E-06	1.26E-06	3.82E-08	3.78E-06	3.81E-06
mul1	0.0001200605	0.0001053708	6.94998E-07	0.0002254582	0.0002261221
mul2	0.0001741762	0.0001438857	5.50449E-07	0.000317955	0.000318688
Grand Total	0.0007768242	0.0003598505	2.407977E-06	0.0011363617	0.0011389783

Figure 5.22 Published Power Analysis Table of Top-most Hierarchy

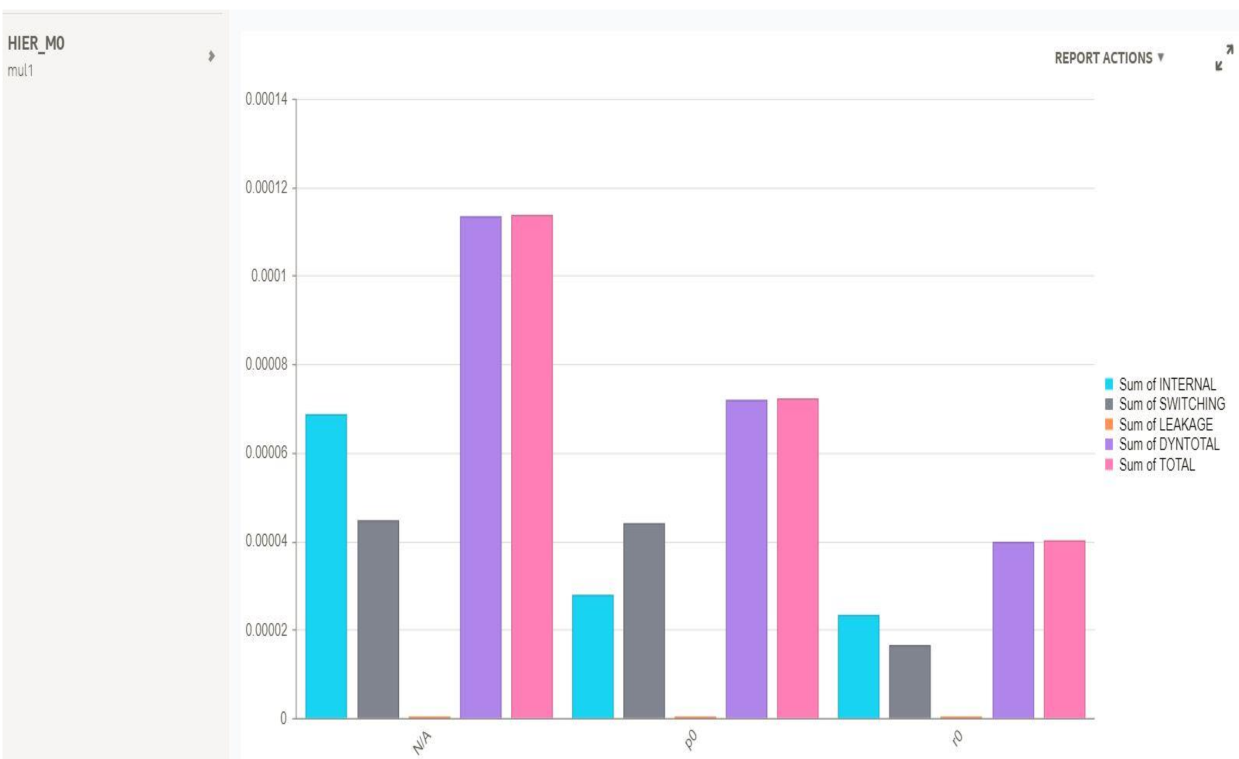
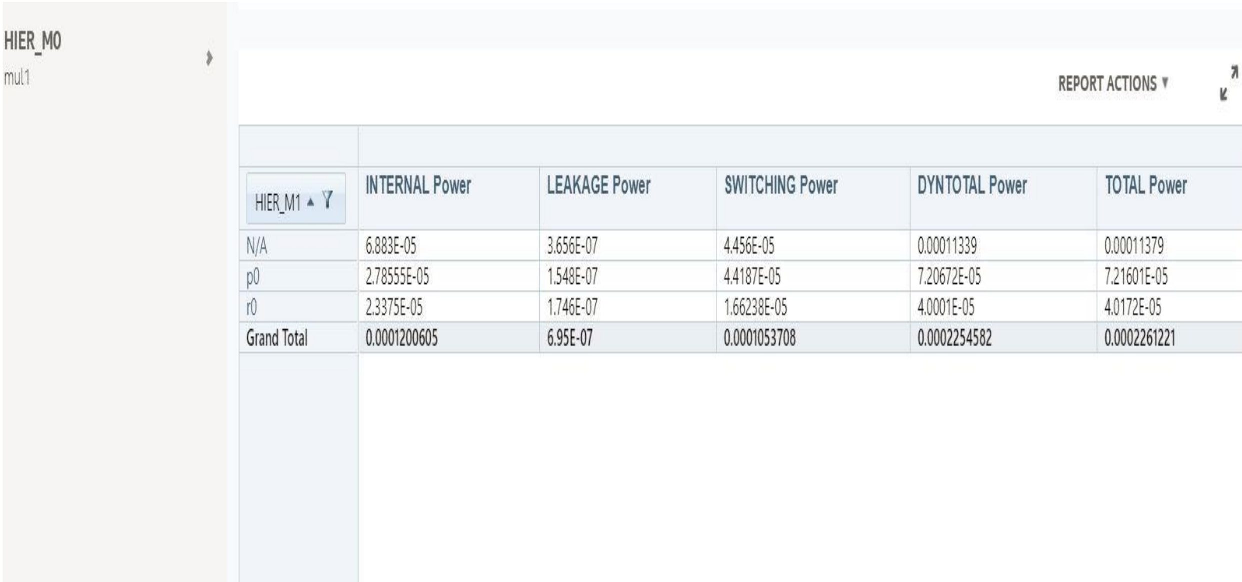


Figure 5.23 Published Power Analysis Chart of One Level Drill Down for Mult1



HIER_M0
mul1

REPORT ACTIONS

HIER_M1	INTERNAL Power	LEAKAGE Power	SWITCHING Power	DYNTOTAL Power	TOTAL Power
N/A	6.883E-05	3.656E-07	4.456E-05	0.00011339	0.00011379
p0	2.78555E-05	1.548E-07	4.4187E-05	7.20672E-05	7.21601E-05
r0	2.3375E-05	1.746E-07	1.66238E-05	4.0001E-05	4.0172E-05
Grand Total	0.0001200605	6.95E-07	0.0001053708	0.0002254582	0.0002261221

Figure 5.24 Published Power Analysis Table of One Level Drill Down for Mult1

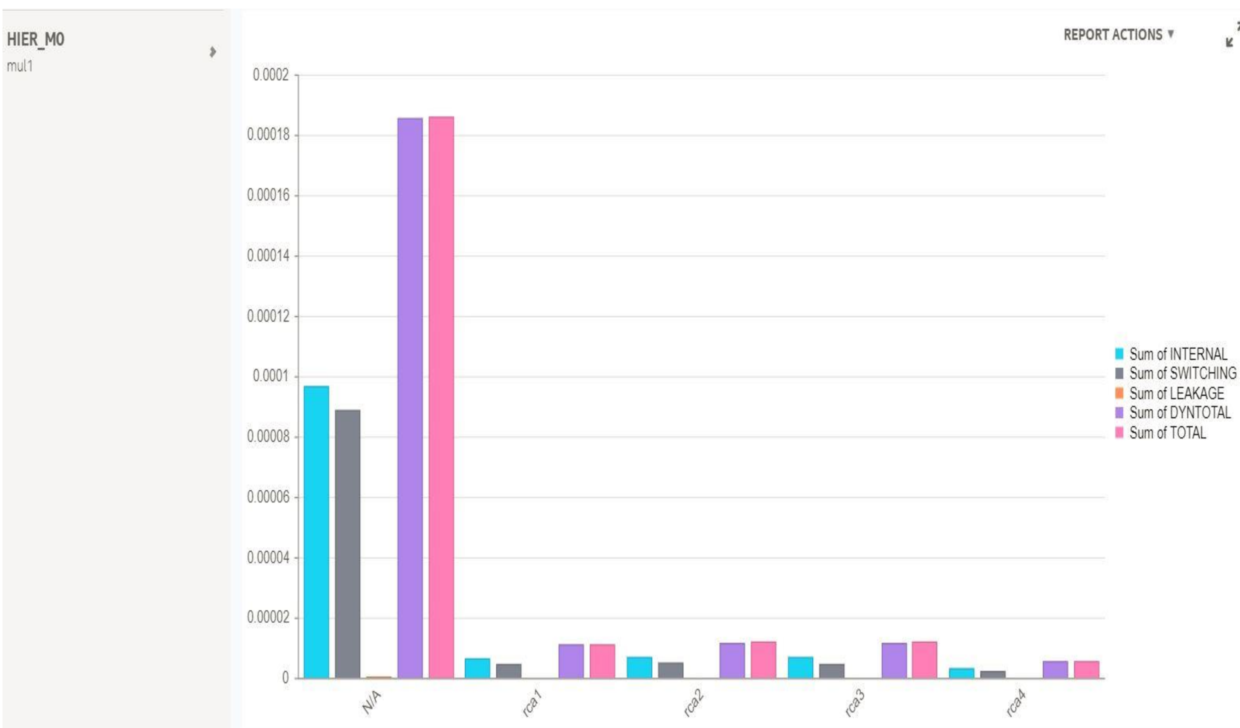


Figure 5.25 Published Power Analysis Chart for Two Level Drill Down for Mult1

HIER_M0

mul1

HIER_M2	Sum of INTERNAL	Sum of SWITCHING	Sum of LEAKAGE	Sum of DYNTOTAL	Sum of TOTAL
N/A	9.66855E-05	8.8747E-05	5.20388E-07	0.0001854572	0.0001859501
rca1	6.275E-06	4.703E-06	4.175E-08	1.0979E-05	1.1011E-05
rca2	6.809E-06	4.948E-06	5.153E-08	1.176E-05	1.1825E-05
rca3	6.996E-06	4.775E-06	5.182E-08	1.1767E-05	1.1814E-05
rca4	3.295E-06	2.1978E-06	2.951E-08	5.495E-06	5.522E-06
Grand Total	**0.0001200605**	**0.0001053708**	**6.94998E-07**	**0.0002254582**	**0.0002261221**

Figure 5.26 Published Power Analysis Table for Two Level Drill Down for Mult1

Figure 5.23 to 5.26 has shown drill down feature of publishing platform. This feature has been very effective in terms of module based power analysis and debug. Figure 5.21 and 5.22 has shown power analysis results of whole SIP design containing every architecture in chart and tabular format. For drill down feature approximate multiplier (mul1) has been selected. Figure 5.23 and 5.24 has shown the one level drilled power analysis chart and table of approximate multiplier structure with elements p0, r0, NA. Figure 5.25 and 5.26 has shown power scenario in chart and tabular format for approximate circuit for r0 within approximate multiplier.

Here N/A refers to flat designs at the specified hierarchical level i.e. no module based design structure.

CHAPTER 6

CONCLUSION AND SCOPE OF FUTURE WORKS

6.1 CHALLENGES IN THE PROPOSED METHODOLOGY

Designing a new architecture which would handle versatile design elements requires a lot of background work before it can be fixed. Knowledge about the nature of design and tool are two important aspects of it. Extracting the common aspects of the design and imparting those into a single structure is a tedious task. Also effective automotive framework should not require much resources.

Some of the issues that we encounter implementing the design and analysis are,

- Efficient approximate sub designs for less power consumption and less error.
- UPF compatibility with different tools.
- Deciding key parameters for rollup and indicator system.
- Excel data will not handle large chunks of data for that we use database.
- Automated process validation for collateral checks.
- Interconnection of automated scripts with already existing scripts for existing tool flow.

6.1.1 Benefits of the proposed methodology

- Less error based approximate multiplier design.
- Low power and high speed implementation of approximate multiplier design.
- Power aware design implementation.
- Fast turnaround time.
- One framework for handling the design flow.
- Generic power template for any type of design.
- Automatic collection of inputs for power characterization
- Automatically updated one time setup indicator system.
- Easy power calculation and correlation using excel.
- Anomaly of power number can be easily shown.
- Backup of every possible set of implementation data.

6.1.2 Scope for improvement

- Approximation of final stage adder is still open.
- Error correctional system based on threshold error value.
- Upgradation of UPF standards.

- Correlation between RTL and synthesis stage.
- Flattening of csv file is required.
- Runtime reduction for analysis, verification and publish.
- Auto updating results require time improvement.
- Generated power template publication in publishing platform.

6.2 CONCLUSION

In this work, an approximate multiplier has been implemented with three different adders namely RCA, CSA and CSA with BEC. Out of all these implementations CSA with BEC gives the optimum performance with 49.1%, 34.5% reduction in power and speed in comparison to the exact multiplier. An error analysis has also been performed using 10^8 random test vectors.

A Gaussian filter has been designed using this approximate multiplier. It processes two images with 3 and 4% deviations in PSNR in comparison to exact multiplier.

UPF implementation of this design with a SIP structure has been done to make power aware system. Two voltage domains operating on 0.85V and 1.05V have been considered. This resulted into 26% power reduction than the domain operated only at 1.05V.

6.3 SCOPE OF FUTURE WORK

Different adder options can be explored further to reduce delay and power. Also approximation of final stage adder along with other approximation circuits can be another area of study.

Coming to the part of power intent, additional features provided by higher standards of UPF can be explored further. Also as UPF will follow the predefined constructs for their description, excel sheet to UPF conversion automation will be a future advancement.

Coming to the power rollup and indicator part, a pre stage power estimation has been planned. It will take the database of previously used cells or IPs and precompute the power before even RTL has been designed. This approach if completed and successfully implemented, will be very efficient for rough power estimation at very early stage of design.

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